# Product Change Notification: SYST-11KCQN749

## Date:

14-Apr-2025

## Product Category:

32-Bit Microcontrollers

## Notification Subject:

SAM D21/DA1 Family Silicon Errata and Data Sheet Clarification

## Affected CPNs:

**SYST-11KCQN749_Affected_CPN_04142025.pdf**
**SYST-11KCQN749_Affected_CPN_04142025.csv**

## Notification Text:

SYST-11KCQN749

Microchip has released a new Document for the SAM D21/DA1 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at **SAM D21/DA1 Family Silicon Errata and Data Sheet Clarification**.

**Notification Status:** Final

**Description of Change:**
Revision M Document
Updated the verbiage for Device errata 1.5.9 One Time Programmable Lock to read Program and Debug Interface Disable.

**Impacts to Data Sheet:** Refer to **DS40001882**.

**Reason for Change:** To improve productivity.

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 14 Apr 2025

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

## Attachments:

### SAM D21/DA1 Family Silicon Errata and Data Sheet Clarification

Please contact your local **Microchip sales office** with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

ATSAMD21J17D-MMZ

ATSAMD21J17D-MMF

ATSAMD21E17D-MZ

ATSAMD21E17D-MZVAO

ATSAMD21E17L-MF

ATSAMD21E17D-MF

ATSAMD21G17D-MF

ATSAMD21G17L-MF

ATSAMD21E17L-AF

ATSAMD21E17D-AF

ATSAMD21E17D-AZ

ATSAMD21E17D-AZVAO

ATSAMD21J17D-MF

ATSAMD21G17D-MZ

ATSAMD21J17D-MZ

ATSAMD21J17D-MZVAO

ATSAMD21J17D-AF

ATSAMD21J17D-AZ

ATSAMD21J17D-AZV08

ATSAMD21J17D-AZVAO

ATSAMD21G17D-AF

ATSAMD21G17D-AZ

ATSAMD21G17D-AZVAO

ATSAMD21J17D-CU

ATSAMD21J17D-MMU

ATSAMD21E17D-MU

ATSAMD21G17D-MU

ATSAMD21G17L-MU

ATSAMD21E17D-AU

ATSAMD21J17D-MU

ATSAMD21J17D-AU

ATSAMD21G17D-AU

ATSAMD21E17L-MN

ATSAMD21G17L-MN

ATSAMD21E17L-MNT

ATSAMD21G17L-MNT

ATSAMD21J17D-CUT

ATSAMD21J17D-MMUT

ATSAMD21E17D-MUT

ATSAMD21G17D-MUT

ATSAMD21G17L-MUT

ATSAMD21E17D-AUT

ATSAMD21J17D-MUT

ATSAMD21J17D-AUT

ATSAMD21G17D-AUT

ATSAMD21J17D-MMZT

ATSAMD21J17D-MMFT

ATSAMD21E17D-MZT

ATSAMD21E17D-MZTV02

ATSAMD21E17D-MZTV07

ATSAMD21E17D-MZTVAO

ATSAMD21E17L-MFT

ATSAMD21E17D-MFT

ATSAMD21G17D-MFT

ATSAMD21G17L-MFT

ATSAMD21E17L-AFT

ATSAMD21E17D-AFT

ATSAMD21E17D-AZT

ATSAMD21E17D-AZTVAO

ATSAMD21J17D-MFT

ATSAMD21G17D-MZT

ATSAMD21G17D-MZTV01

ATSAMD21G17D-MZTV03

ATSAMD21G17D-MZTV04

ATSAMD21G17D-MZTVAO

ATSAMD21G17D-MZTV04-BW

ATSAMD21G17D-MZTV03-VW

ATSAMD21J17D-MZT

ATSAMD21J17D-MZTVAO

ATSAMD21J17D-AFT

ATSAMD21J17D-AZT

ATSAMD21J17D-AZTV06

ATSAMD21J17D-AZTV08

ATSAMD21J17D-AZTVAO

ATSAMD21J17D-AZTV06-VW

ATSAMD21G17D-AFT

ATSAMD21G17D-AZT

ATSAMD21G17D-AZTV05

ATSAMD21G17D-AZTVAO

ATSAMD21J15B-MMF

ATSAMD21J16B-MMF

ATSAMD21E16L-MF

ATSAMD21E15L-MF

ATSAMD21E15B-MF

ATSAMD21E16B-MF

ATSAMD21G15B-MF

ATSAMD21G16B-MF

ATSAMD21E16L-AF

ATSAMD21E15L-AF

ATSAMD21E15B-AF

ATSAMD21E16B-AF

ATSAMD21J15B-MF

ATSAMD21J16B-MF

ATSAMD21J15B-AF

ATSAMD21J16B-AF

ATSAMD21G15B-AF

ATSAMD21G16B-AF

ATSAMD21J16B-MMU

ATSAMD21J15B-MMU

ATSAMD21E16B-MU

ATSAMD21E15B-MU

ATSAMD21G16B-MU

ATSAMD21G15B-MU

ATSAMD21E16B-AU

ATSAMD21E15B-AU

ATSAMD21J16B-MU

ATSAMD21J15B-MU

ATSAMD21J16B-AU

ATSAMD21J15B-AU

ATSAMD21G16B-AU

ATSAMD21G15B-AU

ATSAMD21E16L-MNT

ATSAMD21E15L-MNT

ATSAMD21G16L-MNT

ATSAMD21E16B-UUT

ATSAMD21E15B-UUT

ATSAMD21J16B-MMUT

ATSAMD21J15B-MMUT

ATSAMD21E16B-MUT

ATSAMD21E15B-MUT

ATSAMD21G16B-MUT

ATSAMD21G15B-MUT

ATSAMD21G16L-MUT

ATSAMD21E16B-AUT

ATSAMD21E15B-AUT

ATSAMD21J16B-MUT

ATSAMD21J15B-MUT

ATSAMD21J16B-AUT

ATSAMD21J15B-AUT

ATSAMD21G16B-AUT

ATSAMD21G15B-AUT

ATSAMD21J15B-MMFT

ATSAMD21J16B-MMFT

ATSAMD21E16L-MFT

ATSAMD21E15L-MFT

ATSAMD21E15B-MFT

ATSAMD21E16B-MFT

ATSAMD21G15B-MFT

ATSAMD21G16B-MFT

ATSAMD21E16L-AFT

ATSAMD21E15L-AFT

ATSAMD21E15B-AFT

ATSAMD21E16B-AFT

ATSAMD21J15B-MFT

ATSAMD21J16B-MFT

ATSAMD21J15B-AFT

ATSAMD21J16B-AFT

ATSAMD21G15B-AFT

ATSAMD21G16B-AFT

ATSAMD21J15B-MMZ

ATSAMD21J16B-MMZ

ATSAMD21E16B-MZ

ATSAMD21E15B-MZ

ATSAMD21E15B-MZVAO

ATSAMD21E16B-AZ

ATSAMD21E15B-AZ

ATSAMD21E16B-AZVAO

ATSAMD21G16B-MZ

ATSAMD21G15B-MZ

ATSAMD21G15B-MZVAO

ATSAMD21J16B-MZ

ATSAMD21J15B-MZ

ATSAMD21J16B-MZVAO

ATSAMD21J16B-AZ

ATSAMD21J15B-AZ

ATSAMD21J16B-AZVAO

ATSAMD21G16B-AZ

ATSAMD21G15B-AZ

ATSAMD21G16B-AZVAO

ATSAMD21J16B-CUT

ATSAMD21J15B-CUT

ATSAMD21E16C-UUT

ATSAMD21E15C-UUT

ATSAMD21J15B-MMZT

ATSAMD21J16B-MMZT

ATSAMD21E15B-MZT

ATSAMD21E16B-MZT

ATSAMD21E16B-MZTV16

ATSAMD21E16B-MZTV26

ATSAMD21E15B-MZTVAO

ATSAMD21E16B-MZTVAO

ATSAMD21E16B-AZT

ATSAMD21E15B-AZT

ATSAMD21E15B-AZTV30

ATSAMD21E16B-AZTVAO

ATSAMD21G15B-MZT

ATSAMD21G16B-MZT

ATSAMD21G16B-MZTV15

ATSAMD21G16B-MZTV23

ATSAMD21G15B-MZTVAO

ATSAMD21G16B-MZTVAO

ATSAMD21J16B-MZT

ATSAMD21J15B-MZT

ATSAMD21J16B-MZTVAO

ATSAMD21J16B-AZT

ATSAMD21J15B-AZT

ATSAMD21G16B-AZT

ATSAMD21G15B-AZT

ATSAMD21G16B-AZTV27

ATSAMD21G16B-AZTVAO

ATSAMD21J18A-MMZ

ATSAMD21J18A-MMZVAO

ATSAMD21J17A-MMF

ATSAMD21J18A-MMF

ATSAMD21E18A-MZ

ATSAMD21E17A-MZ

ATSAMD21E18A-MZVAO

ATSAMD21E18A-MF

ATSAMD21E17A-MF

ATSAMD21G17A-MF

ATSAMD21G18A-MF

ATSAMD21E17A-AF

ATSAMD21E18A-AF

ATSAMD21E18A-AZ

ATSAMD21E17A-AZ

ATSAMD21E18A-AZVAO

ATSAMD21J17A-MF

ATSAMD21J18A-MF

ATSAMD21G18A-MZ

ATSAMD21G17A-MZ

ATSAMD21G18A-MZVAO

ATSAMD21J18A-MZ

ATSAMD21J17A-MZ

ATSAMD21J17A-AF

ATSAMD21J18A-AF

ATSAMD21J17A-AZ

ATSAMD21J18A-AZ

ATSAMD21J18A-AZVAO

ATSAMD21G17A-AF

ATSAMD21G18A-AF

ATSAMD21G17A-AZ

ATSAMD21G18A-AZ

ATSAMD21J18A-CU

ATSAMD21J17A-CU

ATSAMD21J17A-MMU

ATSAMD21J18A-MMU

ATSAMD21E18A-MU

ATSAMD21E17A-MU

ATSAMD21G18A-MU

ATSAMD21G17A-MU

ATSAMD21E17A-AU

ATSAMD21E18A-AU

ATSAMD21J17A-MU

ATSAMD21J18A-MU

ATSAMD21J18A-AU

ATSAMD21J17A-AU

ATSAMD21G18A-AU

ATSAMD21G17A-AU

ATSAMD21J18A-CUT

ATSAMD21J17A-CUT

ATSAMD21G18A-UUT

ATSAMD21G17A-UUT

ATSAMD21J17A-MMUT

ATSAMD21J18A-MMUT

ATSAMD21E18A-MUT

ATSAMD21E17A-MUT

ATSAMD21G17A-MUT

ATSAMD21G18A-MUT

ATSAMD21E17A-AUT

ATSAMD21E18A-AUT

ATSAMD21J17A-MUT

ATSAMD21J18A-MUT

ATSAMD21J17A-AUT

ATSAMD21J18A-AUT

ATSAMD21G17A-AUT

ATSAMD21G18A-AUT

ATSAMD21J18A-MMZT

ATSAMD21J18A-MMZTV05

ATSAMD21J18A-MMZTVAO

ATSAMD21J17A-MMFT

ATSAMD21J18A-MMFT

ATSAMD21E18A-MZT

ATSAMD21E17A-MZT

ATSAMD21E18A-MZTVAO

ATSAMD21E18A-MFT

ATSAMD21E17A-MFT

ATSAMD21E15A-MFT

ATSAMD21G17A-MFT

ATSAMD21G18A-MFT

ATSAMD21E17A-AFT

ATSAMD21E18A-AFT

ATSAMD21E18A-AZT

ATSAMD21E17A-AZT

ATSAMD21E18A-AZTVAO

ATSAMD21J17A-MFT

ATSAMD21J18A-MFT

ATSAMD21G18A-MZT

ATSAMD21G17A-MZT

ATSAMD21G18A-MZTV02

ATSAMD21G18A-MZTV07

ATSAMD21G18A-MZTV02-BW

ATSAMD21G18A-MZTVAO

ATSAMD21J18A-MZT

ATSAMD21J17A-MZT

ATSAMD21J18A-MZTV01

ATSAMD21J18A-MZTV03

ATSAMD21J18A-MZTVAO

ATSAMD21J18A-MZTV03-BW

ATSAMD21J17A-AFT

ATSAMD21J18A-AFT

ATSAMD21J17A-AZT

ATSAMD21J18A-AZT

ATSAMD21J18A-AZTV04

ATSAMD21J18A-AZTVAO

ATSAMD21G17A-AFT

ATSAMD21G18A-AFT

ATSAMD21G17A-AZT

ATSAMD21G18A-AZT

ATSAMDA1E16A-MBTV02001

ATSAMDA1E16A-MBT

ATSAMDA1E16A-MBTV02001-VW

ATSAMDA1E16A-ABT

ATSAMDA1E15A-ABT

ATSAMDA1G16A-MBT

ATSAMDA1J16A-ABT

ATSAMDA1J15A-ABT

ATSAMDA1J16A-ABTV01

ATSAMDA1G16A-ABT

ATSAMDA1G15A-ABT

ATSAMDA1G14A-ABT

ATSAMDA1J16B-ABV06

ATSAMDA1E16B-MBTV19001

ATSAMDA1E16B-MBT

ATSAMDA1E15B-MBT

ATSAMDA1E14B-MBT

ATSAMDA1E16B-MBTV01

ATSAMDA1E16B-MBTV09

ATSAMDA1E16B-MBTV11

ATSAMDA1E16B-MBTV13

ATSAMDA1E16B-MBTV22

ATSAMDA1E16B-MBTVAO

ATSAMDA1E14B-MBTVAO

ATSAMDA1E16B-MBTV11-MB

ATSAMDA1E16B-MBTV22-MB

ATSAMDA1E16B-MBTV19001-MB

ATSAMDA1E16B-ABT

ATSAMDA1E15B-ABT

ATSAMDA1E14B-ABT

ATSAMDA1E15B-ABTV10

ATSAMDA1E16B-ABTV12

ATSAMDA1E16B-ABTV17

ATSAMDA1E16B-ABTVAO

ATSAMDA1E15B-ABTVAO

ATSAMDA1G16B-MBT

ATSAMDA1G15B-MBT

ATSAMDA1G14B-MBT

ATSAMDA1G16B-MBTV20

ATSAMDA1G16B-MBTVAO

ATSAMDA1G16B-MBTV20-MB

ATSAMDA1J16B-ABT

ATSAMDA1J15B-ABT

ATSAMDA1J14B-ABT

ATSAMDA1J16B-ABTV03

ATSAMDA1J16B-ABTV05

ATSAMDA1J16B-ABTV06

ATSAMDA1J16B-ABTV18

ATSAMDA1J16B-ABTV21

ATSAMDA1J16B-ABTV24

ATSAMDA1J16B-ABTV28

ATSAMDA1J16B-ABTV03-BW

ATSAMDA1J16B-ABTVAO

ATSAMDA1J16B-ABTVAO-GM

ATSAMDA1G16B-ABT

ATSAMDA1G15B-ABT

ATSAMDA1G14B-ABT

ATSAMDA1G16B-ABTV08

ATSAMDA1G16B-ABTV14

ATSAMDA1G16B-ABTV25

ATSAMDA1G16B-ABTV29

ATSAMDA1G16B-ABTVAO

ATSAMDA1G15B-ABTVAO

ATSAMDA1G16B-ABTVAO-GM

ATSAMDA1G16B-ABTV08-GM

ATSAMDA1G16B-ABTVAO-SG

# SAM D21/DA1 Family Silicon Errata and Data Sheet Clarification

## SAM D21/DA1 Family

## SAM D21/DA1 Family

The SAM D21/DA1 family of devices that you have received conform functionally to the current Device Data Sheet (DS40001882**K**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following table.

The errata described in this document will be addressed in future revisions of the SAM D21/DA1 family silicon.

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in Data Sheet Clarifications, following the discussion of silicon issues.

**Table 1.** SAM D21 Family Silicon Device Identification

| Part Number | Device Identification (DID[31:0]) | Revision (DID.REVISION[3:0]) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A | B | C | D | E | F | G | H | I | J |
| ATSAMD21J18A | 0x10010x00 | 0x0 | 0x1 | 0x2 | 0x3 | N/A | N/A | N/A | 0x7 | N/A | N/A |
| ATSAMD21J17A | 0x10010x01 | | | | | | | | | | |
| ATSAMD21J16A | 0x10010x02 | | | | | | | | | | |
| ATSAMD21J15A | 0x10010x03 | | | | | | | | | | |
| ATSAMD21G18A | 0x10010x05 | | | | | | | | | | |
| ATSAMD21G18AU(1) | 0x10010x0F | | | | | | | | | | |
| ATSAMD21G17A | 0x10010x06 | | | | | | | | | | |
| ATSAMD21G17AU(1) | 0x10010x10 | | | | | | | | | | |
| ATSAMD21G16A | 0x10010x07 | | | | | | | | | | |
| ATSAMD21G15A | 0x10010x08 | | | | | | | | | | |
| ATSAMD21E18A | 0x10010x0A | | | | | | | | | | |
| ATSAMD21E17A | 0x10010x0B | | | | | | | | | | |
| ATSAMD21E16A | 0x10010x0C | | | | | | | | | | |
| ATSAMD21E15A | 0x10010x0D | | | | | | | | | | |
| ATSAMD21J16B | 0x10011x20 | N/A | N/A | N/A | N/A | 0x4 | 0x5 | N/A | N/A | N/A | 0x9 |
| ATSAMD21J15B | 0x10011x21 | | | | | | | | | | |
| ATSAMD21G16B | 0x10011x23 | | | | | | | | | | |
| ATSAMD21G15B | 0x10011x24 | | | | | | | | | | |
| ATSAMD21E16B | 0x10011x26 | | | | | | | | | | |
| ATSAMD21E16BU(1) | 0x10011x55 | | | | | | | | | | |
| ATSAMD21E15B | 0x10011x27 | N/A | N/A | N/A | N/A | 0x4 | 0x5 | N/A | N/A | N/A | 0x9 |
| ATSAMD21E15BU(1) | 0x10011x56 | | | | | | | | | | |
| ATSAMD21G16L | 0x10011x57 | | | | | | | | | | |
| ATSAMD21E16L | 0x10011x3E | | | | | | | | | | |
| ATSAMD21E15L | 0x10011x3F | | | | | | | | | | |
| ATSAMD21E16CU(1) | 0x10011x62 | N/A | N/A | N/A | N/A | N/A | 0x5 | N/A | N/A | N/A | 0x9 |
| ATSAMD21E15CU(1) | 0x10011x63 | | | | | | | | | | |

**Table 1.** SAM D21 Family Silicon Device Identification (continued)

| Part Number | Device Identification (DID[31:0]) | Revision (DID.REVISION[3:0]) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | A | B | C | D | E | F | G | H | I | J |
| ATSAMD21E17D | 0x10012x94 | N/A | N/A | N/A | N/A | N/A | N/A | 0x6 | N/A | 0x8 | N/A |
| ATSAMD21E17DU[1] | 0x10012x95 | | | | | | | | | | |
| ATSAMD21E17L | 0x10012x97 | | | | | | | | | | |
| ATSAMD21G17D | 0x10012x93 | | | | | | | | | | |
| ATSAMD21G17L | 0x10012x96 | | | | | | | | | | |
| ATSAMD21J17D | 0x10012x92 | | | | | | | | | | |

**Note:**

1. Part numbers ending in "U" correspond to the UUT packaging.

**Note:** Refer to the “Device Service Unit” chapter in the current Device Data Sheet (DS40001882**K**) for a detailed information on Device Identification and Revision IDs for your specific device.

**Table 2.** SAM DA1 Family Silicon Device Identification

| Part Number | Device Identification (DID[31:0]) | Revision (DID.REVISION[3:0]) | | |
|---|---|---|---|---|
| | | E | F | J |
| ATSAMDA1E14A | 0x10011x31 | 0x4 | N/A | 0x9 |
| ATSAMDA1E15A | 0x10011x30 | 0x4 | N/A | 0x9 |
| ATSAMDA1E16A | 0x10011x2F | 0x4 | N/A | 0x9 |
| ATSAMDA1G14A | 0x10011x2E | 0x4 | N/A | 0x9 |
| ATSAMDA1G15A | 0x10011x2D | 0x4 | N/A | 0x9 |
| ATSAMDA1G16A | 0x10011x2C | 0x4 | N/A | 0x9 |
| ATSAMDA1J14A | 0x10011x2B | 0x4 | N/A | 0x9 |
| ATSAMDA1J15A | 0x10011x2A | 0x4 | N/A | 0x9 |
| ATSAMDA1J16A | 0x10011x29 | 0x4 | N/A | 0x9 |
| ATSAMDA1E14B | 0x10011x6C | N/A | 0x5 | 0x9 |
| ATSAMDA1E15B | 0x10011x6B | N/A | 0x5 | 0x9 |
| ATSAMDA1E16B | 0x10011x6A | N/A | 0x5 | 0x9 |
| ATSAMDA1G14B | 0x10011x69 | N/A | 0x5 | 0x9 |
| ATSAMDA1G15B | 0x10011x68 | N/A | 0x5 | 0x9 |
| ATSAMDA1G16B | 0x10011x67 | N/A | 0x5 | 0x9 |
| ATSAMDA1J14B | 0x10011x66 | N/A | 0x5 | 0x9 |
| ATSAMDA1J15B | 0x10011x65 | N/A | 0x5 | 0x9 |
| ATSAMDA1J16B | 0x10011x64 | N/A | 0x5 | 0x9 |

**Note:** Refer to the “Device Service Unit” chapter in the current Device Data Sheet (DS40001882**K**) for a detailed information on Device Identification and Revision IDs for your specific device.

# Silicon Errata Summary

**Table 3.** Errata Summary

| Module | Feature | Item Number | Issue Summary | Affected Revisions | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | A | B | C | D | E | F | G | H | I | J |
| XOSC32K | Automatic Gain Control | 1.1.1 | The automatic amplitude control of the XOSC32K does not work. | X | X | X | X | X | X | X | X | X | X |
| XOSC32K | External Reset | 1.1.2 | If the external XOSC32K fails, the external reset will not reset the GCLKs sourced by the XOSC32K. | X | X | X | X | X | X | X | X | X | X |
| DFLL48M | Write Access to DFLL Register | 1.2.1 | The DFLL clock must be requested before being configured. | X | X | X | X | X | X | X | X | X | X |
| DFLL48M | False Out of Bound Interrupt | 1.2.2 | If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated. | X | X | X | X | X | X | X | X | X | X |
| DFLL48M | DFLL Status Bits (PCLKSR Register) | 1.2.3 | The DFLL status bits in the PCLKSR register during the USB Clock Recovery mode can be incorrect after a USB suspend state. | X | X | X | X | X | X | X | X | X | X |
| FDPLL | Lock Flag May Clear Randomly | 1.3.1 | The lock flag (DPLLSTATUS.LOCK) may clear randomly. | X | | | | | | | | | |
| FDPLL | FDPLL96M Operation Below 0°C Temperature | 1.3.2 | 96 MHz Fractional Digital Phased Locked Loop (FDPLL96M) operation above 64 MHz is not functional below 0°C. | X | X | X | X | | | | | | |
| FDPLL | Lock Time-out Values | 1.3.3 | The FDPLL lock time-out values are different from the parameters in the data sheet. | X | | | | | | | | | |
| FDPLL | DPLLRATIO Register FDPLL Ratio Value | 1.3.4 | When FDPLL ratio value in the DPLLRATIO register is changed on the fly, STATUS.DPLLLDRTO will not be set even though the ratio is updated. | X | X | X | X | X | X | X | X | X | X |
| FDPLL | FDPLL Unlock | 1.3.5 | When using the FDPLL **at temperature below 25°C**a spurious DPLL unlock (OSCCTRL.DPLLSTATUS.LOCK = 0) may be detected while the FDPLL still adheres to the Electrical Characteristics metrics. | X | X | X | X | X | X | X | X | X | X |
| ADC | Linearity Error in Single-Shot Mode | 1.4.1 | In Single-Shot mode and at +125°C, ADC conversions have linearity errors. | X | X | X | X | | | | | | |
| ADC | Offset Correction | 1.4.2 | Offset correction is not supported in the 8-bit and 10-bit conversion resolution. | X | X | X | X | X | X | X | X | X | X |
| DEVICE | APB Clock | 1.5.1 | If APB clock is stopped and the GCLK is running, APB read access to read-synchronized registers will freeze the system. | X | X | X | X | X | X | X | X | X | X |
| DEVICE | VDDIN POR Threshold | 1.5.2 | When VDDIN is lower than the POR threshold during power rise or fall, an internal pull-up resistor is enabled on pins with PTC functionality. | X | X | X | | | | | | | |
| DEVICE | Digital Pin Output in Stand-by Mode | 1.5.3 | Digital pin outputs from Timer/Counters, AC, GCLK, and SERCOM do not change the value during Stand-by Sleep mode. | X | X | | | | | | | | |
| DEVICE | NVM User Row Mapping Value for WDT | 1.5.4 | The WDT Window bitfield default value on silicon is not as specified in the NVM User Row Mapping table in the current data sheet. | | | X | X | | | | | | |
| DEVICE | SYSTICK Calibration Value | 1.5.5 | The SYSTICK calibration is incorrect. | X | X | X | X | X | X | | | | |
| DEVICE | High Leakage Current on VDDIO | 1.5.6 | When external reset is active it causes a high leakage current on VDDIO. | X | X | X | X | X | | | | | |
| DEVICE | Standby Entry | 1.5.7 | Potential device lockup upon standby entry when Systick interrupt is enabled. | X | X | X | X | X | X | X | X | X | X |
| DEVICE | Standby Wake-up | 1.5.8 | Potential lockup on standby wakeup with interrupts disabled. | X | X | X | X | X | X | X | X | X | X |
| DEVICE | Program and Debug Interface Disable | 1.5.9 | PDID is not available on some silicon revisions. | X | X | X | X | X | X | X | | | |
| DAC | EMPTY Flag is Set When Leaving Stand-by Mode | 1.6.1 | DAC.INTFLAG.EMPTY will be set after exiting Sleep mode. | X | X | X | X | X | X | X | X | X | X |
| DMAC | Consecutive Write Instructions to CRCDATAIN | 1.7.1 | If data is written to CRCDATAIN in two consecutive instructions, the CRC computation may be incorrect. | X | X | X | X | X | X | | | | |
| DMAC | Linked Descriptors | 1.7.2 | When at least one channel using linked descriptors is already active, enabling another DMA channel can result in a channel Fetch Error or an incorrect descriptor fetch. | X | X | X | X | X | X | | | | |
| DSU | Debugger and DSU Cold-plugging Procedure | 1.8.1 | If a debugger has issued a DSU Cold-Plugging procedure and then released the CPU from the resulting CPU Reset Extension, the CPU will be held in CPU Reset Extension after any upcoming reset event. | X | X | X | X | | | | | | |
| DSU | Pause-on-Error is Not Functional | 1.8.2 | The MBIST Pause-on-Error feature is not functional. | X | X | X | X | X | X | | | | |
| DSU | CRC32 Computation Failure | 1.8.3 | The DSU CRC32 computation is not functional on RAM. | X | X | X | X | | | | | | |
| EIC | Interrupts | 1.9.1 | When the EIC is configured to generate an interrupt on a low level or rising edge or both edges with the filter enabled, a spurious flag may appear. | X | X | X | X | X | X | | | | |
| I²S | Transmit Serializer | 1.10.1 | In LSBIT mode, the I²S RX serializer only works when the slot size is 32 bits. | X | X | X | X | X | X | X | X | X | X |
| I²S | I²S is Not Functional | 1.10.2 | The I²S is not functional. | X | | | | | | | | | |
| I²S | Software Reset | 1.10.3 | The software reset, SWRST, does not propagate inside the I2S module. | | X | | | | | | | | |

**Table 3.** Errata Summary (continued)

| Module | Feature | Item Number | Issue Summary | Affected Revisions | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | A | B | C | D | E | F | G | H | I | J |
| I²S | Client Mode | 1.10.4 | The I²S is not functional in Client mode. | | X | | | | | | | | |
| I²S | CPU Clock/I2S Clock Ratio | 1.10.5 | Depending on the CPU clock/I²S clock ratio, the SYNCBUSY.CKEN0 flag is occasionally stuck. | | X | | | | | | | | |
| I²S | PDM2 Mode | 1.10.6 | The PDM2 mode does not function. | | X | | | | | | | | |
| I²S | Rx Serializer | 1.10.7 | The Rx serializer in the RIGHT Data Slot Formatting Adjust mode does not function when the slot size is not 32 bits. | | X | X | X | | | | | | |
| I²S | Client Mode (CTRLB Register) | 1.10.8 | In I²C Client mode, writing the CTRLB register when in the AMATCH or DRDY interrupt service routines can cause the state machine to reset. | X | X | X | X | X | | | | | |
| NVMCTRL | CRC32 is Not Executed | 1.11.1 | When the device is secured and the EEPROM emulation area configured to none, the CRC32 is not executed on the entire Flash area | X | X | X | X | | | | | | |
| NVMCTRL | Spurious Writes | 1.11.2 | The default value of MANW in NVM.CTRLB is '0', which can lead to spurious writes to the NVM. | X | X | X | X | X | X | X | X | X | X |
| NVMCTRL | NVMCTRL.INTFLAG.READY | 1.11.3 | The NVMCTRL.INTFLAG.READY bit is not updated after a `RWWEEER` command and will keep holding a '1' value. | | | | | X | | | | | |
| NVMCTRL | RWW NVM Command | 1.11.4 | Incorrect data fetch after RWW NVM command | | | | | X | X | X | X | X | X |
| PTC | WCOMP Interrupt Flag | 1.12.1 | The WCOMP interrupt flag is not stable. | X | X | X | X | | | | | | |
| PORT - I/O Pin Controller | PA24 and PA25 Inputs | 1.13.1 | PA24 and PA25 cannot be used as an input when configured as GPIO with continuous sampling. | X | X | X | X | | | | | | |
| PORT - I/O Pin Controller | PA07 Status During Internal Start-up | 1.13.2 | While the internal start-up is not completed, the PA07 pin is driven low by the device. | X | X | X | X | | | | | | |
| PORT - I/O Pin Controller | PA24 and PA25 Pull-up/Pull-down Configuration | 1.13.3 | On PA24 and PA25 pins, the pull-up and pull-down configuration is not disabled automatically when alternative pin function is enabled with the exception for USB. | X | X | X | X | X | X | X | X | X | X |
| PORT - I/O Pin Controller | PA24 and PA25 Pull-down Functionality | 1.13.4 | Pull-down functionality is not available on GPIO pins, PA24 and PA25. | X | X | X | X | X | | | | | |
| PORT - I/O Pin Controller | Write Protect | 1.13.5 | Non-debugger IOBUS writes to PAC Write-protected registers are not prevented when the PORT is PAC Write-protected. | X | X | X | X | X | X | X | X | X | X |
| PM | Debug Logic and Watchdog Reset | 1.14.1 | In Debug mode, if a Watchdog Reset occurs, the debug session is lost. | X | X | X | X | | | | | | |
| PM | Power-down Modes and Wake-up From Sleep | 1.14.2 | In Standby, Idle1, and Idle2 Sleep modes, the device may not wake from sleep. | X | X | X | | | | | | | |
| SERCOM | I²C Client SCL Low Extend Time-out | 1.15.1 | The I²C Client SCL low extend time-out and Host SCL low extend time-out cannot be used if SCL low time-out is disabled. | X | X | X | X | | | | | | |
| SERCOM | I2C Transaction in Debug Mode | 1.15.2 | In I²C Host mode, an ongoing transaction is stopped when the current byte transaction is completed and the corresponding interrupt is triggered if enabled. | X | X | X | X | | | | | | |
| SERCOM | SPI with SPI Select Low Detection | 1.15.3 | If the SERCOM is enabled in SPI mode with SSL detection enabled and CTRLB.RXEN =1, an erroneous SPI select low interrupt can be generated. | X | X | X | X | X | | | | | |
| SERCOM | USART in Auto-baud Mode | 1.15.4 | In USART Auto-baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors. | X | X | X | X | X | X | | | | |
| SERCOM | NACK and Repeated Start in I²C Host Mode | 1.15.5 | For High-Speed Host Read operations, sending a NACK forces a STOP to be issued making repeated start not possible in that mode. | X | X | X | X | X | X | X | X | X | X |
| SERCOM | SERCOM-USART: Collision Detection | 1.15.6 | In USART operating mode with Collision Detection enabled, the SERCOM will not abort the current transfer as expected if a collision is detected. | X | X | X | X | X | X | X | X | X | X |
| SERCOM | SERCOM-USART: USART in Debug Mode | 1.15.7 | In USART operating mode, if DBGCTRL.DBGSTOP=1, data transmission is not halted after entering Debug mode. | X | X | X | X | X | X | X | X | X | X |
| SERCOM | SERCOM-I²C: Client Mode with DMA | 1.15.8 | In I²C Client Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push a data to the DATA register. | X | X | X | X | X | X | X | X | X | X |
| SERCOM | SERCOM-I²C: I²C Mode in 10-bit Address | 1.15.9 | 10-bit addressing in I²C Client mode is not functional. | X | X | X | X | X | X | X | X | X | X |
| SERCOM | SERCOM-SPI: Data Preload | 1.15.10 | In SPI Client mode and with Client Data Preload Enabled, the first data sent from the Client will be a dummy byte. | X | X | X | X | X | X | X | X | X | X |
| SERCOM | CLKHOLD Bit Status in I²C | 1.15.11 | STATUS.CLKHOLD bit can be written whereas it is a read-only status bit in both Host and Client modes. | X | X | X | X | X | X | X | X | X | X |

**Table 3.** Errata Summary (continued)

| Module | Feature | Item Number | Issue Summary | Affected Revisions | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | A | B | C | D | E | F | G | H | I | J |
| SERCOM | Quick Command I²C | 1.15.12 | When Quick command is enabled (CTRLB.QCEN=1), the software can issue a repeated Start by either writing CTRLB.CMD or ADDR.ADDR bitfields. If in these conditions, SCL Stretch Mode is CTRLA.SCLSM=1, a bus error will be generated. | X | X | X | X | X | X | X | X | X | X |
| SERCOM | Repeated Start I²C | 1.15.13 | For High-Speed Host Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start making repeated start not possible in that mode. | X | X | X | X | X | X | X | X | X | X |
| SERCOM | Client Mode I²C | 1.15.14 | In Client mode, BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR STATUS register bits are not automatically cleared when INTFLAG.AMATCH is cleared. | X | X | X | X | X | X | X | X | X | X |
| SERCOM | USART in Auto-Baud Mode | 1.15.15 | In auto-baud mode, communication fails after synchronization byte Sync field is received. | X | X | X | X | | | | | | |
| TCC | WAVE/WAVEB Registers Hardware Exception | 1.16.1 | When the Peripheral Access Controller (PAC) protection is enabled, writing to the WAVE or WAVEB registers will not cause a hardware exception. | X | X | X | X | | | | | | |
| TCC | Interrupts and Wake-up From Stand-by Mode | 1.16.2 | The TCC interrupts, FAULT1, FAULT0, FAULTB, FAULTA, DFS, ERR, and CNT, cannot wake the device from Stand-by mode. | X | | | | | | | | | |
| TCC | Extra Count Cycle | 1.16.3 | If an input event triggered STOP action is performed simultaneously as the counter overflows, the first pulse width of the subsequent counter start can be altered with one prescaled clock cycle. | X | X | X | X | | | | | | |
| TCC | OVF Flag and DMA | 1.16.4 | If the OVF flag in the INTFLAG register is already set when enabling the DMA, this will trigger an immediate DMA transfer and overwrite the current buffered value in the TCC register. | X | | | | | | | | | |
| TCC | MCx Flag and DMA | 1.16.5 | If the MCx flag in the INTFLAG register is set when enabling the DMA, this will trigger an immediate DMA transfer and overwrite the current buffered value in the TCC register. | X | X | X | X | | | | | | |
| TCC | Two-ramp Mode | 1.16.6 | In Two-ramp mode, two events will be generated per cycle, one on each ramp's end. | X | X | X | X | | | | | | |
| TCC | SYNCBUSY Bit in Stand-by Mode | 1.16.7 | When waking up from the Stand-by Power Save mode, the SYNCBUSY.CTRLB, SYNCBUSY.STATUS,SYNCBUSY.COUNT, SYNCBUSY.PATT, SYNCBUSY.WAVE, SYNCBUSY.PER and SYNCBUSY.CCx bits may be locked to '1'. | X | X | X | X | | | | | | |
| TCC | Retrigger in Dual Slope Mode | 1.16.8 | In Dual-Slope mode a retrigger event does not clear the TCC counter. | X | X | X | X | | | | | | |
| TCC | CTRLA.RUNDSTDBY Enable Protection | 1.16.9 | When the RUNSTDBY bit is written after the TCC is enabled, the respective TCC APB bus is stalled and the RUNDSTBY bit in the TCC CTRLA register is not enabled-protected. | X | X | X | X | | | | | | |
| TCC | Fault Filtering of Inverted Fault | 1.16.10 | TCC fault filtering on inverted fault is not functional. | X | X | X | X | | | | | | |
| TCC | Recoverable Fault and Blanking Operation | 1.16.11 | When blanking is enabled, a recoverable fault that occurs during the first increment of a rising TCC is not blanked. | X | X | X | X | | | | | | |
| TCC | RAMP 2 Mode | 1.16.12 | In RAMP 2 mode with Fault keep, qualified and restart, and if a fault occurred at the end of the period during the qualified state, the switch to the next ramp can have two restarts. | X | X | X | X | X | | | | | |
| TCC | CAPTMARK is Not Functional | 1.16.13 | FCTRLX.CAPTURE[CAPTMARK] does not function as described in the data sheet. | | | | | X | X | | | | |
| TCC | Capture Using PWP/PPW Mode | 1.16.14 | When a capture is done using PWP or PPW mode, CC0 and CC1 are always fill with the period. It is not possible to get the pulse width. | | | | | X | | | | | |
| TCC | Advance Capture Mode | 1.16.15 | Advance capture mode does not work. | X | X | X | X | X | X | | | | |
| TCC | MAX Capture Mode | 1.16.16 | In Capture mode while using MAX Capture mode, with the Timer set in up counting mode, if an input event occurred within two cycles before TOP, the value captured is '0' instead of TOP. | X | X | X | X | X | X | | | | |
| TCC | Dithering Mode | 1.16.17 | Using TCC in Dithering mode with external retrigger events can lead to an unexpected stretch of right-aligned pulses, or a shrink of left-aligned pulses. | X | X | X | X | X | X | | | | |
| TCC | TCC0/WO[6] on PA16 and TCC0/WO[7] on PA17 | 1.16.18 | TCC0/WO[6] on PA16 and TCC0/WO[7] on PA17 are not available. | X | | | | | | | | | |
| TCC | Interrupt Flags | 1.16.19 | The TCC interrupt flags are not always properly set when using asynchronous TCC features. | | | | | X | | | | | |
| TCC | PATTB | 1.16.20 | The PATTB register write will not update the PATT register on an update condition. | | | | | X | X | X | X | X | X |
| TCC | PERBUF | 1.16.21 | In downcounting mode, the Lock Update bit (CTRLB.LUPD) does not protect against a PER register update from the PERBUF register. | X | X | X | X | X | X | X | X | X | X |
| TCC | TCC with EVSYS in SYNC/RESYNC Mode | 1.16.22 | TCC Peripheral is not compatible with an EVSYS channel in SYNC or RESYNC Mode. | X | X | X | X | X | X | X | X | X | X |

**Table 3.** Errata Summary (continued)

| Module | Feature | Item Number | Issue Summary | Affected Revisions | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | A | B | C | D | E | F | G | H | I | J |
| TCC | Prescale | 1.16.23 | A DMA transfer to the TCC CC register may not initiate when using the TCC MCx as the trigger source (CTRLB.TRIGSRC) and the TCC Prescale (CTRLA.PRESCALE) value is set to 64/256/1024. | | | | | X | X | X | X | X | X |
| TC | Spurious TC Overflow | 1.17.1 | Spurious TC overflow and Match/Capture events may occur. | X | X | X | X | | | | | | |
| TC | TC with EVSYS in SYNC/RESYNC Mode | 1.17.2 | TC peripheral is not compatible with an EVSYS channel in SYNC or RESYNC mode. | X | X | X | X | X | X | X | X | X | X |
| TC | DMA Trigger | 1.17.3 | When using TC MC0 as a trigger source for the DMA, it will not work. | X | X | X | X | X | X | | | | |
| USB | FLENC Register | 1.18.1 | The FLENC register negative sign management is not correct. | X | | | | | | | | | |
| Voltage Regulator | Low-Power Mode Above +85°C | 1.19.1 | The voltage regulator in Low-Power mode is not functional at temperatures above +85°C. | X | X | X | X | | | | | | |
| SYSCTRL | XOSC | 1.20.1 | The XOSC can prevent entry into Stand-by mode regardless of XOSC.RUNSTDBY value. | | | | | X | X | X | X | X | X |
| SYSCTRL | BOD33 | 1.20.2 | The BOD33 interrupt may not be generated second time if VDDANA does not increase above the user-defined threshold (BOD.LEVEL[5:0]) while in Active mode. | | | X | X | X | X | X | X | X | X |
| BOD33 | Hysteresis | 1.21.1 | The BOD33 Hysteresis does not work if either an external reset or a watchdog reset occurs during the time that the supply voltage is between VBOD- and VBOD+. | X | X | X | X | X | X | X | X | X | X |
| ALL | Voltage Specifications | 1.22.1 | All Data Sheet references to “GND-0.6V” and “VDD+0.6V | X | X | X | X | X | X | X | X | X | X |

# Table of Contents

# 1. Errata Issues

The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

## 1.1. 32.768 kHz Crystal Oscillator (XOSC32K)

### 1.1.1. Automatic Gain Control

The automatic amplitude control of the XOSC32K does not work.

**Workaround**

Use the XOSC32K with Automatic Amplitude control disabled (XOSC32K.AAMPEN = 0).

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.1.2. External Reset

If the external XOSC32K fails, neither the external pin RST, nor the GCLK software reset can reset the GCLK generators using XOSC32K as the source clock.

**Workaround**

Do a power cycle to reset the GCLK generators after an external XOSC32K failure.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

## 1.2. 48 MHz Digital Frequency-Locked Loop (DFLL48M)

### 1.2.1. Write Access to DFLL Register

The DFLL clock must be requested before being configured; otherwise, a write access to a DFLL register can freeze the device.

**Workaround**

Write a '0' to the DFLL ONDEMAND bit in the DFLLCTRL register before configuring the DFLL module.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.2.2. False Out of Bound Interrupt

If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated. These interrupts will be generated even if the final calibration values at DFLL48M lock are not at maximum or minimum, and therefore, may be false out of bounds interrupts.

**Workaround**

Enable the DFLL Out Of Bounds (DFLLOOB) interrupt when configuring the DFLL in closed loop mode. In the DFLLOOB ISR verify the COARSE and FINE calibration bits and process as needed.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.2.3. DFLL Status Bits (PCLKSR Register)

The DFLL status bits in the PCLKSR register during the USB Clock Recovery mode can be incorrect after a USB suspend state.

**Workaround**

Do not monitor the DFLL status bits in the PCLKSR register during the USB Clock Recovery mode.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

## 1.3. 96 MHz Fractional Digital Phase-Locked Loop (FDPLL)

### 1.3.1. Lock Flag May Clear Randomly

The lock flag (DPLLSTATUS.LOCK) may clear randomly. When the lock flag randomly clears, DPLLLCKR and DPLLLCKF interrupts will also trigger, and the DPLL output is masked.

**Workaround**

Set DPLLCTRLB.LBYPASS to '1' to disable masking of the DPLL output by the lock status.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | | | | | | | | | |

### 1.3.2. FDPLL96M Operation Below 0°C Temperature

96 MHz Fractional Digital Phased Locked Loop (FDPLL96M) operation above 64 MHz is not functional below 0°C.

**Workaround**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

### 1.3.3. Lock Time-out Values

The FDPLL lock time-out values are different from the parameters in the data sheet.

**Workaround**

The time-out values are:

- DPLLCTRLB.LTIME[2:0] = 4 : 10 ms
- DPLLCTRLB.LTIME[2:0] = 5 : 10 ms
- DPLLCTRLB.LTIME[2:0] = 6 : 11 ms
- DPLLCTRLB.LTIME[2:0] = 7 : 11 ms

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| X | | | | | | | | | |

### 1.3.4. DPLLRATIO Register FDPLL Ratio Value

When FDPLL ratio value in the DPLLRATIO register is changed on the fly, STATUS.DPLLLDRTO will not be set even though the ratio is updated.

#### Workaround

Monitor the INTFLAG.DPLLLDRTO instead of STATUS.DPLLLDRTO to get the status for DPLLRATIO update.

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.3.5. FDPLL Unlock

When using the FDPLL at temperature below 25°C, a spurious DPLL unlock (OSCCTRL.DPLLSTATUS.LOCK = 0) may be detected while the FDPLL still adheres to the Electrical Characteristics metrics defined in *Section 43.16* of the data sheet. During the unlock periods, the DPLL output clock is halted and then restarts.

#### Workaround

When using the FDPLL at temperature below 25°C, enable the lock bypass (OSCCTRL.DPLLSTATUS.LOCK = 1) to avoid losing the FDPLL clock output during a false unlock status. The workaround does not avoid false unlock indications, but instead disables the gating of the FDPLL clock output by the lock status. Therefore, the clock is issued even if the FDPLL status shows unlocked.

The pseudo codes are as follows:

- Set DPLLCTRLB.LBYPASS = 1
- Set DPLLCTRLA.ENABLE = 1
- Wait (DPLLSTATUS.CLKRDY = 1)
- Set Source for GCLK with DPLL

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

## 1.4. Analog-to-Digital Controller (ADC)

### 1.4.1. Linearity Error in Single-Shot Mode

In single-shot mode and at +125°C, ADC conversions have linearity errors.

#### Workarounds

1. At +125°C, do not use the ADC in single-shot mode. Instead, use the ADC in free-running mode only.
2. At +125°C, use the ADC in single-shot mode only with VDDANA > 3V.

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

### 1.4.2. Offset Correction

Offset correction using the OFFSETCORR register is not supported in the 8-bit and 10-bit conversion resolution.

**Workarounds**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

## 1.5. Device

### 1.5.1. APB Clock

If APB clock is stopped and the GCLK is running, APB read access to read-synchronized registers will freeze the system. The CPU and the DAP AHB-AP are stalled, and as a consequence, debug operation is impossible.

**Workaround**

Do not make read access to read-synchronized registers when the APB clock is stopped and GCLK is running. To recover from this condition, power cycle the device or reset the device using the $\overline{\text{RESET}}$ pin.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.5.2. VDDIN POR Threshold

When VDDIN is lower than the POR threshold during power rise or fall, an internal pull-up resistor is enabled on pins with PTC functionality, refer to the *PORT Function Multiplexing* section in the current data sheet. This behavior will be present even if PTC functionality is not enabled on the pin. The POR level is defined in the "Power-On Reset (POR) Characteristics" chapter of the current data sheet.

**Workaround**

Use a pin without PTC functionality if the pull-up could damage your application during power up.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | | | | | | | |

### 1.5.3. Digital Pin Output in Stand-by Mode

Digital pin outputs from Timer/Counters, Analog Comparator (AC), Generic Clock Controller (GCLK), and SERCOM ($I^2C$ and SPI) do not change the value during Stand-by Sleep mode.

**Workaround**

Set the voltage regulator in Normal mode before entering Standby Sleep mode to keep digital pin output enabled. This is done by setting the RUNSTDBY bit in the VREG register.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | | | | | | | | |

### 1.5.4. NVM User Row Mapping Value for WDT

The WDT Window bitfield default value on silicon is not as specified in the *NVM User Row Mapping* table in the current data sheet. The data sheet defines the default value as 0x5, while it on silicon this value is 0xB.

#### Workaround

None.

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| | | X | X | | | | | | |

### 1.5.5. SYSTICK Calibration Value

The SYSTICK calibration value is incorrect.

#### Workaround

The correct SYSTICK calibration value is 0x40000000. This value should not be used to initialize the Systick RELOAD value register, which should be initialized instead with a value depending on the main clock frequency and on the tick period required by the application. For a detailed description of the SYSTICK module, refer to the official Arm® Cortex®-M0+ documentation.

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | | | | |

### 1.5.6. High Leakage Current on VDDIO

When external reset is active it causes a high leakage current on VDDIO.

#### Workaround

Minimize the time external reset is active.

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | | | | | |

### 1.5.7. Potential Lockup on Standby Entry

When the Systick interrupt is enabled, a device lockup can occur when the Systick interrupt coincides with the standby entry.

#### Workaround

Disable the Systick interrupt before entering standby and re-enable it after wake up.

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.5.8. Potential Lockup on Standby Wakeup with Arm Core PRIMASK=1

Upon wake up from standby with Arm Core register PRIMASK = 1, the first instruction fetched by the CPU in Flash memory will be the first instruction following the WFI. This instruction may be returned corrupted and lead to unpredictable behavior.

If PRIMASK = 0, the first instruction fetched by the CPU will be the first instruction of the interrupt handler. This one will be correctly returned to the CPU.

.

### Workaround

Two possible workarounds can be used independently:

1. Disable Flash sleep in Standby Sleep mode (SLEEPPRM = DISABLED).
2. Place the standby sleep function in SRAM and make sure that at least one dummy Flash fetch is completed before exiting the function. This can be achieved by reading 2 data in memory with addresses separated by at least the cache size. Because the first read could be a cache hit, the second one will be a cache miss and will generate a real read in memory.

The following code may be used:

```
__attribute__((noinline, section(".ramfunc")))
 void ram_sleep(void)
 {
 __DSB();
 __WFI();

// The following sequence ensures that the flash is ready before returning from the RAM code
 #define CACHE_SIZE_IN_BYTES 64
 ((volatile unsigned int *)FLASH_ADDR)[CACHE_SIZE_IN_BYTES/sizeof(unsigned int)];     //will
read a word at FLASH_ADDR + 0x40 in this case
 ((volatile unsigned int *)FLASH_ADDR)[(CACHE_SIZE_IN_BYTES*2)/sizeof(unsigned int)]; //will
read a word at FLASH_ADDR + 0x80 in this case
 }
```

### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

## 1.5.9. Program and Debug Interface Disable

Program and Debug Interface Disable (PDID) is not available on some silicon revisions. See the following table.

### Workaround

None.

### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | | | |

# 1.6. Digital-to-Analog Controller (DAC)

## 1.6.1. EMPTY Flag is Set When Leaving Stand-by Mode

When DAC.CTRLA.RUNSTDBY = 0 and DATABUF is written (not empty), and if the device goes to Stand-by Sleep mode before a Start Conversion event, DAC.INTFLAG.EMPTY will be set after exiting Sleep mode.

### Workaround

After waking from Stand-by mode, ignore and clear the flag DAC.INTFLAG.EMPTY.

### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

## 1.7. Direct Memory Access Controller (DMAC)

### 1.7.1. Consecutive Write Instructions to CRCDATAIN

If data is written to CRCDATAIN in two consecutive instructions, the CRC computation may be incorrect.

#### Workaround

Add a `NOP` instruction between each write to the CRCDATAIN register.

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | | | | |

### 1.7.2. Linked Descriptors

When at least one channel using linked descriptors is already active, enabling another DMA channel (with or without linked descriptors) can result in a channel Fetch Error (FERR) or an incorrect descriptor fetch.

This occurs if the channel number of the channel being enabled is lower than the channel already active.

#### Workaround

When enabling a DMA channel while other channels using linked descriptors are already active, the channel number of the new channel enabled must be greater than the other channel numbers.

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | | | | |

## 1.8. Device Service Unit (DSU)

### 1.8.1. Debugger and DSU Cold-plugging Procedure

If a debugger has issued a DSU Cold-Plugging procedure and then released the CPU from the resulting CPU Reset Extension, the CPU will be held in CPU Reset Extension after any upcoming reset event.

#### Workaround

The CPU must be released from the CPU Reset Extension either by writing a one in the DSU STATUSA.CRSTEXT register or by applying an external reset with SWCLK high or by power cycling the device.

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

### 1.8.2. Pause-on-Error is Not Functional

The MBIST Pause-on-Error feature is not functional.

#### Workaround

None.

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | | | | |

### 1.8.3. CRC32 Computation Failure

The DSU CRC32 computation is not functional on RAM.

#### Workaround

Before using the CRC32 on RAM, execute the following code:

```
*(volatile unsigned int* 0x41007058) &= ~0x30000UL;
```

After using the CRC32, execute the following code:

```
*(volatile unsigned int* 0x41007058) |= 0x20000UL;
```

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

## 1.9. External Interrupt Controller (EIC)

### 1.9.1. Interrupts

When the EIC is configured to generate an interrupt on a low level or rising edge or both edges (CONFIGn.SENSEx) with the filter enabled (CONFIGn.FILTENx), a spurious flag may appear for the dedicated pin on the INTFLAG.EXTINT[x] register as soon as the EIC is enabled using the CTRLA ENABLE bit.

#### Workaround

Clear the INTFLAG bit once the EIC is enabled and before enabling the interrupts.

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | | | | |

## 1.10. Integrated Inter-IC Sound ($I^2S$)

### 1.10.1. Transmit Serializer

In LSBIT mode (i.e., SERCTRL.BITREV is set), the $I^2S$ RX serializer only works when the slot size is 32 bits.

#### Workaround

In SERCTRL.SERMODE RX, SERCTRL.BITREV LSBIT must be used with CLKCTRL.SLOTSIZE 32.

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.10.2. $I^2S$ is Not Functional

The $I^2S$ is not functional.

#### Workaround

None.

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | | | | | | | | | |

### 1.10.3. Software Reset

The software reset, SWRST, does not propagate inside the I²S module. As a consequence, Client mode may not be reconfigured correctly and may result in unexpected behavior of the SYNCBUSY register.

**Workaround**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| | X | | | | | | | | |

### 1.10.4. Module is Not Functional in Client Mode

The I²S is not functional in Client mode (i.e., when (FSSEL = 1, SCKSEL = 1).

**Workaround**

None. FSSEL and SCKSEL must be '0'.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| | X | | | | | | | | |

### 1.10.5. CPU Clock/I²S Clock Ratio

Depending on the CPU clock/I²S clock ratio, the SYNCBUSY.CKEN0 flag is occasionally stuck at '1' when starting a new audio stream with CTRLA.SWRST = 1, CTRLA.ENABLE = 1, and CTRLA.CKEN0 = 1.

**Workaround**

Disable the IP by writing a '0' to CTRLA.ENABLE before resetting it (CTRLA.SWRST = 1).

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| | X | | | | | | | | |

### 1.10.6. PDM2 Mode is Not Functional

The PDM2 mode (i.e., when using two PDM microphones) does not function.

**Workaround**

None. Only one PDM microphone can be connected. Therefore, the I²S controller should be configured in normal Receive mode with one slot.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| | X | | | | | | | | |

### 1.10.7. Rx Serializer

The Rx serializer in the RIGHT Data Slot Formatting Adjust mode (SERCTRL.SLOTADJ clear) does not function when the slot size is not 32 bits.

**Workaround**

In SERCTRL.SERMODE RX, SERCTRL.SLOTADJ RIGHT must be used with CLKCTRL.SLOTSIZE 32.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | X | X | X | | | | | | |

### 1.10.8. Client Mode (CTRLB Register)

In I²C Client mode, writing the CTRLB register when in the AMATCH or DRDY interrupt service routines can cause the state machine to reset.

#### Workaround

Write CTRLB.ACKACT to '0' using the following sequence:

```
// If higher priority interrupts exist, then disable so that the
// following two writes are atomic.
SERCOM - STATUS.reg = 0;
SERCOM - CTRLB.reg = 0;
// Re-enable interrupts if applicable.
```

Write CTRLB.ACKACT to '1' using the following sequence:

```
SERCOM - CTRLB.reg = SERCOM_I2CS_CTRLB_ACKACT;
```

Otherwise, only write to CTRLB in the AMATCH or DRDY interrupts if it is to close out a transaction.

When not closing a transaction, clear the AMATCH interrupt by writing a '1' to its bit position instead of using CTRLB.CMD. The DRDY interrupt is automatically cleared by reading/writing to the DATA register in Smart mode. If not in Smart mode, DRDY should be cleared by writing a '1' to its bit position.

#### Code Replacements Examples:

*Current:*

```
SERCOM - CTRLB.reg |= SERCOM_I2CS_CTRLB_ACKACT;
```

*Change to:*

```
 SERCOM - STATUS.reg = 0;
SERCOM - CTRLB.reg = SERCOM_I2CS_CTRLB_ACKACT;
SERCOM - CTRLB.reg &= ~SERCOM_I2CS_CTRLB_ACKACT;
SERCOM - CTRLB.reg = 0;
/* ACK or NACK address */
SERCOM - CTRLB.reg |= SERCOM_I2CS_CTRLB_CMD(0x3);
// CMD=0x3 clears all interrupts, so to keep the result similar,
// CMD=0x3 clears all interrupts, so to keep the result similar,
// PREC is cleared if it was set.
if (SERCOM - INTFLAG.bit.PREC) SERCOM - INTFLAG.reg = SERCOM_I2CS_INTFLAG_PREC;
SERCOM - INTFLAG.reg = SERCOM_I2CS_INTFLAG_AMATCH;
```

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | | | | | |

## 1.11. Non-Volatile Memory Controller (NVMCTRL)

### 1.11.1. CRC32 is Not Executed on the Entire Flash Area

When the device is secured and the EEPROM emulation area configured to none, the CRC32 is not executed on the entire Flash area but up to the on-chip Flash size minus half a row.

#### Workaround

When using CRC32 on a protected device with the EEPROM emulation area configured to none, compute the reference CRC32 value to the full chip Flash size minus a half row.

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

### 1.11.2. Spurious Writes

The default value of MANW in NVM.CTRLB is '0', which can lead to spurious writes to the NVM if a data write is done through a pointer with a wrong address corresponding to the NVM area.

#### Workaround

Set MANW in the NVM.CTRLB register to '1' at start-up

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.11.3. NVMCTRL.INTFLAD.READY Bit

The NVMCTRL.INTFLAG.READY bit is not updated after a `RWWEEER` command and will keep holding a '1' value. If a new `RWWEEER` command is issued it can be accepted even if the previous `RWWEEER` command is ongoing. The ongoing NVM `RWWEER` command will be aborted, and the content of the row under erase will be unpredictable.

#### Workaround

Perform a dummy write to the page buffer right before issuing a `RWWEEER` command. This will cause the INTFLAG.READY bit to behave as expected.

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| | | | | X | | | | | |

### 1.11.4. RWW NVM Command

#### Incorrect Data Fetch after RWW NVM Command

Issuing an NVM command on RWWEE region while the NVM Controller cache is enabled, can result in incorrect data fetch afterward.

#### Workaround

Disable the NVM Controller cache before issuing any RWW NVM command. Enable the cache only after the internal RWW operation is complete.

#### Pseudo Code

```
NVMCTRL->CTRLB.CACHEDIS |= NVMCTRL_CTRLB_CACHEDIS_Msk;
NVMRWW_ErasePage();
while(NVMCTRL_IsBusy());
NVMCTRL->CTRLB.CACHEDIS &= ~NVMCTRL_CTRLB_CACHEDIS_Msk;
```

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| | | | | X | X | X | X | X | X |

## 1.12. Peripheral Touch Controller (PTC)

### 1.12.1. WCOMP Interrupt Flag

The WCOMP interrupt flag is not stable. The WCOMP interrupt flag will not always be set as described in the data sheet.

#### Workaround

Do not use the WCOMP interrupt, instead use the WCOMP event.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

## 1.13. PORT - I/O Pin Controller

### 1.13.1. PA24 and PA25 Inputs

PA24 and PA25 cannot be used as an input when configured as GPIO with continuous sampling (cannot be read by PORT).

**Workarounds**

1. Use PA24 and PA25 for peripherals or only as output pins.
2. Configure PA31 to PA24 for on-demand sampling (CTRL[31:24] all zeroes) and access the IN register through the APB (not the IOBUS), to allow waiting for on-demand sampling.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

### 1.13.2. PA07 Status During Internal Start-up

While the internal start-up is not completed, the PA07 pin is driven low by the device. Then, as with all of the other pins, it is configured as a High Impedance pin.

**Workaround**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

### 1.13.3. PA24 and PA25 Pull-up/Pull-down Configuration

On PA24 and PA25 pins the pull-up and pull-down configuration is not disabled automatically when alternative pin function is enabled, with the exception for USB.

**Workaround**

For PA24 and PA25 pins, the GPIO pull-up and pull-down must be disabled before enabling alternative functions on them.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.13.4. PA24 and PA25 Pull-down Functionality

Pull-down functionality is not available on GPIO pins, PA24 and PA25

**Workaround**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | | | | | |

### 1.13.5. Write-Protect

The non-debugger IOBUS writes to the PAC Write-protected registers are not prevented when the PORT is PAC Write-protected.

**Workaround**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

## 1.14. Power Manager (PM)

### 1.14.1. Debug Logic and Watchdog Reset

In Debug mode, if a Watchdog Reset occurs, the debug session is lost.

**Workaround**

A new debug session must be restart after a Watchdog Reset.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

### 1.14.2. Power-down Modes and Wake-up From Sleep

In Standby, Idle1, and Idle2 Sleep modes, the device may not wake from sleep. An External Reset, Power on Reset, or Watchdog Reset will start the device again.

**Workaround**

The SLEEPPRM bits in the NVMCTRL.CTRLB register must be written to 3 (NVMCTRL - CTRLB.bit.SLEEPPRM = 3) to ensure correct operation of the device. The average power consumption of the device will increase with 20 µA compared to the values in the *Electrical Characteristics* chapter of the current data sheet.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | | | | | | | |

## 1.15. Serial Communication Interface (SERCOM)

### 1.15.1. $I^2C$ Client SCL Low Extend Time-out

The $I^2C$ Client SCL low extend time-out (CTRLA.SEXTTOEN) and Host SCL low extend time-out (CTRLA.MEXTTOEN) cannot be used if SCL low time-out (CTRLA.LOWTOUT) is disabled. When SCTRLA.LOWTOUT = 0, GCLK_SERCOM_SLOW is not requested.

**Workaround**

To use the Host or Client SCL low extend time-outs, enable the SCL low time-out (CTRLA.LOWTOUT = 1).

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

### 1.15.2. I²C Transaction in Debug Mode

In I²C Host mode, an ongoing transaction should be stalled immediately when DBGCTRL.DBGSTOP is set and the CPU enters Debug mode. Instead, it is stopped when the current byte transaction is completed and the corresponding interrupt is triggered if enabled.

**Workaround**

In I²C Host mode, keep DBGCTRL.DBGSTOP = 0 when in Debug mode.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

### 1.15.3. SPI with SPI Select Low Detection

If the SERCOM is enabled in SPI mode with SSL detection enabled (CTRLB.SSDE) and CTRLB.RXEN = 1, an erroneous SPI select low interrupt (INTFLAG.SSL) can be generated.

**Workaround**

Enable the SERCOM first with CTRLB.RXEN = 0. In a subsequent write, set CTRLB.RXEN = 1.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | | | | | |

### 1.15.4. USART in Auto-baud Mode

In USART Auto-baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.

**Workaround**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | | | | |

### 1.15.5. NACK and Repeated Start in I²C Host Mode

For High-Speed Host Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued, making repeated start not possible in that mode.

**Workaround**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.15.6. SERCOM-USART: Collision Detection

In USART Operating mode with Collision Detection enabled (CTRLB.COLDEN=1), the SERCOM will not abort the current transfer as expected if a collision is detected, and if the SERCOM APB Clock is lower than the SERCOM Generic Clock.

**Workaround**

The SERCOM APB clock must always be higher than the SERCOM Generic Clock to support collision detection.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.15.7. SERCOM-USART: USART in Debug Mode

In USART operating mode, if DBGCTRL.DBGSTOP=1, data transmission is not halted after entering Debug mode.

**Workaround**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.15.8. SERCOM-I$^2$C: Client Mode with DMA

In I$^2$C Client Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push a data to the DATA register. Because a NACK was received, the transfer on the I$^2$C bus will not occur causing the loss of this data.

**Workaround**

Configure the DMA transfer size to the number of data to be received by the I$^2$C Host. DMA cannot be used if the number of data to be received by the Host is unknown.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.15.9. SERCOM-I$^2$C: I$^2$C Mode in 10-bit Address

10-bit addressing in I$^2$C Client mode is not functional.

**Workaround**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.15.10. SERCOM-SPI: Data Preload

In SPI Client mode and with Client Data Preload Enabled (CTRLB.PLOADEN = 1), the first data sent from the Client will be a dummy byte if the Host cannot keep the SPI Select (SS) line low until the end of transmission.

**Workarounds**

In SPI Client mode, the SPI Select pin (SS) must be kept low by the Host until the end of the transmission if the Client Data Preload feature is used (CTRLB.PLOADEN = 1).

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.15.11. CLKHOLD Bit Status in I²C

STATUS.CLKHOLD bit can be written whereas it is a read-only status bit in both Host and Client modes.

**Workarounds**

Do not clear STATUS.CLKHOLD bit to preserve the current clock hold state.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.15.12. Quick Command I²C

When Quick command is enabled (CTRLB.QCEN=1), the software can issue a repeated Start by either writing CTRLB.CMD or ADDR.ADDR bit fields. If, in these conditions, SCL Stretch Mode is CTRLA.SCLSM=1, a bus error will be generated.

**Workarounds**

Use Quick Command mode (CTRLB.QCEN=1) only if SCL Stretch Mode is CTRLA.SCLSM=0.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.15.13. Repeated Start I²C

For High-Speed Host Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start, making repeated start is not possible in that mode.

**Workarounds**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.15.14. Client Mode I²C

In Client mode, the BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR STATUS register bits are not automatically cleared when INTFLAG.AMATCH is cleared.

**Workarounds**

PERBUFlear the STATUS register bits, such as BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR by writing these STATUS bits to 1, when INTFLAG.AMATCH is cleared.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.15.15. USART in Auto-Baud Mode

Communication fails after synchronization byte Sync field is received.

**Workarounds**

Add a delay after synchronization field, before sending any data.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

## 1.16. Timer/Counter for Control Applications (TCC)

### 1.16.1. WAVE/WAVEB Registers Hardware Exception

When the Peripheral Access Controller (PAC) protection is enabled, writing to the WAVE or WAVEB registers will not cause a hardware exception.

**Workaround**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

### 1.16.2. Interrupts and Wake-up From Stand-by Mode

The TCC interrupts, FAULT1, FAULT0, FAULTB, FAULTA, DFS, ERR, and CNT, cannot wake the device from Stand-by mode.

**Workaround**

Do not use the TCC interrupts, FAULT1, FAULT0, FAULTB, FAULTA, DFS, ERR, and CNT, to wake the device from Stand-by mode.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | | | | | | | | | |

### 1.16.3. Extra Count Cycle

If an input event triggered STOP action is performed at the same time as the counter overflows, the first pulse width of the subsequent counter start can be altered with one prescaled clock cycle.

**Workaround**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

### 1.16.4. OVF Flag and DMA

If the OVF flag in the INTFLAG register is already set when enabling the DMA, this will trigger an immediate DMA transfer and overwrite the current buffered value in the TCC register.

**Workaround**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | | | | | | | | | |

### 1.16.5. MCx Flag and DMA

If the MCx flag in the INTFLAG register is set when enabling the DMA, this will trigger an immediate DMA transfer and overwrite the current buffered value in the TCC register.

**Workaround**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

### 1.16.6. Two-ramp Mode

In Two-ramp mode, two events will be generated per cycle, one on each ramp's end. EVCTRL.CNTSEL.END cannot be used to identify the end of a double ramp cycle.

**Workaround**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

### 1.16.7. SYNCBUSY Bit in Stand-by Mode

When waking up from the Stand-by Power Save mode, the SYNCBUSY.CTRLB, SYNCBUSY.STATUS, SYNCBUSY.COUNT, SYNCBUSY.PATT, SYNCBUSY.WAVE, SYNCBUSY.PER and SYNCBUSY.CCx bits may be locked to '1'.

**Workaround**

After waking up from Stand-by Power Save mode, perform a software reset of the TCC if you are using the SYNCBUSY.CTRLB, SYNCBUSY.STATUS, SYNCBUSY.COUNT, SYNCBUSY.PATT, SYNCBUSY.WAVE, SYNCBUSY.PER or SYNCBUSY.CCx bits

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

### 1.16.8. Retrigger in Dual Slope Mode

In Dual Slope mode a retrigger event does not clear the TCC counter.

**Workaround**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

### 1.16.9. CTRLA.RUNDSTDBY Enable Protection

When the RUNSTDBY bit is written after the TCC is enabled, the respective TCC APB bus is stalled and the RUNDSTBY bit in the TCC CTRLA register is not enabled-protected.

**Workaround**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

### 1.16.10. Fault Filtering of Inverted Fault

TCC fault filtering on inverted fault is not functional.

**Workaround**

Use only non-inverted faults.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

### 1.16.11. Recoverable Fault and Blanking Operation

When blanking is enabled, a recoverable fault that occurs during the first increment of a rising TCC is not blanked.

**Workaround**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

### 1.16.12. RAMP 2 Mode

In RAMP 2 mode with Fault keep, qualified and restart, and if a fault occurred at the end of the period during the qualified state, the switch to the next ramp can have two restarts.

**Workaround**

Avoid faults few cycles before the end or the beginning of a ramp.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | | | | | |

### 1.16.13. CAPTMARK is Not Functional

FCTRLX.CAPTURE[CAPTMARK] does not function as described in the data sheet. CAPTMARK cannot be used to identify captured values triggered by fault inputs source A or B on the same channel.

**Workaround**

Use two different channels to timestamp FaultA and FaultB.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| | | | | X | X | | | | |

### 1.16.14. Capture Using PWP/PPW Mode

When a capture is done using PWP or PPW mode, CC0 and CC1 are always fill with the period. It is not possible to get the pulse width.

**Workaround**

Use the PWP feature on TC instead of TCC

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| | | | | X | | | | | |

### 1.16.15. Advance Capture Mode

Advance capture mode (CAPTMIN CAPTMAX LOCMIN LOCMAX DERIV0) doesn't work if an upper channel is not in one of these mode. For example, when CC[0]=CAPTMIN, CC[1]=CAPTMAX, CC[2]=CAPTEN, and CC[3]=CAPTEN, CAPTMIN and CAPTMAX will not work.

**Workaround**

Basic capture mode must be set in lower channel and advance capture mode in upper channel.

For example, CC[0]=CAPTEN , CC[1]=CAPTEN , CC[2]=CAPTMIN, CC[3]=CAPTMAX

All capture will be done as expected.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | | | | |

### 1.16.16. MAX Capture Mode

In Capture mode while using MAX Capture mode, with the Timer set in up counting mode, if an input event occurred within two cycles before TOP, the value captured is '0' instead of TOP.

**Workarounds**

1. If the event is controllable, the capture event should not occur when the counter is within two cycles before the TOP value.
2. Use the Timer in Down Counter mode and capture the MIN value instead of the MAX value.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | | | | |

### 1.16.17. Dithering Mode

Using TCC in Dithering mode with external retrigger events can lead to an unexpected stretch of right-aligned pulses, or a shrink of left-aligned pulses.

**Workaround**

Do not use retrigger events/actions when the TCC is configured in Dithering mode.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | | | | |

### 1.16.18. TCC0/WO[6] on PA16 and TCC0/WO[7] on PA17 Are Not Available

TCC0/WO[6] on PA16 and TCC0/WO[7] on PA17 are not available.

**Workaround**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | | | | | | | | | |

### 1.16.19. Interrupt Flags

The TCC interrupt flags INTFLAG.ERR, INTFLAG.DFS, INTFLAG.UFS, INTFLAG.CNT, INTFLAG.FAULTA,INTFLAG.FAULTB, INTFLAG.FAULT0, INTFLAG.FAULT1 are not always properly set when using asynchronous TCC features.

**Workaround**

Do not use these flags when using asynchronous TCC features.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| | | | | X | | | | | |

### 1.16.20. PATTB

The PATTB register write will not update the PATT register on an update condition.

**Workaround**

Write directly to the PATT register when an update is required.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| | | | | X | X | X | X | X | X |

### 1.16.21. PERBUF

In down-counting mode, the Lock Update bit (CTRLB.LUPD) does not protect against a PER register update from the PERBUF register.

**Workaround**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.16.22. TCC with EVSYS in SYNC/RESYNC Mode

TCC peripheral is not compatible with an EVSYS channel in SYNC or RESYNC mode.

**Workaround**

Use TCC with an EVSYS channel in ASYNC mode.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.16.23. Prescale

A DMA transfer to the TCC.CC register may not initiate when using the TCC MCx as the trigger source (CTRLB.TRIGSRC), and the TCC Prescale (CTRLA.PRESCALE) value is set to 64/256/1024.

**Workaround**

Use the TCC.CCB for DMA transfers, or the GCLK division register (GENDIV.DIV) to divide the TCC input clock to a range that is suitable to match the required 64/256/1024 prescale clock values. To ensure this does not have an impact on other modules in the system, the divided GCLK used to supply the TCC peripheral with its input clock should not source other peripheral modules.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

## 1.17. Timer/Counter (TC)

### 1.17.1. Spurious TC Overflow

Spurious TC overflow and Match/Capture events may occur.

**Workaround**

Do not use the TC overflow and Match/Capture events. Use the corresponding interrupts instead.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

### 1.17.2. TC with EVSYS in SYNC/RESYNC Mode

TC peripheral is not compatible with an EVSYS channel in SYNC or RESYNC mode.

**Workaround**

Use TC with an EVSYS channel in ASYNC mode.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

### 1.17.3. DMA Trigger

When using TC MC0 as a trigger source for the DMA, only the first transfer is performed and after that DMA is blocked and does not do any more transfers.

**Workaround**

Changing the trigger source to TC Overflow makes things work as expected.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | | | | |

## 1.18. Universal Serial Bus (USB)

### 1.18.1. FLENC Register

The FLENC register negative sign management is not correct.

**Workaround**

The following rule must be used for negative values:

- FLENC 0x8 (hex) is equal to '0' decimal.
- FLENC 0x9 to 0xF (hex) are equal to -1 to -7 decimal instead of -7 to -1.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | | | | | | | | | |

## 1.19. Voltage Regulator

### 1.19.1. Low-Power Mode Above +85°C

The voltage regulator in Low-Power mode is not functional at temperatures above +85°C.

**Workaround**

Enable normal mode on the voltage regulator in Stand-by Sleep mode.

Example code:

```
// Set the voltage regulator in normal mode configuration in Stand-by Sleep mode
SYSCTRL->VREG.bit.RUNSTDBY = 1;
```

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | | | | | | |

## 1.20. SYSCTRL

### 1.20.1. XOSC

The XOSC can prevent entry into Stand-by mode regardless of XOSC.RUNSTDBY value.

**Workaround**

Change the clock source for gclk0 to the internal RC OSC, and then disable the XOSC before entering Standby mode.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| | | | | X | X | X | X | X | X |

### 1.20.2. BOD33

The BOD33 interrupt may only generate once if VDDANA does not increase above the user-defined threshold (BOD.LEVEL[5:0]) when in Active mode. If in Standby mode, when the BOD33 interrupt is generated, the device will have to be in Active mode while VDDANA increases above BOD.LEVEL to re-enable the BOD33 interrupt.

**Workaround**

None.

**Affected Silicon Revisions**

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| | | X | X | X | X | X | X | X | X |

## 1.21. BOD33

### 1.21.1. Hysteresis

The BOD33 Hysteresis does not work if either an external reset or a watchdog reset occurs during the time that the supply voltage is between VBOD- and VBOD+. If one of those resets occurs, the device will continue operation if the supply voltage is above VBOD- and the reset condition is lifted.

**Workaround**

Use the BOD33 Level in the NVM User Row as an upper BOD threshold and configure the SYSCTRL.BOD33 Level bitfield to be the lower threshold, and therefore generating a hysteresis.

### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

## 1.22. ALL

### 1.22.1. Voltage Specifications

All Data Sheet references to “GND-0.6V” and “VDD+0.6V” should instead be “GND-0.3V” and “VDD+0.3V”, respectively.

#### Workaround

None.

#### Affected Silicon Revisions

| A | B | C | D | E | F | G | H | I | J |
|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X |

# 2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest revision of the device Data Sheet (DS40001882**K**). The corrected information is shown in **BOLD** type.

There are no new Data Sheet Clarifications to report.

# 3. Appendix A: Revision History

**Revision M Document - 04/2025**

Updated the verbiage for Device errata 1.5.9 One Time Programmable Lock to read *Program and Debug Interface Disable*.

**Revision L Document - 01/2025**

The following updates were performed in this revision:

- Updated the document throughout to reflect new silicon revisions H, I, and J
- Removed obsolete Data Sheet Clarifications
- Added errata Device: 1.5.9 One-Time Programmable Lock

**Revision K Document - 12/2024**

The following updates were performed in this revision:

- The following errata were added:
  - FDPLL: 1.3.5 FDPLL Unlock
  - ALL: 1.22.1 ALL Voltage Specifications

Removed obsolete Data Sheet Clarifications.

The following Data Sheet Clarifications were added in this revision:

- DFLL48M Characteristics - Open Loop Mode 85°C
- DFLL48M Characteristics - Open Loop Mode 105°C
- DFLL48M Characteristics - Open Loop Mode 125°C
- 32 kHz RC Oscillator Characteristics 125°C
- DFLL48M Characteristics - Open Loop Mode (Device Variant A) AEC-Q100 125°C

**Revision J Document - 06/2023**

Internal Engineering updates, Non-public release.

**Revision H Document - 08/2022**

The following updates were performed in this revision:

- The following errata were added:
  - SERCOM: 1.15.15 USART in Auto-Baud Mode
  - TC: 1.17.3 DMA Trigger

**Revision G Document - 08/2021**

The following updates were performed in this revision:

- Added new notes to the SAM D21 Family Silicon Device Identification table
- Added a new Data Sheet Clarification for BOD33
- Added the following silicon errata issue:
  - BOD33: 1.21.1 Hysteresis

**Revision F Document - 03/2021**

The SPI, $I^2S$, and $I^2C$ standards use the terminology "Master" and "Slave." The equivalent Microchip terminology, "Host" and "Client," is used in this document. This terminology has been updated throughout the document for this revision.

The following Data Sheet Clarifications were added in this revision:

- Voltage Reference Names

- DAC Accuracy Characterstics - Conversion Rate
- Decoupling Requirements
- Moisture Sensitivity Level

The following Silicon errata were added in this revision:

- ADC: 1.4.2 Offset Correction
- DEVICE: 1.5.7 Standby Entry
- DEVICE: 1.5.8 Standby Wake-up

**Rev E Document 03/2020**

The following items were updated in this revision:

- The Device Identification was updated in SAM D21 Family Silicon Device Identification
- Added a new table, SAM DA1 Family Silicon Device Identification
- Obsolete Data Sheet Clarifications were removed

The following errata was added in this revision:

- NVMCTRL 1.11.4: RWW NVM Command

**Rev D Document (04/2019)**

The following Data Sheet Clarifications were added:

- System Controller - XOSC
- Electrical Characteristics - Crystal Oscillator (XOSC)
- Schematic Checklist - Crystal Oscillator

**Rev C Document (11/2018)**

The following errata is added:

- Prescale

**Rev B Document (9/2018)**

The following Errata Issues were added:

- Write Protect
- NACK and Repeated Start in $I^2C$ Host Mode
- SERCOM-USART: Collision Detection
- SERCOM-USART: USART in Debug Mode
- SERCOM-$I^2C$: Client Mode with DMA
- SERCOM-$I^2C$: $I^2C$ Mode in 10-bit Address
- SERCOM-SPI: Data Preload
- CLKHOLD Bit Status in $I^2C$
- Quick Command $I^2C$
- Repeated Start $I^2C$
- Client Mode $I^2C$
- PATTB
- PERBUF
- TCC with EVSYS in SYNC/RESYNC Mode
- TC with EVSYS in SYNC/RESYNC Mode
- XOSC

- BOD33

**Rev A Document (4/2018)**
Initial release of this document.

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