



# MPQ4242B

## 5A, 36V, Fully Integrated USB PD Solution with Integrated Buck-Boost Converter, AEC-Q100 Qualified

### DESCRIPTION

The MPQ4242B is a fully integrated power delivery (PD) solution for USB Type-C sourcing ports. It integrates a buck-boost converter with four power switches and a USB PD controller. The device supports up to 5A of continuous output current ( $I_{OUT}$ ) under a certain input supply range.

The MPQ4242B's USB Type-C port supports USB PD revision 3.1 with PPS. It is backward compatible with DCP schemes for battery charging specification (BC1.2), 3A divider mode, and 1.2V/1.2V mode. The MPQ4242B also supports QC 2.0/3.0 and Huawei FCP mode.

The MPQ4242B provides a configurable PD power management state machine when the battery voltage ( $V_{BATT}$ ) is low, or if an over-temperature condition occurs. When two MPQ4242Bs are used as dual PD ports, the internal power sharing logic can effectively distribute the total power.

Fault condition protections include I/O pin short protection for the BUS and VIN pins, CC over-current protection (OCP), current limiting with hiccup mode, output over-voltage protection (OVP), and thermal shutdown.

The MPQ4242B requires a minimal number of readily available, standard external components. It is available in a QFN-22 (4mmx5mm) package.

### FEATURES

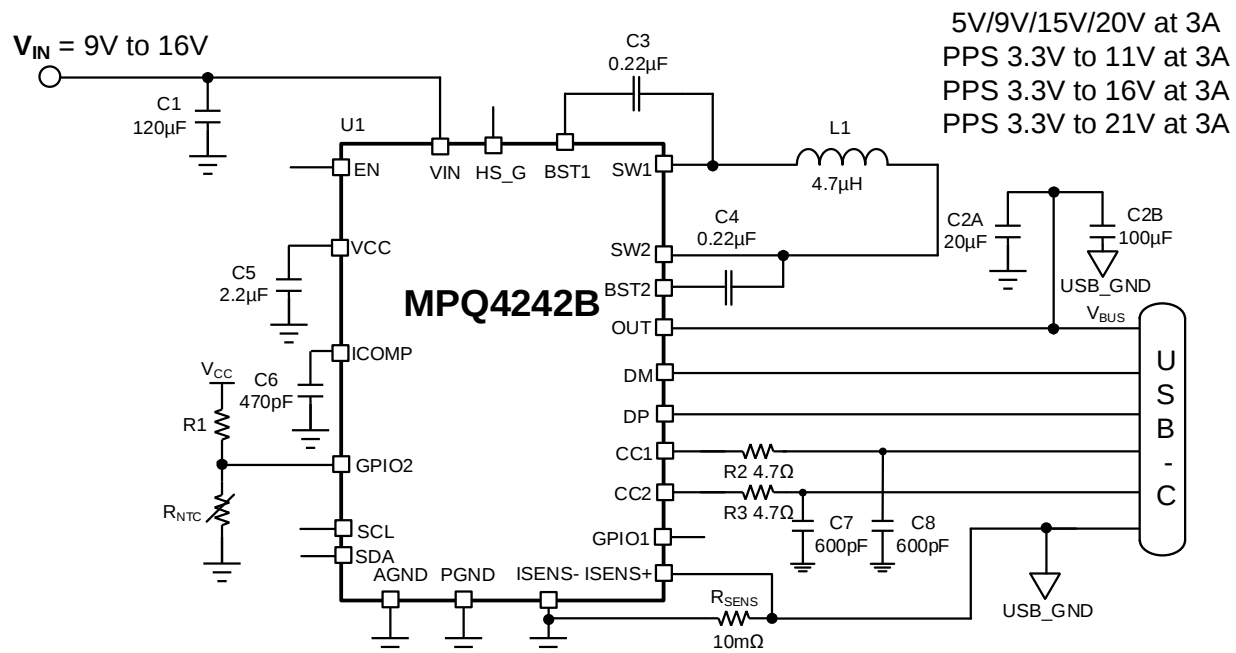
- All-In-One USB Power Delivery (PD) Solution for Automotive Sourcing Ports
- Integrated 4-Switch Buck-Boost Converter
- Integrated PD 3.1 Controller
- Wide 4.8V to 36V Operating Input Voltage ( $V_{IN}$ ) Range
- 3.3V to 22.5V Output Voltage ( $V_{OUT}$ ) Range
- Accurate Output CC Current Limit:  $\pm 5\%$
- External High-Side MOSFET (HS-FET) can be Paralleled
- Low Quiescent Current ( $I_Q$ ) when USB Type-C is Disconnected
- 250kHz / 420kHz Configurable Frequency with Spread Spectrum
- Supports USB PD R3.1, and PPS with 7 Power Data Object (PDO) List
- Passes USB-IF PD3.1 Certification Test (TID: 8822)
- Supports QC 3.0 Specification, Huawei FCP
- Supports DCP Schemes for BC1.2, 3A Divider Mode, and 1.2V/1.2V Mode
- CCx, DP, and DM Short to  $V_{BUS}$  /  $V_{BATT}$  Protection
- Battery Short to Ground Protection Driver
- I<sup>2</sup>C Slave Interface
- Output Line Drop Compensation
- Configurable PD Power Management during Low Battery Voltages or High Temperatures
- Supports Dual-Port PD Power Sharing
- PWM Duty Cycle Configurable LED Driver
- Up to 120 Minutes for EN Off Delay
- Available in a QFN-22 (4mmx5mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

### APPLICATIONS

- USB PD Charging Ports
- USB Power Supplies
- USB PD Hubs

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# TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number*            | Package             | Top Marking | MSL Rating |
|-------------------------|---------------------|-------------|------------|
| MPQ4242BGVE-0000-AEC1   | QFN-22<br>(4mmx5mm) | See Below   | 1          |
| MPQ4242BGVE-xxxx-AEC1** |                     |             |            |
| EVKT-MPQ4242B           | -                   | -           | -          |

\* For Tape & Reel, add suffix -Z (e.g. MPQ4242BGVE-xxxx-AEC1-Z).

\*\* “xxxx” is the configuration code identifier for the register setting stored in the OTP. Each “x” can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number.

\*\*\* The MPQ4242BGVE-0000-AEC1 is the default 60W PD version, which can be configured once by the one-time programmable (OTP) memory. Other suffix codes cannot be written with the OTP again.

## TOP MARKING

**MPSYWW**  
**M4242B**  
**LLLLLL**  
**E**

MPS: MPS prefix  
Y: Year code  
WW: Week code  
MP4242B: Part number  
LLLLLL: Lot number  
E: Wettable flank

## EVALUATION KIT EVKT-MPQ4242B

EVKT-MPQ4242B kit contents (items below can be ordered separately):

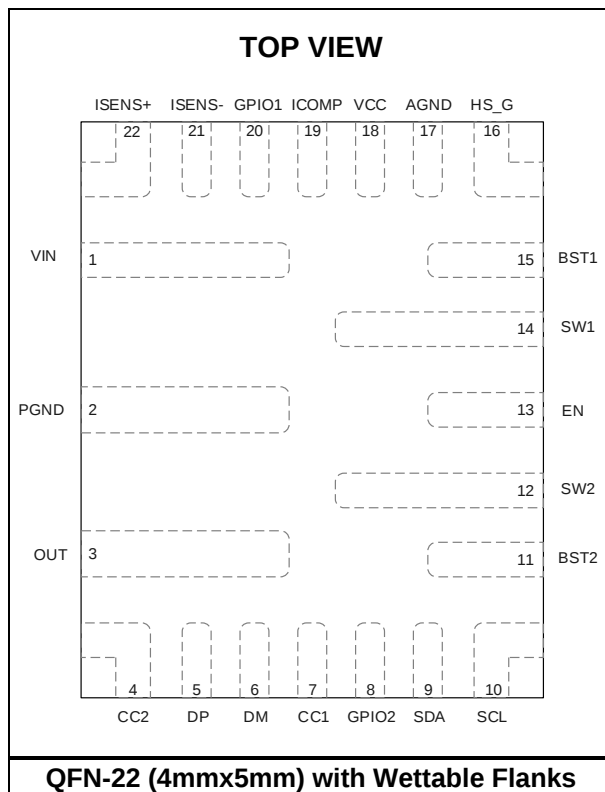
| # | Part Number           | Item                                                                                                     | Quantity |
|---|-----------------------|----------------------------------------------------------------------------------------------------------|----------|
| 1 | EVQ4242B-VE-00A       | The MPQ4242B evaluation board                                                                            | 1        |
| 2 | EVKT-USBI2C-02        | Includes one USB-to-I <sup>2</sup> C communication interface device, one USB cable, and one ribbon cable | 1        |
| 3 | MPQ4242BGVE-0000-AEC1 | The MPQ4242B IC, which can be used for OTP configurations                                                | 2        |

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**Figure 1: EVKT-MPQ4242B Evaluation Kit Set-Up**

## PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin # | Name  | Description                                                                                                                                                                                                                                                                                                                       |
|-------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | VIN   | <b>Supply voltage.</b> The MPQ4242B operates from a 4.8V to 36V unregulated input. An input capacitor ( $C_{IN}$ ) is required to prevent large voltage spikes at the input. Place $C_{IN}$ as close to the IC as possible. The VIN pin is the drain of the internal power device, and it is the power supply for the whole chip. |
| 2     | PGND  | <b>Power ground.</b> Place the PGND pin outside of the $C_{IN}$ and output capacitor ( $C_{OUT}$ ) ground path to prevent switching current spikes. PGND requires extra consideration during the PCB layout. Make the PGND connection with copper traces and vias.                                                                |
| 3     | OUT   | <b>Buck-boost output pin.</b> $C_{OUT}$ is required to prevent large voltage spikes from appearing at the output in buck-boost and boost mode. Place $C_{OUT}$ as close to the IC as possible.                                                                                                                                    |
| 4     | CC2   | <b>Configuration channel (CC).</b> The CC2 pin discovers, configures, and manages connections across a USB Type-C cable.                                                                                                                                                                                                          |
| 5     | DP    | <b>D+ data line to USB connector.</b> The DP pin is the input/output used for handshaking with portable devices. The pin can be trimmed for the ATTACH function. When the DP pin is trimmed as ATTACH, this pin pulls low if the device is attached.                                                                              |
| 6     | DM    | <b>D- data line to USB connector.</b> The DM pin is the input/output used for handshaking with portable devices, and this pin can be trimmed as the FAULT function. When the DM pin is trimmed as FAULT, this pin pulls low if a fault occurs.                                                                                    |
| 7     | CC1   | <b>Configuration Channel (CC).</b> The CC1 pin discovers, configures, and manages connections across a USB Type-C cable.                                                                                                                                                                                                          |
| 8     | GPIO2 | <b>POL</b> <b>USB Type-C polarity indication.</b> The POL pin is an open drain. When CC1 is selected as the CC line, POL pulls low; when CC2 is selected as the CC line, POL is an open drain.                                                                                                                                    |
|       |       | <b>NTC</b> <b>NTC thermal-sense input.</b>                                                                                                                                                                                                                                                                                        |
|       |       | <b>VCONN_IN</b> <b>1W VCONN power supply input.</b>                                                                                                                                                                                                                                                                               |
|       |       | <b>LED_PWM</b> <b>Output for the PWM driver to the LED.</b>                                                                                                                                                                                                                                                                       |
|       |       | <b>ATTACH</b> <b>Output to indicate if the device is attached.</b> The ATTACH pin is active low.                                                                                                                                                                                                                                  |
|       |       | <b>POWER_SHARE2</b> <b>Power sharing 2 input.</b> The POWER_SHARE2 pin is active high. When this pin's voltage exceeds 1.87V, the PD power drops to the PS_PDP_THD setting.                                                                                                                                                       |
| 9     | SDA   | <b>I<sup>2</sup>C data line.</b>                                                                                                                                                                                                                                                                                                  |
| 10    | SCL   | <b>I<sup>2</sup>C clock signal input.</b>                                                                                                                                                                                                                                                                                         |
| 11    | BST2  | <b>Bootstrap 2.</b> Connect a 0.22 $\mu$ F capacitor between the SW2 and BST2 pins to form a floating supply across the high-side switch driver.                                                                                                                                                                                  |
| 12    | SW2   | <b>Switch 2 output.</b> Use a wide PCB trace to make the SW2 connection.                                                                                                                                                                                                                                                          |
| 13    | EN    | <b>Enable control pin.</b> Apply a logic high voltage on the EN pin to enable the IC. Pull EN to logic low to disable the IC. The EN pin has an internal 6 $\mu$ A pull-up.                                                                                                                                                       |
| 14    | SW1   | <b>Switch 1 output.</b> Use a wide PCB trace to make the SW1 connection.                                                                                                                                                                                                                                                          |
| 15    | BST1  | <b>Bootstrap 1.</b> Place a 0.22 $\mu$ F capacitor between the SW1 and BST1 pins to form a floating supply across the high-side switch driver.                                                                                                                                                                                    |
| 16    | HS_G  | <b>High-side gate driver signal for an external N-channel MOSFET.</b>                                                                                                                                                                                                                                                             |
| 17    | AGND  | <b>Analog ground.</b> Connect the AGND pin to PGND.                                                                                                                                                                                                                                                                               |
| 18    | VCC   | <b>Internal 5V LDO regulator output.</b> Decouple the VCC pin with a 2.2 $\mu$ F capacitor.                                                                                                                                                                                                                                       |
| 19    | ICOMP | <b>Compensation pin for the CC current limit loop.</b> Decouple the ICOMP pin with a 470pF capacitor.                                                                                                                                                                                                                             |

## PIN FUNCTIONS *(continued)*

| Pin #          | Name       | Description                                                                                                                                                                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |     |  |  |  |                |   |   |   |   |             |   |   |   |   |                |            |                      |
|----------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|--|--|--|----------------|---|---|---|---|-------------|---|---|---|---|----------------|------------|----------------------|
| 20             | GPIO1      | GATE                                                                                                                                                                               | <b>Gate drive for the external low-side N-channel power MOSFET.</b> The GATE pin is an open-drain structure. GATE pulls low to turn off the power MOSFET when the secondary current limit is triggered. If GATE is not selected, the GND short to V <sub>BATT</sub> detection function is disabled.                                                                                                                                                                                                                                     |     |  |  |  |                |   |   |   |   |             |   |   |   |   |                |            |                      |
|                |            | POWER_SHARE1                                                                                                                                                                       | <b>Power sharing 1 input.</b> The POWER_SHARE1 pin is active low. When this pin's voltage is low, the PD power drops to the value set by PS_PDP_THD.                                                                                                                                                                                                                                                                                                                                                                                    |     |  |  |  |                |   |   |   |   |             |   |   |   |   |                |            |                      |
|                |            | FAULT                                                                                                                                                                              | <b>Fault indication.</b> Open-drain output. If a fault occurs, the FAULT pin pulls low.                                                                                                                                                                                                                                                                                                                                                                                                                                                 |     |  |  |  |                |   |   |   |   |             |   |   |   |   |                |            |                      |
|                |            | NTC2                                                                                                                                                                               | <b>Second NTC detection input.</b> If the NTC2 pin is triggered, PDP reduces its power to the set power share value.                                                                                                                                                                                                                                                                                                                                                                                                                    |     |  |  |  |                |   |   |   |   |             |   |   |   |   |                |            |                      |
|                |            | ATTACH_FLT_ALT                                                                                                                                                                     | <b>Attach and fault indicator.</b> The ATTACH_FLT_ALT pin is an open-drain output. If no fault event has occurred, this pin pulls low for 12μs when a sink plug-in is detected. If a fault occurs, this pin pulls low. See the truth table below for more details. <table><tr><td>Device Plug In</td><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>Fault Event</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>ATTACH_FLT_ALT</td><td>Open drain</td><td>12μs pull-down pulse</td><td>Low</td><td>Low</td></tr></table> |     |  |  |  | Device Plug In | 0 | 1 | 1 | 0 | Fault Event | 0 | 0 | 1 | 1 | ATTACH_FLT_ALT | Open drain | 12μs pull-down pulse |
| Device Plug In | 0          | 1                                                                                                                                                                                  | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 0   |  |  |  |                |   |   |   |   |             |   |   |   |   |                |            |                      |
| Fault Event    | 0          | 0                                                                                                                                                                                  | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 1   |  |  |  |                |   |   |   |   |             |   |   |   |   |                |            |                      |
| ATTACH_FLT_ALT | Open drain | 12μs pull-down pulse                                                                                                                                                               | Low                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Low |  |  |  |                |   |   |   |   |             |   |   |   |   |                |            |                      |
|                |            | IMON                                                                                                                                                                               | <b>Current monitor output.</b> The IMON pin represents the signal between the ISENS+ and ISENS- pins.                                                                                                                                                                                                                                                                                                                                                                                                                                   |     |  |  |  |                |   |   |   |   |             |   |   |   |   |                |            |                      |
| 21             | ISENS-     | <b>Negative node of current-sense signal input.</b> Place a current-sense resistor between the PGND pin and the USB port's GND. Connect the ISENS- pin to the PGND side.           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |     |  |  |  |                |   |   |   |   |             |   |   |   |   |                |            |                      |
| 22             | ISENS+     | <b>Positive node of current-sense signal input.</b> Place a current-sense resistor between the PGND pin and the USB port's GND. Connect the ISENS+ pin to the USB port's GND side. |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |     |  |  |  |                |   |   |   |   |             |   |   |   |   |                |            |                      |

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

|                                                                    |                         |
|--------------------------------------------------------------------|-------------------------|
| Supply voltage ( $V_{IN}$ )                                        | -0.3V to +40V           |
| $V_{HS\_G}$                                                        | -0.3V to $V_{IN} + 12V$ |
| $V_{EN}$                                                           | -0.3V to +40V           |
| $V_{OUT}$ , $V_{CC1}$ , $V_{CC2}$ , $V_{DP}$ , $V_{DM}$            | -0.3V to +24V           |
| $V_{SW1}$                                                          | -0.3V (-5V for <10ns)   |
| to $V_{IN} + 0.3V$ (+43V for <10ns)                                |                         |
| $V_{SW2}$                                                          | -0.3V (-5V for <10ns)   |
| to $V_{OUT} + 0.3V$ (29V for <10ns)                                |                         |
| $V_{BST1}$                                                         | $V_{SW1} + 6.5V$        |
| $V_{BST2}$                                                         | $V_{SW2} + 6.5V$        |
| All other pins                                                     | -0.3V to +5.5V          |
| Continuous power dissipation ( $T_A = 25^\circ C$ ) <sup>(2)</sup> |                         |
| QFN-22 (4mmx5mm)                                                   | 4.55W                   |
| Junction temperature ( $T_J$ )                                     | 150°C                   |
| Lead temperature                                                   | 260°C                   |
| Storage temperature                                                | -65°C to +150°C         |

## ESD Ratings <sup>(3)</sup>

|                                    |       |
|------------------------------------|-------|
| CC1/CC2/DP/DM (HBM) <sup>(4)</sup> | ±8kV  |
| Human body model (HBM)             | ±2kV  |
| Charged-device model (CDM)         | ±750V |

## Recommended Operating Conditions <sup>(5)</sup>

|                                   |                 |
|-----------------------------------|-----------------|
| Supply voltage ( $V_{IN}$ )       | 4.8V to 36V     |
| Output voltage ( $V_{OUT}$ )      | 3.3V to 22.5V   |
| Output current                    | 5A or 100W peak |
| Operating junction temp ( $T_J$ ) | -40°C to +150°C |

| Thermal Resistance              | $\theta_{JA}$ | $\theta_{JC}$ |
|---------------------------------|---------------|---------------|
| EVQ4242B-VE-00A <sup>(6)</sup>  | 27.5          | 5.2           |
| QFN-22 (4mmx5mm) <sup>(7)</sup> | 44            | 9             |

### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature,  $T_J$  (MAX), the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101, AEC specification AECQ100-011. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
- HBM with regard to GND.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on the MPQ4242B test board, 43mmx5mm, 4-layer PCB.
- Measured on a JESD51-7, 4-layer PCB. The value of  $\theta_{JA}$  given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{EN} = \text{floating}$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical value is tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

| Parameter                                              | Symbol                 | Condition                                                                      | Min   | Typ           | Max   | Units       |
|--------------------------------------------------------|------------------------|--------------------------------------------------------------------------------|-------|---------------|-------|-------------|
| Supply current (shutdown)                              | $I_{IN}$               | EN = 0V, $T_J = 25^{\circ}C$                                                   |       | 12            | 20    | $\mu A$     |
|                                                        |                        | EN = 0V, $T_J = -40^{\circ}C$ to $+125^{\circ}C$                               |       | 12            | 80    | $\mu A$     |
| Supply current (standby)                               | $I_{Q\_STB}$           | No device attached, set EN to 1b via the I <sup>2</sup> C, $T_J = 25^{\circ}C$ |       | 150           | 200   | $\mu A$     |
| Supply current (quiescent)                             | $I_{Q\_BB}$            | Buck-boost non-switching, CC attached                                          |       | 4             |       | mA          |
| EN rising threshold                                    | $V_{EN\_RISING}$       |                                                                                | -4%   | 1.3           | +4%   | V           |
| EN hysteresis                                          | $V_{EN\_HYS}$          |                                                                                |       | 100           |       | mV          |
| EN pull-up current                                     | $I_{EN}$               | $V_{EN} = 2V$                                                                  | 3     | 6             | 9     | $\mu A$     |
| Thermal shutdown <sup>(8)</sup>                        | $T_{TSD}$              |                                                                                |       | 175           |       | $^{\circ}C$ |
| Thermal hysteresis <sup>(8)</sup>                      | $T_{TSD\_HYS}$         |                                                                                |       | 20            |       | $^{\circ}C$ |
| $V_{IN}$ under-voltage lockout (UVLO) threshold rising | $V_{IN\_UVLO\_RISING}$ |                                                                                | -4%   | 4.3           | +4%   | V           |
| $V_{IN}$ UVLO threshold hysteresis                     | $V_{IN\_UVLO\_HYS}$    |                                                                                |       | 400           |       | mV          |
| VCC regulator                                          | $V_{CC}$               |                                                                                | 4.75  | 5             | 5.25  | V           |
| VCC load regulation                                    | $V_{CC\_REG}$          | $I_{CC} = 70mA$                                                                |       | 3             |       | %           |
| VBUS_UV falling threshold 1                            | $V_{BUS\_UV1}$         |                                                                                | 2.9   | 3             | 3.1   | V           |
| VBUS_UV falling threshold 2                            | $V_{BUS\_UV2}$         |                                                                                | -3%   | 4.5           | +3%   | V           |
| <b>Buck-Boost Converter</b>                            |                        |                                                                                |       |               |       |             |
| Switch A (SWA) on resistance                           | $R_{DS\_ON\_A}$        |                                                                                |       | 16.3          |       | m $\Omega$  |
| Switch B (SWB) on resistance                           | $R_{DS\_ON\_B}$        |                                                                                |       | 41.5          |       | m $\Omega$  |
| Switch C (SWC) on resistance                           | $R_{DS\_ON\_C}$        |                                                                                |       | 15            |       | m $\Omega$  |
| Switch D (SWD) on resistance                           | $R_{DS\_ON\_D}$        |                                                                                |       | 15.3          |       | m $\Omega$  |
| VHS_G voltage                                          | $V_{HSG}$              |                                                                                |       | $V_{IN} + 10$ |       | V           |
| VHS_G source current <sup>(8)</sup>                    | $I_{HSG}$              |                                                                                |       | 100           |       | $\mu A$     |
| VHS_G pull-down                                        | $R_{HS\_DN}$           |                                                                                |       | 3             | 6.5   | $\Omega$    |
| Output voltage                                         | $V_{OUT0}$             |                                                                                | -3%   | 3.3           | +3%   | V           |
|                                                        | $V_{OUT1}$             |                                                                                | -2%   | 5             | +2%   | V           |
|                                                        | $V_{OUT2}$             |                                                                                | -1.5% | 9             | +1.5% | V           |
|                                                        | $V_{OUT3}$             |                                                                                | -1.5% | 20            | +1.5% | V           |
| Output over-voltage protection (OVP)                   | $V_{OVP}$              |                                                                                |       | 114           |       | %           |
| OVP recovery hysteresis                                | $V_{OVP\_HYS}$         |                                                                                |       | 10            |       | %           |
| Input OVP                                              | $V_{IN\_OVP}$          | OTP trim option                                                                | 21.4  | 22.4          | 23.4  | V           |
| Input OVP recovery hysteresis                          | $V_{OVP\_HYS}$         | OTP trim option                                                                |       | 2             |       | V           |
| Switch leakage                                         | SWLKG                  | $V_{EN} = 0V$ , $V_{SW} = 36V$ , $T_J = 25^{\circ}C$                           |       |               | 1000  | nA          |
|                                                        |                        | $V_{EN} = 0V$ , $V_{SW} = 36V$ , $T_J = -40^{\circ}C$ to $+125^{\circ}C$       |       |               | 80    | $\mu A$     |

## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{EN} = \text{floating}$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical value is tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

| Parameter                                               | Symbol           | Condition                                                                                                                 | Min  | Typ      | Max  | Units      |
|---------------------------------------------------------|------------------|---------------------------------------------------------------------------------------------------------------------------|------|----------|------|------------|
| Line drop compensation                                  | $V_{LDC}$        | Set LINE_DROP_COMP to 01b via the I <sup>2</sup> C, $V_{OUT} = 5V$ , $I_{OUT} = 3A$ (only enabled when $V_{OUT} > 4.9V$ ) |      | 150      |      | mV         |
| ISENS over-current (OC) threshold                       | $I_{OC1}$        | OC threshold = 1A, $R_{SENS} = 10m\Omega$                                                                                 | 9    | 10       | 11   | mV         |
|                                                         | $I_{OC2}$        | OC threshold = 3A, $R_{SENS} = 10m\Omega$ , $T_J = 25^{\circ}C$                                                           | 29   | 30       | 31.5 | mV         |
|                                                         |                  | OC threshold = 3A, $R_{SENS} = 10m\Omega$ , $T_J = -40^{\circ}C$ to $+150^{\circ}C$                                       | 28.5 | 30       | 32.5 | mV         |
| SWA current limit                                       | $I_{LIMIT1}$     | Switch A, boost mode                                                                                                      |      | 20       |      | A          |
| SWB valley limit                                        | $I_{LIMIT2}$     | Switch B, buck mode                                                                                                       |      | 6.7      |      | A          |
| Oscillator frequency                                    | $f_{SW1}$        | Set FREQ to 00b via the I <sup>2</sup> C                                                                                  | 200  | 250      | 300  | kHz        |
|                                                         | $f_{SW2}$        | Set FREQ to 01b via the I <sup>2</sup> C                                                                                  | 350  | 420      | 490  | kHz        |
| Frequency dithering span                                | $f_{DITH\_SPAN}$ | Set FREQ to 01b via the I <sup>2</sup> C                                                                                  |      | $\pm 11$ |      | %          |
| Minimum on time <sup>(8)</sup>                          | $t_{ON\_MIN}$    | Buck SWC                                                                                                                  |      | 80       |      | ns         |
| Minimum off time <sup>(8)</sup>                         | $t_{OFF\_MIN}$   | Buck SWB                                                                                                                  |      | 60       |      | ns         |
| Soft-start time                                         | $t_{SS}$         | 5V output from 10% to 90%, constant slew rate for other $V_{OUT}$                                                         | 0.5  | 1.1      | 1.7  | ms         |
| Output discharge resistance                             | $R_{DIS\_OUT}$   |                                                                                                                           |      | 320      |      | $\Omega$   |
| <b>Mode Transition Threshold</b>                        |                  |                                                                                                                           |      |          |      |            |
| Buck to buck-boost transition threshold <sup>(8)</sup>  | $V_{MODE\_TH1}$  | $V_{OUT} / V_{IN}$                                                                                                        |      | 92       |      | %          |
| Boost to buck-boost transition threshold <sup>(8)</sup> | $V_{MODE\_TH2}$  | $V_{IN} / V_{OUT}$                                                                                                        |      | 90       |      | %          |
| <b>Ground N-Channel MOSFET Gate Driver</b>              |                  |                                                                                                                           |      |          |      |            |
| GND short to battery threshold                          | $V_{RGND}$       | $R_{SENS} = 10m\Omega$                                                                                                    |      | 135      |      | mV         |
| Short to battery retry delay <sup>(8)</sup>             | $t_{SBP}$        |                                                                                                                           |      | 1        |      | s          |
| Gate pull-down resistance                               | $R_{PD}$         |                                                                                                                           |      | 20       | 45   | $\Omega$   |
| <b>NTC, NTC2</b>                                        |                  |                                                                                                                           |      |          |      |            |
| External thermal sense triggering voltage               | $V_{NTC\_ETY}$   | $R_P = 43.2k\Omega$ , $R_{NTC} = 4.79k\Omega$ (100°C)                                                                     | 8%   | 10%      | 12%  | $V_{CC}$   |
| External thermal sense recovery voltage 1               | $V_{NTC\_RCY1}$  | Set NTC_HYSTERESIS to 0b via the I <sup>2</sup> C                                                                         |      | 20%      |      | $V_{CC}$   |
| External thermal sense recovery voltage 2               | $V_{NTC\_RCY2}$  | Set NTC_HYSTERESIS to 1b via the I <sup>2</sup> C                                                                         |      | 30%      |      | $V_{CC}$   |
| <b>GPIO1</b>                                            |                  |                                                                                                                           |      |          |      |            |
| Power share input high                                  | $V_{IH\_PS}$     |                                                                                                                           | 2    |          |      | V          |
| Power share input low                                   | $V_{IL\_PS}$     |                                                                                                                           |      |          | 0.8  | V          |
| Power share pull-up resistance                          | $I_{LK\_PS}$     | 5V pull-up                                                                                                                |      | 1        |      | M $\Omega$ |
| Fault pull-down resistance                              | $R_{PD\_FAULT}$  |                                                                                                                           |      | 20       | 45   | $\Omega$   |
| Fault leakage                                           | $I_{LK\_FAULT}$  |                                                                                                                           |      |          | 3    | $\mu A$    |

## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{EN} = \text{floating}$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical value is tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

| Parameter                                                      | Symbol                  | Condition                                        | Min  | Typ  | Max  | Units      |
|----------------------------------------------------------------|-------------------------|--------------------------------------------------|------|------|------|------------|
| <b>GPIO2</b>                                                   |                         |                                                  |      |      |      |            |
| POL pull-down resistance                                       | $R_{PD\_POL}$           | Connect CC1 to GND with a 5.1k $\Omega$ resistor |      |      | 45   | $\Omega$   |
| POL leakage                                                    | $I_{LK\_POL}$           | Connect CC2 to GND with a 5.1k $\Omega$ resistor |      |      | 3    | $\mu A$    |
| LED PWM output FREQ                                            | $f_{LED}$               |                                                  | 21   | 24   | 27   | kHz        |
| LED_PWM output duty                                            | $D_{LED}$               |                                                  |      | 50   |      | %          |
| Connected output                                               | $V_{ATTO}$              | USB Type-C connected, force 50 $\mu A$           |      |      | 0.4  | V          |
| Power share input threshold                                    | $V_{TH\_PS}$            |                                                  | 1.52 | 1.87 | 2.22 | V          |
| <b>USB Charging Mode Identification</b>                        |                         |                                                  |      |      |      |            |
| <b>BC1.2 DCP Mode</b>                                          |                         |                                                  |      |      |      |            |
| DP and DM short resistance                                     | $R_{DP\_DM\_SHORT}$     | $V_{DP} = 0.8V$ , $I_{DM} = 1mA$                 |      | 30   | 70   | $\Omega$   |
| <b>Divider Mode</b>                                            |                         |                                                  |      |      |      |            |
| DP output voltage                                              | $V_{DIVIDER\_DP}$       | $V_{OUT} = 5V$                                   | 2.5  | 2.7  | 2.9  | V          |
| DM output voltage                                              | $V_{DIVIDER\_DM}$       | $V_{OUT} = 5V$                                   | 3.05 | 3.3  | 3.55 | V          |
| DP output impedance                                            | $R_{DIVIDER\_DP}$       |                                                  |      | 23   |      | k $\Omega$ |
| DM output impedance                                            | $R_{DIVIDER\_DM}$       |                                                  |      | 17   |      | k $\Omega$ |
| <b>1.2V/1.2V Mode</b>                                          |                         |                                                  |      |      |      |            |
| DP/DM output voltage                                           | $V_{DP\_DM\_1.2V}$      | $V_{OUT} = 5V$                                   | 1.15 | 1.25 | 1.35 | V          |
| DP/DM output impedance                                         | $R_{DP\_DM\_1.2V}$      |                                                  |      | 75   |      | k $\Omega$ |
| <b>Quick Charge 3.0 Mode</b>                                   |                         |                                                  |      |      |      |            |
| DP/DM low voltage                                              | $V_{QC\_LOW}$           |                                                  | 0.2  | 0.3  | 0.4  | V          |
| DP/DM high voltage                                             | $V_{QC\_HIGH}$          |                                                  | 1.8  | 2    | 2.2  | V          |
| QC mode entry voltage glitch time (QC identify) <sup>(8)</sup> | $t_{QC\_GLITCH}$        |                                                  |      | 1000 |      | ms         |
| DP output impedance                                            | $R_{DP\_QC}$            |                                                  |      | 350  |      | k $\Omega$ |
| DM output impedance                                            | $R_{DM\_QC}$            |                                                  |      | 20   |      | k $\Omega$ |
| Request voltage time <sup>(8)</sup>                            | $t_{V\_NEW\_REQUEST}$   |                                                  | 200  |      |      | ms         |
| Output voltage change glitch time <sup>(8)</sup>               | $t_{GLITCH\_V\_CHANGE}$ |                                                  | 20   |      | 60   | ms         |
| Unplug $V_{BUS}$ discharge time <sup>(8)</sup>                 | $t_{VBUS\_DISC\_QC}$    |                                                  |      |      | 500  | ms         |
| <b>Charging Downstream Port (CDP) Mode</b>                     |                         |                                                  |      |      |      |            |
| DM CDP output voltage                                          | $V_{DM\_SRC}$           | $V_{DP} = 0.6V$ , DM sink = 250 $\mu A$          | 0.5  | 0.6  | 0.7  | V          |
| DP rising lower window threshold for $V_{DM\_SRC}$ EN          | $V_{DAT\_REF}$          |                                                  | 0.25 | 0.35 | 0.45 | V          |
| DP rising lower window threshold hysteresis                    | $V_{DAT\_REF\_HYS}$     |                                                  |      | 30   |      | mV         |
| DP rising upper window threshold for $V_{DM\_SRC}$             | $V_{LGC\_SRC}$          |                                                  | 0.8  | 0.9  | 1    | V          |
| DP rising upper window threshold hysteresis                    | $V_{LGC\_SRC\_HYS}$     |                                                  |      | 50   |      | mV         |

## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{EN} = \text{floating}$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical value is tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

| Parameter                                           | Symbol             | Condition                                                   | Min  | Typ | Max  | Units      |
|-----------------------------------------------------|--------------------|-------------------------------------------------------------|------|-----|------|------------|
| <b>FCP Mode</b>                                     |                    |                                                             |      |     |      |            |
| DM Tx high voltage <sup>(8)</sup>                   | $V_{FCPT\_H}$      | $R_{LOAD} = 15k\Omega$                                      | 2.55 |     | 5    | V          |
| DM Tx low voltage <sup>(8)</sup>                    | $V_{FCPT\_L}$      | $R_{LOAD} = 15k\Omega$                                      |      |     | 0.4  | V          |
| DM Rx high voltage                                  | $V_{FCPR\_H}$      |                                                             | 1.5  |     | 5    | V          |
| DM Rx low voltage                                   | $V_{FCPR\_L}$      |                                                             |      |     | 1    | V          |
| DM pull-low resistance                              | $R_{LD\_D-}$       |                                                             |      | 15  |      | k $\Omega$ |
| Unit interval of PHY <sup>(8)</sup>                 | UI                 |                                                             | 144  | 160 | 176  | $\mu s$    |
| <b>USB Type-C (CC1 and CC2 Pins)</b>                |                    |                                                             |      |     |      |            |
| CC pull-up current 1 <sup>(8)</sup>                 | $I_{RP1}$          | $V_{BUS} = 5V @ 3A$ , $T_J = 0^{\circ}C$ to $85^{\circ}C$   | -8%  | 330 | +8%  | $\mu A$    |
| CC pull-up current 2 <sup>(8)</sup>                 | $I_{RP2}$          | $V_{BUS} = 5V @ 1.5A$ , $T_J = 0^{\circ}C$ to $85^{\circ}C$ | -8%  | 180 | +8%  | $\mu A$    |
| CC voltage to enable VCONN for 3A USB Type-C mode   | $V_{RA1}$          |                                                             |      |     | 0.75 | V          |
| CC voltage to enable VBUS for 3A USB Type-C mode    | $V_{RD1}$          |                                                             | 0.85 |     | 2.45 | V          |
| CC disconnect threshold for 3A USB Type-C mode      | $V_{OPEN1}$        |                                                             | 2.75 |     |      | V          |
| CC voltage to enable VCONN for 1.5A USB Type-C mode | $V_{RA2}$          |                                                             |      |     | 0.35 | V          |
| CC voltage to enable VBUS for 1.5A USB Type-C mode  | $V_{RD2}$          |                                                             | 0.45 |     | 1.5  | V          |
| CC disconnect threshold for 1.5A USB Type-C mode    | $V_{OPEN2}$        |                                                             | 1.7  |     |      | V          |
| CC voltage falling de-bounce timer                  | $t_{CC\_DEBOUNCE}$ | VBUS enable deglitch                                        | 100  | 150 | 200  | ms         |
| CC voltage rising de-bounce timer                   | $t_{PD\_DEBOUNCE}$ | VBUS disable deglitch                                       | 5    | 10  | 15   | ms         |
| 100mW VCONN output power                            | $P_{VCONN\_100mW}$ | Default                                                     | 100  |     |      | mW         |
| 1W VCONN output power                               | $P_{VCONN\_1W}$    | Set GPIO2 to 011b via the I <sup>2</sup> C                  | 1    |     |      | W          |
| <b>USB PD</b>                                       |                    |                                                             |      |     |      |            |
| Unit interval time <sup>(8)</sup>                   | $t_{UI}$           |                                                             | 3.03 |     | 3.7  | $\mu s$    |
| <b>Transmitter</b>                                  |                    |                                                             |      |     |      |            |
| End drive BMC time <sup>(8)</sup>                   | $t_{EDBMC}$        |                                                             |      |     | 23   | $\mu s$    |
| Falling time <sup>(8)</sup>                         | $t_{FALL}$         |                                                             | 300  | 400 |      | ns         |
| Rising time <sup>(8)</sup>                          | $t_{RISE}$         |                                                             | 300  | 400 |      | ns         |
| Hold low BMC time <sup>(8)</sup>                    | $t_{HLBMC}$        |                                                             | 1    |     |      | $\mu s$    |
| Logic high voltage                                  | $V_{LH}$           |                                                             | 1.05 |     | 1.2  | V          |
| Logic low voltage                                   | $V_{LL}$           |                                                             |      |     | 70   | mV         |
| Output impedance                                    | $Z_{TX}$           |                                                             |      | 45  |      | $\Omega$   |
| <b>Receiver <sup>(8)</sup></b>                      |                    |                                                             |      |     |      |            |
| CC receiver capacitance                             | $C_{RECEIVER}$     |                                                             |      |     | 600  | pF         |
| Transitions for signal detection                    | $N_{TRANSITION}$   |                                                             | 3    |     |      | Edges      |

## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{EN} = \text{floating}$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical value is tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

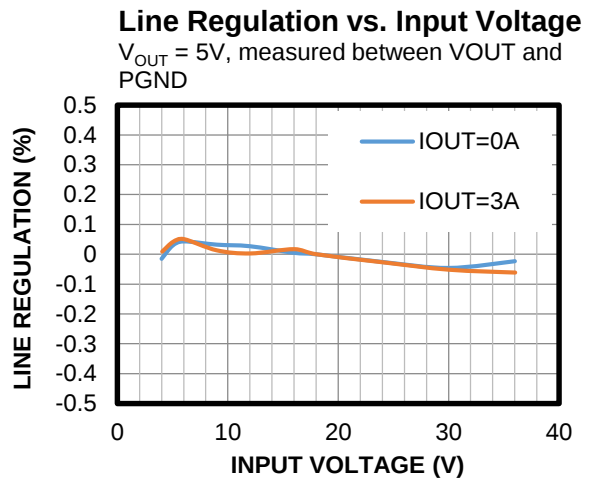
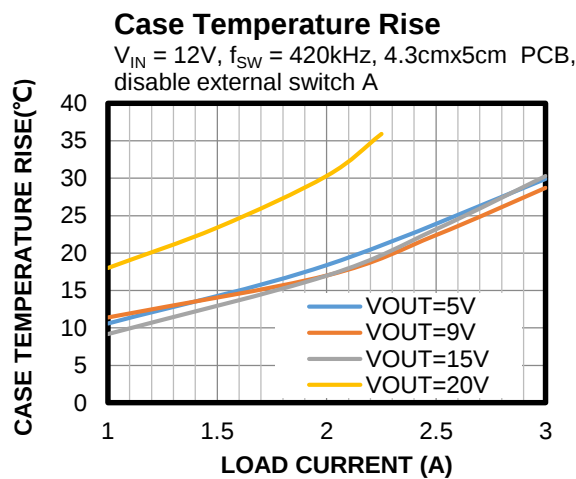
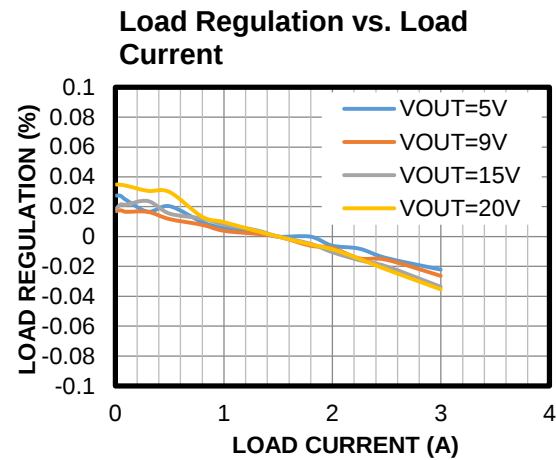
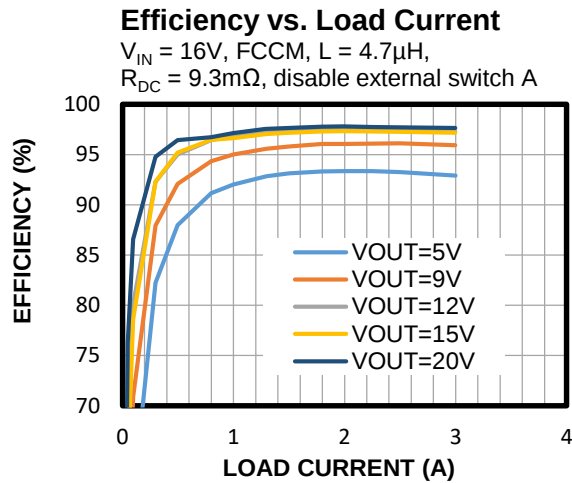
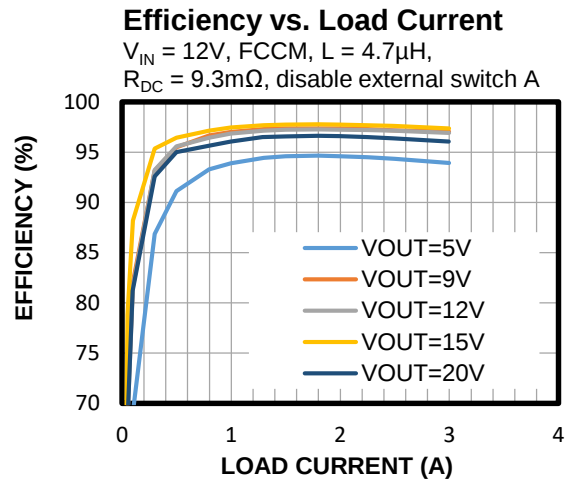
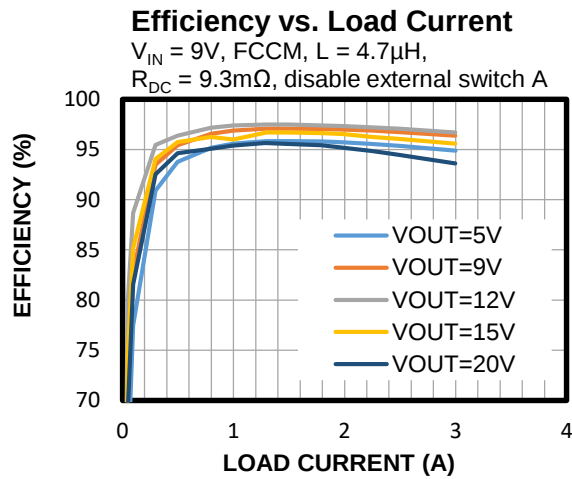
| Parameter                                                     | Symbol                   | Condition                                      | Min  | Typ | Max  | Units      |
|---------------------------------------------------------------|--------------------------|------------------------------------------------|------|-----|------|------------|
| Rx bandwidth limiting filter                                  | $t_{RX\_FILTER}$         |                                                | 100  |     |      | ns         |
| Time window for detecting non-idle                            | $t_{TRANSITION\_WINDOW}$ |                                                | 12   |     | 20   | $\mu s$    |
| Receiver input impedance                                      | $Z_{BMC\_RX}$            |                                                | 1    |     |      | M $\Omega$ |
| <b>I<sup>2</sup>C Interface Specifications</b> <sup>(8)</sup> |                          |                                                |      |     |      |            |
| Input logic high                                              | $V_{IH}$                 | I <sup>2</sup> C pull-up VDD can be 1.8V to 5V | 1.26 |     |      | V          |
| Input logic low                                               | $V_{IL}$                 |                                                |      |     | 0.54 | V          |
| Output voltage logic low                                      | $V_{OUT\_L}$             |                                                |      |     | 0.45 | V          |
| SCL clock frequency                                           | $f_{SCL}$                |                                                |      | 400 |      | kHz        |
| SCL high time                                                 | $t_{HIGH}$               |                                                | 60   |     |      | ns         |
| SCL low time                                                  | $t_{LOW}$                |                                                | 160  |     |      | ns         |
| Data set-up time                                              | $t_{SU\_DAT}$            |                                                | 10   |     |      | ns         |
| Data hold time                                                | $t_{HD\_DAT}$            |                                                |      | 70  |      | ns         |
| Set-up time for repeated start command                        | $t_{SU\_STA}$            |                                                | 160  |     |      | ns         |
| Hold time for repeated start command                          | $t_{HD\_STA}$            |                                                | 160  |     |      | ns         |
| Bus free time between a start and a stop command              | $t_{BUF}$                |                                                | 160  |     |      | ns         |
| Set-up time for stop command                                  | $t_{SU\_STO}$            |                                                | 160  |     |      | ns         |
| Rising time of SCL and SDA                                    | $t_R$                    |                                                | 10   |     | 300  | ns         |
| Falling time of SCL and SDA                                   | $t_F$                    |                                                | 10   |     | 300  | ns         |
| Pulse width of suppressed spike                               | $t_{SP}$                 |                                                | 0    |     | 50   | ns         |
| Capacitance bus for each bus line                             | $C_B$                    |                                                |      |     | 400  | pF         |
| SCL low time                                                  | $t_{LOW}$                |                                                | 160  |     |      | ns         |

### Note:

8) Guaranteed by characterization sample test.

# TYPICAL CHARACTERISTICS

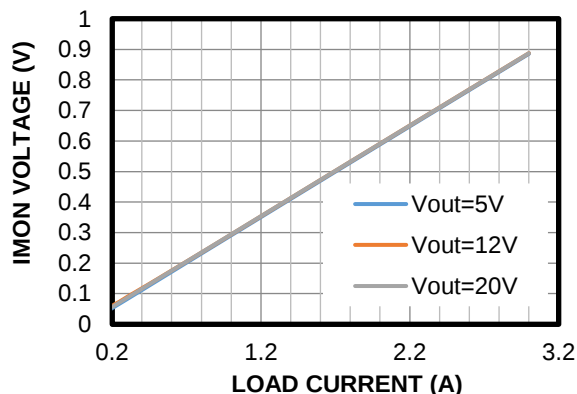
$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



# TYPICAL CHARACTERISTICS (continued)

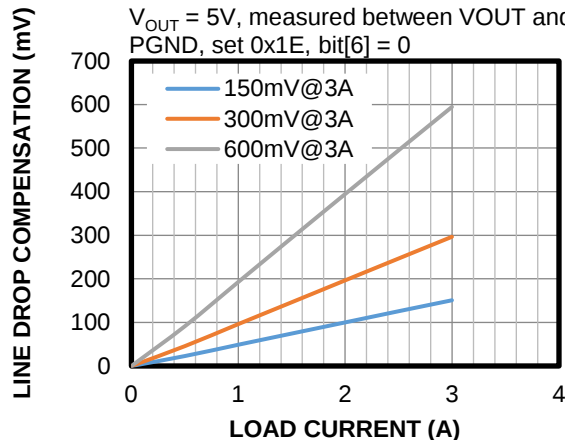
$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

## IMON Voltage vs. Load Current



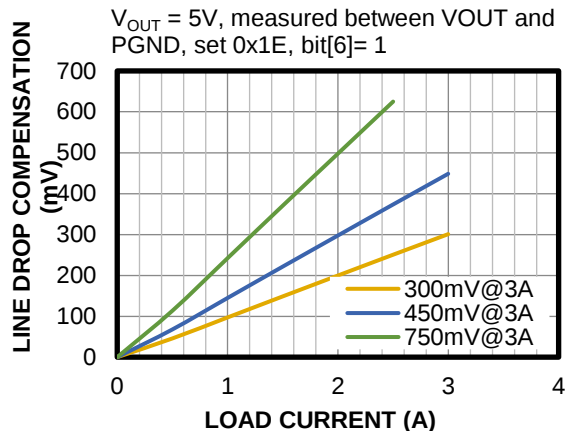
## Line Drop Compensation vs. Load Current

$V_{OUT} = 5V$ , measured between VOUT and PGND, set 0x1E, bit[6] = 0



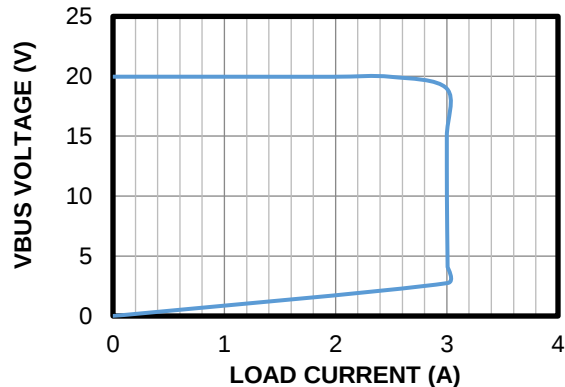
## Line Drop Compensation vs. Load Current

$V_{OUT} = 5V$ , measured between VOUT and PGND, set 0x1E, bit[6] = 1



## VBUS Voltage vs. Load Current

CC limit = 3A

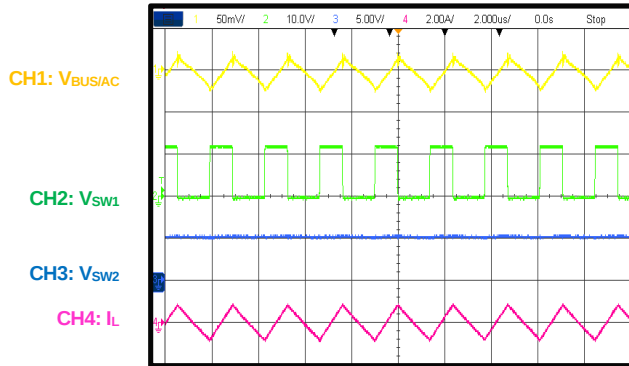


# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

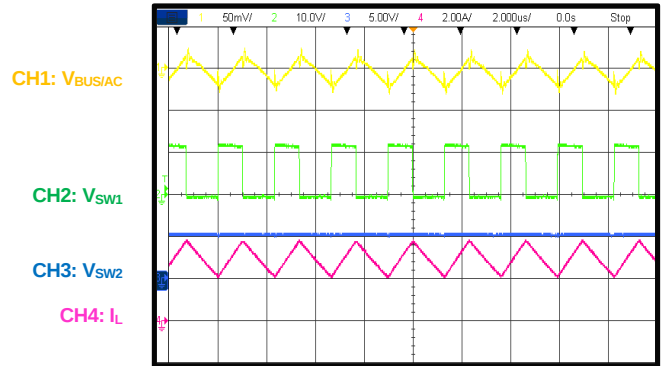
## Output Voltage Ripple

$V_{BUS} = 5V$ , load = 0A



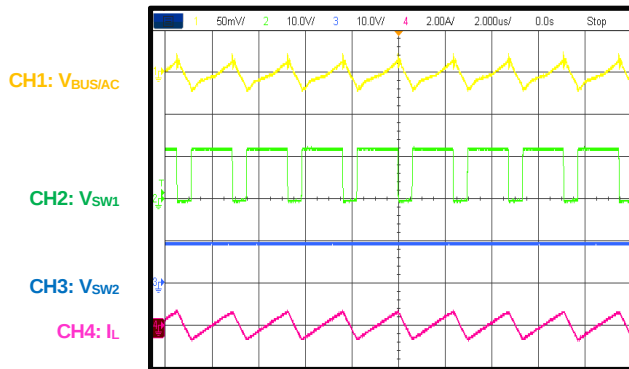
## Output Voltage Ripple

$V_{BUS} = 5V$ , load = 3A



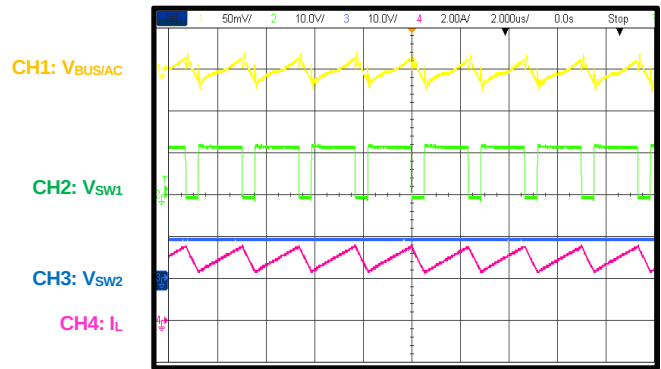
## Output Voltage Ripple

$V_{BUS} = 9V$ , load = 0A



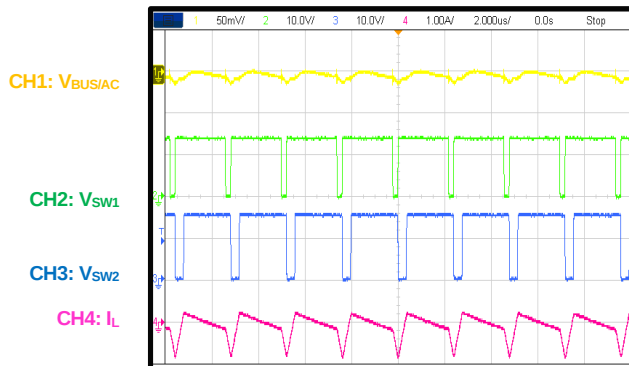
## Output Voltage Ripple

$V_{BUS} = 9V$ , load = 3A



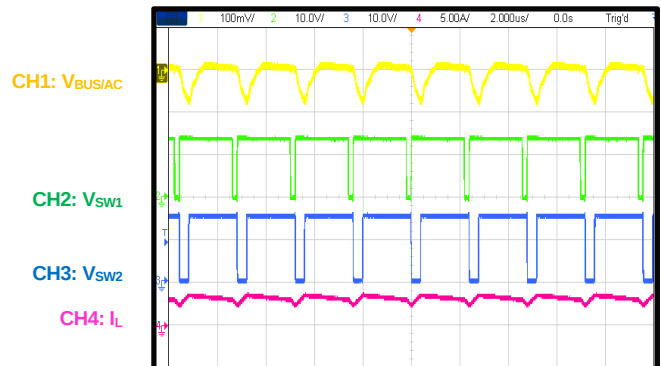
## Output Voltage Ripple

$V_{IN} = 14V$ ,  $V_{BUS} = 15V$ , load = 0A



## Output Voltage Ripple

$V_{IN} = 14V$ ,  $V_{BUS} = 15V$ , load = 3A

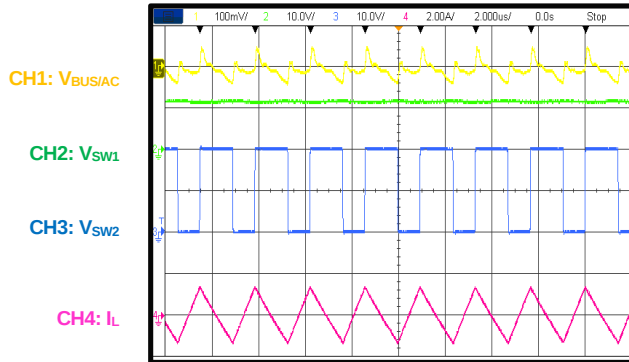


# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

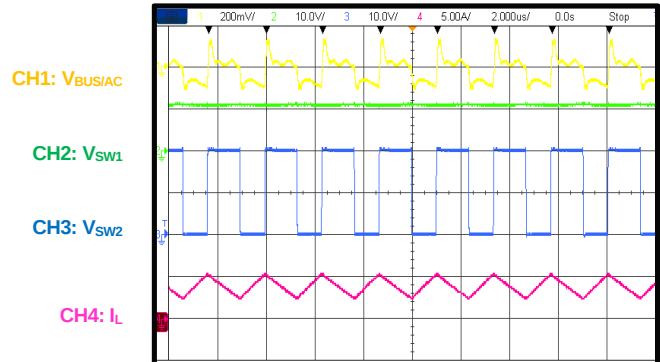
## Output Voltage Ripple

$V_{BUS} = 20V$ , load = 0A



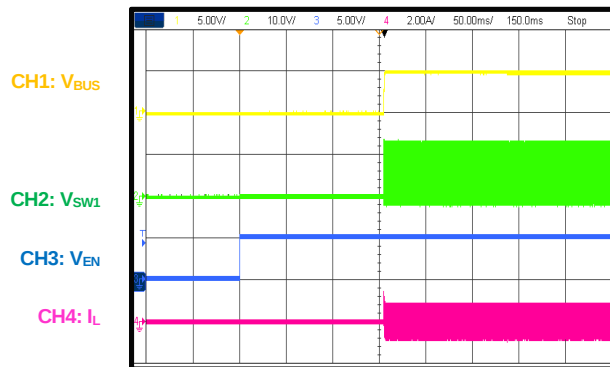
## Output Voltage Ripple

$V_{BUS} = 20V$ , load = 2.25A



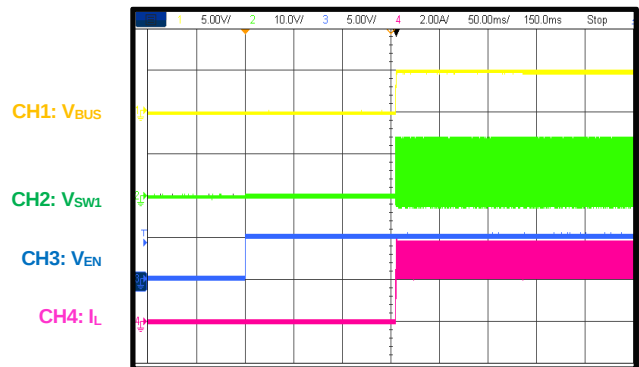
## EN Pin Enabled

CC1 connected to a 5.1kΩ  $R_D$  resistor,  
load = 0A



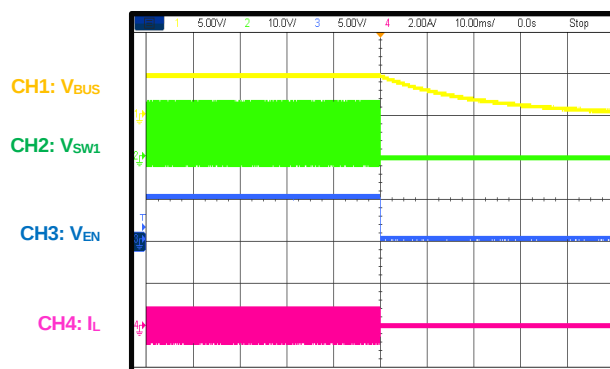
## EN Pin Enabled

CC1 connected to a 5.1kΩ  $R_D$  resistor,  
load = 3A



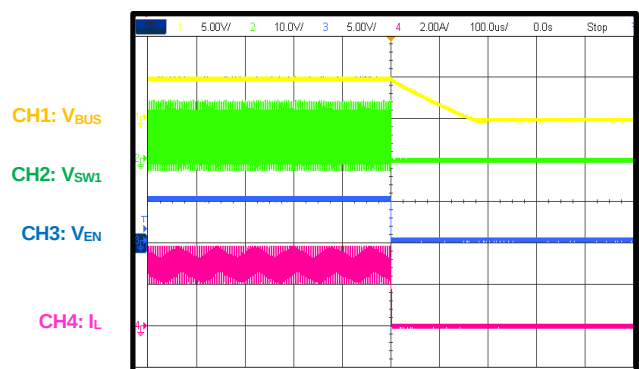
## EN Pin Disabled

CC1 connected to a 5.1kΩ  $R_D$  resistor,  
load = 0A



## EN Pin Disabled

CC1 connected to a 5.1kΩ  $R_D$  resistor,  
load = 3A

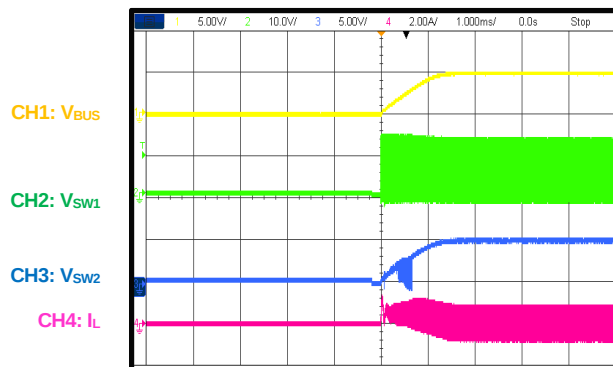


# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

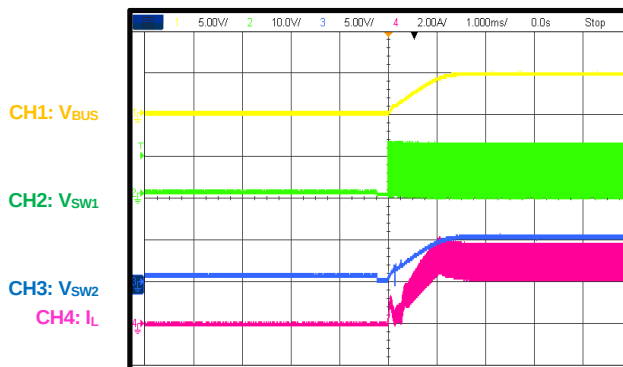
## Input Start-Up

Load = 0A, CC1 connected to a 5.1k $\Omega$   $R_D$  resistor



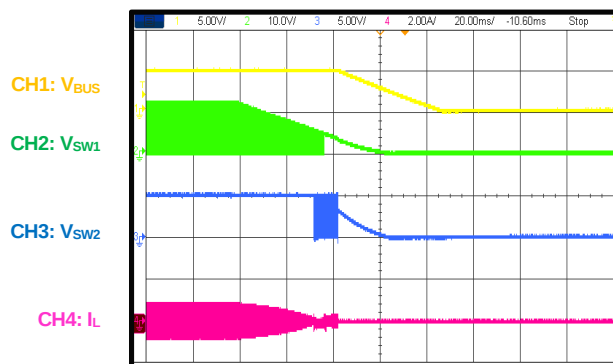
## Input Start-Up

Load = 3A, CC1 connected to a 5.1k $\Omega$   $R_D$  resistor



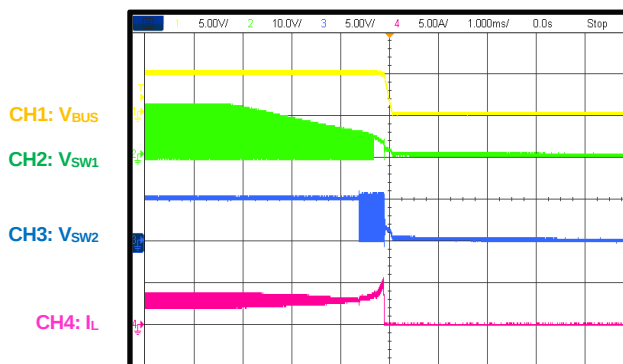
## Input Shutdown

Load = 10mA

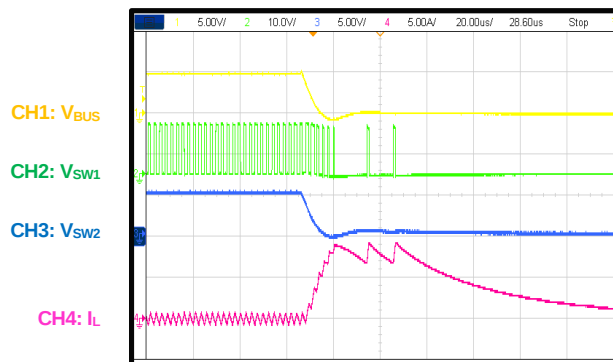


## Input Shutdown

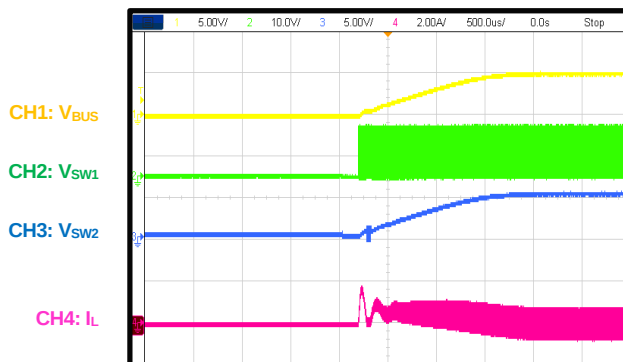
Load = 3A



## SCP Entry



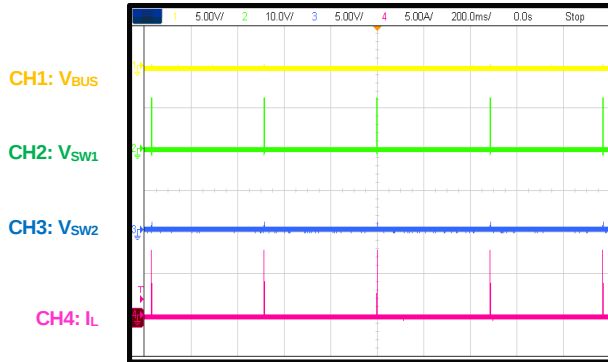
## SCP Recovery



# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

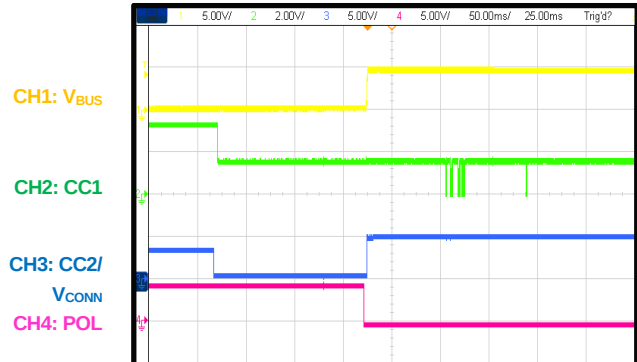
$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

## SCP Steady State



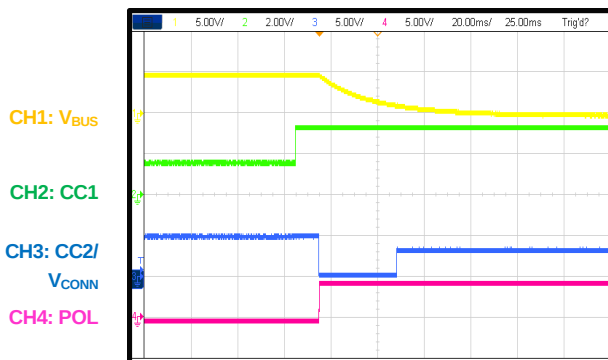
## CC1 Connected to $R_D$ to Enable VBUS

$I_{OUT} = 0A$ , CC2 connected to a  $1k\Omega R_A$  resistor



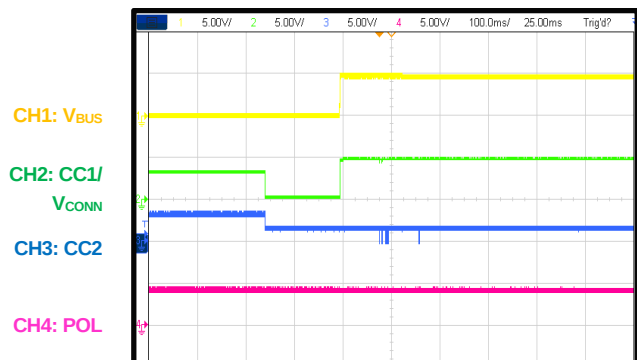
## CC1 Disconnected from $R_D$ to Disable VBUS

$I_{OUT} = 0A$ , CC2 connected to a  $1k\Omega R_A$  resistor



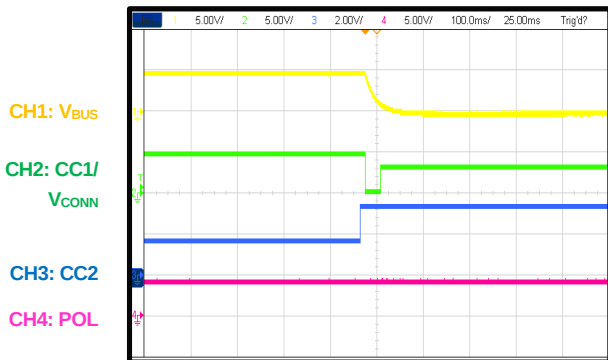
## CC2 Connected to $R_D$ to Enable VBUS

$I_{OUT} = 0A$ , CC1 connected to a  $1k\Omega R_A$  resistor



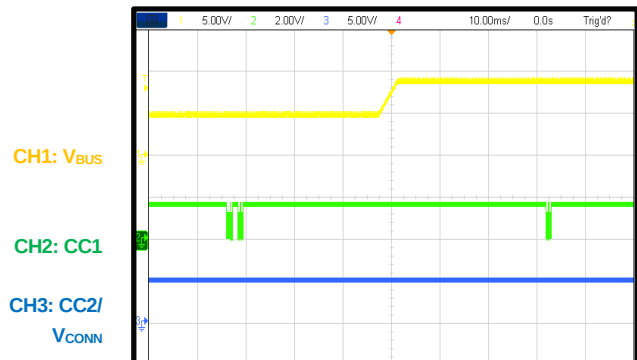
## CC2 Disconnected from $R_D$ to Disable VBUS

$I_{OUT} = 0A$ , CC1 connected to  $1k\Omega R_A$  resistor



## PDO Transition

5V PDO to 9V PDO



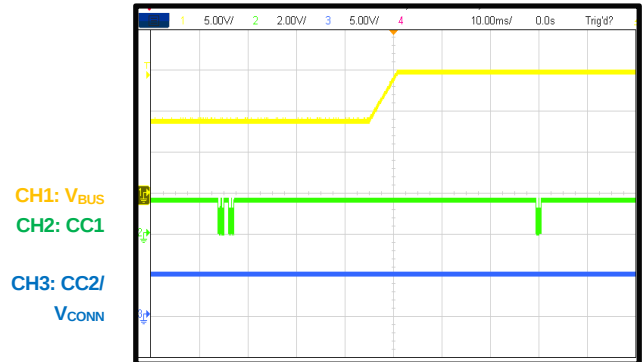
# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**PDO Transition**  
9V PDO to 5V PDO



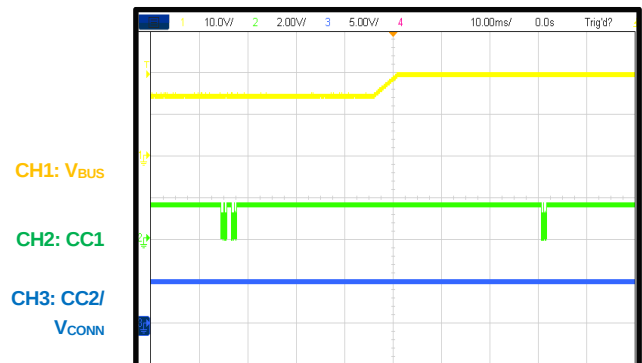
**PDO Transition**  
9V PDO to 15V PDO



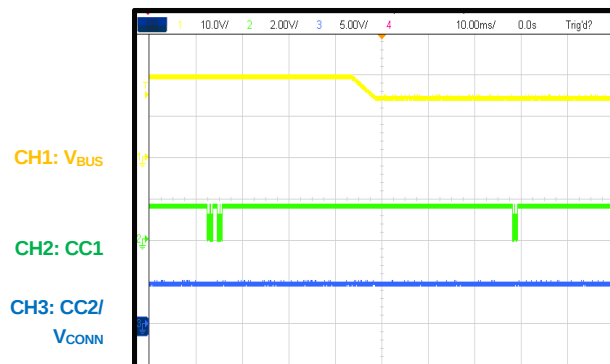
**PDO Transition**  
15V PDO to 9V PDO



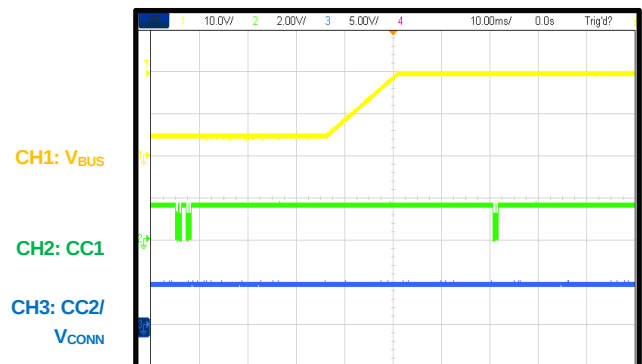
**PDO Transition**  
15V PDO to 20V PDO



**PDO Transition**  
20V PDO to 15V PDO



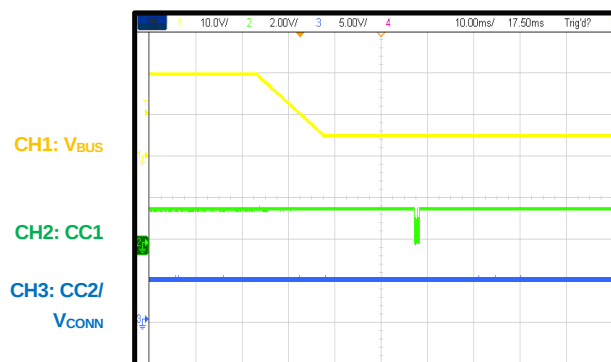
**PDO Transition**  
5V PDO to 20V PDO



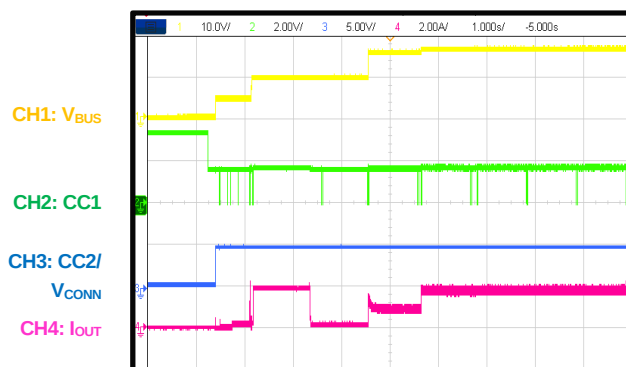
# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

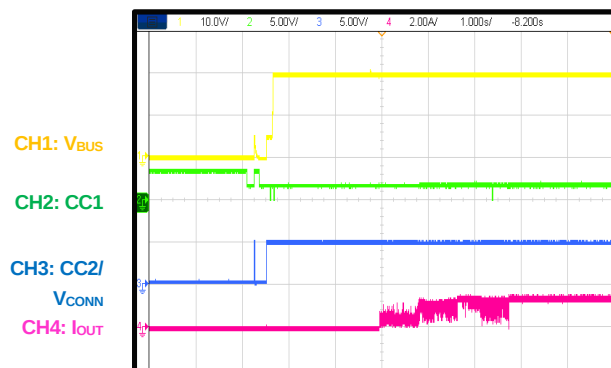
**PDO Transition**  
20V PDO to 5V PDO



**Mobile Phone Charging Test**  
Phone requests 3.3V to 21V APDO

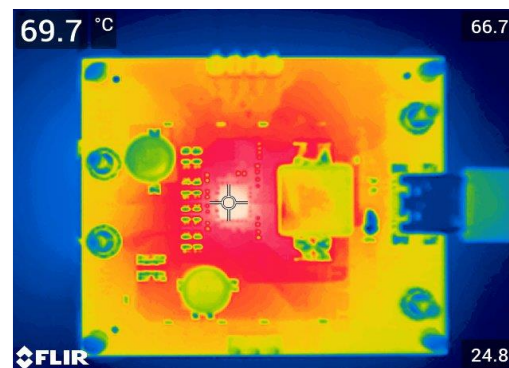


**Laptop Charging Test**  
Laptop requests 20V PDO



**Thermal Image**

$V_{IN} = 13.5V$ ,  $V_{OUT} = 20V$ ,  $I_{OUT} = 3A$ ,  
 $f_{SW} = 420kHz$ , 4.3cmx5cm PCB,  
top/bottom layer: 2oz; mid-layer 1 and 2: 1oz,  
enable external switch A



# FUNCTIONAL BLOCK DIAGRAM

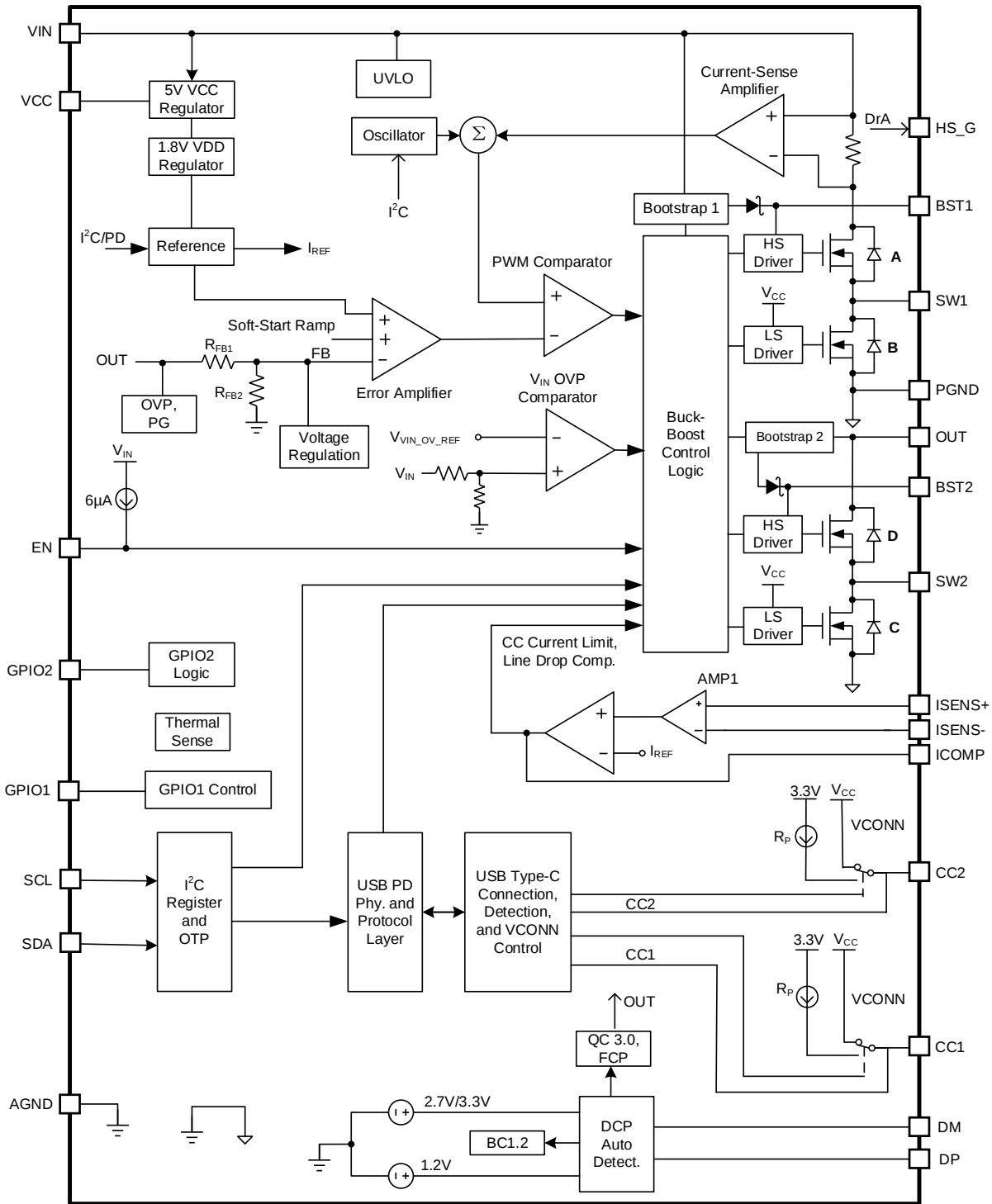


Figure 2: Functional Block Diagram

## OPERATION

The MPQ4242B is a buck-boost converter with four integrated switches and USB charging protocols. The buck-boost converter works in current mode, which provides a fast transient response for buck, boost, and buck-boost modes. One special buck-boost control strategy provides high efficiency across the full input range and smooths transitions between different modes. Figure 2 on page 21 shows the internal block diagram.

### Pulse-Width Modulation (PWM) Operation

The MPQ4242B operates in a fixed-frequency peak current mode control to regulate the output voltage ( $V_{OUT}$ ). The internal clock initiates the pulse-width modulation (PWM) cycle and turns on the related power switch. The switch remains on until its current reaches the value set by the COMP voltage ( $V_{COMP}$ ). When the power switch is off, it remains off until the next clock cycle starts. The switching frequency ( $f_{SW}$ ) can be configured to 250kHz or 420kHz via the I<sup>2</sup>C.

### Buck-Boost Operation

The MPQ4242B can regulate  $V_{OUT}$  to be above, below, or equal to the input voltage ( $V_{IN}$ ). Figure 3 shows a buck-boost power structure with one inductor and four switches (SWA, SWB, SWC, and SWD).

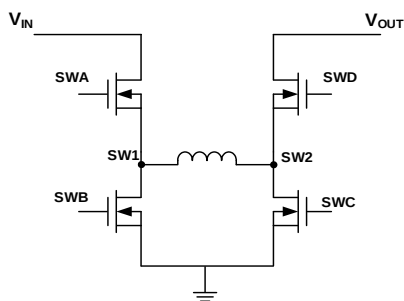


Figure 3: Buck-Boost Topology

Buck mode, boost mode, and buck-boost mode can have different  $V_{IN}$  inputs (see Figure 4).

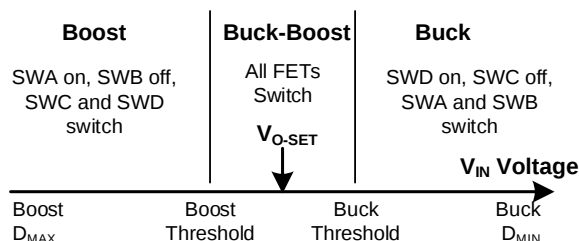


Figure 4: Buck-Boost Operation Range

### Buck Mode ( $V_{IN} > V_{OUT}$ )

When  $V_{IN}$  exceeds  $V_{OUT}$ , the MPQ4242B works in buck mode. In buck mode, switch A (SWA) and switch B (SWB) switch for buck regulation. Meanwhile, switch C (SWC) is off, and switch D (SWD) stays on to conduct the inductor current ( $I_L$ ).

SWA works with a peak current mode control logic, and SWB turns on until  $t_{CLK}$  times out. In each buck mode cycle, SWA turns on to charge  $I_L$ . When  $I_L$  reaches the value set by  $V_{COMP}$ , SWA turns off and SWB turns on. SWB stays on until the next clock begins. Then SWA turns on and the cycle repeats. The COMP signal is the error amplifier (EA) output from the  $V_{OUT}$  feedback and the internal FB reference voltage. Figure 5 shows the buck mode waveform.

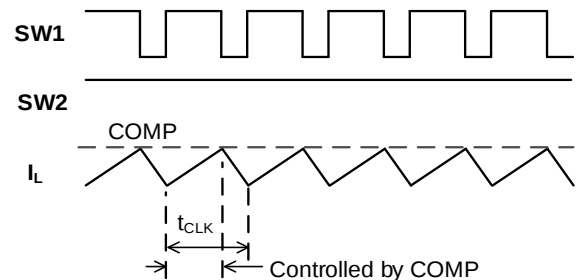


Figure 5: Buck Mode Waveform

### Boost Mode ( $V_{IN} < V_{OUT}$ )

When  $V_{IN}$  is below  $V_{OUT}$ , the MPQ4242B works in boost mode. In boost mode, SWC and SWD switch for boost regulation. Meanwhile, SWB is off and SWA stays on to conduct  $I_L$ .

SWC turns on at the beginning of each clock cycle. SWC turns off when  $I_L$  reaches the value set by  $V_{COMP}$ . SWD turns on until  $t_{CLK}$  times out to boost  $I_L$  to the output. Figure 6 shows the boost work waveform.

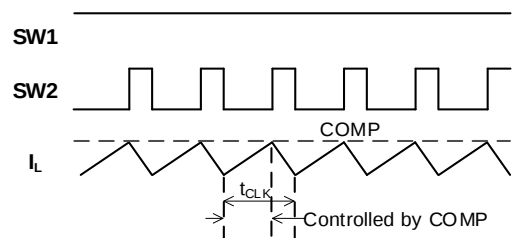


Figure 6: Boost Waveform

### Buck-Boost Mode ( $V_{IN} \approx V_{OUT}$ )

When  $V_{IN}$  is almost equal to  $V_{OUT}$ , the converter cannot provide enough energy to the load in buck mode due to SWA's minimum off time. In boost mode, the converter supplies too much power to the load due to SWC's minimum on time. Under these conditions, the MPQ4242B adopts buck-boost control to regulate the output (see Figure 7).

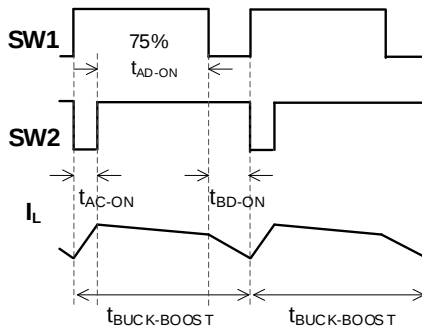


Figure 7: Buck-Boost Waveform

If  $V_{IN}$  is almost equal to  $V_{OUT}$ , buck-boost mode activates. The MOSFET turn-on sequence is as follows:

1. SWA and SWC
2. SWA and SWD
3. SWB and SWD

Throughout this process,  $I_L$  can reach the  $V_{COMP}$  requirement, and supply enough current to the output.

The SWA and SWD turn-on time is fixed to 75% of the buck-boost operation frequency.

If the buck mode minimum off time is almost reached, the IC enters buck-boost mode. If  $V_{IN}$  exceeds  $V_{OUT}$  by about 10% in buck-boost mode, the IC changes to buck mode. If  $V_{IN}$  is about 10% below  $V_{OUT}$ , the IC enters boost mode. If the boost mode minimum on time is almost reached, the IC enters buck-boost mode.

### External High-Side MOSFET Gate Driver

An external N-channel MOSFET can be added to improve system efficiency, especially for PD applications exceeding 45W. For applications below 45W, an external MOSFET is not required, and EXT\_HS\_FET\_RON should be set to 000b.

The external MOSFET is paralleled with the internal SWA. To accurately sense the input current, a 5mΩ to 12mΩ  $R_{DS(ON)}$  MOSFET is

recommended. The EXT\_HS\_FET\_RON configuration value should match (or be close to) the MOSFET's real  $R_{DS(ON)}$  under a 10V<sub>GS</sub> condition. The external MOSFET only turns on in boost mode when  $V_{IN}$  is significantly below  $V_{OUT}$ .

### 5V Internal VCC Regulator

The 5V internal regulator powers the CC pin's pull-up, VCONN, and most of the internal logic circuitries. The regulator takes the  $V_{IN}$  input and operates across the full  $V_{IN}$  range. When  $V_{IN}$  exceeds 5V, the regulator's output is in full regulation. If  $V_{IN}$  is below 5V, the output decreases with  $V_{IN}$ .

The VCC pin can support 0.1W of output power ( $P_{OUT}$ ). The VCC pin requires a 2.2μF ceramic decoupling capacitor.

### Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MPQ4242B's UVLO comparator monitors  $V_{IN}$ .

### Internal Soft Start

Soft start prevents the converter's  $V_{OUT}$  from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage ( $V_{SS}$ ) that ramps up from 0V to 5V. When SS is below the reference voltage ( $V_{REF}$ ), the error amplifier uses  $V_{SS}$  as the reference. When  $V_{SS}$  exceeds  $V_{REF}$ , the error amplifier uses  $V_{REF}$  as the reference. The SS time is internally set to 1ms for a 5V  $V_{OUT}$ .

If the output of the MPQ4242B is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal soft-start capacitor exceeds the internal feedback voltage.

### Constant Current (CC) Mode Over-Current-Protection (OCP)

The MPQ4242B senses the ground current via an external current-sense resistor. The device uses this information to limit the output current ( $I_{OUT}$ ). This is a highly accurate current limit. If  $I_{OUT}$  exceeds the current-limit threshold, the MPQ4242B enters constant current (CC) limit mode, and the current amplitude is limited.

If the MPQ4242B works in fixed power data object (PDO) mode, it sends a hard reset message once  $I_{OUT}$  exceeds the constant current limit. If the MPQ4242B works in augmented power data object (APDO) mode and continues to reduce the load resistance, then  $V_{OUT}$  drops until it reaches its under-voltage (UV) threshold (about 3V). If a UV condition is triggered, the MPQ4242B sends a hard reset message. If  $I_{OUT}$  still exceeds the over-current protection (OCP) threshold, the MPQ4242B enters hiccup mode to periodically restart the part.

This protection is especially useful when the output is dead-short-circuited to ground. This operation greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. The MPQ4242B exits hiccup mode once the OC condition is removed.

The current limit threshold can be set from 1A to 6.35A (with a 50mA resolution) via the I<sup>2</sup>C.

### Peak and Valley Current Limit

In addition to the output CC limit, the MPQ4242B also has SWA peak current and SWB valley current limits.

In buck mode and buck-boost mode, both the SWA peak current limit and the SWB valley current limit work as thresholds. The SWB's valley current limit has a 6.7A falling threshold. In boost mode, only the SWA peak current limit threshold operates. The peak current limit can be configured via the I<sup>2</sup>C or one-time-programmable (OTP) memory.

### Output Over-Voltage Protection (OVP)

The MPQ4242B has output over-voltage protection (OVP). If  $V_{OUT}$  exceeds 117% of  $V_{REF}$ , SWA, SWB, SWC, and SWD turn off. The resistor discharge path from the OUT pin to ground turns on. When  $V_{OUT}$  drops to 107% of  $V_{REF}$ , the chip returns to normal operation.

The absolute output OVP threshold is about 25V. The discharge resistor turns on when absolute OVP is triggered.

### Input Over-Voltage Protection ( $V_{IN}$ OVP)

The MPQ4242B has input OVP. If  $V_{IN}$  exceeds its OVP rising threshold (about 22V), SWA, SWB, SWC, and SWD turn off. The chip returns to normal operation when  $V_{IN}$  drops to its OVP falling threshold (about 20V).

$V_{IN}$  OVP if disabled by default, and it is controlled by OTP trimming.

### Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO rising threshold is 2.2V, with a hysteresis of 150mV. The BST1 capacitor's voltage is regulated internally by VCC through D2, M1, and C4. The BST2 capacitor's voltage is regulated internally by VCC through D3, M2, and C5 (see Figure 8).

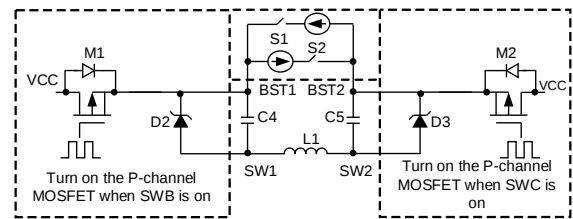


Figure 8: Internal Bootstrap Charging Circuit

In buck mode, S2 is always on, and BST2 is charged by BST1. In boost mode, S1 is always on, and BST1 is charged by BST2.

### Output Line Drop Compensation

The MPQ4242B is capable of compensating for a  $V_{OUT}$  drop.

If  $I_{OUT}$  is 0A, there is no compensation. If  $I_{OUT}$  is 3A, the line drop compensation voltage is 150mV. For example, if the USB output current exceeds 3A, the line drop compensation voltage stays at 150mV and does not rise. The line drop compensation value can be set to 150mV, 300mV, or 600mV via 0x18, bits[2:1]. Set 0x1E, bit[6] = 1 to enable an additional compensation voltage. Then the line drop compensation value can be set to 300mV, 450mV, or 750mV when the load is 3A.

Line drop compensation can be configured via the I<sup>2</sup>C or OTP. The compensated voltage is the same for all voltages.

For the default IC, line drop compensation is disabled in PPS mode. Line drop compensation can be enabled in PPS mode through factory OTP trimming.

## Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures.

If the silicon die temperature exceeds 175°C, the whole chip shuts down. When the temperature falls below its lower threshold (about 155°C), the chip is enabled again.

## CHARGING MODE AUTO-DETECTION

### Legacy USB 2.0 Mode

The MPQ4242B integrates a USB-dedicated charging port automatic detection function that recognizes most mainstream portable devices. The device supports the following charging schemes:

- USB battery charging specification (BC1.2) / Chinese Telecommunications Industry Standard YD/T 1591-2009
- Apple 3A Divider Mode
- 1.2V/1.2V Mode
- QC 3.0
- Huawei FCP Class A

The automatic detection function is a state machine that supports all of the above DCP charging schemes. This function starts in 3A divider mode. If a device compliant to divider mode is connected, the MPQ4242B stays in divider mode. Meanwhile, 3.3V is applied to the DM pin, while 2.7V is applied to the DP pin.

If a BC1.2 or YD/T 1591-2009 compliant device is connected, the MPQ4242B operates in 1.2V/1.2V and BC1.2 DCP mode. In this scenario, DM and DP are shorted together with a resistance. The device then stays in this mode until the data line is released. If this occurs, the MPQ4242B returns to 3A divider mode.

When a QC 3.0 or FCP device (without PD protocol) is connected, the MPQ4242B can automatically enter high-voltage, quick charge mode.

The MPQ4242B supports BC1.2 charging downstream port (CDP) handshaking as well. This can be enabled by setting CDP\_EN to 1b via the I<sup>2</sup>C.

If a USB PD contract is established after the sink is connected, the QC 3.0 and FCP functions are disabled.

## USB Type-C Port

The USB Type-C receptacle, plug, and cable solution incorporates a configuration process to detect a downstream facing port (DFP) to upstream facing port (UFP) connection. This detection function is used for V<sub>BUS</sub> management and can determine the host-to-device connection.

Initially, a DFP-to-UFP connection is detected by a host (DFP) when one of the CC pins at its USB Type-C receptacle senses a specified resistance at GND. Subsequently, DFP-to-UFP disconnect is detected when the CC pin that was terminated at its USB Type-C receptacle is no longer connected to GND via a specified resistance.

Power is not applied to the USB Type-C host or hub receptacle (VBUS or VCONN) until the DFP detects the presence of a connected device (UFP) port. When a DFP-to-UFP connection is detected, the DFP is expected to enable power to the receptacle and proceed to normal USB operation with the connected device. When a DFP-to-UFP disconnect is detected, the port sourcing V<sub>BUS</sub> removes power.

The MPQ4242B's power supply capability is rated for 5V @ 3A by default. V<sub>CONN</sub> is provided by the DFP to power cables with electronics that are plugged in. V<sub>CONN</sub> is provided power over the CC pin that is not connected to the cable's CC wire. The maximum output power of V<sub>CONN</sub> is 1W.

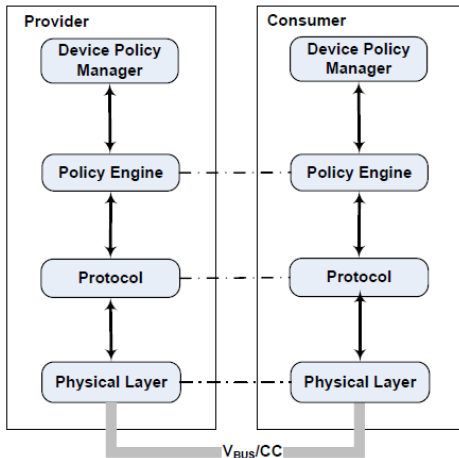
VCONN is disabled until R<sub>A</sub> is detected. R<sub>A</sub> is a pull-down resistor connected from the CC pin to GND. Its resistance must be below 1.2kΩ.

### USB Power Delivery (PD) 3.1

In USB PD, pairs of directly connected ports negotiate the voltage, current, and/or the direction of power flow across the USB cable, using VBUS or the CC wire as the communication channel. The mechanisms used operate independently of other USB methods that negotiate power. USB Type-C connectors can support the CC wire as the communication channel.

The USB PD engine can disable the clock and enter sleep mode if no PD command is detected.

The input current is typically 150µA in sleep mode. Figure 9 shows the USB PD communication stack.



**Figure 9: USB PD Communication Stack**

Table 1 shows the functions and DFP commands supported by the MPQ4242B.

**Table 1: Control Message**

| Transmitted Message | Received Message        |
|---------------------|-------------------------|
| ACCEPT              | GET_PPS_STATUS          |
| GET_STATUS          | GET_STATUS              |
| GOODCRC             | GOODCRC                 |
| NOT_SUPPORTED       | NOT_SUPPORTED           |
| PS_RDY              | REJECT                  |
| REJECT              | SOFT_RESET              |
| SOFT_RESET          | HARD_RESET              |
| HARD_RESET          | VCONN_SWAP              |
| -                   | GET_SOURCE_CAP          |
| -                   | GET_SOURCE_CAP_EXTENDED |
| -                   | GET_REVISION            |

Table 2 shows the data messages.

**Table 2: Data Message**

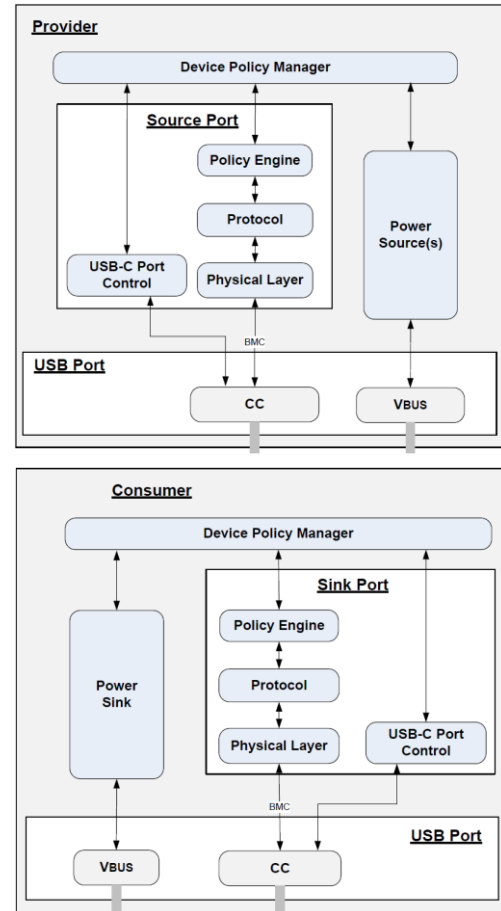
| Transmitted Message | Received Message  |
|---------------------|-------------------|
| SOURCE_CAPABILITIES | SINK_CAPABILITIES |
| BIST                | REQUEST           |
| ALERT               | BIST              |
| REVISION            | ALERT             |

Table 3 shows the extended messages.

**Table 3: Extended Message**

| Transmitted Message          | Received Message |
|------------------------------|------------------|
| STATUS                       | -                |
| PPS_STATUS                   | -                |
| SOURCE_CAPABILITIES_EXTENDED | -                |

Figure 10 shows the MPQ4242B's device policy manager function block.



**Figure 10: Device Policy Manager**

Figure 11 shows a PD contract handshake sequence for the MPQ4242B.

| #  | CH  | OS   | Power  | Data | Cable Plug | Type                |
|----|-----|------|--------|------|------------|---------------------|
| 0  | CC2 | SOP' |        |      | UFP or DFP | Vendor_Defined      |
| 1  | CC2 | SOP' |        |      | Cable Plug | GoodCRC             |
| 2  | CC2 | SOP' |        |      | Cable Plug | Vendor_Defined      |
| 3  | CC2 | SOP' |        |      | UFP or DFP | GoodCRC             |
| 4  | CC2 | SOP  | Source | DFP  |            | Source_Capabilities |
| 5  | CC2 | SOP  | Sink   | UFP  |            | GoodCRC             |
| 6  | CC2 | SOP  | Sink   | UFP  |            | Request             |
| 7  | CC2 | SOP  | Source | DFP  |            | GoodCRC             |
| 8  | CC2 | SOP  | Source | DFP  |            | Accept              |
| 9  | CC2 | SOP  | Sink   | UFP  |            | GoodCRC             |
| 10 | CC2 | SOP  | Source | DFP  |            | PS_RDY              |
| 11 | CC2 | SOP  | Sink   | UFP  |            | GoodCRC             |

**Figure 11: PD Contract Handshake**

### VCONN Power Supply

The integrated VCONN power supply has a maximum of 100mW. The power switch connected from VCC to VCONN has a current limit. During a VCONN short to ground event, the MPQ4242B turns off VCONN.

For a 1W  $V_{CONN}$  application, an external  $V_{CONN}$  supply should be applied to GPIO2.

### LED PWM Driver

The GPIO2 pin can be configured as a PWM output to drive an LED. By default, it is 25kHz, with a 50% PWM duty cycle and a maximum 15mA capability.

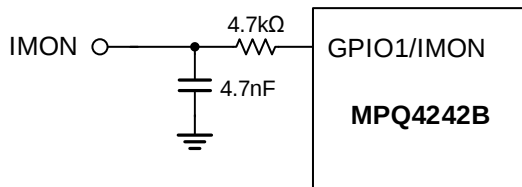
The PWM duty cycle can be set between 5% and 100% (with a 1% resolution) via the I<sup>2</sup>C.

### EN Off Time

The MPQ4242B has a configurable EN off time. When the EN pin is pulled low, the device operates at full functionality until the timer elapses. The maximum EN off delay is 120 minutes. If the EN pin is pulled high within this time, the counter resets.

### Current Monitor Output

When the GPIO1 pin is set as IMON, the MPQ4242B senses the average load current through a current-sense resistor. The IMON amplifier outputs a voltage signal on the GPIO1 pin. This signal is amplified from the voltage difference between the ISEN+ and ISEN- pins. It is recommended to place a 4.7nF + 4.7kΩ filter on the GPIO1 pin (see Figure 12). The minimum load that IMON can recognize is 0.2A.



**Figure 12: IMON Connection**

The relationship between the IMON voltage and the load current can be calculated with Equation (1):

$$V_{IMON} = \text{Gain} \times I_{OUT} \times R_{SENS} \quad (1)$$

Where Gain is 27.5V/V, and  $R_{SENS} = 10\text{m}\Omega$ .

When automatic PFM/PWM mode is set up, the IMON function can only work normally when the part enters continuous conduction mode (CCM).

### NTC Function

When the GPIO2 pin is set to the NTC function, the device compares the NTC voltage to  $V_{REF}$ . If the NTC voltage is below the threshold, the MPQ4242B initiates thermal shutdown

protection. In this scenario, the device will either shut down or reduce the PD power. The response can be selected via NTC\_MODE.

If NTC\_MODE is set to 1, OTW2\_NTC\_PDP determines the value to which PD power should be reduced. OTW2\_NTC\_PDO\_SELECT sets which PDO voltage is enabled after entering NTC mode. See Table 4 on page 29 for more details.

If the NTC voltage rises above the recovery threshold, the device recovers to a normal state. The I<sup>2</sup>C can set one of two NTC recovery hysteresis values. There is no 16s recover delay.

### NTC2 Function

When the GPIO1 pin is set to the NTC2 function, the device compares the NTC2 voltage to  $V_{REF}$ . If the NTC2 voltage drops below this threshold, the MPQ4242B triggers power sharing. When the power share function is triggered, the PD power rating drops to the value set by PS\_PDP\_THD. Table 4 on page 29 shows the PDO/APDO voltage and current.

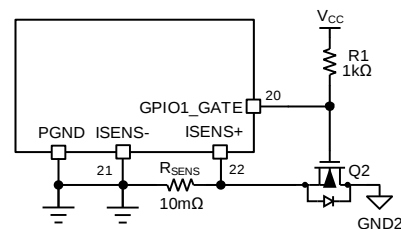
If the NTC2 voltage rises above the recovery threshold, the MPQ4242B exits power sharing. NTC\_HYSTERESIS sets the hysteresis, which also sets the hysteresis for the GPIO1 pin's NTC function.

The NTC\_MODE, OTW2\_NTC\_PDO\_SELECT, and OTW2\_NTC\_PDP bits do not control the NTC2 pin's behavior.

If GPIO2 is set to the power share function while GPIO1 is set for the NTC2 function, the MPQ4242B enters power sharing when either NTC2 or GPIO2\_POWER\_SHARE is triggered.

### Battery-to-Ground Short Protection Driver

The GPIO1 pin can be set to the GATE function for GND-to-battery short protection. If a battery to output ground (GND2) short occurs, the GATE pin pulls low and Q2 turns off. Figure 13 shows the battery-to-ground short driver.



**Figure 13: Battery-to-Ground Short Driver**

### Over Temperature Warning (OTW) Function

The MPQ4242B senses its die temperature internally. If the chip's temperature exceeds the OTW1 threshold, the MPQ4242B reduces the PD power state to the value set by OTW1\_PDP. OTW1\_PDO\_SELECT sets which PDO voltage is enabled after entering OTW1 mode. Table 4 on page 29 shows the OTW\_PDO\_SELECT function.

If the die temperature continues increasing and triggers the second threshold set by OTW2, the MPQ4242B reduces the PD power to the level set by OTW2\_NTC\_PDP.

OTW2\_NTC\_PDO\_SELECT sets which PDO voltage is enabled. The MPQ4242B waits 16 seconds after the OTW condition is removed before recovering to a normal PD rating.

### Low Battery Operation

During the first  $V_{IN}$  start-up, the MPQ4242B is delayed for 1s before detecting  $V_{IN}$ .

If the MPQ4242B detects that the battery voltage (its  $V_{IN}$  voltage) is below the VBATT\_LOW\_THLD1 falling threshold for the VBATT\_LOW\_BLK deglitch time, it reduces the PD power rating according to the set value. Meanwhile, VBATT\_LOW1\_FLAG is set. If there is a PD contract, the PD engine resends the updated PDO with a reduced PDP. The PDO list is determined by VBATT\_L1\_PDO\_SELECT.

If the MPQ4242B detects that the battery voltage (its  $V_{IN}$  voltage) is below the VBATT\_LOW\_THLD2 falling threshold for the VBATT\_LOW\_BLK deglitch time, it reduces the PD power rating according to the set value. Meanwhile, VBATT\_LOW2\_FLAG is set. If there is a PD contract, the PD engine resends the updated PDO with a reduced PDP. The PDO list is determined by VBATT\_L2\_PDO\_SELECT.

If the MPQ4242B detects that the battery voltage (its  $V_{IN}$  voltage) is below the VBATT\_LOW\_THLD3 falling threshold for the VBATT\_LOW\_BLK deglitch time, it shuts down.

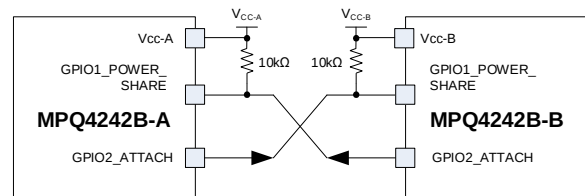
When the battery voltage recovers and exceeds the VBATT\_LOW\_THLD rising threshold with a 1s digital deglitch time, the PDO recovers to a normal PDP.

There are three battery voltage ( $V_{BATT}$ ) low thresholds: VBATT\_LOW\_THLD1, VBATT\_LOW\_THLD2, and VBATT\_LOW\_THLD3. Accordingly, VBATT\_LOW1\_PDP and VBATT\_LOW2\_PDP define the MPQ4242B's reduced PDP level. During the MPQ4242B's first start-up, the internal VBATT\_LOW\_FLAG default state is 0. The VBATT\_LOW detection circuitry starts to work when a USB Type-C receptacle is attached; it is reset by UVLO or an EN shutdown.

### POWER SHARE FUNCTION

#### GPIO1\_POWER\_SHARE

The GPIO1\_POWER\_SHARE pin can accept an external input voltage. If the second MPQ4242B (MPQ4242B-B) detects that a valid sink is attached, the first MPQ4242B's (MPQ4242B-A) GPIO1\_POWER\_SHARE pin is pulled down by the MPQ4242B-B's GPIO2\_ATTACH pin (see Figure 14).



**Figure 14: Power Share Connection Between Two MPQ4242Bs (e.g. Cut Total Power to 50%/50%)**

When the power share function is triggered, the PDO list and current are determined by PS\_PDP\_THD and PS\_PDP\_THD\_PDO\_SELECT (see Table 4 on page 29). For example, a 3.3V to 21V APDO current rating is can be calculated as  $45W / 21V = 2.1A$ .

**Table 4: PDO Voltage and Current Set Table based on the PS\_PDP\_THD and PS\_PDP\_THD\_PDO\_SEL**

| PDO List                                       | 5V<br>(Fixed)  | 9V<br>(Fixed) | 12V<br>(Fixed) | 15V<br>(Fixed) | 20V<br>(Fixed)   | 5V<br>(Prog.)            | 9V<br>(Prog.)   | 15V<br>(Prog.) | 20V<br>(Prog.)   |
|------------------------------------------------|----------------|---------------|----------------|----------------|------------------|--------------------------|-----------------|----------------|------------------|
| Output Current                                 | PDP / 5<br>(9) | PDP / 9       | PDP / 12       | PDP / 15       | PDP / 20<br>(10) | PDP / 5.9                | PDP / 11        | PDP / 16       | PDP / 21<br>(10) |
| PS_PDP_THD_PDO_SEL Register Selection Bit (13) | x              | 1             | 0              | 1              | 1                | 1                        | 1               | 0              | 0                |
| PS_PDP_THD = 22.5W                             | 5V, 3A<br>(11) | 9V, 2.5A      | -              | 15V, 1.5A      | 20V, 1.13A       | 3.3V to 5.9V, 3A<br>(12) | 3.3V to 11V, 2A | -              | -                |

**Notes:**

- 9) A fixed 5V PDO is always enabled after entering power sharing.
- 10) The fixed PDO current is equal to PDP / Voltage. The maximum current is 3A for <20V fixed PDOs. The maximum current can be 5A for 20V PDO and all APDOs.
- 11) The minimum PDP is 5V x 1.5A = 7.5W.  $R_p$  changes to 5V / 1.5A when PDP < 15W.
- 12) The PPS current is calculated with PDP / 5.9V for 5V PPS; PDP / 11V for 9V PPS; PDP / 16V for 15V PPS; PDP / 21V for 20V PPS.
- 13) The registers PS\_PDP\_THD, PS\_PDO\_SELECT, VBATT\_L1\_PDO\_SELECT, VBATT\_L2\_PDO\_SELECT, OTW1\_PDO\_SELECT, and OTW2\_NTC\_PDO\_SELECT share the same format. The gray cells are set by 8-bit register values.

**GPIO2\_POWER\_SHARE**

The GPIO2\_POWER\_SHARE threshold is  $V_{TH\_PS}$  (typically 1.87V). When the GPIO2 pin is set for the power share function, and the

MPQ4242B-A detects that its GPIO2 voltage exceeds  $V_{TH\_PS}$ , the power share function is triggered. In this scenario, the PDO list and current is determined by PS\_PDP\_THD and PS\_PDP\_THD\_PDO\_SELECT (see Table 5).

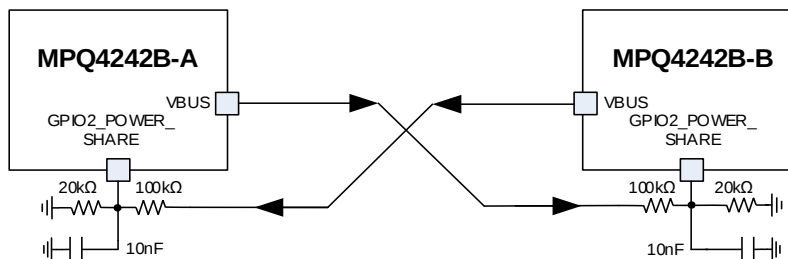
**Table 5: PDO Voltage and Current Set Table based on PS\_PDP\_THD and PS\_PDP\_THD\_PDO\_SEL**

| PDO List                                       | 5V<br>Fixed    | 9V<br>Fixed | 12V<br>Fixed | 15V<br>Fixed | 20V<br>Fixed     | 5V<br>Prog.              | 9V<br>Prog.        | 15V<br>Prog. | 20V<br>Prog.     |
|------------------------------------------------|----------------|-------------|--------------|--------------|------------------|--------------------------|--------------------|--------------|------------------|
| Output Current                                 | PDP / 5<br>(9) | PDP / 9     | PDP / 12     | PDP / 15     | PDP / 20<br>(10) | PDP / 5.9                | PDP / 11           | PDP / 16     | PDP / 21<br>(10) |
| PS_PDP_THD_PDO_SEL Register Selection Bit (13) | x              | 1           | 0            | 0            | 0                | 1                        | 1                  | 0            | 0                |
| PS_PDP_THD = 15W                               | 5V, 3A<br>(11) | 9V, 1.6A    | -            | -            | x                | 3.3V to 5.9V, 3A<br>(12) | 3.3V to 11V, 1.35A | -            | -                |

The MPQ4242B exits the power sharing status after the GPIO2 voltage drops below  $V_{TH\_PS}$ . Figure 15 shows the GPIO2\_POWER\_SHARE connection block.

When  $V_{BUS}$  exceeds 11.2V, the power share function is triggered.

Table 6 on page 30 shows the PDP of the MPQ4242B-A and MPQ4242B-B in the GPIO2\_POWER\_SHARE function.


**Figure 15: GPIO2 Power Share Connection Between Two MPQ4242Bs**

**Table 6: GPIO2 Power Share PDP Management in Dual-Channel Applications <sup>(14)</sup>**

Column Format = <PD Contract W> (<Advertised Power W>)

Total Shared Power = 60W

Each Port PDP = 45W

| Condition | USB Type-C Port 1        | USB Type-C Port 2        | Total Power |
|-----------|--------------------------|--------------------------|-------------|
| 1         | -- (45W) <sup>(15)</sup> | -- (45W) <sup>(15)</sup> | -           |
| 2         | 15W (45W)                | -- (45W) <sup>(15)</sup> | 15W         |
| 3         | 27W (45W)                | -- (45W) <sup>(15)</sup> | 27W         |
| 4         | 45W (45W)                | 15W (15W)                | 60W         |
| 5         | 27W (45W)                | 15W (45W)                | 42W         |
| 6         | 27W (45W)                | 27W (45W)                | 54W         |
| 7         | 15W (15W)                | 45W (45W)                | 60W         |
| 8         | -- (15W) <sup>(16)</sup> | 45W (45W)                | 45W         |
| 9         | -- (45W) <sup>(15)</sup> | 27W (45W)                | 27W         |

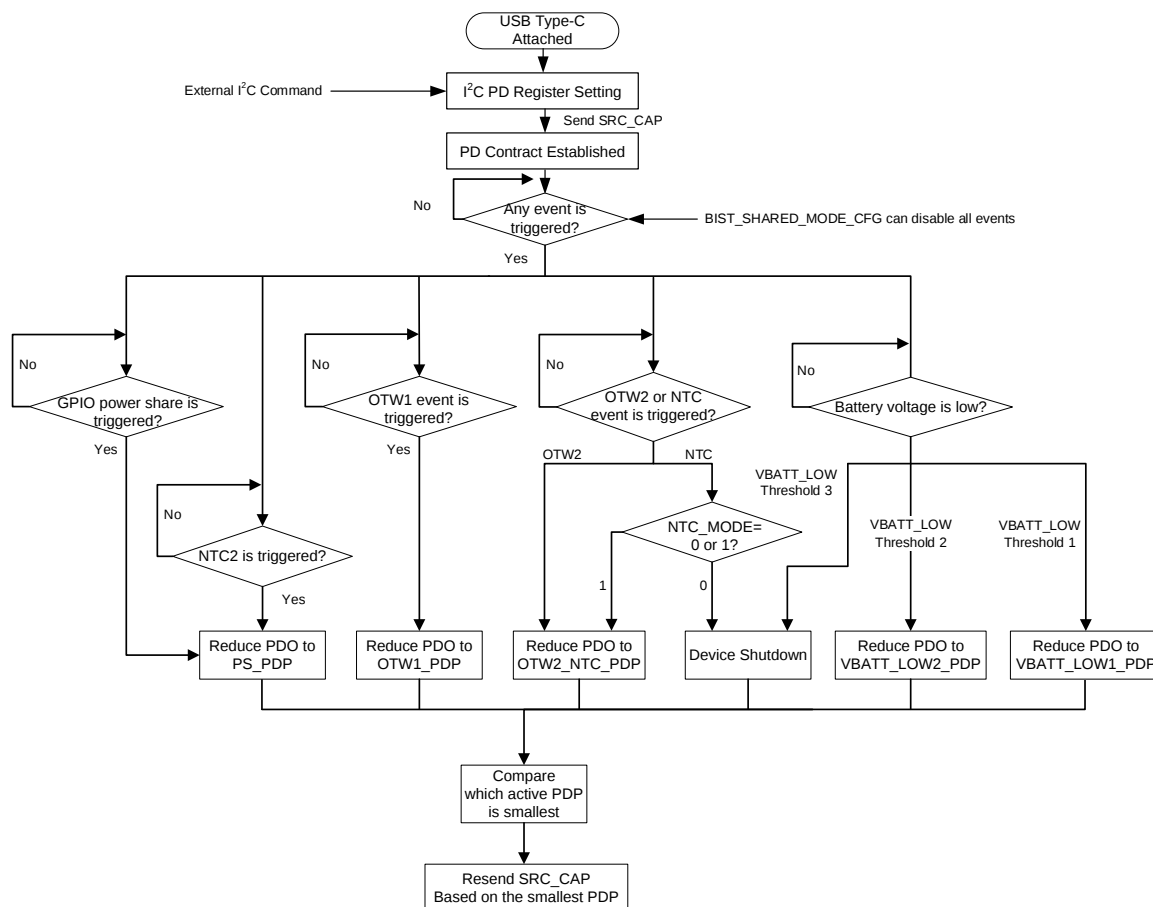
**Notes:**

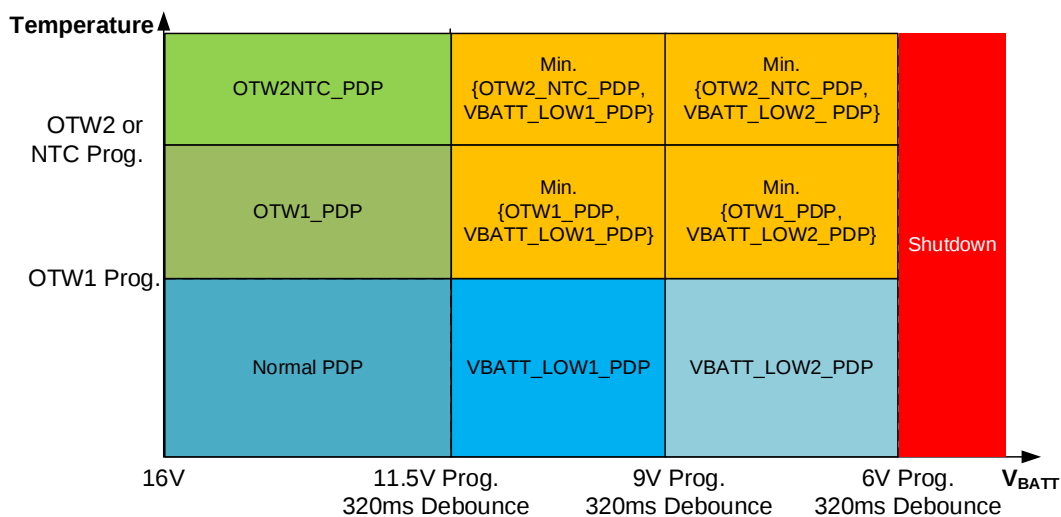
14) The PDP table is based on the GPIO2\_POWER\_SHARE set-up in Figure 15 on page 29. The MPQ4242B-A triggers power sharing when the MPQ4242B-B's  $V_{BUS} > 11.2V$ .

15) The port is not connected and there is no valid PD contract, but the maximum PDP (45W) is still advertised.

16) Power sharing has been triggered because another port has made a PD contract with a high PDP. To limit the total shared power to 60W or below, the advertised power drops to 15W.

Figure 16 shows the PDP state machine. Figure 17 on page 31 shows the PDP foldback scheme.


**Figure 16: PDP State Machine (I²C Still Operates during NTC Shutdown)**



**Figure 17: PDP Foldback Scheme**

## I<sup>2</sup>C INTERFACE

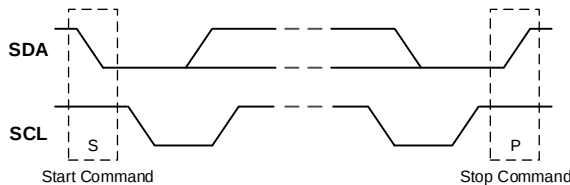
### I<sup>2</sup>C Serial Interface Description

The I<sup>2</sup>C is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address, and arranges the communication sequence.

The MPQ4242B interface is an I<sup>2</sup>C slave that supports fast mode (400kHz). The I<sup>2</sup>C interface adds flexibility to the power supply solution. The output voltage ( $V_{OUT}$ ), transition slew rate, and additional parameters can be instantaneously controlled by the I<sup>2</sup>C interface. When the master sends the address as an 8-bit value, the 7-bit address should be followed by 0 or 1 to indicate a write or read operation, respectively.

### Start and Stop Commands

The start (S) command and stop (P) command are signaled by the master device, which signifies the beginning and the end of the I<sup>2</sup>C transfer. The start command is defined as the SDA signal transitioning from high to low while SCL is high. The stop command is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 18).



**Figure 18: Start and Stop Commands**



|  |                 |                                   |                   |                |
|--|-----------------|-----------------------------------|-------------------|----------------|
|  | Master to Slave | A = Acknowledge (SDA = Low)       | S = Start Command | Write (Wr) = 0 |
|  | Slave to Master | NA = Not Acknowledge (SDA = High) | P = Stop Command  | Read (Rd) = 1  |

**Figure 19: I<sup>2</sup>C Write Example (Write Single Register)**

The master then generates the SCL clocks, and transmits the device address and the read/write (R/W) direction bit on the SDA line.

### Transfer Data

Data is transferred in 8-bit bytes by the SDA line. Each byte of data should be followed by an acknowledge bit.

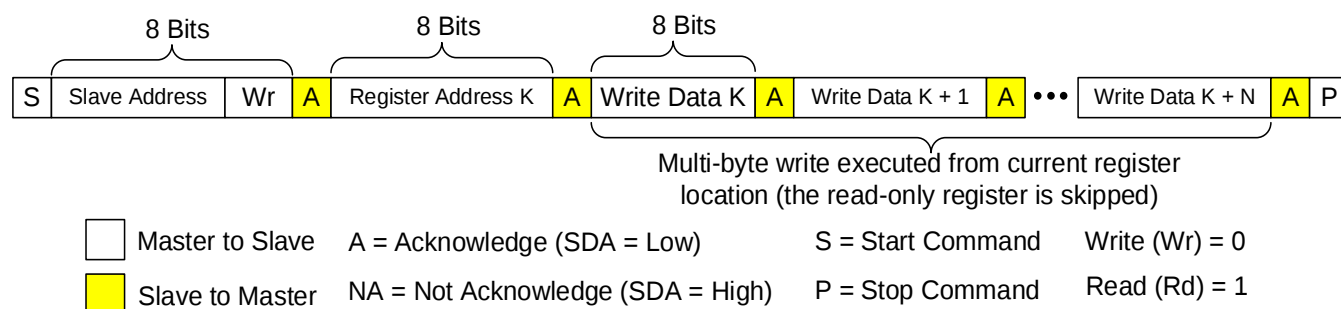
### I<sup>2</sup>C Start-Up Timing

The I<sup>2</sup>C function is enabled once  $V_{IN}$  exceeds its UVLO threshold and EN is active.

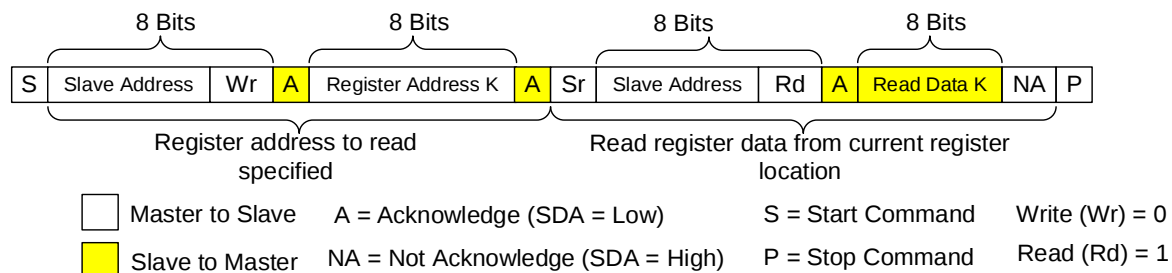
### I<sup>2</sup>C Update Sequence

The MPQ4242B requires a start command, a valid I<sup>2</sup>C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MPQ4242B acknowledges by pulling SDA low during the high period of a single clock pulse. A valid I<sup>2</sup>C address selects the MPQ4242B. The MPQ4242B performs an update on the falling edge of the LSB.

Figure 19 shows an I<sup>2</sup>C write example for a single register. Figure 20 on page 33 shows an I<sup>2</sup>C write example for multiple registers. Figure 21 on page 33 shows an I<sup>2</sup>C read example for a single register.



**Figure 20: I²C Write Example (Write Multiple Registers)**



**Figure 21: I²C Read Example (Read Single Register)**

## I<sup>2</sup>C REGISTER MAP

| Addr.<br>(Hex) | Name     | R/W | D7                                                                 | D6                                                          | D5                  | D4                          | D3                             | D2                     | D1                          | D0                  |        |
|----------------|----------|-----|--------------------------------------------------------------------|-------------------------------------------------------------|---------------------|-----------------------------|--------------------------------|------------------------|-----------------------------|---------------------|--------|
| 00             | PDO_SET1 | R/W | N/A                                                                |                                                             | PDO7_EN<br>(17)     | PDO6_EN<br>(17)             | PDO5_E<br>N (17)               | PDO4_EN<br>(17)        | PDO3_EN<br>(17)             | PDO2_EN<br>(17)     |        |
| 01             | PDO_SET2 | R/W | N/A                                                                |                                                             | PDO7<br>TYPE (17)   | PDO6<br>TYPE (17)           | PDO5<br>TYPE (17)              | PDO4<br>TYPE (17)      | PDO3<br>TYPE (17)           | PDO2<br>TYPE (17)   |        |
| 02             | HOST_SET | R/W | COMM<br>UNICA<br>CAPAB<br>_HOST<br>(17)                            | PRODUCT_TYPE_DF<br>P (17)                                   |                     | HOST_CAPABILITY(000B) (17)  |                                |                        | PORT_NUMBER (17)            |                     |        |
| 03             | PDO_I1   | R/W | PDO1_CURRENT_SETTING (17) (3A default)                             |                                                             |                     |                             |                                |                        |                             |                     |        |
| 04             | PDO_V2_L | R/W | PDO2_VOLTAGE_SETTING (low byte) (17) (9V default)                  |                                                             |                     |                             |                                |                        |                             |                     |        |
| 05             | PDO_V2_H | R/W | PDO2_VOLTAGE_SETTING (high byte) (17) (0x00)                       |                                                             |                     |                             |                                |                        |                             |                     |        |
| 06             | PDO_I2   | R/W | PDO2_CURRENT_SETTING (17) (3A default)                             |                                                             |                     |                             |                                |                        |                             |                     |        |
| 07             | PDO_V3_L | R/W | PDO3_VOLTAGE_SETTING (low byte) (17) (15V default)                 |                                                             |                     |                             |                                |                        |                             |                     |        |
| 08             | PDO_V3_H | R/W | PDO3_VOLTAGE_SETTING (high byte) (17) (0x00)                       |                                                             |                     |                             |                                |                        |                             |                     |        |
| 09             | PDO_I3   | R/W | PDO3_CURRENT_SETTING (17) (3A)                                     |                                                             |                     |                             |                                |                        |                             |                     |        |
| 0A             | PDO_V4_L | R/W | PDO4_VOLTAGE_SETTING (low byte) (17) (20V default)                 |                                                             |                     |                             |                                |                        |                             |                     |        |
| 0B             | PDO_V4_H | R/W | PDO4_VOLTAGE_SETTING (high byte) (17) (0x00)                       |                                                             |                     |                             |                                |                        |                             |                     |        |
| 0C             | PDO_I4   | R/W | PDO4_CURRENT_SETTING (17) (3A)                                     |                                                             |                     |                             |                                |                        |                             |                     |        |
| 0D             | PDO_V5_L | R/W | PDO5_VOLTAGE_SETTING (low byte) (17) (3.3V)                        |                                                             |                     |                             |                                |                        |                             |                     |        |
| 0E             | PDO_V5_H | R/W | PDO5_VOLTAGE_SETTING (high byte) (17) (11V)                        |                                                             |                     |                             |                                |                        |                             |                     |        |
| 0F             | PDO_I5   | R/W | PDO5_CURRENT_SETTING (17) (3A)                                     |                                                             |                     |                             |                                |                        |                             |                     |        |
| 10             | PDO_V6_L | R/W | PDO6_VOLTAGE_SETTING (low byte) (17) (3.3V)                        |                                                             |                     |                             |                                |                        |                             |                     |        |
| 11             | PDO_V6_H | R/W | PDO6_VOLTAGE_SETTING (high byte) (17) (16V)                        |                                                             |                     |                             |                                |                        |                             |                     |        |
| 12             | PDO_I6   | R/W | PDO6_CURRENT_SETTING (17) (3A)                                     |                                                             |                     |                             |                                |                        |                             |                     |        |
| 13             | PDO_V7_L | R/W | PDO7_VOLTAGE_SETTING (low byte) (17) (3.3V)                        |                                                             |                     |                             |                                |                        |                             |                     |        |
| 14             | PDO_V7_H | R/W | PDO7_VOLTAGE_SETTING (high byte) (17) (21V)                        |                                                             |                     |                             |                                |                        |                             |                     |        |
| 15             | PDO_I7   | R/W | PDO7_CURRENT_SETTING (17) (3A)                                     |                                                             |                     |                             |                                |                        |                             |                     |        |
| 16             | PD_CTL1  | R/W | CDP_EN<br>(17)                                                     | LEGACY_CHARGIN<br>G_MODE_SEL (17)                           |                     | USBCOM<br>MUNICAT<br>E (17) | NTC<br>CTL_RP<br>(17)          | TOUCH_TEMP (17)        |                             | TYPE-C<br>MODE (17) |        |
| 17             | PD_CTL2  | R/W | HDRST                                                              | USBSUS<br>PEND<br>(17)                                      | TOUCH CURRENT (17)  |                             |                                | COMPLIANCE (17)        |                             |                     |        |
| 18             | PWR_CLT1 | R/W | EN (17)                                                            | MODE<br>(17)                                                | FREQ (17)           |                             | DITHER<br>(17)                 | LINE_DROP_COMP<br>(17) |                             | SLEW<br>RATE (17)   |        |
| 19             | PWR_CLT2 | R/W | EN_VBU<br>S (17)                                                   | PPS_MI<br>N_SEL<br>(17)                                     | OTW1_THRESHOLD (17) |                             |                                | OTP_THRESHOLD (17)     |                             |                     |        |
| 1A             | VOUT_L   | R/W | RESERVED_ALL: 0                                                    |                                                             |                     |                             |                                |                        | VOUT_DATA_BIT_LOW[2:0] (17) |                     |        |
| 1B             | VOUT_H   | R/W | VOUT_DATA_BIT_HIGH[10:3] (17) (use this as default DAC VREF)       |                                                             |                     |                             |                                |                        |                             |                     |        |
| 1C             | IOUT_LIM | R/W | N/A                                                                | OUTPUT_CURRENT_LIMIT_THRESHOLD (17) (1A to 6.35A/50mA step) |                     |                             |                                |                        |                             |                     |        |
| 1D             | CTL_SYS0 | R/W | N/A                                                                |                                                             |                     |                             |                                |                        |                             |                     | GO_BIT |
| 1E             | CTL_SYS1 | R/W | SEND<br>SRC_CA<br>P                                                | ADDITIO<br>NAL_LIN<br>E_DROP<br>_COMP<br>_ENSATI<br>ON (17) | EN_OFF_TIMER (17)   |                             | I2C_SLAVE_ADDRESS (A4-A1) (17) |                        |                             |                     |        |
| 1F             | CTL_SYS2 | R/W | GPIO1 (17)                                                         |                                                             |                     | GPIO2 (17)                  |                                |                        | I2C_CTL<br>VOUT_E<br>N (17) | N/A                 |        |
| 20             | CTL_SYS3 | R/W | PS_PDP_THD (17) (PDP is reduced to this value after power sharing) |                                                             |                     |                             |                                |                        |                             |                     |        |
| 21             | CTL_SYS4 | R/W | PS_PDP_THD_PDO_SELECT (17)                                         |                                                             |                     |                             |                                |                        |                             |                     |        |
| 22             | CTL_SYS5 | R/W | N/A                                                                | PPS_3A<br>_5A (17)                                          | CC_BLANK_TIMER (17) |                             | N/A                            |                        | PD_CAP_PEAK<br>CURRENT (17) |                     |        |

## I<sup>2</sup>C REGISTER MAP (continued)

| Addr.<br>(Hex) | Name        | R/W | D7                                                                                                          | D6                             | D5        | D4                              | D3                              | D2       | D1                           | D0        |
|----------------|-------------|-----|-------------------------------------------------------------------------------------------------------------|--------------------------------|-----------|---------------------------------|---------------------------------|----------|------------------------------|-----------|
| 23             | CTL_SYS6    | R/W | VBATT_LOW1_PDP <sup>(17)</sup>                                                                              |                                |           |                                 |                                 |          |                              |           |
| 24             | CTL_SYS7    | R/W | VBATT_L1_PDO_SELECT <sup>(17)</sup>                                                                         |                                |           |                                 |                                 |          |                              |           |
| 25             | CTL_SYS8    | R/W | VBATT_LOW2_PDP <sup>(17)</sup>                                                                              |                                |           |                                 |                                 |          |                              |           |
| 26             | CTL_SYS9    | R/W | VBATT_L2_PDO_SELECT <sup>(17)</sup>                                                                         |                                |           |                                 |                                 |          |                              |           |
| 27             | CTL_SYS10   | R/W | OTW1_PDP <sup>(17)</sup>                                                                                    |                                |           |                                 |                                 |          |                              |           |
| 28             | CTL_SYS11   | R/W | OTW1_PDO_SELECT <sup>(17)</sup>                                                                             |                                |           |                                 |                                 |          |                              |           |
| 29             | CTL_SYS12   | R/W | OTW2_NTC_PDP <sup>(17)</sup>                                                                                |                                |           |                                 |                                 |          |                              |           |
| 2A             | CTL_SYS13   | R/W | OTW2_NTC_PDO_SELECT <sup>(17)</sup>                                                                         |                                |           |                                 |                                 |          |                              |           |
| 2B             | CTL_SYS14   | R/W | VBATT_LOW_THLD1 <sup>(17)</sup>                                                                             |                                |           |                                 | VBATT_LOW_THLD2 <sup>(17)</sup> |          |                              |           |
| 2C             | CTL_SYS15   | R/W | VBATT_LOW_THLD3 <sup>(17)</sup>                                                                             |                                |           |                                 | VBATT_LOW_BLK <sup>(17)</sup>   |          | N/A                          |           |
| 2D             | CTL_SYS16   | R/W | N/A                                                                                                         | EXT_HS_FET_RON <sup>(17)</sup> |           |                                 | OTW2_THRESHOLD <sup>(17)</sup>  |          |                              | N/A       |
| 2E             | CTL_SYS17   | R/W | PEAK_CL <sup>(17)</sup>                                                                                     |                                | N/A       | NTC_HYS_TERESIS <sup>(17)</sup> | NTC_MODE <sup>(17)</sup>        | N/A      | VBUS_VOLTAGE <sup>(17)</sup> |           |
| 2F             | CTL_SYS18   | R/W | OTP_PROGRAM                                                                                                 | LED_PWM_DUTY <sup>(17)</sup>   |           |                                 |                                 |          |                              |           |
| 30             | STATUS1     | R   | ATTACHED                                                                                                    | NTC2_ENTER                     | POL       | SHORT_VBATT                     | FAULT                           | OTP_PAGE | CC_CV                        | NTC_ENTER |
| 31             | STATUS2     | R   | VBATT_LOW1_FLAG                                                                                             | VBATT_LOW2_FLAG                | OTW1      | OTW2                            | SELECTED_PDO_INDEX              |          |                              | PDO_TYPE  |
| 32             | STATUS3     | R   | CONTRACT_POWER (CP)                                                                                         |                                |           |                                 |                                 |          |                              |           |
| 33             | ID1         | R   | OTP_SUFFIX_CODE <sup>(17)</sup>                                                                             |                                |           |                                 |                                 |          |                              |           |
| 34             | ID2         | R   | OTP_SOFTWARE_REVISION_NO <sup>(17)</sup>                                                                    |                                |           |                                 |                                 |          |                              |           |
| 35             | FW_REV      | R   | MISMATCH_H                                                                                                  | GIVEBACK_FLAG                  | CABLE_CAP | FIRMWARE_REVISION               |                                 |          |                              |           |
| 36             | MAX_REQ_CUR | R   | Max requested operation current (MISMATCH = 1) in a 20mA unit; only valid when GIVEBACK_FLAG = 0; fixed PDO |                                |           |                                 |                                 |          |                              |           |
| 37             | MFR_ID      | R   | MANUFACTURER_ID <sup>(17)</sup> : 0000 1001b                                                                |                                |           |                                 |                                 |          |                              |           |
| 38             | DEV_ID      | R   | DEVICE_ID <sup>(17)</sup> : 0101 1000b                                                                      |                                |           |                                 |                                 |          |                              |           |
| 39             | CLK_ON      | W   | Write 1b to enable clock                                                                                    |                                |           |                                 |                                 |          |                              |           |

### Note:

<sup>(17)</sup> This register can be configured via the one-time programmable (OTP) memory.

## REGISTER MAP

The default register values are based on the MPQ4242B-0000.

### PDO\_SET1 (0x00)

**Format:** Unsigned binary

The PDO\_SET1 command enables PDOx (where x = 2–7). PDO1 is fixed as a 5V power data object, and it is always enabled. Its voltage can be changed via VBUS\_VOLTAGE.

| Bits | Access | Bit Name | Default | Description                                                             |
|------|--------|----------|---------|-------------------------------------------------------------------------|
| 7:6  | R      | RESERVED | N/A     | Reserved.                                                               |
| 5    | R/W    | PDO7_EN  | 1b      | Enables the PDO7's power object setting.<br>0b: Disabled<br>1b: Enabled |
| 4    | R/W    | PDO6_EN  | 1b      | Enables the PDO6's power object setting.<br>0b: Disabled<br>1b: Enabled |
| 3    | R/W    | PDO5_EN  | 1b      | Enables the PDO5's power object setting.<br>0b: Disabled<br>1b: Enabled |
| 2    | R/W    | PDO4_EN  | 1b      | Enables the PDO4's power object setting.<br>0b: Disabled<br>1b: Enabled |
| 1    | R/W    | PDO3_EN  | 1b      | Enables the PDO3's power object setting.<br>0b: Disabled<br>1b: Enabled |
| 0    | R/W    | PDO2_EN  | 1b      | Enables the PDO2's power object setting.<br>0b: Disabled<br>1b: Enabled |

### PDO\_SET2 (0x01)

**Format:** Unsigned binary

The PDO\_SET2 command configures PDOx (where x = 2–7) to be fixed PDO or APDO.

| Bits | Access | Bit Name  | Default | Description                                                |
|------|--------|-----------|---------|------------------------------------------------------------|
| 7:6  | R      | RESERVED  | N/A     | Reserved.                                                  |
| 5    | R/W    | PDO7_TYPE | 1b      | Sets the PDO7's power object.<br>0b: Fixed PDO<br>1b: APDO |
| 4    | R/W    | PDO6_TYPE | 1b      | Sets the PDO6's power object.<br>0b: Fixed PDO<br>1b: APDO |
| 3    | R/W    | PDO5_TYPE | 1b      | Sets the PDO5's power object.<br>0b: Fixed PDO<br>1b: APDO |
| 2    | R/W    | PDO4_TYPE | 0b      | Sets the PDO4's power object.<br>0b: Fixed PDO<br>1b: APDO |

|   |     |           |    |                                                            |
|---|-----|-----------|----|------------------------------------------------------------|
| 1 | R/W | PDO3_TYPE | 0b | Sets the PDO3's power object.<br>0b: Fixed PDO<br>1b: APDO |
| 0 | R/W | PDO2_TYPE | 0b | Sets the PDO2's power object.<br>0b: Fixed PDO<br>1b: APDO |

### HOST\_SET (0x02)

**Format:** Unsigned binary

The HOST\_SET command controls certain functions.

| Bits | Access | Bit Name              | Default | Description                                                                                                         |
|------|--------|-----------------------|---------|---------------------------------------------------------------------------------------------------------------------|
| 7    | R/W    | COMMUNICA_ CAPAB_HOST | 0b      | Sets the USB communication capabilities for the USB host.<br>0b: Other<br>1b: The product can enumerate USB devices |
| 6:5  | R/W    | PRODUCT_TYPE_ DFP     | 11b     | Sets the product type (DFP).<br>00b: Undefined<br>01b: PDUSB hub<br>10b: PDUSB host<br>11b: Power brick             |
| 4:2  | R/W    | HOST_CAPABILITY       | 000b    | Sets the DFP VDO message's B26...24 bits.                                                                           |
| 1:0  | R/W    | PORT_NUMBER           | 01      | Sets the unique port number to identify a specific port on a multi-port device.                                     |

### PDO\_I1 (0x03)

**Format:** Unsigned binary

The PDO\_I1 command sets PDO1's maximum output current.

| Bits | Access | Bit Name              | Default | Description                                                                                                                                                                                                                                                                       |
|------|--------|-----------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | PDO1_CURRENT_ SETTING | 0x96    | Sets PDO1's maximum output current setting in 20mA units. The default is 0x96 (3A). When this bit is set to exceed 3A, the MPQ4242B checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability. |

### PDO\_V2\_L (0x04)

**Format:** Unsigned binary

If PDO2\_TYPE is set to 0b (fixed PDO), the PDO\_V2\_L command sets PDO2's output voltage. The default for PDO2\_TYPE is 0b.

| Bits | Access | Bit Name              | Default | Description                                                                                                         |
|------|--------|-----------------------|---------|---------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | PDO2_VOLTAGE_ SETTING | 0x5A    | Sets PDO2's output voltage in 100mV units. The default is 0x5A (9V). The maximum voltage that can be set is 22.97V. |

If PDO2\_TYPE is set to 1b (APDO), the PDO\_V2\_L command sets PDO2's minimum output voltage.

| Bits | Access | Bit Name              | Description                                      |
|------|--------|-----------------------|--------------------------------------------------|
| 7:0  | R/W    | PDO2_MINIMUM_ VOLTAGE | Sets PDO2's minimum voltage in 100mV increments. |

### PDO\_V2\_H (0x05)

**Format:** Unsigned binary

If PDO2\_TYPE is set to 1b (APDO), the PDO\_V2\_H command sets PDO2's maximum output voltage.

| Bits | Access | Bit Name             | Description                                      |
|------|--------|----------------------|--------------------------------------------------|
| 7:0  | R/W    | PDO2_MAXIMUM_VOLTAGE | Sets PDO2's maximum voltage in 100mV increments. |

### PDO\_I2 (0x06)

**Format:** Unsigned binary

The PDO\_I2 command sets PDO2's maximum output current.

| Bits | Access | Bit Name             | Default | Description                                                                                                                                                                                                                                                                                                                                 |
|------|--------|----------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | PDO2_CURRENT_SETTING | 0x96    | Sets PDO2's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 0x96 (3A and fixed PDO). When this bit is set to exceed 3A, the MPQ4242B checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability. |

### PDO\_V3\_L (0x07)

**Format:** Unsigned binary

If PDO3\_TYPE is set to 0b (fixed PDO), the PDO\_V3\_L command sets PDO3's output voltage. The default for PDO3\_TYPE is 0b.

| Bits | Access | Bit Name             | Default | Description                                                                                                          |
|------|--------|----------------------|---------|----------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | PDO3_VOLTAGE_SETTING | 0x96    | Sets PDO3's output voltage in 100mV units. The default is 0x96 (15V). The maximum voltage that can be set is 22.97V. |

If PDO3\_TYPE is set to 1b (APDO), the PDO\_V3\_L command sets PDO3's minimum output voltage.

| Bits | Access | Bit Name             | Description                                      |
|------|--------|----------------------|--------------------------------------------------|
| 7:0  | R/W    | PDO3_MINIMUM_VOLTAGE | Sets PDO3's minimum voltage in 100mV increments. |

### PDO\_V3\_H (0x08)

**Format:** Unsigned binary

If PDO3\_TYPE is set to 1b (APDO), the PDO\_V3\_H command sets PDO3's maximum output voltage.

| Bits | Access | Bit Name             | Description                                      |
|------|--------|----------------------|--------------------------------------------------|
| 7:0  | R/W    | PDO3_MAXIMUM_VOLTAGE | Sets PDO3's maximum voltage in 100mV increments. |

### PDO\_I3 (0x09)

**Format:** Unsigned binary

The PDO\_I3 command sets PDO3's maximum output current.

| Bits | Access | Bit Name             | Default | Description                                                                                                                                                                                                                                                                                                                   |
|------|--------|----------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | PDO3_CURRENT_SETTING | 0x96    | Sets PDO3's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 0x96 (3A). When this bit is set to exceed 3A, the MPQ4242B checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability. |

### PDO\_V4\_L (0x0A)

**Format:** Unsigned binary

If PDO4\_TYPE is set to 0b (fixed PDO), the PDO\_V4\_L command sets PDO4's output voltage. The default for PDO4\_TYPE is 0b.

| Bits | Access | Bit Name             | Default | Description                                                                                                          |
|------|--------|----------------------|---------|----------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | PDO4_VOLTAGE_SETTING | 0xC8    | Sets PDO4's output voltage in 100mV units. The default is 0xC8 (20V). The maximum voltage that can be set is 22.97V. |

If PDO4\_TYPE is set to 1b (APDO), the PDO\_V4\_L command sets PDO4's minimum output voltage.

| Bits | Access | Bit Name             | Description                                      |
|------|--------|----------------------|--------------------------------------------------|
| 7:0  | R/W    | PDO4_MINIMUM_VOLTAGE | Sets PDO4's minimum voltage in 100mV increments. |

### PDO\_V4\_H (0x0B)

**Format:** Unsigned binary

If PDO4\_TYPE is set to 1b (APDO), the PDO\_V4\_H command sets PDO4's maximum output voltage.

| Bits | Access | Bit Name             | Description                                      |
|------|--------|----------------------|--------------------------------------------------|
| 7:0  | R/W    | PDO4_MAXIMUM_VOLTAGE | Sets PDO4's maximum voltage in 100mV increments. |

### PDO\_I4 (0x0C)

**Format:** Unsigned binary

The PDO\_I4 command sets PDO4's maximum output current.

| Bits | Access | Bit Name             | Default | Description                                                                                                                                                                                                                                                                                                                                 |
|------|--------|----------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | PDO4_CURRENT_SETTING | 0x96    | Sets PDO4's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 0x96 (3A and fixed PDO). When this bit is set to exceed 3A, the MPQ4242B checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability. |

### PDO\_V5\_L (0x0D)

**Format:** Unsigned binary

If PDO5\_TYPE is set to 0b (fixed PDO), the PDO\_V5\_L command sets PDO5's output voltage.

| Bits | Access | Bit Name             | Description                                |
|------|--------|----------------------|--------------------------------------------|
| 7:0  | R/W    | PDO5_VOLTAGE_SETTING | Sets PDO5's output voltage in 100mV units. |

If PDO5\_TYPE is set to 1b (APDO), the PDO\_V5\_L command sets PDO5's minimum output voltage. The default for PDO5\_TYPE is 1b.

| Bits | Access | Bit Name             | Default | Description                                                                  |
|------|--------|----------------------|---------|------------------------------------------------------------------------------|
| 7:0  | R/W    | PDO5_MINIMUM_VOLTAGE | 0x21    | Sets PDO5's minimum voltage in 100mV increments. The default is 0x21 (3.3V). |

### PDO\_V5\_H (0x0E)

**Format:** Unsigned binary

If PDO5\_TYPE is set to 1b (APDO), the PDO\_V5\_H command sets PDO5's maximum output voltage.

| Bits | Access | Bit Name             | Default | Description                                                                 |
|------|--------|----------------------|---------|-----------------------------------------------------------------------------|
| 7:0  | R/W    | PDO5_MAXIMUM_VOLTAGE | 0x6E    | Sets PDO5's maximum voltage in 100mV increments. The default is 0x6E (11V). |

### PDO\_I5 (0x0F)

**Format:** Unsigned binary

The PDO\_I5 command sets PDO5's maximum output current.

| Bits | Access | Bit Name             | Default | Description                                                                                                                                                                                                                                                                                                                            |
|------|--------|----------------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | PDO5_CURRENT_SETTING | 0x3C    | Sets PDO5's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 0x3C (3A and APDO). When this bit is set to exceed 3A, the MPQ4242B checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability. |

### PDO\_V6\_L (0x10)

**Format:** Unsigned binary

If PDO6\_TYPE is set to 0b (fixed PDO), the PDO\_V6\_L command sets PDO6's output voltage.

| Bits | Access | Bit Name             | Description                                |
|------|--------|----------------------|--------------------------------------------|
| 7:0  | R/W    | PDO6_VOLTAGE_SETTING | Sets PDO6's output voltage in 100mV units. |

If PDO6\_TYPE is set to 1b (APDO), the PDO\_V6\_L command sets PDO6's minimum output voltage. The default for PDO6\_TYPE is 1b.

| Bits | Access | Bit Name             | Default | Description                                                                  |
|------|--------|----------------------|---------|------------------------------------------------------------------------------|
| 7:0  | R/W    | PDO6_MINIMUM_VOLTAGE | 0x21    | Sets PDO6's minimum voltage in 100mV increments. The default is 0x21 (3.3V). |

### PDO\_V6\_H (0x11)

**Format:** Unsigned binary

If PDO6\_TYPE is set to 1b (APDO), the PDO\_V6\_H command sets PDO6's maximum output voltage.

| Bits | Access | Bit Name             | Default | Description                                                                 |
|------|--------|----------------------|---------|-----------------------------------------------------------------------------|
| 7:0  | R/W    | PDO6_MAXIMUM_VOLTAGE | 0xA0    | Sets PDO6's maximum voltage in 100mV increments. The default is 0xA0 (16V). |

### PDO\_I6 (0x12)

**Format:** Unsigned binary

The PDO\_I6 command sets PDO6's output current.

| Bits | Access | Bit Name             | Default | Description                                                                                                                                                                                                                                                                                                                            |
|------|--------|----------------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | PDO6_CURRENT_SETTING | 0x3C    | Sets PDO6's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 0x3C (3A and APDO). When this bit is set to exceed 3A, the MPQ4242B checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability. |

### PDO\_V7\_L (0x13)

**Format:** Unsigned binary

If PDO7\_TYPE is set to 0b (fixed PDO), the PDO\_V7\_L command sets PDO7's output voltage.

| Bits | Access | Bit Name             | Description                                    |
|------|--------|----------------------|------------------------------------------------|
| 7:0  | R/W    | PDO7_VOLTAGE_SETTING | Sets the PDO7's output voltage in 100mV units. |

If PDO7\_TYPE is set to 1b (APDO), the PDO\_V7\_L command sets PDO7's minimum output voltage. The default for PDO7\_TYPE is 1b.

| Bits | Access | Bit Name             | Default | Description                                                                  |
|------|--------|----------------------|---------|------------------------------------------------------------------------------|
| 7:0  | R/W    | PDO7_MINIMUM_VOLTAGE | 0x21    | Sets PDO7's minimum voltage in 100mV increments. The default is 0x21 (3.3V). |

### PDO\_V7\_H (0x14)

**Format:** Unsigned binary

If PDO7\_TYPE is set to 1b (APDO), the PDO\_V7\_H command sets PDO7's maximum output voltage.

| Bits | Access | Bit Name             | Default | Description                                                                 |
|------|--------|----------------------|---------|-----------------------------------------------------------------------------|
| 7:0  | R/W    | PDO7_MAXIMUM_VOLTAGE | 0xD2    | Sets PDO7's maximum voltage in 100mV increments. The default is 0xD2 (21V). |

### PDO\_I7 (0x15)

**Format:** Unsigned binary

The PDO\_I7 command sets PDO7's maximum output current.

| Bits | Access | Bit Name             | Default | Description                                                                                                                                                                                                                                                                                                                            |
|------|--------|----------------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | PDO7_CURRENT_SETTING | 0x3C    | Sets PDO7's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 0x3C (3A and APDO). When this bit is set to exceed 3A, the MPQ4242B checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability. |

### PD\_CTL1 (0x16)

**Format:** Unsigned binary

The PD\_CTL1 command controls certain functions.

| Bits                     | Access   | Bit Name                 | Default                              | Description                                                                                                                                                                                                                                                                                                                                                                                                                          |        |   |   |   |   |                          |   |    |    |       |      |          |                          |                                      |                                                           |
|--------------------------|----------|--------------------------|--------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|---|---|---|---|--------------------------|---|----|----|-------|------|----------|--------------------------|--------------------------------------|-----------------------------------------------------------|
| 7                        | R/W      | CDP_EN                   | 0b                                   | Selects the charging downstream port (CDP) mode. If this bit is set to 1, all the DCP, QC, and Apple modes are disabled. The device only works in CDP handshaking mode.                                                                                                                                                                                                                                                              |        |   |   |   |   |                          |   |    |    |       |      |          |                          |                                      |                                                           |
| 6:5                      | R/W      | LEGACY_CHARGING_MODE_SEL | 00b                                  | Sets certain values based on the truth table below. <table border="1"> <tr> <th>CDP_EN</th><th>1</th><th>0</th><th>0</th><th>0</th></tr> <tr> <th>LEGACY_CHARGING_MODE_SEL</th><td>X</td><td>00</td><td>01</td><td>10/11</td></tr> <tr> <th>Mode</th><td>CDP mode</td><td>All DCP modes are active</td><td>Apple mode and BC1.2 mode are active</td><td>Only BC1.2 is active; Apple mode and QC mode are disabled</td></tr> </table> | CDP_EN | 1 | 0 | 0 | 0 | LEGACY_CHARGING_MODE_SEL | X | 00 | 01 | 10/11 | Mode | CDP mode | All DCP modes are active | Apple mode and BC1.2 mode are active | Only BC1.2 is active; Apple mode and QC mode are disabled |
| CDP_EN                   | 1        | 0                        | 0                                    | 0                                                                                                                                                                                                                                                                                                                                                                                                                                    |        |   |   |   |   |                          |   |    |    |       |      |          |                          |                                      |                                                           |
| LEGACY_CHARGING_MODE_SEL | X        | 00                       | 01                                   | 10/11                                                                                                                                                                                                                                                                                                                                                                                                                                |        |   |   |   |   |                          |   |    |    |       |      |          |                          |                                      |                                                           |
| Mode                     | CDP mode | All DCP modes are active | Apple mode and BC1.2 mode are active | Only BC1.2 is active; Apple mode and QC mode are disabled                                                                                                                                                                                                                                                                                                                                                                            |        |   |   |   |   |                          |   |    |    |       |      |          |                          |                                      |                                                           |

|     |     |                 |     |                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-----|-----|-----------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | R/W | USB_COMMUNICATE | 0b  | Sets whether USB communication is supported.<br>0b: USB communication is not supported<br>1b: USB communication is supported                                                                                                                                                                                                                                                                                                     |
| 3   | R/W | NTC_CTL_RP      | 0b  | Selects whether the device enters USB Type-C 3A or 1.5A mode if an NTC or over-temperature warning (OTW) event occurs. In 5V @ 3A USB Type-C mode, the R <sub>P</sub> pull-up current is 330μA and the R <sub>D</sub> detection range is between 0.8V and 2.6V.<br>0b: PDP <15W, and R <sub>P</sub> = 1.5A; otherwise, R <sub>P</sub> = 3A<br>1b: The device enters 1.5A USB Type-C mode if an NTC or OTW1/OTW2 condition occurs |
| 2:1 | R/W | TOUCH_TEMP      | 00b | Sets the touch temperature default value to 0, 1, or 2. These bits are defined in the SOURCE_CAPABILITIES_EXTENDED message byte 20, bits[1:0].                                                                                                                                                                                                                                                                                   |
| 0   | R/W | TYPE-C_MODE     | 0b  | Selects 3A or 1.5A Type-C mode. In 5V @ 3A USB Type-C mode, the R <sub>P</sub> pull-up current is 330μA, and the R <sub>D</sub> detection range is between 0.85V and 2.45V.<br>0b: 3A USB Type-C mode<br>1b: 1.5A USB Type-C mode                                                                                                                                                                                                |

### PD\_CTL2 (0x17)

**Format:** Unsigned binary

The PD\_CTL2 command controls certain functions.

| Bits | Access | Bit Name      | Default | Description                                                                                                                                                                             |
|------|--------|---------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | R/W    | HDRST         | 0b      | Sends a hard reset command.<br>0b: Normal state<br>1b: Send a hard reset command to the sink. After the HDRST message is sent, this bit automatically resets to 0b                      |
| 6    | R/W    | USB_SUSPEND   | 0b      | Sets whether the USB suspend function is supported.<br>0b: Not supported<br>1b: Supported                                                                                               |
| 5:3  | R/W    | TOUCH_CURRENT | 000b    | Sets the values for bits[2:0] of the touch current, defined in SOURCE_CAPABILITIES_EXTENDED message byte 13, bits[2:0]. Bit[5] of this command sets the touch current value for bit[2]. |
| 2:0  | R/W    | COMPLIANCE    | 101b    | Sets the values for bits[2:0] of the compliance, defined in SOURCE_CAPABILITIES_EXTENDED message byte 12, bits[2:0]. Bit[2] of this command sets the compliance value for bit[2].       |

### PWR\_CTL1 (0x18)

**Format:** Unsigned binary

The PWR\_CTL1 command controls certain functions.

| Bits | Access | Bit Name | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|------|--------|----------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | R/W    | EN       | 1b      | Determines whether I <sup>2</sup> C control turns the part on or off. When the external EN pin is low, the converter is off, and the I <sup>2</sup> C shuts down. When the EN pin is high, the EN bit takes over.<br>0b: The device is off but the I <sup>2</sup> C register does not reset. In addition, the USB Type-C logic is off, and the system clock turns off to save quiescent current (I <sub>Q</sub> )<br>1b: If the USB Type-C receptacle is disconnected, the system clock remains off to save I <sub>Q</sub> |

|     |     |                |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|-----|----------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6   | R/W | MODE           | 1b  | <p>Sets the PWM mode.</p> <p>0b: Enables auto-PFM/PWM mode<br/>1b: Forced PWM mode</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 5:4 | R/W | FREQ           | 01b | <p>Sets the switching frequency (<math>f_{sw}</math>).</p> <p>00b: 250kHz<br/>01b: 420kHz<br/>10b/11b: Reserved</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 3   | R/W | DITHER         | 0b  | <p>Enables the frequency spread spectrum (FSS) function.</p> <p>0b: Disabled<br/>1b: Enabled</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 2:1 | R/W | LINE_DROP_COMP | 00b | <p>Sets the output voltage compensation vs. the load feature. The compensation amplitude is fixed for any output voltage. Set 0x1E, bit[6] = 1 to enable an additional compensation voltage. Line drop compensation has a maximum clamp at 800mV, regardless of the output current.</p> <p>Line drop compensation is disabled once the MPQ4242B enters PPS mode. Line drop compensation can be enabled in PPS mode through the factory OTP trim.</p> <p>00b: No compensation<br/>01b: <math>V_{OUT}</math> compensates 150mV at a 3A <math>I_{OUT}</math><br/>10b: <math>V_{OUT}</math> compensates 300mV at a 3A <math>I_{OUT}</math><br/>11b: <math>V_{OUT}</math> compensates 600mV at a 3A <math>I_{OUT}</math></p> |
| 0   | R/W | SLEW_RATE      | 1b  | <p>Sets the output slew rate to adjust <math>V_{OUT}</math>. The slew rate can be calculated with the following equation:</p> $V_{OUT} \text{ Slew Rate} = V_{REF} \text{ Slew Rate} \times \text{Feedback Resistor Ratio} \quad (12.5)$ <p>0b: 0.4mV/<math>\mu</math>s <math>V_{REF}</math> rising slew rate; 0.08mV/<math>\mu</math>s <math>V_{REF}</math> falling slew rate<br/>1b: 0.08mV/<math>\mu</math>s <math>V_{REF}</math> rising slew rate; 0.08mV/<math>\mu</math>s <math>V_{REF}</math> falling slew rate</p>                                                                                                                                                                                              |

## PWR\_CTL2 (0x19)

**Format:** Unsigned binary

The PWR\_CTL2 command controls certain functions.

| Bits | Access | Bit Name    | Default | Description                                                                                                                                                                                                                                                                                                                                                                                            |
|------|--------|-------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | R/W    | EN_VBUS     | 0b      | <p>Enables the power converter's output directly, even if there is no USB Type-C sink device.</p> <p>0b: The power converter's on/off status is controlled by the USB Type-C controller<br/>1b: The power converter is enabled</p>                                                                                                                                                                     |
| 6    | R/W    | PPS_MIN_SEL | 1b      | <p>Sets the <math>V_{BUS}</math> under-voltage (UV) threshold: This bit also controls the 3.3V or 5V minimum PPS voltage.</p> <p>0b: The <math>V_{BUS}</math> UV falling threshold is 4.5V, with 5% accuracy for 5V minimum PPS voltage applications<br/>1b: The <math>V_{BUS}</math> UV falling threshold is 2.97V (3.135V maximum), with 4.5% accuracy for 3.3V minimum PPS voltage applications</p> |

|     |     |                |      |                                                                                                                                                                                                                                                           |
|-----|-----|----------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5:3 | R/W | OTW1_THRESHOLD | 100b | Sets the over-temperature warning (OTW1) threshold. The OTW1 threshold has a 20°C hysteresis for recovery.<br><br>000: Disable the OTW1 function<br>001b: 105°C<br>010b: 115°C<br>011b: 125°C<br>100b: 135°C<br>101b: 145°C<br>110b: 155°C<br>111b: 165°C |
| 2:0 | R/W | OTP_THRESHOLD  | 010b | Sets the OT shutdown threshold. OT shutdown has a 20°C hysteresis for recovery.<br><br>000b: 155°C<br>001b: 165°C<br>010b: 175°C<br>011b: 185°C<br>100b~111b: Reserved                                                                                    |

### VOUT\_L (0x1A) and VOUT\_H (0x1B)

**Format:** Linear

The VOUT\_L and VOUT\_H registers set  $V_{OUT}$  following an 11-bit direct format.

| Name          | VOUT                            |    |    |    |    |               |     |     |              |     |     |     |     |             |     |     |
|---------------|---------------------------------|----|----|----|----|---------------|-----|-----|--------------|-----|-----|-----|-----|-------------|-----|-----|
| Format        | Direct, unsigned binary integer |    |    |    |    |               |     |     |              |     |     |     |     |             |     |     |
| Register Name | N/A                             |    |    |    |    | VOUT_H[7:0]   |     |     |              |     |     |     |     | VOUT_L[2:0] |     |     |
| Bit           | 15                              | 14 | 13 | 12 | 11 | 10            | 9   | 8   | 7            | 6   | 5   | 4   | 3   | 2           | 1   | 0   |
| Access        | N/A                             |    |    |    |    | R/W           | R/W | R/W | R/W          | R/W | R/W | R/W | R/W | R/W         | R/W | R/W |
| Function      | N/A                             |    |    |    |    | Data Bit High |     |     | Data Bit Low |     |     |     |     |             |     |     |
| Default (5V)  | N/A                             |    |    |    |    | 250 Integer   |     |     |              |     |     |     |     |             |     |     |

The real-world  $V_{OUT}$  (in V) can be calculated with Equation (2):

$$V_{OUT} (V) = V / 100 + 2.5 \quad (2)$$

Where  $V$  is an 11-bit, unsigned binary integer from VOUT[10:0] (ranging between 0 and 2047). The  $V_{OUT}$  resolution (or minimum step) is 10mV. The MPQ4242B has a feedback network from the OUT pin to the internal FB reference voltage. The feedback resistor ratio is  $V_{OUT} / V_{REF} = 12.5$ .

The MPQ4242B can enable its output directly, even there is no USB Type-C sink device, by following the steps below:

1. Write CLOCK\_ON (0x39) = 0x01 to enable the digital clock.
2. Write EN\_VBUS (0x19, bit[7]) = 1b to enable the MPQ4242B's output directly. The default  $V_{OUT}$  is 5V, and the default  $I_{OUT\_LIM}$  is 3.6A.
3. Write I2C\_CTL\_VOUT\_EN (0x1F, bit[1]) = 1b to change  $V_{OUT}$  and  $I_{OUT\_LIM}$ . This bit enables the I<sup>2</sup>C registers VOUT\_L (0x1A), VOUT\_H (0x1B), IOUT\_LIM (0x1C), and GO\_BIT (0x1D).
4. Set GO\_BIT = 1 to start the  $V_{OUT}$  and  $I_{OUT\_LIM}$  change based on VOUT\_L (0x1A), VOUT\_H (0x1B), and IOUT\_LIM (0x1C).

### IOUT\_LIM (0x1C)

**Format:** Unsigned binary

The IOUT\_LIM command configures the CC current limit for the buck-boost output.

| Bits | Access | Bit Name | Default | Description |
|------|--------|----------|---------|-------------|
| 7    | R      | RESERVED | N/A     | Reserved.   |

|     |     |          |      |                                                                                                                                                                                                                               |
|-----|-----|----------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6:0 | R/W | IOUT_LIM | 0x48 | Sets the CC current limit for the buck-boost output CC, in 50mA units. The default is 0x48 (3.6A). When changing IOUT_LIM, the internal I <sub>REF</sub> should have some slew rate control. The ramping slew rate is 1mA/μs. |
|-----|-----|----------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

### CTL\_SYS0 (0x1D)

**Format:** Unsigned binary

The CTL\_SYS0 command controls certain functions.

| Bits | Access | Bit Name | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|--------|----------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6  | R      | RESERVED | N/A     | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 0    | R/W    | GO_BIT   | 0b      | Controls when the MPQ4242B starts to change V <sub>OUT</sub> and I <sub>OUT_LIM</sub> . Set GO_BIT to 1 to start the output / CC limit change based on VOUT_L (0x1A), VOUT_H (0x1B), and IOUT_LIM (0x1C). When V <sub>OUT</sub> or I <sub>OUT_LIM</sub> finishes changing (the internal V <sub>REF</sub> steps to the target V <sub>REF</sub> ), GO_BIT automatically resets to 0. This prevents false operation of the V <sub>OUT</sub> / I <sub>OUT_LIM</sub> scale.<br><br>0b: V <sub>OUT</sub> and I <sub>OUT_LIM</sub> do not change<br>1b: V <sub>OUT</sub> and I <sub>OUT_LIM</sub> change based on their register(s) |

### CTL\_SYS1 (0x1E)

**Format:** Unsigned binary

The CTL\_SYS1 command controls certain functions.

| Bits | Access | Bit Name                          | Default | Description                                                                                                                                                                                                                        |                                     |
|------|--------|-----------------------------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------|
| 7    | R/W    | SEND_SRC_CAP                      | 0b      | Sends the source capability message. Write 1 to this bit to force the MPQ4242B to send an SRC_CAP message. This bit automatically resets to 0 after the SRC_CAP message is sent out.                                               |                                     |
| 6    | R/W    | ADDITIONAL_LINE_DROP_COMPENSATION | 0b      | Enables an additional 150mV for line drop compensation based on the set-up for 0x18, bits[2:1]. This bit is active only when line drop compensation is active.<br><br>0b: Disabled<br>1b: Enabled                                  |                                     |
| 5:4  | R/W    | EN_OFF_TIMER                      | 00b     | Sets the EN off time. There is a shutdown delay time after the EN pin goes low. If EN pulls high while the counter increases, the counter is reset.<br><br>00b: No delay<br>01b: 20 minutes<br>10b: 40 minutes<br>11b: 120 minutes |                                     |
| 3:0  | R/W    | I2C_SLAVE_ADDRESS                 | 0001b   | Set the I <sup>2</sup> C slave address's A4 to A1 bits.                                                                                                                                                                            |                                     |
|      |        |                                   |         | I <sup>2</sup> C Address (A7:A1)                                                                                                                                                                                                   |                                     |
|      |        |                                   |         | Binary                                                                                                                                                                                                                             | Hex                                 |
|      |        |                                   |         | 1100 001 (Default)                                                                                                                                                                                                                 | 61h                                 |
|      |        |                                   |         | I <sup>2</sup> C adjustable for A4~A1                                                                                                                                                                                              | Set by I2C_SLAVE_ADDRESS, bits[3:0] |

## CTL\_SYS2 (0x1F)

**Format:** Unsigned binary

The CTL\_SYS2 command controls certain functions.

| Bits | Access | Bit Name        | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------|--------|-----------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5  | R/W    | GPIO1           | 000b    | <p>Sets the GPIO1 pin function.</p> <p>000b: POWER_SHARE1. See the GPIO1_POWER_SHARE section on page 28 for more details</p> <p>001b: GATE. Provides a GND-to-battery short protection drive</p> <p>010b: FAULT, open-drain output. Pulls low to indicate if a fault has occurred, such as OCP, OTP, and GND/DP/DM/CCx to battery short</p> <p>011b: NTC2. When this function is selected, the power share input is controlled by NTC2. The NTC_MODE bit does not control the NTC2 behavior. NTC_HYSTERESIS sets the hysteresis</p> <p>100/101b: ATTACH_FLT_ALT, open-drain output. This pin pulls low for 12μs at the connection rising edge if no fault event has occurred. Pulls low if a fault occurs</p> <p>111b: Current monitor output. Represents the signal between ISENS+ and ISENS-</p>                                                                                                                            |
| 4:2  | R/W    | GPIO2           | 000b    | <p>Sets the GPIO2 pin function. The default is 000.</p> <p>000b: Reserved</p> <p>001b: POL, open-drain output. Indicates the USB Type-C plug's polarity. When CC1 is selected as the CC line, POL pulls low; when CC2 is selected as the CC line or disconnected, POL is an open drain</p> <p>010b: NTC. Functions as an input pin to sense the external thermal. See the NTC Function section on page 27 for more details</p> <p>011b: VCONN_IN. Apply a 5V / 1.5W power supply on this pin</p> <p>100b: LED_PWM output. It is a 25kHz PWM signal output with an adjustable duty cycle. See the CTL_SYS18 (0x2F) section on page 52 for more details</p> <p>101b: ATTACH. Indicates if the USB Type-C port is connected. Only high or low for two states</p> <p>110b: POWER_SHARE2. GPIO2 power sharing is triggered when the GPIO2 voltage exceeds 1.87V. See the GPIO2_POWER_SHARE section on page 29 for more details</p> |
| 1    | R/W    | I2C_CTL_VOUT_EN | 0b      | <p>Enables the I<sup>2</sup>C registers 0x1A, 0x1B, 0x1C, and 0x1D. The default is 0.</p> <p>0b: V<sub>OUT</sub> and I<sub>OUT_LIM</sub> do not change, even after sending commands to VOUT_L, VOUT_H, GO_BIT, and IOUT_LIM. V<sub>OUT</sub> is controlled by the USB PD engine</p> <p>1b: V<sub>OUT</sub> changes based on the VOUT/IOUT_LIM register setting</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 0    | R      | RESERVED        | N/A     | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

## CTL\_SYS3 (0x20)

**Format:** Unsigned binary

The CTL\_SYS3 command controls certain functions.

| Bits | Access | Bit Name   | Default | Description                                                                                                                                                                                                                                                     |
|------|--------|------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | PS_PDP_THD | 0x5A    | <p>Sets the threshold to which the PDO power rating is reduced. When the GPIOx pin (if set to the POWER_SHARE function) pulls low, the MPQ4242B's PD power drops to the values set by PS_PDP_THD. The default is 45W.</p> <p>0x01: 0.5W</p> <p>0xFF: 127.5W</p> |

### CTL\_SYS4 (0x21)

**Format:** Unsigned binary

The CTL\_SYS4 command controls certain functions.

| Bits | Access | Bit Name              | Default | Description                                                                                                                                                                                                                                    |
|------|--------|-----------------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | PS_PDP_THD_PDO_SELECT | 0xBE    | Selects which voltage is enabled in the PDO list. See Table 4 on page 29 for more details. The final PDO current is determined by PS_PDP_THD. The default means 4 fixed PDOs: 5V/9V/15V/20V and 3 APDOs: 3.3V to 5.9V/3.3V to 11V/3.3V to 16V. |

### CTL\_SYS5 (0x22)

**Format:** Unsigned binary

The CTL\_SYS5 command controls certain functions.

| Bits | Access | Bit Name            | Default | Description                                                                                                                                                                                                              |
|------|--------|---------------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | R      | RESERVED            | N/A     | Reserved.                                                                                                                                                                                                                |
| 6    | R/W    | PPS_3A_5A           | 0b      | Sets the maximum current for APDO after entering a power sharing, V <sub>BATT</sub> low, OTW, or NTC state.<br>0b: 3A<br>1b: 5A (requires 5A cable)                                                                      |
| 5:4  | R/W    | CC_BLANK_TIMER      | 10b     | Sets the blank time when the output CC over-current condition is reached.<br>00b: No additional CC blank timer<br>01b: 2ms<br>10b: 16ms<br>11b: 32ms                                                                     |
| 3:2  | R      | RESERVED            | N/A     | Reserved.                                                                                                                                                                                                                |
| 1:0  | R/W    | PD_CAP_PEAK_CURRENT | 11b     | Enables the peak current 1, 2, and 3 capabilities in the SOURCE_CAP_EXTEND message.<br>00b: Not supported<br>01b: Support peak current 1<br>10b: Support peak currents 1 and 2<br>11b: Support peak currents 1, 2, and 3 |

### CTL\_SYS6 (0x23)

**Format:** Unsigned binary

The CTL\_SYS6 command controls certain functions.

| Bits | Access | Bit Name       | Default | Description                                                                                                                                                                            |
|------|--------|----------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | VBATT_LOW1_PDP | 0x5A    | Sets the maximum power rating when V <sub>BATT</sub> drops below its first threshold. PDP is reduced to the value set by these bits. The default is 45W.<br>0x01: 0.5W<br>0xFF: 127.5W |

### CTL\_SYS7 (0x24)

**Format:** Unsigned binary

The CTL\_SYS7 command controls certain functions.

| Bits | Access | Bit Name            | Default | Description                                                                                                                                                                                                                               |
|------|--------|---------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | VBATT_L1_PDO_SELECT | 0xBE    | Selects which voltage is enabled in the PDO list. See Table 4 on page 29 for more details. The final PDO current is determined by PDP_L. The default means 4 fixed PDOs: 5V/9V/15V/20V and 3 APDOs: 3.3V to 5.9V/3.3V to 11V/3.3V to 16V. |

### CTL\_SYS8 (0x25)

**Format:** Unsigned binary

The CTL\_SYS8 command controls certain functions.

| Bits | Access | Bit Name       | Default | Description                                                                                                                                                                                 |
|------|--------|----------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | VBATT_LOW2_PDP | 0x1E    | Sets the maximum power rating when V <sub>BATT</sub> drops below its second threshold. PDP is reduced to the value set by these bits. The default is 15W.<br><br>0x01: 0.5W<br>0xFF: 127.5W |

### CTL\_SYS9 (0x26)

**Format:** Unsigned binary

The CTL\_SYS9 command controls certain functions.

| Bits | Access | Bit Name            | Default | Description                                                                                                                                                                                                                               |
|------|--------|---------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | VBATT_L2_PDO_SELECT | 0xBE    | Selects which voltage is enabled in the PDO list. See Table 4 on page 29 for more details. The final PDO current is determined by PDP_L. The default means 4 fixed PDOs: 5V/9V/15V/20V and 3 APDOs: 3.3V to 5.9V/3.3V to 11V/3.3V to 16V. |

### CTL\_SYS10 (0x27)

**Format:** Unsigned binary

The CTL\_SYS10 command controls certain functions.

| Bits | Access | Bit Name | Default | Description                                                                                                                                                                            |
|------|--------|----------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | OTW1_PDP | 0x5A    | Sets the maximum power rating when the die temperature drops below its threshold. PDP is reduced to the value set by these bits. The default is 45W.<br><br>0x01: 0.5W<br>0xFF: 127.5W |

### CTL\_SYS11 (0x28)

**Format:** Unsigned binary

The CTL\_SYS11 command controls certain functions.

| Bits | Access | Bit Name        | Default | Description                                                                                                                                                                                                                               |
|------|--------|-----------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | OTW1_PDO_SELECT | 0xBE    | Selects which voltage is enabled in the PDO list. See Table 4 on page 29 for more details. The final PDO current is determined by PDP_L. The default means 4 fixed PDOs: 5V/9V/15V/20V and 3 APDOs: 3.3V to 5.9V/3.3V to 11V/3.3V to 16V. |

### CTL\_SYS12 (0x29)

**Format:** Unsigned binary

The CTL\_SYS12 command controls certain functions.

| Bits | Access | Bit Name     | Default | Description                                                                                                                                                                            |
|------|--------|--------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | OTW2_NTC_PDP | 0x3C    | Sets the maximum power rating when the die temperature drops below its threshold. PDP is reduced to the value set by these bits. The default is 30W.<br><br>0x01: 0.5W<br>0xFF: 127.5W |

### CTL\_SYS13 (0x2A)

**Format:** Unsigned binary

The CTL\_SYS13 command controls certain functions.

| Bits | Access | Bit Name            | Default | Description                                                                                                                                                                                                                               |
|------|--------|---------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R/W    | OTW2_NTC_PDO_SELECT | 0xBE    | Selects which voltage is enabled in the PDO list. See Table 4 on page 29 for more details. The final PDO current is determined by PDP_L. The default means 4 fixed PDOs: 5V/9V/15V/20V and 3 APDOs: 3.3V to 5.9V/3.3V to 11V/3.3V to 16V. |

### CTL\_SYS14 (0x2B)

**Format:** Unsigned binary

The CTL\_SYS14 command controls certain functions.

| Bits | Access | Bit Name        | Default | Description                                                                                                    |                           |                           |
|------|--------|-----------------|---------|----------------------------------------------------------------------------------------------------------------|---------------------------|---------------------------|
| 7:4  | R/W    | VBATT_LOW_THLD1 | 0100b   | Sets the input voltage detection threshold. See the Low Battery Operation section on page 28 for more details. |                           |                           |
|      |        |                 |         | D[7:4]                                                                                                         | Input Voltage Falling     | Hysteresis                |
|      |        |                 |         | 0000                                                                                                           | This function is disabled | This function is disabled |
|      |        |                 |         | 0001                                                                                                           | 12.6V                     | 800mV                     |
|      |        |                 |         | 0010                                                                                                           | 12.2V                     |                           |
|      |        |                 |         | 0011                                                                                                           | 11.8V                     |                           |
|      |        |                 |         | 0100                                                                                                           | 11.4V                     |                           |
|      |        |                 |         | 0101                                                                                                           | 11V                       |                           |
|      |        |                 |         | 0110                                                                                                           | 10.6V                     |                           |
|      |        |                 |         | 0111                                                                                                           | 10.2V                     |                           |
|      |        |                 |         | 1000                                                                                                           | 9.8V                      |                           |
|      |        |                 |         | 1001                                                                                                           | 9.4V                      |                           |
|      |        |                 |         | 1010                                                                                                           | 9V                        |                           |
|      |        |                 |         | 1011                                                                                                           | 8.6V                      |                           |
|      |        |                 |         | 1100                                                                                                           | 8.2V                      |                           |
|      |        |                 |         | 1101                                                                                                           | 7.8V                      |                           |
|      |        |                 |         | 1110                                                                                                           | 7.4V                      |                           |
| 1111 | 7V     |                 |         |                                                                                                                |                           |                           |

|     |     |                 |       |                                                                                                                |                              |                             |
|-----|-----|-----------------|-------|----------------------------------------------------------------------------------------------------------------|------------------------------|-----------------------------|
| 3:0 | R/W | VBATT_LOW_THLD2 | 1000b | Sets the input voltage detection threshold. See the Low Battery Operation section on page 28 for more details. |                              |                             |
|     |     |                 |       | <b>D[3:0]</b>                                                                                                  | <b>Input Voltage Falling</b> | <b>Input Voltage Rising</b> |
|     |     |                 |       | 0000                                                                                                           | This function is disabled    | This function is disabled   |
|     |     |                 |       | 0001                                                                                                           | 11.8V                        | 800mV                       |
|     |     |                 |       | 0010                                                                                                           | 11.4V                        |                             |
|     |     |                 |       | 0011                                                                                                           | 11V                          |                             |
|     |     |                 |       | 0100                                                                                                           | 10.6V                        |                             |
|     |     |                 |       | 0101                                                                                                           | 10.2V                        |                             |
|     |     |                 |       | 0110                                                                                                           | 9.8V                         |                             |
|     |     |                 |       | 0111                                                                                                           | 9.4V                         |                             |
|     |     |                 |       | 1000                                                                                                           | 9V                           |                             |
|     |     |                 |       | 1001                                                                                                           | 8.6V                         |                             |
|     |     |                 |       | 1010                                                                                                           | 8.2V                         |                             |
|     |     |                 |       | 1011                                                                                                           | 7.8V                         |                             |
|     |     |                 |       | 1100                                                                                                           | 7.4V                         |                             |
|     |     |                 |       | 1101                                                                                                           | 7V                           |                             |
|     |     |                 |       | 1110                                                                                                           | 6.6V                         |                             |
|     |     |                 |       | 1111                                                                                                           | 6.2V                         |                             |

### CTL\_SYS15 (0x2C)

**Format:** Unsigned binary

The CTL\_SYS15 command controls certain functions.

| Bits | Access | Bit Name        | Default | Description                                                                                                                                                                                                                                                         |                           |                           |
|------|--------|-----------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|---------------------------|
| 7:4  | R/W    | VBATT_LOW_THLD3 | 1010b   | Sets the input voltage detection threshold. See the Low Battery Operation section on page 28 for more details.                                                                                                                                                      |                           |                           |
|      |        |                 |         | D[7:4]                                                                                                                                                                                                                                                              | Input Voltage Falling     | Input Voltage Rising      |
|      |        |                 |         | 0000                                                                                                                                                                                                                                                                | This function is disabled | This function is disabled |
|      |        |                 |         | 0001                                                                                                                                                                                                                                                                | 9.8V                      | 800mV                     |
|      |        |                 |         | 0010                                                                                                                                                                                                                                                                | 9.4V                      |                           |
|      |        |                 |         | 0011                                                                                                                                                                                                                                                                | 9V                        |                           |
|      |        |                 |         | 0100                                                                                                                                                                                                                                                                | 8.6V                      |                           |
|      |        |                 |         | 0101                                                                                                                                                                                                                                                                | 8.2V                      |                           |
|      |        |                 |         | 0110                                                                                                                                                                                                                                                                | 7.8V                      |                           |
|      |        |                 |         | 0111                                                                                                                                                                                                                                                                | 7.4V                      |                           |
|      |        |                 |         | 1000                                                                                                                                                                                                                                                                | 7V                        |                           |
|      |        |                 |         | 1001                                                                                                                                                                                                                                                                | 6.6V                      |                           |
|      |        |                 |         | 1010                                                                                                                                                                                                                                                                | 6.2V                      |                           |
|      |        |                 |         | 1011                                                                                                                                                                                                                                                                | 5.8V                      |                           |
|      |        |                 |         | 1100                                                                                                                                                                                                                                                                | 5.4V                      |                           |
|      |        |                 |         | 1101                                                                                                                                                                                                                                                                | 5V                        |                           |
|      |        |                 |         | 1110                                                                                                                                                                                                                                                                | 4.6V                      |                           |
|      |        |                 |         | 1111                                                                                                                                                                                                                                                                | 4.2V                      |                           |
| 3:2  | R/W    | VBATT_LOW_BLK   | 10b     | Sets the V <sub>BATT</sub> low 1, V <sub>BATT</sub> low 2, and V <sub>BATT</sub> low 3 blank times.<br>00b: 10ms<br>01b: 160ms<br>10b: 320ms<br>11b: 640ms. There is an internal trim option to double the blank timer. Contact the factory for a longer blank time |                           |                           |
|      |        |                 |         |                                                                                                                                                                                                                                                                     |                           |                           |
|      |        |                 |         |                                                                                                                                                                                                                                                                     |                           |                           |
|      |        |                 |         |                                                                                                                                                                                                                                                                     |                           |                           |
| 1:0  | R      | RESERVED        | N/A     | Reserved.                                                                                                                                                                                                                                                           |                           |                           |

## CTL\_SYS16 (0x2D)

**Format:** Unsigned binary

The CTL\_SYS16 command controls certain functions.

| Bits | Access | Bit Name       | Default | Description                                                                                                                                                                                                                                                                                                                                                             |
|------|--------|----------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | R      | RESERVED       | N/A     | Reserved.                                                                                                                                                                                                                                                                                                                                                               |
| 6:4  | R/W    | EXT_HS_FET RON | 000b    | <p>Sets the <math>R_{(DS)ON}</math> for the external N-channel MOSFET at a 10V <math>V_{GS}</math>. Select <math>R_{(DS)ON}</math> such that it matches the MOSFET's actual <math>R_{(DS)ON}</math> at a 10V <math>V_{GS}</math>.</p> <p>000b: This function is disabled<br/> 001b: 5mΩ<br/> 010b: 7.5mΩ<br/> 011b: 10mΩ<br/> 100b: 12.5mΩ<br/> 101b~111b: Reserved</p> |
| 3:1  | R/W    | OTW2_THRESHOLD | 110b    | <p>Sets the over-temperature warning (OTW) threshold. The default is 110b. OTW has a 20°C hysteresis for recovery.</p> <p>000b: Disable OTW<br/> 001b: 105°C<br/> 010b: 115°C<br/> 011b: 125°C<br/> 100b: 135°C<br/> 101b: 145°C<br/> 110b: 155°C<br/> 111b: 165°C</p>                                                                                                  |
| 0    | R      | RESERVED       | N/A     | Reserved.                                                                                                                                                                                                                                                                                                                                                               |

## CTL\_SYS17 (0x2E)

**Format:** Unsigned binary

The CTL\_SYS17 command controls certain functions.

| Bits | Access | Bit Name       | Default | Description                                                                                                                                                |
|------|--------|----------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6  | R/W    | PEAK_CL        | 11b     | <p>Sets the high-side peak current limit in boost mode.</p> <p>00b: 8A<br/> 01b: 12A<br/> 10b: 16A<br/> 11b: 20A</p>                                       |
| 5    | R      | RESERVED       | N/A     | Reserved.                                                                                                                                                  |
| 4    | R/W    | NTC_HYSTERESIS | 1b      | <p>Sets the NTC thermal recovery hysteresis. This bit controls both NTC and NTC2.</p> <p>0b: 10%<br/> 1b: 20%</p>                                          |
| 3    | R/W    | NTC_MODE       | 0b      | <p>Sets the behavior if the NTC function is triggered.</p> <p>0b: Shut down the MPQ4242B<br/> 1b: Reduce the PD power to the value set by OTW2_NTC_PDP</p> |
| 2    | R      | RESERVED       | N/A     | Reserved.                                                                                                                                                  |
| 1:0  | R/W    | VBUS_VOLTAGE   | 10b     | <p>Sets the default VBUS voltage.</p> <p>00b: 5V<br/> 01b: 5.05V<br/> 10b: 5.1V<br/> 11b: 5.15V</p>                                                        |

## CTL\_SYS18 (0x2F)

**Format:** Unsigned binary

The CTL\_SYS18 command controls certain functions.

| Bits | Access | Bit Name     | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                    |
|------|--------|--------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | R/W    | OTP_PROGRAM  | 0x0     | Configures the I <sup>2</sup> C register value into the OTP memory cell. A password is required before using the OTP. The OTP can be configured once. Only the MPQ4242B-0000 and OTP_PAGE = 0 can be used to configure the OTP. Write 1 to this bit to implement OTP configurations. After configuring is complete, this bit automatically resets to 0. Apply a 12V V <sub>IN</sub> while configuring the OTP. |
| 6:0  | R/W    | LED_PWM_DUTY | 0x32    | Sets the LED_PWM output duty cycle. The minimum value is 5%; the maximum is 100%.<br>0x05: 5%<br>0x64: 100%                                                                                                                                                                                                                                                                                                    |

## STATUS1 (0x30)

**Format:** Unsigned binary

The STATUS1 command returns 1 data byte with information related to the MPQ4242B.

| Bits | Access | Bit Name    | Description                                                                                                                                                                                |
|------|--------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | R      | ATTACHED    | Returns whether the sink is connected.<br>0b: Disconnected<br>1b: Connected                                                                                                                |
| 6    | R      | NTC2_ENTER  | Returns whether an NTC2 event has occurred.<br>0b: No NTC2 event has occurred<br>1b: An NTC2 event has occurred                                                                            |
| 5    | R      | POL         | Indicates the USB Type-C polarity.<br>0b: CC1 is selected as the CC line<br>1b: CC2 is selected as the CC line                                                                             |
| 4    | R      | SHORT_VBATT | Indicates the output bus voltage status.<br>0b: Normal state<br>1b: DP, DM, CC1, CC2, or USB_GND is shorted with the battery voltage                                                       |
| 3    | R      | FAULT       | Indicates whether a fault has happened. Fault conditions include OCP, OTP, and GND/DP/DM/CCx to battery shorts.<br>0b: No fault has occurred<br>1b: One or more fault events have occurred |
| 2    | R      | OTP_PAGE    | Indicates the current OTP page index.<br>0b: Page 0. No OTP configurations<br>1b: Page 1                                                                                                   |
| 1    | R      | CC_CV       | Indicates the output power status.<br>0b: The output is in a CV state<br>1b: The output is in a CC current limit state                                                                     |
| 0    | R      | NTC_ENTER   | Returns whether an NTC event has occurred.<br>0b: No NTC event has occurred<br>1b: An NTC event has occurred                                                                               |

### STATUS2 (0x31)

**Format:** Unsigned binary

The STATUS2 command returns 1 data byte with contents related to the MPQ4242B. This register is a latch-off register, and it is cleared when it is read.

| Bits | Access | Bit Name           | Description                                                                                                                                                            |
|------|--------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | R      | VBATT_LOW1_FLAG    | Indicates whether V <sub>IN</sub> is below its first lower threshold.<br>0b: V <sub>IN</sub> is not below its threshold<br>1b: V <sub>IN</sub> is below its threshold  |
| 6    | R      | VBATT_LOW2_FLAG    | Indicates whether V <sub>IN</sub> is below its second lower threshold.<br>0b: V <sub>IN</sub> is not below its threshold<br>1b: V <sub>IN</sub> is below its threshold |
| 5    | R      | OTW1               | Indicates whether the device is in an over-temperature warning (OTW1) state.<br>0b: No OTW1 state has been detected<br>1b: The device is in an OTW1 state              |
| 4    | R      | OTW2               | Indicates if the device is in an over-temperature warning (OTW2) state.<br>0b: No OTW2 state has been detected<br>1b: The device is in an OTW2 state                   |
| 3:1  | R      | SELECTED_PDO_INDEX | Returns the sink's selected PDO index.<br>0: No PD contract<br>1~7: PDO1~7 has been selected                                                                           |
| 0    | R      | PDO_TYPE           | Indicates if the sink's selected PDO is fixed PDO or APDO (PPS).<br>0b: Fixed PDO<br>1b: APDO                                                                          |

### STATUS3 (0x32)

**Format:** Unsigned binary

The STATUS3 command returns an instantaneous value. It is a non-latch register.

| Bits | Access | Bit Name       | Description                                                                                                                                                                                                                                                                                                                                                                              |
|------|--------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R      | CONTRACT_POWER | Returns the PD contracted power in 0.5W units. Calculate the fixed PDO value with the following equation:<br>$\text{Fixed PDO} = \text{Voltage} \times \text{Maximum Current};$<br>Calculate the PPS with the following equation:<br>$\text{PPS} = \text{Max Voltage} \times \text{Max Current}.$<br>If there is no PD contract, the value is 7.5W or 15W, depending on R <sub>P</sub> . |

### ID1 (0x33)

**Format:** Unsigned binary

The ID1 command sets the OTP suffix code, which is defined by MPS.

| Bits | Access | Bit Name        | Description                          |
|------|--------|-----------------|--------------------------------------|
| 7:0  | R      | OTP_SUFFIX_CODE | "0x00" represents the MPQ4242B-0000. |

## ID2 (0x34)

**Format:** Unsigned binary

The ID2 command sets the OTP software revision number, as defined by MPS.

| Bits | Access | Bit Name                 | Description                                         |
|------|--------|--------------------------|-----------------------------------------------------|
| 7:0  | R      | OTP_SOFTWARE_REVISION_NO | Stores the revision number, which is the OTP value. |

## FW\_REV (0x35)

**Format:** Unsigned binary

The FW\_REV command controls certain functions.

| Bits | Access | Bit Name          | Description                                                                                                                                                 |
|------|--------|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | R      | MISMATCH          | Indicates if the sink request sets a mismatch bit. Defined in the PD specification.<br>0b: The MISMATCH bit is set to 0<br>1b: The MISMATCH bit is set to 1 |
| 6    | R      | GIVEBACK_FLAG     | This bit is set if the sink requests a GIVEBACK flag.                                                                                                       |
| 5    | R      | CABLE_CAP         | 0b: The cable can handle 3A only<br>1b: 5A cable                                                                                                            |
| 4:0  | R      | FIRMWARE_REVISION | Returns the PD firmware revision number.                                                                                                                    |

## MAX\_REQ\_CUR (0x36)

**Format:** Unsigned binary

The MAX\_REQ\_CUR command controls certain functions.

| Bits | Access | Bit Name    | Description                                                                                                                                                                |
|------|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | R      | MAX_REQ_CUR | Sets the sink-requested maximum operation current (when the MISMATCH bit = 1) in 20mA units. These bits are only valid when GIVEBACK_FLAG = 0 and a fixed PDO is selected. |

## MFR\_ID (0x37)

**Format:** Unsigned binary

The MFR\_ID command returns the manufacturer ID.

| Bits | Access | Bit Name        | Description                                             |
|------|--------|-----------------|---------------------------------------------------------|
| 7:0  | R      | MANUFACTURER_ID | Returns the manufacturer ID. The default is 0000 1001b. |

## DEV\_ID (0x38)

**Format:** Unsigned binary

The DEV\_ID command returns the device ID.

| Bits | Access | Bit Name  | Description                                       |
|------|--------|-----------|---------------------------------------------------|
| 7:0  | R      | DEVICE_ID | Returns the device ID. The default is 0101 1000b. |

## CLK\_ON (0x39)

**Format:** Unsigned binary

The CLK\_ON command enables the digital clock.

| Bits | Access | Bit Name | Description                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------|--------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0  | W      | CLOCK_ON | Enables the digital clock. Write 0x01 to enable the digital clock. No I <sup>2</sup> C registers can be modified before the digital clock is enabled. This bit automatically resets to 0 after the clock is enabled. The digital clock is enabled when a USB Type-C device is connected. Write 0 to 0x39, set the EN bit to 0, or pull down the EN pin and VIN pin below their UVLO thresholds to disable the digital clock again. |

## GPIO1 and GPIO2 Options

| GPIO1 Options | GATE | POWER_SHARE1 | FAULT                | NTC2    | ATTACH_FLT_ALT | IMON         |
|---------------|------|--------------|----------------------|---------|----------------|--------------|
| GPIO2 Options | POL  | NTC          | VCONN_IN (max 5.25V) | LED_PWM | ATTACH         | POWER_SHARE2 |

## APPLICATION INFORMATION

### COMPONENT SELECTION

#### Selecting the Inductor

In a buck-boost topology, the inductor must support buck applications with the maximum input voltage ( $V_{IN}$ ) and boost applications with the minimum  $V_{IN}$ . Two critical inductances can be determined according to the buck mode and boost mode current ripple. The first inductance ( $L_{MIN\_BUCK}$ ) can be calculated with Equation (3):

$$L_{MIN\_BUCK} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{REQ} \times \Delta I_L} \quad (3)$$

The second inductance ( $L_{MIN\_BOOST}$ ) can be estimated with Equation (4):

$$L_{MIN\_BOOST} = \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{V_{OUT} \times f_{REQ} \times \Delta I_L} \quad (4)$$

Where  $f_{REQ}$  is the switching frequency, and  $\Delta I_L$  is the peak-to-peak inductor current ripple.

Typically, the peak-to-peak ripple is between 1A and 3A. In addition to the inductance, the inductor must support the peak current in buck and boost applications to avoid saturation. The peak current in buck mode can be calculated with Equation (5):

$$I_{PEAK\_BUCK} = I_{OUT} + \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{2 \times V_{IN(MAX)} \times f_{REQ} \times L} \quad (5)$$

The peak current in boost mode can be estimated with Equation (6):

$$I_{PEAK\_BOOST} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN(MIN)}} + \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{2 \times V_{OUT} \times f_{REQ} \times L} \quad (6)$$

Where  $\eta$  is MPQ4242B's estimated efficiency.

#### Selecting the Input Capacitor

It is recommended to use ceramic capacitors plus an electrolytic capacitor for the input and output capacitors. This filters the input and output ripple current and helps achieve stable operation. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For automotive applications, a 100 $\mu$ F electrolytic capacitor and two 10 $\mu$ F + 0.1 $\mu$ F ceramic capacitors are recommended.

The input capacitor can be electrolytic, tantalum, or ceramic. When using an electrolytic capacitor, place two additional, high-quality ceramic capacitors as close to VIN as possible.

#### Selecting the Output Capacitor

The device requires an output capacitor ( $C_{OUT}$ ) to maintain the DC output voltage. Typically, a 100 $\mu$ F polymer or hybrid electric capacitor and two 10 $\mu$ F + 0.1 $\mu$ F ceramic output capacitors are recommended for excellent loop stability and transient response.

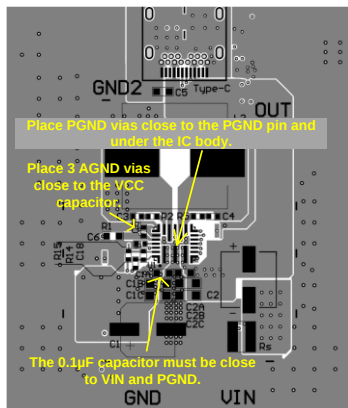
The E-capacitor's ESR must be below 50m $\Omega$  for excellent loop stability, transient response, and efficiency.

In GND-to-battery short applications, the output E-capacitor's negative node must be connected to the current-sense resistor (see Figure 24 on page 58).

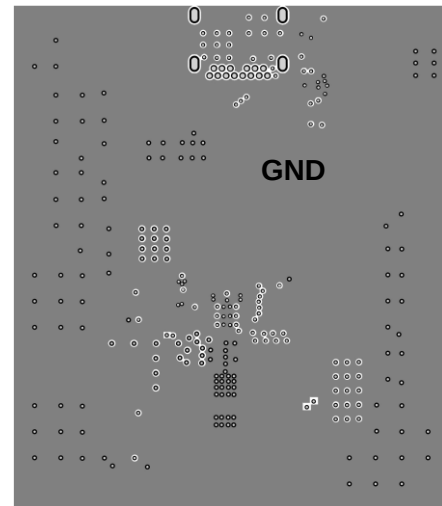
## PCB Layout Guidelines

Efficient PCB layout is critical for standard operation and thermal dissipation. For the best results, refer to Figure 23 and follow the guidelines below:

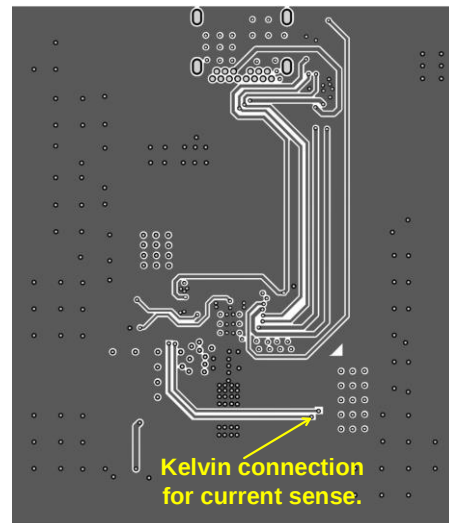
1. Use short, direct, and wide traces to connect OUT.
2. Add vias under the IC, then route the OUT trace on both PCB layers.
3. Place a large copper plane for PGND. Add multiple vias to improve thermal dissipation and connect AGND to PGND.
4. Place PGND vias close to PGND pin and under the IC's body.
5. Place the VCC decoupling capacitor as close as possible to the VCC pin.
6. Place 3 vias close to the VCC decoupling capacitor's AGND terminal.
7. Place a large copper plane for SW.
8. Place two ceramic input decoupling capacitors as close as possible to VIN, VOUT, and PGND to improve EMI performance.
9. Place an input filter at the bottom layer to improve EMI performance.
10. Use Kelvin connections for the output current sense traces (ISENS+ and ISENS-).
11. Place the input capacitor also close to the VIN pin as possible; in particular, the 0.1 $\mu$ F capacitor should be placed close to the VIN pin and PGND.
12. Make the HS\_G trace wide and short.



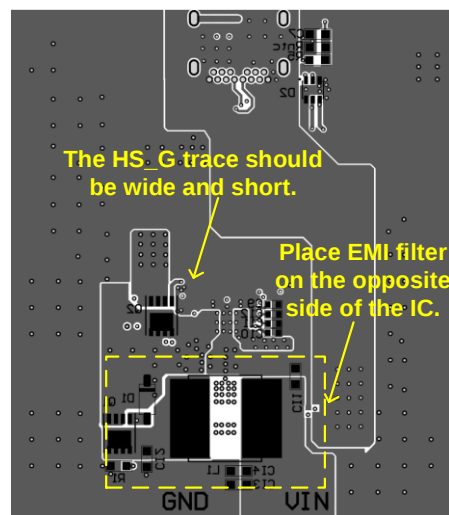
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 23: Recommended PCB Layout

# TYPICAL APPLICATION CIRCUITS

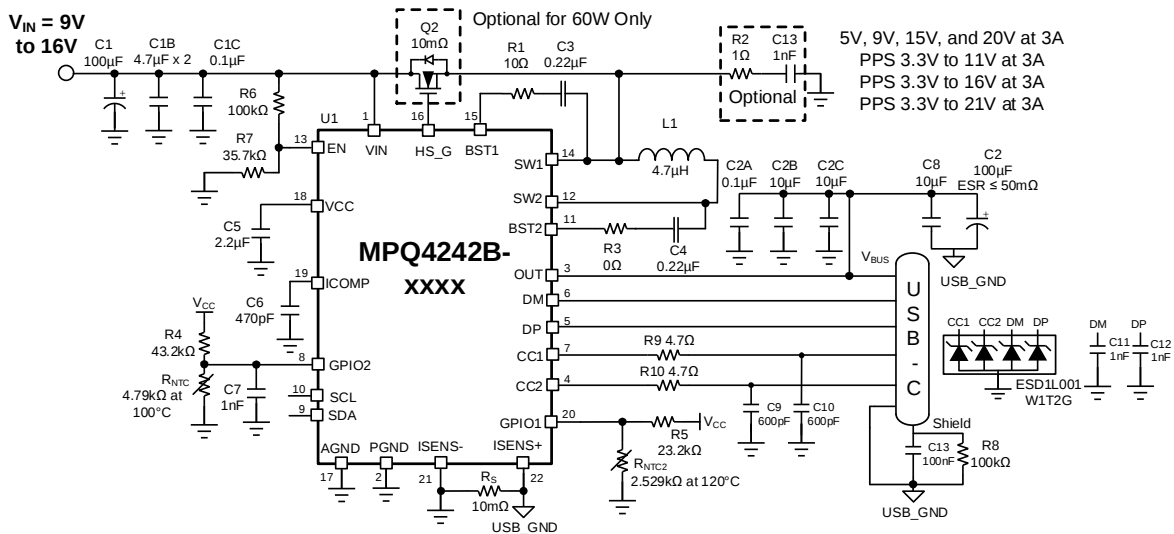


Figure 24: Typical Application Circuit (60W PD Application)

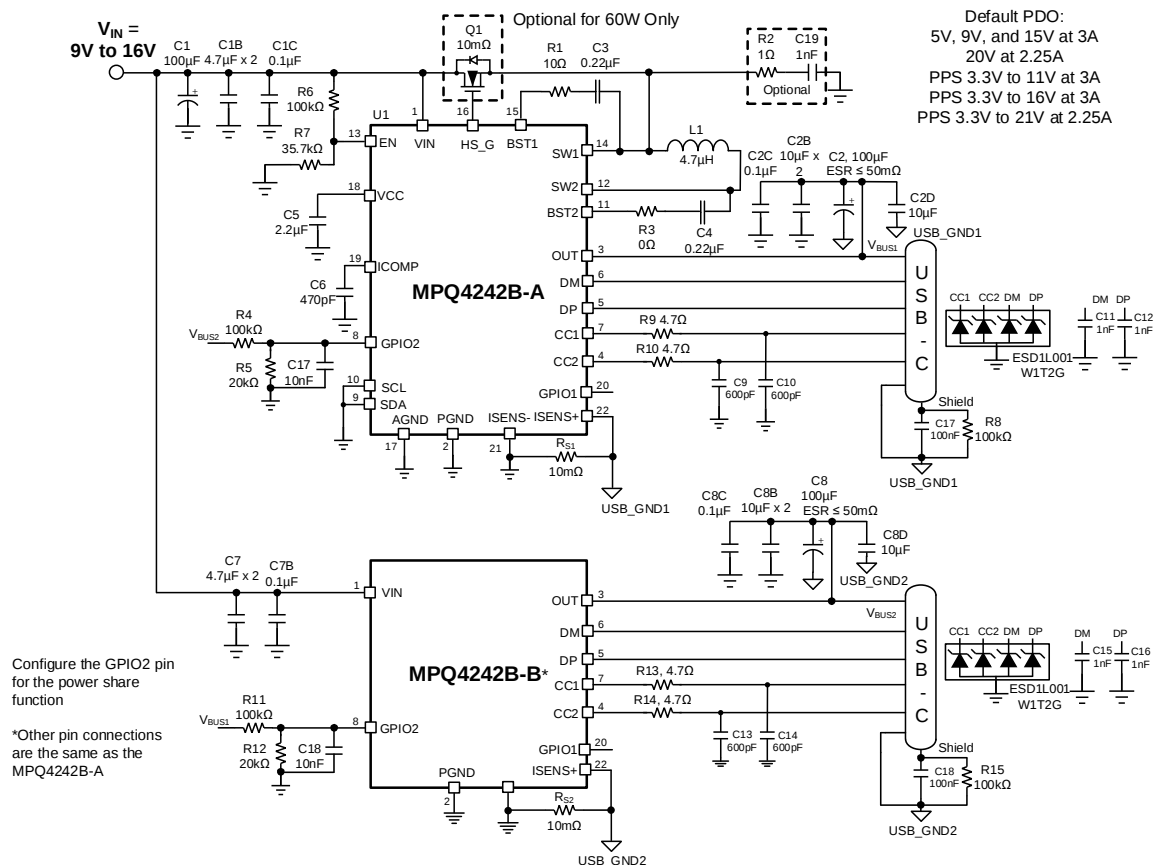


Figure 25: Typical Application Circuit (Dual-Channel 45W PD Application with GPIO2\_POWER\_SHARE) (18) (19) (20)

## Notes:

- 18) See Table 5 on page 29 for the GPIO2 power share PDP management.  $V_{BUS}$  exceeds 11.2V to trigger power share function (GPIO2 input voltage > 1.87V).
- 19) GPIO1 can be configured as a gate drive for the external low-side N-channel power MOSFET used for USB\_GND short to battery protection.
- 20) TVS diodes are required to pass the  $\pm 8kV$  contact  $\pm 15kV$  air discharge per IEC ESD specifications.

## MPQ4242BGVE-0000 CONFIGURATION TABLE

| OTP Items(PDO) | Enabled/Disabled      | PDO Type                | Voltage Setting | Current Setting |
|----------------|-----------------------|-------------------------|-----------------|-----------------|
| PDO1           | Enabled               | Fixed PDO               | 5V              | 3A              |
| PDO2           | 1b: Enabled (default) | 0b: Fixed PDO (default) | 9V (default)    | 3A              |
| PDO3           | 1b: Enabled (default) | 0b: Fixed PDO (default) | 15V (default)   | 3A              |
| PDO4           | 1b: Enabled (default) | 0b: Fixed PDO (default) | 20V (default)   | 3A              |
| PDO5           | 1b: Enabled (default) | 1b: APDO (default)      | 3.3V to 11V     | 3A              |
| PDO6           | 1b: Enabled (default) | 1b: APDO (default)      | 3.3V to 16V     | 3A              |
| PDO7           | 1b: Enabled (default) | 1b: APDO (default)      | 3.3V to 21V     | 3A              |

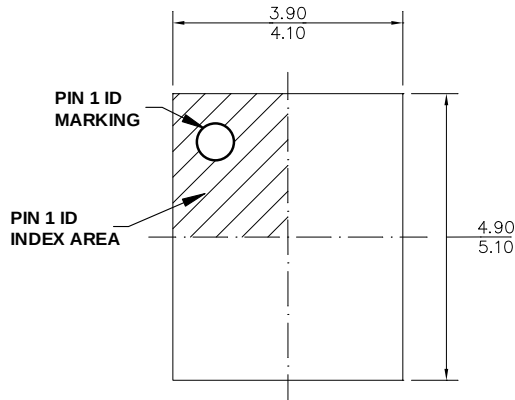
Table 7: OTP Descriptions

| OTP Items             | Description                                                                                                      | Value                                |
|-----------------------|------------------------------------------------------------------------------------------------------------------|--------------------------------------|
| GPIO1                 | Configures the GPIO1 pin's function.                                                                             | 000b: POWER_SHARE function (default) |
| GPIO2                 | Configures the GPIO2 pin's function.                                                                             | 000b: Reserved                       |
| OTP_THRESHOLD         | Sets the over-temperature shutdown threshold.                                                                    | 010b: 175°C (default)                |
| OTW1_THRESHOLD        | Sets-the over-temperature warning threshold.                                                                     | 100b: 135°C (default)                |
| OTW1_PDP              | Sets the maximum power rating when the die temp drops below its threshold.                                       | 45W (default)                        |
| OTW1_PDO_SELECT       | Selects which voltage is enabled in the PDO list.                                                                | 0xBE (default)                       |
| OTW2_THRESHOLD        | Sets the over-temperature warning threshold.                                                                     | 110b: 155°C (default)                |
| OTW2_NTC_PDP          | Set the maximum power rating when the die temperature drops below its threshold.                                 | 30W (default)                        |
| OTW2_NTC_PDO_SELECT   | Selects which voltage is enabled in the PDO list.                                                                | 0xBE (default)                       |
| NTC_HYSTERESIS        | Sets the NTC thermal recovery hysteresis.                                                                        | 1b: 20%( default)                    |
| NTC_MODE              | Sets the MPQ4242B behavior when the NTC is triggered.                                                            | 0b: Shut down the MPQ4242B (default) |
| VBATT_LOW_THLD1       | Sets the first threshold for V <sub>IN</sub> detection.                                                          | 0100b: 11.4V (default)               |
| VBATT_LOW_THLD2       | Sets the second threshold for V <sub>IN</sub> detection.                                                         | 1000b: 9V (default)                  |
| VBATT_LOW_THLD3       | Sets the third threshold for V <sub>IN</sub> detection. The device shuts down after this threshold is triggered. | 1010b: 6.2V (default)                |
| VBATT_LOW_BLK         | Sets the V <sub>BATT</sub> low 1 and V <sub>BATT</sub> low 2 blank times.                                        | 10b: 320ms (default)                 |
| VBATT_LOW1_PDP        | Sets the maximum power rating when V <sub>BATT</sub> falls below its first threshold.                            | 45W (default)                        |
| VBATT_L1_PDO_SELECT   | Select the voltage that is enabled in the PDO list.                                                              | 0xBE (default)                       |
| VBATT_LOW2_PDP        | Sets the maximum power rating when V <sub>BATT</sub> falls below its second threshold.                           | 15W (default)                        |
| VBATT_L2_PDO_SELECT   | Selects the voltage that is enabled in the PDO list.                                                             | 0xBE (default)                       |
| PS_PDP_THD            | Set the thresholds to which the PDO power rating is reduced.                                                     | 45W (default)                        |
| PS_PDP_THD_PDO_SELECT | Selects which voltage is enabled in the PDO list.                                                                | 0xBE (default)                       |
| VBUS_VOLTAGE          | Sets the default VBUS voltage.                                                                                   | 10b: 5.1V (default)                  |

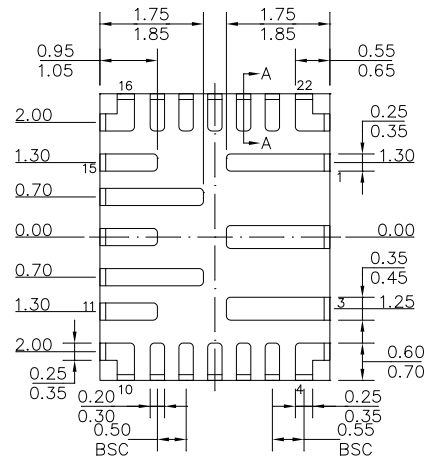
|                          |                                                                               |                                                                                                       |
|--------------------------|-------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------|
| MODE                     | Sets the PFM/PWM mode.                                                        | 1b: Forced PWM mode (default)                                                                         |
| FREQ                     | Sets the switching frequency                                                  | 01b: 420kHz (default)                                                                                 |
| DITHER                   | Sets the spread spectrum feature                                              | 0b: No frequency spread spectrum (default)                                                            |
| EN_OFF_TIMER             | Sets the EN off timer.                                                        | 000b: No delay (default)                                                                              |
| LINE_DROP_COMP           | Sets the output voltage compensation vs load feature.                         | 00b: No compensation (default)                                                                        |
| SLEW_RATE                | Sets the output slew rate to adjust $V_{OUT}$ .                               | 1b: 0.08mV/ $\mu$ s $V_{REF}$ rising slew rate, 0.08mV/ $\mu$ s $V_{REF}$ falling slew rate (default) |
| PEAK_CL                  | Sets the high-side peak current limit in boost mode.                          | 11b: 20A (default)                                                                                    |
| RSENS                    | Sets the external CC limit $R_{SENS}$ resistor value.                         | 1b: 10m $\Omega$                                                                                      |
| EXT_HS_FET RON           | Sets the $R_{DS(ON)}$ of the external N-channel MOSFET at 10V <sub>GS</sub> . | 000b: This function is disabled (default)                                                             |
| CC_BLANK_TIMER           | Sets the blank time when the output CC over-current condition is reached.     | 10b: 16ms (default)                                                                                   |
| LEGACY_CHARGING_MODE_SEL | Selects QC 3.0/DCP short mode / Divider mode.                                 | 00b: All DCP modes are active (default)                                                               |
| I2C_SLAVE_ADDRESS        | Sets the MPQ4242B's I <sup>2</sup> C slave address.                           | 61h (default)                                                                                         |
| VIN_OVP                  | Enables the VIN_OVP function. When $V_{IN} > 22V$ , the MPQ4242B shuts down.  | 0b: Disable VIN_OVP function                                                                          |

# PACKAGE INFORMATION

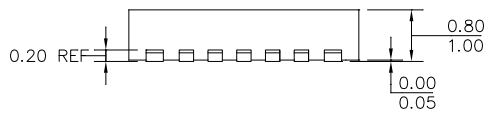
## QFN-22 (4mmx5mm)



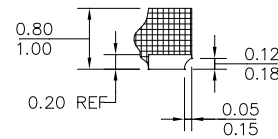
**TOP VIEW**



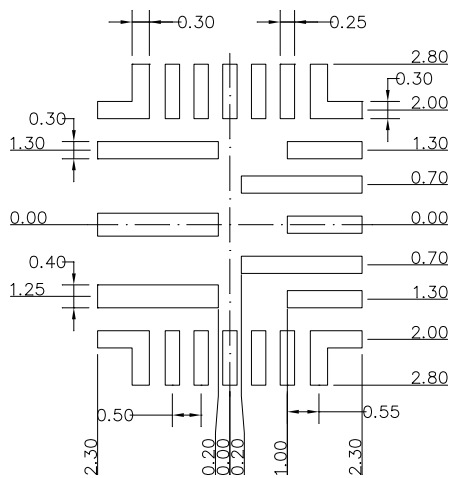
**BOTTOM VIEW**



**SIDE VIEW**



**SECTION A-A**

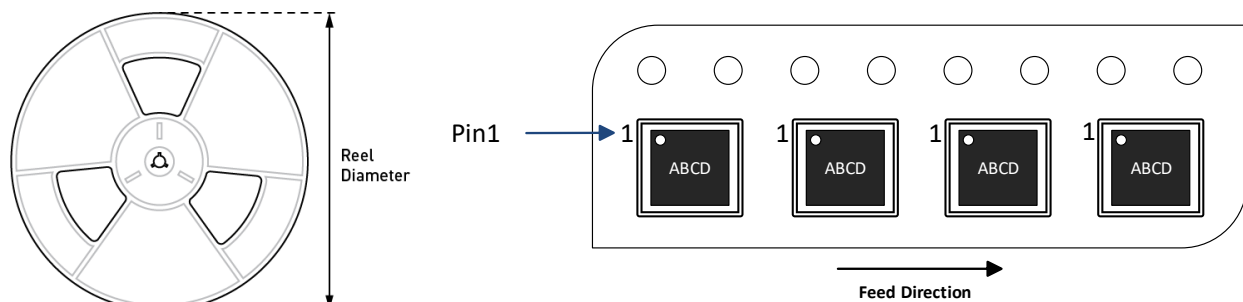


**RECOMMENDED LAND PATTERN**

### NOTE:

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

# CARRIER INFORMATION



| Part Number             | Package Description | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|-------------------------|---------------------|----------------|----------------|----------------|---------------|--------------------|--------------------|
| MPQ4242BGVE-0000-AEC1-Z | QFN-22 (4mmx5mm)    | 5000           | N/A            | N/A            | 13in          | 12mm               | 8mm                |
| MPQ4242BGVE-xxxx-AEC1-Z | QFN-22 (4mmx5mm)    |                |                |                |               |                    |                    |

## REVISION HISTORY

| Revision # | Revision Date | Description     | Pages Updated |
|------------|---------------|-----------------|---------------|
| 1.0        | 9/11/2024     | Initial Release | -             |

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