EVQ4242B-VE-00A

5A, 36V, Fully Integrated USB PD Solution with Integrated Buck-Boost Converter Evaluation Board, AEC-Q100 Qualified

DESCRIPTION

The EVQ4242B-VE-00A evaluation board is designed to demonstrate the capabilities of the MPQ4242B, a fully integrated power delivery (PD) solution for USB Type-C sourcing ports. It includes a buck-boost converter with four integrated power switches and a USB PD controller.

The MPQ4242B's USB Type-C port supports USB PD revision 3.1 with a programmable power supply (PPS). It is backward compatible with dedicated charging port (DCP) schemes for battery charging specification BC1.2, Apple 3A divider mode, and 1.2V/1.2V mode. The MPQ4242B also supports QC2.0/3.0 and Huawei FCP mode.

It is recommended to read the MPQ4242B datasheet prior to making any changes to the EVQ4242B-VE-00A.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V_{IN}) range		4.8V to 36V
Output voltage (V_{OUT})	V_{IN} = 13.5V	3.3V to 22.5V
Maximum output current (I_{OUT})	V_{IN} = 13.5V, V_{OUT} = 3.3V to 22.5V	5A
Typical efficiency	V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A	93.93%
Peak efficiency	V_{IN} = 16V, V_{OUT} = 20V, I_{OUT} = 2A	97.79%
Switching frequency (f_{SW})		420kHz

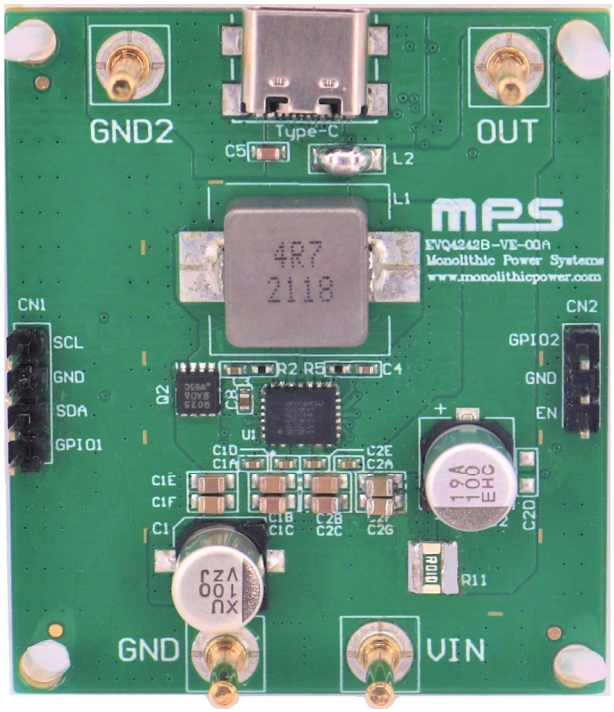
Input Voltage (V_{IN}) (1)	9V to 16V, Typical V_{IN} = 13.5V	
Default PDO List (2)	Output Voltage (V_{OUT})	Output Current (I_{OUT})
1	5V	3A
2	9V	3A
3	15V	3A
4	20V	3A
5	3.3V to 11V	3A
6	3.3V to 16V	3A
7	3.3V to 21V	3A

Notes:

1) The PD power is reduced when V_{IN} is low.
2) The power delivery object (PDO) list can be configured by setting the MPQ4242B's registers via the I^2C interface.

MPL Optimized Performance with MPS Inductor MPL-AL5030 Series

EVQ4242B-VE-00A EVALUATION BOARD



LxWxH (4.3cmx5cmx2.2cm)
4 Layers, 2oz/1oz/1oz/2oz

Board Number	MPS IC Number
EVQ4242B-VE-00A	MPQ4242BGVE-0000-AEC1

QUICK START GUIDE

The EVQ4242B-VE-00A evaluation board is easy to set up and use to evaluate the MPQ4242B's performance. For proper measurement equipment set-up, refer to Figure 1 on page 4 and follow the steps below:

1. Preset the power supply (V_{IN}) to 13.5V, then turn off the power supply.
2. Connect the power supply terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND
3. Connect the electronic load terminals to:
   a. Positive (+): VOUT
   b. Negative (-): GND2
4. Connect the power delivery (PD) protocol sniffer or mobile device to the USB Type-C port.
5. After making the connections, turn on the power supply. V_{BUS} should start up automatically at the default voltage set by the PD protocol sniffer or mobile device. The PD protocol sniffer can be used to select different PDO outputs.
6. For the battery voltage sensing function, if V_{IN} is below 11.4V, then the PD power is reduced to 45W. If V_{IN} is below 9V, the PD power is reduced to 15W. If V_{IN} is below 6.2V, the MPQ4242B shuts down. Table 1 shows the PDO list based on the battery voltage level.

Table 1: PDO List Based on Battery Voltage

Battery Voltage	PDO List
V_{IN} > 12.2V	5V/3A
	9V/3A
	15V/3A
	20V/3A
	3.3V to 11V, 3A
	3.3V to 16V, 3A
	3.3V to 21V, 3A
11.4V > V_{IN} > 9.8V	5V/3A
	9V/3A
	15V/3A
	20V/2.25A
	3.3V to 5.9V, 3A
	3.3V to 11V, 3A
	3.3V to 16V, 2.8A
V_{IN} < 9V	5V/3A
	9V/1.66A
	15V/1A
	20V/0.75A
	3.3V to 5.9V, 2.5A
	3.3V to 11V, 1.35A
	3.3V to 16V, 0.9A

7. For the over-temperature (OT) warning function, the MPQ4242B internally senses the die temperature. If the silicon die temperature exceeds 135°C, the PD power is reduced to 45W. If the temperature exceeds 155°C, the PD power is reduced to 30W.

If the MPQ4242B's silicon die temperature exceeds 175°C, over-temperature protection (OTP) is triggered and the entire chip shuts down. Once the temperature returns to below 155°C, the chip is enabled again and resumes normal operation.

8. To modify the MPQ4242B's register settings, connect the EVQ4242B-VE-00A to the USB-to-I²C communication kit (EVKT-USBI2C-02). Use Virtual Bench Pro 4.0 to read and write the I²C registers. (3) Before modifying the I²C register setting, enable CLOCK_ON to turn on the internal digital clock by writing 0x01 to register 39h.
9. Figure 1 shows the measurement equipment set-up.

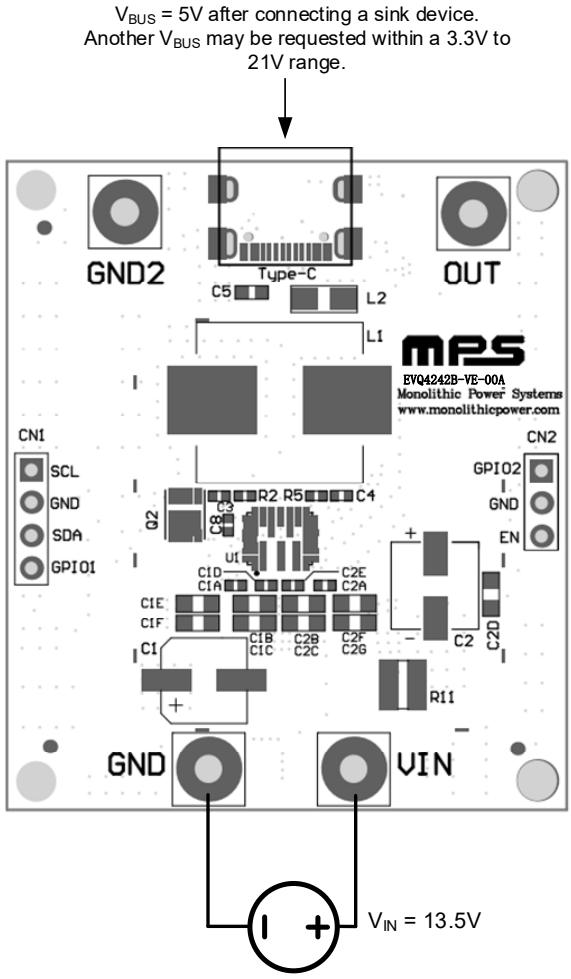


Figure 1: Measurement Equipment Set-Up

Note:

3) Contact and MPS FAE to request the Virtual Bench Pro 4.0 GUI.

GUI AND OTP MEMORY OPERATION

The MPQ4242B's default 60W PD version is the MPQ4242BGVE-0000-AEC1. It can be configured once via the one-time programmable (OTP) memory. To configure the device using the graphical user interface (GUI) and OTP memory, follow the steps below:

1. Connect the I²C communication interface (EVKT-USBI2C-02) to the EVQ4242B-VE-00A evaluation board.
2. Set V_{IN} to 13.5V, then turn on the power supply.
3. Open Virtual Bench Pro 4.0, click create new project to start a new connection (see Figure 2). (4)

Note:

4) Contact and MPS FAE to request the Virtual Bench Pro 4.0 GUI.

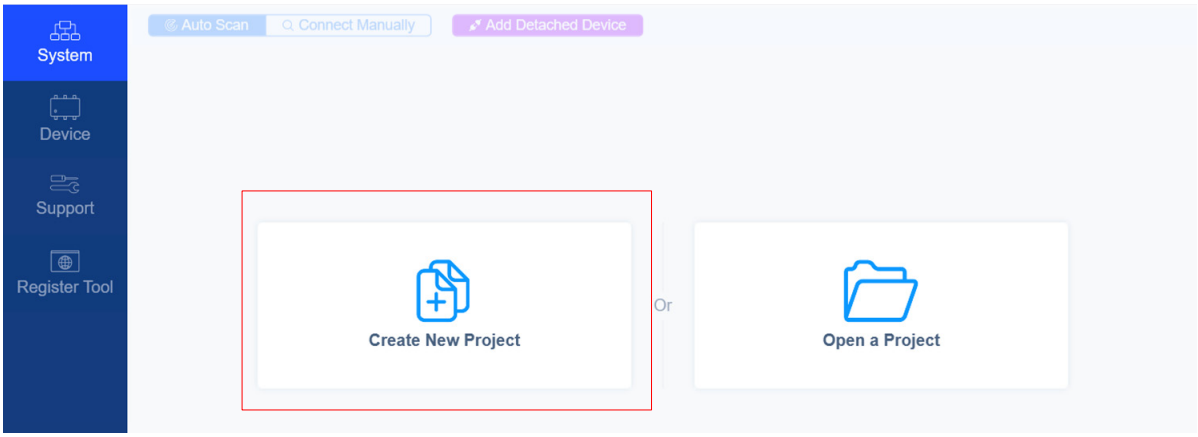


Figure 2: Creating a New Project in Virtual Bench Pro 4.0

4. Click “auto-scan” or connect manually to select the MPQ4242B and find the I²C device address (see Figure 3).

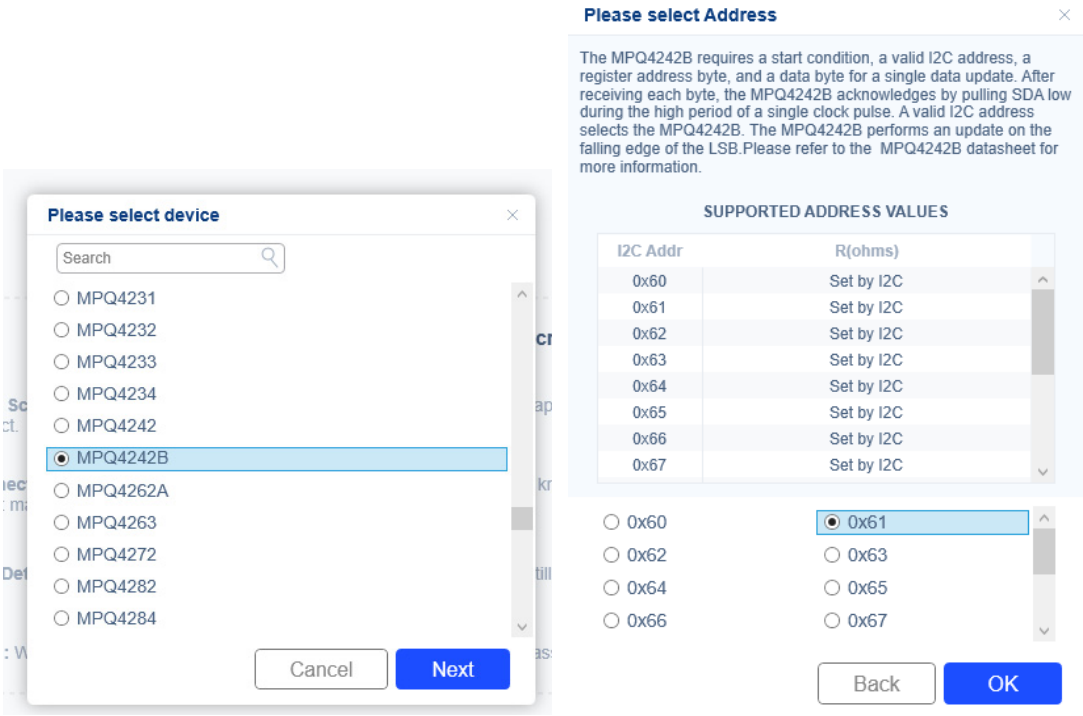


Figure 3: Find the I²C Device Address in Virtual Bench Pro 4.0

5. Click “ rRead RAM” on the toolbar to read the MPQ4242B-0000’s register values (see Figure 4).

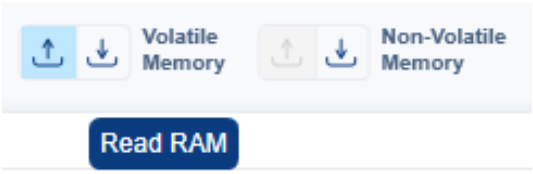


Figure 4: Read the MPQ4242B’s Register Values

6. Click “ Write RAM” on the toolbar to write the I²C command to the MPQ4242B (see Figure 5).

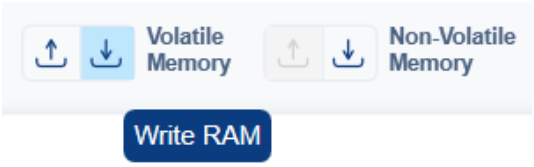


Figure 5: Write the MPQ4242B’s Register Values via the I²C

7. From this point, the user can change any register value. Read back the values once to ensure that all registers have been changed as expected, then click “ Write RAM” (see Figure 6).
8. Click “ Write ROM” and select “User OTP,” then click “OK” (see Figure 6).

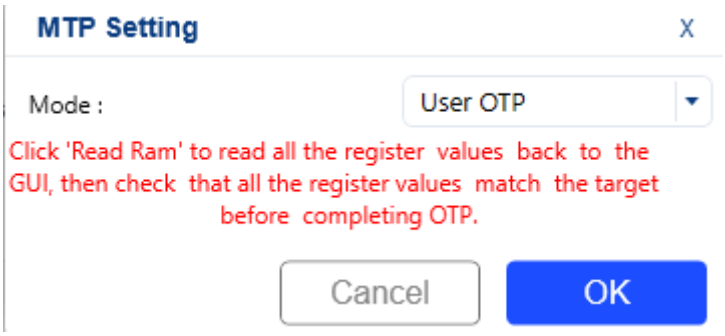


Figure 6: Select the OTP Type

9. Each MPQ4242BGVE-0000-AEC1 device can be configured once by the OTP memory. Click “ Read RAM” to read all the register values back to the GUI, then check that all the register values match the target before completing OTP.

EVALUATION BOARD SCHEMATIC

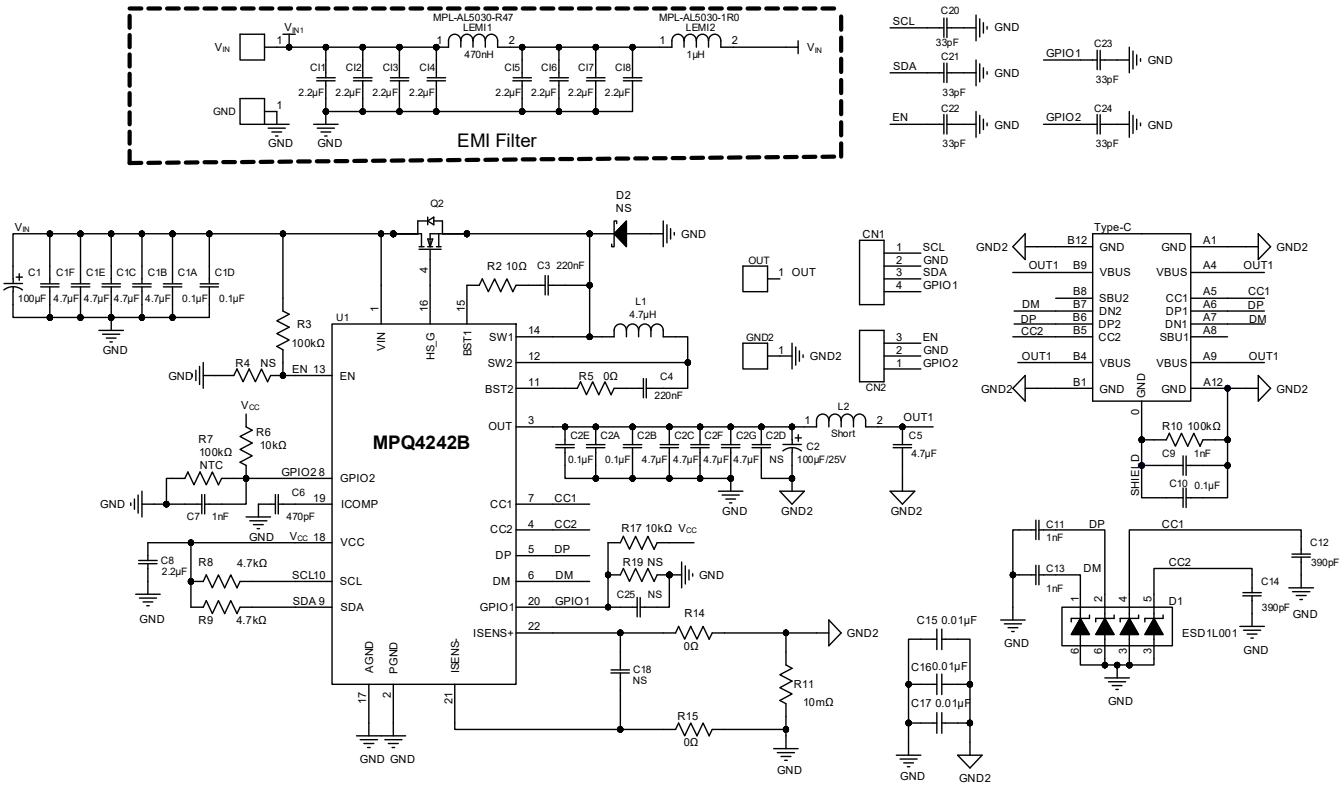


Figure 7: Evaluation Board Schematic (5) (6)

Notes:

5) Add an external N-channel MOSFET (Q2) to improve the thermal performance, especially for ≥45W PD applications. Q2 is disabled in the MPQ4242BGVE-0000-AEC1 configuration.

6) The EXT_HS_FET_RON set-up in the register should match Q2's on resistance ($R_{DS(ON)}$) at 10V V_{GS}.

EVQ4242B-VE-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	L1	4.7μH	Inductor, I_{SAT} = 16A, R_{DS} = 9.3mΩ	1005	Superworld	PIAQ1005S4R7MN
1	L2	Short				
8	CI1, CI2, CI3, CI4, CI5, CI6, CI7, CI8	2.2μF	Ceramic capacitor, 50V, X5R	0603	Murata	GRM188R61H225ME11D
1	C1	100μF	Aluminum electrolytic capacitor, 35V	SMD	Chemi-Con	EMZJ350ADA101MF80G
1	C2	100μF	Aluminum organic polymer capacitor, 25V, 30mΩ	SMD	Chemi-Con	HHXC250ARA101MF80G
4	C1A, C1D, C2A, C2E	0.1μF	Ceramic capacitor, 50V, X7R	0402	Murata	GRM155R71H104ME14D
8	C1B, C1C, C1E, C1F, C2B, C2C, C2F, C2G	4.7μF	Ceramic capacitor, 50V, X5R	0805	Murata	GRT21BR61H475ME13L
2	C3, C4	220nF	Ceramic capacitor, 25V, X5R	0402	Murata	GRM155R61E224KE01D
1	C5	4.7μF	Ceramic capacitor, 25V, X5R	0603	Murata	GRM188R61E475KE11D
1	C6	470pF	Ceramic capacitor, 50V, C0G	0402	Murata	GRM1555C1H471JA01D
2	C7, C9	1nF	Ceramic capacitor, 25V, X7R	0603	Wurth	885012206059
1	C8	2.2μF	Ceramic capacitor, 25V, X5R	0402	Murata	GRM155R61E225KE11D
1	C10	0.1μF	Ceramic capacitor, 50V, X7R	0603	Samsung	CL05B104KB5NNNC
2	C11, C13	1nF	Ceramic capacitor, 16V, X7R	0402	Murata	GRM155R71C102KA01D
2	C12, C14	390pF	Ceramic capacitor, 50V, C0G	0402	Murata	GRM1555C1H391JA01D
3	C15, C16, C17	10nF	Ceramic capacitor, 50V	0402	Murata	GCM155R71H103KA55D
5	C20, C21, C22, C23, C24	33pF	Ceramic capacitor, 50V, C0G	0603	Murata	GRM1885C1H330JA01D
0	C18, C25, D2, C2D, R4, R19	NS				
1	R2	10Ω	Film resistor, 1%	0402	Yageo	RC0402FR-0710RL
3	R5, R14, R15	0Ω	Film resistor, 1%	0402	Yageo	RC0402FR-070RL
1	R3	100kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07100KL
2	R6, R17	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
1	R7	100kΩ	NTC resistor	0603	TDK	NTCG164KF104FTDS
2	R8, R9	4.7kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-074K7L
1	R10	100kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07100KL
1	R11	10mΩ	Current-sensing resistor, 1%, long side, 1W	L1508	Susumu	RL3720WT-R010-F

EVQ4242B-VE-00A BILL OF MATERIALS *(continued)*

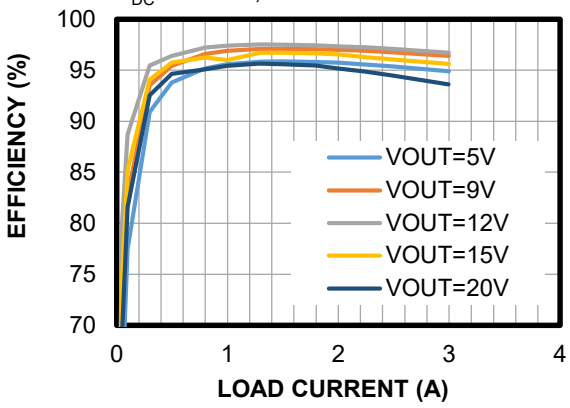
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	CN2	2.54mm	Connector, 1x3-pin, straight	DIP	Wurth	Any
1	CN1	2.54mm	Connector, 1x4-pin, straight	DIP	Wurth	Any
1	Q2	40V	N-channel MOSFET	SMD	Alpha & Omega Semiconductor	AONR66406
1	D1	16V	ESD diode	SOT-363-6	onsemi	ESD1L001W1T2G
1	TYPE-C	7.35mm	Type-C connector, 16P	Any	Any	PC-071603863-R
1	LEM1	470nH	Inductor, R_{DC} = 3.78mΩ, I_{SAT} = 26.5A	5030	MPS	MPL-AL5030-R47
1	LEM2	1μH	Inductor, R_{DC} = 6.5mΩ, I_{SAT} = 16A	5030	MPS	MPL-AL5030-1R0
1	U1	MPQ4242B	5A, 36V, fully integrated USB PD solution	QFN-22 (4mmx 5mm)	MPS	MPQ4242BGVE-0000-AEC1

EVB TEST RESULTS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

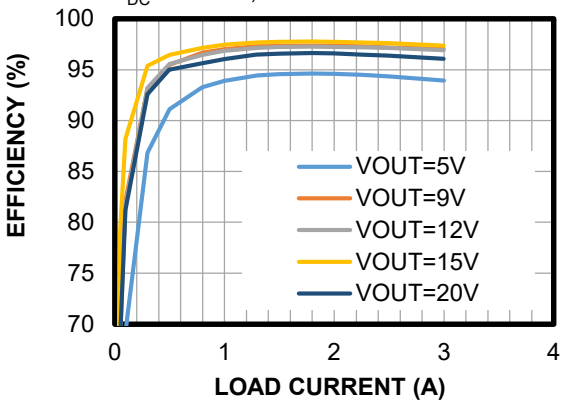
Efficiency vs. Load Current

V_{IN} = 9V, FCCM, L = 4.7µH,
R_{DC} = 9.3mΩ, external SWA disabled



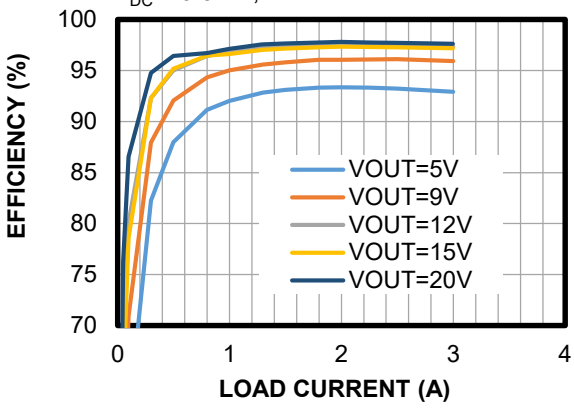
Efficiency vs. Load Current

V_{IN} = 12V, FCCM, L = 4.7µH,
R_{DC} = 9.3mΩ, external SWA disable



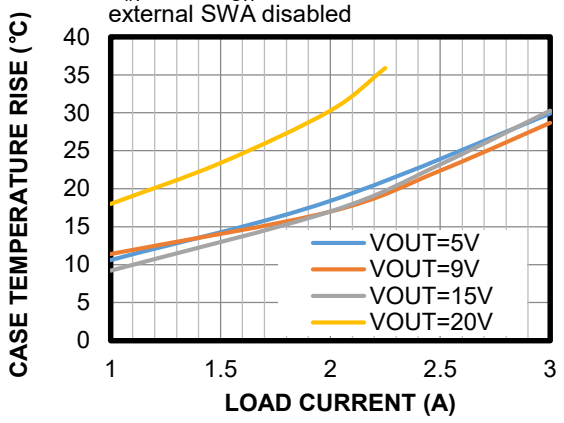
Efficiency vs. Load Current

V_{IN} = 16V, FCCM, L = 4.7µH,
R_{DC} = 9.3mΩ, external SWA disabled



Case Temperature Rise

V_{IN} = 12V, f_{SW} = 420kHz, 4.3cmx5cm PCB,
external SWA disabled

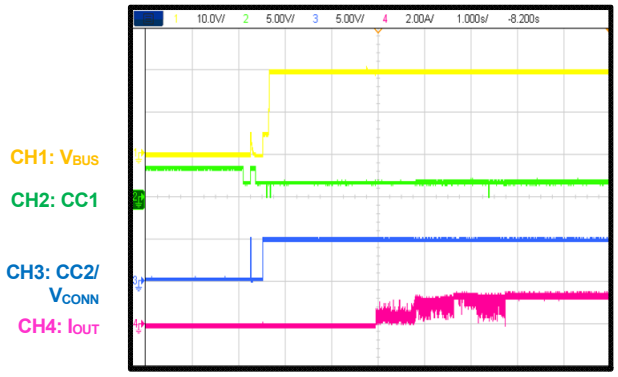


EVB TEST RESULTS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

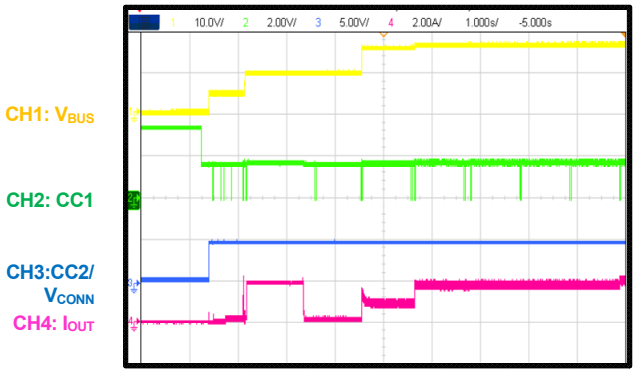
Laptop Charging Test

Laptop requests 20V PDO



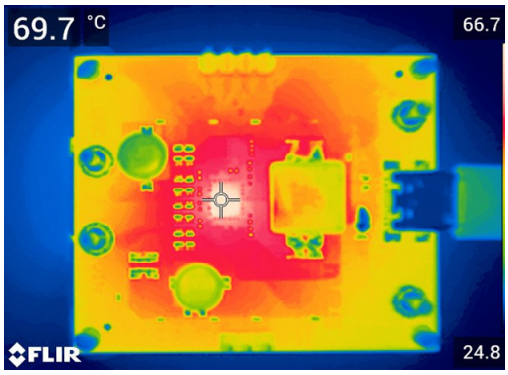
Mobile Phone Charging Test

Phone requests 3.3V to 21V APDO



Thermal Image

V_{IN} = 13.5V, V_{OUT} = 20V, I_{OUT} = 3A, f_{SW} = 420kHz, 4.3cmx5cm PCB, 2oz top and bottom layer, 1oz mid-layer 1 and mid-layer 2, external SWA enabled



PCB LAYOUT

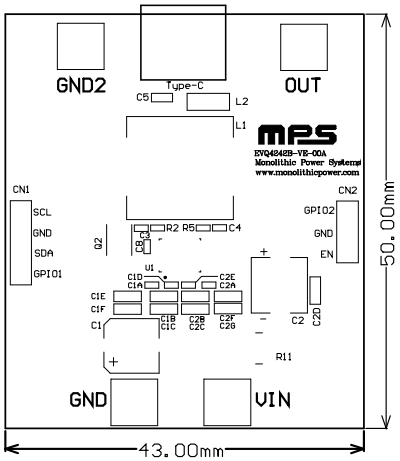


Figure 8: Top Silk

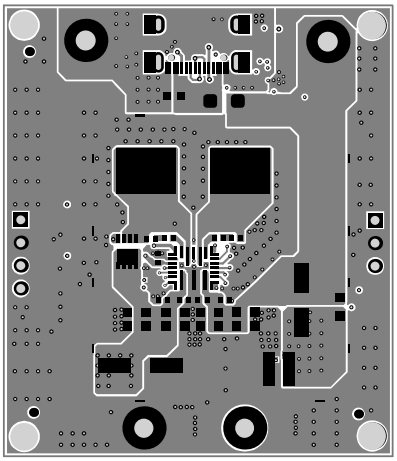


Figure 9: Top Layer

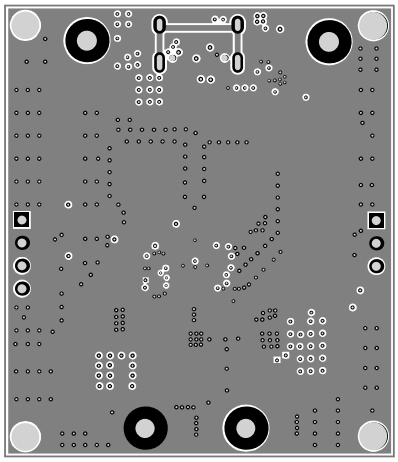


Figure 10: Mid-Layer 1

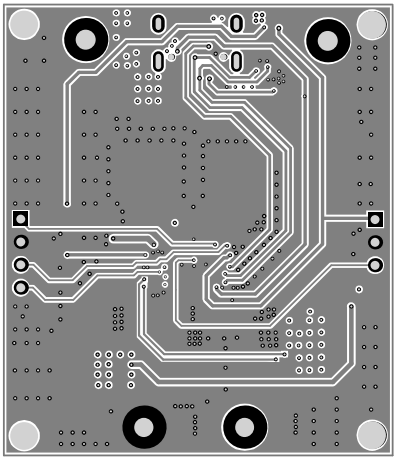


Figure 11: Mid-Layer 2

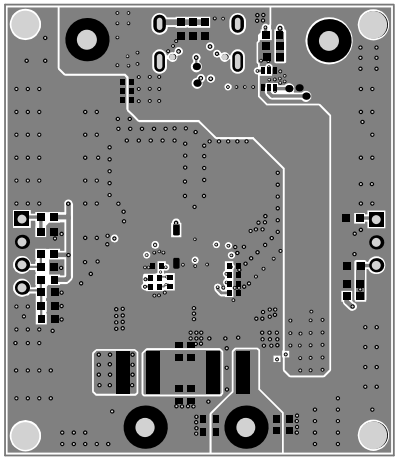


Figure 12: Bottom Layer

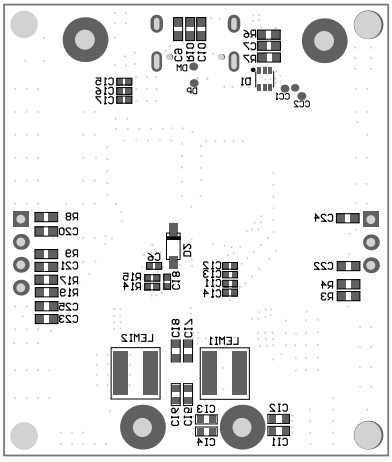


Figure 13: Bottom Silk

MPQ4242BGVE-0000 CONFIGURATION TABLE

Table 2 shows the PDO list set-up.

Table 2: PDO List Set-Up

OTP Items (PDO)	Enabled/Disabled	PDO Type	Voltage Setting	Current Setting
PDO1	Enabled	Fixed PDO	5V	3A
PDO2	1b: Enabled (default)	0b: Fixed PDO (default)	9V (default)	3A
PDO3	1b: Enabled (default)	0b: Fixed PDO (default)	15V (default)	3A
PDO4	1b: Enabled (default)	0b: Fixed PDO (default)	20V (default)	3A
PDO5	1b: Enabled (default)	1b: APDO (default)	3.3V to 11V	3A
PDO6	1b: Enabled (default)	1b: APDO (default)	3.3V to 16V	3A
PDO7	1b: Enabled (default)	1b: APDO (default)	3.3V to 21V	3A

Table 3 shows the OTP descriptions for the GPIOx and PDP set-up.

Table 3: OTP Descriptions

OTP Items	Description	Value
GPIO1	Configures the GPIO1 pin's function.	000b: POWER_SHARE function (default)
GPIO2	Configures the GPIO2 pin's function.	000b: Reserved
OTP_THRESHOLD	Sets the over-temperature (OT) shutdown threshold.	010b: 175°C (default)
OTW1_THRESHOLD	Sets the OT warning (OTW) 2 threshold.	100b: 135°C (default)
OTW1_PDP	Sets the maximum power rating when the die temp drops below its threshold.	45W (default)
OTW1_PDO_SELECT	Selects which voltage is enabled in the PDO list for OTW 1.	0xBE (default)
OTW2_THRESHOLD	Sets the OTW 1 threshold.	110b: 155°C (default)
OTW2_NTC_PDP	Sets the maximum power rating when the die temperature drops below its threshold.	30W (default)
OTW2_NTC_PDO_SELECT	Selects which voltage is enabled in the PDO list for OTW 2.	0xBE (default)
NTC_HYSTERESIS	Sets the NTC thermal recovery hysteresis.	1b: 20% (default)
NTC_MODE	Sets the MPQ4242B behavior when the NTC is triggered.	1b: Reduce PD power to the value set by OTW2_NTC_PDP
VBATT_LOW_THLD1	Sets the first threshold for V_{IN} detection.	0100b: 11.4V (default)
VBATT_LOW_THLD2	Sets the second threshold for V_{IN} detection.	1000b: 9V (default)
VBATT_LOW_THLD3	Sets the third threshold for V_{IN} detection. The device shuts down if this threshold is triggered.	1010b: 6.2V (default)
VBATT_LOW_BLK	Sets the V_{BATT} low 1 and V_{BATT} low 2 blank times.	10b: 320ms (default)
VBATT_LOW1_PDP	Sets the maximum power rating when V_{BATT} falls below its first threshold.	45W (default)
VBATT_L1_PDO_SELECT	Selects which voltage is enabled in the PDO list.	0xBE (default)
VBATT_LOW2_PDP	Sets the maximum power rating when V_{BATT} falls below its second threshold.	15W (default)
VBATT_L2_PDO_SELECT	Selects which voltage is enabled in the PDO list.	0xBE (default)
PS_PDP_THD	Set the thresholds to which the PDO power rating is reduced.	45W (default)
PS_PDP_THD_PDO_SELECT	Selects which voltage is enabled in the PDO list.	0xBE (default)

VBUS_VOLTAGE	Sets the default V_{BUS}.	10b: 5.1V (default)
MODE	Sets the PFM/PWM mode.	1b: Forced PWM mode (default)
FREQ	Sets the switching frequency.	01b: 420kHz (default)
DITHER	Enables spread spectrum.	0b: No frequency spread spectrum (default)
EN_OFF_TIMER	Sets the EN off timer.	000b: No delay (default)
LINE_DROP_COMP	Sets the output voltage compensation vs. load feature.	00b: No compensation (default)
SLEW_RATE	Sets the output slew rate to adjust V_{OUT}.	1b: 0.08mV/μs V_{REF} rising slew rate, 0.08mV/μs V_{REF} falling slew rate (default)
PEAK_CL	Sets the high-side peak current limit in boost mode.	11b: 20A (default)
RSENS	Sets the external CC limit R_{SENS} resistance.	1b: 10mΩ
EXT_HS_FET_RON	Sets the $R_{DS(ON)}$ of the external N-channel MOSFET at 10V_{GS}.	000b: This function is disabled (default)
CC_BLANK_TIMER	Sets the blanking time when the output CC over-current (OC) limit is reached.	01b: 2ms (default)
LEGACY_CHARGING_MODE_SEL	Selects QC 3.0/DCP short mode/divider mode.	00b: All DCP modes are active (default)
I2C_SLAVE_ADDRESS	Sets the MPQ4242B's I^2C slave address.	61h (default)
VIN_OVP	Enables the VIN_OVP function. If V_{IN} > 22V, the MPQ4242B shuts down.	0b: Disable VIN_OVP function

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/9/2024	Initial Release	-