MPQ6530

5V to 60V, Three-Phase, Brushless DC Motor Pre-Driver, AEC-Q100 Qualified

DESCRIPTION

The MPQ6530 is a gate driver IC designed for three-phase brushless DC (BLDC) motor driver applications. It features three half-bridges that consist of six N-channel power MOSFETs, with each of them capable to driving up to 60V.

The MPQ6530 integrates a regulated charge pump to generate gate drive power, and uses a bootstrap (BST) capacitor (C_{BST}) to generate supply voltage for the high-side MOSFET (HS-FET) driver. An internal trickle-charge circuit maintains a sufficient HS-FET driver voltage, even when the output is at 100% duty cycle.

Internal safety features include configurable short-circuit protection (SCP), over-current protection (OCP), adjustable dead-time (DT) control, under-voltage lockout (UVLO), and thermal shutdown.

The MPQ6530 is available in a QFN-28 (4mmx5mm) package with wettable flanks and an exposed thermal pad on the back, and is available in AEC-Q100 Grade 1.

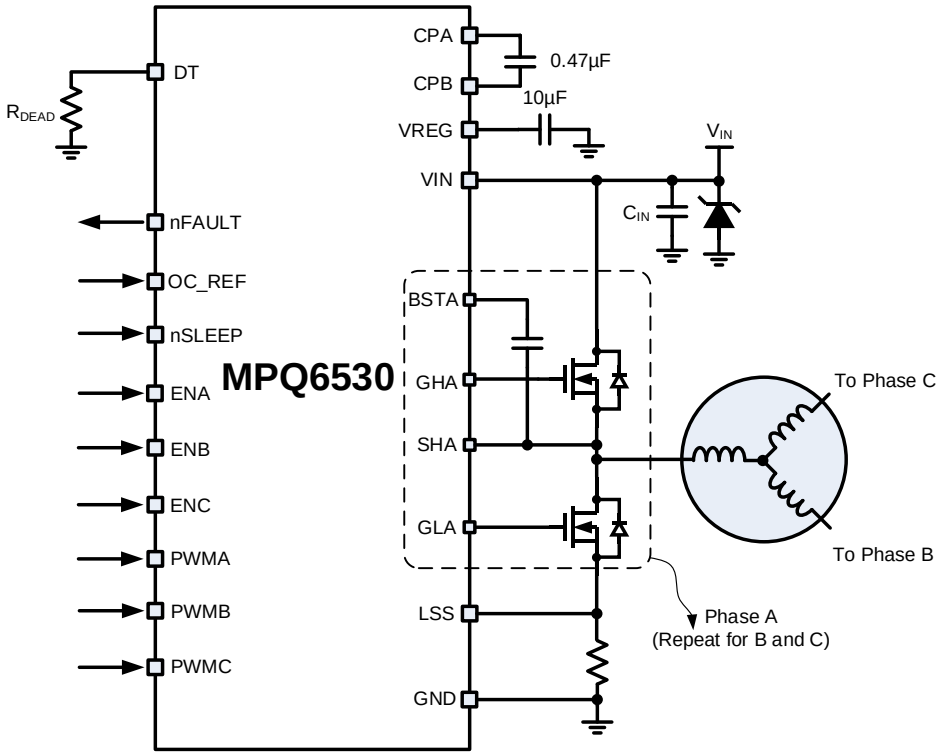
FEATURES

- Charge Pump Gate Drive Supply
- Bootstrap (BST) High-Side MOSFET (HS-FET) Driver with Trickle-Charge Circuit to Support 100% Duty Cycle Operation
- Low-Power Sleep Mode
- Configurable Short-Circuit Protection (SCP)
- Over-Current Protection (OCP)
- Adjustable Dead-Time (DT) Control to Prevent Shoot-Through
- Thermal Shutdown
- Under-Voltage Lockout (UVLO) Protection
- Fault Indication Output
- Thermally Enhanced Surface-Mount Package
- Available in a QFN-28 (4mmx5mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Three-Phase Brushless DC (BLDC) Motors and Permanent Magnet Synchronous Motors (PMSMs)
- Automotive Actuators, Pumps, and Fans

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MPQ6530GVE-AEC1*	QFN-28 (4mmx5mm)	*See Below*	2

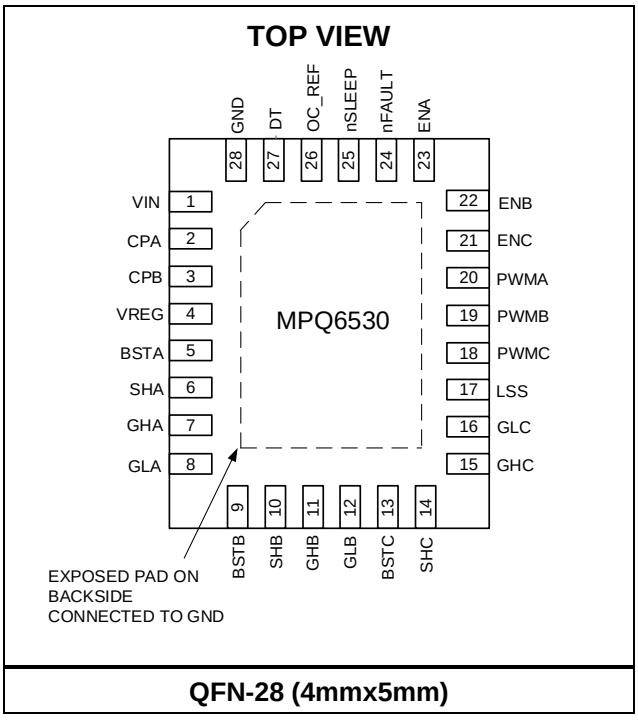
* For Tape & Reel, add suffix -Z (e.g. MPQ6530GVE-AEC1-Z).

TOP MARKING

MPSYWW
MP6530
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP6530: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-28 (4mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1	VIN	**Input supply voltage.** Bypass the VIN pin to ground with a ceramic capacitor. Additional bulk capacitance may be required. See the Application Information section on page 14 for more details.
2	CPA	**Charge pump capacitor.** Connect a ceramic capacitor between the CPA and CPB pins. See the Application Information section on page 14 for more details.
3	CPB	**Charge pump capacitor connection terminal.**
4	VREG	**Gate drive supply output.** Connect a ceramic capacitor between the VREG pin and ground. See the Application Information section on page 14 for more details.
5	BSTA	**Bootstrap for phase A.** Connect a ceramic capacitor from the BSTA pin to SHA. See the Application Information section on page 14 for more details.
6	SHA	**High-side (HS) source connection for phase A.**
7	GHA	**HS gate drive for phase A.**
8	GLA	**Low-side (LS) gate drive for phase A.**
9	BSTB	**Bootstrap for phase B.** Connect a ceramic capacitor from BSTB to SHB. See the Application Information section on page 14 for more details.
10	SHB	**HS source connection for phase B.**
11	GHB	**HS gate drive for phase B.**
12	GLB	**LS gate drive for phase B.**
13	BSTC	**Bootstrap for phase B.** Connect a ceramic capacitor from BSTC to SHC. See the Application Information section on page 14 for more details.
14	SHC	**HS source connection for phase C.**
15	GHC	**HS gate drive for phase C.**
16	GLC	**LS gate drive for phase C.**
17	LSS	**LS source connection for phases A, B, and C.**
18	PWMC	**PWM input pin for phase C.** Pull the PWNC pin high to drive phase C high; pull this pin low to drive phase C low. This pin has an internal pull-down resistor.
19	PWMB	**PWM input pin for phase B.** Pull the PWNB pin high to drive phase B high; pull this pin low to drive phase B low. This pin has an internal pull-down resistor.
20	PWMA	**PWM input pin for phase A.** Pull the PWNA pin high to drive phase A high; pull this pin low to drive phase A low. This pin has an internal pull-down resistor.
21	ENC	**Enable pin for phase C.** Pull the ENC pin high to enable the phase C gate driver; pull this pin low to disable the phase C gate driver. This pin has an internal pull-down resistor.
22	ENB	**Enable pin for phase B.** Pull the ENB pin high to enable the phase B gate driver; pull this pin low to disable the phase B gate driver. This pin has an internal pull-down resistor.
23	ENA	**Enable pin for phase A.** Pull the ENA pin high to enable the phase A gate driver; pull this pin low to disable the phase A gate driver. This pin has an internal pull-down resistor.
24	nFAULT	**Fault indication.** The nFAULT pin is an open-drain output, and is pulled low if a fault condition occurs.
25	nSLEEP	**Sleep mode input.** Pull the nSLEEP pin low to force the MPQ6530 to enter low-power sleep mode; pull this pin high to enable the device. This pin is pulled down internally to GND via a pull-down resistor.
26	OC_REF	**Over-current protection (OCP) reference voltage input.**
27	DT	**Dead time setting.** Connect a resistor between the DT pin and ground to set the dead time. See the Application Information section on page 14 for more details.
28	GND	**Ground.**

ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{IN}) .....-0.3V to +62V
CPA .....-0.3V to +55V
CPB .....-0.3V to +12.5V
CPB (transient, <2µs) .....-0.3V to +13V
VREG.....-0.3V to +13V
BSTA/B/C .....-0.3V to +70V
GHA/B/C (continuous) .....-0.3V to +70V
GHA/B/C (transient, <2µs).....-8V to +70V
SHA/B/C (continuous).....-0.3V to +62V
SHA/B/C (transient, <2µs) .....-8V to +62V
GLA/B/C (continuous).....-0.3V to +13V
GLA/B/C (transient, <2µs).....-2V to +13V
LSS (continuous) .....-0.3V to +1V
LSS (transient, <2µs).....-2V to +2V
All other pins to AGND.....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
QFN-28 (4mmx5mm)..... 3.1W
Storage temperature..... -55°C to +150°C
Junction temperature (T_J) .....150°C
Lead temperature (solder) .....260°C

ESD Ratings

Human body model (HBM) ..... ±1.2kV
Charged-device model (CDM) ..... ±750V

Recommended Operating Conditions (3)

Input voltage (V_{IN}) .....5V to 60V
OC_REF voltage (V_{OC_REF}).....0.125V to 2.4V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance (4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
QFN-28 (4mmx5mm)	40	9	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		5		60	V
Quiescent current	I_Q	nSLEEP = 1, gate driver is not switching		1.8	4	mA
	I_{SLEEP}	nSLEEP = 0, sleep mode			2.5	µA
Control Logic						
Input logic low threshold	V_{IL}				0.8	V
Input logic high threshold	V_{IH}		2.2			V
Logic input current	$I_{IN(H)}$	V_{IH} = 5V	-20		+20	µA
	$I_{IN(L)}$	V_{IL} = 0.8V	-20		+20	µA
nSLEEP pull-down current	I_{SLEEP_PD}			1		µA
Internal pull-down resistance	R_{PD}	All logic inputs except nSLEEP		880		kΩ
Fault Outputs (Open-Drain Outputs)						
Output low voltage	V_{OL}	I_{OUT} = 5mA			0.5	V
Output high leakage current	I_{OH}	V_{OUT} = 3.3V			1	µA
Protection Circuits						
Under-voltage lockout (UVLO) rising threshold	V_{IN_RISE}		3.2	3.9	5	V
UVLO hysteresis	V_{IN_HYS}			200		mV
VREG rising threshold	V_{REG_RISE}		6.8	7.6	8.4	V
VREG hysteresis	V_{REG_HYS}			0.65	1	V
VREG start-up delay	t_{REG_DELAY}			880		µs
OC__REF threshold	V_{OC_REF}	V_{OC_REF} = 1V	0.8	1	1.2	V
		V_{OC_REF} = 2.4V	2.18	2.4	2.62	V
Over-current protection (OCP) deglitch time	t_{OCP}			3		µs
Sleep mode wake-up time	t_{SLEEP}			1		ms
LSS OCP threshold	V_{LSS_OCP}		0.4	0.5	0.6	V
Thermal shutdown (5)	T_{TSD}			190		°C
Thermal shutdown hysteresis (5)	T_{TSD_HYS}			30		°C

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

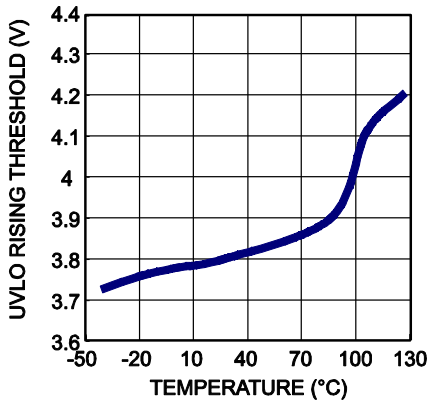
Parameter	Symbol	Condition	Min	Typ	Max	Units
Gate Driver						
Bootstrap (BST) diode forward voltage	V_{FBOOT}	I_D = 10mA			1	V
		I_D = 100mA			1.4	V
VREG output voltage (V_{OUT})	V_{REG}	V_{IN} = 5.5V to 60V	9.5	11.5	13	V
		V_{IN} = 5V to 5.5V	2 x V_{IN} - 1			V
Maximum source current (5)	I_{SOURCE}			0.8		A
Maximum sink current (5)	I_{SINK}			1		A
Gate driver pull-up resistance	R_{PU}	V_{DS} = 1V		8		Ω
Hide-side (HS) gate driver pull-down resistance	R_{HS_PD}	V_{DS} = 1V	1		6	Ω
Low-side (LS) gate driver pull-down resistance	R_{LS_PD}	V_{DS} = 1V	0.7		6.7	Ω
LS passive pull-down resistance	R_{LS_PPD}			590		kΩ
LS automatic start-up time	t_{LS}	At ENx rising edge		2		µs
Charge pump frequency	f_{CP}			110		kHz
LS automatic start-up time	t_{LS}	At ENx rising edge		2		µs
Dead time	t_{DEAD}	R_{DT} = 10kΩ		0.7		µs
	I_{SLEEP}	R_{DT} = 100kΩ		5.7		µs
		DT tied to GND		90		ns

Note:

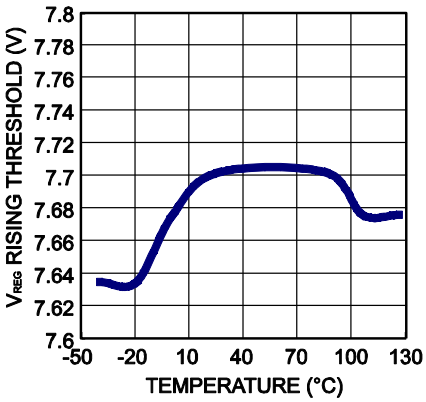
5) Not tested in production.

TYPICAL CHARACTERISTICS

UVLO Rising Threshold vs. Temperature

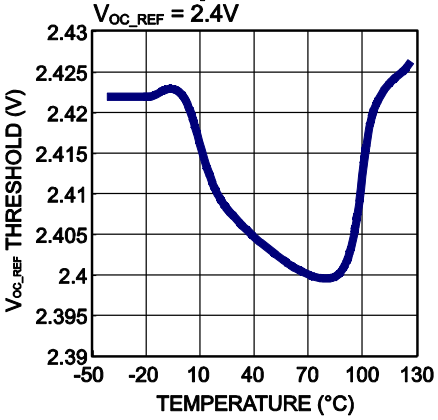


V_{REG} Rising Threshold vs. Temperature

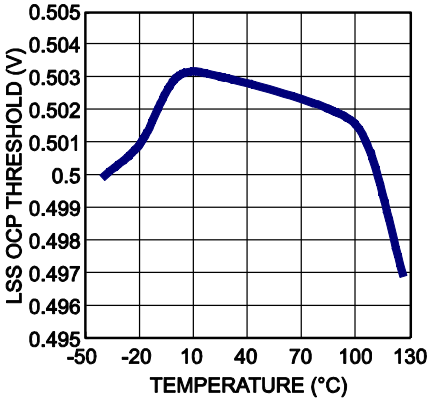


V_{OC_REF} Threshold vs. Temperature

V_{OC_REF} = 2.4V



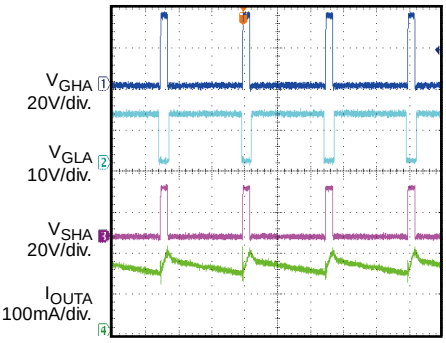
LSS OCP Threshold vs. Temperature



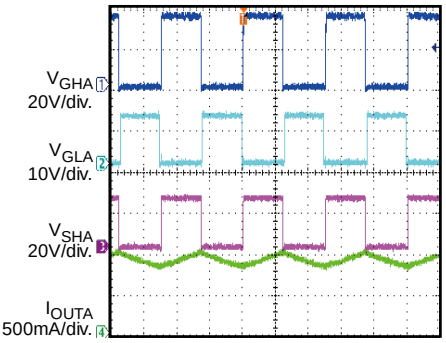
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, V_{OC_REF} = 0.5V, R_{DT} = 20kΩ, ENA = ENC = H, ENB = PWMC = L, f_{PWMA} = 20kHz, T_A = 25°C, resistor and inductor load = 5Ω + 1mH/phase with star connection, unless otherwise noted.

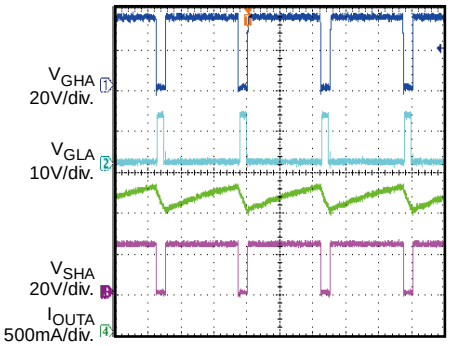
Steady State
Duty cycle = 10%



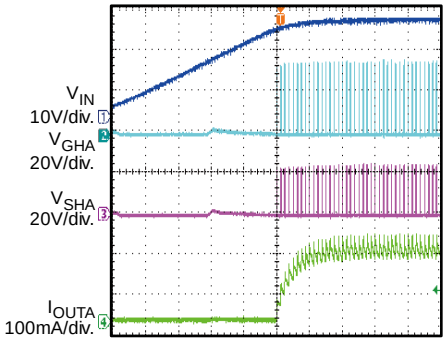
Steady State
Duty cycle = 50%



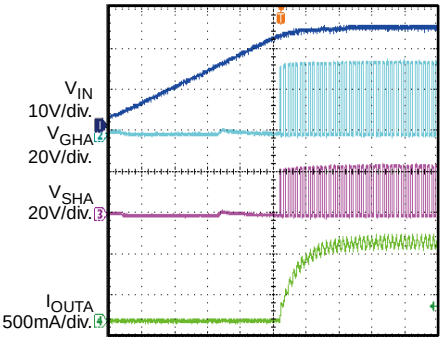
Steady State
Duty cycle = 90%



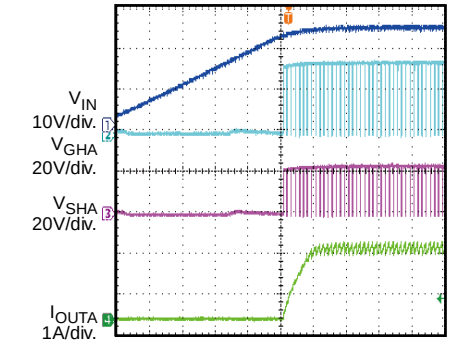
Power Ramping Up
Duty cycle = 10%



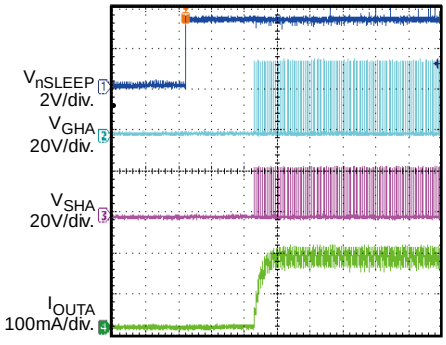
Power Ramping Up
Duty cycle = 50%



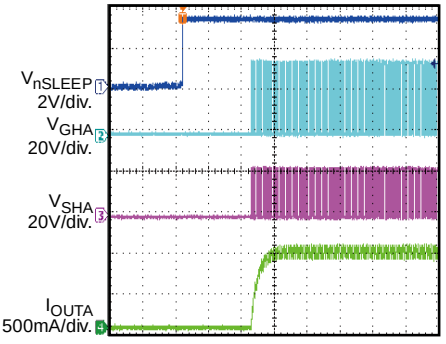
Power Ramping Up
Duty cycle = 90%



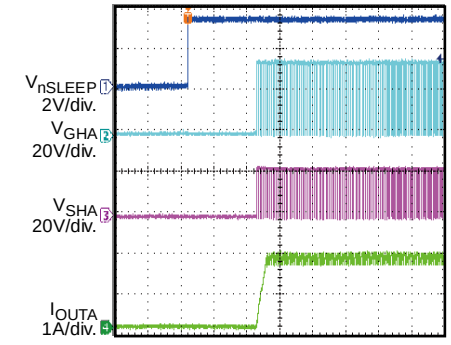
Sleep Mode Recovery
Duty cycle = 10%



Sleep Mode Recovery
Duty cycle = 50%



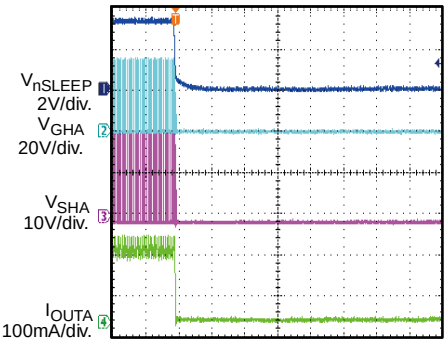
Sleep Mode Recovery
Duty cycle = 90%



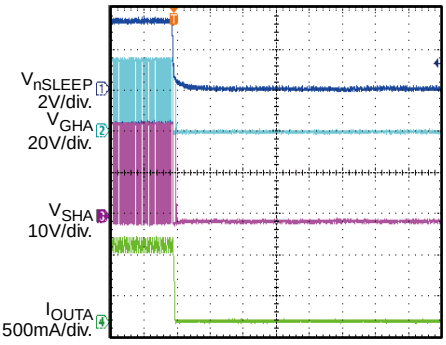
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OC_REF} = 0.5V, R_{DT} = 20kΩ, ENA = ENC = H, ENB = PWMC = L, f_{PWMA} = 20kHz, T_A = 25°C, resistor and inductor load = 5Ω + 1mH/phase with star connection, unless otherwise noted.

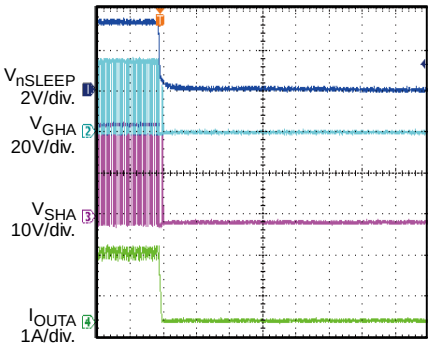
Sleep Mode Entry
Duty cycle = 10%



Sleep Mode Entry
Duty cycle = 50%



Sleep Mode Entry
Duty cycle = 90%



FUNCTIONAL BLOCK DIAGRAM

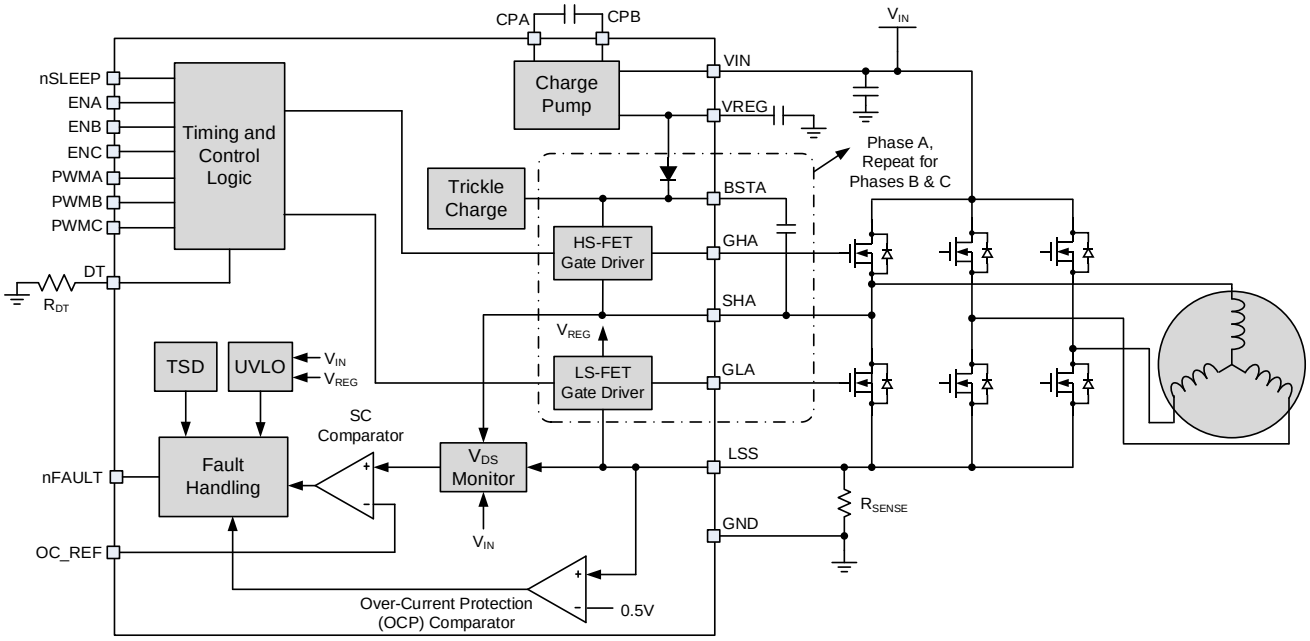


Figure 1: Functional Block Diagram

OPERATION

The MPQ6530 is a three-phase, BLDC motor pre-driver that drives three external N-channel MOSFET half-bridges, with a 0.8A source and 1A sink current capability. It operates across a wide 5V to 60V input voltage (V_{IN}) range, generating a boosted gate drive voltage when the input supply is below 12V. The MPQ6530 features low-power sleep mode, which disables the device and draws a very low supply current.

The MPQ6530 also features several flexible functions, such as adjustable dead-time (DT) control and over-current protection (OCP), to support a wide range of applications.

Start-Up Sequence

To initiate the start-up sequence, apply a voltage to V_{IN}. The voltage to V_{IN} must exceed the under-voltage lockout (UVLO) threshold (V_{IN_RISE}) to initiate start-up.

After start-up begins, the VREG supply starts operating and must exceed the VREG rising threshold (V_{REG_RISE}) before the device becomes functional.

The start-up process takes between 1ms and 2ms. Once start-up is complete, the MPQ6530 responds to logic inputs and drives the outputs.

Gate Drive Power Supplies

V_{IN} generates voltage for the gate drives. A regulated charge pump doubler circuit supplies a voltage (typically about 11.5V) to the VREG pin, and is used for the low-side (LS) gate drive supply. The charge pump requires external capacitors placed between CPA and CPB, and from VREG to ground.

The high-side (HS) gate drive is generated by a bootstrap (BST) capacitor (C_{BST}) and an internal trickle-charge pump. When the low-side MOSFET (LS-FET) is on, the BST capacitors charge the VREG voltage (V_{REG}). This charge is then used to drive the high-side MOSFET (HS-FET) gate when it turns on.

To keep the BST capacitors charged and allow operation at 100% duty cycle, an internal trickle-charge pump supplies a small current (typically about 5µA) to overcome leakages that would discharge the BST capacitors.

See the Application Information section on page 14 for details on selecting the external capacitor.

Sleep Mode (nSLEEP Input)

The MPQ6530 features a low-power sleep state. Pull the nSLEEP pin low to force the device to enter low-power sleep mode. In this state, all internal circuits are disabled and all inputs are ignored. nSLEEP is pulled down internally, so it must be pulled high for the MPQ6530 to operate. To exit sleep mode and operate the MPQ6530 normally, pull the nSLEEP pin high.

Input Logic

The ENx input pins control both the HS and LS gate drive outputs for each phase. When the ENx pin is pulled low, the gate drive outputs are pulled low and the PWMx input of that phase is ignored. When the ENx pin is pulled high, the gate drive outputs are enabled and the PWM input is recognized. Table 1 shows the input logic truth table.

Table 1: Input Logic Truth Table

ENx	PWMx	SHx
H	H	VIN
H	L	GND
L	x	High impedance (Hi-Z)

Low-Side (LS) Automatic Turn-On

To ensure that C_{BST} is sufficiently charged to turn on the HS-FET, each time that the ENx pin transitions from low to active high, the LS-FET for that phase turns on for a short pulse (t_{LS}). This occurs regardless of the PWMx input pin's state.

nFAULT

The nFAULT pin is an open-drain output. If a fault condition, such as over-current (OC) or over-temperature (OT), is detected, the nFAULT output pin is pulled low and reports the fault to the system. Once the fault condition is removed, an external pull-up resistor drives the nFAULT pin high again.

Short-Circuit Protection (SCP) with V_{DS} Sensing

To protect the power stage from damage due to high currents, the MPQ6530 implements drain-to-source voltage (V_{DS}) sensing circuitry to sense the voltage drop across each MOSFET.

This voltage is proportional to the MOSFET's on resistance ($R_{DS(ON)}$) and the drain-to-source current (I_{DS}) passing through the MOSFET. If the voltage drop exceeds the voltage supplied to the OC_REF terminal, a short circuit is recognized.

In the event of a short circuit, the MPQ6530 disables all gate drive outputs. The nFAULT is pulled active low, and the device remains latched off until it is reset by either the nSLEEP or V_{IN} under-voltage lockout (UVLO).

Short-circuit protection (SCP) can be disabled by connecting a 100kΩ resistor between the VREG and OC_REF pins.

Over-Current Protection (OCP)

The MPQ6530 implements output over-current protection (OCP) by monitoring the current through an LS shunt resistor connected to the LS-FETs. This resistor is connected to the LSS input pin and LS-FET source terminals. If the OCP function is not necessary, connect the LSS input pin and LS-FET source terminals directly to ground.

If the LSS voltage (V_{LSS}) (i.e. the voltage across the shunt resistor) exceeds the LSS OCP threshold (V_{LSS_OCP}, typically 0.5V), an OCP event is recognized. Once an OCP event is detected, the MPQ6530 latches off and disables all functions. The device remains latched off until it is reset by either the nSLEEP or V_{IN} UVLO.

The OCP current limit level is selected by the current-sense resistor's value that is connected at the LSS. See the Application Information section on page 15 for more information.

OCP can be disabled by connecting a 100kΩ resistor between the VREG and OC_REF pins.

Short-Circuit and OCP Deglitch Time

A current spike often occurs during switching transitions, caused by either the body diode's reverse-recovery current or the distributed capacitance of the load. This current spike requires filtering to prevent the spike from erroneously triggering OCP. When the outputs are switched, an internal fixed deglitch time (t_{OCP}) blanks the V_{DS} monitor's output.

Dead-Time (DT) Adjustment

To prevent shoot-through during any phase of the bridge, it is necessary to have a dead time (t_{DEAD}) between when the HS-FET or LS-FET turns off and the next complementary turns on. t_{DEAD} for all three phases is set via a single DT resistor (R_{DT}) between the DT pin and ground. t_{DEAD} can be estimated with Equation (1):

$$t_{DEAD}\,(ns) = 60 \times R_{DT}\,(k\Omega) \quad (1)$$

If DT is connected to ground, a 90ns t_{DEAD} is generated.

Under-Voltage Lockout (UVLO) Protection

If V_{IN} falls below the UVLO threshold (V_{IN_RISE}), all circuitry in the MPQ6530 is disabled and the internal logic resets. Once V_{IN} exceeds V_{IN_RISE}, the device begins the start-up sequence and resumes normal operation.

If V_{REG} drops below V_{REG_RISE}, the gate drive outputs are disabled and the nFAULT pin is pulled active low. Once V_{REG} exceeds V_{REG_RISE}, normal operation resumes.

Thermal Shutdown

If the die temperature exceeds safe limits (typically 190°C), the MPQ6530 disables its outputs and nFAULT is pulled low. Once the temperature has dropped to a safe level (typically 160°C), the device resumes normal operation.

PCB Mounting

To comply with IPC-2221 or IPC-9592 standards, conformal coating may be required after mounting the device on the PCB.

APPLICATION INFORMATION

Input Voltage (V_{IN})

V_{IN} supplies all power to the device, and must be properly bypassed with a capacitor connected to ground. The normal operating V_{IN} range is 5V to 60V.

V_{IN} must never exceed the absolute maximum ratings or it may damage the device, even under short-term transient conditions. In some cases, especially when mechanical energy can transform a motor into a generator, it may be necessary to use some form of over-voltage protection (OVP) between VIN and ground, such as a TVS diode.

Selecting the MOSFET

Correctly selecting the power MOSFETs for driving a motor is crucial for successful motor drive design.

The MOSFET must have a breakdown voltage (V_{DS}) greater than the supply voltage. A 10V to 15V margin is recommended to prevent damage to the MOSFET from transient voltages, which are caused by parasitic inductance in the PCB layout and wiring. As an example, MOSFETs in 24V power supply applications should have a minimum V_{DS} between 40V and 60V. An additional margin is ideal for high-current applications, as the transients caused by parasitic inductance may be larger. Conditions such as regenerative braking can also inject current back into the power supply. Care must be taken to ensure that such conditions do not increase the power supply voltage enough to damage components.

The MOSFETs should be able to safely pass the current necessary to run the motor. The motor's stall current is the highest current condition that must be supported, typically when the motor is first started or stalled.

The MOSFET's on resistance ($R_{DS(ON)}$) is similar to its current capability. The power (P) dissipated by the MOSFET is proportional to $R_{DS(ON)}$ and the motor current, and can be calculated using Equation (2):

$$P = I^2 \times R_{DS(ON)} \quad (2)$$

$R_{DS(ON)}$ must be selected to support safe heat dissipation for the desired motor current. In some cases, this may require special PCB design considerations, or implementing external heatsinks for the MOSFETs.

Considerations should be made for the MOSFETs' safe operating area (SOA) during fault conditions, such as a short circuit. The IC acts quickly in the event of a short. However, large currents can flow in the MOSFETs for a short time (typically about 3µs) before protection circuits recognize the fault and disable the outputs.

Selecting the External Capacitor

The MPQ6530 can provide a 9.5V to 13V gate drive voltage (V_{REG}), even if the input supply voltage drops as low as 5V. V_{REG} is generated by a charge pump inside the IC via external capacitors.

The charge pump flying capacitor (C_{CP}) should have a capacitance of 470nF, and must be rated to withstand the maximum V_{IN} supply voltage. An X7R or X5R ceramic capacitor is recommended. With a 470nF capacitor, V_{REG} can output approximately 10mA when V_{IN} is 5V. If operation below 10V is not necessary, a 220nF capacitor can be used.

Use BST capacitors to provide the large peak currents required to turn on the HS-FET. These capacitors are charged when the output is pulled low, then the charge in the BST capacitors turn on the HS-FET when the output is pulled high. An internal trickle charge circuit keeps the BST capacitors charged when the output is held high for an extended period.

Select the BST capacitors based on the MOSFET's total gate charge. When the HS-FET is on, the charge stored in the BST capacitor is transferred to the HS-FET gate. For simplification, the minimum BST capacitance (C_{BST}) can be estimated using Equation (3):

$$C_{BST} > 8 \times Q_G \quad (3)$$

Where Q_G is the total gate charge of the MOSFET (in nC), and C_{BST} is the minimum BST capacitance (in nF).

The BST capacitors should not exceed 1µF, or it may cause improper operation during start-up.

For most applications, each of the BST capacitors should be between 0.1µF and 1µF, X5R or X7R ceramic, and rated for at least 25V.

The VREG pin requires placing a bypass capacitor between this pin and ground, as close to the device as possible. This capacitor should be a 10µF, X7R or X5R ceramic capacitor rated for at least 16V.

The VIN pin requires placing a bypass capacitor between this pin and ground, as close to the device as possible. It is recommended to use a 0.1µF, X5R or X7R ceramic capacitor that is rated for V_{IN}.

Depending on the power supply impedance and the distance between the MOSFETs and power supply, additional bulk capacitance may be required. Low-ESR electrolytic capacitors between 47µF and 470µF are recommended.

Selecting the Dead-Time Resistor

During the transitions between driving an output low and high, t_{DEAD} is the short period during which neither the HS-FET nor LS-FET turns on. t_{DEAD} is necessary to prevent shoot-through, a condition where any overlaps in conduction between HS-FETs and LS-FETs can cause a short circuit between the power supply and ground. Shoot-through causes large transient currents and can damage the MOSFETs.

Since motors are naturally inductive, the current cannot stop immediately once current is flowing in the motor, even if the MOSFETs are turned off. This recirculation current continues to flow in the original direction until the magnetic field decays.

When the MOSFETs turn off, the recirculation current flows through the body diode in the MOSFET.

The MOSFET body diodes have a significantly greater voltage drop than the MOSFET during conduction, so more power is dissipated during body diode conduction than during the MOSFET's on time. Therefore, it is ideal to minimize t_{DEAD}. However, t_{DEAD} must still be long enough to guarantee that the HS-FETs and LS-FETs are never turned on at the same time.

t_{DEAD} can be set to a large range of times by selecting the value of the external resistor connected to DT (R_{DT}). Typically, a good t_{DEAD} is about 1µs, which requires a 16kΩ resistance. If faster switching or a high PWM frequency (f_{PWM}) (above 30kHz) is used, a shorter t_{DEAD} may be ideal. If switching is slowed using external gate resistors, a longer t_{DEAD} may be necessary.

Figure 2 shows a waveform with a t_{DEAD} of about 300ns between when the LS-FET gate turns off and the HS-FET gate turns on.

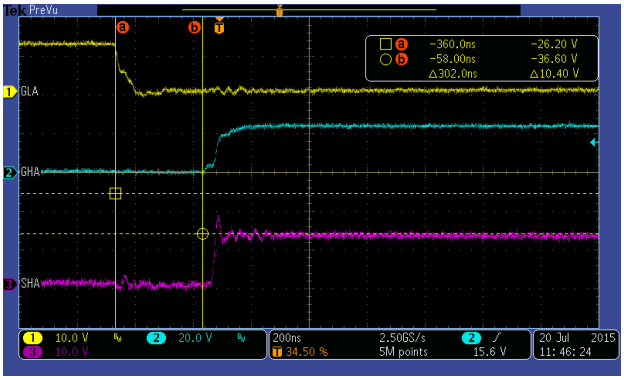


Figure 2: Dead Time

Selecting the LSS Resistor

If V_{LSS} exceeds 500mV, an OC event is recognized. The external current-sense resistor provides a drop below 500mV at the maximum expected motor current. For example, if a 50mΩ resistor is used, then a 10A current causes a 500mV drop and activates OCP.

If this function is not necessary, connect the LSS directly to ground.

Selecting the OC_REF Voltage

An internal comparator compares the voltage drop across each MOSFET via the voltage from the OC_REF input pin (V_{OC_REF}). This voltage is typically provided via an external resistor divider from the logic power supply. If the drop across any MOSFET exceeds V_{OC_REF}, a short-circuit event is recognized.

If this function is not necessary, connect OC_REF to VREG through a 100kΩ resistor.

Gate Drive Considerations

The selected MOSFETs' gate characteristics affect how fast the MOSFETs switch on and off. The MPQ6530's gate drive outputs can be directly connected to the power MOSFETs gates, which results in the fastest possible turn-on and turn-off times. However, it may be advantageous to add external components,

such as resistors and/or diodes, to modify the MOSFET turn-on and turn-off characteristics.

Adding external series resistance (typically 10Ω to 100Ω) limits the current that charges and discharges the MOSFET gate, slowing down turn-on and turn-off times. This is sometimes useful to control EMI and noise. However, slowing the transition too much during switching results in a large power dissipation in the MOSFET.

In some cases, it is desirable to have a slow turn-on, but a fast turn-off time. This can be implemented by using a series resistor in parallel with a diode (see Figure 3). During turn-on, the resistor limits the current flow into the gate. During turn-off, the gate is discharged quickly through the diode.

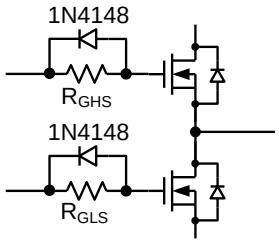


Figure 3: Gate Circuit for Fast Turn-Off

Figure 4 shows a waveform representing the LS-FET and HS-FET gates, and the phase node (output) with no series resistance. The gates transition quickly, and the resulting rise time on the phase node is quite fast. The scale of Figure 4 is 100ns/div.

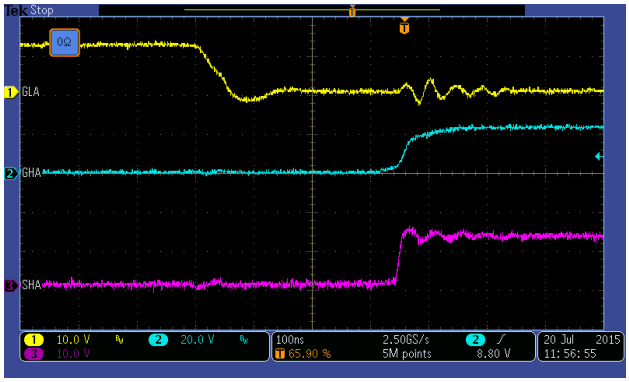


Figure 4: Switching with No Series Resistance

Figure 5 shows the waveform that results from adding a 100Ω series resistor between the GLA pin and the LS-FET gate, and between the GHA pin and the HS-FET gate, respectively. The rise time on the phase node has been slowed significantly. The scale of Figure 5 is 200ns/div.

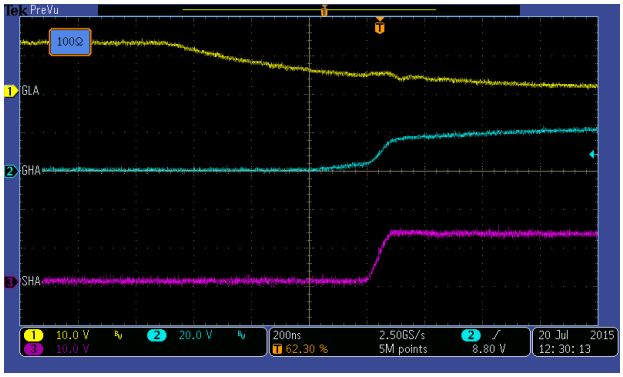


Figure 5: Switching with 100Ω Series Resistance

Figure 6 shows the waveform that results from adding a 1N4148 diode in parallel with the 100Ω resistors and the cathode connected to the IC. The LS gate's fall time is fast compared to the HS gate's rise time. The phase node moves even slower because of a longer time period between when the LS-FET turns off and the HS-FET turns on.

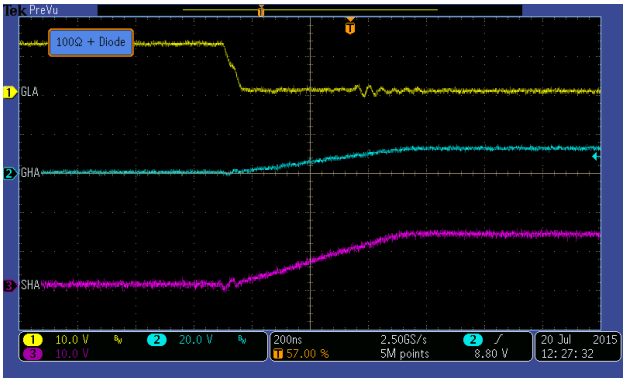


Figure 6: Switching with 100Ω Resistance and Diode

PCB Layout Guidelines

Efficient PCB layout is critical for optimal performance. The pre-driver is designed to accommodate negative undershoot. However, excessive undershoot can lead to unpredictable operation or damage to the IC. For best results, refer to Figure 7 and follow the guidelines below:

1. Make the connection between the HS-FET source and the LS-FET drain as direct as possible to avoid a negative undershoot on the phase node due to parasitic inductance.
2. Use surface-mount N-channel MOSFETs that allow a very short connection between the HS-FETs and LS-FETs.
3. Use wide copper areas for all high-current paths.
4. Connect the LS-FET sense resistor, which is composed of five resistors in parallel (R7, R8, R9, R10, and R11), between the input supply ground and LS-FET source terminals with wide copper areas.
5. Place the charge pump and supply bypass capacitors as close to the IC as possible. Connect the grounded side of these capacitors to a ground plane that is also connected to the GND pin and exposed pad.
6. Keep the high-current ground path between the input supply, input bulk capacitor (C7), and MOSFETs away from the IC's ground plane.

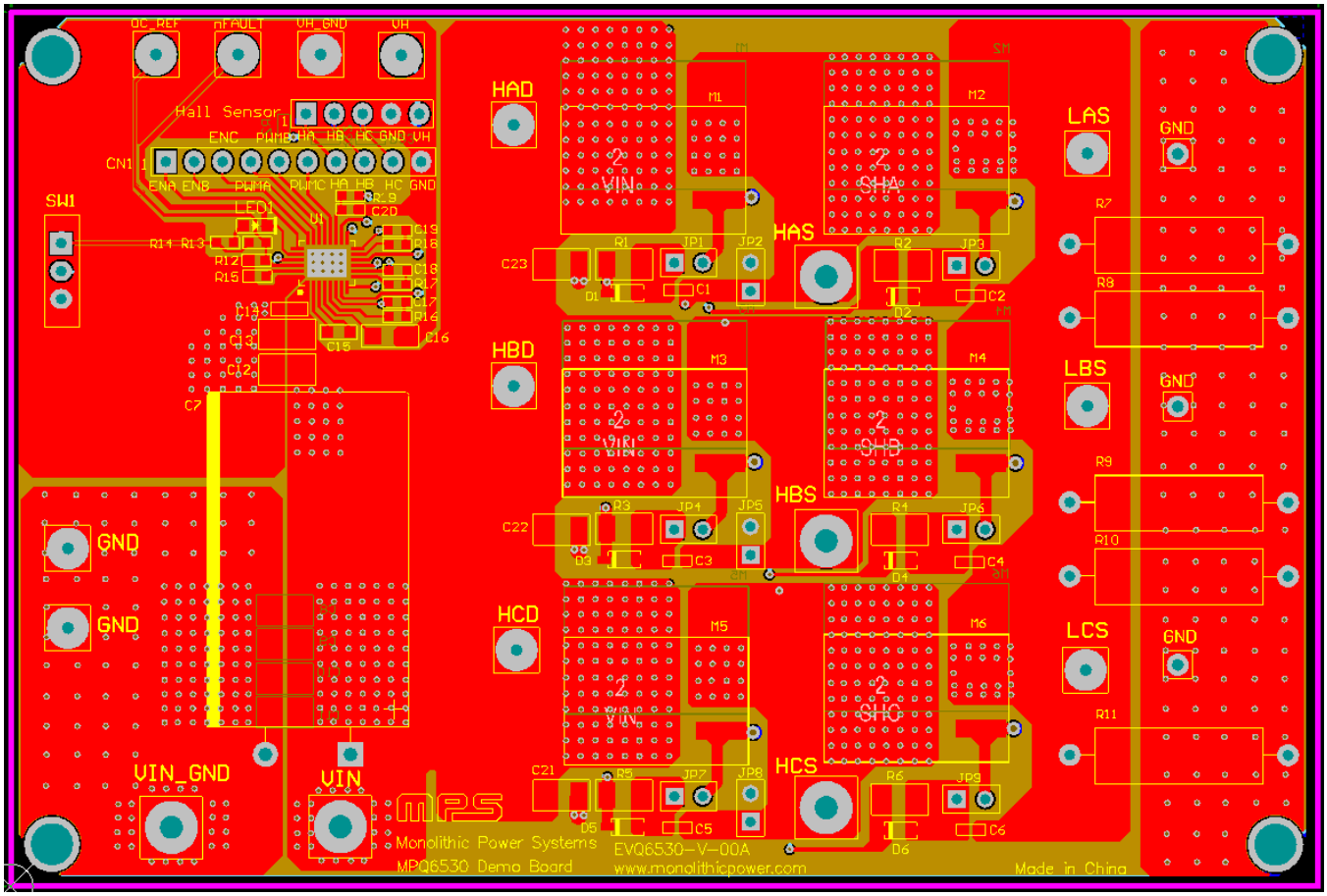


Figure 7: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

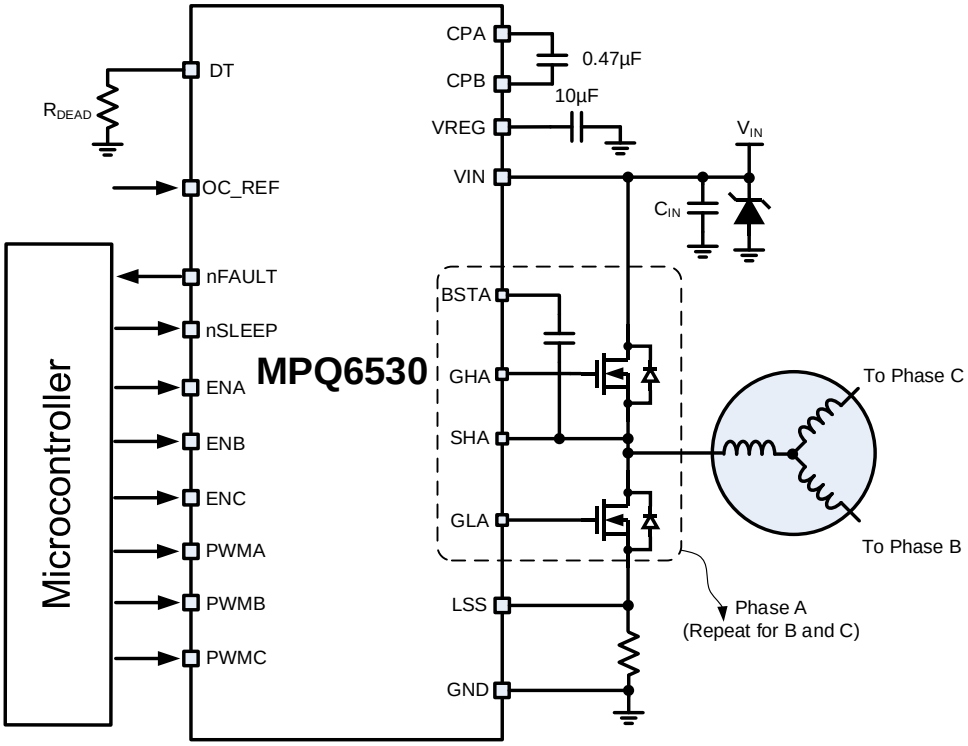
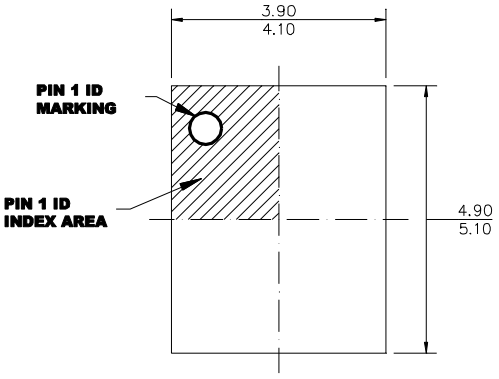


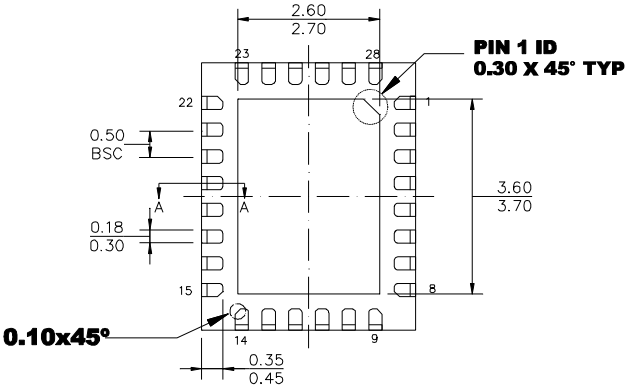
Figure 8: Typical Application Circuits

PACKAGE INFORMATION

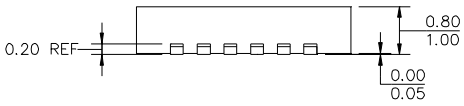
QFN-28 (4mmx5mm)
Wettable Flank



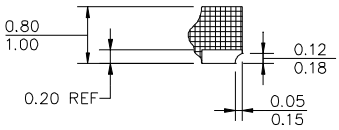
TOP VIEW



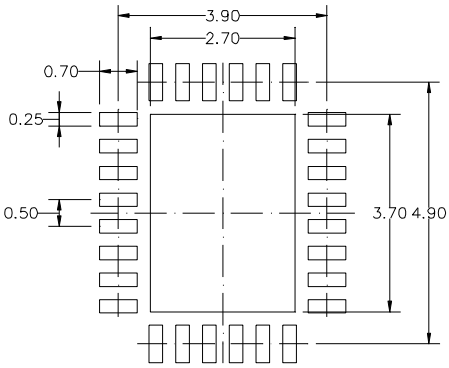
BOTTOM VIEW



SIDE VIEW



SECTION A-A

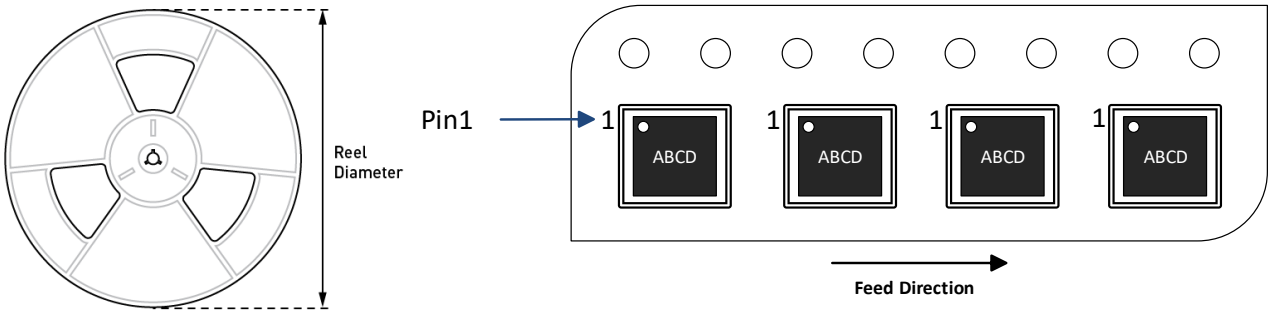


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION VGHD-3.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tray	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ6530GVE-AEC1-Z	QFN-28 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/24/2024	Initial Release	-