Product Change Notification: SYST-19EYKR028

Date:

01-Jul-2025

Product Category:

32-Bit Microcontrollers

Notification Subject:

PIC32CM LE00/LS00/LS60 Family Silicon Errata and Data Sheet Clarifications

Affected CPNs:

SYST-19EYKR028_Affected_CPN_07012025.pdf
SYST-19EYKR028_Affected_CPN_07012025.csv

Notification Text:

SYST-19EYKR028

Microchip has released a new Document for the PIC32CM LE00/LS00/LS60 Family Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at **PIC32CM LE00/LS00/LS60 Family Silicon Errata and Data Sheet Clarifications**.

Notification Status: Final

Description of Change:

Revision L - 06/2025

The following updates were performed for this revision:

• Updated the tables in PIC32CM LE00/LS00/LS60 Family Errata to reflect new silicon

• Updated the Silicon Errata Summary to reflect new silicon

• Updated all Silicon Revision tables in each Errata category to reflect new silicon

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity.

Change Implementation Status: Complete

Date Document Changes Effective: 01 Jul 2025

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC32CM LE00/LS00/LS60 Family Silicon Errata and Data Sheet Clarifications

Please contact your local **Microchip sales office** with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC32CM5164LE00100-I/PF

PIC32CM5164LE00100T-I/PF

PIC32CM5164LE00064-I/5LX

PIC32CM5164LE00064-I/PT

PIC32CM5164LE00064T-I/5LX

PIC32CM5164LE00064T-I/PT

PIC32CM5164LE00048-I/U5B

PIC32CM5164LE00048-I/Y8X

PIC32CM5164LE00048T-I/U5B

PIC32CM5164LE00048T-I/Y8X

PIC32CM2532LE00100-I/PF

PIC32CM2532LE00100T-I/PF

PIC32CM2532LE00100-E/PF

PIC32CM2532LE00100T-E/PF

PIC32CM2532LE00064-I/5LX

PIC32CM2532LE00064-I/PT

PIC32CM2532LE00064T-I/5LX

PIC32CM2532LE00064T-I/PT

PIC32CM2532LE00064-E/5LX

PIC32CM2532LE00064-E/PT

PIC32CM2532LE00064T-E/5LX

PIC32CM2532LE00064T-E/PT

PIC32CM2532LE00048-I/U5B

PIC32CM2532LE00048-I/Y8X

PIC32CM2532LE00048T-I/U5B

PIC32CM2532LE00048T-I/Y8X

PIC32CM2532LE00048-E/U5B

PIC32CM2532LE00048-E/Y8X

PIC32CM2532LE00048T-E/U5B

PIC32CM2532LE00048T-E/Y8X

PIC32CM5164LS00100-I/PF

PIC32CM5164LS00100T-I/PF

PIC32CM5164LS00064-I/5LX

PIC32CM5164LS00064-I/PT

PIC32CM5164LS00064T-I/5LX

PIC32CM5164LS00064T-I/PT

PIC32CM5164LS00048-I/U5B-SL3

PIC32CM5164LS00048-I/U5B

PIC32CM5164LS00048-I/Y8X

PIC32CM5164LS00048T-I/U5B

PIC32CM5164LS00048T-I/Y8X

PIC32CM2532LS00100-I/PF

PIC32CM2532LS00100T-I/PF

PIC32CM2532LS00100-E/PF

PIC32CM2532LS00100T-E/PF

PIC32CM2532LS00064-I/5LX

PIC32CM2532LS00064-I/PT

PIC32CM2532LS00064T-I/5LX

PIC32CM2532LS00064T-I/PT

PIC32CM2532LS00064-E/5LX

PIC32CM2532LS00064-E/PT

PIC32CM2532LS00064T-E/5LX

PIC32CM2532LS00064T-E/PT

PIC32CM2532LS00048-I/U5B

PIC32CM2532LS00048-I/Y8X

PIC32CM2532LS00048T-I/U5B

PIC32CM2532LS00048T-I/Y8X

PIC32CM2532LS00048-E/U5B

PIC32CM2532LS00048-E/Y8X

PIC32CM2532LS00048T-E/U5B

PIC32CM2532LS00048T-E/Y8X

PIC32CM5164LS60100-I/PF

PIC32CM5164LS60100-I/PF-PROTO

PIC32CM5164LS60100T-I/PF-PROTO

PIC32CM5164LS60064-I/5LX-PROTO

PIC32CM5164LS60064-I/PT-PROTO

PIC32CM5164LS60064T-I/5LX-PROTO

PIC32CM5164LS60064T-I/PT-PROTO

PIC32CM5164LS60048-I/U5B-PROTO

PIC32CM5164LS60048T-I/U5B-PROTO

PIC32CM LE00/LS00/LS60 Family Silicon Errata and Data Sheet Clarifications

PIC32CM LE00/LS00/LS60

PIC32CM LE00/LS00/LS60 Family Errata

The PIC32CM LE00/LS00/LS60 family of devices that you have received conform functionally to the current Device Data Sheet (DS60001615), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following tables. The silicon issues are summarized in the Silicon Issues Summary.

The errata described in this document will be addressed in future revisions of the PIC32CM LE00/LS00/LS60 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in Data Sheet Clarifications, following the discussion of silicon issues.

Table 1. PIC32CM LE00 Family Silicon Device Identification

Devices	Device ID (DID[31:0])	Silicon Revision ID (DID.REVISION[3:0])		
		A0	B0	C0
PIC32CM5164LE00100	0x20850X00	0x0	0x1	—
PIC32CM5164LE00064	0x20850X01	0x0	0x1	—
PIC32CM5164LE00048	0x20850X02	0x0	0x1	—
PIC32CM2532LE00100	0x20850X04	0x0	0x1	0x2
PIC32CM2532LE00064	0x20850X05	0x0	0x1	0x2
PIC32CM2532LE00048	0x20850X06	0x0	0x1	0x2
PIC32CM1216LE00048	0x2085200A	0x0	—	—
PIC32CM1216LE00032	0x2085200B	0x0	—	—

Table 2. PIC32CM LS00 Family Silicon Device Identification

Devices	Device ID (DID[31:0])	Silicon Revision ID (DID.REVISION[3:0])		
		A0	B0	C0
PIC32CM5164LS00100	0x20860X00	0x0	0x1	—
PIC32CM5164LS00064	0x20860X01	0x0	0x1	—
PIC32CM5164LS00048	0x20860X02	0x0	0x1	—
PIC32CM2532LS00100	0x20860X04	0x0	0x1	0x2
PIC32CM2532LS00064	0x20860X05	0x0	0x1	0x2
PIC32CM2532LS00048	0x20860X06	0x0	0x1	0x2
PIC32CM1216LS00048	0x2086200A	0x0	—	—
PIC32CM1216LS00032	0x2086200B	0x0	—	—

Table 3. PIC32CM LS60 Family Silicon Device Identification

Devices	Device ID (DID[31:0])	Silicon Revision ID (DID.REVISION[3:0])		
		A0	B0	C0
PIC32CM5164LS60100	0x20870X00	0x0	0x1	—
PIC32CM5164LS60064	0x20870X01	0x0	0x1	—
PIC32CM5164LS60048	0x20870X02	0x0	0x1	—

Note: Refer to the “Device Service Unit” chapter in the current Device Data Sheet (DS60001615) for a detailed information on Device Identification and Revision IDs for your specific device.

Table of Contents

1. Silicon Errata Summary

Module	Feature	Item #	Issue Summary	Affected Revisions			
				PFM (KB)	A0	B0	C0
ADC	Reference Buffer Offset Compensation	2.1.1	First ADC conversions are incorrect when using Reference Buffer Offset Compensation.	128	x		
				256	x	x	x
				512	x	x	
ADC	Offset Correction	2.1.2	Offset correction is not supported in the 8-bit and 10-bit conversion resolution.	128	x		
				256	x	x	x
				512	x	x	
ADC	Sequence State	2.1.3	The SEQSTATUS register is not updated properly when exiting Standby mode by an ADC conversions sequence event.	128	x		
				256	x	x	x
				512	x	x	
Boot ROM	Secure Boot using the ATECC608B (PIC32CM LS60 only)	2.2.1	Secure Boot using the ATECC608B is not functional if the Non-Secure Callable Flash (BOOT region) is used.	128			
				256	x		
				512	x		
DAC	First Conversion	2.3.1	First DAC Conversion after device power-up or after wake-up from Standby Low-Power mode is smaller than the expected value.	128	x		
				256	x	x	x
				512	x	x	
DAC	Spurious EMPTY Interrupt	2.3.2	When DAC refresh mode is disabled and a write to the DATABUFx register is performed, INTFLAG.EMPTYx interrupt is incorrectly set.	128	x		
				256	x	x	x
				512	x	x	
Device	Standby Current Consumption	2.4.1	Standby with PDSW power domain (Power Domain Switchable) configured in retention is not functional and generates an increased power consumption in Standby Sleep mode.	128			
				256	x		
				512	x		
Device	Standby entry	2.4.2	Potential hard fault upon standby entry when Systick interrupt is enabled	128	x		
				256	x	x	x
				512	x	x	
Device	Performance Level 0 Mode (PL0)	2.4.3	Performance Level 0 Mode (PL0) is incorrectly. configured and must not be used out of Boot ROM startup phase.	128			
				256	x		
				512	x		
Device	Performance Level 0 Mode (PL0)	2.4.4	PL0 is non-functional for E-temp devices.	128	x		
				256			x
				512			
EIC	PAC Protection	2.5.1	8-bit and 16-bit reads/writes on the reserved areas of the EIC registers mapping starting from the EVCTRL register do not generate a PAC protection error.	128	x		
				256	x	x	x
				512	x	x	
EIC	NMI Interrupt	2.5.2	If the NMI is configured in synchronous edge detection mode, spurious NMI interrupts may occur.	128	x		
				256	x	x	x
				512	x	x	
EVSYS	Software Events in Synchronous and Resynchronized modes	2.6.1	Software events in Synchronous and Resynchronized modes are not functional.	128			
				256	x	x	x
				512	x	x	
EVSYS	Synchronous Mode	2.6.2	Spurious Overrun Interrupt when the generic clock for a channel is always on.	128	x		
				256	x	x	x
				512	x	x	
EVSYS	Synchronous and Resynchronized modes	2.6.3	In synchronous and resynchronized modes, spurious event detections can be generated when registers in peripherals connected to the AHB-APB bridge on which the EVSYS is connected are accessed.	128	x		
				256	x	x	x
				512	x	x	

Silicon Errata Summary (continued)

Module	Feature	Item #	Issue Summary	Affected Revisions			
				PFM (KB)	A0	B0	C0
I²S	Client Mode with Host Clock Output enabled	2.7.1	When a Clock Unit n is configured in Client Mode, with the Serial Clock (SCKn) and the Frame Sync (FSn) as inputs, and with the Host Clock output (MCKn) enabled, the Host Clock output (MCKn) is not generated until the Serial Clock (SCKn) receives an active bit clock on its input.	128			
				256	x	x	x
				512	x	x	
MCLK	DFLLULP clock	2.8.1	Hardfault exception after having selected DFLLULP clock as main clock.	128	x		
				256	x	x	x
				512	x	x	
NVMCTRL	Data FLASH Silent Access and Scrambling	2.9.1	Silent Access and Scrambling on the Data FLASH are not functional when both are enabled.	128	x		
				256	x	x	x
				512	x	x	
NVMCTRL	Debug Mode	2.9.2	In Debug, if VREGPLL is enabled as well as the NVM Fast Wake Up feature, any flash controller access will stall.	128	x		
				256	x	x	x
				512	x	x	
NVMCTRL	Idle Mode Flash Corruption	2.9.3	Upon wake-up from IDLE in specific conditions, if the instruction following the WFI instruction is not prefetched or cached, CPU read in Flash can be corrupted.	128	x		
				256	x	x	x
				512	x	x	
OSCCTRL	FDPLL96M On Demand	2.10.1	The FDPLL96M On Demand mode is not functional in Standby Sleep mode.	128	x		
				256	x	x	x
				512	x	x	
OSC32KCTRL	External 32.768KHz Crystal Oscillator	2.11.1	External 32.768 kHz crystal oscillator operation is not supported over the full temperature range of -40°C to +85°C.	128			
				256	x		
				512	x		
SERCOM I²C	Fast-Mode Plus and Highspeed mode	2.12.1	When configured in HS or Fast-Mode Plus, SDA and SCL fall times are shorter than I²C specification requirement and can lead to reflection.	128			
				256	x	x	x
				512	x	x	
SERCOM SPI	Baud Register in Host mode	2.13.1	In Host mode, when Inter-Character Spacing is disabled, transmitted data on the MOSI pin is corrupted when BAUD = 0 in the BAUD register (i.e., when SCK = GCLK/2).	128			
				256	x		
				512	x		
SERCOM SPI	Hardware SPI Select Control	2.13.2	When Hardware SPI Select Control is enabled, the SPI Select ($\overline{SS}$) pin goes high after each byte transfer.	128	x		
				256	x	x	x
				512	x	x	
SERCOM SPI	Client Data Preload	2.13.3	Preloading a new SPI data before going into Standby Sleep mode, may lead to extra power consumption.	128	x		
				256	x	x	x
				512	x	x	
SERCOM SPI	SPI Transaction Length Error Status	2.13.4	When exiting from Standby with retention Sleep mode, the SPI Transaction Length Error Status value STATUS.LENERR can be wrong.	128	x		
				256	x	x	x
				512	x	x	
SERCOM USART	ISO7816 mode	2.14.1	In ISO7816 mode, the Receive Error Count register will be incremented twice if an error is detected when another Host (different from the CPU) makes an access during Standby mode.	128	x		
				256	x	x	x
				512	x	x	
SERCOM USART	LIN Host Delays	2.14.2	In SERCOM USART LIN Host mode, in the case where break, sync and identifier fields are automatically transmitted when DATA is written with the identifier, the LIN Host Header delay between the sync and the ID transmission fields is not correct.	128	x		
				256	x	x	x
				512	x	x	
SERCOM USART	Two Stop Bits Mode in LIN Host	2.14.3	Two stop bits mode is not supported in SERCOM USART LIN Host mode in the case where break, sync and identifier fields are automatically transmitted when DATA is written with the identifier.	128	x		
				256	x	x	x
				512	x	x	
TC	Capture mode / Over Consumption	2.15.1	Over consumption in Capture mode when entering Standby mode.	128	x		
				256	x	x	x
				512	x	x	

Silicon Errata Summary (continued)

Module	Feature	Item #	Issue Summary	Affected Revisions			
				PFM (KB)	A0	B0	C0
TC	Re-trigger	2.15.2	If a Re-trigger event occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is missing or disturbed.	128	x		
				256	x	x	x
				512	x	x	
TCC	Dithering Mode	2.16.1	Re-trigger in RAMP2 operations is not supported in Dithering mode.	128			
				256	x	x	x
				512	x	x	
TCC	RAMP2 Operations	2.16.2	Timer/Counter counting down mode is not supported in RAMP2 operations.	128			
				256	x	x	x
				512	x	x	
TCC	DMA Trigger	2.16.3	DMA trigger on Channel Compare Match does not work.	128			
				256	x	x	x
				512	x	x	
TCC	Re-trigger	2.16.4	If a Re-trigger event occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is missing or disturbed.	128			
				256	x	x	x
				512	x	x	
TCC	Re-trigger in RAMP2 Operations	2.16.5	Re-trigger in RAMP2 operations is not supported if a prescaler is used and the re-trig of the counter is done on the next GCLK.	128			
				256	x	x	x
				512	x	x	
TCC	DMA One-Shot Trigger mode	2.16.6	TCC Counter Overflow (OVF) DMA Trigger in DMA One-Shot Trigger mode is not functional for Critical RAMP2C and RAMP2CS operation modes.	128			
				256	x	x	x
				512	x	x	
FREQM	Lost interrupt	2.17.1	FREQM DONE interrupts interrupt may be lost.	128	x		
				256	x	x	x
				512	x	x	
FREQM	STATUS.BUSY	2.17.2	No timeout period for a FREQM measurement cycle.	128	x		
				256	x	x	x
				512	x	x	

2. Silicon Errata Issues

The following errata issues apply to the PIC32CM LE00/LS00/LS60 family of devices.

2.1. ADC

2.1.1. Reference Buffer Offset Compensation

Total Unadjusted Error (TUE) of the ADC conversion result is out of specification when,

- Using the reference source as REFCTRL.REFSEL ≠ AVDD
- Reference Buffer Offset Compensation is enabled (REFCTRL.REFCOMP = 1)

Workaround

The first five conversions after enabling ADC must be ignored. All further ADC conversions are within the specification.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.1.2. Offset Correction

Offset correction using the OFFSETCORR register is not supported in the 8-bit and 10-bit conversion resolution.

Workaround

None.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.1.3. Sequence State

The SEQSTATUS register is not updated properly when exiting Standby mode by an ADC conversions sequence event.

The first conversion source is done (available in the RESULT register), but is not identified and reported in the SEQSTATUS register.

Workaround

None.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.2. Boot ROM

2.2.1. Secure Boot Using the ATECC608B (PIC32CM LS60 only)

Secure Boot using the ATECC608B (BOCOR.BOOTOPT > 3) is not functional if the Non-Secure Callable Flash (BOOT region) is used (BOCOR.BNSC ! = 0)

Workaround

Set BOCOR.BNSC = 0 and use the Non-Secure Callable Flash (APPLICATION region) region (ANSC) instead of BSNC one to invoke functions from the BOOT region.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128						
256	X					
512	X					

2.3. DAC

2.3.1. First Conversion

First DAC Conversion after device power-up or after wake-up from Standby Low-Power mode is less than the expected value.

Workaround

Perform a second DAC conversion to get the desired value.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.3.2. Spurious EMPTY Interrupt

When DAC Refresh mode is disabled (DACCTRLx.REFRESH = 0x0) and a write to the DATABUFx register is performed, INTFLAG.EMPTYx interrupt is incorrectly set.

Workaround

Use DAC only in Refresh mode.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.4. Device

2.4.1. Increased Power Consumption in Standby Sleep Mode

Standby with PDSW power domain (Power Domain Switchable) configured in retention (STDBYCFG.PDCFG = 0, reset condition) is not functional and generates an increased power consumption in Standby Sleep mode.

Workaround

Force the PDSW power domain in Active mode by setting STDBYCFG.PDCFG = 1.

Note: Disabling the PDSW retention mode makes the Dynamic Power Gating feature unusable.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128						
256	X					
512	X					

2.4.2. Standby Entry

When the Systick interrupt is enabled and the standby back-bias option is set (STDBYCFG.BBIAS = 1), an hard fault can occur when the Systick interrupt coincides with the standby entry.

Workaround

Disable the Systick interrupt before entering standby and re-enable it after wake up.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.4.3. Performance Level 0 (PL0) Mode

Performance Level 0 (PL0) mode is incorrectly configured and must not be used out of Boot ROM startup phase. As a result, any information related to PL0 mode given in the "Electrical Characteristics" chapter is not valid and must be disregarded.

Workaround

User code must switch to Performance Level 2 (PL2) mode (PM -> PLCFG.PLSEL = 0x2) before accessing any other peripheral's registers.

Note: Arm® Cortex®-M23 core peripherals can be accessed before, if required.

As a result:

- The voltage regulators (MAINVREG and VREGPLL) cannot operate in PL0 including during Standby Sleep mode. This prevents from setting the SUPC -> VREG.STDBYPL0 to 1.
- The low-power voltage reference (ULPVREF) is not usable as it can only be used in PL0.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128						
256	X					
512	X					

2.4.4. Performance Level 0 (PL0) Mode

Performance Level 0 (PL0) mode is not functional on devices designated for Extended Temperature range (-E).

Workaround

User code must use Performance Level 2 (PL2) mode (PM -> PLCFG.PLSEL = 0x2).

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					

Performance Level 0 (PL0) Mode (continued)						
PFM (KB)	A0	B0	C0			
256			X			
512						

2.5. EIC

2.5.1. PAC Protection

8-bit and 16-bit read/write on the reserved areas of the EIC registers mapping starting from the EVCTRL register do not generate a PAC protection error.

Workaround

None.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.5.2. NMI Interrupt

If the NMI is configured in synchronous edge detection mode (NMICTRL.NMISENSE = 1, 2, or 3; NMICTRL.NMIASYNCH = 0), spurious NMI interrupts may occur after a software reset (CTRLA.SWRST = 1).

Workaround

- Configure one dummy EIC external interrupt x (EXTINTx) in edge detection mode.
- Enable the EIC: CTRLA.ENABLE = 1.
- Wait for synchronization completion (SYNCBUSY.ENABLE = 0).
- Configure the NMI in edge detection mode.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.6. EVSYS

2.6.1. Software Events in Synchronous and Resynchronized Modes

Software events in Synchronous and Resynchronized modes are not functional.

Workaround

Use software events in Asynchronous mode.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128						
256	X	X	X			
512	X	X				

2.6.2. Synchronous Mode

In Synchronous mode, spurious overrun interrupts can be generated when the generic clock for a channel is always ON (CHANNEL.ONDEMAND = 0).

Workaround

Set Generic Clock on Demand feature by setting CHANNEL.ONDEMAND = 1.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.6.3. Synchronous and Resynchronized modes

In Synchronous mode, including RESYNC mode, spurious event detections can be generated when accessing peripherals used in conjunction with the EVSYS.

Workaround

To avoid spurious EVSYS detections, EVSYS must be write protected by configuring the WRCTRL register in the PAC before being used.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.7. I^2S

2.7.1. Client Mode with Host Clock Output enabled

When a Clock Unit 'n' is configured in Client mode, with the Serial Clock (SCKn) and the Frame Sync (FSn) as inputs (CLKCTRLn.SCKSEL = 1, CLKCTRLn.FSSEL = 1), and with the Host Clock output (MCKn) enabled (CLKCTRLn.MCKEN = 1), the Host Clock output (MCKn) is not generated until the Serial Clock (SCKn) receives an Active Bit Clock on its input.

Workaround

Disable the Host Clock output (CLKCTRLn.MCKEN = 0) and use another clock source to generate the Host Clock output.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128						
256	X	X	X			
512	X	X				

2.8. MCLK

2.8.1. DFLLULP Clock Reference

A Hard fault exception can occur after selecting the DFLLULP clock as the main clock source (CTRLA.CKSEL = 1).

Workaround

Add 6 NOP instructions after writing the CTRAL.CKSEL bit.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.9. NVMCTRL

2.9.1. Data Flash Silent Access and Scrambling

Silent Access and Scrambling on the Data Flash are not functional when both are enabled. Silent Access as Data Flash scrambling remain functional if only one of them is configured by the application.

Workaround

None.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.9.2. Debug Mode

In Debug mode, if VREGPLL is enabled (SUPC VREGPLL.ENABLE = 1) as well as the NVM Fast Wake Up feature (NVMCTRL CTRLB.FWUP = 1), any Flash controller access will stall. If CPU is executing from Flash, this results in stalling the debug access port.

Workaround

In Debug mode, do not configure NVM Fast Wake Up mode (NVMCTRL CTRLB.FWUP = 1) if VREGPLL is enabled (SUPC VREGPLL.ENABLE = 1).

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.9.3. Idle Mode Flash Corruption

In the following conditions:

- CPU is in Thread mode (CPU core register PRIMASK = 1)
- CPU is in Idle Sleep mode
- Flash Power Reduction mode is enabled (CTRLB.SLEEPPRM = 0x0 or 0x1)

Upon wake up, if the instruction following the WFI instruction is not prefetched or cached, CPU read in Flash can be corrupted.

Workaround

Use any one of the following workarounds:

- Disable the Flash Power Reduction mode (CTRLB.SLEEPPRM = 0x3). This will affect the Standby Low-Power mode current consumptions.

- Relocate the WFI critical section in SRAM or in cache

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.10. OSCCTRL

2.10.1. FDPLL96M On Demand in Standby

The FDPLL96M On Demand mode (DPLLCTRLA.ONDEMAND = 1) is not functional in Standby Sleep mode.

Workaround

Set the DPLLCTRLA.ONDEMAND = 0 which makes the FDPLL96M always running in Standby Sleep mode.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.11. OSC32KCTRL

2.11.1. External 32.768 kHz Crystal Oscillator

The external 32.768 kHz crystal oscillator operation is not supported over the full temperature range of -40°C to +85°C.

Workaround

Limit the external 32.768 kHz crystal oscillator operation temperature range from 0°C to 85°C with a crystal ESR<70 kΩ.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128						
256	X					
512	X					

2.12. SERCOM I^2C

2.12.1. Fast-Mode Plus and High-Speed Mode

When configured in HS or Fast-Mode Plus, SDA and SCL fall times are not compliant to I^2C specification requirement and can lead to reflection.

Workaround

When reflection is observed, a 100Ω serial resistor can be added on the impacted line.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128						

Fast-Mode Plus and High-Speed Mode (continued)						
PFM (KB)	A0	B0	C0			
256	X	X	X			
512	X	X				

2.13. SERCOM SPI

2.13.1. BAUD Register in Host Mode

In Host mode, when Inter-Character Spacing is disabled (CTRLC.ICSPACE = 0), transmitted data on the MOSI pin is corrupted when BAUD = 0 in the BAUD register (i.e., when SCK = GCLK/2). This results in not achieving the maximum SCK frequency as documented in the "SPI Electrical Characteristics" chapter (MSP_1 parameter number).

Workaround

Select one of the following workarounds:

- Use a BAUD value in the BAUD register different from '0' by increasing the GCLK frequency.
- Enable the Host Inter-Character Spacing by writing a non-zero value to CTRLC.ICSPACE.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128						
256	X					
512	X					

2.13.2. Hardware SPI Select Control

When Hardware SPI Select Control is enabled (CTRLB.MSSEN = 1), the SPI Select ($\overline{SS}$) pin goes high after each byte transfer even if new data is ready to be sent.

Workaround

Set CTRLB.MSSEN = 0 and handle the SPI Select ($\overline{SS}$) pin by software.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.13.3. Client Data Preload

Preloading a new SPI data (CTRLB.PLOADEN = 1) before going into Standby Sleep mode, may lead to extra power consumption.

Workaround

None

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.13.4. SPI Transaction Length Error Status

When exiting from Standby with retention Sleep mode, the SPI Transaction Length Error Status value (STATUS.LENERR) can be wrong.

Workaround

Check the Transaction Length Error Status before entering Standby with retention Sleep mode. When exiting from Standby with retention Sleep mode, discard the STATUS.LENERR value by clearing it.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.14. SERCOM USART

2.14.1. ISO7816 Mode

In ISO7816 mode, the Receive Error Count register (RXERRCNT) will be incremented twice if an error is detected when another Host (different from the CPU) makes an access during Standby mode.

Workaround

None.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.14.2. LIN Host Delays

In SERCOM USART LIN Host mode (CTRLA.FORM = 0x2), in the case where break, sync, and identifier fields are automatically transmitted when data is written with the identifier (CTRLB.LINCMD = 0x2), the LIN Host Header delay between the sync and the ID transmission fields is not correct for the following cases:

- CTRLC.HDRDLY = 0x2, where the delay between sync and ID transmission fields is 8-bit time instead of 4-bit time.
- CTRLC.HDRDLY = 0x3, where the delay between sync and ID transmission fields is 14-bit time instead of 4-bit time.

Workaround

None.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.14.3. Two Stop Bits Mode in LIN Host

Two Stop bits mode (CTRLB.SBMODE = 0x1) is not supported in SERCOM USART LIN Host mode (CTRLA.FORM = 0x2) in the case where break, sync, and identifier fields are automatically

transmitted when data is written with the identifier (CTRLB.LINCMD = 0x2). Only one Stop bit is supported.

Workaround

None.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.15. TC

2.15.1. Capture Mode/Over Consumption

If the Time Counter x (TCx) is in Capture mode (TC.CTRLA.CAPTENx = 1) and TC.CTRLA.RUNSTBY = 0, the clock source driving GCLK_TCx can be kept running in Standby mode causing extra power consumption.

Workaround

Disable the Time Counter x (TCx) (TC.CTRLA.ENABLE = 0) which has a channel configured in Capture mode before going to Standby mode.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.15.2. Re-trigger

If a Re-trigger event (EVCTRL.EVACTn = 0x1, RETRIGGER) occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is corrupted.

Workaround

Use two channels to store their two successive (n and n+1) CC register values and combine their related waveform outputs to make signal redundancy.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.16. TCC

2.16.1. Dithering Mode

Re-trigger in RAMP2 operations (RAMP2, RAMP2A, RAMP2C, RAMP2CS) is not supported in Dithering mode.

Workaround

None.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128						
256	X	X	X			
512	X	X				

2.16.2. RAMP2 Operations

Timer/Counter counting down mode (CTRLBCLR.DIR = CTRLBSET.DIR = 1) is not supported in RAMP2 operations (RAMP2, RAMP2A, RAMP2C, RAMP2CS).

Workaround

Use Timer/Counter counting up mode (CTRLBCLR.DIR = CTRLBSET.DIR = 0).

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128						
256	X	X	X			
512	X	X				

2.16.3. DMA Trigger

DMA trigger on Channel Compare Match does not work.

Workaround

Use DMA trigger on Counter Overflow (OVF) or use the Channel Compare Match event output using the Event System as DMA trigger.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128						
256	X	X	X			
512	X	X				

2.16.4. Re-trigger

If a Re-trigger event (EVCTRL.EVACTn = 0x1, RETRIGGER) occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is corrupted.

Workaround

Use two channels to store their two successive (n and n+1) CC register values and combine their related waveform outputs to make signal redundancy.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128						
256	X	X	X			
512	X	X				

2.16.5. Re-trigger in RAMP2 Operations

Re-trigger in RAMP2 operations (RAMP2, RAMP2A, RAMP2C, RAMP2CS) is not supported if a prescaler is used (CTRLA.PRESCALER != 0) and the re-trig of the counter is done on the next GCLK (CTRLA.PRESCSYNC = GCLK or CTRLA.PRESCSYNC = RESYNC).

Workaround

Configure the re-trig of the counter on the next prescaler clock (CTRLA.PRESCSYNC = PRESC).

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128						
256	X	X	X			
512	X	X				

2.16.6. DMA One-Shot Trigger Mode

The TCC Counter Overflow (OVF) DMA Trigger in DMA One-Shot Trigger mode (CTRLA.DMAOS = 1) is not functional for Critical RAMP2C and RAMP2CS operation modes.

Workaround

None.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128						
256	X	X	X			
512	X	X				

2.17. Frequency Meter (FREQM)

2.17.1. Lost Interrupt

The FREQM DONE interrupts may be lost when the measurement period (CFGA.REFNUM * the reference clock period) is less than 4 APB clock periods.

Workaround

The measurement reference period must be longer than 4 APB clock periods.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

2.17.2. STATUS.BUSY

There is no timeout period for a FREQM measurement cycle. If the cycle count does not reach CFGA.REFNUM, the measurement cycle will not end and STATUS.BUSY will never deassert.

Workaround

If the measure signal may be very slow, may stop during the measurement, or have a frequency of 0Hz, the application code must monitor the measurement cycle and terminate it in an appropriate period of time.

Affected Silicon Revisions

PFM (KB)	A0	B0	C0			
128	X					
256	X	X	X			
512	X	X				

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest revision of the device data sheet (DS60001615):

Note: Corrections in tables, registers, and text are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

There are no new data sheet clarifications to report.

4. Revision History

Revision L - 06/2025

The following updates were performed for this revision:

- Updated the tables in *PIC32CM LE00/LS00/LS60 Family Errata* to reflect new silicon
- Updated the *Silicon Errata Summary* to reflect new silicon
- Updated all Silicon Revision tables in each Errata category to reflect new silicon

Revision K - 12/2024

Added the following new errata:

- Device: 2.4.4 Performance Level 0 Mode (PL0)

Revision J - May 2024

Updated Silicon Revision C0 in PIC32CM LE00/LS00/LS60 Family Errata to remove erroneous Silicon Revision ID designations.

Revision H - May 2024

Updated the silicon revision to C0 for this version of the document.

Revision G - May 2023

Added the following new errata:

- FREQM: 2.17.1 Lost Interrupt
- FREQM: 2.17.2 STATUS.BUSY

Revision F - December 2022

Added the following new errata:

- EIC: 2.5.2 NMI Interrupt
- SERCOM USART: 2.14.2 LIN Host Delays
- SERCOM USART: 2.14.3 Two Stop Bits in LIN Host

Revision E - June 2022

Added the following new errata:

- EVSYS: 2.6.3 Synchronous/Resynchronized Modes
- TCC: 2.16.6 DMA One-Shot Trigger Mode

Updated Table 3. PIC32CM LS60 Family Silicon Device Identification

Revision D - February 2022

The following updates were implemented in this revision:

- Updated the Silicon Revision throughout the document to B0

Revision C - January 2022

The following updates were implemented in this revision:

- Updated the Device ID in the Introduction
- Added the following new errata:
  - ADC: 2.1.3 Sequence State
- Removed obsolete Data Sheet Clarifications

Revision B - November 2021

The SPI, I^2S, and I^2C standards use the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client" respectively. These terms have been updated throughout this document for this revision.

Added the following silicon errata issues:

- Boot ROM: 2.2.1 Secure Boot Using the ATECC608B
- DAC: 2.3.2 Spurious EMPTY Interrupt
- I^2S: 2.7.1 Client Mode with Host Clock Output enabled
- NVMCTRL: 2.9.1 Data Flash Silent Access and Scrambling
- NVMCTRL: 2.9.2 Debug Mode
- NVMCTRL: 2.9.3 Idle Mode Flash Corruption
- OSCCTRL: 2.10.1 FDPLL96M On Demand in Standby
- OSC32KCTRL: 2.11.1 External 32.768KHz Crystal Oscillator

Revision A - November 2020

This is the initial released version of this document.

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