IC Card Interface Technical Note

BD8905F/FV, BD8906F/FV

●Summary

3V, 5V Smart card interfaces IC.
Install between smart card and controller. This IC operates as bi-directional buffer, and supply 3V or 5V to smart card.
Card contact pin will be protected by I/O cell, ESD capability is more than HBM: ±6000V.

●Feature

1) Half duplex bi-directional buffer 3 system.
2) All card contact pin is protected from short.
3) Card power supply (VREG) 3V or 5V.
4) Card supply has over current protection.
5) Include thermal shutdown circuit.
6) Include power supply voltage detector.
7) Automatically rising and Falling sequencer function
   Rising sequence：Depend on controller signal（CMDVCCB↓）
   Falling sequence：Depend on controller signal（CMDVCCB↑）and fault detection (ejection of card, card supply short, IC heat detect, VDD or VDDP drop).
8) Enhanced ESD protection on Card contact pin (≧±6000V).
9) 2MHz – 26MHz crystal oscillator.
10) Clock generation for card is 1, 2, 4 or 8 divisions available.
11) RST output is controlled by RSTIN input signal (positive conversion output).
12) Card status output by OFFB.

●Application

Smart card interface
B-CAS card interface

2007.Oct.

●Absolute Maximum Ratings（Ta=25℃）

Parameter		Symbol	Limit	Unit	Condition	
VDD Supply voltage		V_{DD}	-0.3～6.5	V		
VDDP Supply voltage		V_{DDP}	-0.3～6.5	V		
I/O pin voltage		V_{IN} V_{OUT}	-0.3～+6.5	V	Pin：XTAL1, XTAL2, VSEL, RSTIN, AUX1C, AUX2C, IOC, CLKDIV1, CLKDIV2, CMDVCCB, OFFB, PORADJ, S2	
Card contact pin voltage		V_{REG}	-0.3～+6.5	V	Pin：PRES, PRESB, CLK, RST, IO, AUX1, AUX2	
Charge pump voltage		V_n	-0.3～+14.0	V	Pin：VCH, S1	
Junction temperature		T_{jmax}	+150	℃		
Operating temperature		T_{opr}	-25～+85	℃		
Storage temperature		T_{stg}	-55～+150	℃		
Power dissipation	BD890XF	P_{tot}	750	mW	Ta=-25～+85℃	*See below about. package power dissipation
	BD890XFV		1060			

・This product is not designed for protection against radioactive rays.
・Absolute Maximum Ratings does not warrant operating.
・BD890XF: BD8905F/BD8906F (Package: SOP28)
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・BD890XF: BD8905F/BD8906F (Package: SOP28)
・BD890XFV: BD8905FV/BD8906FV (Package: SSOP-B28)

●Operating Condition (Ta=25℃)

Parameter		Symbol	MIN	TYP	MAX	Unit	Condition
VDD voltage	BD8905F/FV	V_{DD}	2.7	-	5.5	V	
	BD8906F/FV		3.0	-	5.5	V	
VDDP voltage		V_{DDP}	4.5	5.0	5.5	V	VREG=5V; Ivreg≦60mA
			3.0	-	4.5	V	VREG=5V; Ivreg≦20mA
			3.0	5.0	5.5	V	VREG=3V; Ivreg≦60mA

●Package Dissipation

Package thermal capacity is plotted on figure below, only when you use Rohm standard board.
Don't use at over thermal capacity condition. Please check your thermal capacity out.

BD890XF: Pd=750mW, however de-rating in done at 6mW/℃ for operating above Ta≧25℃.
BD890XFV: Pd=1060mW, however de-rating in done at 8.5mW/℃ for operating above Ta≧25℃.

Rohm standard board： size: 70×70×1.6(mm^3) material: FR4 glass epoxy board (Copper foil area is below 3%)

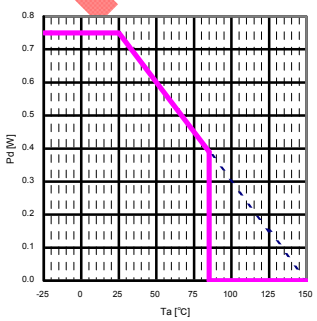


Fig.1 BD890XF

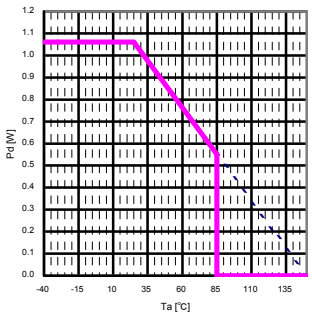


Fig.2 BD890XFV

●Block diagram

BD8905F/FV, BD8906F/FV

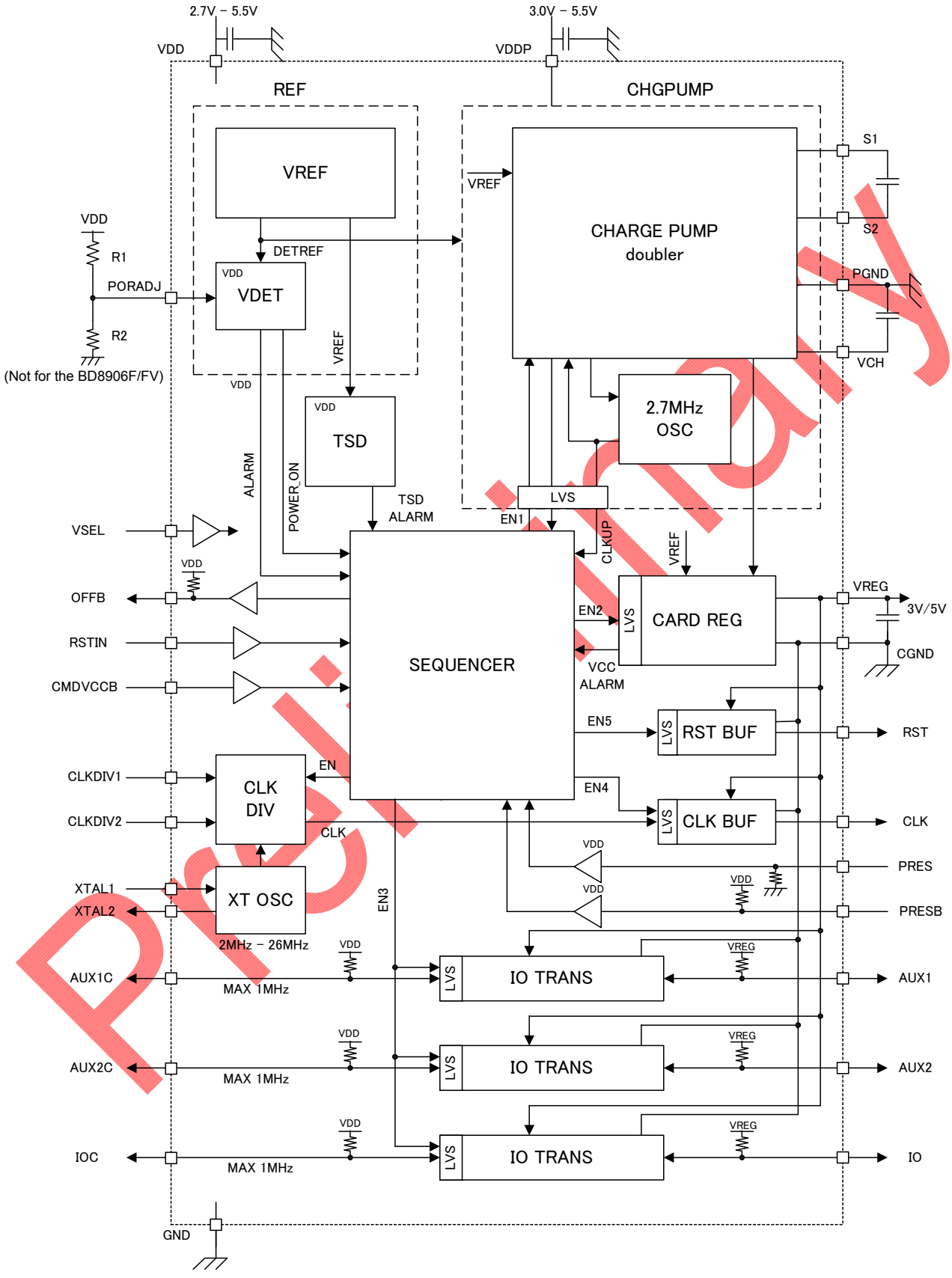


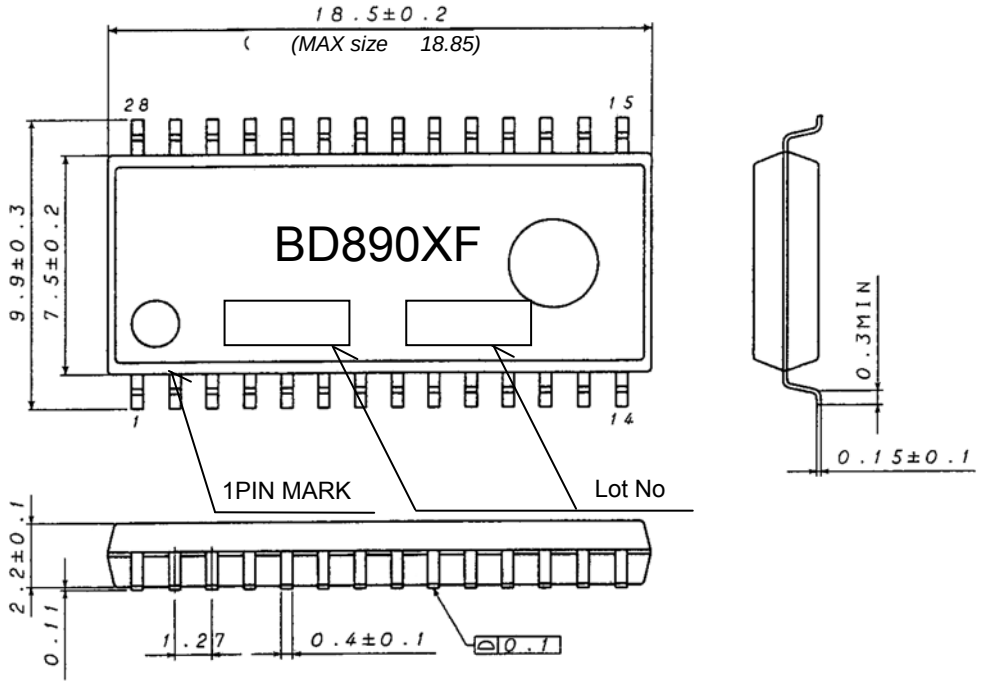
Fig.3

●Pin Direction

Pin no.	Pin name	I/O	Signal level	Condition
1	CLKDIV1	I	VDD	Clock frequency setting input1
2	CLKDIV2	I	VDD	Clock frequency setting input1
3	VSEL	I	VDD	Card supply voltage setting input: “H”: VREG=5V, “L”: VREG=3V
4	PGND	S	GND	GND for charge pump
5	S2	I/O	-	Capacitors connection for charge pump (S1 to S2)：C = 100nF (ESR < 100mΩ)
6	VDDP	S	VDDP	Charge pump power supply
7	S1	I/O	-	Capacitors connection for charge pump (S1 to S2):C = 100nF (ESR < 100mΩ)
8	VCH	I/O	-	Charge pump output: decupling capacitor; C = 100nF (ESR < 100mΩ) connect during VCH and PGND.
9	PRESB	I	VDD	Card insertion detect pin (Active ”L”) When PRES or PRESB are active, decision on card inserted, and it will enter input stabilization time of typ8ms. 2MΩ pull-up to VDD.
10	PRES	I	VDD	Card insertion detect pin (Active ”H”) When PRES or PRESB are active, decision on card inserted, and it will enter input stabilization time of typ. 8ms. 2MΩ pull-down to GND
11	IO	I/O	VREG	I/O data line to smart card 11kΩ pull-up to VREG
12	AUX2	I/O	VREG	I/O data line to smart card 11kΩ pull-up to VREG
13	AUX1	I/O	VREG	I/O data line to smart card 11kΩ pull-up to VREG
14	CGND	S	GND	GND
15	CLK	O	VREG	Card clock output
16	RST	O	VREG	Card reset output
17	VREG	O	VREG	Connected capacitance (ESR < 100mΩ) of 100nF～220nF between Card power supply and CGND.
18	PORADJ/NC	I	-	Power-on-reset voltage set pin; using external bridge (Not for the BD8906F/FV)
19	CMDVCCB	I	VDD	Activation sequence will start after detection of falling edge from controller.
20	RSTIN	I	VDD	Card reset signal input
21	VDD	S	VDD	VDD pin
22	GND	S	GND	GND
23	OFFB	O	VDD	Alarm output pin (Active “L”) NMOS output, 20kΩ pull-up to V_{DD}
24	XTAL1	I	VDD	Cristal connected or external Clock input
25	XTAL2	O	VDD	Cristal connected (treat as open if clock supplied externally.)
26	IOC	I/O	VDD	I/O data line to controller 11kΩ pull-up to VDD
27	AUX1C	I/O	VDD	I/O data line to controller 11kΩ pull-up to VDD
28	AUX2C	I/O	VDD	I/O data line to controller 11kΩ pull-up to VDD

●Package

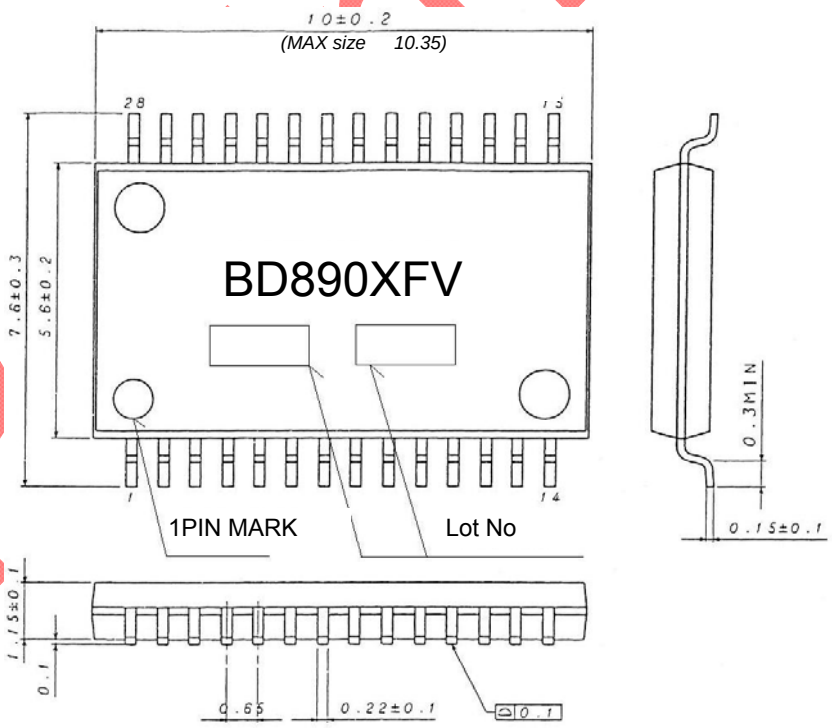
Package product name SOP28



(UNIT : mm)

Fig.4-1 BD890XF Package Outline

Package product name SSOP-B28



(UNIT : mm)

Fig.4-2 BD890XFV Package Outline

●Function

1) Power supply

Power supply terminal is VDD and VDDP. VDD make a same voltage to signal from the system controller side.
VDDP and PGND are the power supplies, GND of charge pump circuit, and it is a POWER source of supply to the card.
Depends on setup pin VSEL 3V (VSEL: L) or 5V (VSEL: H) is supplied to the card through a VREG terminal.

2) VDD supply voltage detector (Not for the BD8906F/FV)

VDD power supply voltage detector setup (VDETR and VDETF: Fig.3) is done by connecting a resistance bridge (R1 and R2: Fig.1) to the PORADJ.
After VDD rises more than V_{DETR} and takes about 16ms (internal reset) more, power on reset (Alarm) is released.
And IC becomes sleep state until CMDVCCB becomes H to L.

◆The calculation of the power supply voltage detector resistance bridge R1 and R2.

Alarm release voltage (V_{DETR}) and a low voltage detection voltage (V_{DETF}) are calculated with the following equation.
You must set up VDETF more than 2.3V.

VDD rising PORADJ voltage: VDD_{THR}
VDD falling PORADJ voltage: VDD_{THF}

$$V_{DETR} = \left(\frac{R1}{R2} + 1\right) \times VDD_{THR} \qquad V_{DETF} = \left(\frac{R1}{R2} + 1\right) \times VDD_{THF}$$

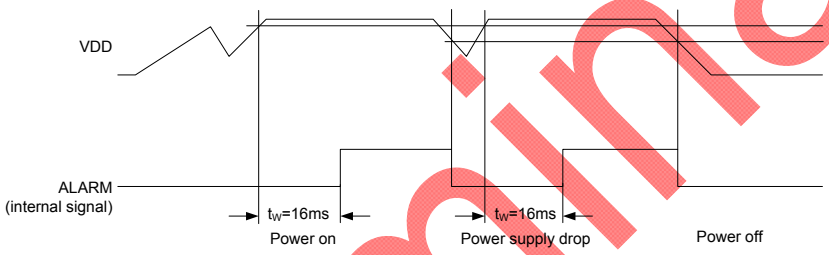


Fig.5 VDD power supply detection

3) Operation sequence

3-1) Standby mode

An IC becomes standing by condition until a CMDVCCB signal becomes H->L after a VDD voltage rose more than VDTER and the power on resetting (Alarm) was canceled.
VDD power supply voltage detector (VDET) a thermal shutdown circuit (TSD), a voltage reference circuit (VREF), a crystal oscillation circuit (XT OSC) and internal oscillator circuit (OSC) operate in this mode.
Pull-up is done by the resistance of 11KΩ with IOC, AUX1C and AUX2C to VDD. And all card contact terminals are Lo levels.

3-2) Card insertion

The insertion condition of the card is detected by the PRES or the PRESB. It is judged that a card is being inserted when either a PRES terminal or a PRESB terminal is active.

Table 1

PRES	“High” Active
PRESB	“Lo” Active

When a card is inserted under the sleep condition, either terminal of the card insertion distinction terminal PRES (H: It is active.) and PRESB (L: It is active.) becomes active. OFFB becomes H about 8mS in that (debounce time) rest.
OFFB becomes H after it was reset inside and debounce time passed when a card is being inserted before a VDD power supply stands up and internal resetting is released. PRESS is being pull-down to GND by 2MΩ, and PRESSB is being pull-up to VDD by 2MΩ.

3-3) Rising sequence

When a CMDVCCB signal from the controller becomes H->L under the OFFB = H, a rising sequence is started, and each function block starts in the following order.

RSTIN is enabled after I/O TRANS ON and passes 300ns.

After I/O TRANS turns it on, TIN input becomes effective in about 300ns.

CLK signal is outputted when RSTIN becomes Lo before RST output is canceled after RSTIN becomes effective. In case of RSTIN is High when RST is released, CLK output correspond to RST release.（See Fig.4、Fig.5、Fig.6）

CHARGE PUMP ON (VCH voltage output)

↓

CARDREG ON (VREG output)

↓

I/O TRANS ON (All I/O Bus: Pull-up)

↓

↓ (RSTIN ≠ Always High) ↓ RSTIN to RST release during High ↓ (RSTIN = Always High)

↓

CLK BUF ON (CLK output) CLK,RST BUF ON (CLK output, RST release)

↓

RST BUF ON (RST release)

【Rising sequence by the difference in the RSTIN input timing】

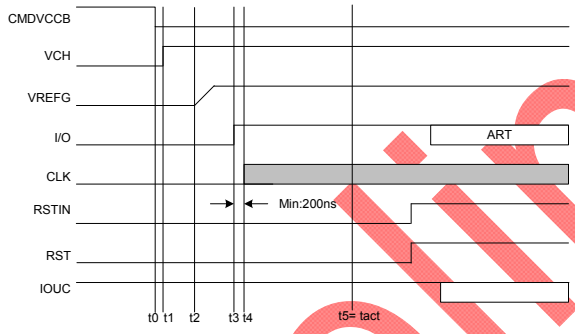


Fig.6-1 Rising sequence1

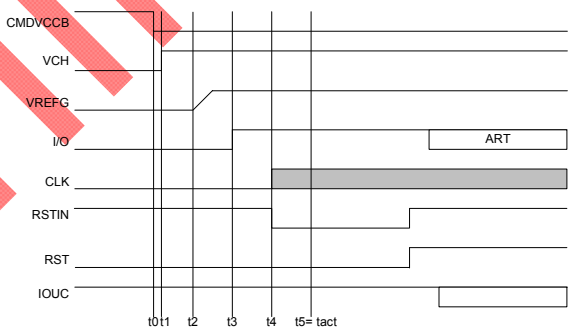


Fig.6-2 Rising sequence2

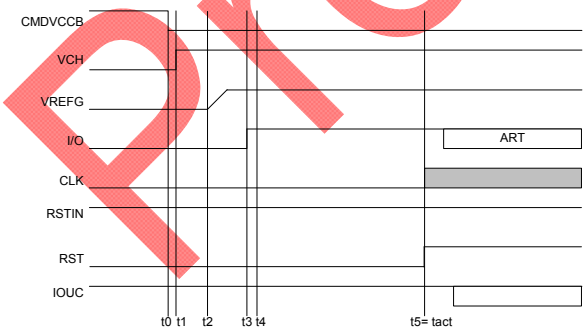


Fig.6-3 Rising sequence 3

t1: VCH rise startup time = typ. 21.4 μ s

t2: VREG rise startup time = typ. 57 μ s

t3: I/O ON time = typ. 116.2 μ s

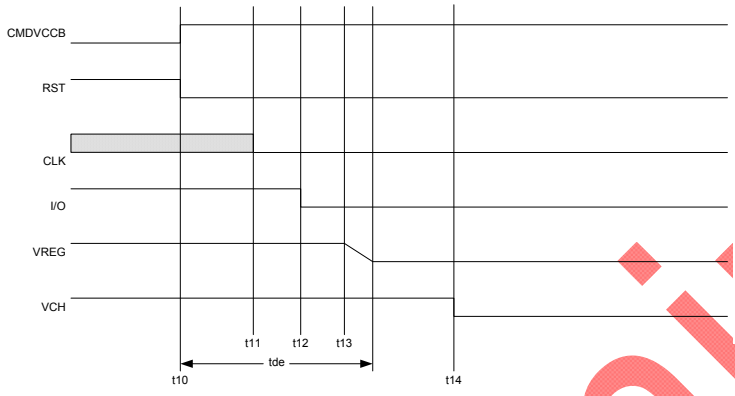
t4: CLK output release time (t4-t3) = Min. 200 μ s

t5: RST release time (Activation time) = typ. 187.4 μ s

3-4) Falling sequence

When CMDVCCB input becomes L->H or Alarm signal (mentioning later) is detected, falling sequence start in the following order and a sequence shifts to the standby mode.

RST BUF OFF (RST: Lo)
↓
CLK BUF OFF (CLK: Lo)
↓
I/O TRANS OFF (Controller side I/O Bus: Pull-up)
↓ (Card side I/O Bus: Lo)
↓
CARDREG OFF (VREG: Lo)
↓
CHARGE PUMP OFF



t11: CLK OFF time = typ. 11.9 μs
t12: I/O OFF time = typ. 23.7 μs
t13: VREG shutdown time = typ. 35.6 μs
t14: VCH shutdown time = typ. 118.5 μs
tde: finishing sequence complete time = Max. 100 μs

Fig.7 Falling sequence

4) CHARGE PUMP

Charge circuit is the power supply of the CARD REG output. It starts operation when CMDVCCB input becomes H->L. Then, it operates as double boost circuit or voltage follower by VDDP voltage.

VCH output becomes the power supply of the CARDREG circuit.

Arrange two flying capacitance (S1-S2 space and the VCH-PGND space) in the neighborhood of the IC as much as possible so that ESR may become less than 100mΩ so that charge pump circuit may wash away big charge electric current. Arrange capacitor in VDDP and the space of PGND as well in the neighborhood of the IC as much as possible again so that ESR may become less than 100mΩ.

5) CARD REG

CARD REG does the power supply from the VREG terminal to the IC card.

VREG output voltage is changed to 3V or 5V by the setup of the VSEL.

Table2 VSEL pin setting

VSEL	VREG output voltage	VDDP voltage	MAX current
0	3V	3.0V ～ 5.5V	65mA
1	5V	3.0V ～ 4.5V	20mA
1	5V	4.5V ～ 5.5V	60mA

This regulator built-in an over current limit circuit. Internal Alarm signal is taken out at the load current of about 140m A and more. And it goes into shutdown sequence. When VREG output voltage falls below 0.6V for 3V mode and 1.0V for 5V mode, detect fault, cutoff output current, output internal alarm and being shutdown sequence.

To suppress output voltage fluctuation, install capacitance (100nF, 200nF, 330nF) as near as possible between VREG and CGND. And ESR is less than 100mΩ.

CARD REG output is power supply of CLK and RST output. Therefore, CLK and RST output level become VREG output levels.

6) I/O data conversion

Three data lines IOC - IO, AUX1C - AUX1 and AUX2C - AUX2 transmit and receive data bi-directionally and independently. Until it becomes I/O TRANS ON by rising sequence, controller side pin IOC, AUX1C and AUX2C are done pull-up to High (VDD level) by 11KΩ, and IOC, AUX1C and AUX2C of card contact pin are Lo.

When I/O TRANS it becomes On, IC becomes idol state, IOC, AUX1C and AUX2C pin are VDD electric potential (High), and IO, AUX1 and AUX2 pin are VREG electric potential (High). I/O pins are pull-up by 11KΩ to VDD level (IOC, AUX1C and AUX2C) or VREG level (IO, AUX1, AUX2).

The one that data transited in H->L first as to either becomes muster, and output on the opposition side becomes slave with the controller side terminal and the card contact terminal. Then, data are transmitted on slave side from muster side. It takes a drive to High the data by active Pull-up (less than 100ns) to do a data transition at high speed at the moment when it got over threshold when a signal transits in H from L. Pull-up is done by the resistance of 11KΩ with a terminal after the active Pull-up end. Transmitter and receiver make a signal to 1MHz possible by this function. And over current limit of 15mA is given to IO, AUX1 and AUX2 of the card contact terminal.

7) Card clock supply

Clock supply to the card has an input signal from the XTAL1 terminal by 1 by the setup of CLKDIV1 and the CLKDIV2 terminal, and it is outputted more than a CLK terminal. Divider changeover time is within 8 clock of the XTAL1 signal. (See; Table1)

XTAL1 terminal input signal inputs a pulse signal from the signal by crystal frequency (2MHz to 26MHz) between XTAL1 and the XTAL2 terminal or the outside. The one within 48%-52% at duty with a XTAL1 terminal must do transition time in the signal period within 5% to set duty in the CLK terminal at 45%-55 %.

Use it by 1/2, 1/4 and a 1/ 8-minute lap setup though it depends to draw a circuit board to assure duty 45%-55 %.

Table3 Clock frequency selection list (f_{XTAL}:XTAL1 in frequency)

CLKDIV1	CLKDIV2	f_{clk}
0	0	$\frac{f_{XTAL}}{8}$
0	1	$\frac{f_{XTAL}}{4}$
1	1	$\frac{f_{XTAL}}{2}$
1	0	$\frac{f_{XTAL}}{1}$

8) RSTIN input, RST output

CMDVCCB signal: RSTIN input becomes effective in about 300ns after I/O TRANS turns it on after H->L is inputted and rising sequence starts. After a CMDVCCB signal becomes H->L again, it is canceled in about 200μsec, and it follows RSTIN input, and RST output outputs a signal.

9) Fault detection

When the following fault condition is detected, internal alarm signal is taken out, and it stands up, and lowered, and a sequence is shifted to the action, the standing by condition. Still it is standing by condition when a card hasn't been inserted from the beginning.

・When a VREG terminal lowered more than 1V (when VSEL=H) or 0.6V (when VSEL=L) or over current (TYP: 150mA) flowed to the terminal.

・When VDD electric potential is lower than a detect voltage. (When power supply voltage detector is detected.)

・When it was detected in the high temperature by the thermal shutdown circuit.

・When a VCH terminal voltage unusually fell down.

・When a card was removed during the movement or when a card hasn't been inserted from the beginning. (When PRES=L and PRESB=H)

10) OFFB output

OFFB output is the output terminal which shows that it is in the condition that IC can work. Pull-up is being raised by the resistance of 20KΩ in VDD.

OFFB is High when it is in the condition that it can work. When fault condition is detected, OFFB output outputs off condition (Lo).

Internal alarm signal is canceled, and OFFB output becomes High when a card is being inserted and fault condition is canceled and CMDVCCB becomes High.

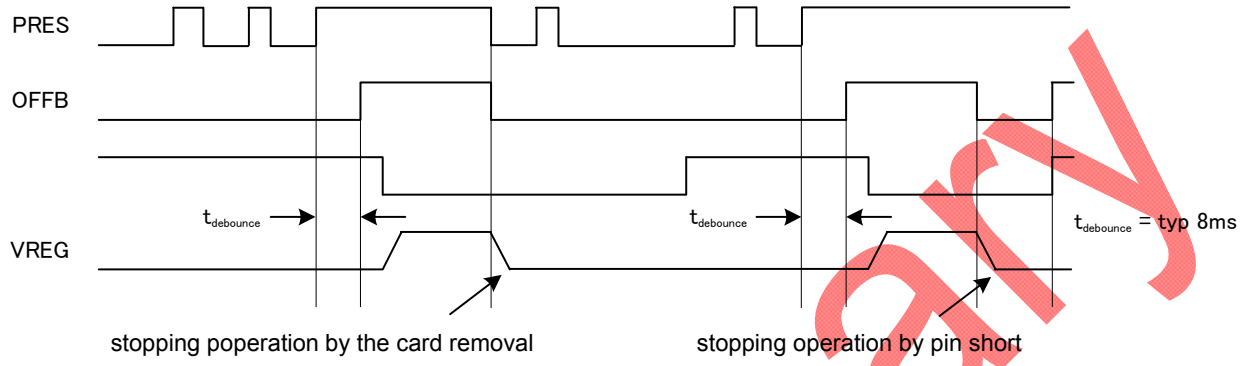


Fig.8 OFFB, CMDVCCB, PRES, VREG Operation

●Caution in use

1) Put two capacitor for charge pump on in the space between S1 in the neighborhood of the IC and S2 and in VCH and the space of PGND as much as possible so that ESR may become less than 100mΩ.
2) Put capacitor of the VREG terminal on VREG in the neighborhood of the IC and the space of CGND as much as possible so that ESR may become less than 100mΩ.
3) Put a capacitor beyond 10μF+0.1μF between GND's in the neighborhood of the IC in VDD and VDDP as much as possible because of the power supply noise decrease so that ESR may become less than 100mΩ. Using the capacitor of the big capacity as much as possible is recommended.

●Application

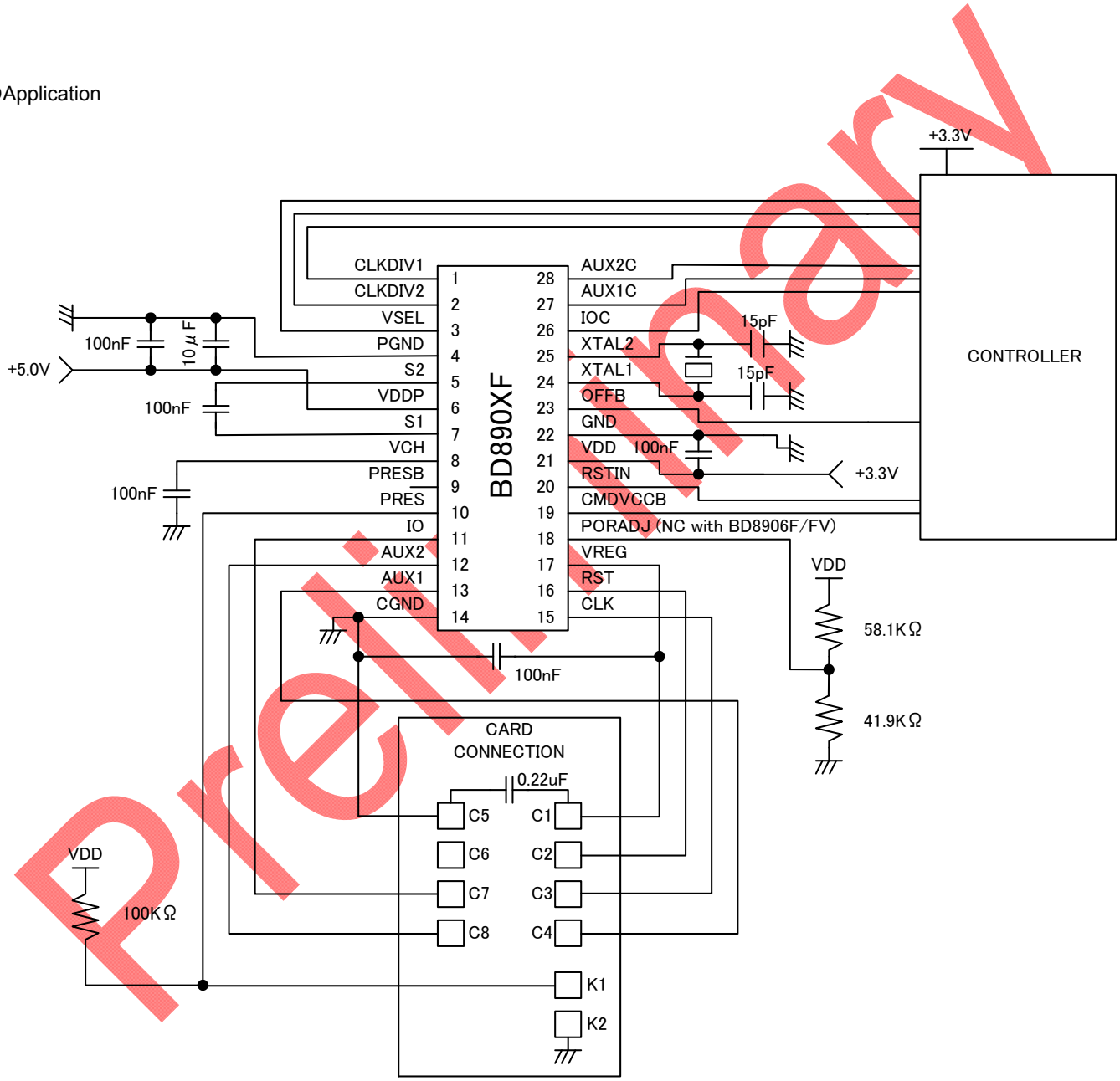


Fig.9