MPQ5852

36V, Smart Diode Controller with Two Voltage Monitors, AEC-Q100 Qualified

DESCRIPTION

The MPQ5852 is a smart diode controller that can drive an external N-channel MOSFET to replace a Schottky diode for reverse input protection. The device's 20mV ultra-low dropout minimizes power loss and enables a low minimum input voltage (V_{IN}). Its 4μA standby current makes the device ideal for battery-powered applications. The MPQ5852's ultra-fast transient response rectifies the AC frequency up to 50kHz.

The MPQ5852 integrates an internal boost to provide a boost voltage that turns on the external N-MOSFET even at a low V_{IN}. With an extremely low under-voltage (UV) threshold, the device provides a wide operating range to meet the harsh start-up conditions defined in ISO 16750. The device also supports cold-crank voltages down to 0V.

The MPQ5852 provides reverse polarity protection and reverse pulse protection. In addition, the device provides multiple diagnostics for automotive electronic control units (ECUs) under fault conditions, such as UV, over-voltage (OV), and over-temperature (OT) conditions.

The MPQ5852 is available in a QFN-13 (3mmx3mm) package with wettable flanks, and is AEC-Q100 qualified.

FEATURES

- Built to Handle Tough Automotive Transients and Meet AEC-Q100 Requirement
  - Load Dump Up to 42V
  - -40V Reverse Polarity Voltage
  - Cold Crank Down to 0V
  - Rectifies AC Frequency Up to 50kHz
  - Available in AEC-Q100 Grade 1

FEATURES *(continued)*

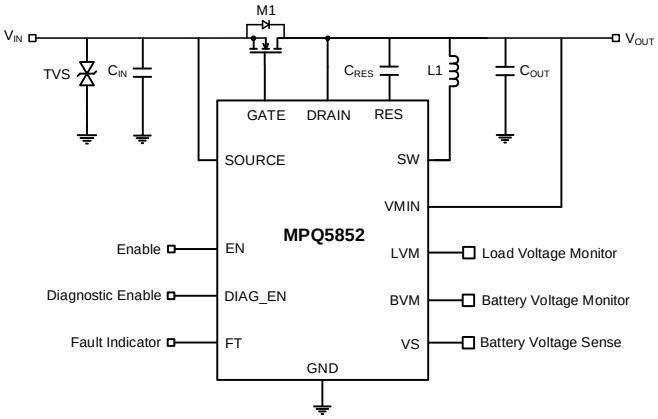
- Cooler Thermals
  - Strong Gate Drive Ability and Small Switching Loss
  - 20mV Ultra-Low Dropout
- Extends Vehicle Battery Life
  - Low Quiescent Current (I_Q) in Standby (4μA)
  - Low I_Q in Rectify Mode (30μA)
  - DIAG_EN Pin to Disable Diagnostics for Low-I_Q Operation
- Reduces Board Size
  - Available in a QFN-13 (3mmx3mm) Package
  - Available in Wettable-Flank Package
- Robust Protection and Diagnostics
  - Battery and Load Under-Voltage (UV) and Over-Voltage (OV) Monitoring
  - Battery Voltage Sensing
  - Over-Temperature (OT) Warning
  - Fault Indication via the FT pin
- Functional Safety System Design Capability
  - MPSafe™ Compatible: Functional Safety Supporting Document Available

MPSafe™ Fusa Compatible

APPLICATIONS

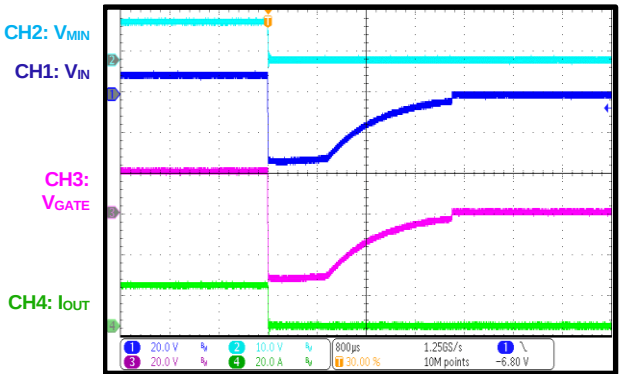
- Automotive System Protection
- Automotive Advanced Driver-Assistance Systems (ADAS)
- Automotive Infotainment Systems: Digital Clusters, Head Units, and Cameras
- Industrial Equipment
- Battery-Powered Systems

TYPICAL APPLICATION



Negative Pulse

V_{OUT} = 12V, I_{OUT} = 20A, TVS diode: SMBJ26CA



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ5852GQE-xxxx-AEC1***, ****	QFN-13 (3mmx3mm)	*See Below*	1

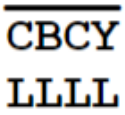
* For Tape & Reel, add suffix -Z (e.g. MPQ5852GQE-xxxx-AEC1-Z).

** Moisture Sensitivity Level Rating

*** Wettable Flanks

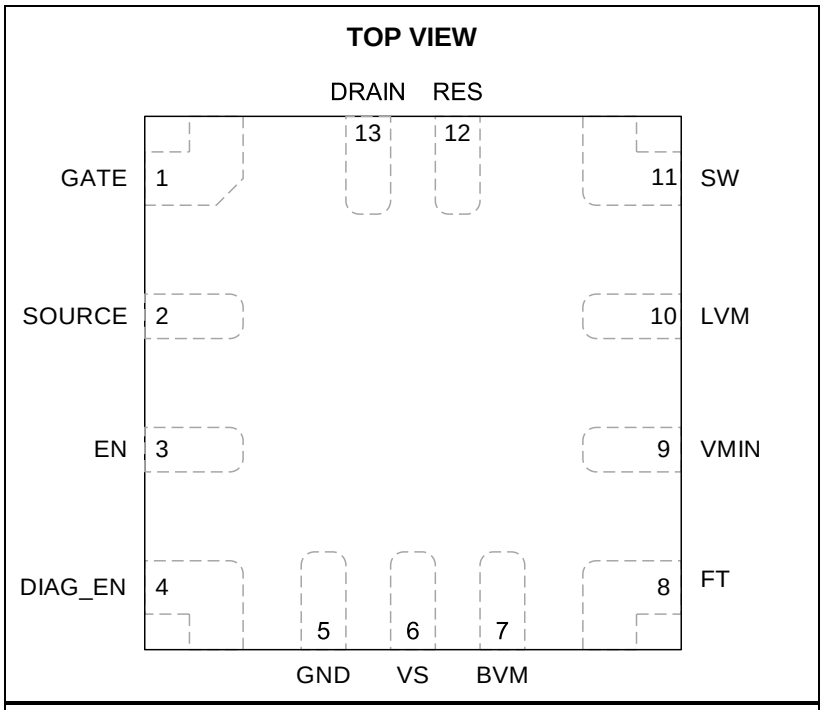
**** “xxxx” is the configuration code identifier. Each “x” can be a hexadecimal value between 0 and F. The default code is “0000”. Work with an MPS FAE to create this unique number.

TOP MARKING



CBC: Product code
Y: Year code
LLLL: Lot number

PACKAGE REFERENCE



QFN-13 (3mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	GATE	**Gate connection.** Connect the GATE pin to the external power MOSFET's gate.
2	SOURCE	**Source connection.** Connect the SOURCE pin to the source of the external power MOSFET. The voltage sensed on this pin works with the DRAIN pin voltage (V_{DRAIN}) to control the MOSFET gate.
3	EN	**Enable**. Pull the EN pin above the rising threshold (1.2V) to enable the chip; pull EN below the falling threshold (1V) to shut down the chip. Do not float the EN pin. If the shutdown function is not used, connect EN to the DRAIN pin.
4	DIAG_EN	**Diagnostic enable.** Pull the DIAG_EN pin above the rising threshold (1.2V) to enable the diagnostic features; pull DIAG_EN below the falling threshold (1V) to disable diagnostics, which reduces the standby current. The diagnostic features include the voltage monitors and voltage sensing. Do not float the DIAG_EN pin. Connect this pin to the GND pin if not used.
5	GND	**Device ground.** Connect the GND pin to the board's ground plane.
6	VS	**Voltage sense**. The VS pin outputs a voltage proportional to the SOURCE pin voltage (V_{SOURCE}) when V_{SOURCE} is between 4V and 28V. If V_{SOURCE} exceeds 28V, the VS output is clamped to 3.1V. Float the VS pin if not used.
7	BVM	**Battery voltage monitor**. BVM is an open-drain pin. When V_{SOURCE} is below its configurable under-voltage (UV) threshold, this pin asserts low.
8	FT	**Fault indicator.** FT is an open-drain pin. When the device is enabled and the diagnostic function is enabled, this pin is pulled low if a fault condition is detected, including thermal warning or the VMIN pin being under over-voltage (OV) conditions for longer than 140µs. FT is also pulled low if the boost converter loses regulation. Float the FT pin if not used.
9	VMIN	**Voltage monitor input**. The VMIN pin is connected to a power rail to monitor whether an OV or UV condition occurs. Connect this pin to the DRAIN pin if not used.
10	LVM	**Load voltage monitor**. LVM is the VMIN monitor and is an open-drain pin. When the voltage on the VMIN pin (V_{MIN}) is below its configurable UV threshold, this pin asserts low. Float the LVM pin if not used.
11	SW	**Switch node of the internal boost regulator.** Connect an inductor between the SW and DRAIN pins.
12	RES	**Reservoir supply.** The RES pin is the power supply for the external power MOSFET gate driver. Connect a minimum 1µF ceramic capacitor between the RES and DRAIN pins.
13	DRAIN	**Drain connection.** Connect the DRAIN pin to the external power MOSFET's drain. DRAIN is the power supply of the internal circuitry, and also controls the MOSFET's gate voltage. Connect a minimum 4.7µF capacitor between the DRAIN pin and ground, placed as close as possible to the device.

ABSOLUTE MAXIMUM RATINGS (1)

SOURCE, EN.....-40V to +42V
DRAIN, VMIN.....-0.3V to +42V
GATE to SOURCE.....-0.3V to +14V
DRAIN to SOURCE .....-2V to +52V (2)
RES to DRAIN .....-0.3V to +14V
SW .....-0.3V to +56V
DIAG_EN, BVM, FT, LVM.....-0.3V to +6V
VS .....-0.3V to +5V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C
Continuous power dissipation (3) 1.92W

ESD Ratings

Human body model (HBM) .....Class 2 (4)
Charged-device model (CDM) ..... Class C2b (5)

Recommended Operating Conditions

Supply voltage (V_{IN}) .....5V to 36V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-13 (3mmx3mm)
JESD51-7.....65.1…4.7...°C/W (6)

Ψ_{JT}
JESD51-7.....1.9...°C/W (6)

Notes:

1) Exceeding these ratings may damage the device.
2) Absolute maximum ratings are rated under room temperature. Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can generate excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Per AEC-Q100-002.
5) Per AEC-Q100-011.
6) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The θ_{JC} value shows the thermal resistance from the junction-to-case bottom, and the Ψ_{JT} value shows the characterization parameter from the junction-to-case top.

ELECTRICAL CHARACTERISTICS

V_{SOURCE} = 12V, V_{EN} = 2V, V_{RES} = 23V, T_J = -40°C to +150°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Operating Voltage						
DRAIN under-voltage lockout (UVLO) rising threshold	V_{DRUV_R}			2.8	3.2	V
DRAIN UVLO falling threshold	V_{DRUV_F}		2.4	2.6	2.8	V
DRAIN UVLO hysteresis	V_{DRUV_HYS}			0.2		V
Operating Current						
Standby current	I_{SBY}	V_{EN} = V_{DIAG_EN} = 0V, T_J = 25°C		4	10	µA
		V_{EN} = V_{DIAG_EN} = 0V, T_J = -40°C to +150°C			20	µA
Quiescent current in rectify mode	I_{Q_REC}	V_{EN} = 2V, V_{DIAG_EN} = 0V, T_J = 25°C		30	50	µA
		V_{EN} = 2V, V_{DIAG_EN} = 0V, T_J = -40°C to +125°C			100	µA
		V_{EN} = 2V, V_{DIAG_EN} = 0V, T_J = -40°C to +150°C			120	µA
Quiescent current in diagnostics mode	I_{Q_DIAG}	V_{EN} = 0V, V_{DIAG_EN} = 2V, T_J = 25°C		50	80	µA
		V_{EN} = 0V, V_{DIAG_EN} = 2V, T_J = -40°C to +150°C			120	µA
Total quiescent current	I_Q	V_{EN} = 2V, V_{DIAG_EN} = 2V, T_J = 25°C		70	100	µA
		V_{EN} = 2V, V_{DIAG_EN} = 2V, T_J = -40°C to +150°C			200	µA
Rectifier						
SOURCE-to-DRAIN regulation voltage	V_{SD}		10	20	30	mV
SOURCE-to-DRAIN fast pull-up threshold	V_{SD_FPU}		50	75	100	mV
SOURCE-to-DRAIN fast pull-down threshold	V_{SD_FPD}		-10	-4	0	mV
Fast pull-up resistance	R_{FPU}	$V_{GATE\text{-}TO\text{-}RES}$ = -2V		30	50	Ω
Fast pull-down resistance	R_{FPD}	$V_{GATE\text{-}TO\text{-}SOURCE}$ = 2V		3.5	9	Ω
Reverse biased gate-to-source voltage	V_{GS_RB}	V_{SOURCE} = -5V, I_{GATE} = 1mA		0.01	0.3	V
		V_{SOURCE} = -36V, I_{GATE} = 1mA		0.01	0.3	V
Gate turn-on delay time	t_{ON}	Step (V_{SOURCE} - V_{DRAIN}) from -100mV to +3V, $V_{RES\text{-}TO\text{-}DRAIN}$ = 11V, $C_{GATE\text{-}TO\text{-}SOURCE}$ = 10nF		1.2	2	µs
Gate turn-off delay time	t_{OFF}	Step (V_{SOURCE} - V_{DRAIN}) from +3V to -100mV, $V_{RES\text{-}TO\text{-}DRAIN}$ = 11V, $C_{GATE\text{-}TO\text{-}SOURCE}$ = 10nF		1	2	µs
Gate rising time (7)	t_{RISING}	Step (V_{SOURCE} - V_{DRAIN}) from -100mV to +3V, $V_{RES\text{-}TO\text{-}DRAIN}$ = 11V, $C_{GATE\text{-}TO\text{-}SOURCE}$ = 10nF		1200		ns
Gate falling time (7)	$t_{FALLING}$	Step (V_{SOURCE} - V_{DRAIN}) from +3V to -100mV, $V_{RES\text{-}TO\text{-}DRAIN}$ = 11V, $C_{GATE\text{-}TO\text{-}SOURCE}$ = 10nF		150		ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{SOURCE} = 12V, V_{EN} = 2V, V_{RES} = 23V, T_J = -40°C to +150°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Maximum rectification frequency (7)	f_{MAX}	V_{PP} = 6V, $C_{GATE-TO-SOURCE}$ = 15nF		50		kHz
Boost Converter						
Reservoir UVLO rising threshold	V_{RES_R}		9	10.5	12	V
Reservoir UVLO falling threshold	V_{RES_F}		8.6	10.3	11.9	V
Reservoir UVLO hysteresis	V_{RES_HYS}	V_{RES_R} - V_{RES_F}		0.2		V
Reservoir regulation rising voltage	V_{REG_R}		9.5	11	12.5	V
Reservoir regulation falling voltage	V_{REG_F}		9.4	10.9	12.4	V
Reservoir regulation UVLO hysteresis	$V_{REG\_UVLO\_HYS}$	V_{REG_R} - V_{REG_F}		0.1		V
Boost current limit	I_{BOOST}		160	220	280	mA
SW leakage current	I_{SW}				1	µA
Boost power MOSFET on resistance	$R_{DS(ON)\_SW}$			1.7	3.8	Ω
Boost rectifier diode's voltage drop	V_{DIODE}	I_{DIODE} = 220mA		0.9		V
Boost blanking time	t_{BLANK}			100	250	ns
Enable (EN) and DIAG_EN						
EN rising threshold	V_{EN_R}		1.1	1.2	1.3	V
EN falling threshold	V_{EN_F}		0.9	1	1.1	V
EN hysteresis	V_{EN_HYS}			200		mV
EN leakage current	I_{EN}	V_{EN} = 2V			3	µA
		V_{EN} = 12V			6	
DIAG_EN rising threshold	V_{DIAG_R}		1.1	1.2	1.3	V
DIAG_EN falling threshold	V_{DIAG_F}		0.9	1	1.1	V
DIAG_EN hysteresis	V_{DIAG_HYS}			200		mV
DIAG_EN leakage current	I_{DIAG}	V_{DIAG_EN} = 2V		1	3	µA
Voltage Sensing and Monitor						
SOURCE under-voltage (UV) falling threshold	$V_{UV\_BVM\_F}$		5	5.25	5.5	V
SOURCE UV hysteresis	$V_{UV\_BVM\_HYS}$			10		% of $V_{UV\_BVM\_F}$
BVM output voltage low	V_{BVM_LOW}	I_{SINK} = 1mA		0.1	0.3	V
BVM UV status reporting deglitch time	t_{BVM_DEG}		100	125	150	µs
VMIN UV falling threshold	$V_{UV\_LVM\_F}$		4.2	4.4	4.6	V
VMIN UV hysteresis	$V_{UV\_LVM\_HYS}$			10		% of $V_{UV\_LVM\_F}$

ELECTRICAL CHARACTERISTICS *(continued)*

V_{SOURCE} = 12V, V_{EN} = 2V, V_{RES} = 23V, T_J = -40°C to +150°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
LVM output voltage low	V_{LVM_LOW}	I_{SINK} = 1mA		0.1	0.3	V
VMIN UV or over-voltage (OV) status reporting deglitch time	t_{LVM_DEG}		115	140	165	µs
VMIN OV rising threshold	V_{OVM}		15.5	16.5	17.5	V
VMIN OV hysteresis	V_{OVM_HYS}			10		% of V_{OVM}
VS sensing ratio	k_{VS}	V_S to V_{SOURCE}		1/10		V/V
VS OV clamping voltage	V_{CL_VS}		2.9	3.1	3.3	V
VS current capability	I_{VS}			1		mA
VS sensing accuracy	$\Delta V_S / V_S$	4V ≤ V_{SOURCE} < 6V	-2.5		+2.5	% of V_S
		6V ≤ V_{SOURCE} < 9V	-2		+2	% of V_S
		9V ≤ V_{SOURCE} < 28V	-1.5		+1.5	% of V_S
Fault						
FT output voltage low	V_{FT_LOW}	I_{SINK} = 1mA		0.1	0.3	V
Thermal warning threshold (7)	T_{OTW}	T_J > T_{OTW}, FT reports		155		°C
Thermal warning hysteresis (7)	T_{OTW_HYS}	T_J < T_{OTW} - T_{OTW_HYS}, FT recovers		20		°C

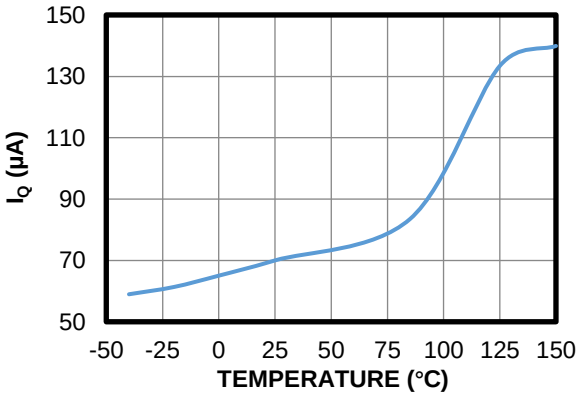
Note:

7) Derived from bench characterization. Not tested in production.

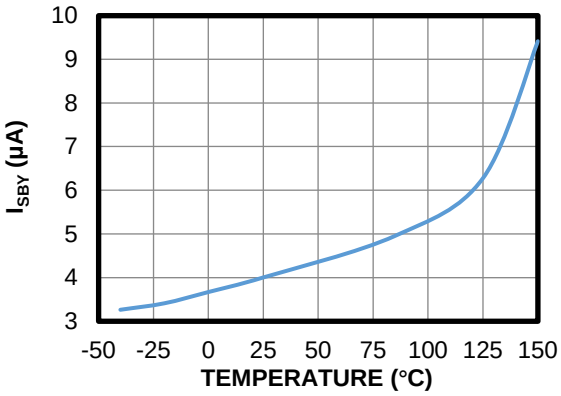
TYPICAL CHARACTERISTICS

V_{IN} = 12V, L = 22µH, T_J = -40°C to +150°C, unless otherwise noted.

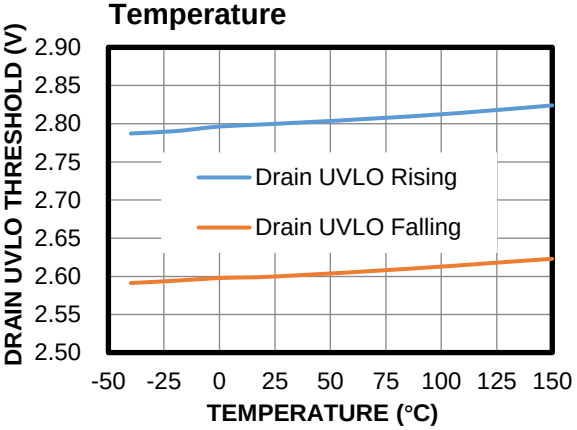
Total Quiescent Current vs. Temperature



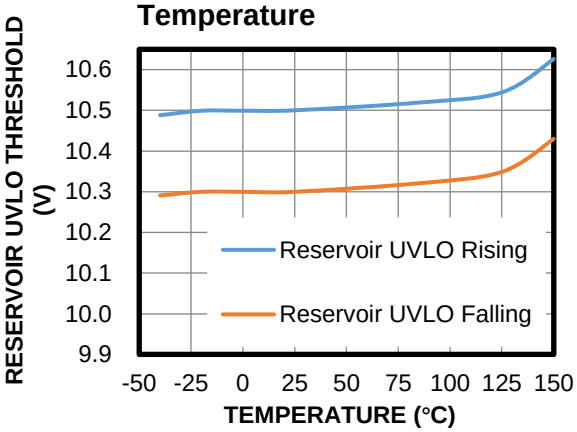
Standby Current vs. Temperature



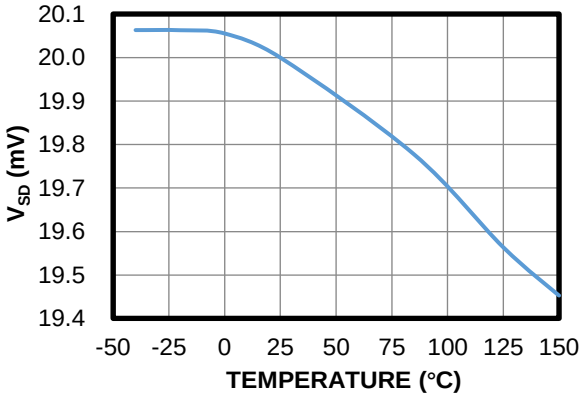
DRAIN UVLO Threshold vs. Temperature



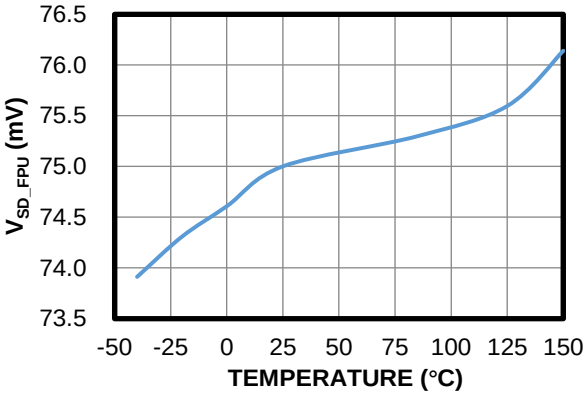
Reservoir UVLO Threshold vs. Temperature



SOURCE-to-DRAIN Regulation Voltage vs. Temperature



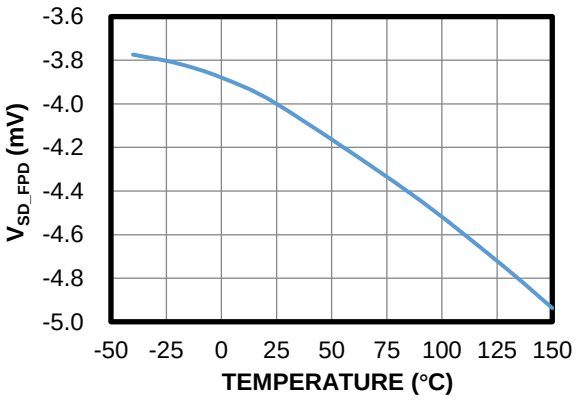
SOURCE-to-DRAIN Fast Pull-Up Threshold vs. Temperature



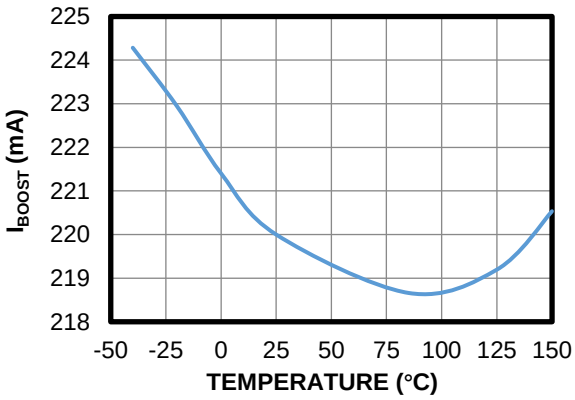
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, L = 22µH, T_J = -40°C to +150°C, unless otherwise noted.

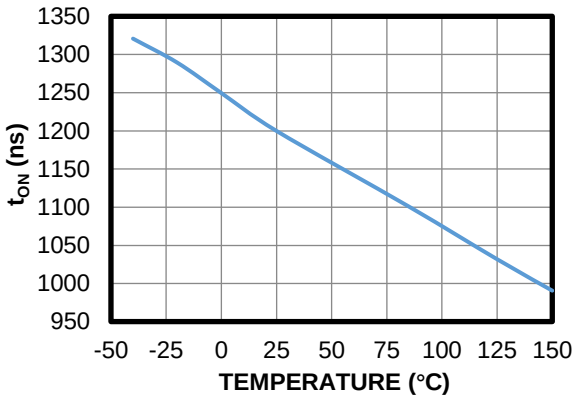
SOURCE-to-DRAIN Fast Pull-Down Threshold vs. Temperature



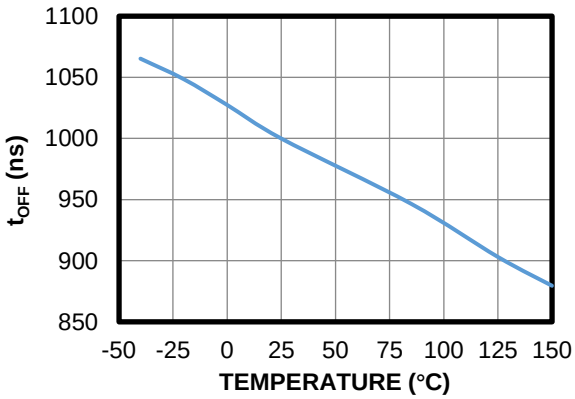
Boost Current Limit vs. Temperature



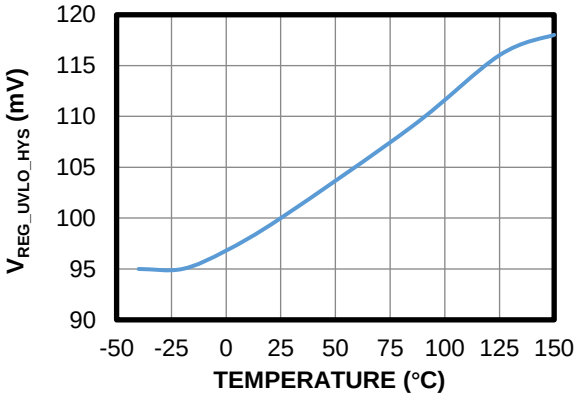
Gate Turn-On Delay Time vs. Temperature



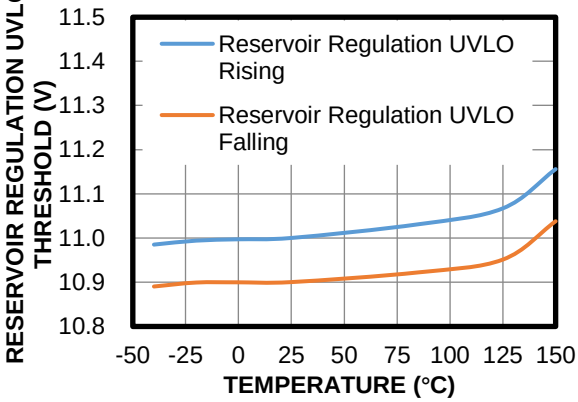
Gate Turn-Off Delay Time vs. Temperature



Reservoir Regulation UVLO Hysteresis vs. Temperature



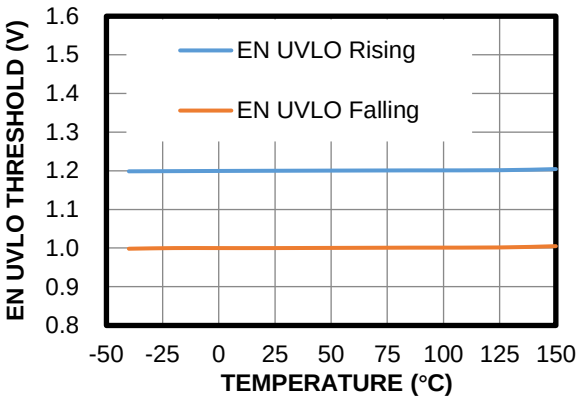
Reservoir Regulation UVLO Threshold vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, L = 22µH, T_J = -40°C to +150°C, unless otherwise noted.

EN UVLO Threshold vs. Temperature

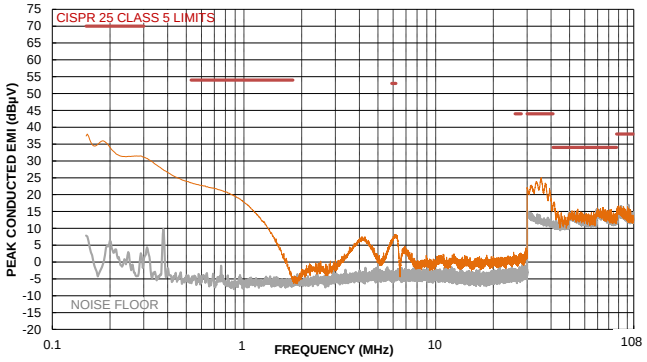


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 20A, L = 22µH, C_{OUT} = 440µF, T_A = 25°C, unless otherwise noted. (8)

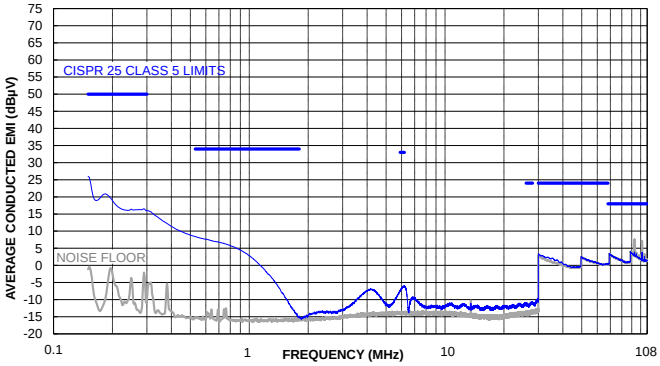
CISPR 25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



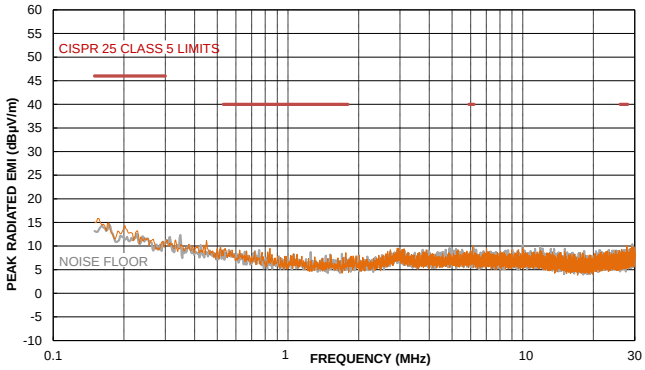
CISPR 25 Class 5 Average Conducted Emissions

150kHz to 108MHz



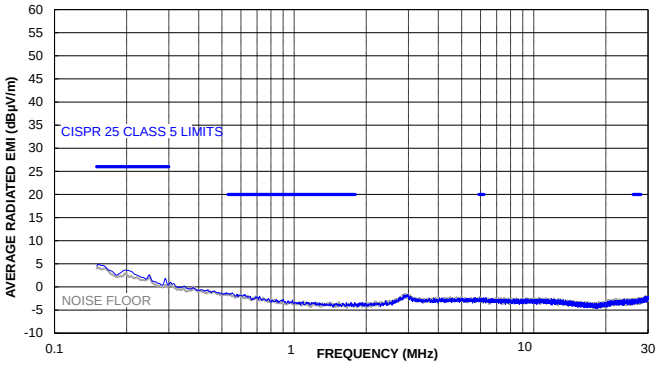
CISPR 25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



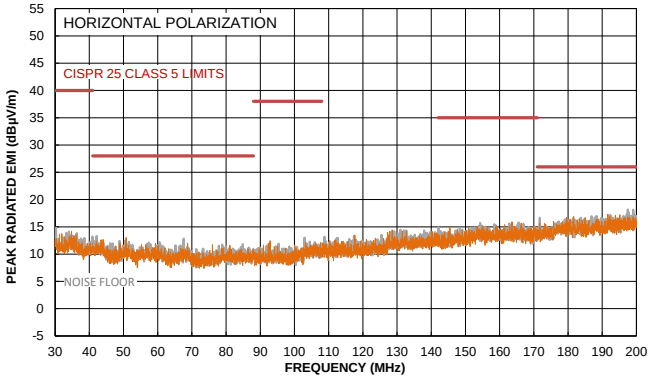
CISPR 25 Class 5 Average Radiated Emissions

150kHz to 30MHz



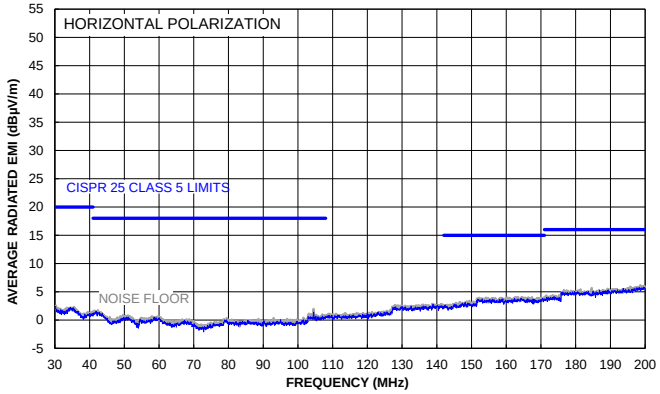
CISPR 25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



CISPR 25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz

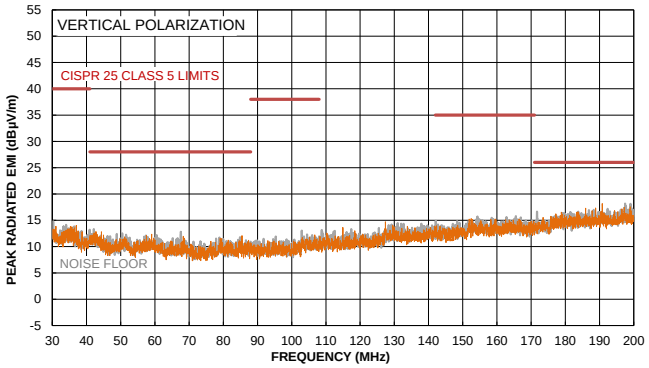


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 20A, L = 22µH, C_{OUT} = 470µF, T_A = 25°C, unless otherwise noted. (8)

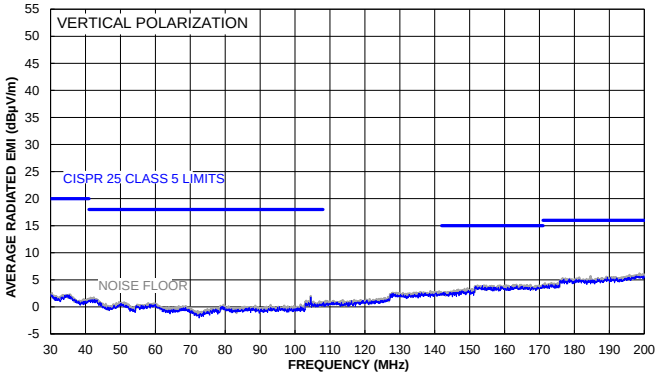
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



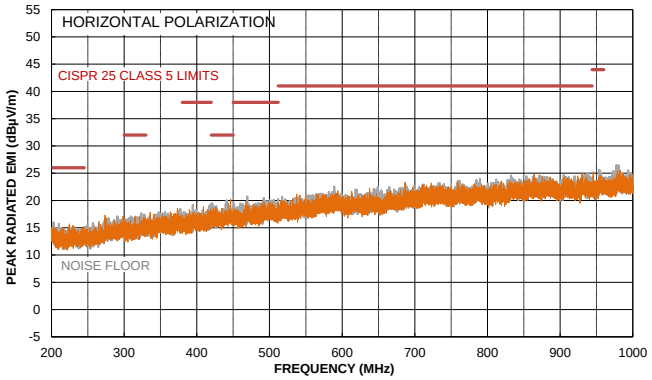
CISPR 25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



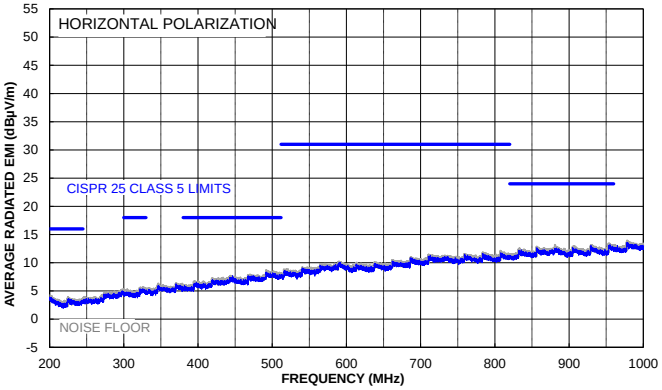
CISPR 25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



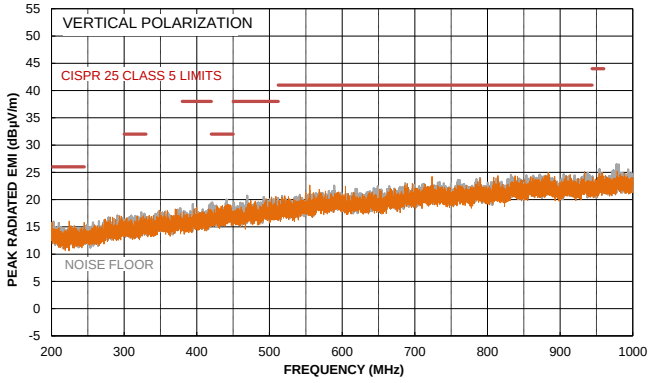
CISPR 25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



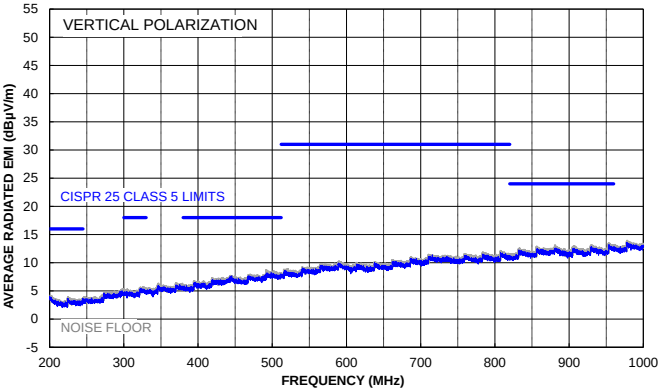
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Vertical, 200MHz to 1GHz



Note:

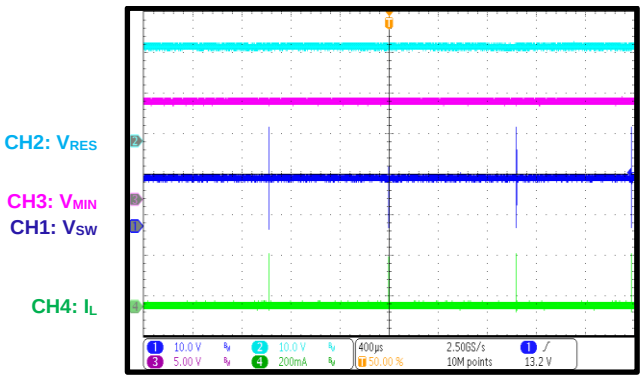
8) The EMC test results are based on the application circuit and tested on the EVQ5852-Q-00A (see Figure 7 on page 33).

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 20A, L = 22µH, T_A = 25°C, unless otherwise noted.

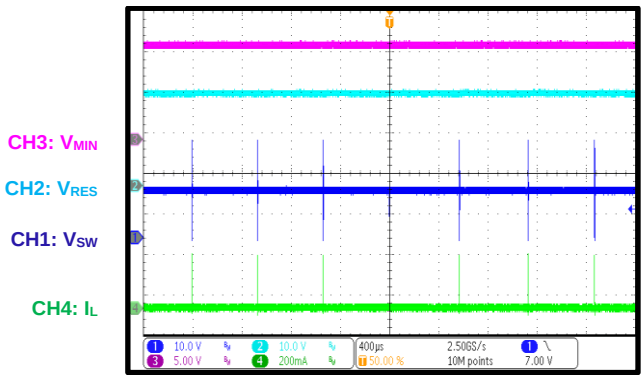
Steady State (for Internal Boost)

I_{OUT} = 0A



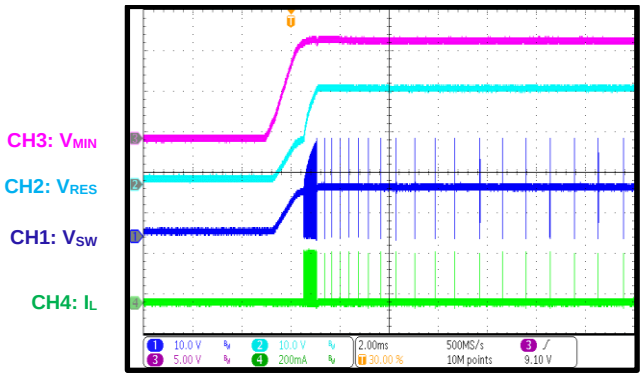
Steady State (for Internal Boost)

I_{OUT} = 20A



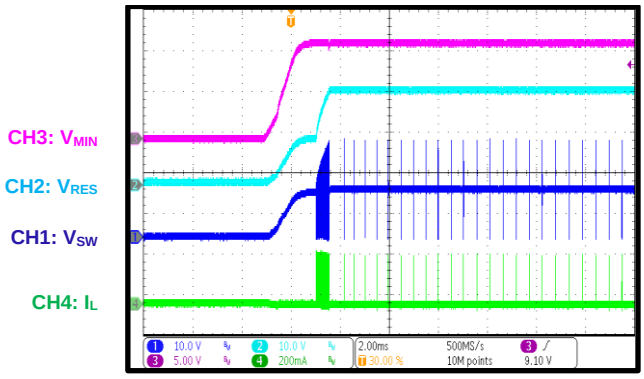
Start-Up through VIN (for Internal Boost)

I_{OUT} = 0A



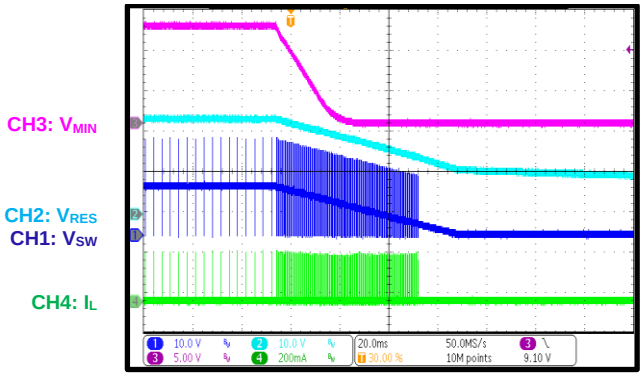
Start-Up through VIN (for Internal Boost)

I_{OUT} = 20A



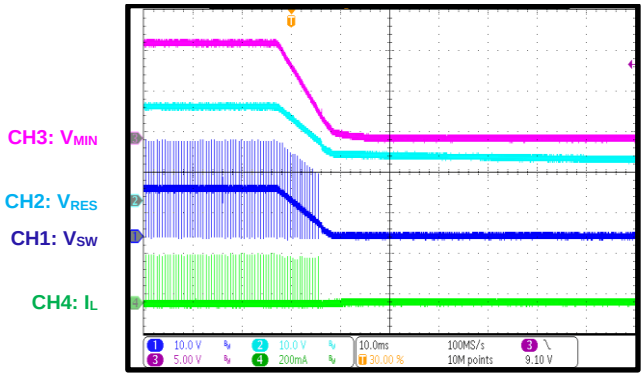
Shutdown through VIN (for Internal Boost)

I_{OUT} = 0A



Shutdown through VIN (for Internal Boost)

I_{OUT} = 20A

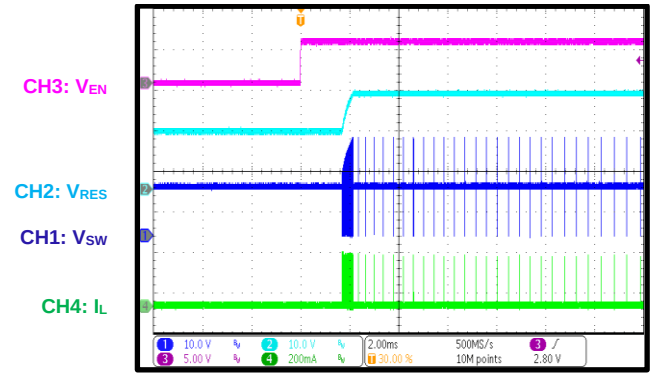


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 20A, L = 22µH, T_A = 25°C, unless otherwise noted.

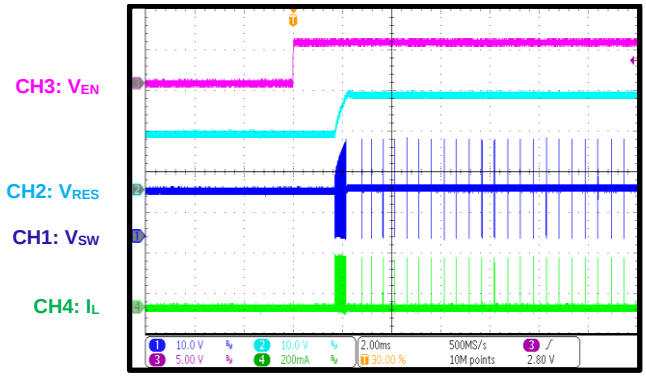
Start-Up through EN (for Internal Boost)

I_{OUT} = 0A



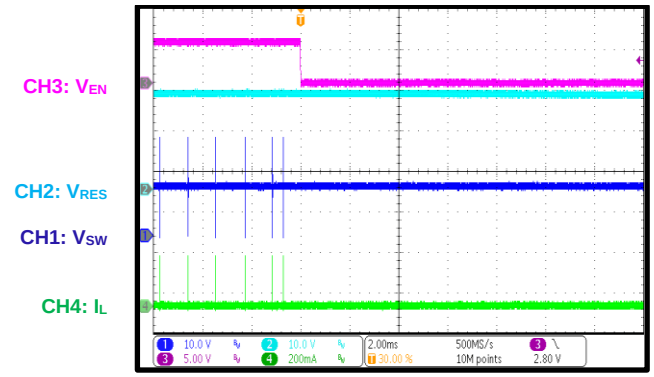
Start-Up through EN (for Internal Boost)

I_{OUT} = 20A



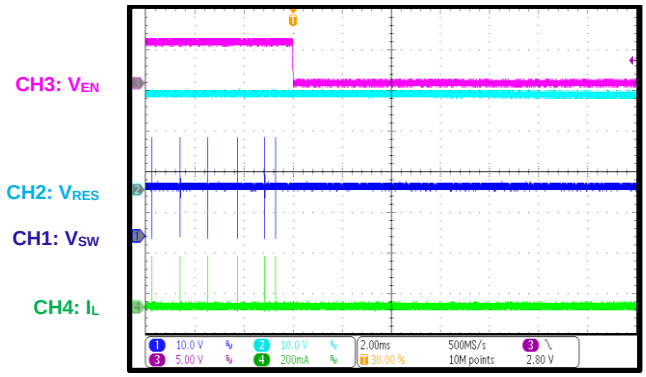
Shutdown through EN (for Internal Boost)

I_{OUT} = 0A



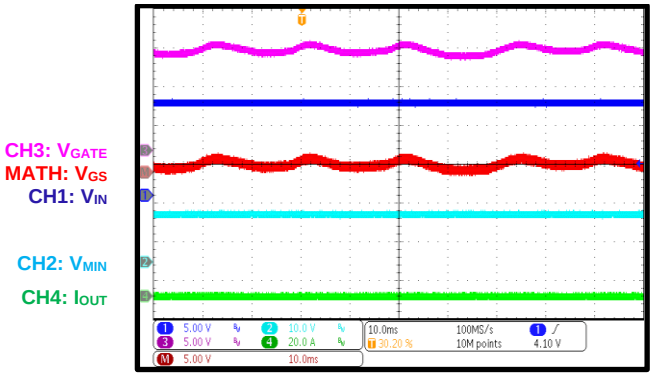
Shutdown through EN (for Internal Boost)

I_{OUT} = 20A



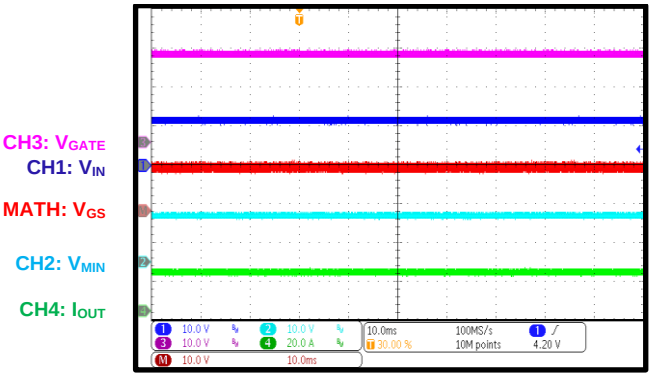
Steady State (for Smart Diode)

I_{OUT} = 0A



Steady State (for Smart Diode)

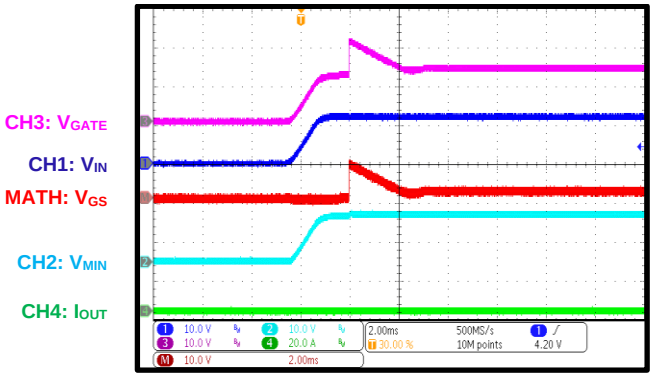
I_{OUT} = 20A



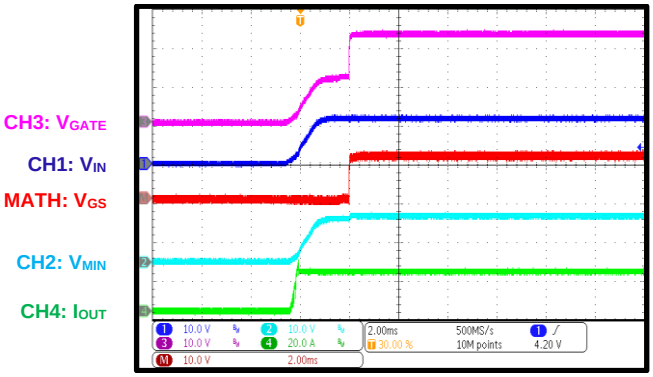
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 20A, L = 22µH, T_A = 25°C, unless otherwise noted.

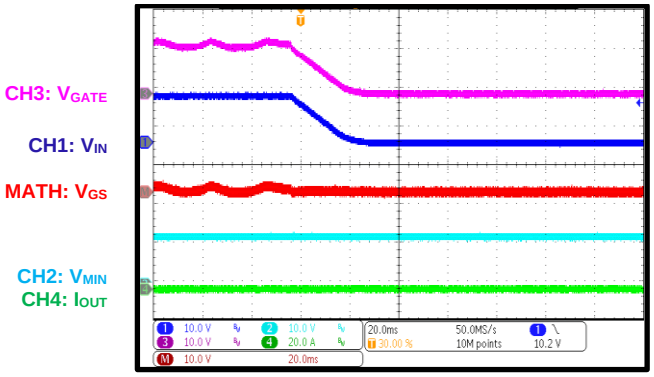
Start-Up through VIN
I_{OUT} = 0A



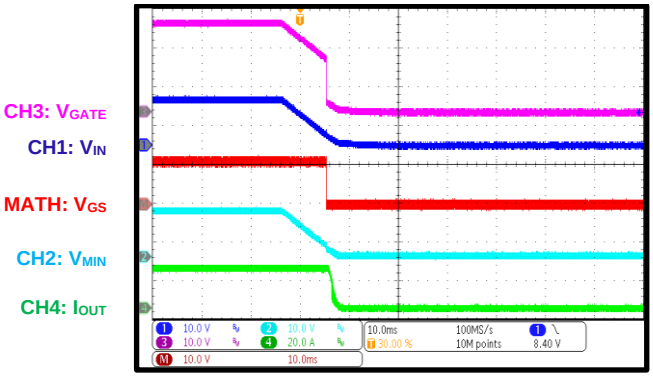
Start-Up through VIN
I_{OUT} = 20A



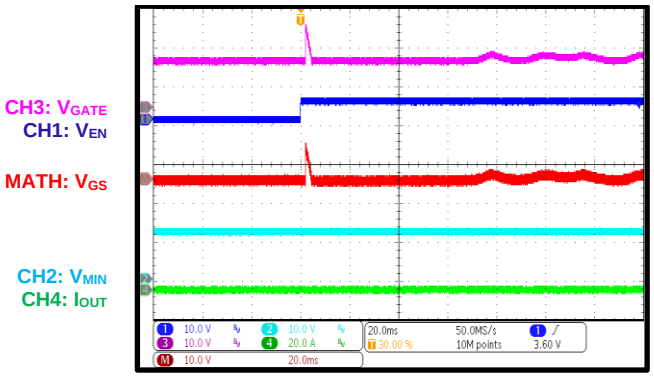
Shutdown through VIN
I_{OUT} = 0A



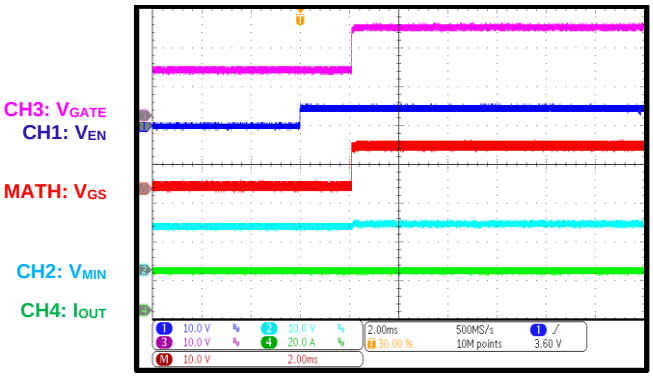
Shutdown through VIN
I_{OUT} = 20A



Start-Up through EN
I_{OUT} = 0A



Start-Up through EN
I_{OUT} = 20A

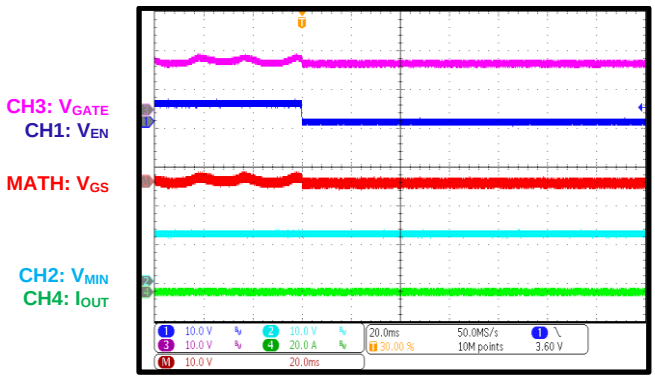


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 20A, L = 22µH, T_A = 25°C, unless otherwise noted.

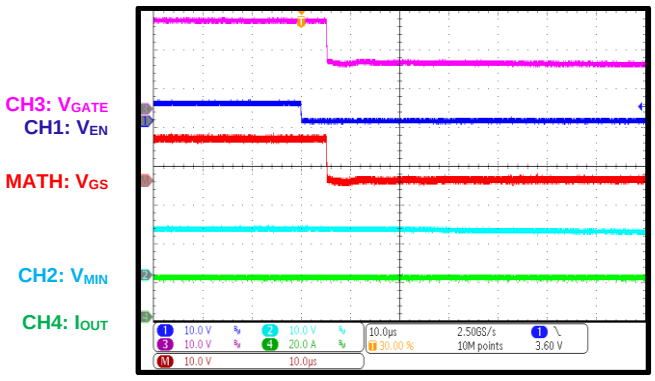
Shutdown through EN

I_{OUT} = 0A



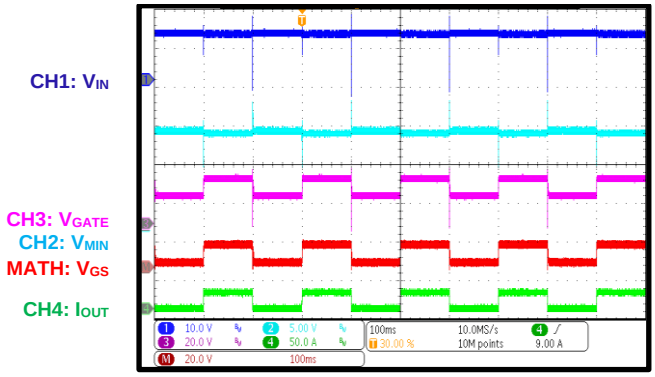
Shutdown through EN

I_{OUT} = 20A



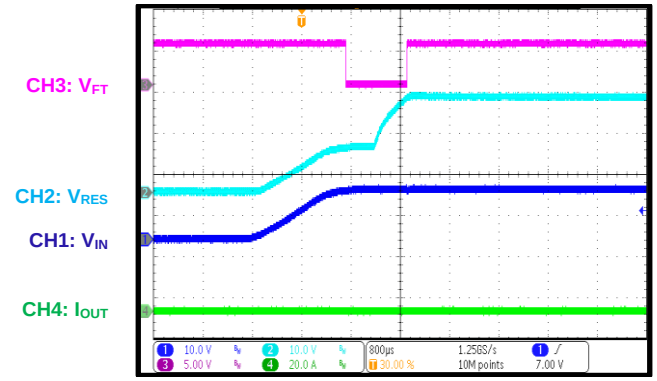
Load Transient

I_{OUT} = 0A to 20A



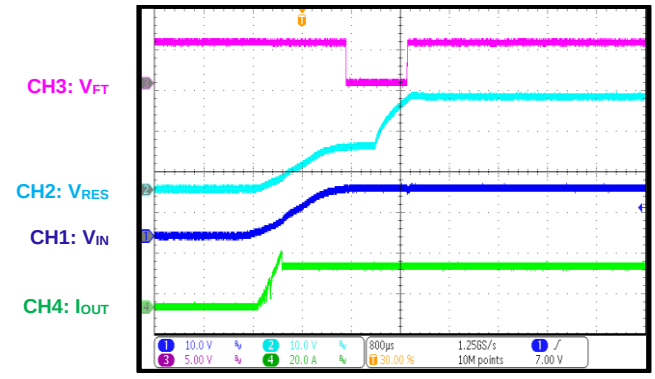
FT Start-Up through VIN

I_{OUT} = 0A



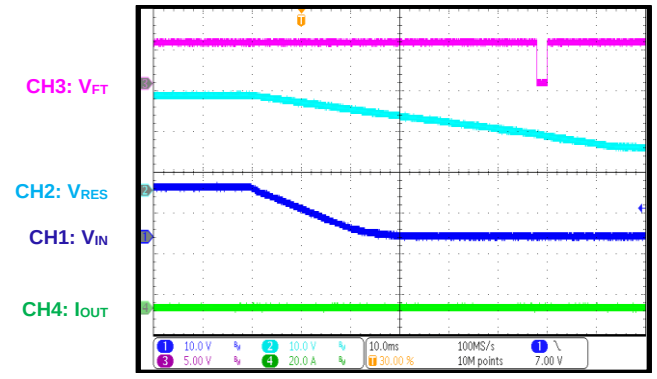
FT Start-Up through VIN

I_{OUT} = 20A



FT Shutdown through VIN

I_{OUT} = 0A

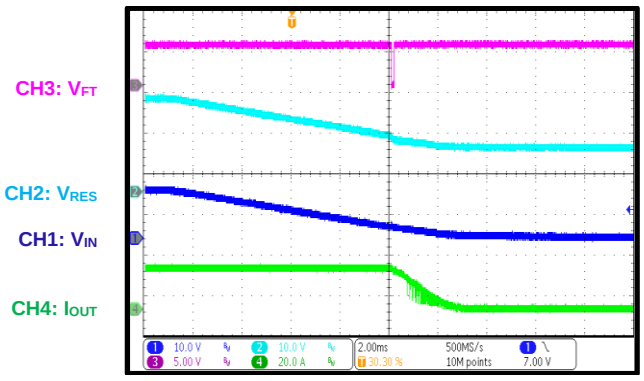


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 20A, L = 22µH, T_A = 25°C, unless otherwise noted.

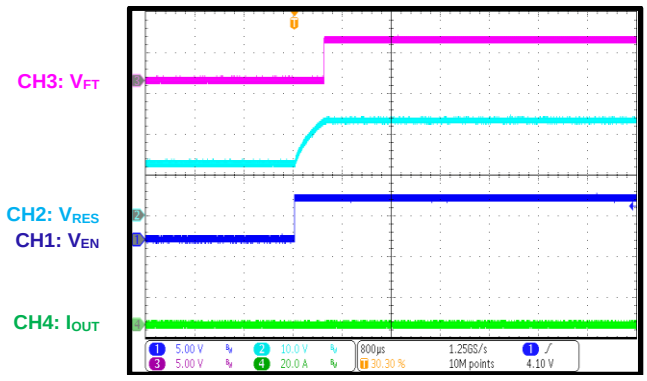
FT Shutdown through VIN

I_{OUT} = 20A



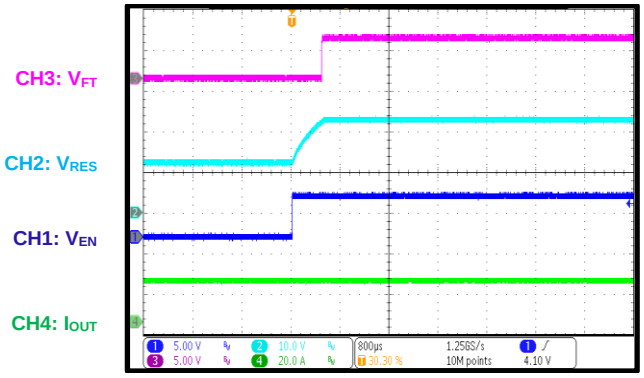
FT Start-Up through EN

I_{OUT} = 0A



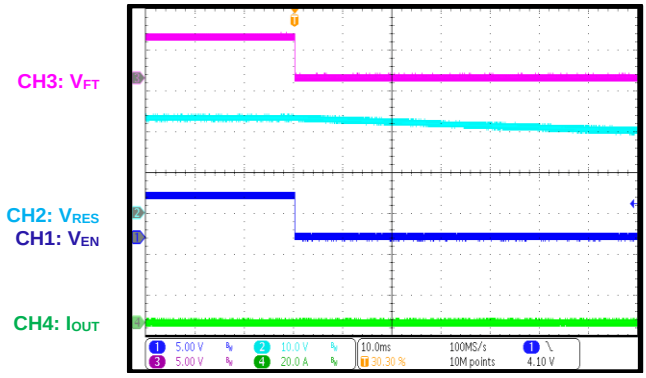
FT Start-Up through EN

I_{OUT} = 20A



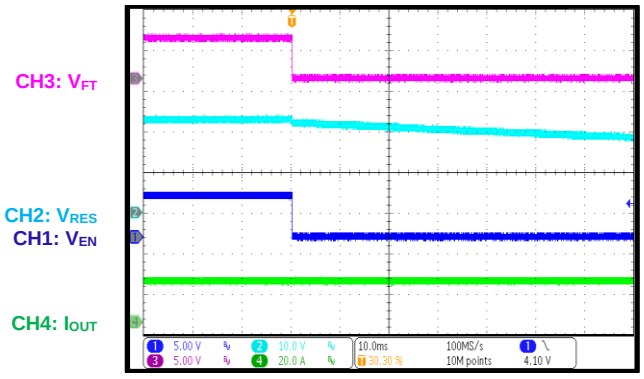
FT Shutdown through EN

I_{OUT} = 0A



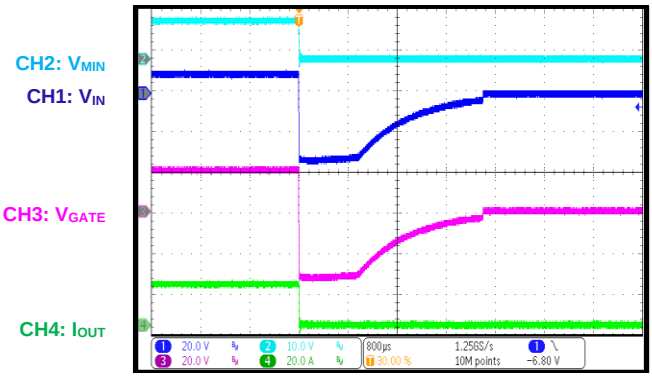
FT Shutdown through EN

I_{OUT} = 20A



Negative Pulse

I_{OUT} = 20A

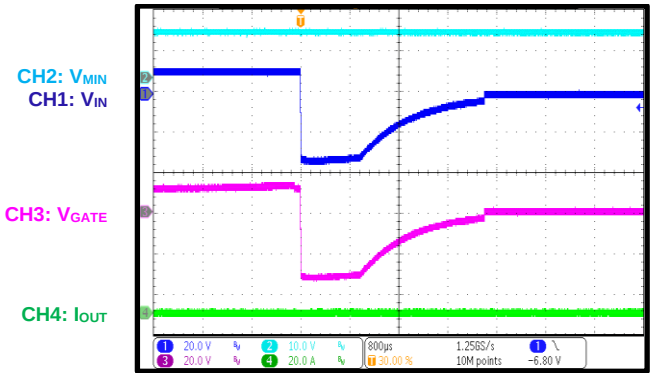


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 20A, L = 22µH, T_A = 25°C, unless otherwise noted.

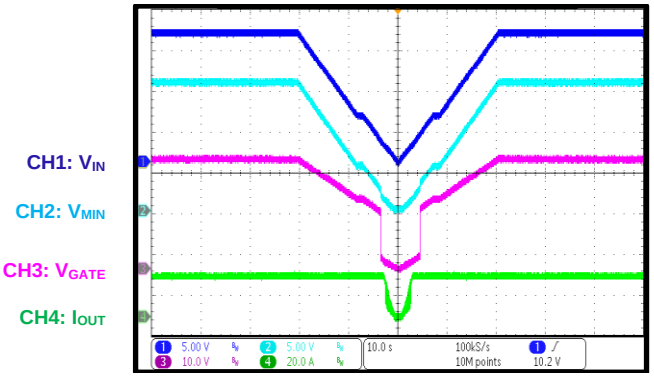
Negative Pulse

I_{OUT} = 0A



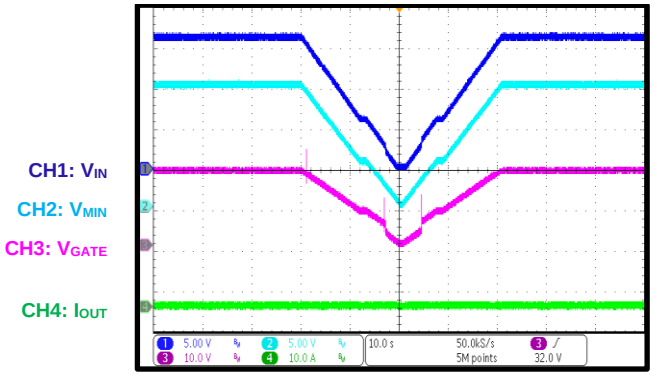
Supply Voltage Ramps Up and Down Slowly

I_{OUT} = 20A



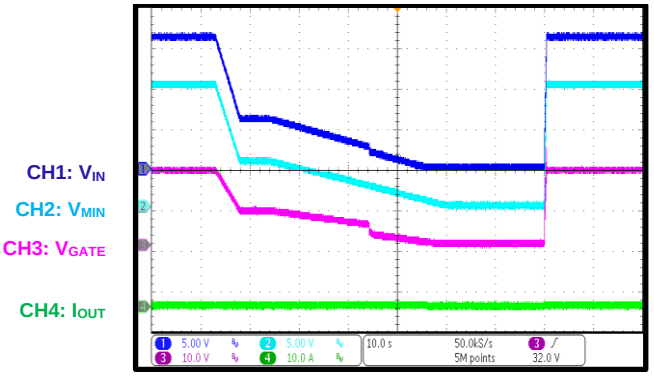
Supply Voltage Ramps Up and Down Slowly

I_{OUT} = 0A



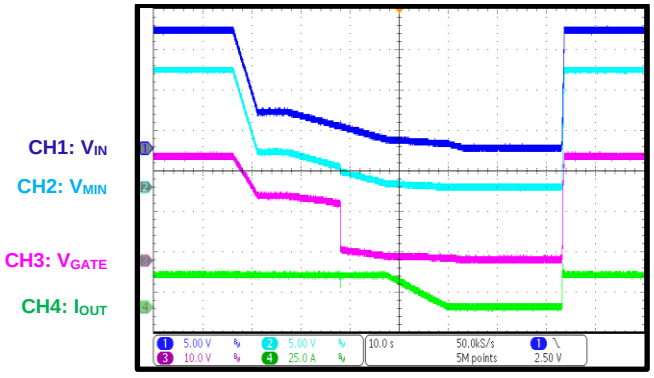
Supply Voltage Ramps Up Quickly and Ramps Down Slowly

I_{OUT} = 0A



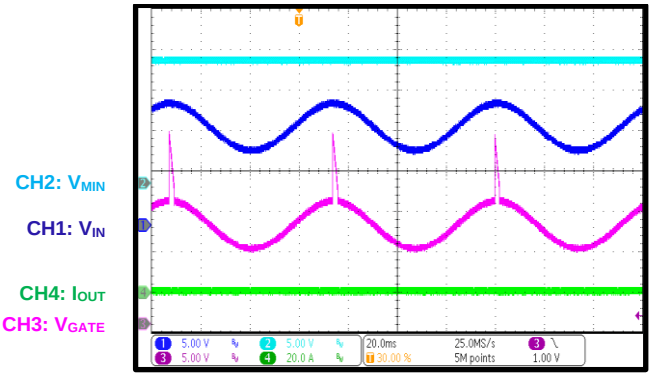
Supply Voltage Ramps Up Quickly and Ramps Down Slowly

I_{OUT} = 20A



Superimposed Alternating voltage

V_{PP} = 6V, f_{SW} = 15Hz, I_{OUT} = 0A

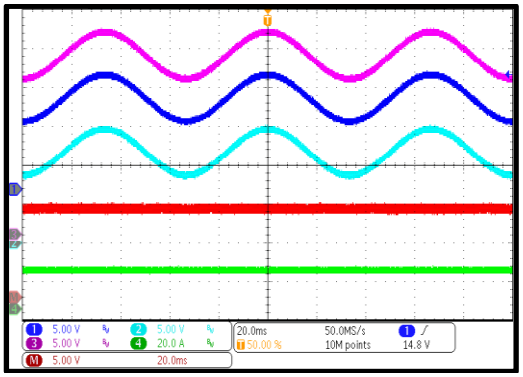


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 20A, L = 22µH, T_A = 25°C, unless otherwise noted.

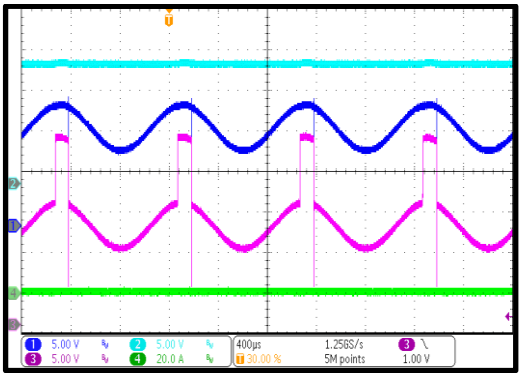
Superimposed Alternating Voltage

V_{PP} = 6V, f_{SW} = 15Hz, I_{OUT} = 20A



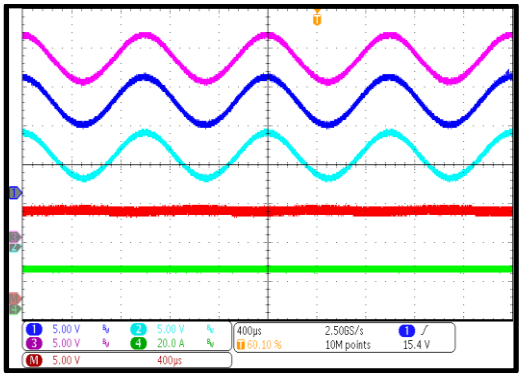
Superimposed Alternating Voltage

V_{PP} = 6V, f_{SW} = 1kHz, I_{OUT} = 0A



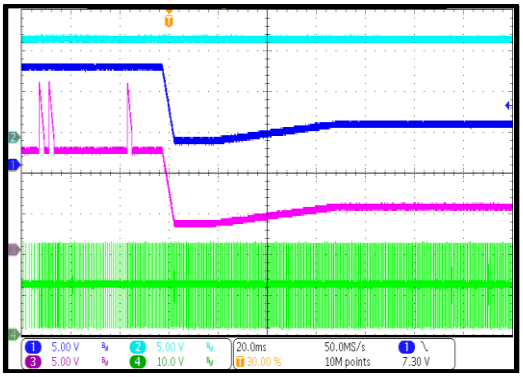
Superimposed Alternating Voltage

V_{PP} = 6V, f_{SW} = 1kHz, I_{OUT} = 20A



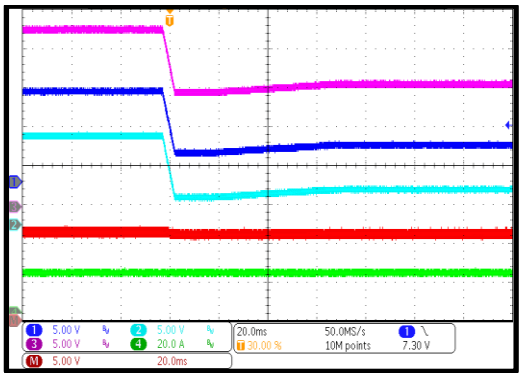
Cold Crank

I_{OUT} = 0A



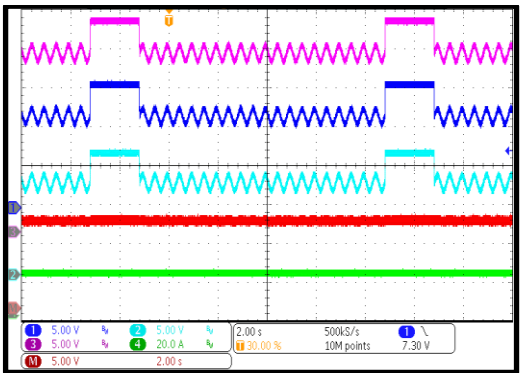
Cold Crank

I_{OUT} = 20A



Start Pulse

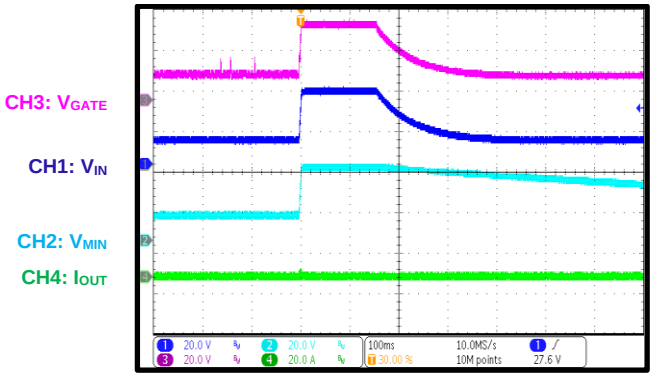
I_{OUT} = 20A



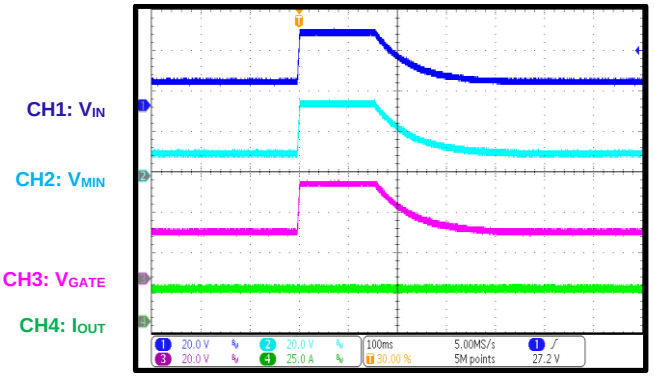
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 20A, L = 22µH, T_A = 25°C, unless otherwise noted.

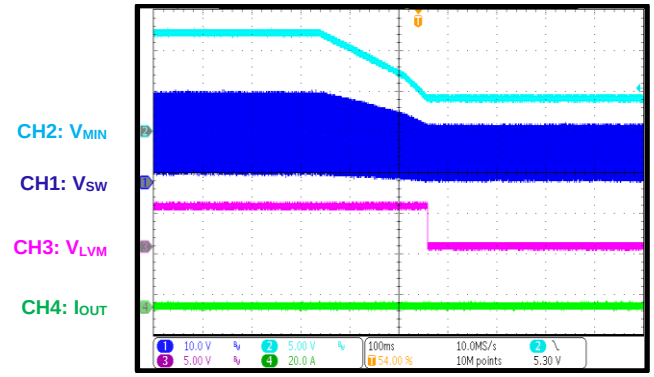
Load Dump
I_{OUT} = 0A



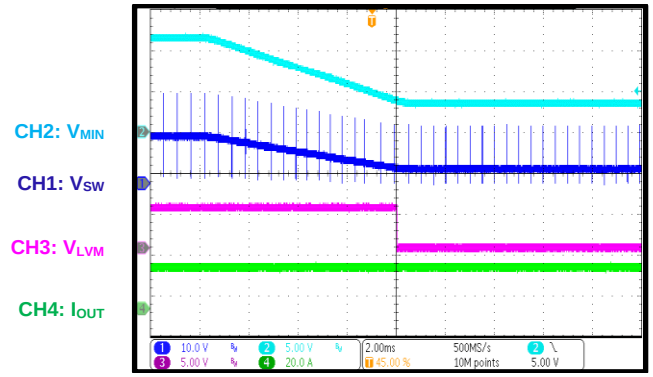
Load Dump
I_{OUT} = 20A



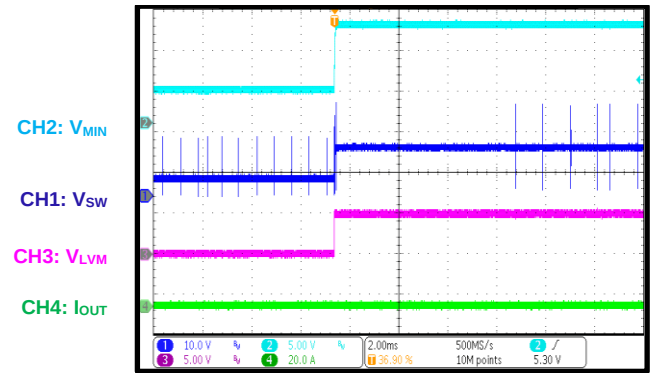
VMIN UV Entry
I_{OUT} = 0A



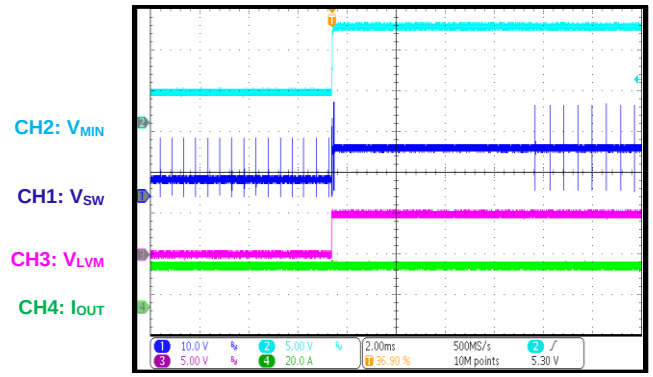
VMIN UV Entry
I_{OUT} = 20A



VMIN UV Recovery
I_{OUT} = 0A



VMIN UV Recovery
I_{OUT} = 20A

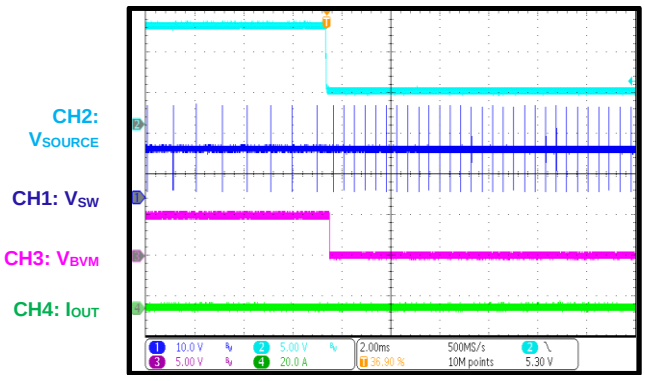


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 20A, L = 22µH, T_A = 25°C, unless otherwise noted.

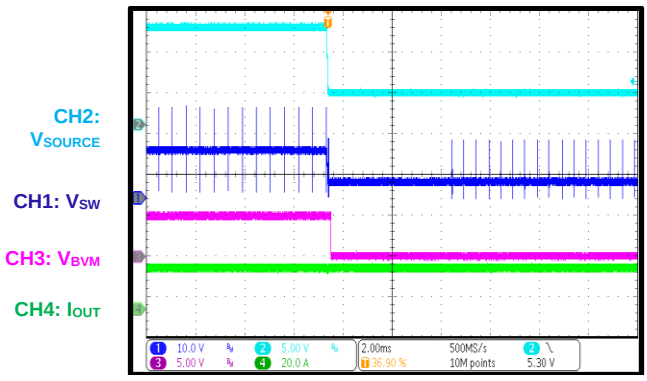
Source UV Entry

I_{OUT} = 0A



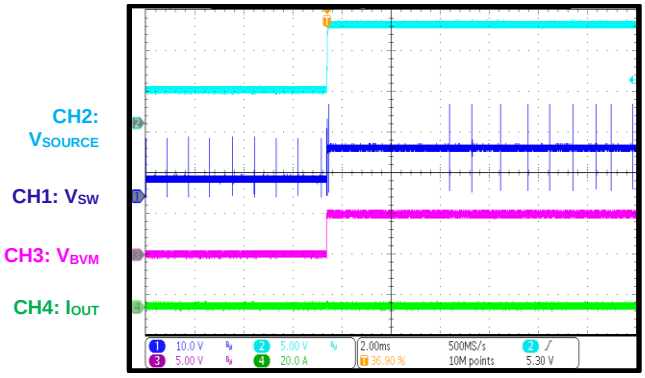
Source UV Entry

I_{OUT} = 20A



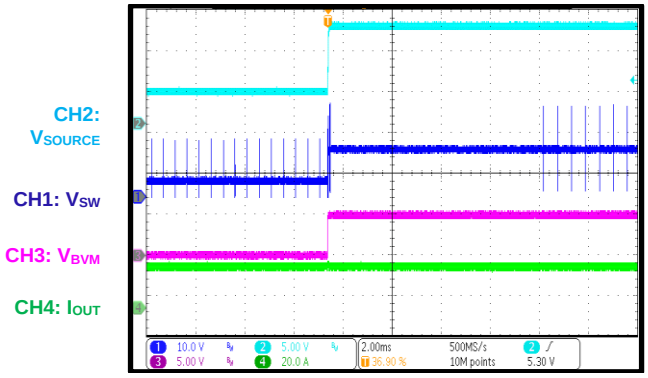
Source UV Recovery

I_{OUT} = 0A



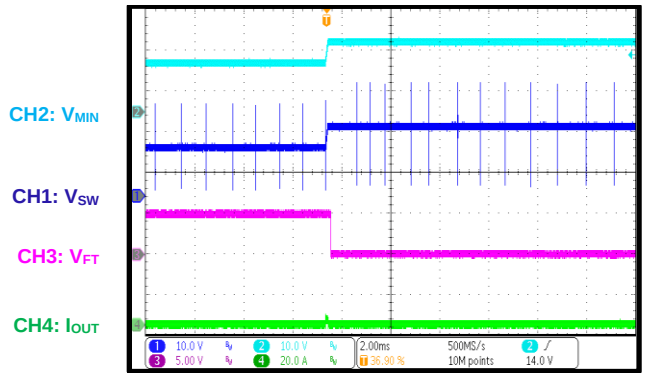
Source UV Recovery

I_{OUT} = 20A



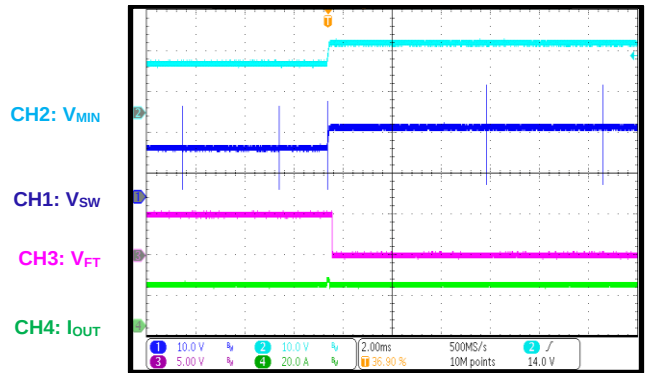
VMIN OV Entry

I_{OUT} = 0A



VMIN OV Entry

I_{OUT} = 20A

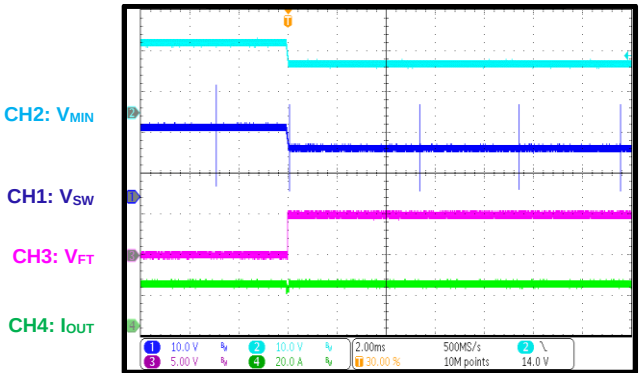


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 20A, L = 22µH, T_A = 25°C, unless otherwise noted.

VMIN OV Recovery

I_{OUT} = 20A



FUNCTIONAL BLOCK DIAGRAM

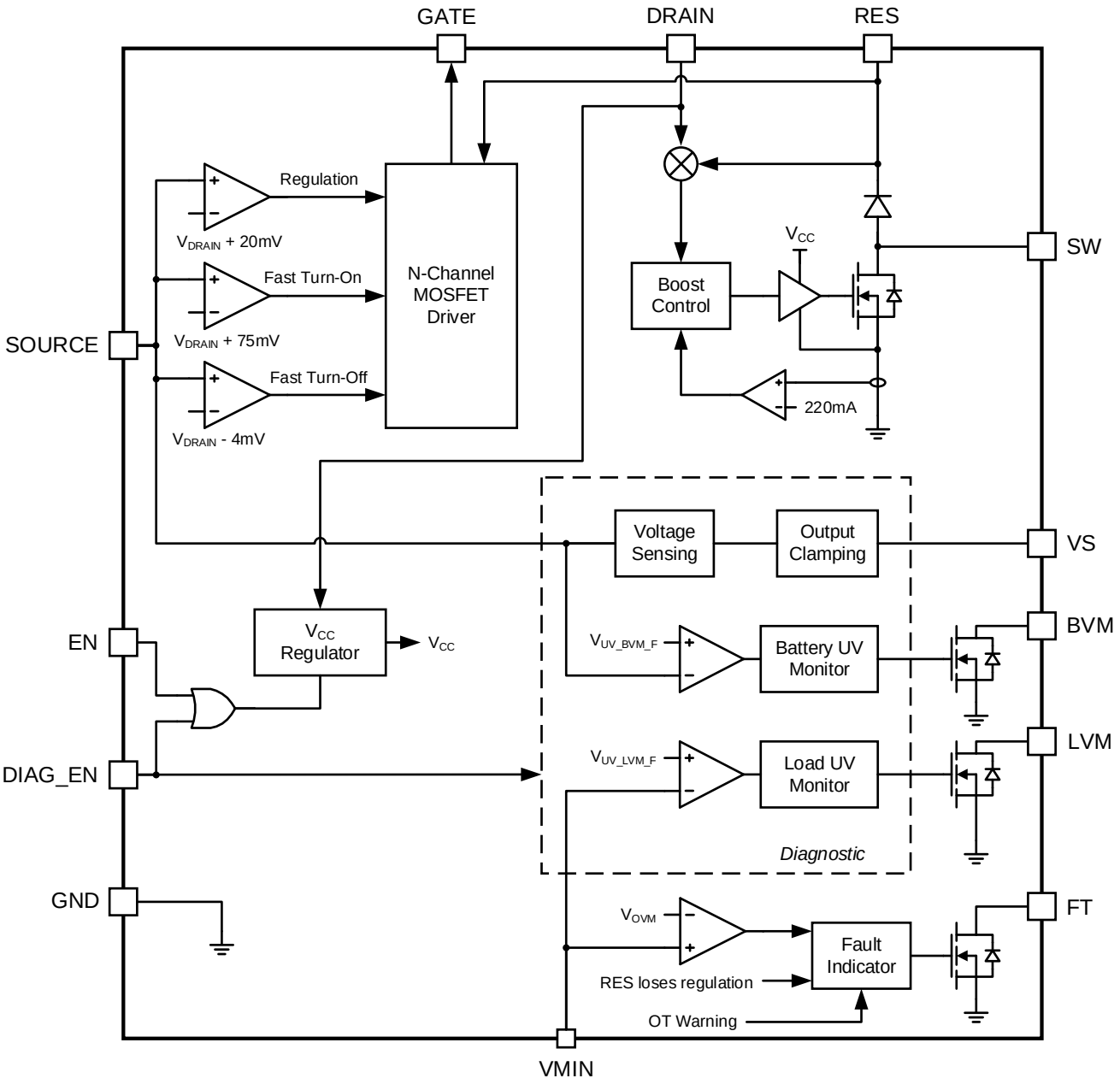


Figure 1: Functional Block Diagram

OPERATION

The MPQ5852 is a smart diode controller that provides reverse protection and various diagnostic functions. The device drives an external power N-channel MOSFET to minimize power loss, including DC forward loss and AC rectification loss.

The voltage monitors are defined for the system to take actions to protect the downstream loads during over-voltage (OV) or under-voltage (UV) conditions, such as load dump or cold crank.

Standby, Diagnostic, and Rectify Modes and Low-Voltage Operation

When the DRAIN pin voltage (V_{DRAIN}) is below the UV threshold, the MPQ5852 shuts down. In this off state, the gate is passively pulled to the SOURCE pin, and the boost converter is disabled. Once V_{DRAIN} exceeds the under-voltage lockout (UVLO) threshold (V_{DRUV_R}), the device enters standby state to wait for the EN or DIAG_EN pin to enter a logic high state. The standby current (I_{SBY}) is about 4μA.

Once the EN pin is pulled high, the boost converter starts to operate. When the voltage on the reservoir capacitor exceeds the reservoir UVLO rising threshold (V_{RES_R}), normal operation begins, the gate is actively modulated based on the SOURCE pin voltage (V_{SOURCE}) and V_{DRAIN}, and the FT pin is high when the SOURCE-to-DRAIN voltage is in regulation.

When the DIAG_EN pin is pulled high and the EN pin is still low, the diagnostic functions including voltage sensing and monitoring are enabled, while MOSFET rectification is not enabled. Table 1 shows the standby, diagnostic, and rectify modes of the MPQ5852.

Table 1: Standby, Diagnostic, and Rectify Modes (9)

Mode	EN	DIAG_EN	Boost	MOSFET	DIAG (10)
Standby	L	L	Off	Off	Off
Diag.	L	H	Off	Off	On
Rectify	H	L	On	On	Off
	H	H	On	On	On

Notes:

9) Where L indicates “low,” and H indicates “high.”
10) Where DIAG refers to the diagnostic features.

The DRAIN pin is the internal circuitry’s power supply . If V_{DRAIN} exceeds its UVLO threshold, the MPQ5852 operates normally, even when the input voltage (V_{IN}) drops to 0V under severe cold-crank conditions. A large electrolytic output capacitor is required under these conditions.

If V_{DRAIN} drops below the UVLO falling threshold (V_{DRUV_F}), the device does not pull the GATE pin down to the SOURCE pin until the voltage on the reservoir capacitor discharges below the reservoir UVLO falling threshold (V_{RES_F}). This allows the device to minimize forward voltage drops during temporary low-voltage transients, such as cold-crank conditions.

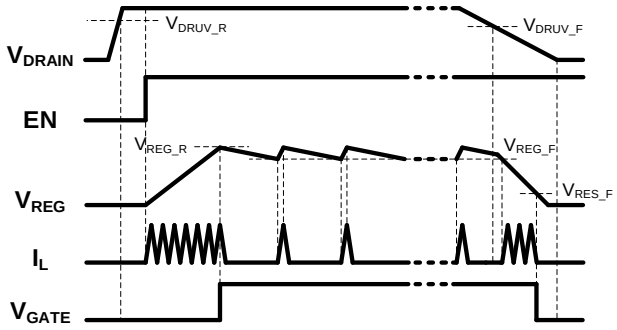


Figure 2: Start-Up and Low-Voltage Operation Timing Diagram

Smart Diode Operation

During normal operation, when V_{SOURCE} exceeds V_{DRAIN}, the MPQ5852 modulates the external N-channel MOSFET’s gate to regulate the SOURCE-to-DRAIN voltage to about 20mV. This minimizes power loss and allows small negative currents to be easily detected.

Generally, the SOURCE-to-DRAIN voltage is regulated to about 20mV. When the load current increases further, the GATE pin voltage (V_{GATE}) rises until the MOSFET is fully on. If the load current decreases, the GATE amplifier drives the MOSFET’s gate lower to maintain a 20mV drop.

If the SOURCE-to-DRAIN voltage exceeds 20mV, a large current modifies V_{GATE} to regulate the SOURCE-to-DRAIN voltage. If a negative current flows through the external N-channel MOSFET, the MPQ5852 detects a SOURCE-to-DRAIN negative voltage drop. If the drop exceeds -4mV, the device pulls down the GATE pin to quickly turn off the external N-channel MOSFET. If a forward current flows through the external N-channel MOSFET (either the body or channel), the MPQ5852 detects a SOURCE-to-

DRAIN forward voltage drop. If the drop exceeds 75mV, the MPQ5852 pulls the GATE pin up to quickly turn on the external N-channel MOSFET. This allows high-frequency AC waveforms (up to 50kHz) to be rectified with minimal power loss in the system and the external N-channel MOSFET. In addition, the MPQ5852 also meets the transients defined in ISO 7637-2 for 12V systems with an input TVS diode. If the SOURCE-to-DRAIN forward voltage drop exceeds 75mV for 20µs, the FT pin asserts low, which indicates an over-current (OC) condition. This configuration is masked by default.

Enable (EN) Input

The EN pin sets the enable/disable control for the MPQ5852. If the shutdown function is not used, do not float the EN pin, and connect a 100kΩ resister to the DRAIN pin. If the EN pin voltage (V_{EN}) exceeds the 1.2V rising threshold, the MPQ5852 starts up some internal circuits and the boost converter begins operation. If V_{EN} is below than its 1V falling threshold, the boost converter is disabled, and the device pulls the GATE pin down to turn off the external N-channel MOSFET.

Diagnosis Enable (DIAG_EN) Input

The DIAG_EN pin sets the enable/disable control for the diagnostics function. The diagnostic functions include battery voltage sensing, battery voltage UV monitor, and load voltage UV and OV monitor. If the DIAG_EN pin voltage (V_{DIAG_EN}) exceeds 1.2V, the MPQ5852's diagnostics features are enabled, and the results are reported via the BVM, LVM, and VS pins. If V_{DIAG_EN} is below its 1V falling threshold, the voltage sensing and monitor is disabled to reduce the quiescent current (I_Q). Connect this pin to the GND pin if not used.

Boost Converter

The integrated boost converter provides fixed peak current mode control. When the reservoir floating supply is below the reservoir regulation falling voltage (V_{REG_F}), the boost converter requests another turn-on pulse. This pulse terminates once the inductor current (I_L) reaches 220mA.

I_L must reach 0mA before the next turn-on cycle begins. This sets the maximum frequency (f_{MAX}), depending on V_{DRAIN} and the inductance (L). f_{MAX} can be calculated with Equation (1):

$$f_{MAX} = \frac{1}{t_{ON} + t_{OFF}} \quad (1)$$

Where t_{ON} is the on time, and t_{OFF} is the off time.

t_{ON} can be calculated with Equation (2):

$$t_{ON} = \frac{I_{BOOST} \times L}{V_{DRAIN} - R_{DS(ON)\_SW} \times \frac{I_{BOOST}}{2}} \quad (2)$$

Where I_{BOOST} is the boost peak current limit (typically 220mA), L is the external boost inductance, and $R_{DS(ON)\_SW}$ is the boost power MOSFET on resistance (typically 1.7Ω).

t_{OFF} can be calculated with Equation (3):

$$t_{OFF} = \frac{I_{BOOST} \times L}{V_{REG\_R} + V_{DIODE}} \quad (3)$$

Where V_{REG_R} is the reservoir regulation rising voltage, and V_{DIODE} is the boost rectifier diode's forward voltage (typically 0.9V).

Battery Voltage Sensing and Monitor

When the DIAG_EN pin is high, the MPQ5852's battery voltage is monitored, including UV detection and battery voltage sense.

When V_{SOURCE} is between 4V and 28V, the VS pin outputs a voltage (V_S) proportional to V_{SOURCE} based on the set VS sensing ratio (k_{VS}) divider. k_{VS} can be selected by the user based on Table 2. If V_{SOURCE} exceeds 28V, V_S is clamped to its OV clamping voltage (V_{CL_VS}) to indicate an OV status and protect the GPIO of the microcontroller unit (MCU). V_{CL_VS} can also be set by the user.

Table 2 shows the options for k_{VS} and V_{CL_VS}.

Table 2: Options for the VS Sensing Ratio and VS OV Clamping Voltage

Parameter	Option 1	Option 2	Option 3	Option 4
k_{VS}	1 / 10	1 / 13	1 / 18	1 / 27
V_{CL_VS}	3.1V	2.3V	1.65V	1.1V

When V_{SOURCE} is below its UV falling threshold ($V_{UV\_BVM\_F}$), the BVM pin asserts low to indicate the UV status after the BVM UV status reporting deglitch time (t_{BVM_DEG}). The pin remains low until V_{SOURCE} increases and exceeds the 10% hysteresis. The V_{SOURCE} UV threshold and UV report deglitch can be respectively selected by

the user based on Table 3 and Table 4.

Table 3 shows the options for $V_{UV\_BVM\_F}$.

Table 3: Options for the SOURCE UV Falling Threshold

Parameter	Option 1	Option 2	Option 3	Option 4
$V_{UV\_BVM\_F}$	4.4V	5.25V	7V	7.8V

Table 4 shows the options for t_{BVM_DEG}.

Table 4: Options for the BVM UV Status Reporting Deglitch Time

Parameter	Option 1	Option 2	Option 3	Option 4
t_{BVM_DEG}	125µs	250µs	500µs	1000µs

BVM is an open-drain pin. If the pin is used, pull BVM up to the external 3.3V or 5V supply via a 100kΩ resister. Figure 3 shows the battery voltage monitor timing diagram.

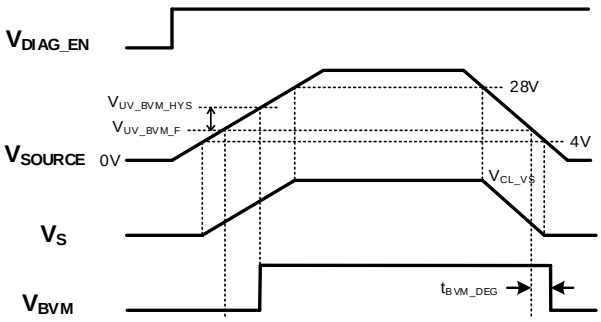


Figure 3: Battery Voltage Monitor Timing Diagram

Load Voltage Monitor

The MPQ5852's load is monitored, including over-voltage (OV) and under-voltage (UV) detection. The VMIN pin must be connected to the power rail to be monitored, where the power rail can be the downstream DC/DC converter. Connect VMIN to the DRAIN pin if this function is not used.

When the voltage on the VMIN pin (V_{MIN}) is below its UV falling threshold ($V_{UV\_LVM\_F}$), the LVM pin pulls low to report the UV status after the VMIN UV or OV status reporting deglitch time (t_{LVM_DEG}). The VMIN UV threshold and UV report deglitch can be selected by the user based on Table 5 and Table 6.

Table 5 shows the options for $V_{UV\_LVM\_F}$.

Table 5: Options for the VMIN UV Falling Threshold

Parameter	Option 1	Option 2	Option 3	Option 4
$V_{UV\_LVM\_F}$	2.6V	3.2V	3.9V	4.4V

Table 6 shows the options for t_{BVM_DEG} and t_{LVM_DEG}.

Table 6: Options for the BVM UV Status Reporting Deglitch Time and VMIN UV or OV Status Reporting Deglitch Time

Parameter	Option 1	Option 2	Option 3	Option 4
t_{BVM_DEG}	125µs	250µs	500µs	1000µs
t_{LVM_DEG}	140µs	250µs	500µs	1000µs

If V_{MIN} exceeds its OV rising threshold (V_{OVM}), the FT pin asserts low after t_{LVM_DEG} completes to report the OV status. The V_{MIN} OV threshold as well as the OV report deglitch time also can be set by the user based on Table 6 and Table 7.

Table 7: VMIN OV Rising Threshold

Parameter	Option 1	Option 2
V_{OVM}	16.5V	18.5V

LVM is an open-drain pin. If the pin is used, pull LVM up to an external 3.3V or 5V supply via a 100kΩ resister. Figure 4 shows the load voltage monitor timing diagram.

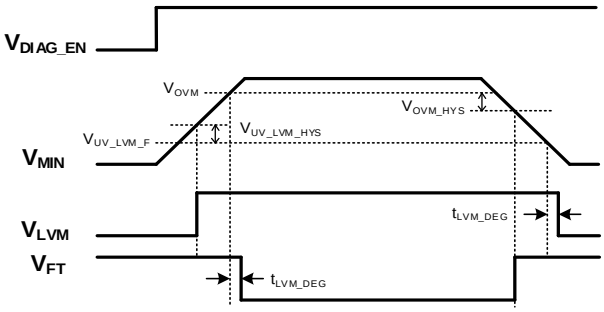


Figure 4: Load Voltage Monitor Timing Diagram

Voltage sensing and monitoring are defined for the system to take actions to protect downstream loads during OV or UV conditions, such as load dump or cold crank.

Fault Report

FT is an open-drain pin that is designed to indicate the MPQ5852's status. The FT pin asserts low if any of the below errors occurs:

1. The boost converter goes out of regulation.
2. A V_{MIN} OV fault is detected for longer than 140µs.
3. The device has a thermal warning.
4. The OC status lasts for longer than 20µs.

Once the fault is cleared, the FT pin recovers automatically, and an external pull-up resistor pulls up the FT pin voltage. For VMIN OV reporting and the VMIN OC function, the fault report function can be masked if not to be used for the user. The VMIN OC function is masked by default.

Transient Disturbances Tests

The MPQ5852 meets the requirements specified in the ISO 7637-2 and ISO 16750-2 standards, based on the application circuit (see Figure 8 on page 34). Table 8 shows the tests for ISO 7637-2 and ISO 16750-2.

Table 8: Tests in ISO 7637-2 and ISO 16750-2 (11)

Standard	Test Item	Level	Description (12)
7637-2	1	IV	-150V / 2ms / R_I = 10Ω
	2a	IV	112V / 50µs / R_I = 2Ω
	2b	IV	10V / R_{IN} = 0Ω
	3a	IV	-220V / 0.1µs / R_{IN} = 50Ω
	3b	IV	150V / 0.1µs / R_I = 50Ω
16750-2	Load dump, Test B	-	V_{US} = 42V t_R ≤ 5ms
	Superimposed alternating voltage	-	V_{US} = 16V f_R = 50Hz to 25kHz

Notes:

11) Considering the worst-case test condition, the device is tested without any additional filter capacitors connected to the SOURCE and DRAIN pins.

12) Where R_I is the internal resistance of the power source, R_{IN} is the input resistance, V_{US} is the source voltage, t_R is the load dump rising time, and f_R is the sinusoidal AC voltage frequency.

APPLICATION INFORMATION

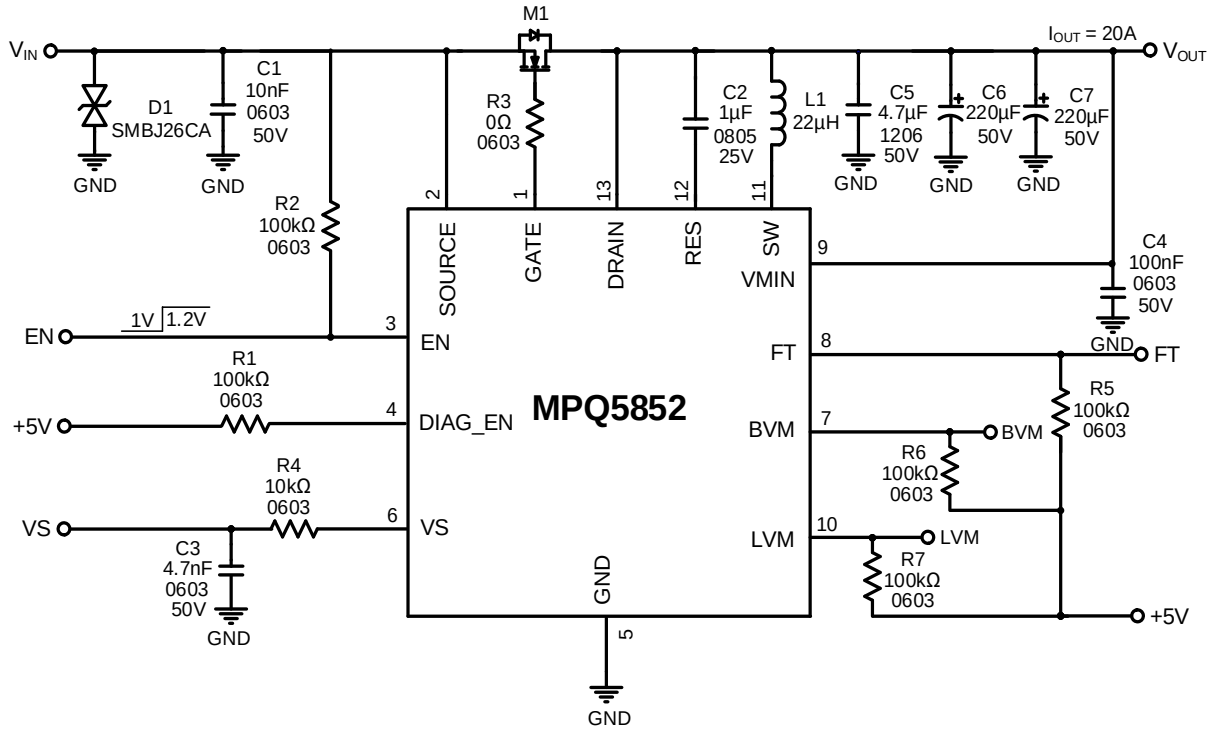


Figure 5: Typical Application Circuit (V_{IN} = V_{OUT} = 5V to 36V, I_{OUT} = 20A)

Table 9: Design Guide Index

Pin #	Pin Name	Component	Design Guide Index
1	GATE	R3, M1	Selecting the Power MOSFET (GATE, Pin 1)
2	SOURCE	D1, C1	Selecting the TVS Diode (VIN, Pin 2)
3	EN	R2	Enable Power Output (EN, Pin 3; DIAG_EN, Pin 4)
4	DIAG_EN	R1	Enable Power Output (EN, Pin 3; DIAG_EN, Pin 4)
5	GND	-	Ground Connection (GND, Pin 5)
6	VS	R4, C3	Voltage-Sense Output (VS, Pin 6)
7	BVM	R6	Selecting the BVM Resistor and Capacitor (BVM, Pin 7)
8	FT	R5	Fault Report (FT, Pin 8)
9	VMIN	C4, C5, C6, C7	Selecting the Electrolytic Capacitor and Ripple Voltage (VMIN, Pin 9)
10	LVM	R7	Selecting the LVM Resistor (LVM, Pin 10)
11	SW	L1	Selecting the Boost Inductor (SW, Pin 11)
12	RES	C2	Selecting the Reservoir Capacitor (RES, Pin 12)
13	DRAIN	-	Power MOSFET Drain Connection (DRAIN, Pin 13)

Selecting the Power MOSFET (GATE, Pin 1)

The power MOSFET must support the maximum steady current during forward operation, and withstand the worst-case battery transients during reverse blocking operation.

Steady-state power dissipation is based on the on resistance ($R_{DS(ON)}$) of the power MOSFET and the load current (I_{LOAD}). If the load is light (I_{LOAD} x $R_{DS(ON)}$ < V_{SD}), the forward drop is regulated to the SOURCE-to-DRAIN regulation voltage (V_{SD}, typically 20mV). The power loss ($P_{CONDUCTION}$) under light loads can be calculated with Equation (4):

$$P_{CONDUCTION} = V_{SD} \times I_{LOAD} \quad (4)$$

Under heavy loads, the MOSFET is fully enhanced, meaning power dissipation depends on the MOSFET's $R_{DS(ON)}$. $P_{CONDUCTION}$ under heavy loads can be estimated with Equation (5):

$$P_{CONDUCTION} = I_{LOAD}^2 \times R_{DS(ON)} \quad (5)$$

As the high-amplitude ripple on the input is rectified, a MOSFET with the smallest total gate charge (Q_{GTOT}) is required. A MOSFET with smaller Q_{GTOT} reduces reverse current during the turn-off delay and also lowers driver loss.

The operating MOSFET's drain-to-source voltage must be able to support the worst-case conditions, such as when there is a voltage step or the battery voltage goes from a positive to negative voltage. The worst-case condition occurs when the SOURCE pin voltage (V_{SOURCE}) is in reverse and the DRAIN pin voltage (V_{DRAIN}) is not discharged to low. The external N-channel MOSFET's drain-to-source voltage (V_{DSS}) must meet the condition calculated with Equation (6):

$$V_{DSS} \geq V_{DRAIN} + |V_{SOURCE}| \quad (6)$$

The gate-to-source voltage must be rated to a minimum of ±15V.

Selecting the TVS Diode (SOURCE, Pin 2)

The MPQ5852 can be damaged by the negative pulse on the SOURCE pin since V_{SOURCE} is limited to -40V. Connect a TVS diode between the SOURCE and GND pins to protect the part.

The SMBJ26CA is recommended, as it can protect the MPQ5852 from negative pulses and over-voltage (OV) conditions. It is recommended to add a 10nF capacitor on SOURCE.

Enable Power Output (EN, Pin 3; DIAG_EN, Pin 4)

EN and DIAG_EN are digital control pins that turn the external N-channel MOSFET (M1) on or off, and enable or disable the diagnostic features.

Pull EN above the rising threshold (1.2V) to enable the reverse blocking function and enable the internal boost. Pull EN below the falling threshold (1V) to disable the function.

Pull EN_DIAG above the rising threshold (1.2V) to enable the diagnostic features. Pull EN_DIAG below the falling threshold (1V) to disable diagnostics to reduce the standby current (I_{SBY}).

There is no internal pull-up or pull-down resistor connected to the EN or DIAG_EN pin, meaning do not float EN and DIAG_EN. An external pull-up or pull-down resistor is required if the control signal cannot provide an accurate high or low logic. A 100kΩ pull-up resistor is recommended.

Ground Connection (GND, Pin 5)

See the PCB Layout Guidelines section on page 33 for more details.

Voltage-Sense Output (VS, Pin 6)

It is recommended to add a 4.7nF capacitor and 10kΩ resistor to the VS pin to stabilize the output.

Selecting the BVM Resistor and Capacitor (BVM, Pin 7)

BVM is an open-drain pin and powered by an external supply. This pin monitors the battery voltage and asserts low to indicate an under-voltage (UV) status for the battery voltage. BVM is connected to GND internally with a 1kΩ resistor. The external BVM pull-up resistor is recommended to be 100kΩ.

The deglitch time of BVM and LVM (t_{BVM_DEG} and t_{LVM_DEG}, respectively) is typically set to the same level. However, if a longer t_{BVM_DEG} is required, an RC network can be added on BVM (see Figure 6 on page 31).

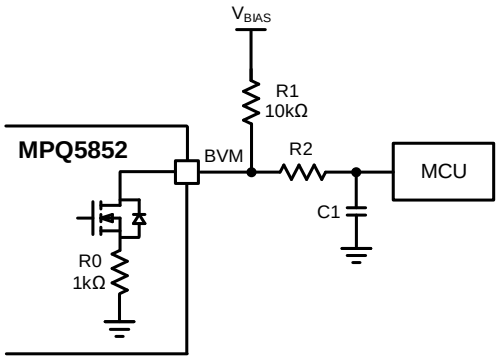


Figure 6: RC Network for BVM

Pulling up R1 affects the BVM output voltage low level (V_{BVM_LOW}), meaning R1 must meet the condition calculated with Equation (7):

$$R1 > \frac{R0 \times (V_{BIAS} - V_L)}{V_L} \quad (7)$$

Where V_{BIAS} is the external pull-up supply voltage, V_L is the microcontroller (MCU) logic low threshold, and R0 is the internal pull-down resistor (typically 1kΩ). It is recommended to set R1 to 10kΩ.

The final SOURCE UV report deglitch time (t_F) can be calculated with Equation (8):

$$t_F = t_{BVM\_DEG} + C1 \times (R0 + R2) \times \ln \frac{R1 \times V_{BIAS}}{V_L \times R1 - R0 \times V_{BIAS}} \quad (8)$$

The BVM rising time (t_R) can be calculated with Equation (9):

$$t_R = C1 \times (R1 + R2) \times \ln \frac{V_{BIAS}}{V_H} \quad (9)$$

Where V_H is the MCU logic high threshold, and R2 and C1 are part of the additional RC circuit.

For example, when V_{BIAS} is 5V, V_L is 0.8V, V_H is 2V, R1 is 10kΩ, and t_{BVM_DEG} is 250µs, by setting R2 to 1.65kΩ and C1 to100nF, t_F is 1000µs.

Fault Report (FT, Pin 8)

A 100kΩ FT pull-up resistor is recommended. The FT pin can monitor the status of the part.

Selecting the Electrolytic Capacitor and Ripple Voltage (VMIN, Pin 9)

During rectification, the electrolytic capacitance (C_{LOAD}) reduces the load's ripple voltage. The load ripple voltage (V_R) is determined by C_{LOAD}, the source ripple frequency, the ripple amplitude, and I_{LOAD}.

V_R decreases with the source ripple frequency, and the relationship between C_{LOAD} and I_{LOAD} can be calculated with Equation (10):

$$C_{LOAD} \geqslant \frac{4 \times V_{AC} - V_R}{4 \times V_{AC} \times f_{RIPPLE} \times V_R} \times I_{LOAD} \quad (10)$$

Where V_{AC} is the SOURCE voltage ripple amplitude (in V), f_{RIPPLE} is the ripple frequency (in Hz), C_{LOAD} is the electrolytic capacitance (in F), and I_{LOAD} is the load current (in A).

To maintain V_R below 2V, f_{RIPPLE} is 5kHz, V_{AC} is 3V (6V V_{PP}, where V_{PP} is the peak-to-peak rectification voltage), and I_{LOAD} is 5A, then C_{LOAD} is 417µF.

Selecting the LVM Resistor (LVM, Pin 10)

The LVM pin provides the load voltage status report. The LVM pull-up resistance is recommended to be 100kΩ. If LVM is powered by an external 5V supply, the pin monitors the load voltage and asserts low to indicate the UV status of the load voltage.

If a longer t_{LVM_DEG} is required, an RC delay network can be added on the LVM pin, similar to BVM. The internal pull-down resistance is also 1kΩ.

Selecting the Boost Inductor (SW, Pin 11)

The inductance (L) affects the driver's maximum current capability. There is a blanking time (t_{BLANK}) in the boost converter, and the inductor current (I_L) is not detected during t_{BLANK}. To ensure that I_L does not exceed 220mA during t_{BLANK}, L must meet the condition estimated with Equation (11):

$$L > \frac{V_{DRAIN} \times t_{BLANK}}{I_{BOOST}} \quad (11)$$

Where V_{DRAIN} is the DRAIN pin voltage (in V), and I_{BOOST} is the integrated boost converter's current limit (typically 220mA).

To select the required inductor for high-voltage applications, if V_{DRAIN} is 36V and the ambient temperature (T_A) is at 25°C, the inductor must exceed 17µH. Consider the derating of the inductance at different temperatures and currents. It is recommended to select a minimum 22µH inductor with a saturation current exceeding 220mA and an RMS current exceeding 100mA. Small-chip inductors (e.g. the LQH2MPZ220MGRL) are recommended.

Selecting the Reservoir Capacitor (RES, Pin 12)

A large capacitor can be used to support the IC if V_{DRAIN} is below its UVLO falling threshold (V_{DRUV_F}). The minimum reservoir capacitor (C_{RES_MIN}) can be calculated with Equation (12):

$$C_{RES\_MIN} \geqslant \frac{I_{GATE} \times (t_S - t_{ON})}{V_{REG\_UVLO\_HYS}} \quad (12)$$

Where I_{GATE} is the real-time current follow to M1 (in mA), $V_{REG\_UVLO\_HYS}$ is the reservoir regulation UVLO hysteresis (typically 0.1V), t_S is the boost period, and t_{ON} is the on time estimated with Equation (2) on page 26. It is recommended to use a minimum 1µF capacitor with a 25V or higher rating between the RES and DRAIN pins.

Power MOSFET Drain Connection (DRAIN, Pin 13)

See the PCB Layout Guidelines section on page 33 for more details.

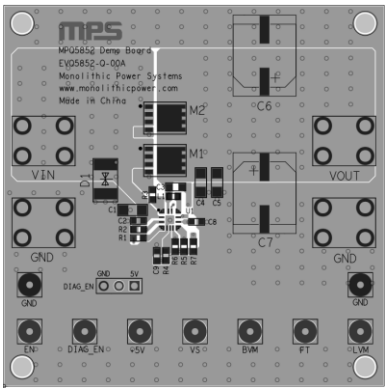
PCB Layout Guidelines (13)

An optimized PCB layout is critical for proper operation. A four-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 7 and follow the guidelines below:

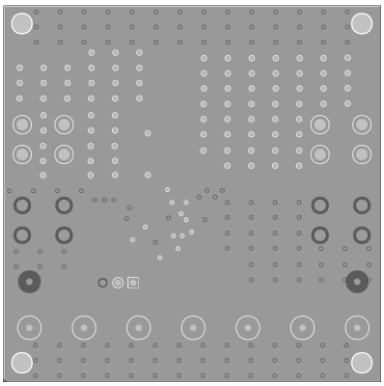
1. Place the SW pin close to the device using short, direct, and wide traces.
2. Use large copper areas to minimize conduction loss and thermal stress.
3. Place the ceramic input capacitors as close to the SOURCE and GND pins as possible to minimize high-frequency noise.
4. Route SW away from sensitive analog areas.
5. Use multiple vias to connect the power planes to the internal layer.

Note:

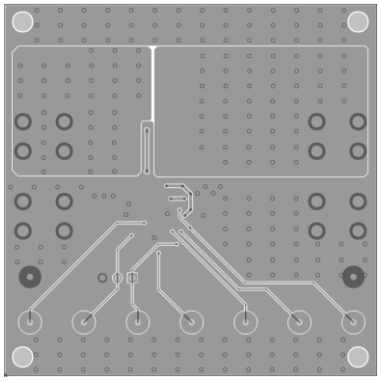
13) The recommended PCB layout is based on Figure 8 on page 34.



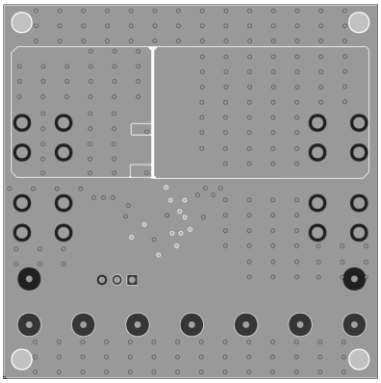
Top Silk and Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer and Bottom Silk

Figure 7: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

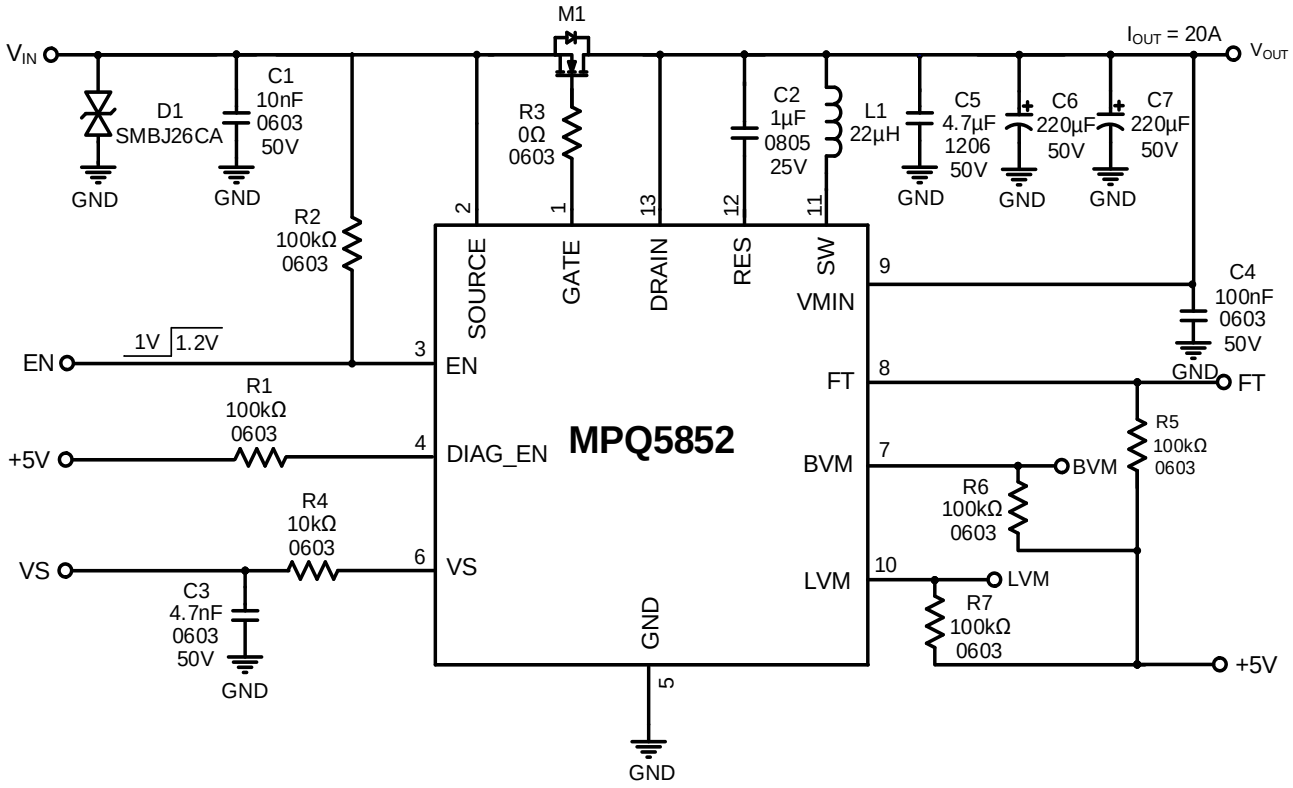


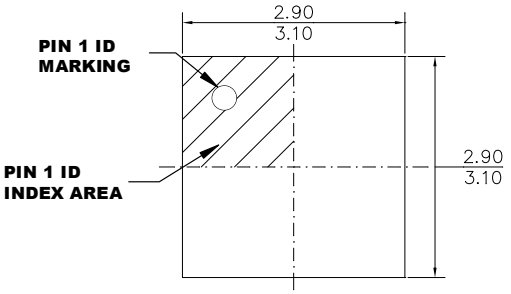
Figure 8: Typical Application Circuit (12V Automotive Battery with a 20A Load) (14) (15) (16)

Notes:

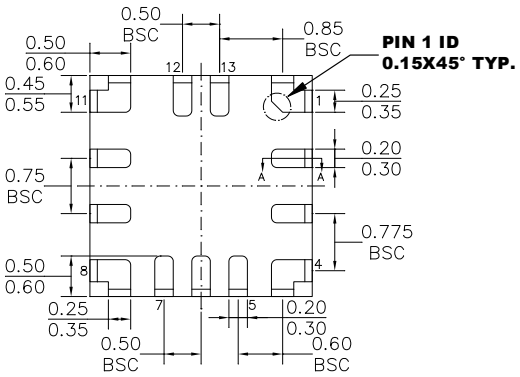
14) To support the short interruption function, remove R2 and add a 3.3V external supply to the EN terminal.
15) If the user needs to test a load dump exceeding 36V, change D1 to a suitable TVS diode for the specific application.
16) To support a constant input voltage (V_{IN}) exceeding 26V, it is recommended to remove the input TVS diode (D1).

PACKAGE INFORMATION

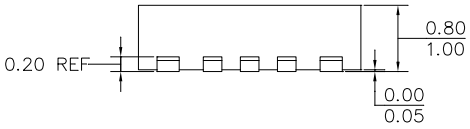
QFN-13 (3mmx3mm)
Wettable Flanks



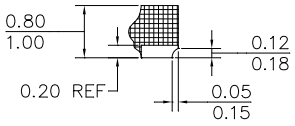
TOP VIEW



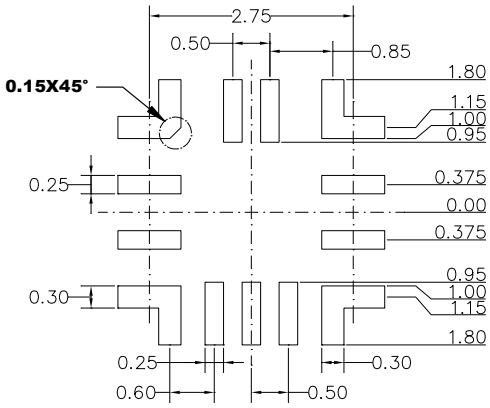
BOTTOM VIEW



SIDE VIEW



SECTION A-A

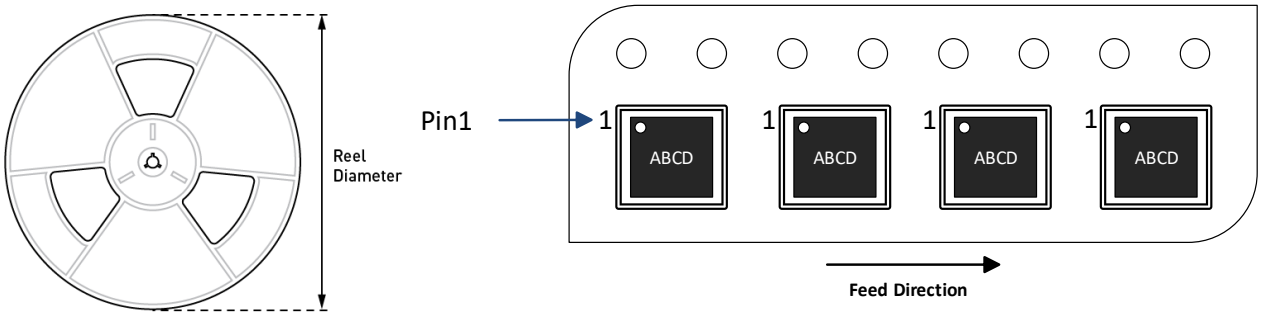


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ5852GQE-xxxx-AEC1-Z	QFN-13 (3mmx3mm)	5000	NA	NA	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/4/2025	Initial Release	-