MPQ70240FS

MPSafe™, 18V, 4-Channel PMIC with 3 Bucks and 1 LDO, ASIL-B Rated, AEC-Q100 Qualified

DESCRIPTION

The MPQ70240FS is a power management IC (PMIC) solution integrating three high-efficiency step-down DC/DC converters and a low-noise low-dropout (LDO) regulator. Its dual-stage, 18V buck architecture maximizes efficiency for the 1.8V image sensor I/O rail in the complementary metal oxide semiconductor (CMOS) sensor in high-resolution camera modules.

Constant-on-time (COT) control with phase-locked loop (PLL) provides fast transient response. During continuous conduction mode (CCM), the fixed 2.2MHz switching frequency (f_{SW}) greatly reduces external inductor and capacitor sizes.

The digital interface allows for application flexibility. The output voltage (V_{OUT}), power sequence, and protection thresholds can all be adjusted via the interface. Fault statuses can also be monitored. under-voltage lockout (UVLO), over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and thermal shutdown. The one-time programmable (OTP) memory is provided to preset such functions.

The MPQ70240FS supports applications with a high automotive safety integrity level up to ASIL-B. Functional safety features include analog built-in self-testing (ABIST), diagnostics, and a power good (PG) output pin. The MPQ70240FS is developed under MPS's advanced MPSafe™ functional safety product development process, which has been independently certified to meet ISO26262 guidelines.

The MPQ70240FS minimizes the external components count, and is available in a space-saving QFN-15 (2.5mmx3.5mm) package with wettable flanks. It is available in AEC-Q100 Grade 1.

FEATURES

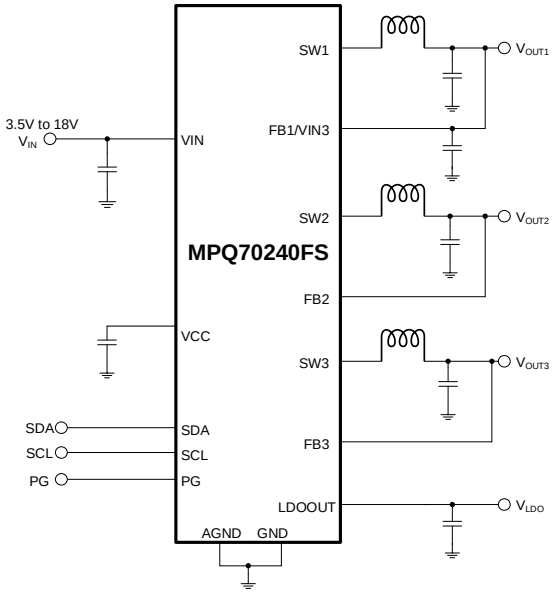
- Optimized for Automotive Cameras
  - Buck 1: 600mA with 3.5V to 18V Input
  - Buck 2: 600mA with 3.5V to 18V Input
  - Buck 3: 1A with 2.5V to 4V Input
  - Low-Dropout (LDO) Regulator: 200mA for Large CMOS Sensors
- Optimized for EMC/EMI Reduction
  - 2.2MHz Fixed Switching Frequency (f_{SW})
  - Stepped Triangle Spread Spectrum On/Off Function
  - Symmetric Input Capacitor (C_{IN}) for Reduced EMI
  - CISPR25 Class 5 Compliant
  - MeshConnect™ Flip-Chip Package
- Additional Features
  - Selectable Discontinuous Conduction Mode (DCM) and Forced Continuous Conduction Mode (FCCM)
  - Over-Current Protection (OCP) with Valley-Current Detection and Hiccup Mode
  - Power Good (PG) Output
  - Digital Interface Compliant Interface with Packet Error Checking (PEC)
  - Available in a QFN-15 (2.5mmx3.5mm) Package
  - Available in a Wettable Flank Package
  - Available in AEC-Q100 Grade 1
- Functional Safety
  - Hardware Capable to ASIL-B
  - Integrated Analog Built-In Self-Testing (ABIST) and Reference Monitor
  - Failure Modes Effects and Diagnostic Analysis (FMEDA)
  - Safety Manual

MPSafe™ Developed for Functional Safety Applications: ISO26262 Compliant

APPLICATIONS

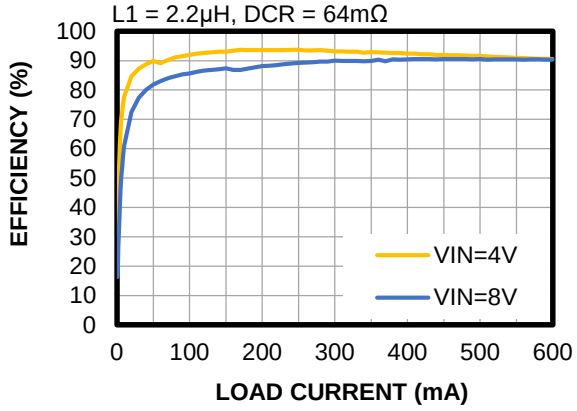
- Automotive Camera Modules
- Space-Constrained Applications

TYPICAL APPLICATION



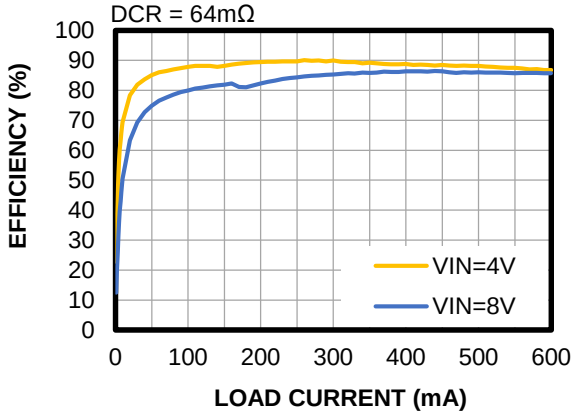
Efficiency vs. Load Current (Buck 1)

V_{OUT1} = 3V, f_{SW1} = 2.2MHz, DCM, other channels are disabled, L1 = 2.2µH, DCR = 64mΩ



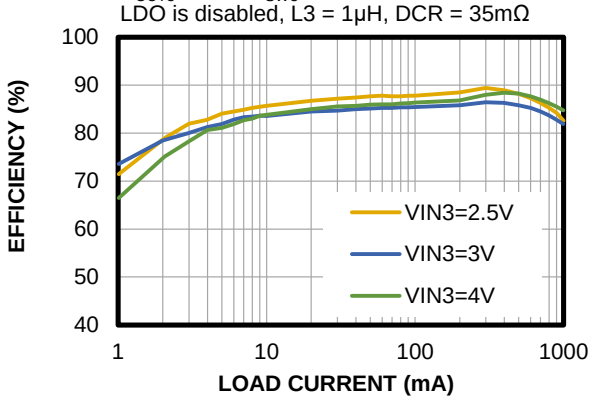
Efficiency vs. Load Current (Buck 2)

V_{OUT2} = 1.8V, f_{SW2} = 2.2MHz, DCM, other channels are disabled, L2 = 2.2µH, DCR = 64mΩ



Efficiency vs. Load Current (Buck 3)

V_{OUT3} = 1.2V, f_{SW3} = 2.2MHz, DCM, LDO is disabled, L3 = 1µH, DCR = 35mΩ



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating***
MPQ70240FSGRHE-xxxxAEC1**, ****	QFN-15 (2.5mmx3.5mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ70240FSGRHE-xxxxAEC1-Z).

** "xxxx" is the configuration code identifier for the register settings stored in the OTP register. The first "x" must be a number between 0 and 9, while the last three can be a hexadecimal value between 0 and F. The default code is "0000". Contact an MPS FAE to create this unique number.

*** Moisture Sensitivity Level Rating

****Wettable flank

TOP MARKING

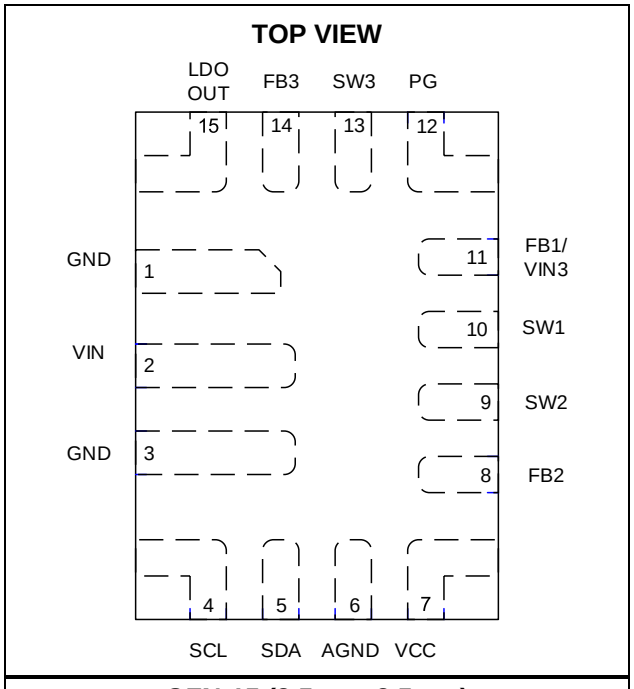
BQP

YWW

LLL

BQP: Production code of MPQ70240FS
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



QFN-15 (2.5mmx3.5mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 3	GND	**Power ground.** The two GND pins are connected inside. These pins should be electrically connected to the system power ground plane with the shortest and lowest-impedance connection possible.
2	VIN	**Input supply voltage.** The VIN pin supplies power to all the internal control circuitry and the power MOSFET connected to SW1 and SW2. A decoupling capacitor to ground is recommended to be placed close to VIN to minimize switching spikes
4	SCL	**Digital interface clock pin.** Use an external pull-up resistor to connect SCL to the external supply rail. Connect SCL ground if not used.
5	SDA	**Digital interface data pin.** Use an external pull-up resistor to connect SDA to the external supply rail. Connect SDA to ground if not used.
6	AGND	**Analog ground.** AGND is the reference GND for the internal logic and signal circuit. AGND is internally connected to GND. AGND should be connected to GND in the PCB layout design.
7	VCC	**Biased supply.** The VCC pin supplies power to the internal control circuitry and gate drivers. Place a decoupling capacitor from VCC to ground. Place this capacitor as close to VCC as possible.
8	FB2	**Buck 2 feedback.** Connect the FB2 pin directly to the buck 2 output. See the VOUT_COMMAND (21h) section on page 53 for V_{OUT2} setting.
9	SW2	**Buck 2 switch node.** The SW2 pin is the output of the internal power MOSFET. Connect SW2 to an external inductor using a wide PCB trace.
10	SW1	**Buck 1 switch node.** The SW1 pin is the output of the internal power MOSFET. Connect SW1 to an external inductor using a wide PCB trace.
11	FB1/VIN3	**Buck 1 feedback, buck 3 power source, and LDO power source.** Connect the FB1/VIN3 pin directly to the buck 1 output. See the VOUT_COMMAND (21h) section on page 44 for V_{OUT1} setting. To minimize switching spikes, place a decoupling capacitor from FB1/VIN3 to ground. Place this capacitor as close to FB1/VIN3 as possible.
12	PG	**Power good output.** The output of PG is push-pull. The high output level can be configured to either 3.3V or 1.8V. Float PG if not used.
13	SW3	**Buck 3 switch node.** The SW3 pin is the output of the internal power MOSFET. Connect SW3 to an external inductor using a wide PCB trace.
14	FB3	**Buck 3 feedback.** Connect the FB3 pin directly to the buck 3 output. See the VOUT_COMMAND (21h) section on page 56 for V_{OUT3} setting.
15	LDOOUT	**LDO output pin.** See the VOUT_COMMAND (21h) section on page 59 for the LDO output voltage (V_{LDOOUT}) setting. A 2.2µF ceramic capacitor is recommended for the LDO output.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN}..... -0.3V to +21V
V_{SW1}, V_{SW2}....-0.6V (-5V for <10ns) to V_{IN} + 0.3V
All other pins..... -0.3V to +6.25V
Continuous power dissipation (T_A = 25°C) (2) (6)
QFN-15 (2.5mmx3.5mm)..... 5.95W
Junction temperature (T_J) .....150°C
Lead temperature..... .....260°C
Storage temperature..... -40°C to +150°C

ESD Ratings

Human body model (HBM).....Class 2 (3)
Charged-device model (CDM).....Class C2b (4)

Recommended Operating Conditions

Input voltage (V_{IN}).....3.5V to 18V
Buck 1 output voltage (V_{OUT1}).....2.5V to 4V
Buck 2 output voltage (V_{OUT2}).....0.6V to 3.75V
Buck 3 output voltage (V_{OUT3}).....0.6V to 2.55V
LDO output voltage (V_{LDOOUT}).....0.6V to 3.75V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-15 (2.5mmx3.5mm)		
JESD51-7 (5)	51	5 °C/W
EVQ70240FS-RH-00A (6)	21	1.7 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The value of θ_{JC} shows the thermal resistance from junction-to-case bottom.
6) Measured on the MPS standard EVB for the MPQ70240FS: a 6.35cmx6.35cm, 2oz copper, 4-Layer PCB. The value of θ_{JC} shows the thermal resistance from junction-to-case top.

ELECTRICAL CHARACTERISTICS

V_{IN} = 8V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage						
VIN quiescent current	I_Q	Disable all channels via the digital interface		1	2	mA
Input voltage (V_{IN}) under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$		2.5	2.8	3.1	V
V_{IN} UVLO Hysteresis	$V_{IN\_UVLO\_HYS}$			150		mV
V_{IN} starting level	V_{IN_START}	VIN_START[1:0] = 01	3.7	4	4.3	V
		VIN_START[1:0] = 10	4.7	5	5.3	V
		VIN_START[1:0] = 11	5.7	6	6.3	V
V_{IN} stopping level	V_{IN_STOP}	VIN_STOP[1:0] = 01	3.2	3.5	3.8	V
		VIN_STOP[1:0] = 10	4.2	4.5	4.8	V
		VIN_STOP[1:0] = 11	5.2	5.5	5.8	V
VCC regulation voltage	V_{CC}	C_{VCC} = 4.7µF	4.85	5	5.15	V
V_{CC} UVLO rising threshold	$V_{CC\_UVLO\_RISING}$		2.4	2.6	2.8	V
V_{CC} UVLO hysteresis	V_{CC_HYS}			200		mV
Oscillator						
Switching frequency	f_{SW}	FREQUENCY[0] = 0	1.9	2.2	2.5	MHz
		FREQUENCY[0] = 1	2.9	3.3	3.7	MHz
Minimum on time (7)	t_{ON_MIN}			48		ns
Minimum off time (7)	t_{OFF_MIN}			40		ns
Buck 1						
Buck 1 output voltage (V_{OUT1}) Accuracy	V_{OUT1_ACC}	T_J = 25°C	-1		+1	%
			-1.5		+1.5	%
Buck 1 high-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS\_BUCK1}$			280	500	mΩ
Buck 1 low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS\_BUCK1}$			150	250	mΩ
SW1 HS-FET leakage current	$I_{LEAK\_HS\_BUCK1}$			0.01	1.5	µA
SW1 LS-FET leakage current	$I_{LEAK\_LS\_BUCK1}$			12.5	25	µA
SW1 peak current limit (I_{LIMIT})	$I_{LIM0\_HS\_BUCK1}$	ILIM[0] = 0	800	1000	1250	mA
		ILIM[0] = 1	1000	1250	1650	mA
SW1 valley I_{LIMIT}	I_{VALLEY_BUCK1}	ILIM[0] = 0	650	850	1100	mA
		ILIM[0] = 1	800	1100	1400	mA
SW1 zero-current detection (ZCD) current	I_{ZCD_BUCK1}		-20	+50	+150	mA
SW1 reverse I_{LIMIT}	I_{REV_BUCK1}		600			mA
V_{OUT1} feedback leakage	I_{FB_BUCK1}	V_{OUT1} = 4V, buck 3 and LDO are disabled		35	80	µA
V_{OUT1} output discharge	I_{DIS_BUCK1}	V_{OUT1} = 0.3V	2			mA
Buck 1 soft-start time (7) (8)	t_{SS_BUCK1}		0.5		2.25	ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 8V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Buck 2						
Buck 2 output voltage (V_{OUT2}) accuracy	V_{OUT2_ACC}	V_{OUT2} ≥ 1.25V, T_J = 25°C	-1		+1	%
		V_{OUT2} ≥ 1.25V	-1.5		+1.5	%
		V_{OUT2} < 1.25V, T_J = 25°C	-1.5		+1.5	%
		V_{OUT2} < 1.25V	-2		+2	%
Buck 2 HS-FET on resistance	$R_{DS(ON)\_HS\_BUCK2}$			280	500	mΩ
Buck 2 LS-FET on resistance	$R_{DS(ON)\_LS\_BUCK2}$			150	250	mΩ
SW2 HS-FET leakage current	$I_{LEAK\_HS\_BUCK2}$			0.01	1.5	µA
SW2 LS-FET leakage current	$I_{LEAK\_LS\_BUCK2}$			10	25	µA
SW2 peak I_{LIMIT}	$I_{LIM0\_HS\_BUCK2}$	ILIM[0] = 0	800	1000	1250	mA
		ILIM[0] = 1	1000	1250	1650	mA
SW2 valley I_{LIMIT}	I_{VALLEY_BUCK2}	ILIM[0] = 0	650	850	1100	mA
		ILIM[0] = 1	800	1100	1400	mA
SW2 ZCD current	I_{ZCD_BUCK2}		-20	+50	+150	mA
SW2 Reverse I_{LIMIT}	I_{REV_BUCK2}		600			mA
V_{OUT2} feedback leakage	I_{FB_BUCK2}	V_{OUT2} = 4V		30	45	µA
V_{OUT2} output discharge	I_{DIS_BUCK2}	V_{OUT2} = 0.3V	2			mA
Buck 2 soft-start time (7) (8)	t_{SS_BUCK2}		0.5		2.25	ms
Buck 2 power good (PG) over-voltage protection (OVP) rising threshold (9)	$V_{PG\_OVP0\_RISING\_BUCK2}$	PG_THRESHOLD[0] = 0, V_{OUT2} = 1.8V	102	104	106	% of V_{OUT}
	$V_{PG\_OVP1\_RISING\_BUCK2}$	PG_THRESHOLD[0] = 1, V_{OUT2} = 1.8V	104	106	108	% of V_{OUT}
Buck 2 PG OVP falling threshold (9)	$V_{PG\_OVP0\_FALLING\_BUCK2}$	PG_THRESHOLD[0] = 0, V_{OUT2} = 1.8V	101.4	103.4	105.4	% of V_{OUT}
	$V_{PG\_OVP1\_FALLING\_BUCK2}$	PG_THRESHOLD[0] = 1, V_{OUT2} = 1.8V	103.4	105.4	107.4	% of V_{OUT}
Buck 2 PG OVP hysteresis (9)	$V_{PG\_OVP\_HYS\_BUCK2}$			0.6		% of V_{OUT}
Buck 2 PG under-voltage protection (UVP) rising threshold (9)	$V_{PG\_UVP0\_RISING\_BUCK2}$	PG_THRESHOLD[0] = 0, V_{OUT2} = 1.8V	95.1	97.1	99.1	% of V_{OUT}
	$V_{PG\_UVP1\_RISING\_BUCK2}$	PG_THRESHOLD[0] = 1, V_{OUT2} = 1.8V	92.6	94.6	96.6	% of V_{OUT}
Buck 2 PG UVP falling threshold (9)	$V_{PG\_UVP0\_FALLING\_BUCK2}$	PG_THRESHOLD[0] = 0, V_{OUT2} = 1.8V	94.5	96.5	98.5	% of V_{OUT}
	$V_{PG\_UVP1\_FALLING\_BUCK2}$	PG_THRESHOLD[0] = 1, V_{OUT2} = 1.8V	92	94	96	% of V_{OUT}
Buck 2 PG UVP hysteresis (9)	$V_{PG\_UVP\_HYS\_BUCK2}$			0.6		% of V_{OUT}

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 8V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Buck 3						
Buck 3 output voltage (V_{OUT3}) accuracy	V_{OUT3_ACC}	V_{OUT3} ≥ 1.25V, T_J = 25°C	-1		+1	%
		V_{OUT3} ≥ 1.25V	-1.5		+1.5	%
		V_{OUT3} < 1.25V, T_J = 25°C	-1.5		+1.5	%
		V_{OUT3} < 1.25V	-2		+2	%
Buck 3 HS-FET on resistance	$R_{DS(ON)\_HS\_BUCK3}$	V_{OUT1} = 4V		115	215	mΩ
Buck 3 LS-FET on resistance	$R_{DS(ON)\_LS\_BUCK3}$	V_{OUT1} = 4V		50	120	mΩ
SW3 HS-FET leakage current	$I_{LEAK\_HS\_BUCK3}$			0.01	80	µA
SW3 LS-FET leakage current	$I_{LEAK\_LS\_BUCK3}$			0.01	10	µA
SW3 peak I_{LIMIT}	$I_{LIM0\_HS\_BUCK3}$	ILIM[0] = 0	1.4	1.65	1.9	A
		ILIM[0] = 1	1.7	2.1	2.5	A
SW3 valley I_{LIMIT}	I_{VALLEY_BUCK3}		1.2	1.7	2.2	A
SW3 ZCD current	I_{ZCD_BUCK3}		-50	+60	+200	mA
SW3 reverse I_{LIMIT}	I_{REV_BUCK3}		0.6			A
V_{OUT3} feedback leakage	I_{FB_BUCK3}	V_{OUT3} = 2.7V		30	50	µA
V_{OUT3} output discharge	I_{DIS_BUCK3}	V_{OUT3} = 0.3V	2			mA
Buck 3 soft-start time (7) (8)	t_{SS_BUCK3}		0.5		2.25	ms
Buck 3 PG OVP rising threshold (9)	$V_{PG\_OVP0\_RISING\_BUCK3}$	PG_THRESHOLD[0] = 0, V_{OUT3} = 1.2V	102	104	106	% of V_{OUT}
	$V_{PG\_OVP1\_RISING\_BUCK3}$	PG_THRESHOLD[0] = 1, V_{OUT3} =1.2V	104	106	108	% of V_{OUT}
Buck 3 PG OVP falling threshold (9)	$V_{PG\_OVP0\_FALLING\_BUCK3}$	PG_THRESHOLD[0] = 0, V_{OUT3} = 1.2V	101.3	103.3	105.3	% of V_{OUT}
	$V_{PG\_OVP1\_FALLING\_BUCK3}$	PG_THRESHOLD[0] = 1, V_{OUT3} = 1.2V	103.3	105.3	107.3	% of V_{OUT}
Buck 3 PG OVP hysteresis (9)	$V_{PG\_OVP\_HYS\_BUCK3}$			0.7		% of V_{OUT}
Buck 3 PG UVP rising threshold (9)	$V_{PG\_UVP0\_RISING\_BUCK3}$	PG_THRESHOLD[0] = 0, V_{OUT3} = 1.2V	95.1	97.1	99.1	% of V_{OUT}
	$V_{PG\_UVP1\_RISING\_BUCK3}$	PG_THRESHOLD[0] = 1, V_{OUT3} = 1.2V	92.7	94.7	96.7	% of V_{OUT}
Buck 3 PG UVP falling threshold (9)	$V_{PG\_UVP0\_FALLING\_BUCK3}$	PG_THRESHOLD[0] = 0, V_{OUT3} = 1.2V	94.4	96.4	98.4	% of V_{OUT}
	$V_{PG\_UVP1\_FALLING\_BUCK3}$	PG_THRESHOLD[0] = 1, V_{OUT3} = 1.2V	92	94	96	% of V_{OUT}
Buck 3 PG UVP hysteresis (9)	$V_{PG\_UVP\_HYS\_BUCK3}$			0.7		% of V_{OUT}

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 8V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Low-Dropout (LDO) Output						
LDO accuracy	V_{OUT4_ACC}	V_{OUT4} ≥ 1.25V, T_J = 25°C	-1		+1	%
		V_{OUT4} ≥ 1.25V	-1.5		+1.5	%
		V_{OUT4} < 1.25V, T_J = 25°C	-1.5		+1.5	%
		V_{OUT4} < 1.25V	-2		+2	%
LDO power supply rejection ratio (PSRR) (7)	L_{DO_PSRR}	No input capacitor, C_{OUT} = 22µF, f = 2MHz, I_{LDO} = 100mA		50		dB
LDO dropout voltage	V_{DROP_LDO}	V_{IN3} = 3.2V, setting LDO output = 3.3V, I_{LDO} = 200mA		100	220	mV
LDO I_{LIMIT}	I_{LIMIT_LDO}	V_{IN3} = 3V, setting LDO output = 2.5V	280			mA
LDO output discharge	I_{DIS_LDO}	V_{LDO} = 0.3V	2			mA
LDO soft-start time	t_{SS_LDO}	V_{OUT} = 10% to 90%, C_{OUT} = 4.7µF, V_{OUT} = 2.5V	50	130	200	µs
LDO line regulation	$L_{DO\_LINE\_REG}$	V_{IN3} = 2.7V to 4V		0.02	0.1	% / V
LDO load regulation	$L_{DO\_LOAD\_REG}$	V_{IN3} = 3.3V, I_{OUT} from 10mA to 200mA		0.03	0.15	%
LDO noise (7)	V_{LDO_NOISE}	V_{IN3} = 3.7V, V_{LDO} = 3.3V, I_{LDO} = 200mA, buck 1 is not switching, buck 3 and buck 2 are disabled		105		µVrms
LDO PG OVP rising threshold (9)	$V_{PG\_OVP0\_RISING\_LDO}$	PG_THRESHOLD[0] = 0, V_{LDO} = 2.5V	102	104	106	% of V_{OUT}
	$V_{PG\_OVP1\_RISING\_LDO}$	PG_THRESHOLD[0] = 1, V_{LDO} = 2.5V	104	106	108	% of V_{OUT}
LDO PG OVP falling threshold (9)	$V_{PG\_OVP0\_FALLING\_LDO}$	PG_THRESHOLD[0] = 0, V_{LDO} = 2.5V	101.4	103.4	105.4	% of V_{OUT}
	$V_{PG\_OVP1\_FALLING\_LDO}$	PG_THRESHOLD[0] = 1, V_{LDO} = 2.5V	103.4	105.4	107.4	% of V_{OUT}
LDO PG OVP hysteresis (9)	$V_{PG\_OVP\_HYS\_LDO}$			0.6		% of V_{OUT}
LDO PG UVP rising threshold (9)	$V_{PG\_UVP0\_RISING\_LDO}$	PG_THRESHOLD[0] = 0, V_{LDO} = 2.5V	94.6	96.6	98.6	% of V_{OUT}
	$V_{PG\_UVP1\_RISING\_LDO}$	PG_THRESHOLD[0] = 1, V_{LDO} = 2.5V	92.6	94.6	96.6	% of V_{OUT}
LDO PG UVP falling threshold (9)	$V_{PG\_UVP0\_FALLING\_LDO}$	PG_THRESHOLD[0] = 0, V_{LDO} = 2.5V	94	96	98	% of V_{OUT}
	$V_{PG\_UVP1\_FALLING\_LDO}$	PG_THRESHOLD[0] = 1, V_{LDO} = 2.5V	92	94	96	% of V_{OUT}
LDO PG UVP hysteresis (9)	$V_{PG\_UVP\_HYS\_LDO}$			0.6		% of V_{OUT}

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 8V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal Protection						
Thermal warning (7)	T_{TW}		110	125	140	°C
Thermal warning hysteresis (7)	T_{TW_HYS}			20		°C
Thermal shutdown (7)	T_{SD}		155	170	185	°C
Thermal shutdown hysteresis (7)	T_{SD_HYS}			20		°C
Output Voltage (V_{OUT}) Protection						
V_{OUT} OVP threshold (9)	V_{OUT_OVP}	V_{OUT} > 1.25V	112	115	118	% of V_{OUT}
		V_{OUT} < 1.25V	110	115	120	% of V_{OUT}
V_{OUT} OVP hysteresis (9)	$V_{OUT\_OVP\_HYS}$	V_{OUT} > 1.25V	3.5	6	8.5	% of V_{OUT}
		V_{OUT} < 1.25V	2.5	6	10	% of V_{OUT}
V_{OUT} UVP threshold (9)	V_{OUT_UVP}	V_{OUT} > 1.25V	72	75	78	% of V_{OUT}
		V_{OUT} < 1.25V	70	75	80	% of V_{OUT}
Hiccup time	t_{HIC}			1		ms
Reference Monitor						
Reference OVP threshold	R_{EF_OVP}		102	103.3	104.6	% of V_{OUT}
Reference UVP threshold	R_{EF_UVP}		95.4	96.7	98	% of V_{OUT}
Configuration Options						
V_{OUT} range (7)	V_{OUT1}		2.5		4	V
	V_{OUT2}		0.6		3.75	V
	V_{OUT3}		0.6		2.55	V
	V_{LDOOUT}		0.6		3.75	V
Start delay range (7)	t_{START_DELAY}		0		37.5	ms
Stop delay range (7)	t_{STOP_DELAY}		0		37.5	ms
Digital Interface (7)						
Digital interface ready time	t_{PMB_R}	From V_{IN} > $V_{IN\_UVLO\_RISING}$ to digital interface ready			12	ms
Input logic high	V_{IH}		1.6			V
Input logic low	V_{IL}				0.4	V
V_{OUT} logic low	V_{OUT_L}	RSTO pin, sink 4mA			0.4	V
SCL clock frequency	f_{SCL}				1000	kHz
SCL high time	t_{HIGH}		260			ns
SCL low time	t_{LOW}		500			ns
Data set-up time	$t_{SU.DAT}$		50			ns
Data hold time	$t_{HD.DAT}$		0			ns

ELECTRICAL CHARACTERISTICS *(continued)*

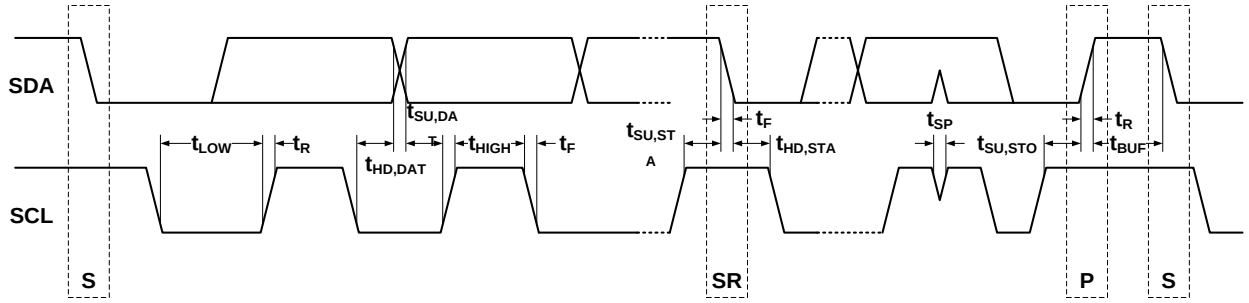
V_{IN} = 8V, T_J= -40°C to +150°C, unless otherwise noted. Typical values are at T_J= +25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Set-up time for repeated start	t_{SU_STA}		260			ns
Hold time for repeated start	t_{HD_STA}		260			ns
Bus free time between a start and a stop command	t_{BUF}		500			ns
Set-up time for stop command	t_{SU_STO}		260			ns
Rising time of SCL and SDA	t_R				120	ns
Falling time of SCL and SDA	t_F	V_{DD} supplies the digital interface	20 x (V_{DD} / 5.5V)		120	ns
Pulse width of suppressed spike	t_{SP}				50	ns
Capacitance bus for each bus line	C_B				550	pF

Notes:

7) Guaranteed by design and bench characterization. Not tested in production.
8) Write to the relevant register to update this parameter.
9) The threshold is based on the nominal V_{OUT} of each output.

DIGITAL INTERFACE COMPATIBLE TIMING DIAGRAM



S: Start Condition

SR: Repeated Start Condition

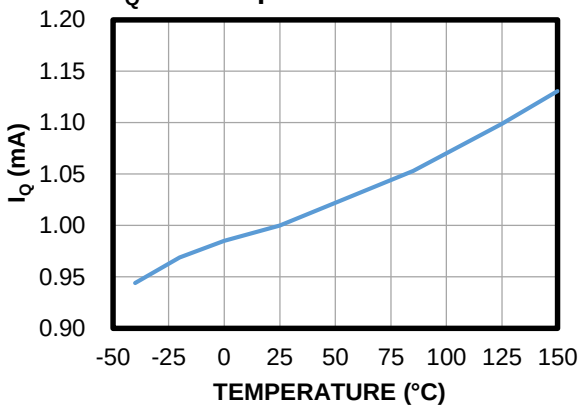
P: Stop Condition

Figure 1: Digital Interface Compatible Timing Diagram

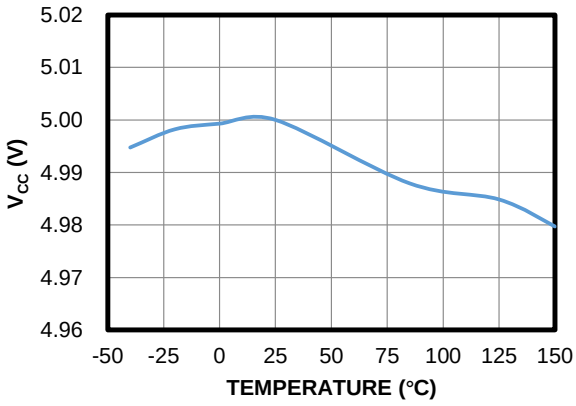
TYPICAL CHARACTERISTICS

V_{IN} = 8V, T_A = -40°C to +150°C, unless otherwise noted.

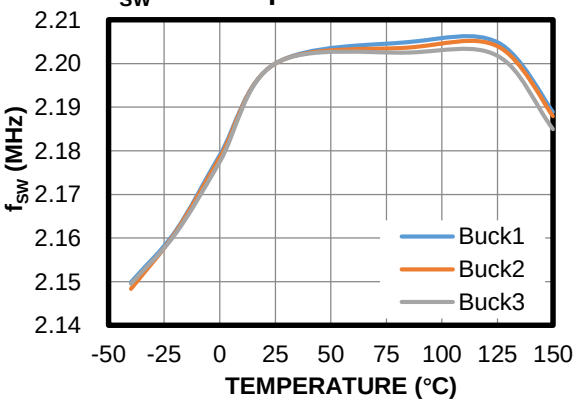
I_Q vs. Temperature



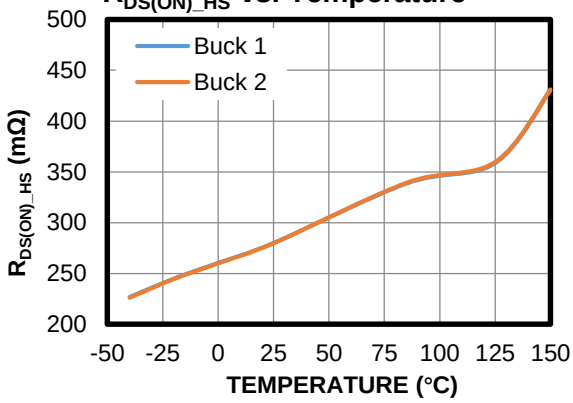
V_{CC} vs. Temperature



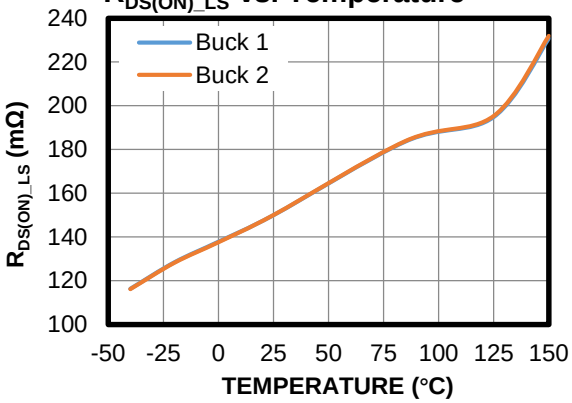
f_{SW} vs. Temperature



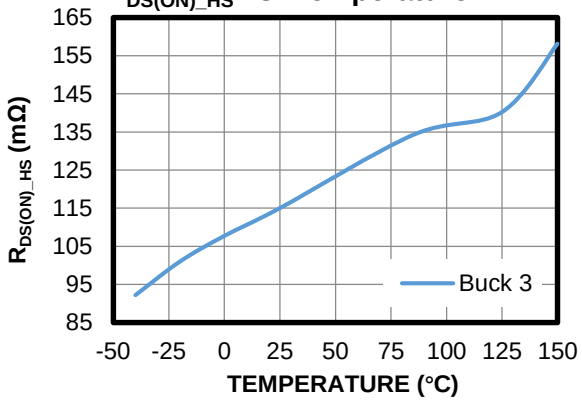
$R_{DS(ON)\_HS}$ vs. Temperature



$R_{DS(ON)\_LS}$ vs. Temperature



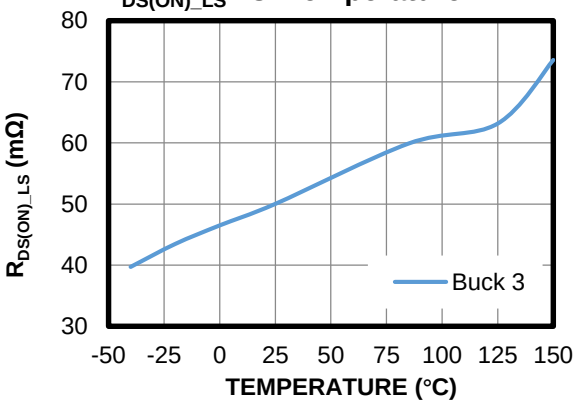
$R_{DS(ON)\_HS}$ vs. Temperature



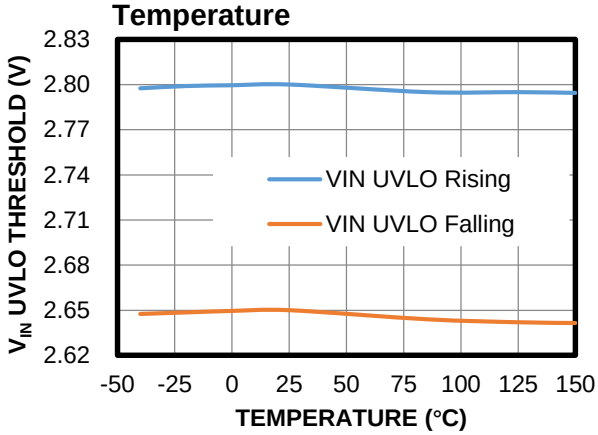
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 8V, T_A = -40°C to +150°C, unless otherwise noted.

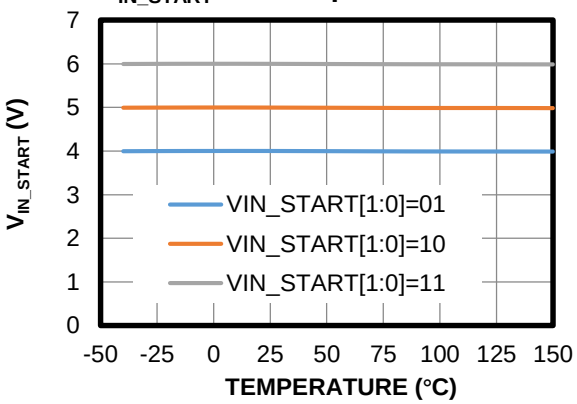
$R_{DS(ON)\_LS}$ vs. Temperature



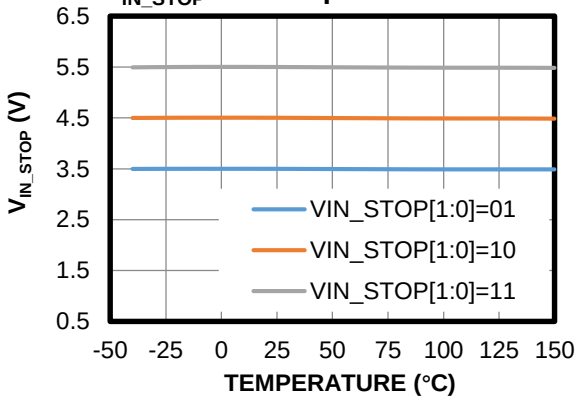
V_{IN} UVLO Threshold vs. Temperature



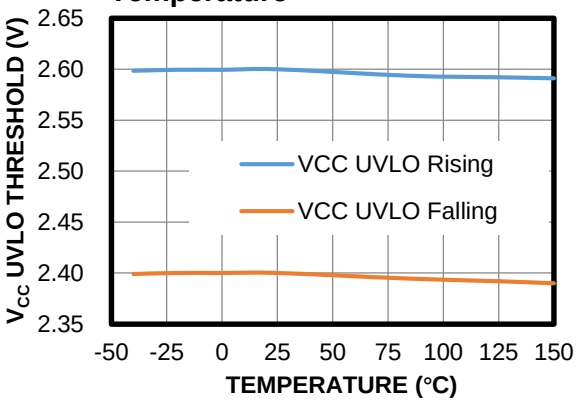
V_{IN_START} vs. Temperature



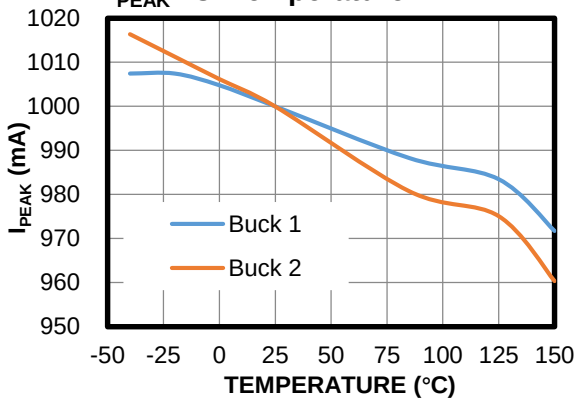
V_{IN_STOP} vs. Temperature



V_{CC} UVLO Threshold vs. Temperature



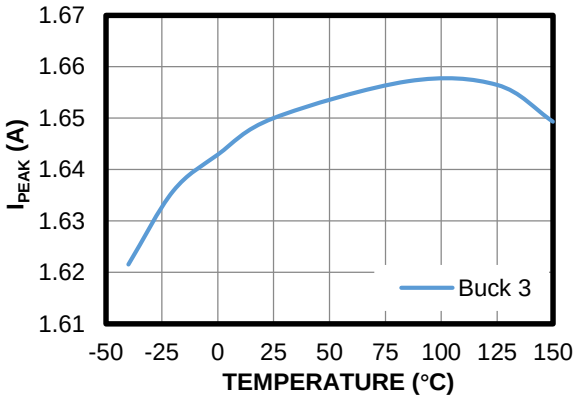
I_{PEAK} vs. Temperature



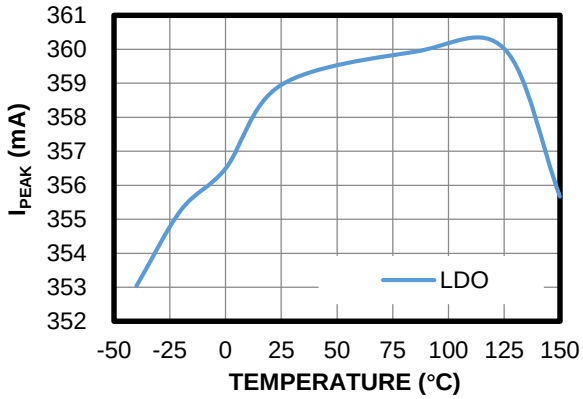
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 8V, T_A = -40°C to +150°C, unless otherwise noted.

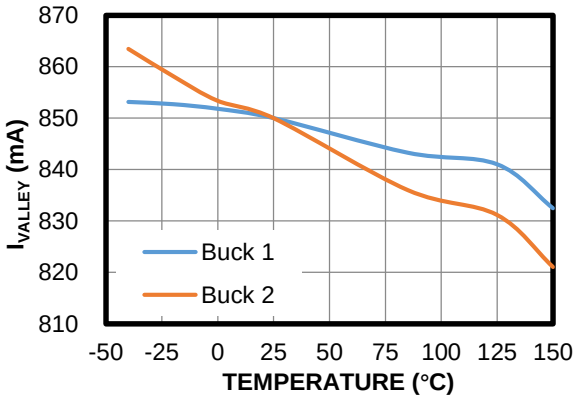
I_{PEAK} vs. Temperature



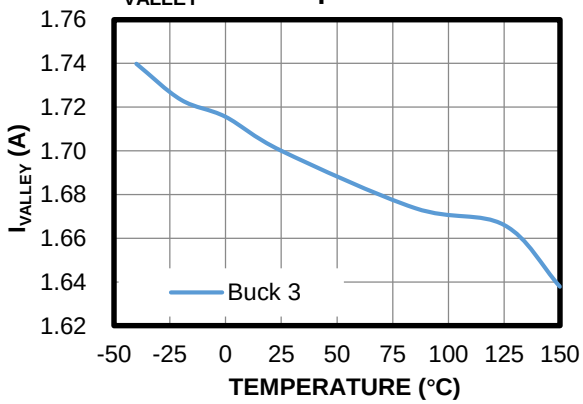
I_{PEAK} vs. Temperature



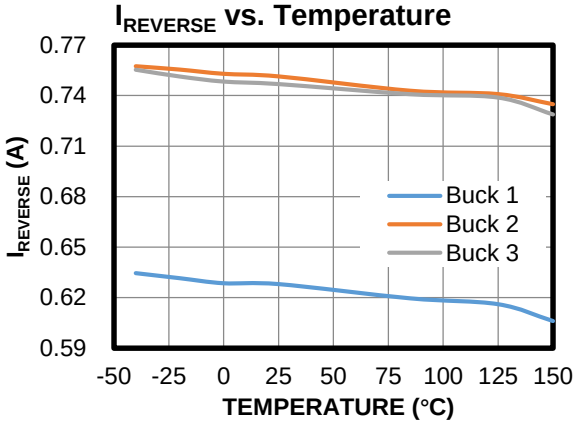
I_{VALLEY} vs. Temperature



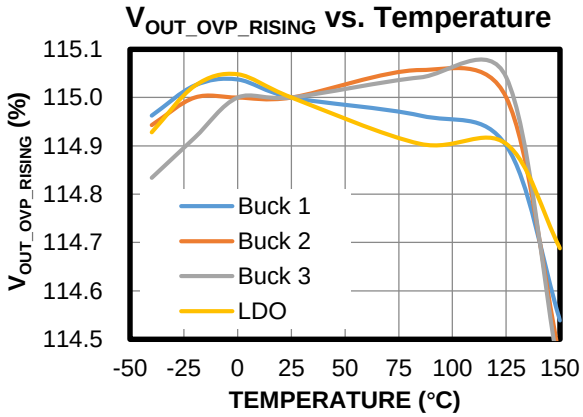
I_{VALLEY} vs. Temperature



$I_{REVERSE}$ vs. Temperature

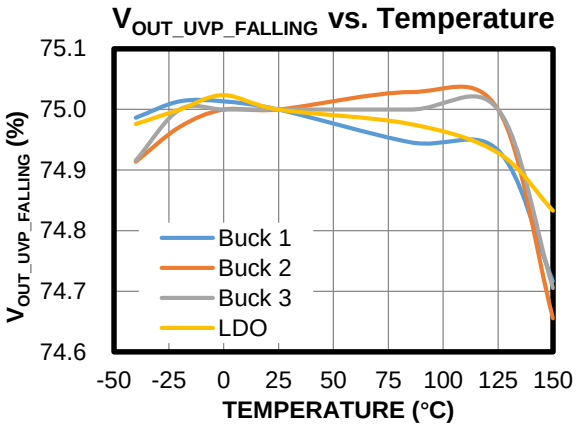


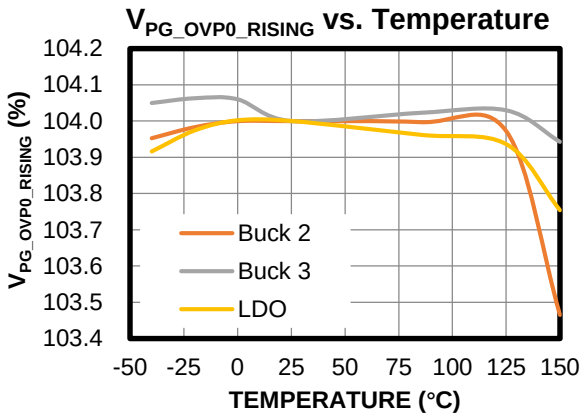
$V_{OUT\_OVP\_RISING}$ vs. Temperature

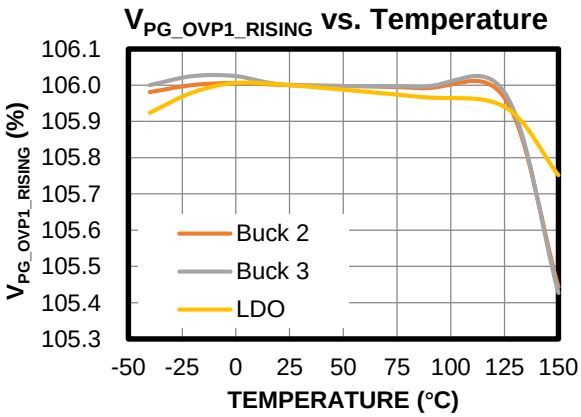


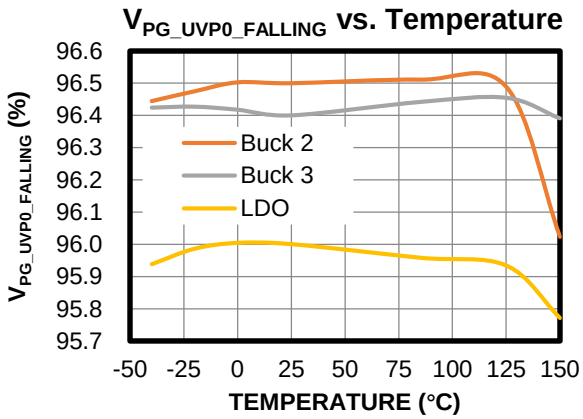
TYPICAL CHARACTERISTICS *(continued)*

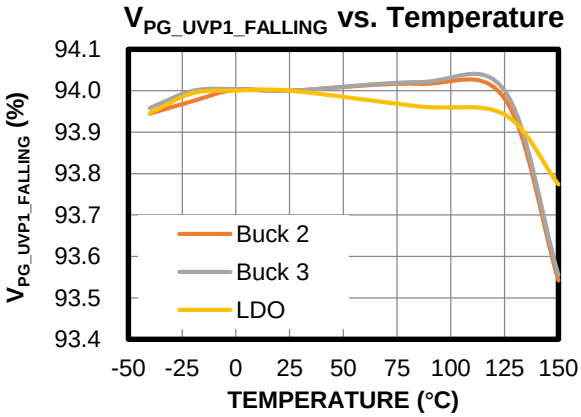
V_{IN} = 8V, T_A = -40°C to +150°C, unless otherwise noted.

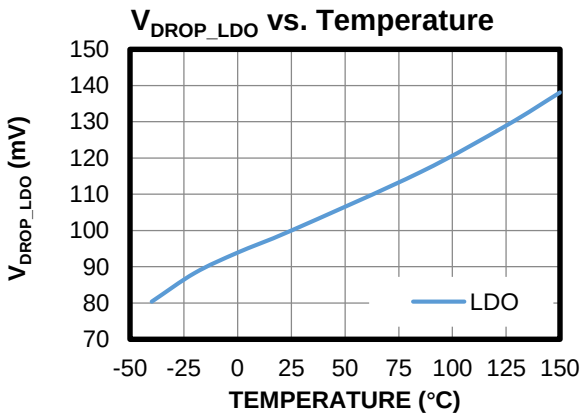










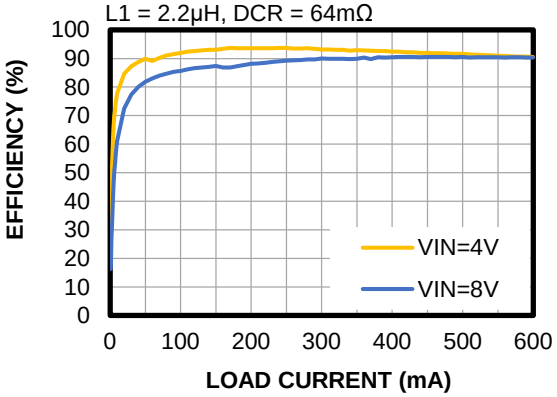


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

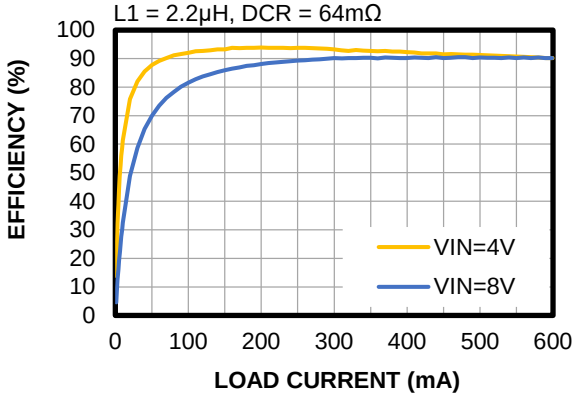
Efficiency vs. Load Current (Buck 1)

V_{OUT1} = 3V, f_{SW1} = 2.2MHz, DCM, other channels are disabled, L1 = 2.2µH, DCR = 64mΩ



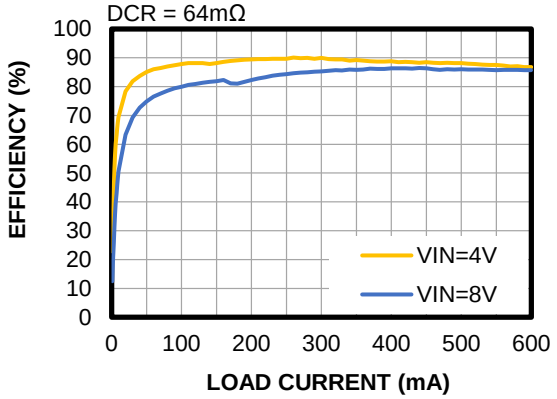
Efficiency vs. Load Current (Buck 1)

V_{OUT1} = 3V, f_{SW1} = 2.2MHz, FCCM, other channels are disabled, L1 = 2.2µH, DCR = 64mΩ



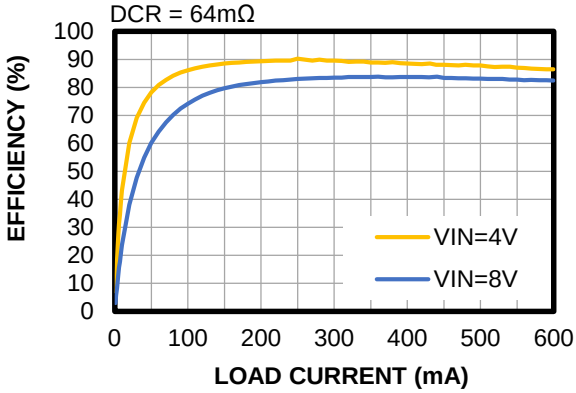
Efficiency vs. Load Current (Buck 2)

V_{OUT2} = 1.8V, f_{SW2} = 2.2MHz, DCM, other channels are disabled, L2 = 2.2µH, DCR = 64mΩ



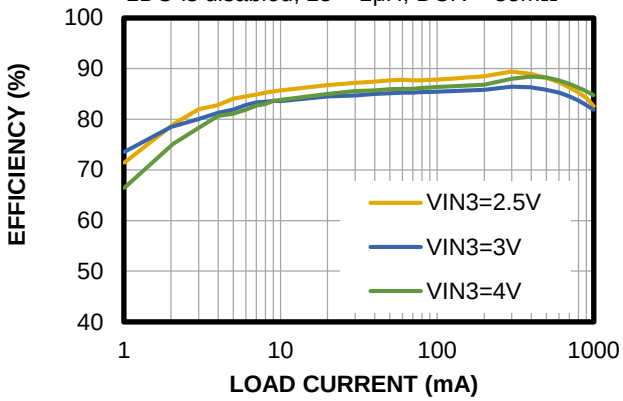
Efficiency vs. Load Current (Buck 2)

V_{OUT2} = 1.8V, f_{SW2} = 2.2MHz, FCCM, other channels are disabled, L2 = 2.2µH, DCR = 64mΩ



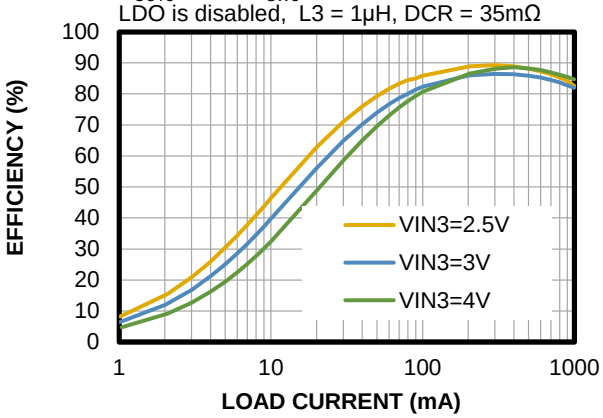
Efficiency vs. Load Current (Buck 3)

V_{OUT3} = 1.2V, f_{SW3} = 2.2MHz, DCM, LDO is disabled, L3 = 1µH, DCR = 35mΩ



Efficiency vs. Load Current (Buck 3)

V_{OUT3} = 1.2V, f_{SW3} = 2.2MHz, FCCM, LDO is disabled, L3 = 1µH, DCR = 35mΩ

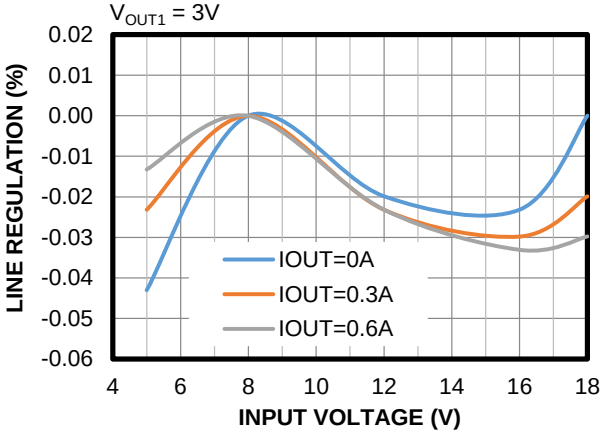


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

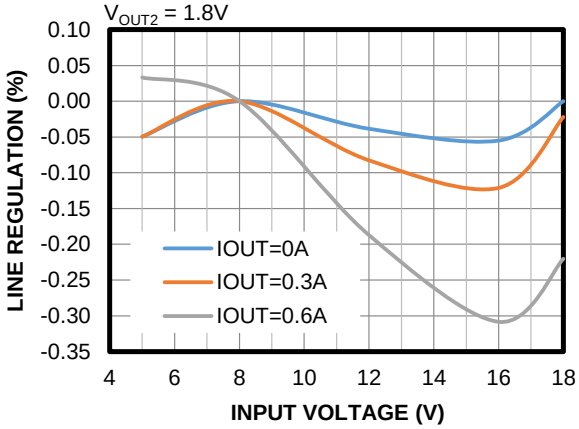
Line Regulation (Buck 1)

V_{OUT1} = 3V



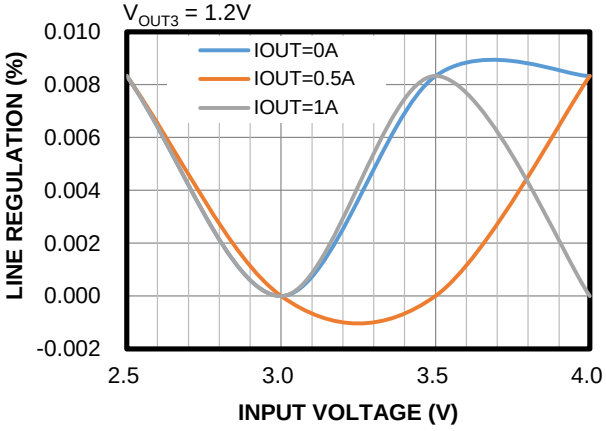
Line Regulation (Buck 2)

V_{OUT2} = 1.8V



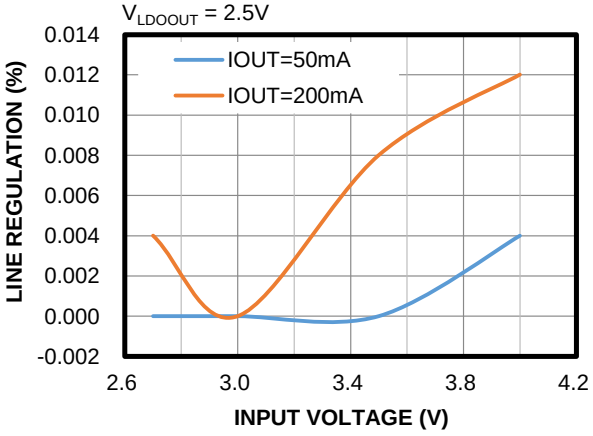
Line Regulation (Buck3)

V_{OUT3} = 1.2V



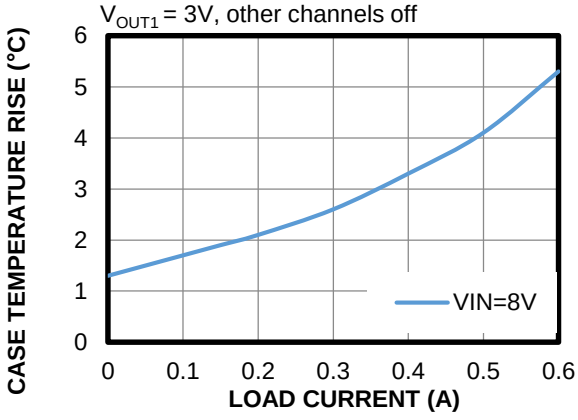
Line Regulation (LDO)

V_{LDOOUT} = 2.5V



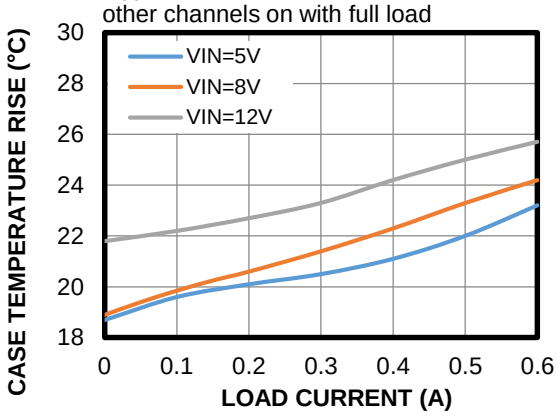
Case Temperature Rise (Buck 1)

V_{OUT1} = 3V, other channels off



Case Temperature Rise (Buck 2)

V_{OUT2} = 1.8V, channel 1 on with no load, other channels on with full load

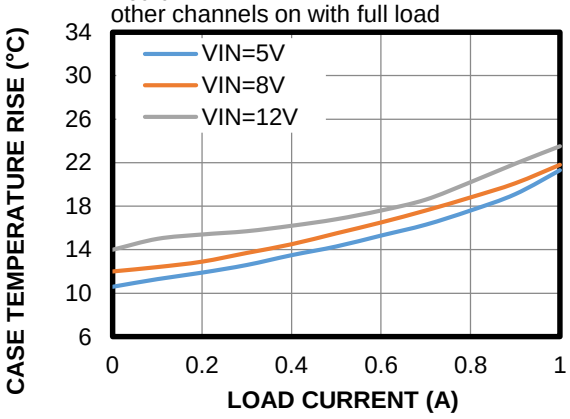


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

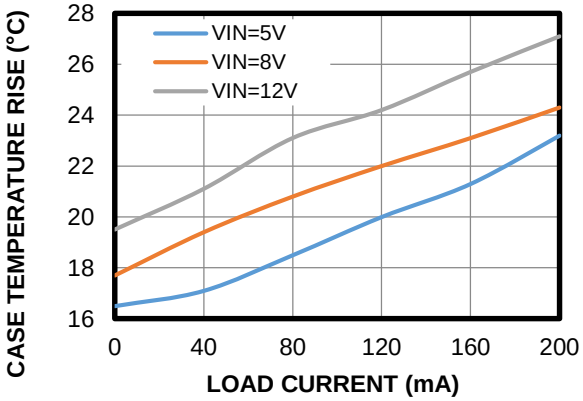
Case Temperature Rise (Buck 3)

V_{OUT3} = 1.2V, channel 1 on with no load, other channels on with full load



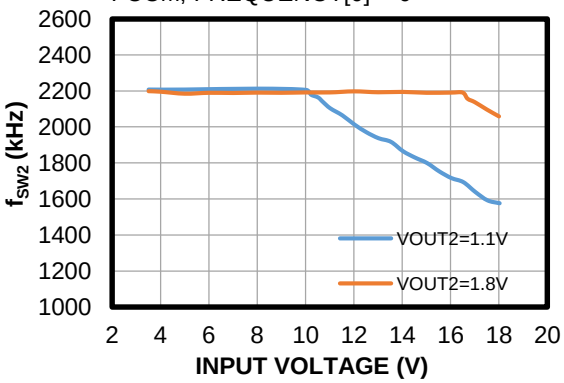
Case Temperature Rise (LDO)

V_{LDOOUT} = 2.5V, channel 1 on with no load, other channels on with full load



f_{SW2} vs. V_{IN}

FCCM, FREQUENCY[0] = 0

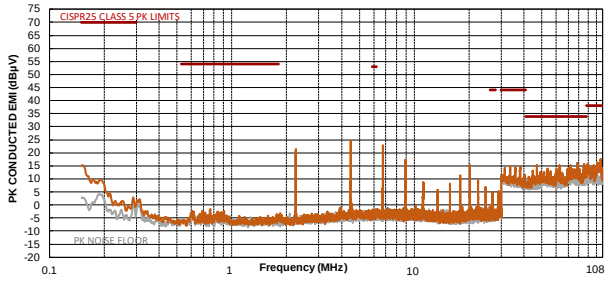


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted. (10)

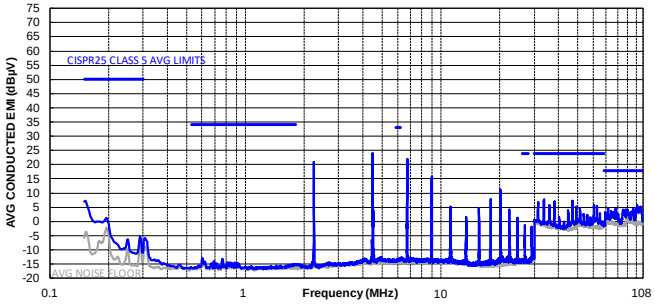
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



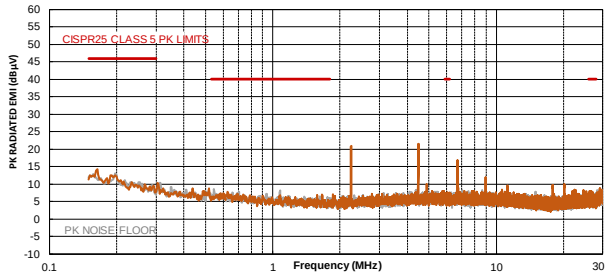
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



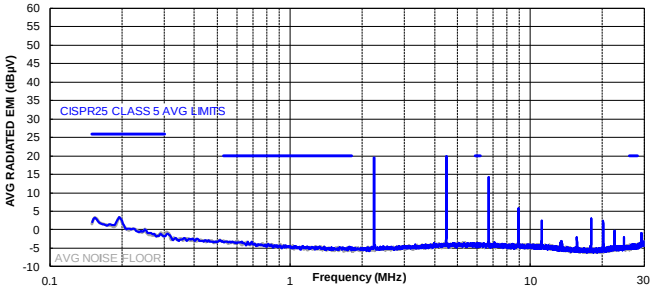
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



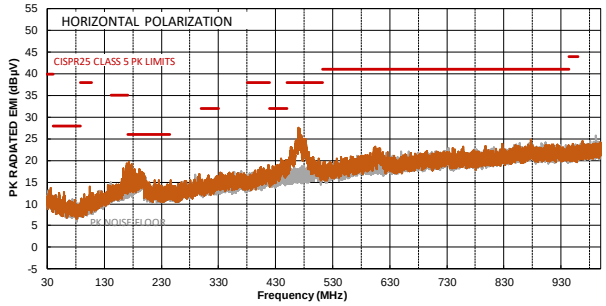
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



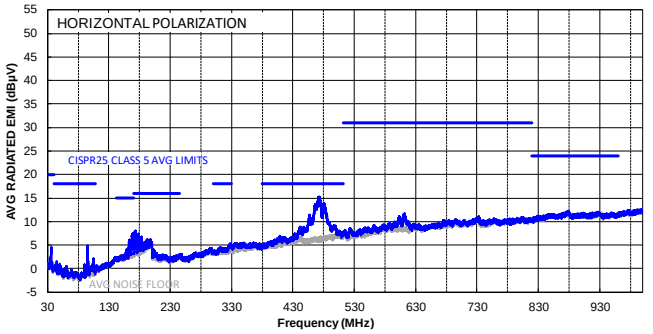
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

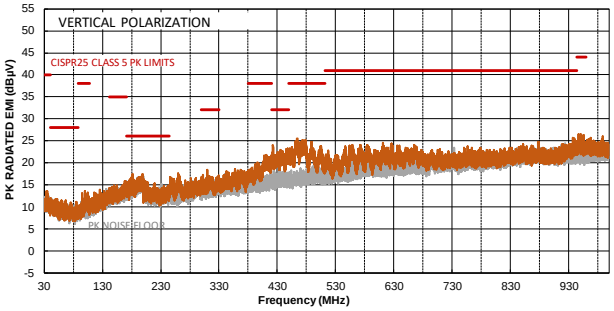


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted. (10)

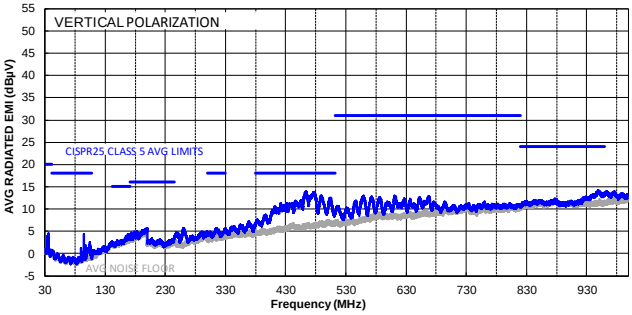
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz-1GHz



Note:

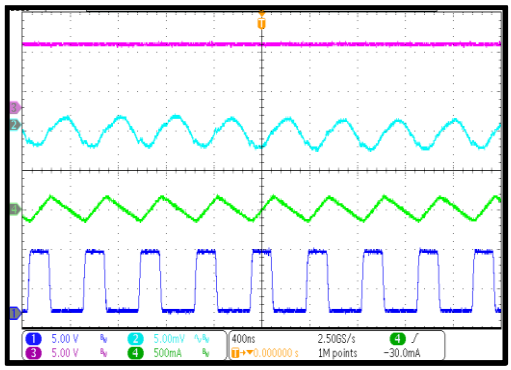
10) The EMC test results are based on the typical application circuit with EMI filters and frequency spread spectrum (FSS) function (see Figure 17 on page 72).

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

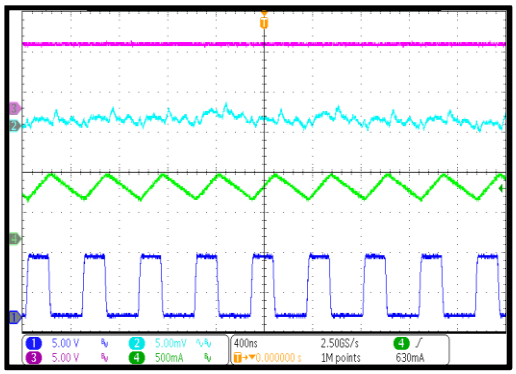
Steady State (Buck 1)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



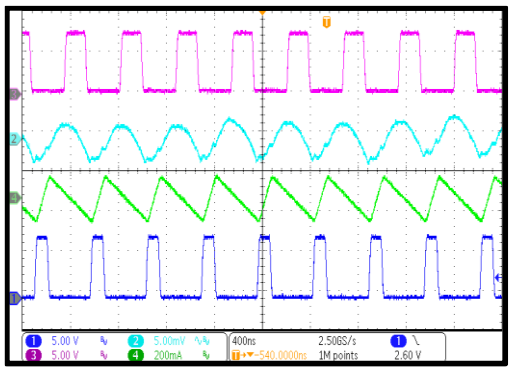
Steady State (Buck 1)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



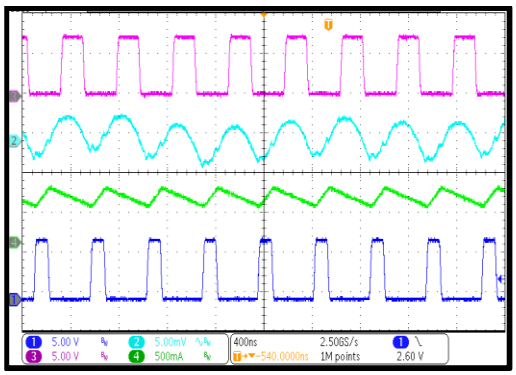
Steady State (Buck 2)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



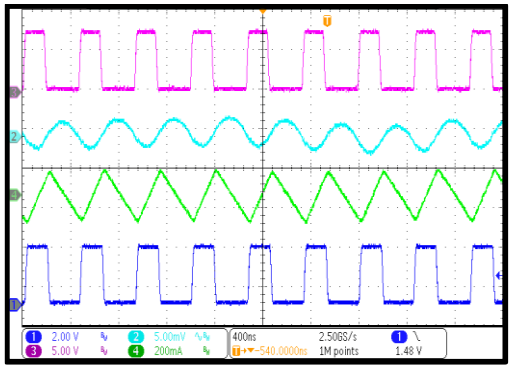
Steady State (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



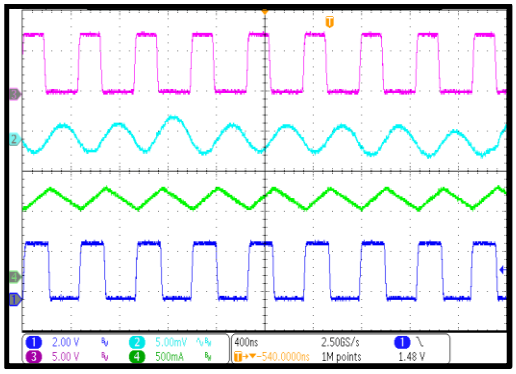
Steady State (Buck 3)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



Steady State (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA

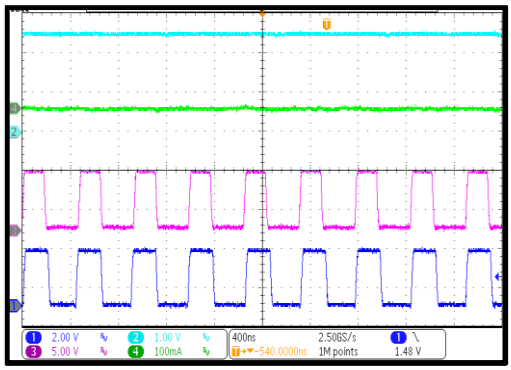


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

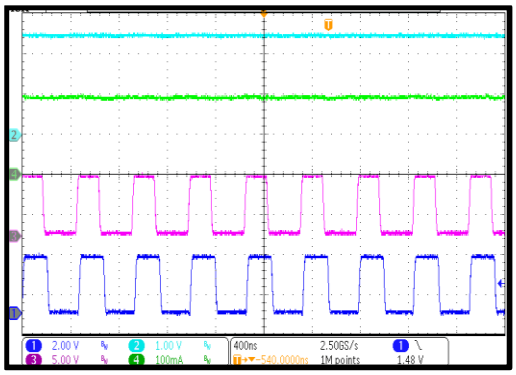
Steady State (LDO)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



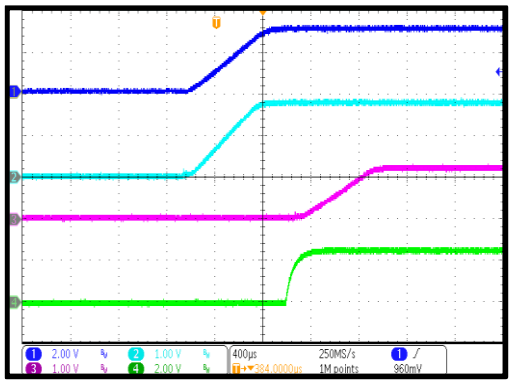
Steady State (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



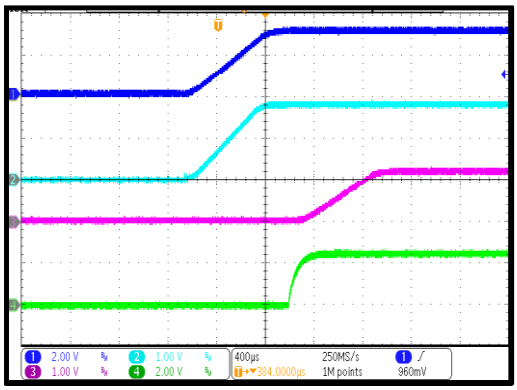
Start-Up through VIN (Start-Up Sequence)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



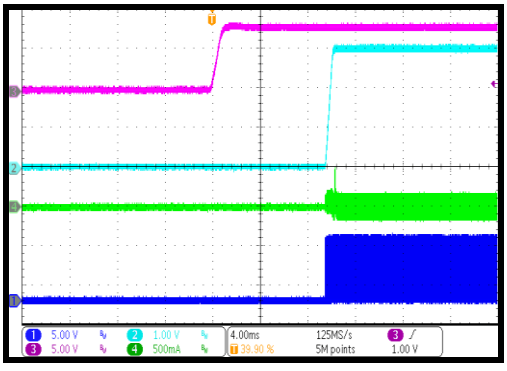
Start-Up through VIN (Start-Up Sequence)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



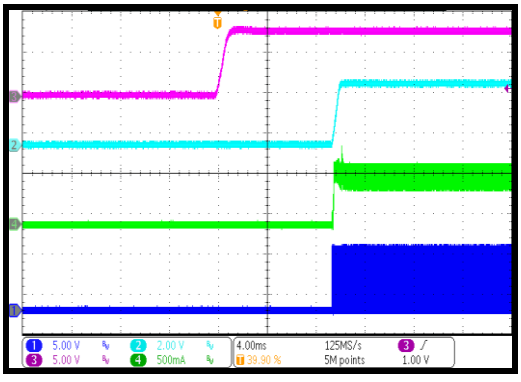
Start-Up through VIN (Buck 1)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



Start-Up through VIN (Buck 1)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA

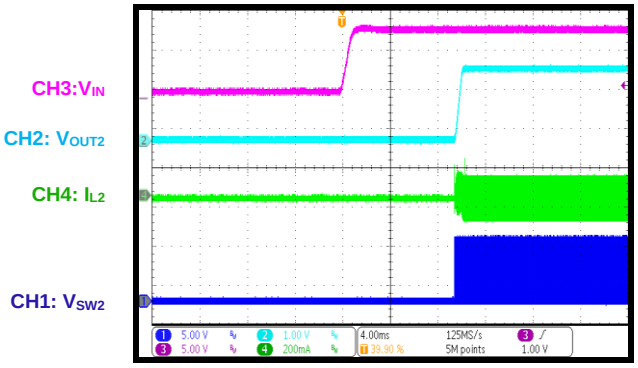


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

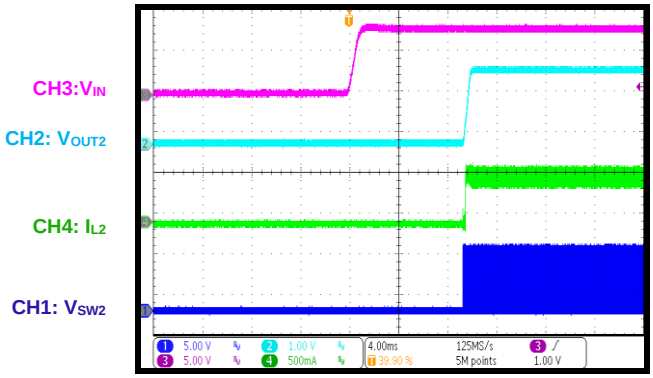
Start-Up through VIN (Buck 2)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



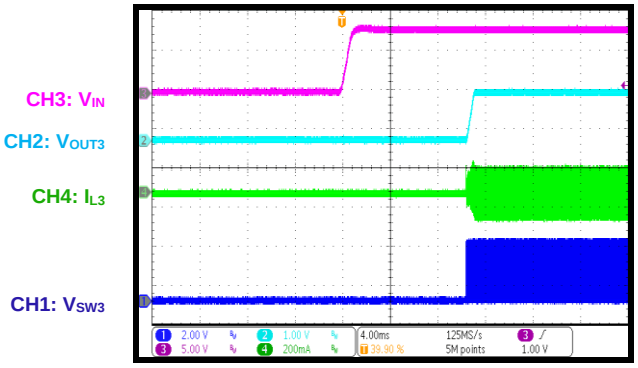
Start-Up through VIN (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



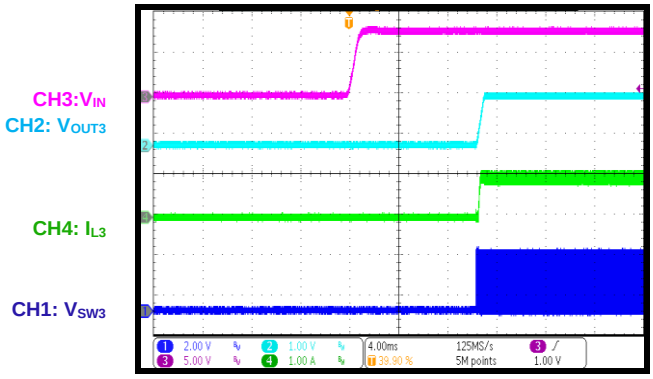
Start-Up through VIN (Buck 3)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



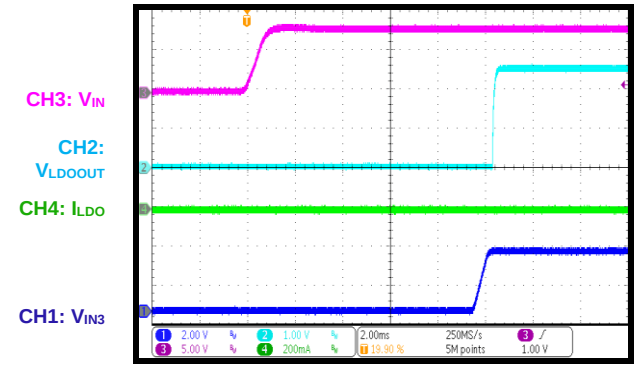
Start-Up through VIN (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



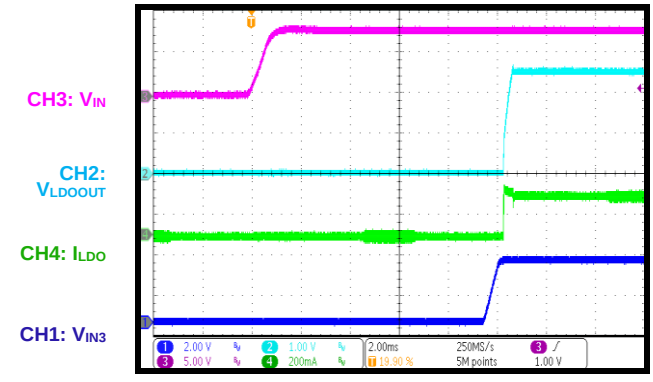
Start-Up through VIN (LDO)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



Start-Up through VIN (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA

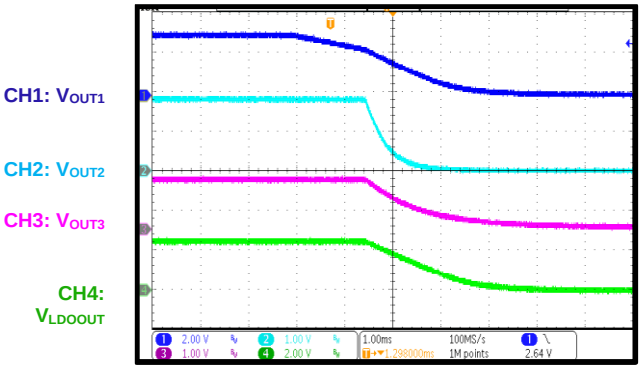


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

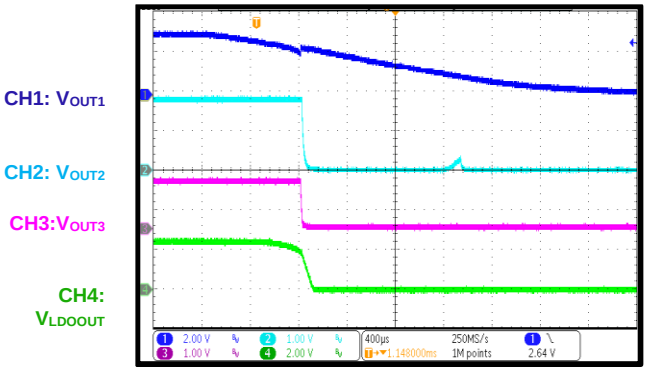
Shutdown through VIN

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



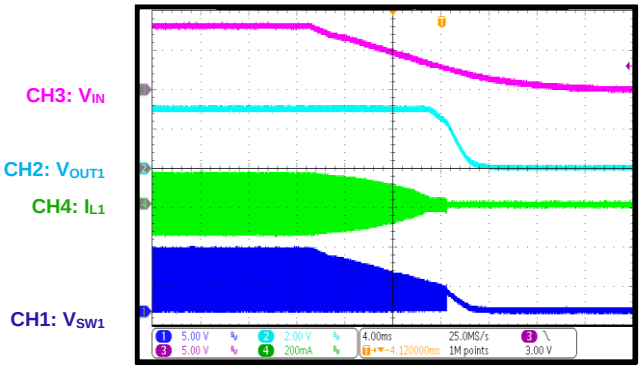
Shutdown through VIN

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



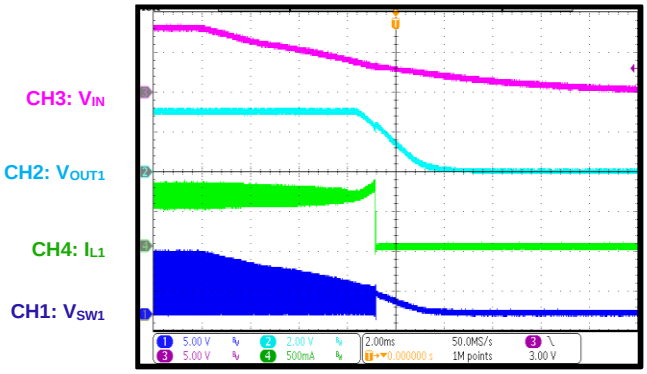
Shutdown through VIN (Buck1)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



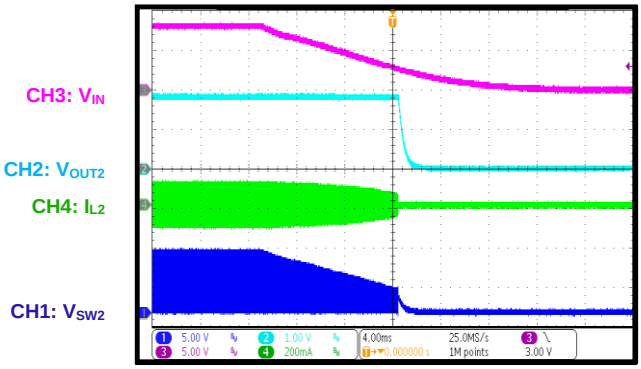
Shutdown through VIN (Buck1)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



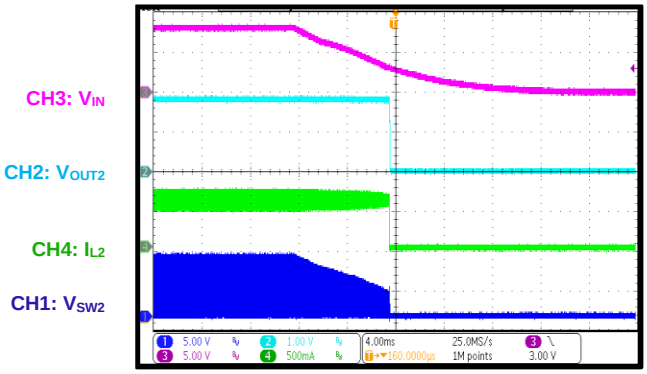
Shutdown through VIN (Buck 2)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



Shutdown through VIN (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA

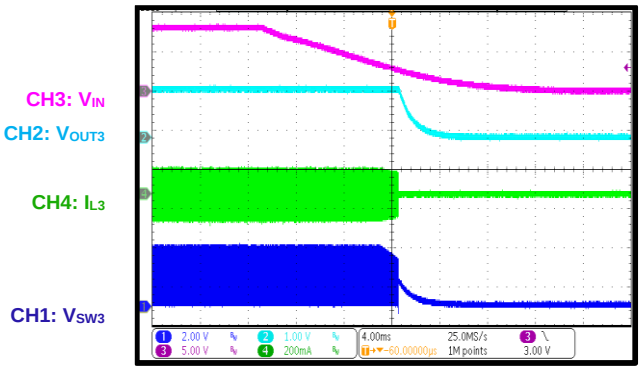


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

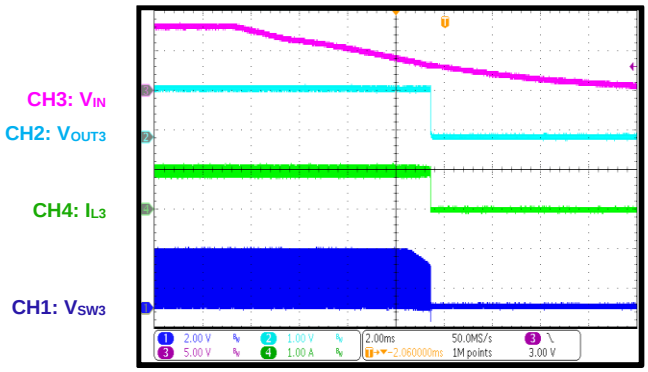
Shutdown through VIN (Buck 3)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



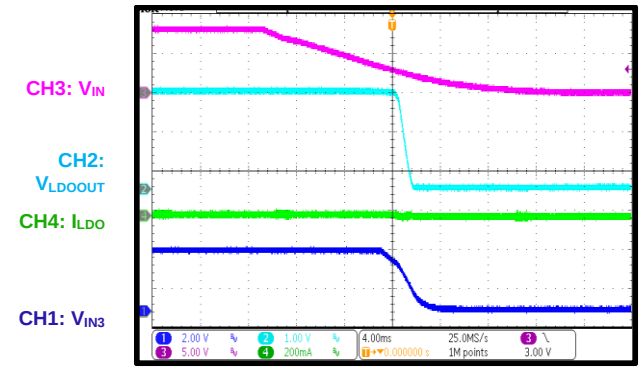
Shutdown through VIN (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



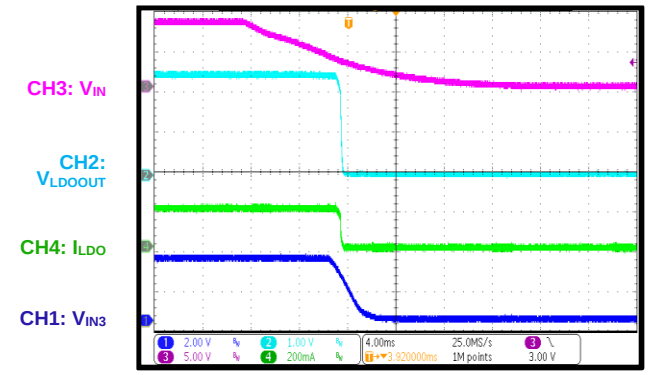
Shutdown through VIN (LDO)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A

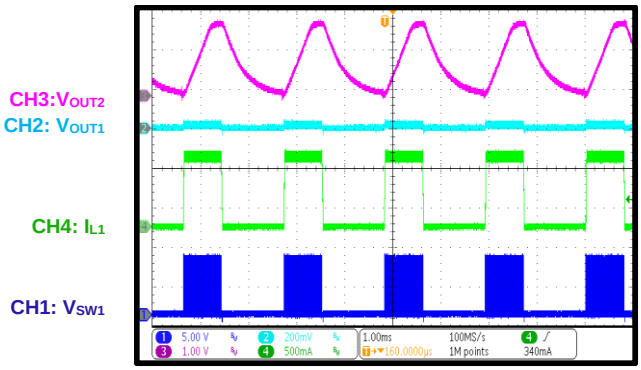


Shutdown through VIN (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA

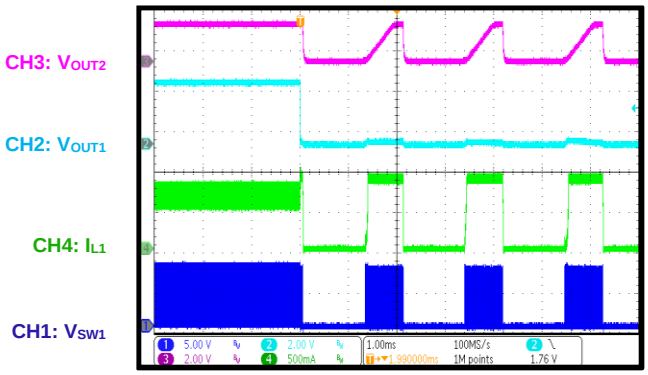


SCP Steady State (Buck 1)



SCP Entry (Buck 1)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA

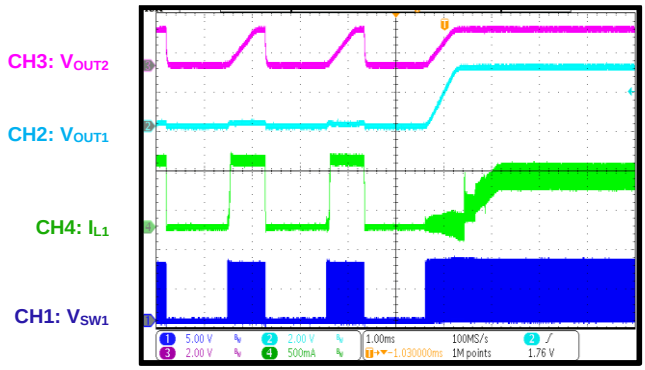


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

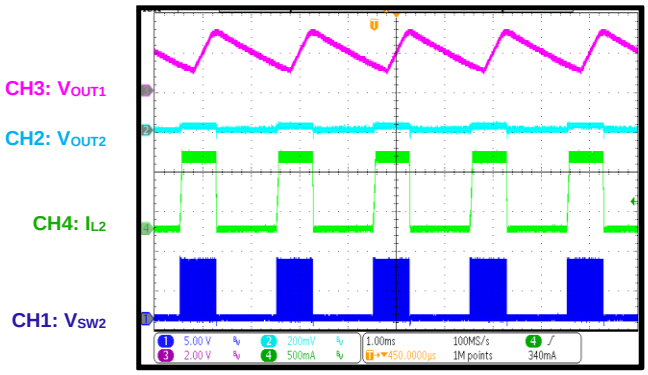
V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

SCP Recovery (Buck 1)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA

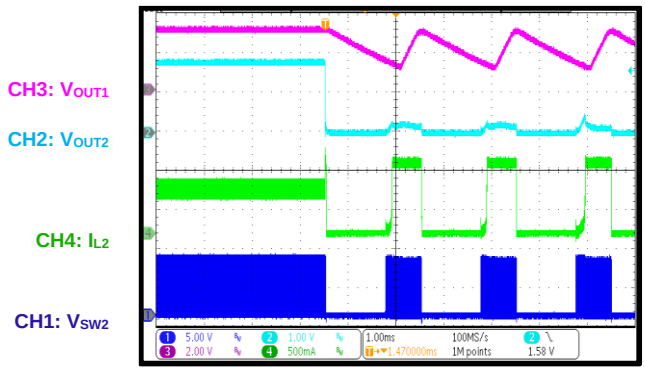


SCP Steady State (Buck 2)



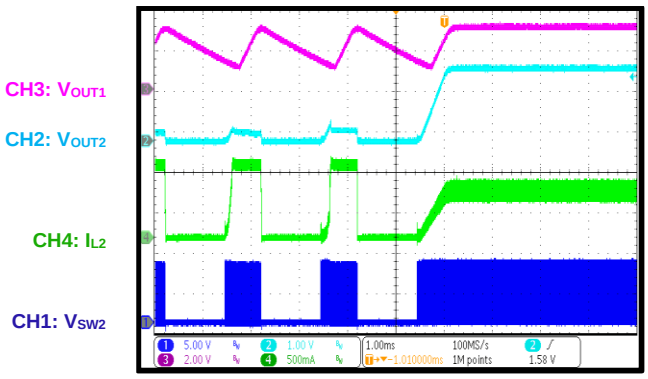
SCP Entry (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA

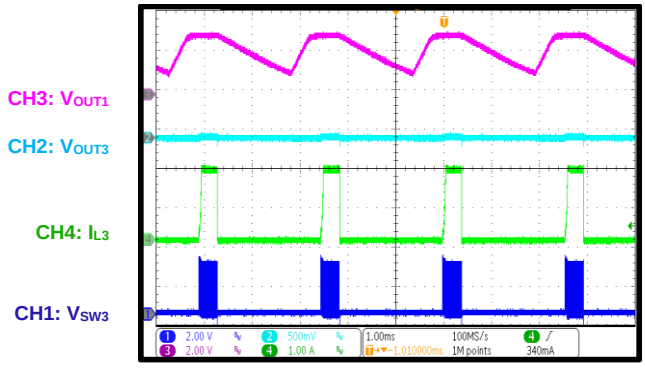


SCP Recovery (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA

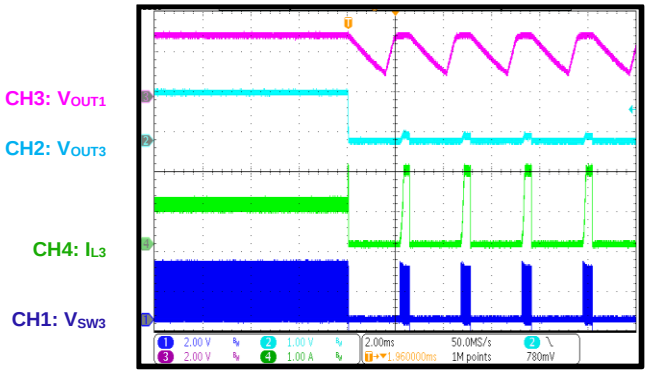


SCP Steady State (Buck 3)



SCP Entry (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA

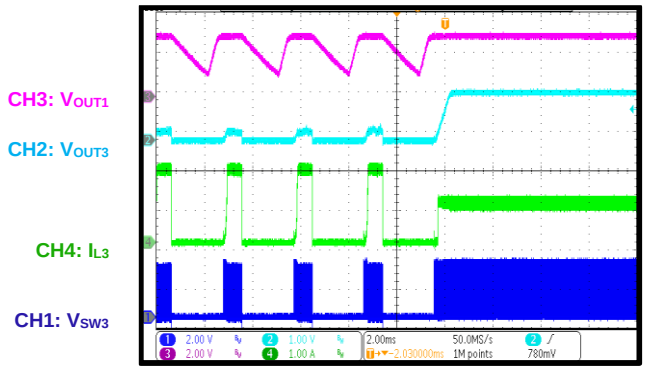


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

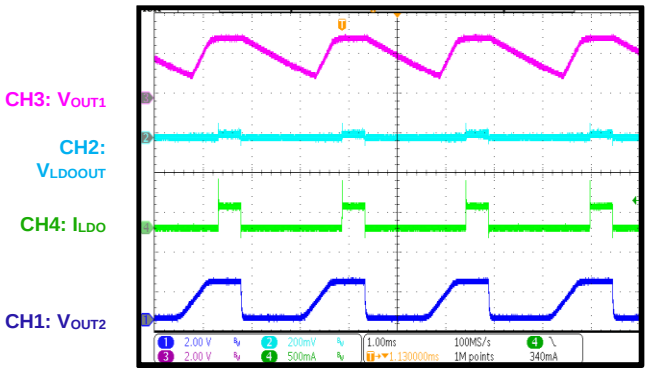
V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

SCP Recovery (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA

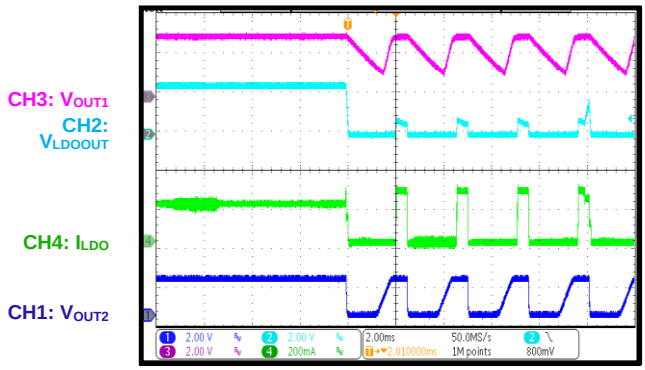


SCP Steady State (LDO)



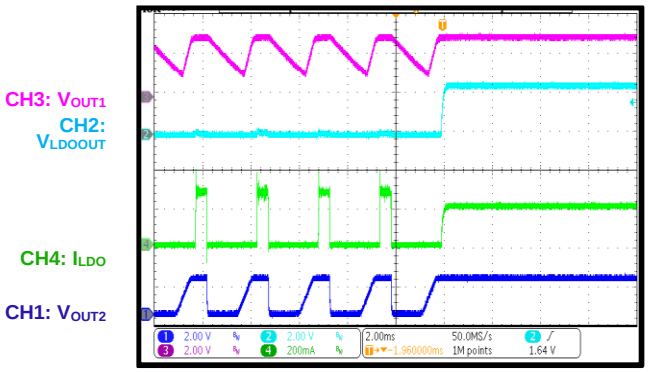
SCP Entry (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



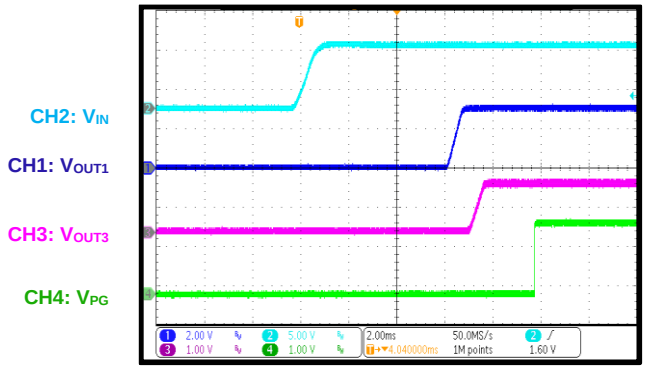
SCP Recovery (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



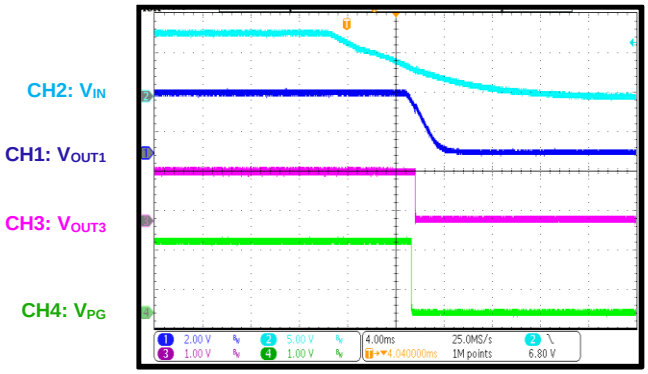
PG Start-Up through VIN

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



PG Shutdown through VIN

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA

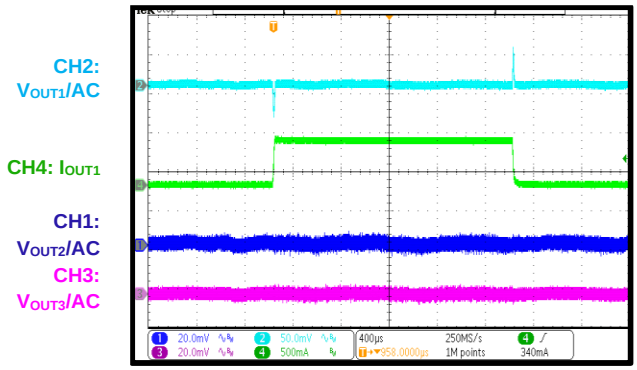


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

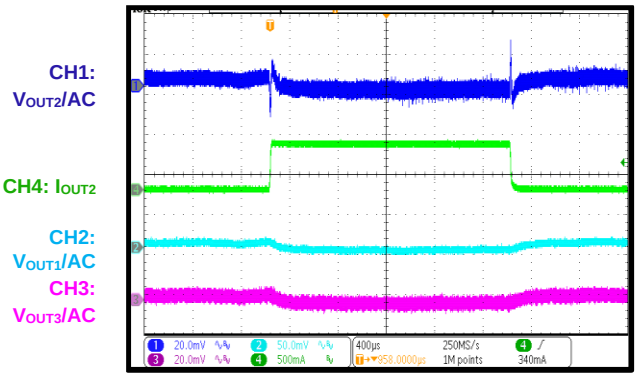
Load Transient (Buck 1)

I_{OUT1} = 0A to 600mA, I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



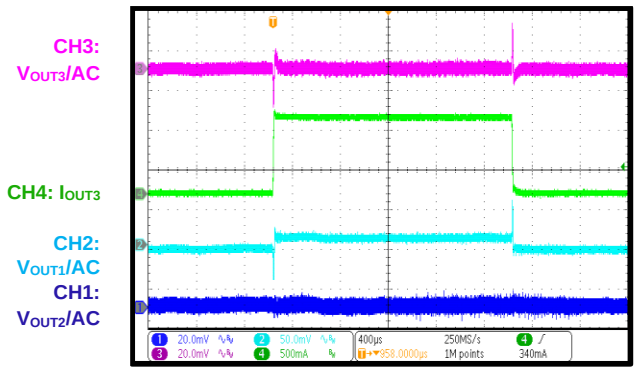
Load Transient (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 0A to 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



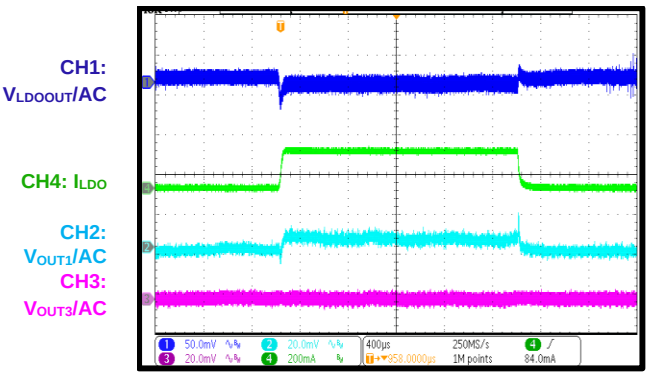
Load Transient (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 0A to 1A, I_{LDO} = 200mA



Load Transient (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 0 to 200mA



FUNCTIONAL BLOCK DIAGRAM

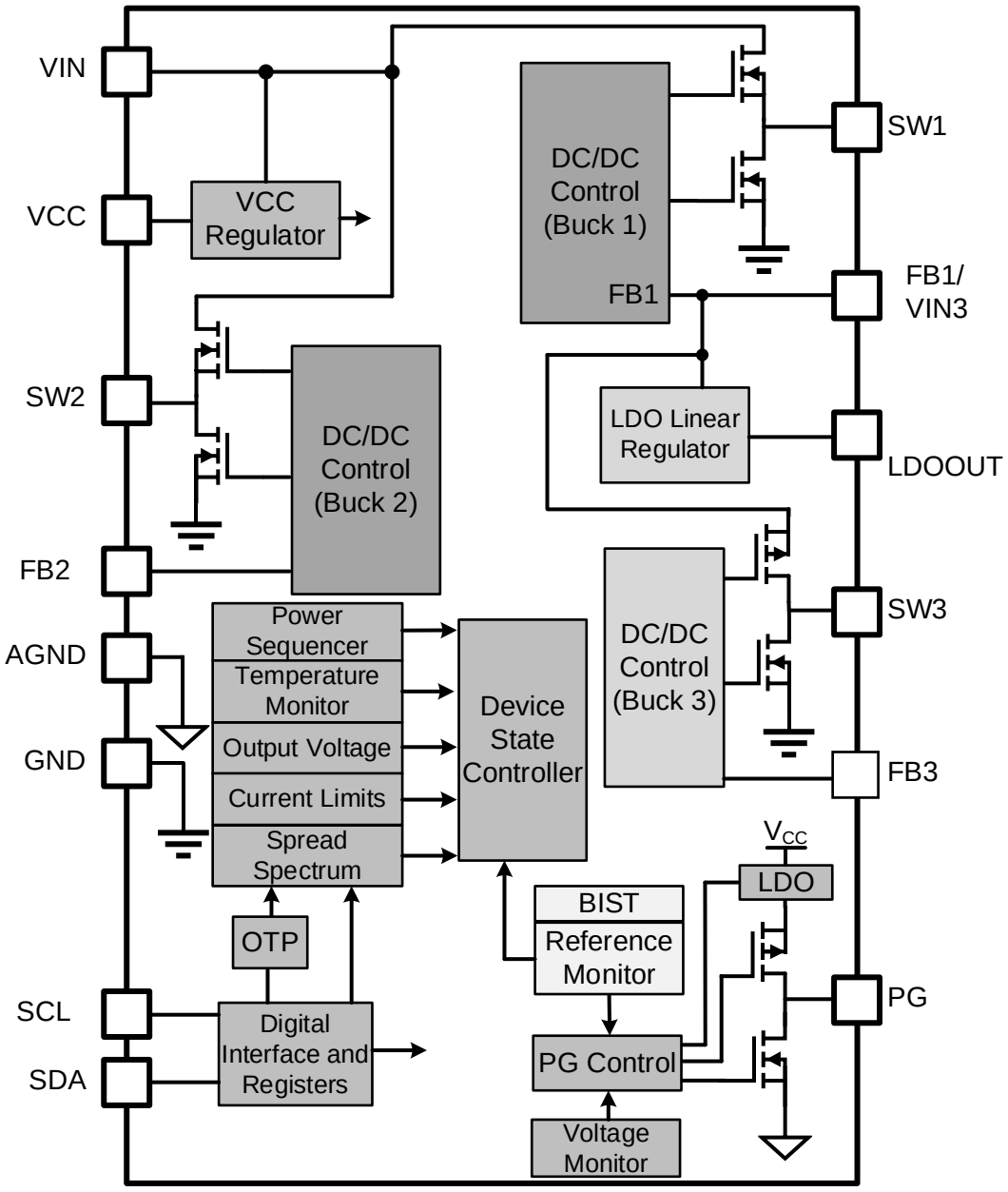
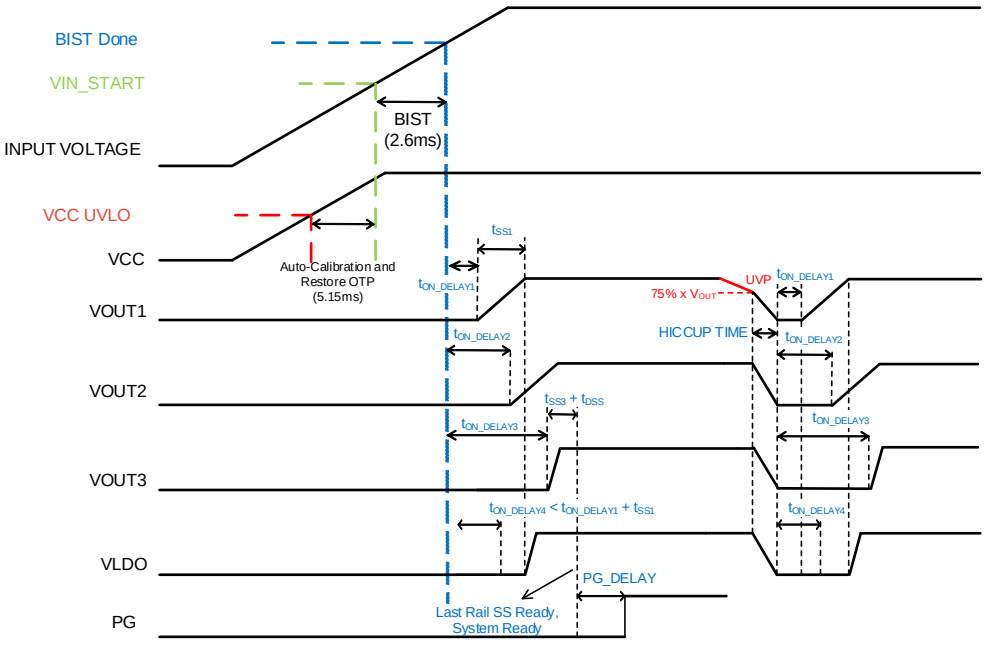


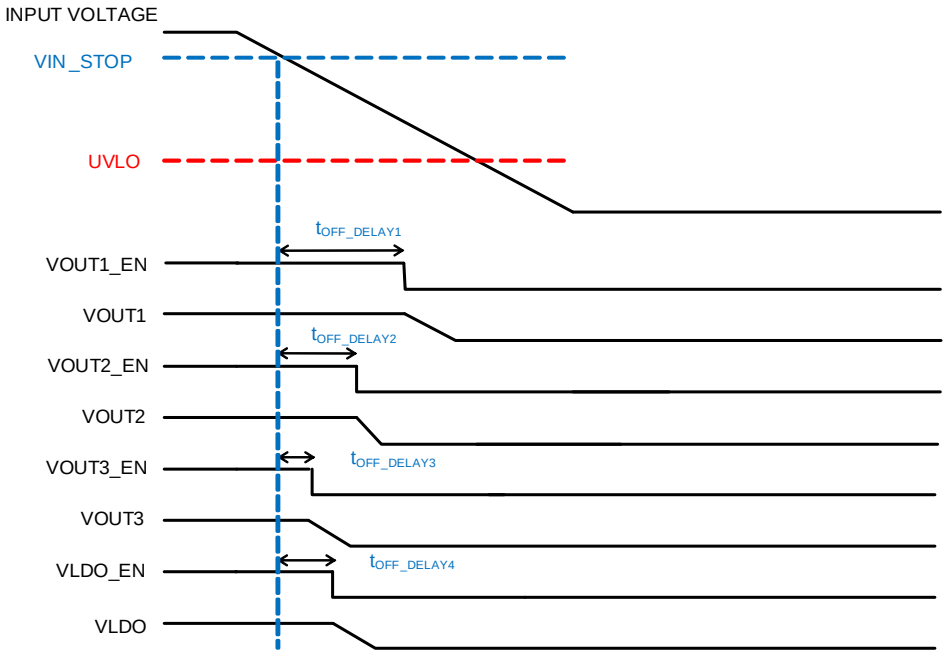
Figure 2: Functional Block Diagram

POWER-ON AND POWER-OFF SEQUENCE



Notes: If $V_{IN} > V_{IN\_START}$ while restoring OTP, BIST starts after restoring OTP finishes.
If $t_{ON\_DELAY} + t_{SS1} > t_{ON\_DELAY3} / t_{ON\_DELAY4}$, buck 3 and the LDO begin to rise after V_{OUT1} is ready.
Assuming $t_{ON\_DELAYy} > t_{ON\_DELAYx}$, ensure that $t_{ON\_DELAYy} < t_{ON\_DELAYx} + t_{SSx} + t_{DSSx}$

Figure 3: Power-On Sequence



Notes: The falling time depends on the load.
If the output discharge function is enabled, a pull-down resistor turns on after VOUTX_EN falls until UVLO.

Figure 4: Power-Off Sequence

OPERATION

The MPQ70240FS provides a complete power management solution for 8V automotive systems, such as satellite cameras. It integrates three high-frequency, synchronous rectified, step-down switch-mode converters and a low-dropout (LDO) regulator. The MPQ70240FS greatly reduces PCB size with its compact QFN-15 (2.5mmx3.5mm) package.

The digital interface provides an adjustable default output voltage (V_{OUT}), power-on sequence, and dynamic voltage scaling. It also provides powerful logic functions.

High-Efficiency Buck Converters

Buck converter 1 (buck 1), buck converter 2 (buck 2), and buck converter 3 (buck 3) are synchronous, step-down DC/DC converters that have built-in under-voltage lockout (UVLO), soft start (SS), compensation, and current-limit protection with hiccup mode. Fixed-frequency, constant-on-time (COT) control provides fast transient response. Both buck 1 and buck 2 are medium-voltage (MV) bucks, and their input is the input voltage (V_{IN}). Buck 3 is a low-voltage (LV) buck, and its input is buck 1's output.

Compared to fixed-frequency pulse-width modulation (PWM) control, constant-on-time (COT) control offers a simpler control loop and faster transient response. The internal clock's phase-locked loop (PLL) can ensure a fixed operating frequency. When the low-side MOSFET (LS-FET) turns on, it remains on for at least the high-side MOSFET (HS-FET) minimum off time (t_{OFF_MIN}). Then the HS-FET turns on when the feedback voltage (V_{FB}) drops below the reference voltage (V_{REF}). After the HS-FET turns on for a calculated on time (t_{ON}), the LS-FET turns on.

The switching clock is phase-shifted from buck 1 to buck 2 during continuous conduction mode (CCM). Buck 1 is in phase with buck 3 during CCM.

LDOOUT

The MPQ70240FS supports an adjustable output and low-noise LDO output with over-voltage protection (OVP) and under-voltage protection (UVP). The LDO has an output that can be adjusted via the digital interface (from 0.6V to 3.75V, with 50mV/step). The LDO supports 200mA of output current (I_{LDO}) with over-current protection (OCP).

Power Supply and Under-Voltage Lockout (UVLO)

VIN is the power supply for buck 1 and buck 2, and for the bias and internal logic blocks. VIN generates the VCC voltage (V_{CC}) through a regulator, and V_{CC} supplies power to each internal module. FB1/VIN3 is the feedback of buck 1, as well as the power supply for buck 3 and LDOOUT. If buck 1 is disabled via the digital interface, buck 3 and the LDO output shut down.

When V_{IN} is below its UVLO threshold and V_{CC} exceeds its UVLO threshold, the MPQ70240FS turns off all outputs (each channel turns off one by one according to the set shutdown sequence). If the output discharge function is enabled, the energy of the output capacitor (C_{OUT}) is released through the internal discharge path during shutdown.

When V_{CC} is below its UVLO threshold, the MPQ70240FS turns off all outputs at the same time. During the shutdown process, the internal discharge path is not open, even if the output discharge function is enabled.

Internal Soft Start (SS)

SS is implemented to prevent the MPQ70240FS's V_{OUT} from overshooting during start-up. When the PMIC starts up, the internal circuitry of each power rail generates a soft-start voltage (V_{SS}) that ramps up from 0V. The soft-start time (t_{SS}) lasts until V_{SS} exceeds the reference voltage (V_{REF}). At this point, V_{REF} is used by the error amplifier (EA). Each buck's t_{SS} can be adjusted. See the TON_RISE (61h) sections on pages 45, 53, and 56 for more details. The LDO's t_{SS} depends on C_{OUT} and the output current (I_{OUT}) during start-up. See Equation (11) on page 70 for more details.

Light-Load Operation

The MPQ70240FS supports two light-load operation modes: continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

In DCM, the inductor current (I_L) stays above 0A. After the HS-FET turns on for a calculated t_{ON}, the LS-FET turns on. The LS-FET stays on until I_L reaches zero-current detection (ZCD). Then the LS-FET turns off and enters a high-impedance (Hi-Z) state. When V_{FB} drops below V_{REF}, the HS-FET turns on and stays on for the calculated t_{ON}.

In CCM, I_L can be negative, so the LS-FET stays on due to ZCD. After the HS-FET turns on for a calculated t_{ON}, the LS-FET turns on. When V_{FB} drops below V_{REF}, the HS-FET turns on and stays on for the calculated t_{ON}.

Output Discharge

To discharge the energy of C_{OUT} during the power-off sequence, there is an active discharge path from the bucks and the LDO output to ground. The discharge path turns on when the corresponding channel is disabled. It is recommended to fully discharge all of the outputs before beginning a new start-up sequence.

Diagnostics

The MPQ70240FS integrates several diagnostic features in order to improve system safety. If enabled, several built-in self-test (BIST) functions run in the BIST state before power on sequence begins. These functions are described below.

- Digital interface protocol packet error checking (PEC): Data transferring through the digital interface includes a PEC code. The slave device rejects receiving data if the master device sends an incorrect PEC value (failure). PEC is an optional function that can be selected via the digital interface.
- Analog built-in self-test (ABIST): ABIST ensures that the OV and UV comparators operate normally. If any diagnostic function detects a failure during the power-on state, the PG flag asserts and the corresponding fault bit is set to 1. Once the fault has been cleared, the device restarts all channels according to the power-on sequence. If any diagnostic functions detect a failure during the BIST state, the device restarts BIST at the end of its current BIST, and the end of its current BIST, and the corresponding fault bit is set to 1.
- One-time programmable (OTP) memory cyclic redundancy check (CRC): During the power-off state, and after the non-volatile memory (NVM) is read into the working registers, the CRC code is checked. If the CRC code does not match the previous CRC code, a memory fault is indicated. During the BIST state, the OTP CRC code is checked again. Load the data from the OTP for the CRC calculation. If the CRC code does not match the previous CRC code, a memory fault is indicated, and BIST restarts at the end of the current BIST. During the power-on state, the PMIC can set a continuous OTP CRC check by writing 0x06 to register D9h. If there is an OTP CRC failure, the PG pin is pulled low, and a memory fault is indicated.
- Memory CRC: During BIST, the memory CRC code is checked using CRC-8 (polynomial: $x^8 + x^6 + x^3 + x^2 + 1$), which checks 224 bits, including the user page and trimming page. During start-up, the MPQ70240FS can set a continuous memory CRC by writing 0x05 to register D9h. If there is a memory CRC failure, PG pulls low, and a memory fault is indicated.
- Reference monitor: A second reference continuously monitors the main reference. If the main reference is out of its tolerance window, the PG flag asserts, and the reference fault bit is set to 1. If the reference returns to compliance and the fault register is cleared, the PG flag de-asserts.

Power Good (PG)

The PG pin is a push-pull output that pulls logic high when the device is powered on, all outputs are within the PG range, and no other faults occur. The high output level can be set to either 3.3V or 1.8V.

PG asserts if any of the following occur:

- Buck 1's output is out of its V_{OUT} OVP/UVP threshold
- Buck 2's output is out of its PG range
- Buck 3's output is out of its PG range
- The LDO output is out of its PG range
- Thermal warning/thermal shutdown

- The LDO enters its dropout region
- Over-current (OC) failure
- Reference check failure
- BIST failure
- Digital interface communication failure
- Digital interface CRC failure
- $V_{IN} < V_{IN\_STOP}$
- $V_{CC} < V_{CC\_UVLO\_FALLING}$

These errors force PG to be pulled down. If the error is removed, PG pulls up after a delay. The PG de-assertion delay time is configurable. If PG is pulled down due to a shutdown event, wait until the error is gone and all channels have finished starting, then wait for the PG de-assertion time before PG is pulled up again.

Certain events can be masked (see Table 1). The PG_MAPPING register can determine whether PG is masked for these faults.

Table 1: Maskable Fault Types

Fault Type	PG Asserts?	
	PG Masked	PG Not Masked
BIST failure	No	Yes
Digital interface communication Failure	No	Yes
Digital interface CRC failure	No	Yes

PG does not indicate the output for disabled channels. If SAFETY_CONFIG (CBh), bit[1] = 1, the MPQ70240FS shuts down when PG goes low.

Over-Voltage Protection (OVP)

If any buck's output or the LDO output exceeds the over-voltage protection (OVP) threshold, all outputs shut down at the same time. The MPQ70240FS restarts BIST, and all outputs stay off for a hiccup time after BIST finishes. Then the normal start-up sequence starts again. If enabled, the output discharge function operates during the hiccup time.

Under-Voltage Protection (UVP)

If any buck's output or the LDO output falls below the under-voltage protection (UVP) threshold, all outputs shut down at the same time. The MPQ70240FS restarts BIST, and all outputs stay off for a hiccup time after BIST finishes. Then the normal power-up sequence starts again. If enabled, the output discharge function operates during the hiccup time.

Over-Current Protection (OCP)

For the three bucks, the MPQ70240FS provides a peak/valley current limit (I_{LIMIT}) scheme designed to limit the peak/valley I_L. This ensures that the switching currents remain within the device's capabilities during overload conditions or an output short circuit.

When the HS-FET turns on, the device monitors the increased I_L through the relevant operating main power switch. Once the peak I_L exceeds the peak I_{LIMIT} threshold, the HS-FET turns off immediately, and the LS-FET turns on to conduct and decrease I_L. The HS-FET does not turn on again until I_L falls below the valley I_{LIMIT} threshold. If I_L exceeds the peak I_{LIMIT} during the minimum t_{ON} (t_{ON_MIN}), the HS-FET does not turn off immediately, and it does not turn off until the end of t_{ON_MIN}.

If I_L does not fall below the valley I_{LIMIT} during the off time (the LS-FET turns on), or the peak I_L exceeds I_{LIMIT} during t_{ON} (HS-FET turns on) and lasts longer than the deglitch time, then an OC fault is recorded and OCP is triggered.

For the LDO, an internal, fixed LDO I_{LIMIT} can ensure that the LDO's current remains within the device's capabilities during overload conditions or an output short circuit.

If any channel triggers an OC fault, all outputs shut down at the same time and stay off for the hiccup time. If enabled, the output discharge function operates during shutdown. Then the normal start-up sequence starts again with a configured turn-on delay. Bucks 1, 2, and 3 start according to the set t_{SS}, and the LDO determines the rising rate according to its load and capacitance. If no channel triggers OCP at the end of SS, then the MPQ70240FS resumes normal operation.

Gate Drive Strength Control

To reduce EMI, the MPQ70240FS has four options set via GATE_DRIVE_STRENGTH to adjust the SW1 and SW2 slew rate by adjusting the gate driver ability. EMI can be reduced with a slower SW1 and SW2 slew rate, though this

is a tradeoff that reduces efficiency.

Frequency Spread Spectrum (FSS)

To further optimize EMI performance, the MPQ70240FS features frequency spread spectrum (FSS) (see Figure 5).

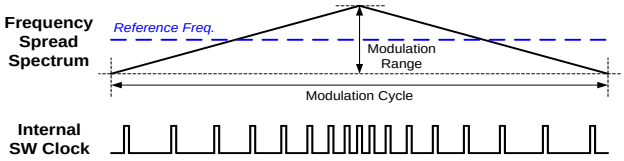


Figure 5: Frequency Spread Spectrum

The reference frequency and FSS modulation range can be set via the digital interface. Once FSS is enabled, the triangular frequency modulation mode varies the switching frequency (f_{SW}) between a same ratio higher and lower than the reference value. f_{SW} varies from the lowest value to its highest value, then drops back to the lowest value within a whole modulation cycle. See the FREQUENCY_DITHER (C4h) section on page 47 for more information.

Thermal Warning and Shutdown

PG asserts low once the silicon die temperature exceeds its upper threshold (about 125°C) and de-asserts until the temperature drops below its lower threshold (about 105°C).

Thermal shutdown is implemented to protect the chip from thermal runaway. If the silicon die temperature exceeds its upper threshold (about 170°C), the device and power MOSFETs shut down. If the temperature drops below its lower threshold (about 150°C), the thermal shutdown condition is removed, and the chip is enabled again.

One-Time Programmable (OTP) Memory

The MPQ70240FS provides an OTP memory function to set custom default parameters.

MPS provides a GUI (Virtual Bench Pro 4.0) and digital interface tool (EVKT-USBI2C-03) to configure the MPQ70240FS during the development process. Contact an MPS FAE to configure in application.

Only the MPQ70240FS-0000 code can be configured via the OTP once. Other codes cannot be configured via the OTP. The OTP can be written once via the STORE_USER_ALL command. See the STORE_USER_ALL (15h) section on page 43 for more details.

POWER CONTROL

Figure 6 shows several states of the MPQ70240FS, and the transition conditions between each state. The state machine's statuses are described below.

No Supply

The PMIC has a UVLO detection circuit. If V_{CC} is below its UVLO rising threshold, all of the MPQ70240FS's functions are disabled.

Power Off

All power rails turn off. When V_{CC} exceeds its UVLO rising threshold, the MPQ70240FS enters a power off state. The digital block is reset and the MPQ70240FS loads its OTP data in the register.

Built-In Self-Test (BIST)

If V_{IN} exceeds the VIN start voltage (V_{IN_START}), the built-in self-test (BIST) is performed. BIST includes analog built-in self-testing (ABIST), OTP CRC calculation, and memory CRC calculation. ABIST consists of a self-check for the PGOV and PGUV comparators. It only includes buck 2, buck 3, and the LDO; buck 1 is not checked. After BIST is finished, the device enters the power-on state once V_{IN} exceeds V_{IN_START}.

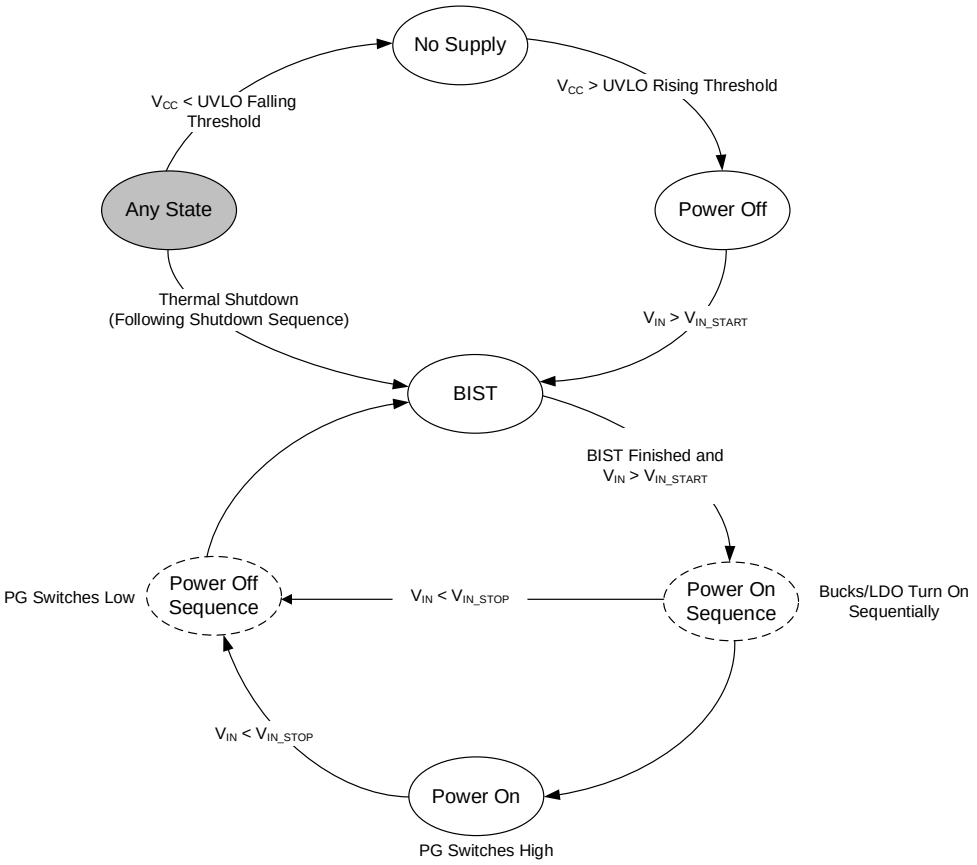


Figure 6: State Machine of the MPQ70240FS

Start-Up Sequence

The start-up delay for the bucks and LDO can be configured via the OTP. Each output turns on after its configured delay time. The bucks and the LDO turn on once their pre-configured on-time delay (ON_DELAY[7:4]) finishes. Buck 3 and the LDO must wait until buck 1 rises to its nominal output, then they begin to start up after a delay time. Figure 7 on page 36 shows the start-up sequence.

The MPQ70240FS has certain requirements for the start-up sequence, which can be divided into the following two cases, according to the different settings for PG_REACTION.

Case 1 (PG_REACTION = 0)

For case 1, PG going low does not force all channels to shut down.

- If (t_{ON_DELAY2} - t_{SS_REDY1}) > PG_DELAY, the PG signal pulls high after (t_{SSREDY_1} + PG_DELAY). Then the PG signal falls after t_{ON_DELAY2}.
- If (t_{ON_DELAY3} - $t_{SSREDY2}$) > PG_DELAY, the PG signal pulls high after (t_{SSREDY_2} + PG_DELAY). Then the PG signal falls after t_{ON_DELAY3}.
- If (t_{ON_DELAY4} - $t_{SSREDY3}$) > PG_DELAY, the PG signal pulls high after (t_{SSREDY_3} + PG_DELAY). Then the PG signal falls after t_{ON_DELAY4}.

Case 2 (PG_REACTION = 1)

For case 2, PG going low can cause all channels to shut down.

- If t_{ON_DELAY2} > $t_{SSREDY1}$, the MPQ70240FS shuts down all channels at the same time at the end of $t_{SSREDY1}$ and enters a BIST state.
- If t_{ON_DELAY3} > $t_{SSREDY2}$, the MPQ70240FS shuts down all channels at the same time at the end of $t_{SSREDY2}$ and enters a BIST state.
- If t_{ON_DELAY3} > $t_{SSREDY4}$, the MPQ70240FS shuts down all channels at the same time at the end of $t_{SSREDY3}$ and enters a BIST state.

If the t_{ON_DELAYx} of the next starting channel is shorter than the $t_{SSREDYx}$ of the previous starting channel, shutdown and PG pulse do not occur during the entire start-up process.

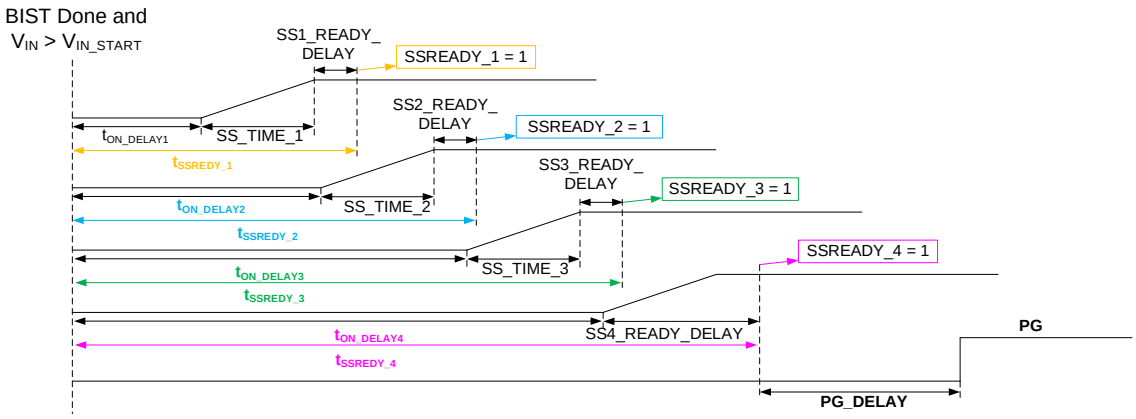


Figure 7: Start-Up Sequence

Power On

In this stage, the bucks and LDO are on. The power good (PG) pin switches high while the outputs are within their defined thresholds.

Power-Off Sequence

The device enters the power-off sequence when it detects that V_{IN} is below V_{IN_STOP} in a power-on state, or during the power-on sequence. The bucks and LDO turn off once the pre-configured off time delay (OFF_DELAY[3:0]) elapses for that output (see Figure 8). If a shutdown event occurs, the bucks and LDO turn off at the same time.

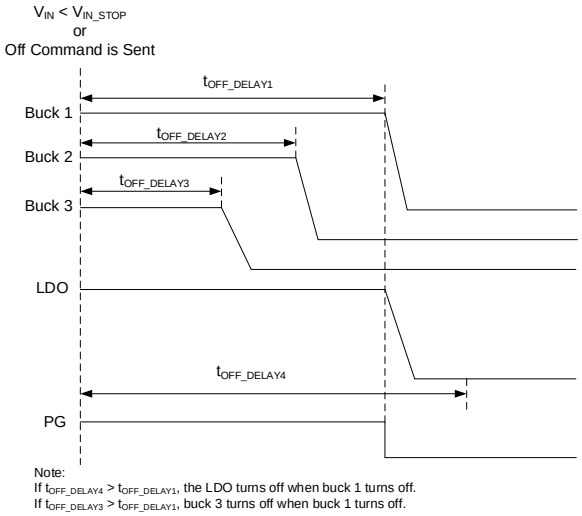


Figure 8: Shutdown Sequence

Shutdown Event

If the device detects a shutdown condition, it shuts down all channels at the same time and changes the current state. Table 2 shows certain shutdown events.

Table 2: Shutdown Event

Fault Type	Result
V_{CC} < UVLO falling threshold	Enter no supply state
V_{IN} < UVLO falling threshold and V_{CC} > UVLO falling threshold	Wait V_{IN} > V_{IN_START} again
Thermal shutdown	Enter BIST state
ABIST fault during BIST	Enter BIST state
OTP CRC fault during BIST	Enter BIST state
Memory CRC fault during BIST	Enter BIST state
V_{OUT} over-voltage (OV) fault	Enter BIST state
V_{OUT} under-voltage (UV) fault	Enter BIST state
Over-current (OC) fault	Enter BIST state
Reference fault	Enter BIST state

If PG_REACTION = 1, there are additional shutdown events when PG goes low (see Table 3).

Table 3: Additional Shutdown Events

Fault Type	Result
V_{OUT} PGOV fault	Enter BIST state
V_{OUT} PGUV fault	Enter BIST state
Digital interface Communication error	Enter BIST state
Digital interface CRC failure	Enter BIST state
Thermal warning	Enter BIST state
LDO enters the dropout range	Enter BIST state

DIGITAL INTERFACE

Digital Serial Interface Description

The digital interface is an open-standard, power-management protocol that defines a means of communication with power conversion and other devices. The digital interface is a 2-wire, bidirectional serial interface, consisting of a serial data line (SDA) and a serial clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address, then arranges the communication sequence.

The MPQ70240FS works as a slave-only device that supports standard mode (100kbps), fast mode (400kbps), and fast mode plus (1Mbps) bidirectional data transfer, adding flexibility to the power supply solution. V_{OUT}, the transition slew rate, and other parameters can be instantaneously controlled via the digital interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the SDA line can only change when the clock signal on the SCL line is low (see Figure 9).

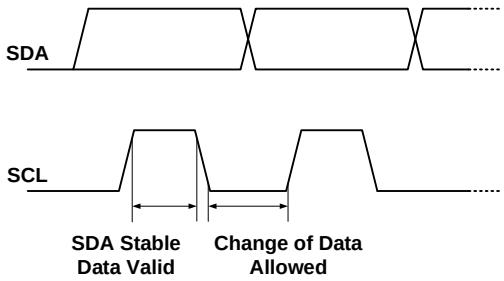


Figure 9: Bit Transfer

Start and Stop Commands

The start (S) and stop (P) commands are signaled by the master device, which signifies the beginning and end of the digital interface transfer. The start command is defined as the SDA signal transitioning from high to low while the SCL line is high. The stop command is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 10).

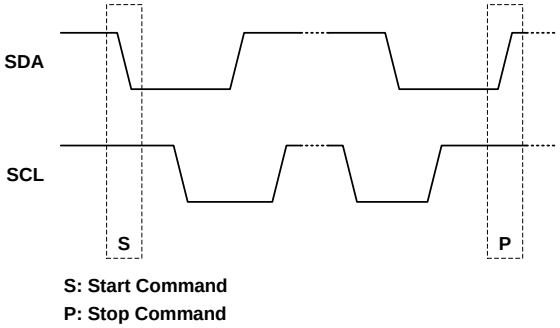


Figure 10: Start and Stop Commands

Start and stop commands are always generated by the master. The bus is considered busy after the start command. The bus is considered free again after a certain time after the stop command. The bus stays busy if a repeated start is generated instead of a stop command. The start and repeated start commands are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the ACK clock pulse. The receiver must pull down the SDA line during the ACK clock pulse, so that it remains stable low during the high period of the clock pulse.

Figure 11 shows the data transfer format. After the start command, a slave address is sent. This address is 7 bits long followed by an eighth bit, which is a data direction bit (R/W). A 0 indicates a transmission (write), while a 1 indicates a request for data (read). A data transfer is terminated by a stop command, which is generated by the master. However, if the master still wishes to communicate on the bus, it can generate a repeated start command and address another slave without first generating a stop command.

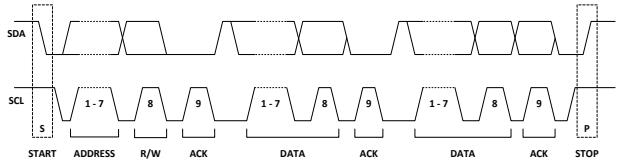


Figure 11: A Complete Data Transfer

Packet Error Checking (PEC)

The packet error checking (PEC) mechanism is employed to improve communication reliability and robustness. When applicable, PEC is implemented by appending a packet error code after the data of each message transfer. The PEC is a CRC-8 error-checking byte (where C(x) = $x^8 + x^2 + x^1 + 1$), calculated on all the message bytes (including addresses and read/write bits). The PEC is appended to the message by the device that supplied the last data byte.

If an incorrect PEC is received, a communication fault is triggered, and the PG flag asserts until the fault register is cleared.

Digital Interface Communication Failure

A data transmission fault occurs when the data is not properly transferred between the devices. There are several data transmission faults, which are listed below:

- Sending too little data
- Reading too little data
- The host sends too many bytes
- The host reads too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

The communication failure is recorded in the STATUS_CML register.

Write/Read Sequence

All digital interface commands are supported by the MPQ70240FS. Figure 12 shows the read/write sequence without PEC. Figure 13 on page 40 shows the write/read sequence with PEC. There are five commands that can be implemented with or without PEC:

1. Send command only
2. Write byte
3. Write word
4. Read byte
5. Read word

If the master sends a write command to a read-only register, the MPQ70240FS performs the same action as it would if the host has sent too many bytes. If the master sends a read command from a write-only register, the MPQ70240FS performs the same action as it would if the host read too many bytes.

Chip Address

The MPQ70240FS supports 16 addresses, which can be set via the ADDRESS register. The default 7-bit address is 03h.

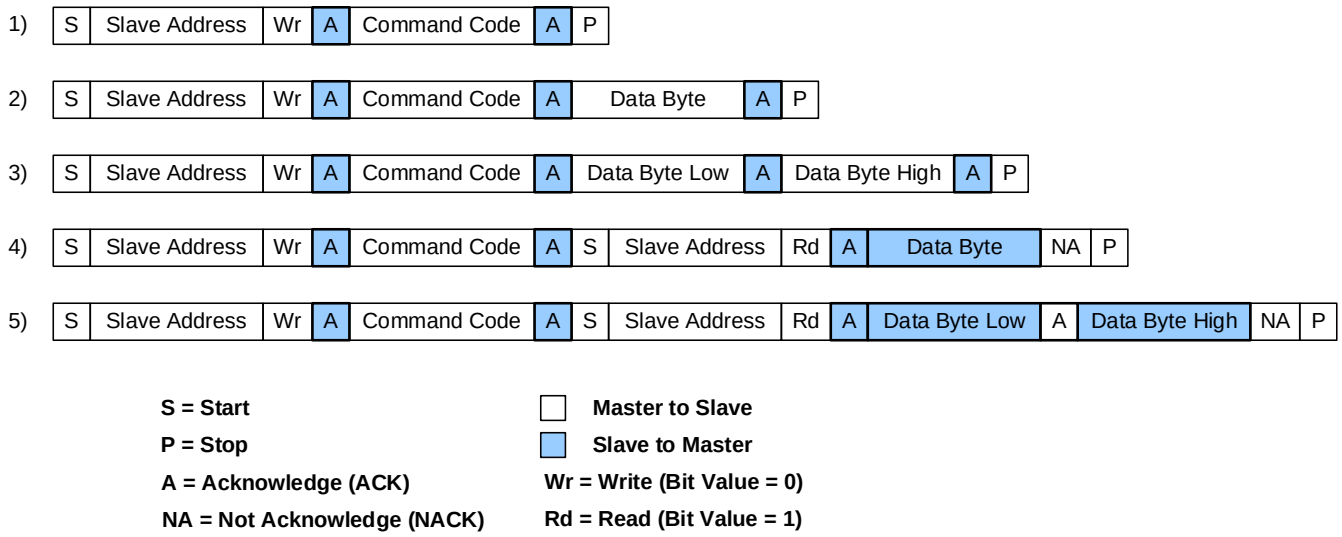


Figure 12: Digital Interface Write/Read Sequence without PEC

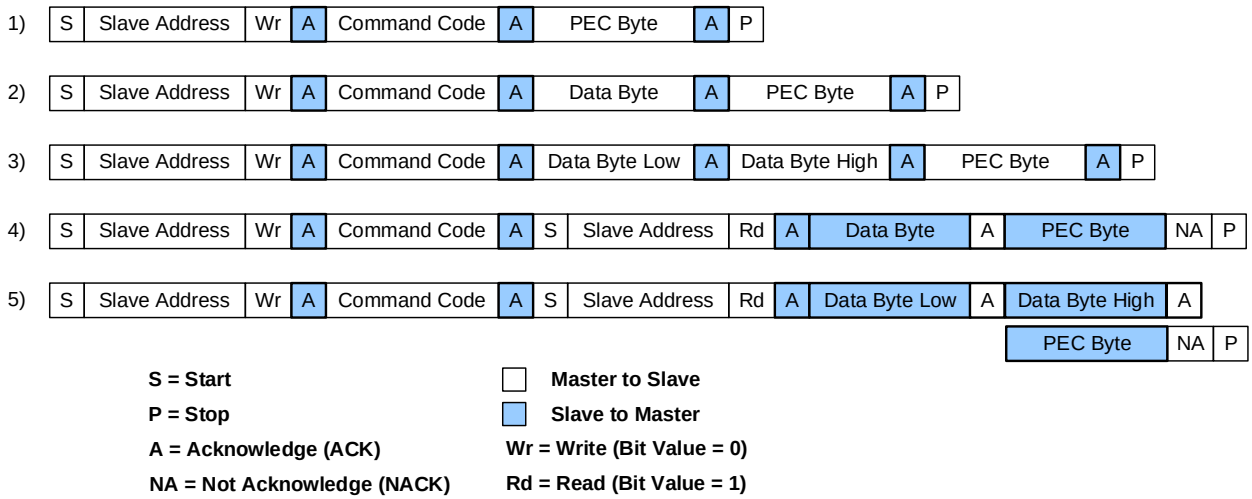


Figure 13: Digital Interface Write/Read Sequence with PEC

REGISTER MAP

Command Code	Command Name	Type	Bytes	Page 0 (Rail 1)	Page 1 (Rail 2)	Page 2 (Rail 3)	Page 3 (Rail 4)	Page FF (All Rails) (11)
00h	PAGE	R/W	1	✓	✓	✓	✓	✓ (12)
01h	OPERATION	R/W	1	✓	✓	✓	✓	✓
03h	CLEAR_FAULTS	Send	0	✓	-	-	-	✓
10h	WRITE_PROTECT	R/W	1	✓	-	-	-	✓
15h	STORE_USER_ALL	Send	0	✓	-	-	-	✓
16h	RESTORE_USER_ALL	Send	0	✓	-	-	-	✓
19h	CAPABILITY	R	1	✓	-	-	-	-
20h	VOUT_MODE	R	1	✓	-	-	-	-
21h	VOUT_COMMAND	R/W	2	✓	✓	✓	✓	✓
61h	TON_RISE	R/W	2	✓	✓	✓	-	✓
78h	STATUS_BYTE	R	1	✓	✓	✓	✓	-
79h	STATUS_WORD	R	2	✓	✓	✓	✓	-
7Ah	STATUS_VOUT	R	1	✓	✓	✓	✓	-
7Bh	STATUS_IOUT	R	1	✓	✓	✓	✓	-
7Dh	STATUS_ TEMPERATURE	R	1	✓	-	-	-	-
7Eh	STATUS_CML	R	1	✓	-	-	-	-
80h	STATUS_MFR_ SPECIFIC	R	1	✓	-	-	-	-
C4h	FREQ_DITHER	R/W	1	✓	-	-	-	✓
C5h	PG_MAPPING	R/W	1	✓	-	-	-	✓
CBh	SAFETY_CONFIG	R/W	1	✓	-	-	-	✓
CCh	PG_CONFIG	R/W	1	✓	-	-	-	✓
CDh	GATE_DRIVE_ STRENGTH	R/W	1	✓	-	-	-	✓
CEh	LIGHT_LOAD	R/W	1	✓	-	-	-	✓
CFh	TON_OFF_DELAY	R/W	1	✓	✓	✓	✓	✓
D0h	TON_OFF_SCALE	R/W	1	✓	-	-	-	✓
D1h	FREQUENCY_ILIM_ SCALE	R/W	1	✓	-	-	-	✓
D2h	VIN_START_STOP	R/W	1	✓	-	-	-	✓
D3h	ADDRESS	R/W	1	✓	-	-	-	✓

REGISTER MAP *(continued)*

Command Code	Command Name	Type	Bytes	Page 0 (Rail 1)	Page 1 (Rail 2)	Page 2 (Rail 3)	Page 3 (Rail 4)	Page FF (All Rails) (11)
D4h	CONFIGURATION_ CODE	R	1	✓	-	-	-	-
D5h	MEMORY_CRC	R	1	✓	-	-	-	-
D6h	LATEST_PEC	R	1	✓	-	-	-	-
D7h	REGISTER_CRC	R	1	✓	-	-	-	-
D9h	MFR_OTP_MEM_CHK	R/W	1	✓	-	-	-	✓
DAh	MFR_OTP_MEM_ STATUS	R	2	✓	-	-	-	-

Note:

11) Read commands are invalid, but write commands are valid.
12) Read and write commands are valid.

PAGE 0 REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command on Page 0 provides the ability to configure, control, and monitor all outputs through only one physical address. All subsequent commands that allow for multi-page actions are applied to the corresponding regulators selected by the PAGE command (00h on Page 0).

Bits	Access	Bit Name	Description
7:0	R/W	PAGE	8'b00000000: V_{OUT1} (Page 0) 8'b00000001: V_{OUT2} (Page 1) 8'b00000002: V_{OUT3} (Page 2) 8'b00000003: LDO (Page 3) 8'b11111111: All rails (Page FF) Others: Ineffective input

OPERATION (01h)

Format: Unsigned binary

The OPERATION command on Page 0 configures buck 1's output on/off state.

Bits	Access	Bit Name	Description
7	R/W	OPERATION	1'b1: The output is on 1'b0: The output is off
6:0	R/W	RESERVED	Reserved.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command on Page 0 clears any fault bits in the following status registers: STATUS_BYTE (78h), STATUS_WORD (79h), STATUS_VOUT (7Ah), STATUS_IOUT (7Bh), STATUS_INPUT (7Ch), STATUS_TEMPERATURE (7Dh), STATUS_CML (7Eh), and STATUS_MFR_SPECIFIC (80h).

This command is write-only. There is no data byte for this command.

WRITE_PROTECT (10h)

Format: Unsigned binary

The WRITE_PROTECT command on Page 0 controls writing to the converter. The intent of this command is to provide protection against accidental changes. It is not intended to provide protection against deliberate changes to the converter's configuration or operation. All the supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Bits	Access	Bit Name	Description
7:0	R/W	WRITE_PROTECT	8'b10000000: Disables all writes except to the WRITE_PROTECT command 8'b 01000000: Disables all writes except to the WRITE_PROTECT, OPERATION, and PAGE commands 8'b 00100000: Disables all writes except to the WRITE_PROTECT, OPERATION, PAGE, and VOUT_COMMAND commands 8'b 00000000: Enables all writes to all commands Others: Ineffective input

STORE_USER_ALL (15h)

The STORE_USER_ALL command on Page 0 instructs the MPQ70240FS to copy the contents from the operating memory to the matching locations in the OTP, excluding the trim registers. This process occurs when the MPQ70240FS receives a STORE_USER_ALL command from the digital interface.

This command is write-only. There is no data byte for this command.

RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command on Page 0 instructs the MPQ70240FS to copy the contents from the OTP and overwrite the matching locations in the operating memory, excluding the trim registers. Any items in the OTP that do not have matching locations in the operating memory are ignored.

The RESTORE_USER_ALL command can be used while the MPQ70240FS is operating; however, the MPQ70240FS may be unresponsive during the operation with unpredictable or undesirable results.

This command is write-only. There is no data byte for this command.

CAPABILITY (19h)

Format: Unsigned binary

The CAPABILITY command on Page 0 provides 1 byte to return the key digital interface features that the MPQ70240FS can support.

Bits	Access	Bit Name	Description
7	R	PACKET_ERR_ CHECKING	1'b1: Packet error checking (PEC) is supported Others: Ineffective input
6:5	R	MAX_BUS_SPEED	2'b10: The maximum supported bus speed is 1MHz Others: Ineffective input
4	R	SMBALERT#	1'b0: The device does not have a SMBALERT# pin and does not support the SMBus alert response protocol Others: Ineffective input
3	R	NUMERIC_FORMAT	1'b0: Numeric data is in LINEAR11, ULINEAR16, SLINEAR16, or DIRECT format Others: Ineffective input
2	R	AVSBUS_SUPPORT	1'b0: The AVSBus is not supported Others: Ineffective input
1:0	R	RESERVED	Reserved.

VOUT_MODE (20h)

Format: Unsigned binary

The VOUT_MODE command on Page 0 commands and reads the output voltage (V_{OUT}) mode. The 3 most significant bits (MSB) are used to determine the data format (only direct format is supported by the MPQ70240FS).

Bits	Access	Bit Name	Description
7:0	R	VOUT_MODE	8'b01000000: Direct mode. The coefficients are m = 2, R = 1, and b = -1.2 Others: Ineffective input

VOUT_COMMAND (21h)

Format: Unsigned binary

The VOUT_COMMAND command on Page 0 sets buck 1's V_{OUT} (V_{OUT1}).

Bits	Access	Bit Name	Description
15:4	R/W	RESERVED	Reserved.
3:0	R/W	VOUT_CMD	V_{OUT1} can be calculated with the following equation: V_{OUT1} = VOUT_CMD x 100mV + 2.5V 2.5V to 4V. 100mV/step.

TON_RISE (61h)

Format: Unsigned binary

The TON_RISE command on Page 0 sets buck 1's soft-start time (t_{SS_BUCK1}).

Bits	Access	Bit Name	Description
15:3	R/W	RESERVED	Reserved.
2:0	R/W	TON_RISE	t_{SS_BUCK1} can be calculated with the following equation: t_{SS_BUCK1} = (TON_RISE + 2) x 0.25ms 0.5ms to 2.25ms.

STATUS_BYTE (78h)

Format: Unsigned binary

The STATUS_BYTE command on Page 0 returns the value of certain flags that indicate the state of the MPQ70240FS.

Bits	Access	Bit Name	Description
7	R	BUSY	1'b0: No busy fault has occurred 1'b1: A fault was declared because the device was busy and unable to respond
6	R	OFF	1'b0: Device is on 1'b1: Device is off
5:3	R	RESERVED	Reserved.
2	R	TEMPERATURE	1'b0: No temperature fault or warning has occurred 1'b1: A temperature fault or warning has occurred
1	R	CML	1'b0: No communications, memory, or logic fault has occurred 1'b1: A communications, memory, or logic fault has occurred
0	R	FAULT_OTHER	1'b0: No other fault has occurred 1'b1: A fault not covered by bits[7:1] of this command has occurred

STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD command on Page 0 returns 2 bytes of information with a summary of the device's fault/warning conditions. The higher bytes return more detailed information of the fault conditions. The lower bytes are the same as what is returned by register STATUS_BYTE (78h).

Bits	Access	Bit Name	Description
15	R	VOUT_FAULT	1'b0: No V_{OUT} fault has occurred 1'b1: An V_{OUT} fault has occurred
14	R	IOUT_OC_FAULT	1'b0: No output current (I_{OUT}) fault has occurred 1'b1: An I_{OUT} fault has occurred
13	R	RESERVED	Reserved.
12	R	MANUFAC_FAULT	1'b0: No manufacturer-specific fault has occurred 1'b1: A manufacturer-specific fault has occurred
11	R	PGOOD	1'b0: PG is high 1'b1: PG is low
10:8	R	RESERVED	Reserved.
Low byte	R	STATUS_BYTE	The same as STATUS_BYTE (78h).

STATUS_VOUT (7Ah)

Format: Unsigned binary

The STATUS_VOUT command on Page 0 returns the value of flags that indicate the device's V_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	VOUT_OV_FAULT	1'b0: No output over-voltage (OV) fault has occurred 1'b1: An output OV fault has occurred
6:5	R	RESERVED	Reserved.
4	R	VOUT_UV_FAULT	1'b0: No output under-voltage (UV) fault has occurred 1'b1: An output UV fault has occurred
3:0	R	RESERVED	Reserved.

STATUS_IOUT (7Bh)

Format: Unsigned binary

The STATUS_IOUT command on Page 0 returns the value of flags indicating the device's I_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	IOUT_OC_FAULT	1'b0: No output over-current (OC) fault has occurred 1'b1: An output OC fault has occurred
6:0	R	RESERVED	Reserved.

STATUS_ TEMPERATURE (7Dh)

Format: Unsigned binary

The STATUS_TEMPERATURE command on Page 0 returns the value of flags that indicate the device's temperature fault status.

Bits	Access	Bit Name	Description
7	R	TEMP_OT_FAULT	1'b0: No over-temperature (OT) fault has occurred 1'b1: An OT fault has occurred
6	R	TEMP_OT_WARNING	1'b0: No OT warning has occurred 1'b1: An OT warning has occurred
5:0	R	RESERVED	Reserved.

STATUS_CML (7Eh)

Format: Unsigned binary

The STATUS_CML command on Page 0 returns the value of flags that indicate the device's communication fault status.

Bits	Access	Bit Name	Description
7	R	INVALID_CMD	1'b0: No invalid or unsupported commands have been received 1'b1: An invalid or unsupported command have been received
6	R	INVALID_DATA	1'b0: No invalid or unsupported data has been received 1'b1: Invalid or unsupported data has been received
5	R	PEC_ERROR	1'b0: The PEC has not failed 1'b1: The PEC has failed
4	R	CRC_ERROR	1'b0: The CRC has not failed 1'b1: The CRC has failed
3:0	R	RESERVED	Reserved.

STATUS_ MFR_SPECIFIC (80h)

Format: Unsigned binary

The STATUS_MFR_SPECIFIC command on Page 0 returns the value of flags indicating the device's fault status.

Bits	Access	Bit Name	Description
7	R	RESERVED	Reserved.
6	R	PGOV_FAULT	1'b0: No PG OV fault has occurred in the buck 2, buck 3, or LDO channel 1'b1: A PG OV fault has occurred in the buck 2, buck 3, or LDO channel
5	R	PGUV_FAULT	1'b0: No PG UV fault has occurred at any channel 1'b1: A PG UV fault has occurred at a channel
4	R	REFERENCE_FAULT	1'b0: No reference fault has occurred 1'b1: A reference fault has occurred
3	R	OTP_CRC_IND_ FAULT	1'b0: No OTP, CRC, or OTP indicator fault has occurred 1'b1: An OTP, CRC, or OTP indicator fault has occurred
2	R	MEM_CRC _FAULT	1'b0: No memory CRC fault has occurred 1'b1: A memory CRC fault has occurred
1	R	ABIST_FAULT	1'b0: No analog built-in self-test (ABIST) fault has occurred 1'b1: An ABIST fault has occurred
0	R	BIST_DONE	1'b0: A built-in self-test (BIST) has not started 1'b1: A BIST has started

FREQUENCY_DITHER (C4h)

Format: Unsigned binary

The FREQUENCY_DITHER command on Page 0 configures the frequency spread spectrum (FSS) parameters.

Bits	Access	Bit Name	Description
7	R/W	FSS_EN	Enables FSS control. 1'b0: Disabled 1'b1: Enabled
6:5	R/W	RESERVED	Reserved.
4	R/W	SSM_RAN	1'b0: ±5% FSS modulation range 1'b1: ±10% FSS modulation range
3:1	R/W	RESERVED	Reserved.
0	R/W	SSM_FRE	1'b0: 4.5kHz FSS modulation frequency 1'b1: 9kHz FSS modulation frequency

PG_MAPPING (C5h)

Format: Unsigned binary

The PG_MAPPING command on Page 0 configures PG mapping for certain faults.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3	R/W	PM_CML_PG#_ MAPPING	Sets the PG mapping for digital interface communication failures. 1'b0: A digital interface communication failure causes PG to go low and register assertion 1'b1: A digital interface communication failure causes register assertion only

2	R/W	PM_CRC_PG#_ MAPPING	Sets the PG mapping for digital interface CRC faults. 1’b0: A digital interface CRC failure causes PG to go low and register assertion 1’b1: A digital interface CRC failure causes register assertion only
1	R/W	REF_FAULT_PG#_ MAPPING	Sets the PG mapping for reference failures. 1’b0: A reference/internal rail failure causes PG to go low and register assertion 1’b1: A reference/internal rail failure causes register assertion only
0	R/W	BIST_FAULT_PG#_ MAPPING	Sets the PG mapping for BIST failures. 1’b0: A BIST failure causes PG to go low and register assertion 1’b1: A BIST failure causes register assertion only

SAFETY_CONFIG (CBh)

Format: Unsigned binary

The SAFETY_CONFIG command on Page 0 configures safety functions.

Bits	Access	Bit Name	Description
7:3	R/W	RESERVED	Reserved.
2	R/W	BIST_EN	Enables BIST. 1’b0: Disabled 1’b1: Enabled
1	R/W	PG_REACTION	Sets the PG pin’s reaction. 1’b0: A PG low fault does not cause a safe state 1’b1: A PG low fault causes a safe state (all outputs turn off)
0	R/W	PEC_REQ	Indicates whether PEC is required. 1’b0: PEC is disabled 1’b1: PEC is optional

PG_CONFIG (CCh)

Format: Unsigned binary

The PG_CONFIG command on Page 0 configures the PG parameters.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3	R/W	PG_OUT	Sets the PG V_{OUT}. 1’b0: 1.8V 1’b1: 3.3V
2:1	R/W	PG_DELAY	Sets the PG de-assertion delay. 2’b00: Immediate 2’b01: 2ms 2’b10: 5ms 2’b11: 10ms
0	R/W	PG_THRESHOLD	Sets the PG threshold. 1’b0: ±4% 1’b1: ±6%

GATE_DRIVE STRENGTH (CDh)

Format: Unsigned binary

The GATE_DRIVE STRENGTH command on Page 0 configures the drive strength for buck 1's and buck 2's low-side (LS)/high-side (HS) gate.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1:0	R/W	GATE_STR	2'b00: Low gate drive strength 2'b01: Medium-low gate drive strength 2'b10: Medium-high gate drive strength 2'b11: High gate drive strength

LIGHT_LOAD (CEh)

Format: Unsigned binary

The LIGHT_LOAD command on Page 0 configures the light-load operation mode and enables the output discharge function.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1	R/W	OUT_DIS	1'b0: Output discharge disabled 1'b1: Output discharge enabled
0	R/W	LIGHT_MODE	1'b0: Continuous conduction mode (CCM) 1'b1: Discontinuous conduction mode (DCM)

TON_OFF_DELAY (CFh)

Format: Unsigned binary

The TON_OFF_DELAY command on Page 0 configures buck 1's turn-off and turn-on times.

Bits	Access	Bit Name	Description
7:4	R/W	ON_DELAY	Sets the turn-on delay, which can be calculated with the following equation: Turn-On Delay = ON_DELAY x DELAY_SCALE Where DELAY_SCALE is between 0ms and 3.75ms, or between 0ms and 37.5ms.
3:0	R/W	OFF_DELAY	Sets the turn-off delay, which can be calculated with the following equation: Turn-Off Delay = OFF_DELAY x DELAY_SCALE Where DELAY_SCALE is between 0ms and 3.75ms, or between 0ms and 37.5ms.

TON_OFF_SCALE (D0h)

Format: Unsigned binary

The TON_OFF_SCALE command on Page 0 configures the scale for the turn-off and turn-on times.

Bits	Access	Bit Name	Description
7:1	R/W	RESERVED	Reserved.
0	R/W	DELAY_SCALE	Sets the delay scale. 1'b0: Scale = 0.25ms. The delay is between 0ms and 3.75ms 1'b1: Scale = 2.5ms. The delay is between 0ms and 37.5ms

FREQUENCY_ILIM_SCALE (D1h)

Format: Unsigned binary

The FREQUENCY_ILIM_SCALE command on Page 0 configures the switching frequency (f_{SW}) and current limit (I_{LIMIT}) for buck 1, buck 2, and buck 3.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1	R/W	FREQUENCY	Sets f_{SW} for buck 1, buck 2, and buck 3. 1'b0: 2.2MHz 1'b1: 3.3MHz
0	R/W	ILIM	Sets I_{LIMIT} for buck 1, buck 2, and buck 3. 1'b0: 100% 1'b1: 125%

VIN_START_STOP (D2h)

Format: Unsigned binary

The VIN_START_STOP command on Page 0 configures the start voltage for VIN (V_{IN_START}) and stop voltage for VIN (V_{IN_STOP}). V_{IN_START} and V_{IN_STOP} must change simultaneously when under-voltage lockout (UVLO) occurs.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3:2	R/W	VIN_START	Sets V_{IN_START}. 2'b00: UVLO threshold 2'b01: 4V 2'b10: 5V 2'b11: 6V
1:0	R/W	VIN_STOP	Sets V_{IN_STOP}. 2'b00: UVLO threshold 2'b01: 3.5V 2'b10: 4.5V 2'b11: 5.5V

ADDRESS (D3h)

Format: Unsigned binary

The ADDRESS command on Page 0 sets the digital interface communication address.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3:0	R/W	ADDRESS	Sets 4 bits of the digital interface address.

CONFIGURATION_CODE (D4h)

Format: Unsigned binary

The CONFIGURATION_CODE command on Page 0 returns information regarding the configuration code.

Bits	Access	Bit Name	Description
7:4	R	RESERVED	Reserved.
3:0	R	CONFIG_CODE	Sets the OTP configuration code at shipment.

MEMORY_CRC (D5h)

Format: Unsigned binary

The MEMORY_CRC command on Page 0 stores the CRC code for all of the OTP.

Bits	Access	Bit Name	Description
7:0	R	MEMORY_CRC	Stores CRC of all OTP. Checked at startup and after writing.

LATEST_PEC (D6h)

Format: Unsigned binary

The LATEST_PEC command on Page 0 stores the latest calculated packet error code from the previous write transition.

Bits	Access	Bit Name	Description
7:0	R	LATEST_PEC	Stores the latest calculated packet error code from the previous write transition.

REGISTER _CRC (D7h)

Format: Unsigned binary

The REGISTER_CRC command on Page 0 stores the CRC code for all of the registers.

Bits	Access	Bit Name	Description
7:0	R	REGISTER_CRC	Stores the CRC code for all of the registers.

MFR_OTP_MEM_CHK (D9h)

Format: Unsigned binary

The MFR_OTP_MEM_CHK command on Page 0 configures the memory and OTP check.

Bits	Access	Bit Name	Description
7:3	R/W	RESERVED	Reserved.
2	R/W	MFR_OTP_MEM_CHK	Selects the memory and OTP check mode. 1’b1: Continuously check after OTP_CHK_EN and MEM_CHK_EN are set to 1 1’b0: Check once after OTP_CHK_EN and MEM_CHK_EN generate a posedge
1	R/W	MFR_OTP_CRC_CHK_EN	Enables or disables OTP CRC check. 1’b1: Enabled 0’b1: Disabled
0	R/W	MFR_MEM_CRC_CHK_EN	Enables or disables memory CRC check. 1’b1: Enabled 0’b1: Disabled

MFR_OTP_MEM_STATUS (DAh)

Format: Unsigned binary

The MFR_OTP_MEM_STATUS command on Page 0 returns the value of certain flags that indicate the device’s fault status.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Reserved.
9	R	PAGE3_WRITE_CHK_ERR	1’b0: No Page 3 write check error has occurred 1’b1: A Page 3 write check error has occurred

8	R	PAGE2_WRITE_CHK_ERR	1’b0: No Page 2 write check error has occurred 1’b1: A Page 2 write check error has occurred
7	R	PAGE1_WRITE_CHK_ERR	1’b0: No Page 1 write check error has occurred 1’b1: A Page 1 write check error has occurred
6	R	PAGE0_WRITE_CHK_ERR	1’b0: No Page 0 write check error has occurred 1’b1: A Page 0 write check error has occurred
5	R	STRUP_OTP_CRC_ERR	1’b0: No start-up load OTP CRC error has occurred 1’b1: A start-up load OTP CRC error has occurred
4	R	STRUP_OTP_IND_ERR	1’b0: No start-up load OTP indicator error has occurred 1’b1: A start-up load OTP indicator error has occurred
3	R	STORE_OTP_ERR	1’b0: No store OTP failure has occurred 1’b1: A store OTP failure has occurred
2	R	BIST_CHK_MEM_CRC_ERR	1’b0: No BIST check memory CRC error has occurred 1’b1: A BIST check memory CRC error has occurred
1	R	BIST_CHK_OTP_CRC_ERR	1’b0: No BIST check OTP CRC error has occurred 1’b1: A BIST check OTP CRC error has occurred
0	R	BIST_CHK_MEM_IND_ERR	1’b0: No BIST check OTP indicator error has occurred 1’b1: A BIST check OTP indicator error has occurred
8	R	PAGE2_WRITE_CHK_ERR	1’b0: No Page 0 write check error has occurred 1’b1: A Page 0 write check error has occurred
7	R	PAGE1_WRITE_CHK_ERR	1’b0: No start-up load OTP CRC error has occurred 1’b1: A start-up load OTP CRC error has occurred

PAGE 1 REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command on Page 1 provides the ability to configure, control, and monitor all outputs through only one physical address. All subsequent commands that allow for multi-page actions are applied to the corresponding regulators selected by the PAGE command (00h on Page 0).

Bits	Access	Bit Name	Description
7:0	R/W	PAGE	8'b00000000: V_{OUT1} (Page 0) 8'b00000001: V_{OUT2} (Page 1) 8'b00000002: V_{OUT3} (Page 2) 8'b00000003: LDO (Page 3) 8'b11111111: All rails (Page FF) Others: Ineffective input

OPERATION (01h)

Format: Unsigned binary

The OPERATION command on Page 1 configures buck 2's output on/off state.

Bits	Access	Bit Name	Description
7	R/W	OPERATION	1'b1: The output is on 1'b0: The output is off
6:0	R/W	RESERVED	Reserved.

VOUT_COMMAND (21h)

Format: Unsigned binary

The VOUT_COMMAND command on Page 1 sets buck 2's V_{OUT} (V_{OUT2}).

Bits	Access	Bit Name	Description
15:6	R/W	RESERVED	Reserved.
5:0	R/W	VOUT_CMD	V_{OUT2} can be calculated with the following equation: V_{OUT2} = VOUT_CMD x 50mV + 0.6V 0.6V to 3.75V. 50mV/step.

TON_RISE (61h)

Format: Unsigned binary

The TON_RISE command on Page 1 sets buck 2's soft-start time (t_{SS_BUCK2}).

Bits	Access	Bit Name	Description
15:3	R/W	RESERVED	Reserved.
2:0	R/W	TON_RISE	t_{SS_BUCK2} can be calculated with the following equation: t_{SS_BUCK2} = (TON_RISE + 2) x 0.25ms 0.5ms to 2.25ms.

STATUS_BYTE (78h)

Format: Unsigned binary

The STATUS_BYTE command on Page 1 returns the value of the flags that indicate the state of the MPQ70240FS.

Bits	Access	Bit Name	Description
7	R	BUSY	1'b0: No busy fault 1'b1: A fault was declared because the device was busy and unable to respond
6	R	OFF	1'b0: Device is on 1'b1: Device is off
5:3	R	RESERVED	Reserved.
2	R	TEMPERATURE	1'b0: No temperature fault or warning has occurred 1'b1: A temperature fault or warning has occurred
1	R	CML	1'b0: No communications, memory, or logic fault has occurred 1'b1: A communications, memory, or logic fault has occurred
0	R	FAULT_OTHER	1'b0: No other fault has occurred 1'b1: A fault not covered by bits[7:1] of this command has occurred

STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD command on Page 1 returns 2 bytes of information with a summary of the device's fault/warning conditions. The higher bytes return more detailed information of the fault conditions. The lower bytes are the same as what is returned by register STATUS_BYTE (78h).

Bits	Access	Bit Name	Description
15	R	VOUT_FAULT	1'b0: No V_{OUT} fault has occurred 1'b1: An V_{OUT} fault has occurred
14	R	IOUT_OC_FAULT	1'b0: No I_{OUT} fault has occurred 1'b1: An I_{OUT} fault has occurred
13	R	RESERVED	Reserved.
12	R	MANUFAC_FAULT	1'b0: No manufacturer-specific fault has occurred 1'b1: A manufacturer-specific fault has occurred
11	R	PGOOD	1'b0: PG is high 1'b1: PG is low
10:8	R	RESERVED	Reserved.
Low byte	R	STATUS_BYTE	The same as STATUS_BYTE (78h).

STATUS_VOUT (7Ah)

Format: Unsigned binary

The STATUS_VOUT command on Page 1 returns the value of flags that indicate the device's V_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	VOUT_OV_FAULT	1'b0: No output OV fault has occurred 1'b1: An output OV fault has occurred
6:5	R	RESERVED	Reserved.

4	R	VOUT_UV_FAULT	1’b0: No output UV fault has occurred 1’b1: An output UV fault has occurred
3:0	R	RESERVED	Reserved.

STATUS_IOUT (7Bh)

Format: Unsigned binary

The STATUS_IOUT command on Page 1 returns the value of flags indicating the device’s I_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	IOUT_OC_FAULT	1’b0: No output OC fault has occurred 1’b1: An output OC fault has occurred
6:0	R	RESERVED	Reserved.

TON_OFF_DELAY (CFh)

Format: Unsigned binary

The TON_OFF_DELAY command on Page 1 configures buck 2’s turn-off and turn-on times.

Bits	Access	Bit Name	Description
7:4	R/W	ON_DELAY	Sets the turn-on delay, which can be calculated with the following equation: Turn-On Delay = ON_DELAY x DELAY_SCALE Where DELAY_SCALE is between 0ms and 3.75ms, or between 0ms and 37.5ms.
3:0	R/W	OFF_DELAY	Sets the turn-off delay, calculated with the following equation: Turn-Off Delay = OFF_DELAY x DELAY_SCALE Where DELAY_SCALE is between 0ms and 3.75ms, or between 0ms and 37.5ms.

PAGE 2 REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command on Page 2 provides the ability to configure, control, and monitor all outputs through only one physical address. All subsequent commands that allow for multi-page actions are applied to the corresponding regulators selected by the PAGE command (00h on Page 0).

Bits	Access	Bit Name	Description
7:0	R/W	PAGE	8'b00000000: V_{OUT1} (Page 0) 8'b00000001: V_{OUT2} (Page 1) 8'b00000002: V_{OUT3} (Page 2) 8'b00000003: LDO (Page 3) 8'b11111111: All rails (Page FF) Others: Ineffective input

OPERATION (01h)

Format: Unsigned binary

The OPERATION command on Page 2 configures buck 3's output on/off state.

Bits	Access	Bit Name	Description
7	R/W	OPERATION	1'b1: The output is on 1'b0: The output is off
6:0	R/W	RESERVED	Reserved.

VOUT_COMMAND (21h)

Format: Unsigned binary

The VOUT_COMMAND command on Page 2 sets buck 3's V_{OUT} (V_{OUT3}).

Bits	Access	Bit Name	Description
15:6	R/W	RESERVED	Reserved.
5:0	R/W	VOUT_CMD	V_{OUT3} can be calculated with the following equation: V_{OUT3} = VOUT_CMD x 50mV + 0.6V 0.6V to 2.55V. This value is clamped to 2.55V when V_{OUT3} is set to exceed 2.55V. 50mV/step.

TON_RISE (61h)

Format: Unsigned binary

The TON_RISE command on Page 2 sets buck 3's soft-start time (t_{SS_BUCK3}).

Bits	Access	Bit Name	Description
15:3	R/W	RESERVED	Reserved.
2:0	R/W	TON_RISE	t_{SS_BUCK3} can be calculated with the following equation: t_{SS_BUCK3} = (TON_RISE + 2) x 0.25ms 0.5ms to 2.25ms.

STATUS_BYTE (78h)

Format: Unsigned binary

The STATUS_BYTE command on Page 2 returns the value of flags that indicate the state of the MPQ70240FS.

Bits	Access	Bit Name	Description
7	R	BUSY	1'b0: No busy fault 1'b1: A fault was declared because the device was busy and unable to respond
6	R	OFF	1'b0: Device is on 1'b1: Device is off
5:3	R	RESERVED	Reserved.
2	R	TEMPERATURE	1'b0: No temperature fault or warning has occurred 1'b1: A temperature fault or warning has occurred
1	R	CML	1'b0: No communications, memory, or logic fault has occurred 1'b1: A communications, memory, or logic fault has occurred
0	R	FAULT_OTHER	1'b0: No other fault has occurred 1'b1: A fault not covered by bits[7:1] of this command has occurred

STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD command on Page 2 returns 2 bytes of information with a summary of the device's fault/warning conditions. The higher bytes return more detailed information of the fault conditions. The lower bytes are the same as what is returned by register STATUS_BYTE (78h).

Bits	Access	Bit Name	Description
15	R	VOUT_FAULT	1'b0: No V_{OUT} fault has occurred 1'b1: An V_{OUT} fault has occurred
14	R	IOUT_OC_FAULT	1'b0: No output current (I_{OUT}) fault has occurred 1'b1: An I_{OUT} fault has occurred
13	R	RESERVED	Reserved.
12	R	MANUFAC_FAULT	1'b0: No manufacturer-specific fault has occurred 1'b1: A manufacturer-specific fault has occurred
11	R	PGOOD	1'b0: PG is high 1'b1: PG is low
10:8	R	RESERVED	Reserved.
Low byte	R	STATUS_BYTE	The same as STATUS_BYTE (78h).

STATUS_VOUT (7Ah)

Format: Unsigned binary

The STATUS_VOUT command on Page 2 returns the value of flags that indicate the device's V_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	VOUT_OV_FAULT	1'b0: No output OV fault has occurred 1'b1: An output OV fault has occurred
6:5	R	RESERVED	Reserved.
4	R	VOUT_UV_FAULT	1'b0: No output UV fault has occurred 1'b1: An output UV fault has occurred

3:0	R	RESERVED	Reserved.

STATUS_IOUT (7Bh)

Format: Unsigned binary

The STATUS_IOUT command on Page 2 returns the value of flags indicating the device's I_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	IOUT_OC_FAULT	1'b0: No output over-current (OC) fault has occurred 1'b1: An output OC fault has occurred
6:0	R	RESERVED	Reserved.

TON_OFF_DELAY (CFh)

Format: Unsigned binary

The TON_OFF_DELAY command on Page 2 configures buck 3's turn-off and turn-on times.

Bits	Access	Bit Name	Description
7:4	R/W	ON_DELAY	Sets the turn-on delay, which can be calculated with the following equation: Turn-On Delay = ON_DELAY x DELAY_SCALE Where DELAY_SCALE is between 0ms and 3.75, or between 0ms and 37.5ms.
3:0	R/W	OFF_DELAY	Sets the turn-off delay, calculated with the following equation: Turn-Off Delay = OFF_DELAY x DELAY_SCALE Where DELAY_SCALE is between 0ms and 3.75, or between 0ms and 37.5ms.

PAGE 3 REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command on Page 3 provides the ability to configure, control, and monitor all outputs through only one physical address. All subsequent commands that allow for multi-page actions are applied to the corresponding regulators selected by the PAGE (00h on Page 0) command.

Bits	Access	Bit Name	Description
7:0	R/W	PAGE	8'b00000000: V_{OUT1} (Page 0) 8'b00000001: V_{OUT2} (Page 1) 8'b00000002: V_{OUT3} (Page 2) 8'b00000003: LDO (Page 3) 8'b11111111: All rails (Page FF) Others: Ineffective input

OPERATION (01h)

Format: Unsigned binary

The OPERATION command on Page 3 is used to configure LDO's output on/off state.

Bits	Access	Bit Name	Description
7	R/W	OPERATION	1'b1: Output on 1'b0: Output off
6:0	R/W	RESERVED	Reserved.

VOUT_COMMAND (21h)

Format: Unsigned binary

The VOUT_COMMAND command on Page 3 sets the LDO's V_{OUT} (V_{LDOOUT}).

Bits	Access	Bit Name	Description
15:6	R/W	RESERVED	Reserved.
5:0	R/W	VOUT_CMD	V_{LDOOUT} can be calculated with the following equation: V_{LDOOUT} = VOUT_CMD x 50mV + 0.6V 0.6V to 3.75V. 50mV/step.

STATUS_BYTE (78h)

Format: Unsigned binary

The STATUS_BYTE command on Page 3 returns the value of flags that indicate the state of the MPQ70240FS.

Bits	Access	Bit Name	Description
7	R	BUSY	1'b0: No busy fault 1'b1: A fault was declared because the device was busy and unable to respond
6	R	OFF	1'b0: Device is on 1'b1: Device is off
5:3	R	RESERVED	Reserved.
2	R	TEMPERATURE	1'b0: No temperature fault or warning has occurred 1'b1: A temperature fault or warning has occurred
1	R	CML	1'b0: No communications, memory, or logic fault has occurred 1'b1: A communications, memory, or logic fault has occurred

0	R	FAULT_OTHER	1'b0: No other fault has occurred 1'b1: A fault not covered by bits[7:1] of this command has occurred

STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD command on Page 3 returns 2 bytes of information with a summary of the device's fault/warning conditions. The higher bytes return more detailed information of the fault conditions. The lower bytes are the same as what is returned by register STATUS_BYTE (78h).

Bits	Access	Bit Name	Description
15	R	VOUT_FAULT	1'b0: No V_{OUT} fault has occurred 1'b1: An V_{OUT} fault has occurred
14	R	IOUT_OC_FAULT	1'b0: No I_{OUT} fault has occurred 1'b1: An I_{OUT} fault has occurred
13	R	RESERVED	Reserved.
12	R	MANUFAC_FAULT	1'b0: No manufacturer-specific fault has occurred 1'b1: A manufacturer-specific fault has occurred
11	R	PGOOD	1'b0: PG is high 1'b1: PG is low
10:8	R	RESERVED	Reserved.
Low byte	R	STATUS_BYTE	The same as STATUS_BYTE (78h).

STATUS_VOUT (7Ah)

Format: Unsigned binary

The STATUS_VOUT command on Page 3 returns the value of flags that indicate the device's V_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	VOUT_OV_FAULT	1'b0: No output over-voltage (OV) fault has occurred 1'b1: An output OV fault has occurred
6:5	R	RESERVED	Reserved.
4	R	VOUT_UV_FAULT	1'b0: No output under-voltage (UV) fault has occurred 1'b1: An output UV fault has occurred
3:0	R	RESERVED	Reserved.

STATUS_IOUT (7Bh)

Format: Unsigned binary

The STATUS_IOUT command on Page 3 returns the value of flags indicating the device's I_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	IOUT_OC_FAULT	1'b0: No output OC fault has occurred 1'b1: An output OC fault has occurred
6:0	R	RESERVED	Reserved.

TON_OFF_DELAY (CFh)

Format: Unsigned binary

The TON_OFF_DELAY command configure turn off and turn on time for LDO.

Bits	Access	Bit Name	Description
7:4	R/W	ON_DELAY	Sets the turn-on delay, which can be calculated with the following equation: Turn-On Delay = ON_DELAY x DELAY_SCALE Where DELAY_SCALE can be between 0ms and 3.75ms, or between 0ms and 37.5ms.
3:0	R/W	OFF_DELAY	Sets the turn-off delay, which can be calculated with the following equation: Turn-Off Delay = OFF_DELAY x DELAY_SCALE Where DELAY_SCALE can be between 0ms and 3.75ms, or between 0ms and 37.5ms.

PAGE FF REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command provides the ability to configure, control, and monitor all outputs through only one physical address. All subsequent commands that allows multipage action are applied to the corresponding regulators selected by the PAGE command.

Bits	Access	Bit Name	Description
7:0	R/W	PAGE	8'b00000000: V_{OUT1} (Page 0) 8'b00000001: V_{OUT2} (Page 1) 8'b00000002: V_{OUT3} (Page 2) 8'b00000003: V_{LDOOUT} (Page 3) 8'b11111111: All rails (Page FF) Others: Ineffective input

OPERATION (01h)

Format: Unsigned binary

The OPERATION command is used to configure the output on/off state of the converter.

Bits	Access	Bit Name	Description
7	R/W	OPERATION	1'b1: Output on 1'b0: Output off
6:0	R/W	RESERVED	Reserved.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear any fault bit in all status registers: STATUS_BYTE (78h), STATUS_WORD (79h), STATUS_VOUT (7Ah), STATUS_IOUT (7Bh), STATUS_INPUT (7Ch), STATUS_TEMPERATURE (7Dh), STATUS_CML (7Eh), and STATUS_MFR_SPECIFIC (80h).

This command is write-only. There is no data byte for this command.

WRITE_PROTECT (10h)

Format: Unsigned binary

The WRITE_PROTECT command is used to control writing to the converter. The intent of this command is to provide protection against accident changes. It's not intended to provide protection against deliberate or malicious changes to the converter's configuration or operation. All the supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Bits	Access	Bit Name	Description
7:0	R/W	WRITE_PROTECT	8'b10000000: Disable all writes except to the WRITE_PROTECT command 8'b 01000000: Disable all writes except to the WRITE_PROTECT, OPERATION and PAGE commands 8'b 00100000: Disable all writes except to the WRITE_PROTECT, OPERATION, PAGE and VOUT_COMMAND commands 8'b 00000000: Enable writes to all commands Others: Ineffective input

STORE_USER_ALL (15h)

The STORE_USER_ALL command instructs the part to copy the contents of the operating memory to the matching locations in the OTP, except the internal trim registers. This process will operate when MPQ70240FS receives a STORE_USER_ALL command from the digital interface.

This command is write-only . There is no data byte for this command.

RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command instructs the MPQ70240FS to copy the contents from the OTP and overwrite the matching locations in the operating memory. Trim registers are not overwritten by this process. Any items in OTP that do not have matching locations in the operating memory are ignored.

It is permitted to use the RESTORE_USER_ALL command while the part is operating. However, the MPQ70240FS may be unresponsive during the operation with unpredictable, undesirable, or even catastrophic results.

This command is write-only. There is no data byte for this command.

VOUT_COMMAND (21h)

Format: Unsigned binary

The VOUT_COMMAND command sets the MPQ70240FS's V_{OUT}.

Bits	Access	Bit Name	Description
15:6	R/W	RESERVED	Reserved.
5:0	R/W	VOUT_CMD	V_{OUT1} = Bit [3:0] x 100mV + 2.5V, 2.5V to 4V, 100mV/step V_{OUT2} = Bit [5:0] x 50mV + 0.6V, 0.6V to 3.75V, 50mV/step V_{OUT3} = Bit [5:0] x 50mV + 0.6V, 0.6V to 2.55V(will be clamped to 2.55V when V_{OUT3} set higher than 2.55V), 50mV/step V_{LDOOUT} = Bit [5:0] x 50mV + 0.6V, 0.6V to 3.75V, 50mV/step

TON_RISE (61h) (13)

Format: Unsigned binary

The TON_RISE command sets the MPQ70240FS's channels soft start (SS) rising time.

Bits	Access	Bit Name	Description
15:3	R/W	RESERVED	Reserved.
2:0	R/W	TON_RISE	SS = (TON_RISE[2:0] + 2) x 0.25ms(0.5 - 2.25ms)

Note:

13) Writing to this register is not valid for Page 3 (LDO rail).

FREQUENCY_DITHER (C4h)

Format: Unsigned binary

The FREQUENCY_DITHER command can configure FSS with different parameters.

Bits	Access	Bit Name	Description
7	R/W	FSS_EN	FSS control. 1'b0: Disabled 1'b1: Enabled
6:5	R/W	RESERVED	Reserved.
4	R/W	SSM_RAN	1'b0: ±5% FSS modulation range 1'b1: ±10% FSS modulation range
3:1	R/W	RESERVED	Reserved.
0	R/W	SSM_FRE	1'b0: 4.5kHz FSS modulation frequency 1'b1: 9kHz FSS modulation frequency

PG_MAPPING (C5h)

Format: Unsigned binary

The PG_MAPPING command configures power good (PG) mapping for the below faults.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3	R/W	PM_CML_PG#_ MAPPING	Digital interface communication PG mapping. 1'b0: Digital interface communication failure causes PG low and register assertion 1'b1: Digital interface communication failure causes register assertion only
2	R/W	PM_CRC_PG#_ MAPPING	Digital interface cyclic redundancy check (CRC) PG mapping. 1'b0: Digital interface CRC Failure causes PG low & register assertion 1'b1: Digital interface CRC Failure cause register assertion only
1	R/W	REF_FAULT_PG#_ MAPPING	Reference failure PG mapping. 1'b0:Reference/Internal Rail Failure causes PG low & register assertion 1'b1:Reference/Internal Rail Failure cause register assertion only
0	R/W	BIST_FAULT_PG#_ MAPPING	BIST failure PG mapping. 1'b0:BIST Failure causes PG low & register assertion 1'b1:BIST Failure cause register assertion only

SAFETY_CONFIG (CBh)

Format: Unsigned binary

The SAFETY_CONFIG command configures the safety relationship function.

Bits	Access	Bit Name	Description
7:3	R/W	RESERVED	Reserved.
2	R/W	BIST_EN	BIST enable. 1'b0: BIST Disabled 1'b1: BIST Enabled
1	R/W	PG_REACTION	PG reaction. 1'b0: PG low fault does not move to safe state 1'b1: PG low fault causes safe state (all outputs off)
0	R/W	PEC_REQ	PEC required. 1'b0: PEC Disabled 1'b1: PEC Optional

PG_CONFIG (CCh)

Format: Unsigned binary

The PG_CONFIG command configure the PG parameters.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3	R/W	PG_OUT	PG V_{OUT}. 1'b0: 1.8V 1'b1: 3.3V

2:1	R/W	PG_Delay	PG de-assertion delay. 2'b00: Immediate 2'b01: 2ms 2'b10: 5ms 2'b11: 10ms
0	R/W	PG_THRESHOLD	PG threshold. 1'b0: ±4% 1'b1: ±6%

GATE_DRIVE STRENGTH (CDh)

Format: Unsigned binary

The GATE_DRIVE STRENGTH command configures the drive strength for buck 3's LS/HS gate.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1:0	R/W	GATE_STR	2'b00: Low gate drive strength 2'b01: Medium-low gate drive strength 2'b10: Medium-high gate drive strength 2'b11: High gate drive strength

LIGHT_LOAD (CEh)

Format: Unsigned binary

The LIGHT_LOAD command configures the light-load operation mode and output discharge.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1	R/W	OUT_DIS	1'b0: Output discharge disabled 1'b1: Output discharge enabled
0	R/W	LIGHT_MODE	1'b0: CCM 1'b1: DCM

TON_OFF_DELAY (CFh)

Format: Unsigned binary

The TON_OFF_DELAY command configures the turn-off and turn-on times for all channels.

Bits	Access	Bit Name	Description
7:4	R/W	ON_DELAY	Turn on delay = ON_DELAY [7:4] x Scale. (0 - 3.75ms / 0 - 37.5ms)
3:0	R/W	OFF_DELAY	Turn off delay = OFF_DELAY [3:0] x Scale. (0 - 3.75ms / 0 - 37.5ms)

TON_OFF_SCALE (D0h)

Format: Unsigned binary

The TON_OFF_SCALE command configures the scale of the turn-off and turn-on times.

Bits	Access	Bit Name	Description
7:1	R/W	RESERVED	Reserved.
0	R/W	DELAY_SCALE	Delay scale. 1'b0: Scale = 0.25ms. Delay ranges from 0ms to 3.75ms 1'b1: Scale = 2.5ms. Delay ranges from 0ms to 37.5ms

FREQUENCY_ILIM_SCALE (D1h)

Format: Unsigned binary

The FREQUENCY_ILIM_SCALE command configured f_{SW} and the I_{LIMIT} for buck 1, buck 2, and buck 3.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1	R/W	FREQUENCY	f_{SW} setting. 1'b0: 2.2MHz 1'b1: 3.3MHz
0	R/W	ILIM	I_{LIMIT} setting. 1'b0: 100% 1'b1: 125%

VIN_START_STOP (D2h)

Format: Unsigned binary

The VIN_START_STOP command configures the V_{IN_START} and V_{IN_STOP}. (14)

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3:2	R/W	VIN_START	V_{IN_START} setting. 2'b00: UVLO 2'b01: 4V 2'b10: 5V 2'b11: 6V
1:0	R/W	VIN_STOP	V_{IN_STOP} setting. 2'b00: UVLO 2'b01: 3.5V 2'b10: 4.5V 2'b11: 5.5V

Note:

14) V_{IN_START} and V_{IN_STOP} must be changed simultaneously when VIN_START or VIN_STOP during UVLO.

ADDRESS (D3h)

Format: Unsigned binary

The ADDRESS command sets the digital interface communication address.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3:0	R/W	ADDRESS	4-bit digital interface address.

MFR_OTP_MEM_CHK (D9h)

Format: Unsigned binary

The MFR_OTP_MEM_CHK command configures the memory and OTP check.

Bits	Access	Bit Name	Description
7:3	R/W	RESERVED	Reserved.
2	R/W	MFR_OTP_MEM_CHK	Memory and OTP check mode selection. 1'b1: Continuously check after OTP_CHK_EN and MEM_CHK_EN are set 1 1'b0: Check once after OTP_CHK_EN and MEM_CHK_EN generate a posedge
1	R/W	MFR_OTP_CRC_CHK_EN	OTP check enable.
0	R/W	MFR_MEM_CRC_CHK_EN	Memory check enable.

APPLICATION INFORMATION

Figure 14 shows the MPQ70240FS's typical application circuit.

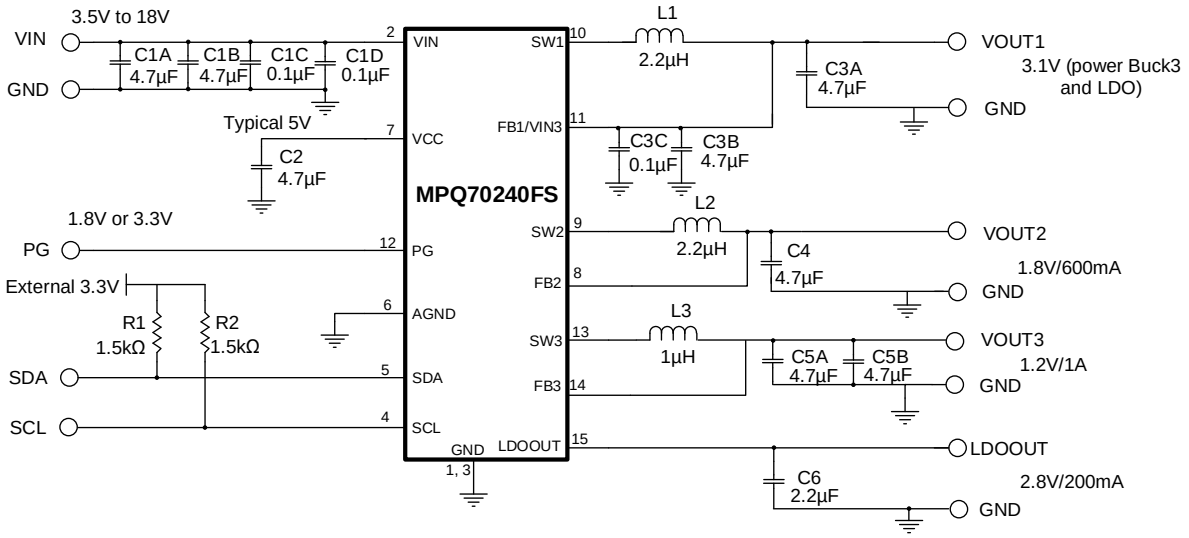


Figure 14: Typical Application Circuit (V_{OUT1} = 3.1V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.8V)

Table 4: Design Guide Index

Pin #	Pin Name	Component	Design Guide Index
1, 3	GND	-	GND Connection (GND, Pins 1 and 3; AGND, Pin 6)
2	VIN	C1A, C1B, C1C, C1D	Selecting the Input Capacitors (VIN, Pin 2; VIN3, Pin 11)
4	SCL	-	Digital interface (SCL, Pin4; SDA, Pin 5)
5	SDA	-	Digital interface (SCL, Pin4; SDA, Pin 5)
6	AGND	-	GND Connection (GND, Pins 1 and 3; AGND, Pin 6)
7	VCC	C2	Internal VCC (VCC, Pin 7)
8	FB2	-	Setting the Output Voltage (FB1, Pin 11; FB2, Pin 8; FB3, Pin 14)
9	SW2	L2, C4	Selecting the Output Capacitors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13; LDOOUT, Pin 15); Selecting the Inductors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13)
10	SW1	L1, C3A	Selecting the Output Capacitors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13; LDOOUT, Pin 15); Selecting the Inductors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13)
11	FB1/VIN3	C3B, C3C	Selecting the Input Capacitors (VIN, Pin 2; VIN3, Pin 11); Setting the Output Voltage (FB1, Pin 11; FB2, Pin 8; FB3, Pin 14)
12	PG	-	Power Good Indicator (PG, Pin 12)
13	SW3	L3, C5A, C5B	Selecting the Output Capacitors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13; LDOOUT, Pin 15); Selecting the Inductors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13)
14	FB3	-	Setting the Output Voltage (FB1, Pin 11; FB2, Pin 8; FB3, Pin 14)
15	LDOOUT	C6	Selecting the Output Capacitors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13; LDOOUT, Pin 15)

Setting the Output Voltage (FB1, Pin 11; FB2, Pin 8; FB3, Pin 14)

OTP registers VOUT_COMMAND set the output voltage (V_{OUT}). Write the VOUT_CMD bits in multi-page to set each rail's V_{OUT}. See the Register Map section on page 41 for details.

V_{OUT1} can be calculated with Equation (1):

$$V_{OUT1}(V) = VOUT\_CMD[3:0] \times 0.1 + 2.5 \quad (1)$$

V_{OUT2} can be calculated with Equation (2):

$$V_{OUT2}(V) = VOUT\_CMD[5:0] \times 0.05 + 0.6 \quad (2)$$

V_{OUT3} can be calculated with Equation (1):

$$V_{OUT3}(V) = VOUT\_CMD[5:0] \times 0.05 + 0.6 \quad (3)$$

V_{LDOOUT} can be calculated with Equation (4):

$$V_{LDOOUT}(V) = VOUT\_CMD[5:0] \times 0.05 + 0.6 \quad (4)$$

Selecting the Input Capacitors (VIN, Pin 2; VIN3, Pin 11)

The step-down converter has a input current (I_{IN}) discontinuous and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage (V_{IN}). For the best performance, use low ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their low ESR and small temperature coefficients.

It is strongly recommended to use another lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since the input capacitor (C_{IN}) absorbs the switching I_{IN}, it requires an adequate ripple current rating. The RMS current in C_{IN} (I_{CIN}) can be estimated with Equation (5):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (6):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose a C_{IN} with an RMS current rating greater than half of the maximum load current (I_{LOAD_MAX}).

C_{IN} can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible.

When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive input voltage (ΔV_{IN}). ΔV_{IN} caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

Selecting the Output Capacitors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13; LDOOUT, Pin 15)

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the V_{OUT} ripple (ΔV_{OUT}) low. The buck converter's ΔV_{OUT} can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \cdot (1 - \frac{V_{OUT}}{V_{IN}}) \cdot (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (8)$$

Where L is the inductance, and R_{ESR} is (ESR) value of C_{OUT}.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple.

For simplification, ΔV_{OUT} can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency (f_{SW}). For simplification, ΔV_{OUT} can be approximated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (10)$$

The characteristics of C_{OUT} also affect the stability of the regulation system. The MPQ70240FS can be optimized for a wide range of capacitance and ESR values.

The LDO is specifically designed to work with a standard ceramic C_{OUT} to save space and improve performance. The LDO charges C_{OUT} during start-up. The charge current is the LDO current limit (I_{LIMIT}) minus the load current (I_{LOAD}). There is minimum 385µs internal under-voltage (UV) blanking time, and C_{OUT} must be fully charged during this period. For example, if there is a constant 200mA load during start-up and the LDO setting voltage is 2.8V, then C_{OUT} should be below 6.9µF to be fully charged. A 2.2µF (e.g. 16V, X7R) ceramic capacitor is recommended for most applications.

A higher LDO C_{OUT} is feasible if I_{LOAD} during start-up is kept sufficiently low. The maximum allowed effective C_{OUT} can be calculated with Equation (11):

$$C_{MAX} = (I_{LIMIT\_MIN} - I_{LOAD}) \times BT / V_{LDO} \quad (11)$$

Where I_{LIMIT_MIN} is 280mA, and BT is 385µs.

For example, if I_{LOAD} is a constant 10mA during start-up and the LDO setting voltage is 2.8V, then the maximum allowed effective C_{OUT} should be 37µF (0.27A / 2.8V x 385µs).

Selecting the Inductors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13)

A 1µH to 10µH inductor with a DC current rating at least 25% higher than I_{LOAD_MAX} is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower ΔV_{OUT}; however, a larger-value inductor also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance is to allow the inductor ripple current to be approximately 30% of I_{LOAD_MAX}. The inductance (L) can be calculated with Equation (12):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of I_{LOAD_MAX}. The maximum inductor peak current (I_{LP}) can be calculated with Equation (13):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (13)$$

Internal VCC (VCC, Pin 7)

The VCC capacitor (C2) should be between 1µF and 10µF. Generally, a 2.2µF or 4.7µF ceramic capacitor is recommended.

Most of the internal circuitry is powered by the internal 5V VCC regulator. This regulator uses V_{IN} as its input and operates across the entire V_{IN} range. When V_{IN} exceeds 5V, VCC is in full regulation. When V_{IN} drops below 5V, the VCC output degrades.

Digital Interface (SCL, Pin4; SDA, Pin 5)

The MPQ70240FS works as a slave-only device, which supports up to 1000kbs of bidirectional data transfer in fast mode, adding flexibility to the power supply solution. See the Digital Interface section on page 38 for details.

The SCL and SDA lines are pulled externally to an external voltage using resistor (e.g. 1kΩ). The MPQ70240FS does not use any of its outputs as the SCL/SDA lines of the pull-up voltage. If this is required in application, please contact an MPS FAE.

Power Good Indicator (PG, Pin 12)

The PG pin integrates push-pull structure internally; no external components are needed.

GND Connection (GND, Pins 1 and 3; AGND, Pin 6)

See the PCB Layout Guidelines section on page 71 for more details.

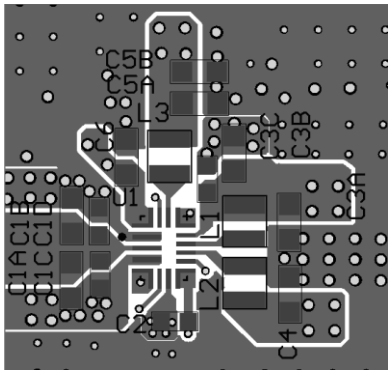
PCB Layout Guidelines (15)

Efficient PCB layout, especially for C_{IN} placement, is critical for stable operation. A four-layer layout is strongly recommended for improved thermal performance. For best results, refer to Figure 15 and follow the guidelines below:

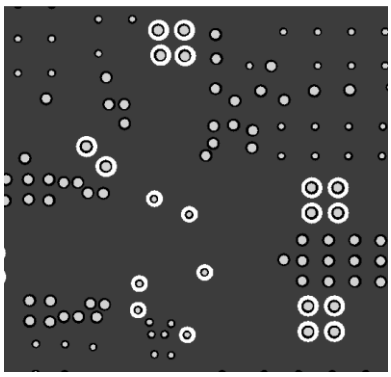
1. Place the symmetric input capacitors as close to VIN and GND as possible.
2. Use a large ground plane to connect to GND directly.
3. Connect the high-current paths at GND and VIN using short, direct, and wide traces.
4. Place the ceramic C_{IN}, especially the small package size (0603) input bypass capacitor, as close to VIN, VIN3, and GND as possible to minimize high-frequency noise.
5. Keep the connection between C_{IN} and VIN as short and wide as possible.
6. Place the VCC capacitor as close to VCC and AGND as possible.
7. Route SW away from sensitive analog areas, such as FB.
8. Ensure that the trace between FB and the output is as short as possible.
9. Use multiple vias to connect the power planes to the internal layers.

Note:

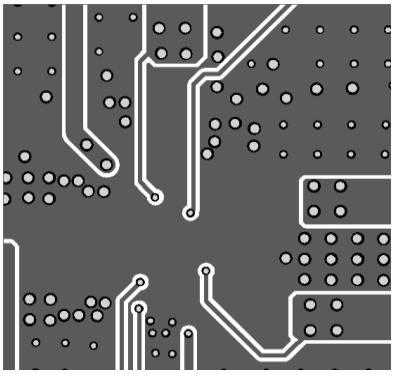
15) The recommended PCB layout is based on Figure 16 on page 72.



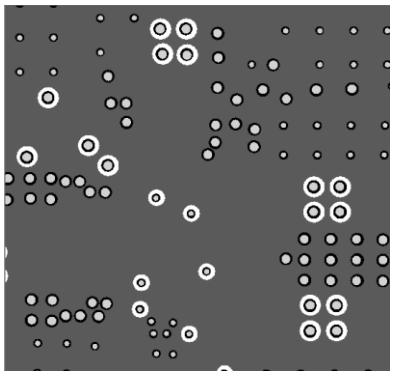
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 15: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

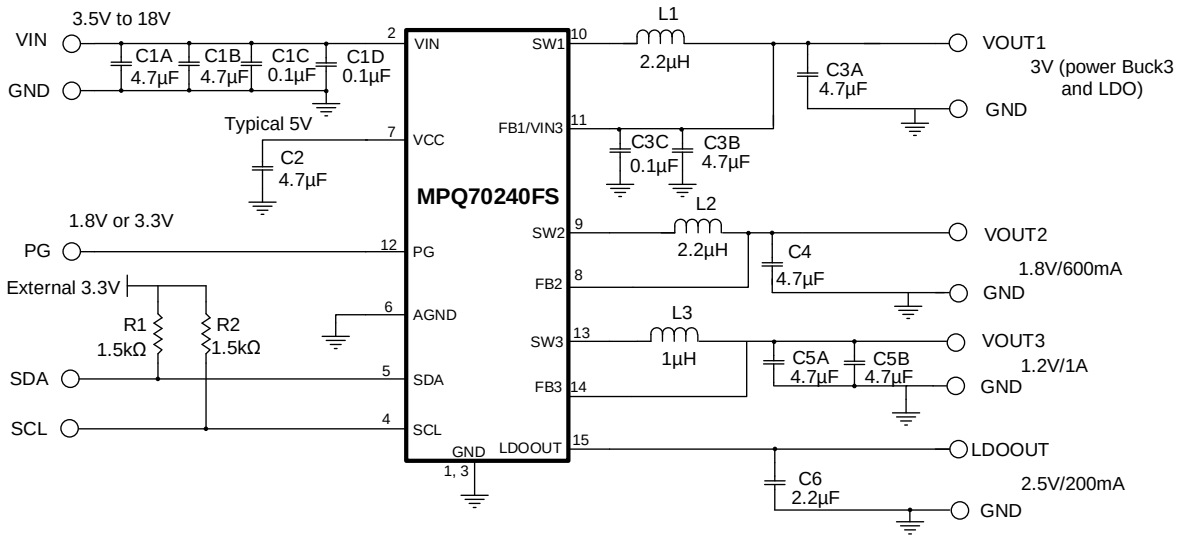


Figure 16: Typical Application Circuit (V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V)

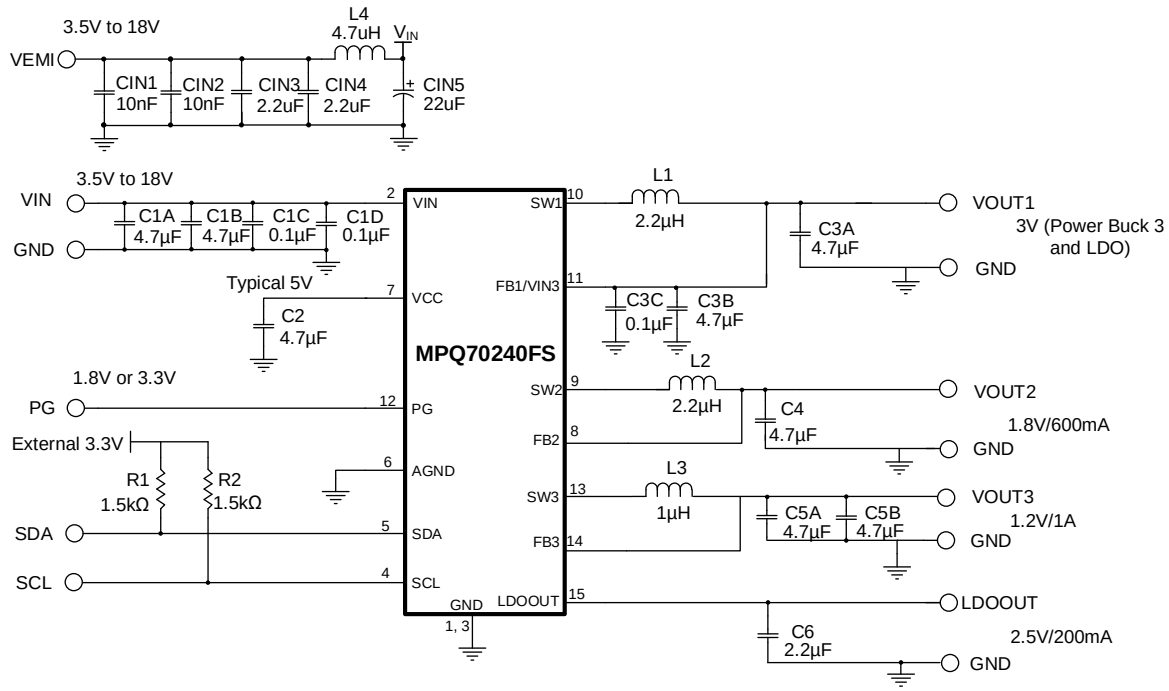


Figure 17: Typical Application Circuit with EMI Filters (V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V)

TYPICAL APPLICATION CIRCUITS *(continued)*

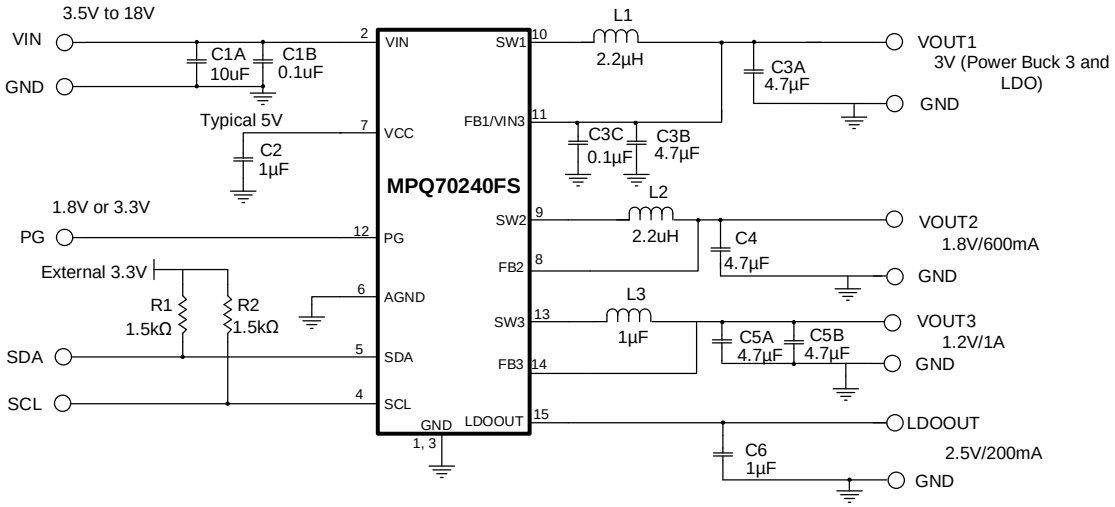
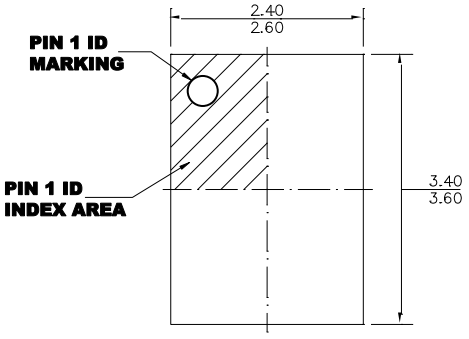


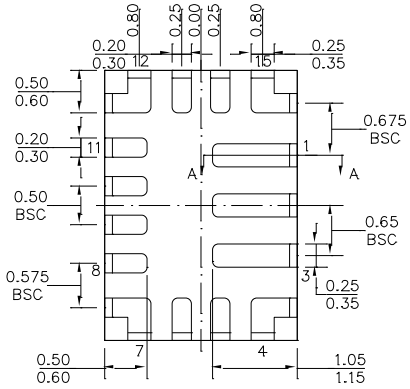
Figure 18: Typical Application Circuit with Reduced External Component Count (V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V)

PACKAGE INFORMATION

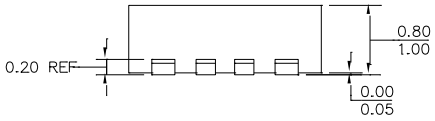
QFN-15 (2.5mmx3.5mm)
Wettable Flank



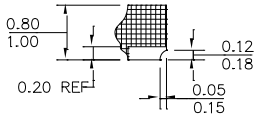
TOP VIEW



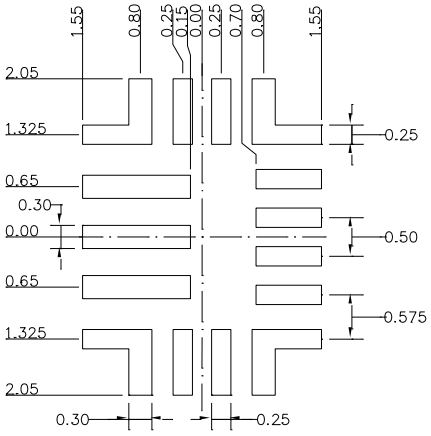
BOTTOM VIEW



SIDE VIEW



SECTION A-A

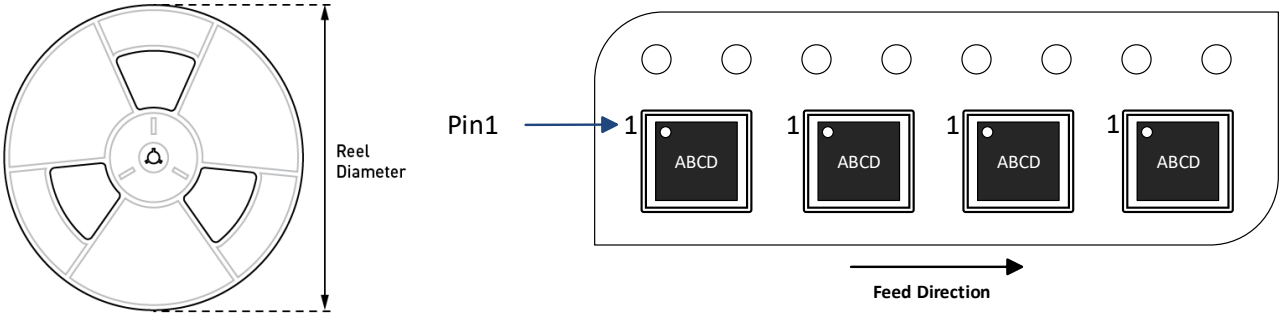


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube (16)	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ70240FSGRHE -xxxxAEC1-Z	QFN-15 (2.5mmx3.5mm)	5000	N/A	N/A	13in	12mm	8mm

Note:

16) N/A indicates “not available” in tubes. For the 500 pieces tape and reel prototype quantities, contact the factory. (The order code for a 500-piece partial reel is “-P”; and the tape and reel dimensions are same as the full reel.).

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/13/2023	Initial Release	-