Evaluation Board User Guide

EVAL-ADPL74101-AZ

High Voltage Step-Down Controller

General Description

Evaluation circuit *EVAL-ADPL74101-AZ*, features the ADPL74101, a 100V step-down synchronous controller. The *ADPL74101* features low I_Q, up to 1MHz programmable/synchronizable switching frequency, spread spectrum, and a small 28-lead (4mm x 5mm) QFN package. These features allow for a wide variety of applications, including industrial, military, medical, and telecommunications systems.

The EVAL-ADPL74101-AZ operates from a 16V to 72V input voltage range and generates a 12V, 15A output. The ADPL74101 has a precision voltage reference that can generate an output voltage with less than 2% tolerance over the full operating conditions. The EVAL-ADPL74101-AZ is set to a 300kHz switching frequency, which results in a small and efficient circuit. The converter achieves over 94% efficiency with a 15A load at full operating V_{IN}, with a peak efficiency of over 96%.

This board can be easily modified to regulate output voltages from 0.8V to 60V. The evaluation circuit has been specifically designed with 100V field-effect transistors (FETs); various FETs with similar footprints can be replaced to fit a wide array of applications.

The EVAL-ADPL74101-AZ provides a high-performance, cost-effective solution for generating a 12V output. The ADPL74101 data sheet provides a complete description of this device, including its operation and application information. The data sheet must be read in conjunction with this user guide for EVAL-ADPL74101-AZ.

Design files for this circuit board are available at *www.analog.com*.

Ordering Information **appears at end of data sheet.**

Performance Summary (T_A = 25°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range, V_{IN}		16		72	V
Output Voltage, V_{OUT}	V_{IN} = 16V to 72V	11.82	12	12.18	V
Maximum Load Current, I_{OUT}	V_{IN} = 16V to 72V, Airflow (see *Figure 8*)			15	A
	VIN = 16V to 60V, No airflow, Maximum Board Temperature < 100°C			15	A
Output Voltage Ripple (Peak-to-Peak)	V_{IN} = 48V, I_{OUT} = 15A		115		mV_{P-P}
Run Rising Threshold			15.4		V
Run Falling Threshold			13.9		V
Switching Frequency	J5 = Fixed Frequency (Spread Spectrum Frequency Modulation (SSFM) Off)		300		kHz
	J5 = Spread (SSFM On)	300		360	kHz
Typical Efficiency	V_{IN} = 24V, I_{OUT} = 15A		96.3		%
	V_{IN} = 48V, I_{OUT} = 15A		95.5		%

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Quick Start Procedure

Evaluation circuit EVAL-ADPL74101-AZ is easy to set up to evaluate the performance of the ADPL74101. For a proper measurement equipment setup, see *Figure 1* and use the following procedure.

1. Set the input power supply to a voltage between 16V and 72V. Disable the power supply.

   Note: Make sure that the input voltage V_{IN} does not exceed 72V.

2. Connect the positive terminal of the power supply to V_{IN} and the negative terminal to GND.
3. Connect the load (≤15A) between V_{OUT} and GND.
4. Verify that the RUN switch (SW1) is set to the ON position.
5. Enable the input power supply and adjust the input voltage to 48V.
6. Verify that the output voltage measures 12V on the voltmeter connected to V_{OUT}. If there is no output, temporarily disconnect the load to ensure that the load is not set too high.
7. Once the proper output voltage is established, adjust the load and observe the output voltage regulation, ripple voltage, efficiency, and other parameters.

Note: When measuring the input or output voltage ripple, care must be taken to minimize the length of the oscilloscope probe ground lead. Measure the input or output voltage ripple by connecting the probe tip directly across the V_{IN} or V_{OUT} and GND terminals, preferably across the input or output capacitors.

The EVAL-ADPL74101-AZ is a fully assembled and tested board that demonstrates the ADPL74101's performance. The evaluation circuit is designed to deliver 12V output at a load current up to 15A from a 16V to 72V input supply. The board is programmed at a 300kHz switching frequency for optimum efficiency and component size.

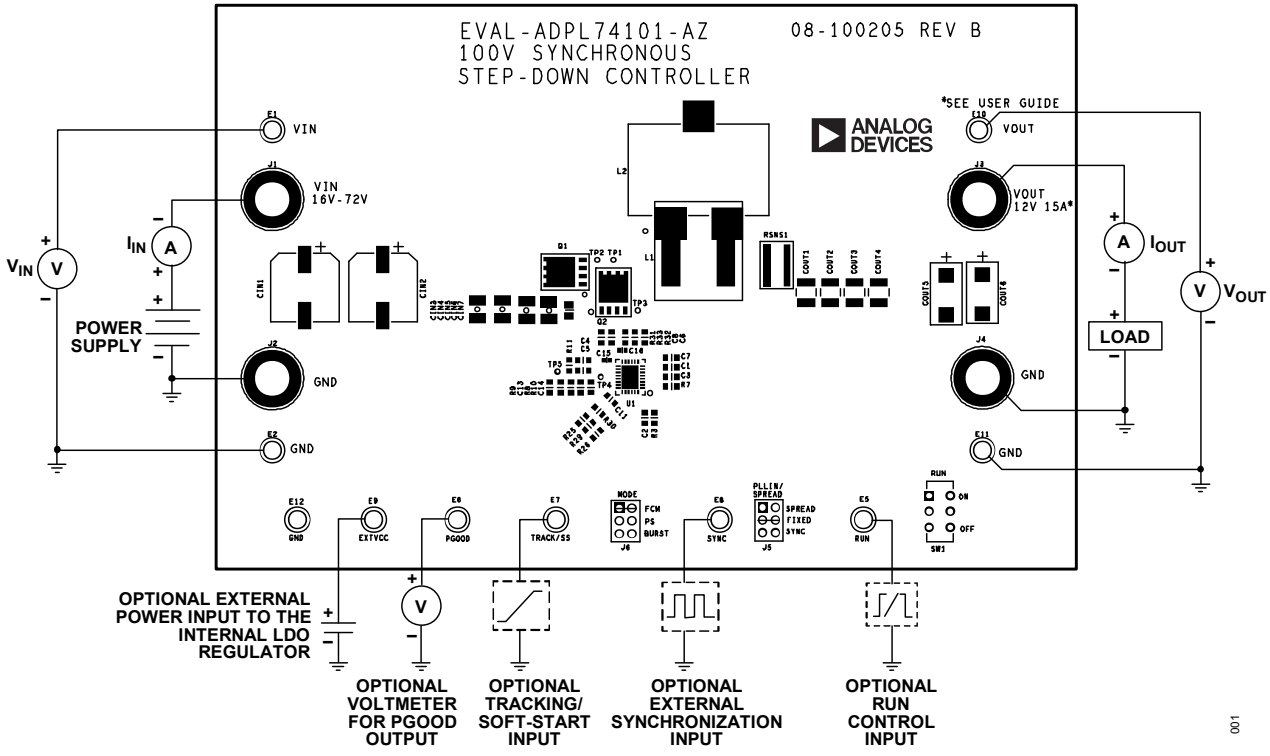

Figure 1. EVAL-ADPL74101-AZ Board Connections

Adjusting the Output Voltage

The ADPL74101 supports an adjustable output voltage range, from 0.8V to 60V. To change the output voltage from the programmed 12V, change R8 and R10, and remove R21 to float the VPRG pin. Refer to the *Setting the Output Voltage* section in the ADPL74101 data sheet for how to calculate the VFB resistor divider values for the desired output voltage. All the corresponding power components will also need to be changed to meet the desired output voltage.

Setting the Switching Frequency

Selecting the switching frequency is a trade-off between efficiency and component size. For optimal performance, a switching frequency of 300kHz is chosen for a 12V output. R7 programs the desired switching frequency. The switching frequency is set using the FREQ and PLLIN/SPREAD pins. Refer to the *Setting the Operating Frequency* section in the ADPL74101 data sheet for more details.

RUN Control (RUN, SW1)

The RUN turret of the evaluation circuit serves as an external on/off control for the controller. The EVAL- ADPL74101-AZ includes a resistive voltage divider (R2 and R3) connected between the V_{IN} and GND pins to act as an undervoltage lockout. Turn the switch (SW1) to the ON position to connect the RUN pin to the center of this resistor divider. The EVAL-ADPL74101-AZ is designed to turn on ADPL74101 at around 15V. However, this threshold can be easily adjusted by changing R2 and R3. Turn SW1 to the “OFF” position to disable the controller. See *Table 3* to configure SW1.

TRACK and Soft-Start Input (TRACK/SS)

The ADPL74101’s TRACK/SS pin can be used to program an external soft-start function or to allow V_{OUT} to track another supply during startup. The adjustable soft-start function limits inrush current during startup. The soft-start time is adjusted by C3. An external supply can be connected to the TRACK/SS turret to make the startup of the V_{OUT} track an external supply. Typically, this requires connecting to the TRACK/SS turret through an external resistor divider from the external supply to GND. Refer to the *Soft-Start and Tracking (TRACK/SS Pin)* section in the ADPL74101 data sheet for details.

Mode Selection (MODE, J6)

The EVAL-ADPL74101-AZ provides a jumper (J6) to allow the ADPL74101 to operate in either forced continuous, pulse-skipping, or burst modes at lighter loads. Refer to the ADPL74101 data sheet for more details on the modes of operation. *Table 1* shows the mode selection J6 settings that can be used to configure the desired mode of operation.

Spread Spectrum, Phase-Locked Loop, and External Frequency Synchronization (PLLIN/SPREAD, J5)

The ADPL74101 features spread-spectrum mode operation to improve electromagnetic interference (EMI). This mode varies the switching frequency within the typical range of the frequency set by the FREQ pin, up to +20%. Spread-spectrum operation is enabled by tying the PLLIN/SPREAD pin to $INTV_{CC}$. The EVAL-ADPL74101-AZ includes a jumper (J5) to conveniently enable or disable the spread-spectrum operation. See *Table 2* to configure J5.

The ADPL74101 also features a phase-locked loop to synchronize the internal oscillator to an external clock source. The EVAL-ADPL74101-AZ provides a SYNC turret to connect an external clock source to synchronize with the device switching. Keep the jumper (J5) in the SYNC position when the external clock signal is applied. Refer to the *External Clock Synchronization* in the ADPL74101 data sheet for more details.

Open-Drain PGOOD Output (PGOOD)

The EVAL-ADPL74101-AZ provides a PGOOD turret to monitor the status of the PGOOD output. PGOOD is high when V_{FB} voltage is within ±10% of the 0.8V reference. PGOOD is pulled low when the V_{FB} voltage is not within 0.8V ±10% or when the RUN pin is low (shutdown). The voltage on the PGOOD pin should not exceed 6V.

$EXTV_{CC}$ Linear Regulator

The $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high-efficiency external source. On EVAL- ADPL74101-AZ, the $EXTV_{CC}$ pin is connected to V_{OUT}. The $EXTV_{CC}$ turret can be used to connect an external power supply to source the $EXTV_{CC}$ LDO. When using an external power supply on the $EXTV_{CC}$ turret, make sure to disconnect the V_{OUT} connection to the $EXTV_{CC}$ pin by removing R19. Populate R20 with a 0Ω resistor.

Thermal Performance

The ADPL74101 features excellent thermal performance due to the high efficiency of the synchronous step-down controller circuitry. The component temperatures of EVAL-ADPL74101-AZ with a typical 48V input and 15A load are shown in *Figure 7*. The six-layer printed circuit board (PCB) layout features solid copper planes that provide adequate heat spreading across the whole board.

Table 1. MODE Selection Jumper (J6) Settings

SHUNT POSITION	MODE PIN	MODE
1 to 2* (FCM)	Connected to $INTV_{CC}$	FCM mode of operation
3 to 4 (PS)	Connected to $INTV_{CC}$ with a 100kΩ	Pulse-skipping mode of operation
5 to 6 (BURST)	Connected to GND	Burst mode of operation

**Default position*

Table 2. PLLIN/SPREAD Jumper (J5) Settings

SHUNT POSITION	PLLIN/SPREAD PIN	DESCRIPTION
1 to 2 (SPREAD)	Connected to $INTV_{CC}$	Enable spread spectrum
3 to 4* (FIXED)	Connected to GND	Fixed frequency
5 to 6 (SYNC)	Connected to the center node of R17 and C9	External SYNC input

**Default position*

Table 3. RUN Switch (SW1) Settings

SWITCH POSITION	RUN PIN	CONTROLLER
ON	Connected to the center node of the resistor-divider (R2 and R3)	Programmed to start up at the desired input voltage level
OFF*	Connected to GND	Disabled

**Default position*

Performance

(V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 15A, f_{SW} = 300kHz, MODE =, T_A = +25°C, unless otherwise noted.)

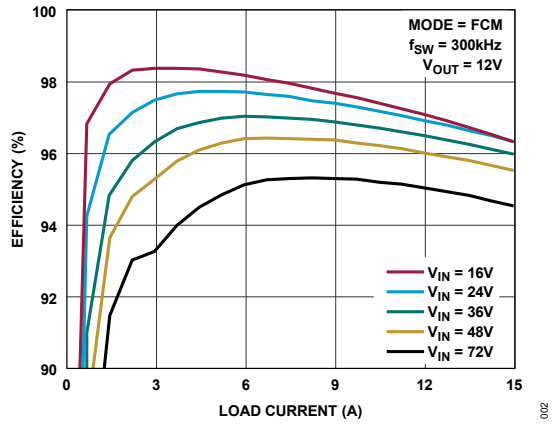

Figure 2. Efficiency vs. Load Current. At V_{IN} = 48V, EVAL-ADPL74101-AZ performs with an efficiency of over 95% with a 12V Output and a 15A Load

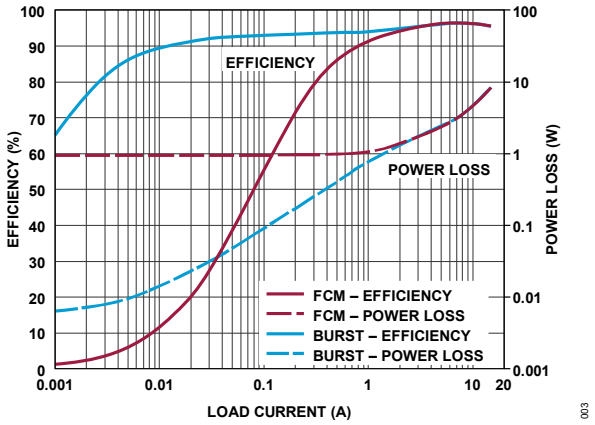

Figure 3. Efficiency and Power Loss vs. Load Current at V_{IN} = 48V. At low load, burst mode significantly improves power loss compared to FCM

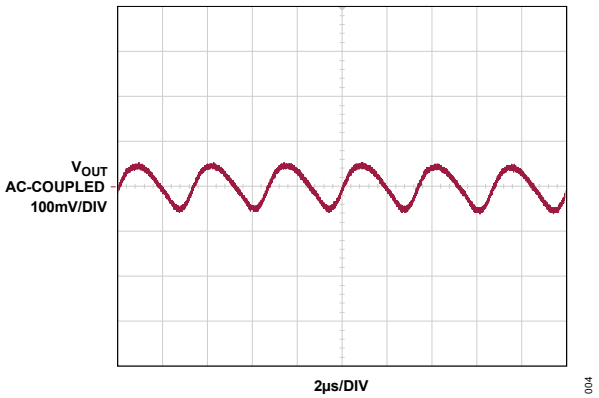

Figure 4. Output Ripple at V_{IN} = 48V, V_{OUT} = 12V, with a 15A Load

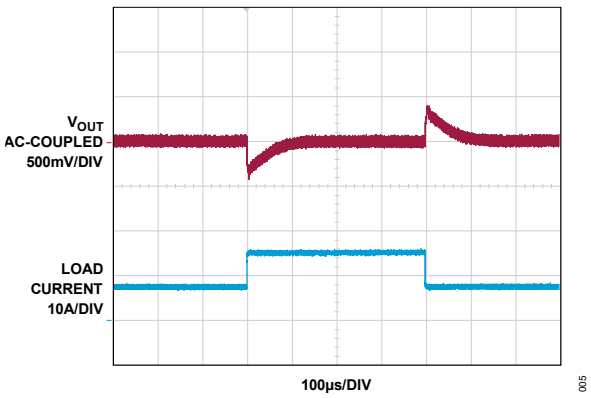

Figure 5. Load Step Response. EVAL-ADPL74101-AZ has a good load step response with small output capacitors

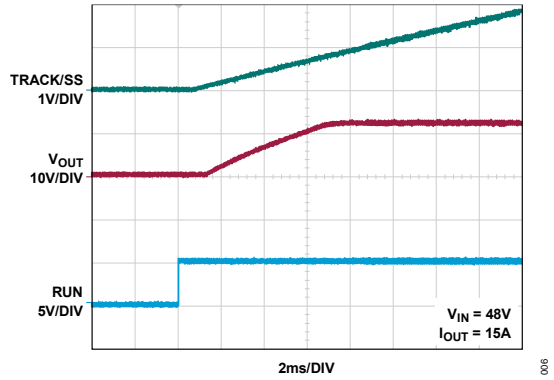

Figure 6. Soft-Start Behavior. EVAL-ADPL74101-AZ ramps the output slowly at startup without output voltage overshoot

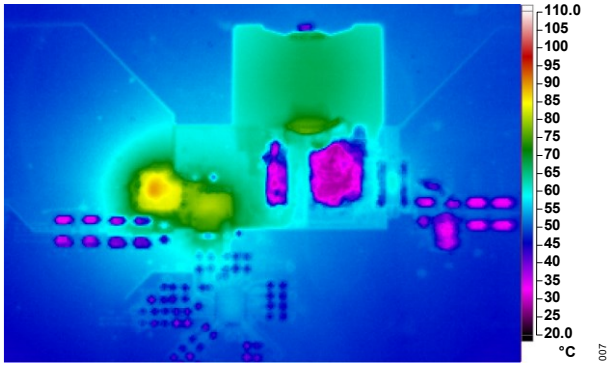

Figure 7. Thermal Performance with 48V Input, 12V Output, and 15A Load. No airflow. The hottest component on EVAL-ADPL74101-AZ stays under 100°C. (T_A = 25°C)

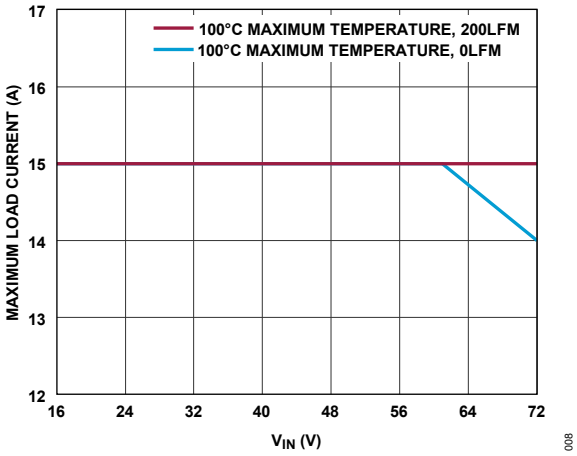

Figure 8. Maximum recommended output current vs. V_{IN}, keeping maximum board temperature under 100°C at room temperature. With airflow, the board can operate at the full 15A load for the entire input range (16V to 72V)

Ordering Information

PART	TYPE
EVAL-ADPL74101-AZ	Evaluation Board

EVAL-ADPL74101-AZ Bill of Materials

ITEM	QTY	DESIGNATOR	PART DESCRIPTION	MANUFACTURER/PART NUMBER
REQUIRED CIRCUIT COMPONENTS				
1	1	C1	CAP., 0.1µF, X7R, 100V, 10%, 0603	MURATA, GRM188R72A104KA35D
2	2	C6, C10	CAP., 1µF, X7R, 25V, 10%, 0603, AEC-Q200	MURATA, GCM188R71E105KA64D
3	1	C11	CAP., 1000pF, X7R, 25V, 10%, 0603	AVX, 06033C102KAT2A
4	3	C3, C7, C12	CAP., 0.1µF, X7R, 25V, 10%, 0603	KEMET, C0603C104K3RACTU
5	3	C2, C5, C9	CAP., 100pF, X7R, 50V, 10%, 0603	YAGEO, CC0603KRX7R9BB101
6	1	C4	CAP., 4700pF, C0G, 50V, 10%, 0603	KEMET, C0603C104K3RACTU
7	1	C8	CAP., 4.7µF, X5R, 25V, 10%, 0603, AEC-Q200	MURATA, GRT188R61E475KE13D
8	2	CIN1, CIN2	CAP., 47µF, AL-ELEC., 100V, 20%, AEC-Q200	NICHICON, UUX2A470MNL1GS
9	4	CIN3, CIN4, CIN5, CIN6	CAP., 10µF, X7S, 100V, 10%, 0603, AEC-Q200	MURATA, GRM32EC72A106KE05L
10	1	CIN7	CAP., 1µF, X7S, 100V, 10%, 0805	TDK, C2012X7S2A105K125AB
11	2	COUT1, COUT2	CAP., 22µF, X5R, 25V, 20%, 1210	AVX, 12103D226MAT2A
12	1	COUT5	AP., 150µF, TANT., 16V, 20%, 7343	PANASONIC, 16TQC150MY
13	1	L2	IND., 5.5µH, WE-HCF, PWR, 15%, 22A, 4.4mΩ, 2013	WÜRTH ELEKTRONIK, 7443630550
14	1	Q1	TRAN., N-CH, Power Mosfet, 100V, 44A, PG-TDSON-8	INFINEON, BSC146N10LS5ATMA1
15	1	Q2	TRAN., N-CH, Power Mosfet, 100V, 79A, PG-TDSON-8	INFINEON, BSC070N10LS5ATMA1
16	11	R1, R8, R9, R12, R14, R19, R21, R23, R26, R31, R32	RES., 0Ω, 1/10W, 0603, AEC-Q200	VISHAY, CRCW06030000Z0EA
17	1	R11	RES., 7.68kΩ, 1%, 1/10W, 0603, AEC-Q200	VISHAY, CRCW06037K68FKEA
18	1	R17	RES., 1kΩ, 1%, 1/10W, 0603, AEC-Q200	PANASONIC, ERJ-3EKF1001V
19	1	R18	RES., 100kΩ, 1%, 1/10W, 0603, AEC-Q200	PANASONIC, ERJ-3EKF1003V
20	1	R2	RES., 412kΩ, 1%, 1/10W, 0603, AEC-Q200	VISHAY, CRCW0603412KFKEA
21	1	R25	RES., 20Ω, 1%, 1/10W, 0603, AEC-Q200	VISHAY, CRCW060320R0FKEA
22	1	R3	RES., 36.5kΩ, 1%, 1/10W, 0603, AEC-Q200	PANASONIC, ERJ-3EKF3652V
23	1	R30	RES., 100Ω, 1%, 1/10W, 0603	YAGEO, RC0603FR-07100RL
24	1	R33	RES., 2Ω, 1%, 1/10W, 0603	YAGEO, RC0603FR-072RL
25	1	R4	RES., 1MΩ, 5%, 1/10W, 0603	VISHAY, CRCW06031M00JNEA
26	1	R7	RES., 124kΩ, 1%, 1/10W, 0603, AEC-Q200	PANASONIC, ERJ-3EKF1243V
27	1	RSNS1	RES., 0.003Ω, 1%, 3W, 1225, AEC-Q200	SUSUMU, KRL6432E-M-R003-F-T1
28	1	U1	IC, Step-down Controller, QFN-28	ANALOG DEVICES, ADPL74101ACPZ-RL

ITEM	QTY	DESIGNATOR	PART DESCRIPTION	MANUFACTURER/PART NUMBER
OPTIONAL CIRCUIT COMPONENTS				
1	2	C13, C14	CAP., 100pF, X7R, 50V, 10%, 0603	YAGEO, CC0603KRX7R9BB101
2	2	C15, C16	CAP., 0.1µF, X7R, 25V, 10%, 0402	AVX, 04023C104KAT2A
3	2	COUT3, COUT4	CAP., 22µF, X5R, 25V, 20%, 1210	AVX, 12103D226MAT2A
4	1	COUT6	AP., 150µF, TANT., 16V, 20%, 7343	PANASONIC, 16TQC150MY
5	1	D1	Dio Schottky Barrier Rectifier	DIODES INCORPORATED, DFLS1100-7
6	1	L1	IND., 10µH, PWR, 20%, 26A, AEC-Q200	COILCRAFT, XGL1313-103MED
7	10	R5, R10, R13, R15, R16, R20, R22, R24, R27, R29	RES., 0Ω, 1/10W, 0603, AEC-Q200	VISHAY, CRCW06030000Z0EA
HARDWARE – FOR EVALUATION CIRCUIT ONLY				
1	10	E1, E2, E5, E6, E7, E8, E9, E10, E11, E12	Est Point, Turret, 0.094" MTG. Hole, PCB 0.062" Thick	MILL-MAX, 2501-2-00-80-00-00-07-0
2	4	J1, J2, J3, J4	CONN-PCB Banana Jack	KEYSTONE, 575-4
3	2	J5, J6	CONN., HDR, MALE, 2 x 3, 2mm, VERT, STR, THT	SAMTEC, TMM-103-02-L-D
4	4	MECH1, MECH2, MECH3, MECH4	Standoff, Nylon, Snap-on, 0.625 (5/8"), 15mm	KEYSTONE, 9032
28	1	SW1	Switch Slide, DPDT, 300mA, 6V, Through Hole	C&K, JS202011CQN

ADPL74101-AZ Schematic Diagram

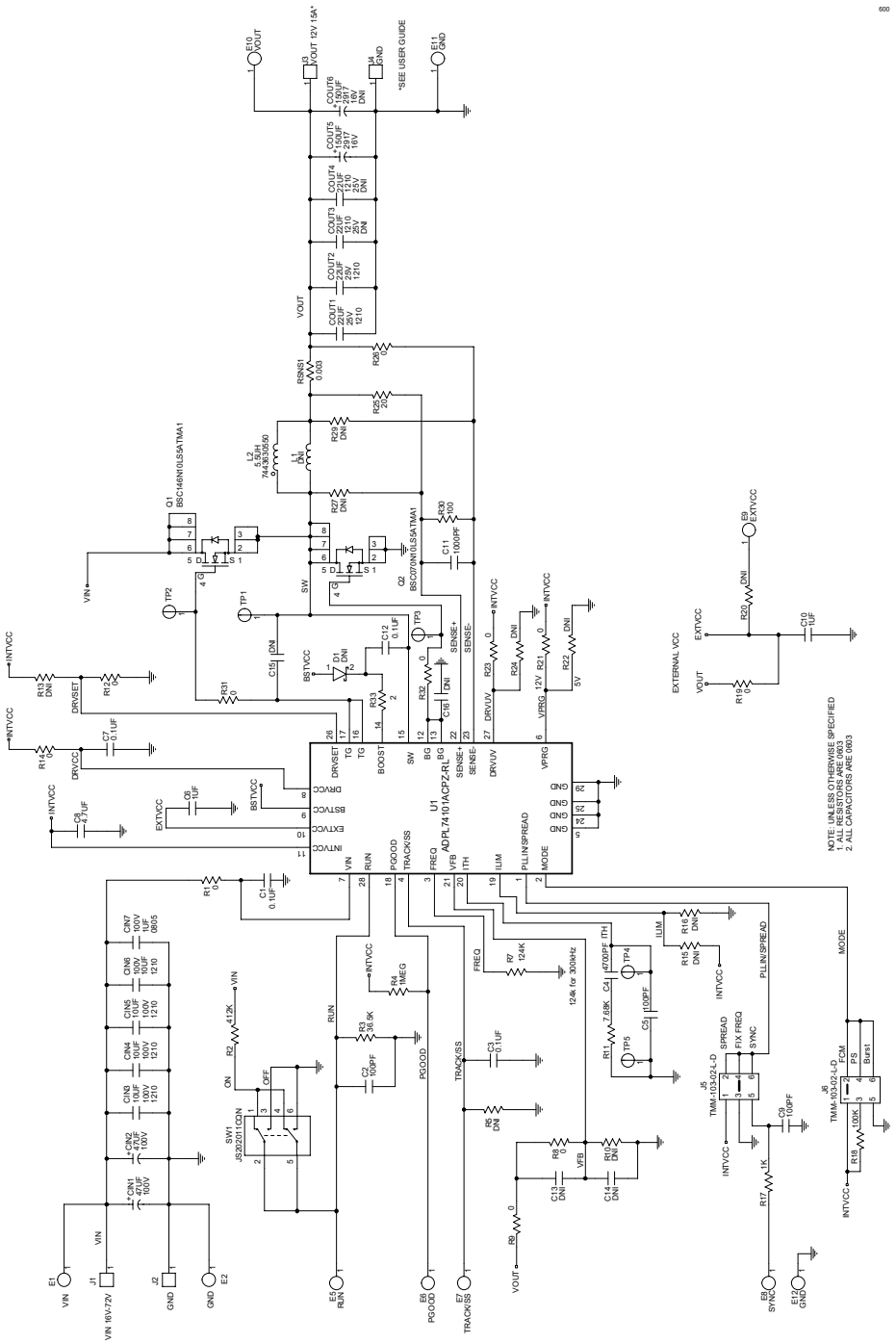

Figure 9. ADPL74101-AZ Schematic Diagram

EVAL-ADPL74101-AZ PCB Layout Diagrams

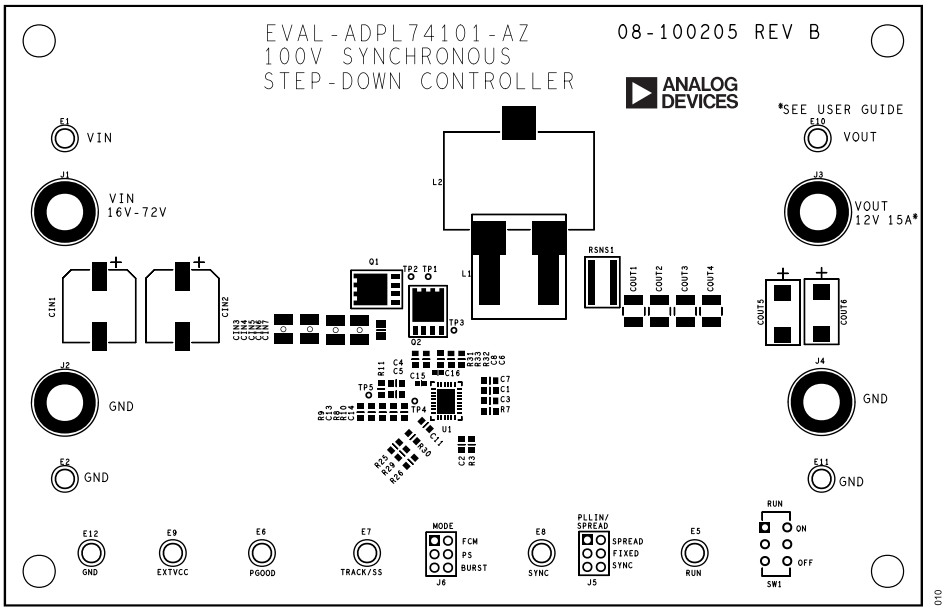

Figure 10. EVAL-ADPL74101-AZ Component Placement Guide—Top Silkscreen

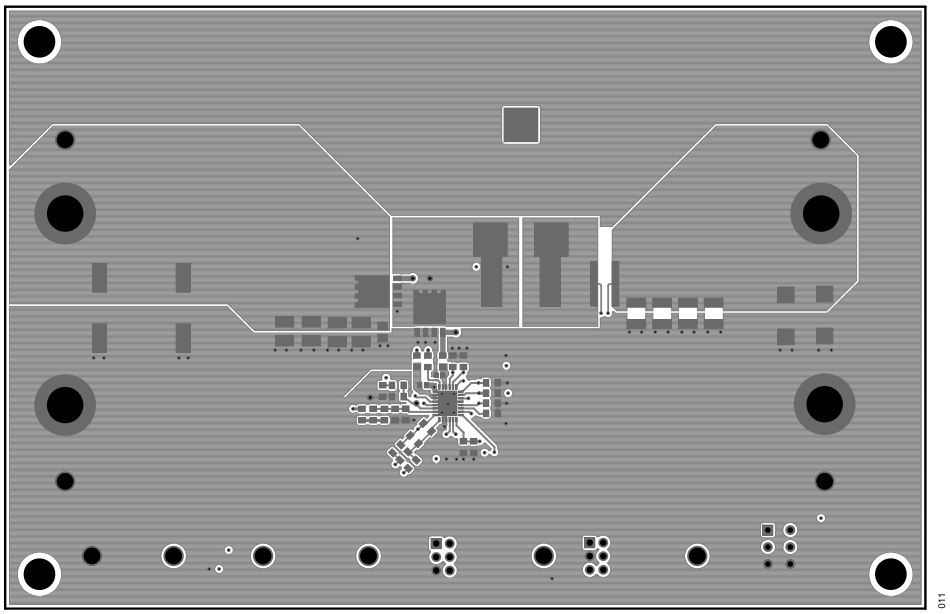

Figure 11. EVAL-ADPL74101-AZ PCB Layout—Top View

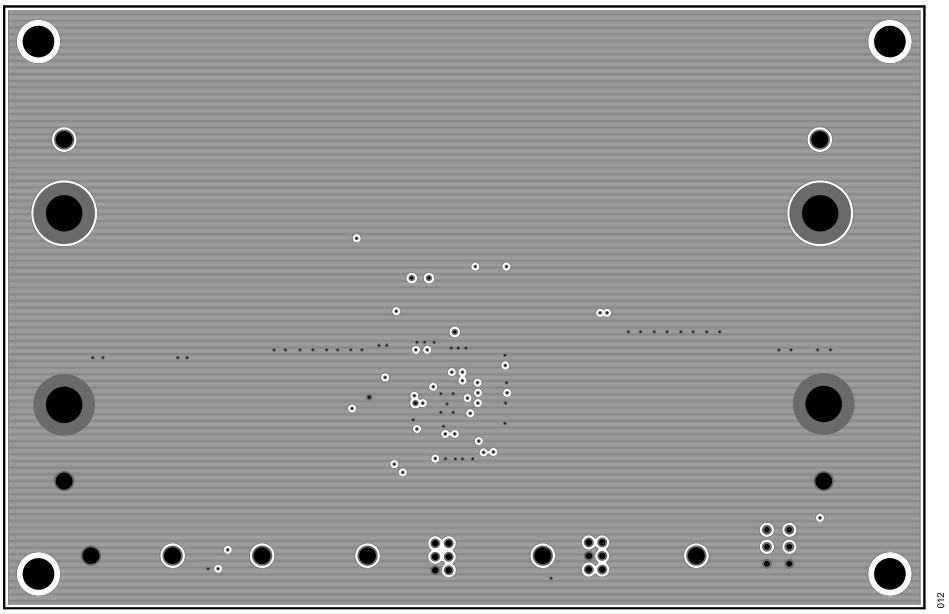

Figure 12. EVAL-ADPL74101-AZ PCB Layout—Layer 2

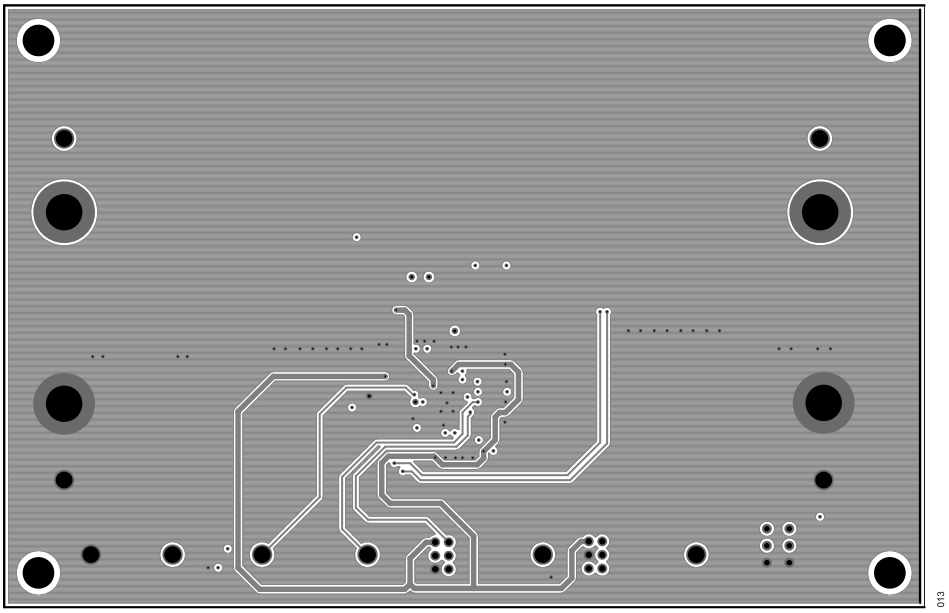

Figure 13. EVAL-ADPL74101-AZ PCB Layout—Layer 3

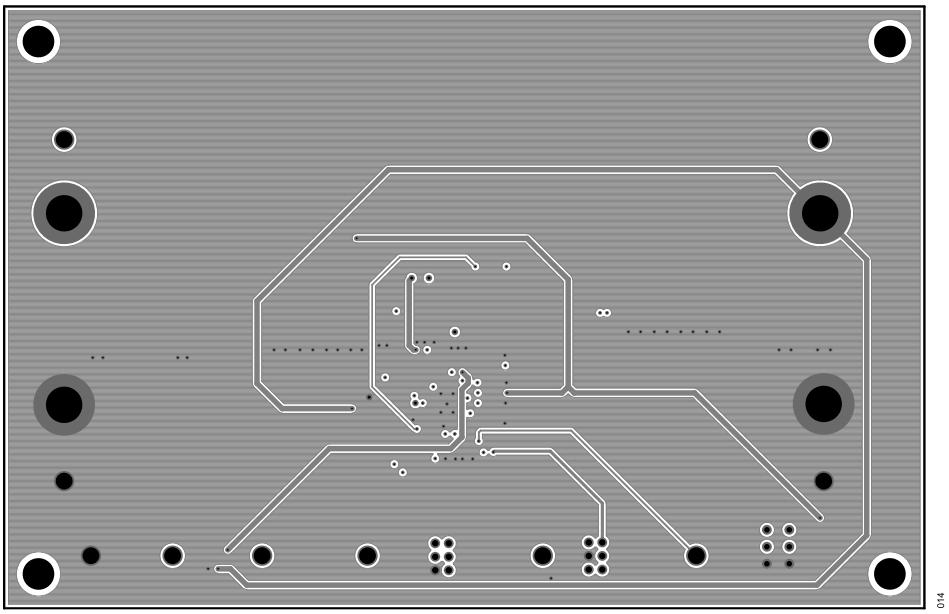

Figure 14. EVAL-ADPL74101-AZ PCB Layout—Layer 4

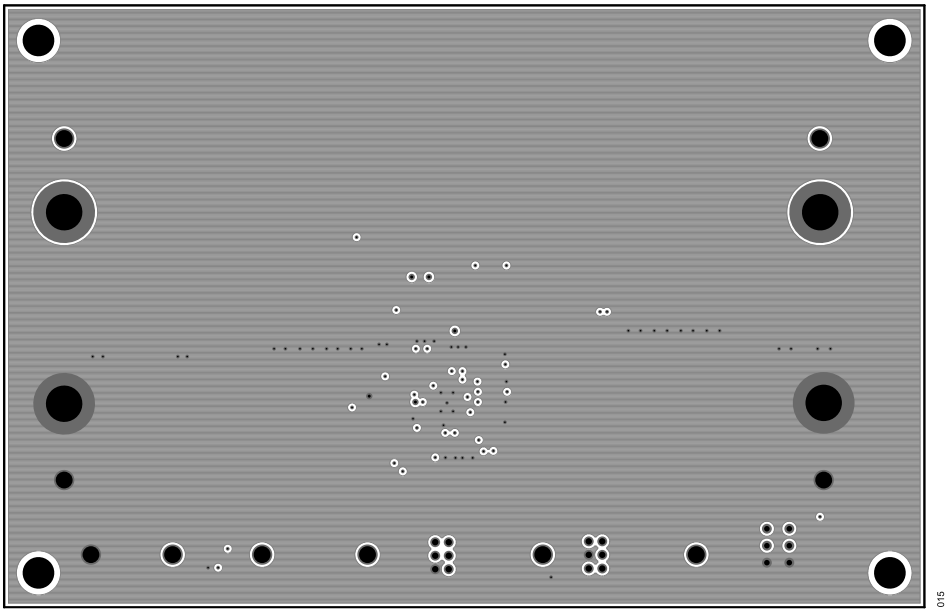

Figure 15. EVAL-ADPL74101-AZ PCB Layout—Layer 5

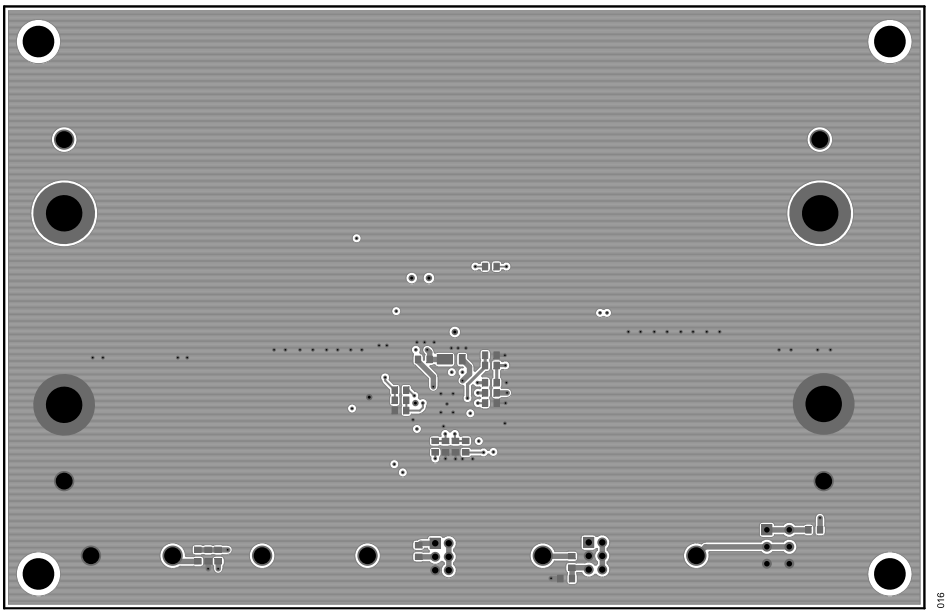

Figure 16. EVAL-ADPL74101-AZ PCB Layout—Bottom View

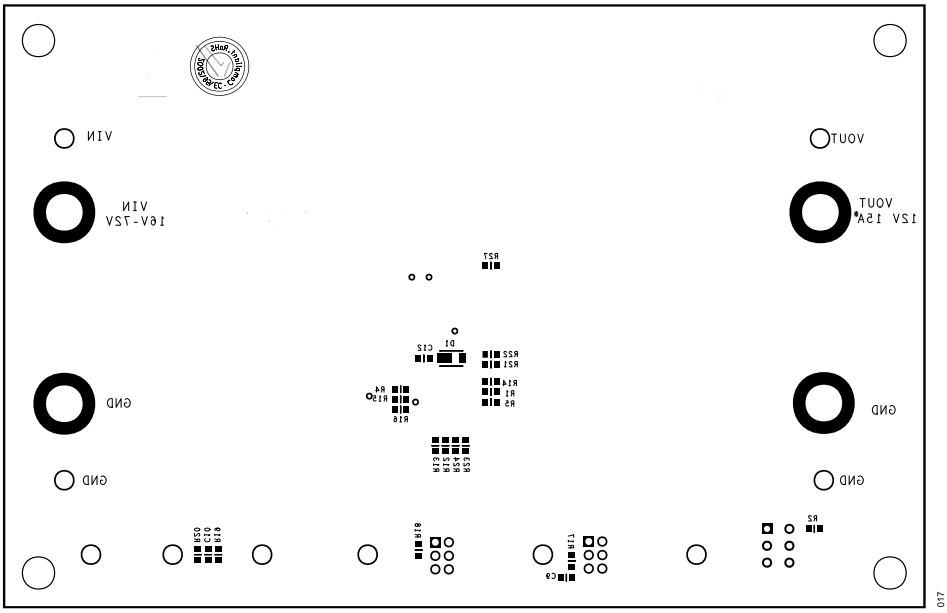

Figure 17. EVAL-ADPL74101-AZ Component Placement Guide—Bottom Silkscreen

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/25	Initial release	—

Notes