PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	ANALOG MEMS SENSORS/26/16321
1.3 Title of PCN	New Polyimides for HCMOS5 / HF5CMOS General Purpose Analog products
1.4 Product Category	See product list
1.5 Issue date	2026-04-27

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	PIKE EMMA
2.1.2 Phone	+44 1628896111
2.1.3 Email	emma.pike@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Marcello SAN BIAGIO
2.1.2 Marketing Manager	Lionel GRILLO
2.1.3 Quality Manager	David MOCELLIN

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Wafer Fab (Materials)	Direct and indirect materials/consumables (excluding substrate) : Change of supplier or source (new plant) with same material (same molecule) and equivalent or better performance	UMC Taiwan

4. Description of change		
	Old	New
4.1 Description	I-8124ER polyimide used on P/Ns TSV852AIYST, TSV854AIYPT, LMV824AIYPT	HD4100 or LTC9310 polyimide used on P/Ns TSV852AIYST, TSV854AIYPT, LMV824AIYPT
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No change on electrical and reliability performance	

5. Reason / motivation for change	
5.1 Motivation	Due to delivery disruption of polyimide I-8124ER from Asahi need to qualify two new polyimide HD4100 from Resonac and LTC9310 from Fujifilm, sharing similar characteristics with the qualified one. This polyimide I-8124ER is in use in UMC Taiwan for technology HCMOS5 and HF5CMOS for product General Purpose Analog
5.2 Customer Benefit	SERVICE CONTINUITY

6. Marking of parts / traceability of change	
6.1 Description	New Finished good codes

7. Timing / schedule	
7.1 Date of qualification results	2026-12-30
7.2 Intended start of delivery	2027-01-15
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	16321 PCN__Report-new-polyimide-H5_rev.2.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2026-04-27

9. Attachments (additional documentations)
16321 Public product.pdf 16321 PCN__Report-new-polyimide-H5_rev.2.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	TSV851IYLT	

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PRODUCT/PROCESS
CHANGE NOTIFICATION
ANALOG MEMS SENSORS/26/16321

Analog, Power&discrete, MEMS and Sensor Group

New Polyimides for HCMOS5 / HF5CMOS
General Purpose Analog products

WHAT:

Due to delivery disruption of polyimide I-8124ER from Asahi need to qualify two new polyimides HD4100 from Resonac and LTC9310 from Fujifilm, sharing similar characteristics with the qualified one. This polyimide I-8124ER is in use in UMC Taiwan for technology HCMOS5 and HF5CMOS for product General Purpose Analog

Material	Current process	additional process	Comment
Diffusion location	UMC Taiwan	UMC Taiwan	
Passivation	USG-PSG-SiON-PIX (I-8124ER)	USG-PSG-SiON-PIX (HD4100 or LTC9310)	
EWS	ST Singapore	ST Singapore	No change
Assembly location	TSHT (China) ST Bouskoura Morocco	TSHT (China) ST Bouskoura Morocco	No change neither location nor Bill of material

For the complete list of part numbers affected by the change, please refer to the attached Product list.

Samples are available, upon request.

WHY:
To manage direct material disruption for the affected technologies.

HOW:
Products are qualified based on qualification plan below described.

Qualification program and results:

The qualification program consists mainly of comparative electrical characterization and reliability tests. Please refer to Reliability evaluation plan for all the details.

WHEN:
Production in UMC Taiwan with the New Polyimides for selected products, is forecasted in January 2027.

Marking and traceability:

The traceability of the parts assembled with the new materials set will be ensured by new Internal sales codification, unique during the production phase.

Upon request by the Customer, engineering samples will be shipped using different FG codification for each polyimide material.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets.
There is as well no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).
In any case, first shipments may start earlier with customer's written agreement.

Change Qualification Plan

New polyimide for HCMOS5 / HF5CMOS
in UMC Taiwan

Test vehicle	
Product Lines:	*V802, V804, V814,*
Product Families:	• Low-power (180uA), general-purpose 5V Bipolar Op Amps, GBP=1.3MHz, dual • Low-power (180uA), general-purpose 5V Bi-polar Op-Amps, GBP=1.3MHz, quad • Low power (440uA), general purpose Bipolar 5V Op-Amps, GBP=5.5MHz, quad
P/Ns:	*TSV852AIYST, TSV854AIYPT, LMV824AIYPT*
Product Groups:	*AMS*
Product Divisions:	*General Purpose Analog*
Packages:	*Miniso, TSSOP14*
Silicon Process techn.:	*HF5CMOS*

Locations	
Wafer Diffusion Plants:	*UMC Taiwan*
EWS Plants:	*ST Singapore*
Assembly Plants:	*ST Bouskoura (Morocco),, TSHT (China),*
T&F Plants:	*, ST Bouskoura (Morocco),, TSHT (China)*

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits
AEC-Q006	Guidelines for Characterizing the Electrical Performance of IC Products

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 QUALIFICATION EVALUATION OVERVIEW

3.1 Objectives

To Qualify New polyimides for technology HF5CMOS/ HCMOS5 in UMC Taiwan.

3.2 Conclusion

Qualification Plan requirements must be fulfilled without exception. It is stressed that reliability tests must show that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests must demonstrate the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 CHANGE CHARACTERISTICS

4.1 Change description

New polyimide for products in HF5CMOS / HCMOS5 in UMC Taiwan

4.2 Change details

Material	Current process	additional process	Comment
diffusion location	UMC Taiwan	UMC Taiwan	
Passivation	USG-PSG-SiON-PIX (I-8124ER)	USG-PSG-SiON-PIX (HD4100 or LTC9310)	
EWS	ST Singapore	ST Singapore	No change
Assembly location	TSHT (China) ST Bouskoura Morocco	TSHT (China) ST Bouskoura Morocco	No change neither location nor Bill of material

4.3 Test vehicles description

	P/N TSV852AIYST	P/N TSV854AIYPT	P/N LMV824AIYPT
Wafer fab manufacturing location	UMC Taiwan	UMC Taiwan	UMC Taiwan
Technology	HF5CMOS	HF5CMOS	HF5CMOS
Process family	HF5CMOS	HF5CMOS	HF5CMOS
Die finishing back side	RAW SILICON	RAW SILICON	RAW SILICON
Die size (microns)	1062 x 812µm²	1092 x 1322µm²	1092 x 1322µm²
Bond pad metallization layers	AlCu	AlCu	AlCu
Passivation type	USG-PSG-SiON-PIX	USG-PSG-SiON-PIX	USG-PSG-SiON-PIX
Wafer Testing (EWS) information			
Electrical testing manufacturing location	ST Singapore	ST Singapore	ST Singapore
Assembly information			
Assembly site	TSHT China	ST Bouskoura	ST Bouskoura
Package description	MiniSO	TSSOP14	TSSOP14
Molding compound	Hitachi CEL-9220HF10TS	Sumitomo G700KC	Sumitomo G700KC
Frame material	Copper	Copper	Copper
Die attach process	Epoxy glue	Epoxy glue	Epoxy glue
Die attach material	8200T Henkel	Ablestick 8601S-25	Ablestick 8601S-25
Wire bonding process	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding
Wires bonding materials/diameters	CuPd 1 mil	Copper wire 1 mil	Copper wire 1 mil
Lead finishing process	Electroplating	Preplated frame	Preplated frame
Lead finishing/bump solder material	Tin (Sn)	NiPdAu Pre-plated	NiPdAu Pre-plated
Final testing information			
Testing location	TSHT China	ST Bouskoura	ST Bouskoura

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	P/N	Process/ Package	Comments
1	TSV852AIYST	HF5CMOS/MiniSO	
2	TSV854AIYPT	HF5CMOS/TSSOP14	
3	LMV824AIYPT	HF5CMOS/TSSOP14	

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS						Note
						HD4100			LTC9310			
						Lot 1	Lot 2	Lot 3	Lot 1	Lot 2	Lot 3	
HTB High Temp. Bias	N	JESD22 A-108	Tj = 125°C, BIAS	77	168H 500H 1000H 2000H	77 77 77 77	77 77 77 77	77 77 77 77	77 77 77 77	77 77 77 77	77 77 77 77	
HTSL High Temp. Storage Life	N	JESD22 A-103	Ta = 150°C	77	500H 1000 H 2000H	50 50 50	50 50 50	50 50 50	50 50 50	50 50 50	50 50 50	
PC Preconditioning		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times		Final	MSL1	MSL1	MSL1	MSL1	MSL1	MSL1	
UHAST Unbiased humidity accel-erated stress	Y	JESD22 A-102	Pa=2Atm / Ta=121°C	77	96 H	77	77	77	77	77	77	
TC Temperature Cycling	Y	JESD22 A-104	Ta = -55°C to 150°C	77	500cy 1000cy 2000cy	77 77 77	77 77 77	77 77 77	77 77 77	77 77 77	77 77 77	
THB Temperature Humidity Bias	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS	77	168H 500 H 1000 H 2000H	77 77 77 77	77 77 77 77	77 77 77 77	77 77 77 77	77 77 77 77	77 77 77 77	
ESD Electro Static Discharge	-	AEC Q101-001, 002 and 005	HBM	3		3	3	3	3	3	3	
			CDM	3		3	3	3	3	3	3	
LU Latch up	N	AEC Q100-004	LU	6		6	6	6	6	6	6	

ANNEXES

Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTRB High Temperature Reverse Bias **HTFB / HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
THS Temperature Humidity Storage	The device is stored at controlled conditions of ambient temperature and relative humidity.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.

Test name	Description	Purpose
PTC Power & Temperature Cycling	The power and temperature cycling test is performed to determine the ability of a device to withstand alternate exposures at high and low temperature extremes with operating biases periodically applied and removed.	It is intended to simulate worst case conditions encountered in typical applications. Typical failure modes are related to parametric limits and functionality. Mechanical damage such as cracking, or breaking of the package will also be considered a failure provided such damage was not uinduced by fixturing or handling.
EV External Visual	Inspect device construction, marking and workmanship	To verify visual defects on device (form, marking,…).
LI Lead Integrity	Various tests allow determining the integrity lead/package interface and the lead itself when the lead(s) are bent due to faulty board assembly followed by rework of the part for reassembly.	This test is applicable to all throughhole devices and surface-mount devices requiring lead forming by the user.
WBP Wire Bond Pull	The wire is submitted to a pulling force (approximately normal to the surface of the die) able to achieve wire break or interface separation between ball/pad or stitch/lead.	To investigate and measure the integrity and robustness of the interface between wire and die or lead metallization
WBS Wire Bond Shear	The ball bond is submitted to a shear force (parallel to the pad area) able to cause the separation of the bonding surface between ball bond and pad area.	To investigate and measure the integrity and robustness of the bonding surface between ball bond and pad area.
DS Die Shear	This determination is based on a measure of force applied to the die, the type of failure resulting from this application of force (if failure occurs) and the visual appearance of the residual die attach media and substrate/header metallization.	The purpose of this test is to determine the integrity of materials and procedures used to attach semiconductor die or surface mounted passive elements to package headers or other substrates.
PD Physical Dimension	All physical dimension quoted in datasheet of the device are measured.	Verify physical dimensions to the applicable user device packaging specification for dimensions and tolerances.
SD Solderability	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finishes.	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CBM**: Charged Device Model **HBM**: Human Body Model **MM**: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.

Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : New Polyimides for HCMOS5 / HF5CMOS General Purpose Analog products

PCN Reference : ANALOG MEMS SENSORS/26/16321

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

LMV824IYDT	LMV822IYST	TSV852AIYST
TSV852IYST	LMV824AIYPT	TSV851AIYLT
LMV822AIYDT	LMV824AIYDT	LMV821IYLT
TSV854AIYPT	LMV821AIYLT	LMV822IYDT
TSV852IYDT	LMV822AIYST	TSV851IYLT
LMV824IYPT	TSV854IYPT	TSV852AIYDT

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