2603251786 SiWx917 Data Sheet v1.2, SiWG917 SoC Errata v0.4 and SiWT917 RCP Errata v0.1 Release

PCN Issue Date: Mar 25, 2026 **Effective Date:** Jul 01, 2026

PCN Type: Datasheet; Errata

Description of Change

Silicon Labs is pleased to announce the release of data sheet version 1.2 for SiWG917 (SoC), SiWN917 (NCP) and SiWT917 (RCP), jointly referred to as the SiWx917 devices.

Links to data sheets:
SiWG917 SoC: https://www.silabs.com/documents/public/data-sheets/siwg917-datasheet.pdf
SiWN917 NCP: https://www.silabs.com/documents/public/data-sheets/siwn917-ncp-datasheet.pdf
SiWT917 RCP: https://www.silabs.com/documents/public/data-sheets/siwt917-rcp-datasheet.pdf

Silicon Labs also announces the release of errata version 0.4 for SiWG917 (SoC) and errata version 0.1 for SiWT917 (RCP) devices.

Links to errata:
SiWG917 SoC: https://www.silabs.com/documents/public/errata/siwg917-soc-ic-errata.pdf
SiWT917 RCP: https://www.silabs.com/documents/public/errata/siwt917-rcp-ic-errata.pdf

Software Impact Description

For the PSRAM corruption issue described in SiWG917 Errata v0.4 (DCACHE_E301), use the documented workaround options corresponding to the applicable WiSeConnect SDK version.

Reason for Change

SoC data sheet
Revision 1.2
• Updated Block Diagram
• Updated Section 1 feature list including increase in number of Bluetooth simultaneous connections
• Removed D-Cache support for PSRAM in section 5
• Removed GPIO_TIMESTAMP from UULP-Peripherals in section 5.4
• Updated Table 5.9 List of Wakeup sources in different states
• Updated section 5.6.2.2 Digital to Analog Converter (DAC) Max sampling frequency for DAC_CLK is updated from 5 MHz to 2.5 MHz
• Added new section 5.13 Host Interface Peripherals
• Updated SoC/ULP GPIO Pin multiplexing modes configurations in Table 6.5 & 6.9; removed ULP GPIO modes 8,9,10,11 in table 6.6 & 6.10; removed AGPIO_3 - ULP_GPIO_3 from table 6.8; Updated Table 6.11 Peripheral Interface Options for some GPIOs
• Updated Table 6.3. Chip Packages - Peripheral Interfaces: Replaced HighZ default state with High for GPIO_30/SDIO_D3 pin
• Updated Note in Table 7.13 40 MHz Crystal specifications
• Updated Various WLAN and Bluetooth Transmitter/Receiver tables with additional notes and test conditions.
• Updated Bluetooth LE Current typical consumption in section 7.63
• Updated section 8 Reference schematics, BOM and Layout guidelines

SoC errata
Revision 0.4
• Added 7. ANTIROLLBACK_E301 – Anti-rollback functionality requires M4 firmware version must be same or greater than NWP firmware version
• Added 8. DCACHE_E301 – PSRAM Data Corruption whenever D-Cache is enabled
• Added 9. GPIO_TIMESTAMP_E301 – GPIO Timestamp removed from the data sheet

NCP data sheet
Revision 1.2
• Updated Table 6.3. Chip Packages - Peripheral Interfaces: Replaced HighZ default state with High for GPIO_30/SDIO_D3 pin
• Updated Note in Table 7.13 40 MHz Crystal specifications
• Updated Various WLAN and Bluetooth Transmitter/Receiver tables with additional notes and test conditions
• Updated Bluetooth LE Current typical consumption in section 7.33
• Updated notes in section 8. Reference Schematics, BOM and Layout Guidelines

RCP data sheet
Revision 1.2
• Updated Table 6.3. Chip Packages - Peripheral Interfaces: Replaced HighZ default state with High for GPIO_30/SDIO_D3 pin
• Updated Note in Table 7.13 40 MHz Crystal specifications
• Updated Various WLAN and Bluetooth Transmitter/Receiver tables with additional notes and test conditions
• Updated Bluetooth LE Current typical consumption in section 7.26
• Updated notes in section 8. Reference Schematics, BOM and Layout Guidelines

RCP errata
Revision 0.1
• Initial release
• Added OSC_32kHz_E321: Recommendation for an External XTAL as Mandatory Requirement

For complete list of changes, please refer to data sheet or errata revision history.

Impact on Form, Fit, Function, Quality, Reliability

No impact on Form, Fit, Quality or Reliability. Function is impacted as follows:

SoC data sheet
Revision 1.2
• Removed GPIO_TIMESTAMP from UULP-Peripherals
• Removed D-Cache support for PSRAM
• Updated Max sampling frequency for Digital to Analog Converter (DAC) from 5 MHz to 2.5 MHz in section 5.6.2.2
• Updated Table 6.3. Chip Packages - Peripheral Interfaces: Replaced HighZ default state with High for GPIO_30/SDIO_D3 pin
• Updated SoC/ULP GPIO Pin multiplexing modes configurations in Table 6.5 & 6.9; removed ULP GPIO modes 8,9,10,11 in table 6.6 & 6.10; removed AGPIO_3 - ULP_GPIO_3 from table 6.8; Updated Table 6.11 Peripheral Interface Options for some GPIOs
• Bluetooth LE Current typical consumption values have been updated in section 7.63. They have increased from 36 µA to 48 µA for 1.28s connection interval parameter and 115 µA to 149 µA for 200 ms connection interval

NCP data sheet
Revision 1.2
• Updated Table 6.3. Chip Packages - Peripheral Interfaces: Replaced HighZ default state with High for GPIO_30/SDIO_D3 pin
• Bluetooth LE Current typical consumption values have been updated in section 7.33. They have increased from 36 µA to 41 µA for 1.28s connection interval parameter and 115 µA to 125 µA for 200 ms connection interval

RCP data sheet
Revision 1.2
• Updated Table 6.3. Chip Packages - Peripheral Interfaces: Replaced HighZ default state with High for GPIO_30/SDIO_D3 pin
• Bluetooth LE Current typical consumption values have been updated in section 7.26. They have increased from 36 µA to 41 µA for 1.28s connection interval parameter and 115 µA to 125 µA for 200 ms connection interval

Product Identification

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Existing Part #
SIWG917M100MGTBA
SIWG917M100MGTBAR
SIWG917M110LGTBA
SIWG917M110LGTBAR
SIWG917M111MGTBA
SIWG917M111MGTBAR
SIWG917M111XGTBA
SIWG917M111XGTBAR
SIWG917M121XGTBA
SIWG917M121XGTBAR
SIWG917M141XGTBA
SIWG917M141XGTBAR
SIWN917M100LGTBA
SIWN917M100LGTBAR
SIWT917M100XGTBA
SIWT917M100XGTBAR
```

Last Date of Unchanged Product: Jul 01, 2026

Qualification Samples

NA

Customer Response

Lack of acknowledgment of the PCN within 30 days constitutes acceptance of the change,Ref. JEDEC-J-STD-046.

To request further data or inquire about this notification, please contact your Silicon Labs sales representative. A list of Silicon Labs sales representatives is available at https://www.silabs.com.

Customers may approve early PCN acceptance by emailing approval, along with PCN # to PCN@silabs.com

User Registration

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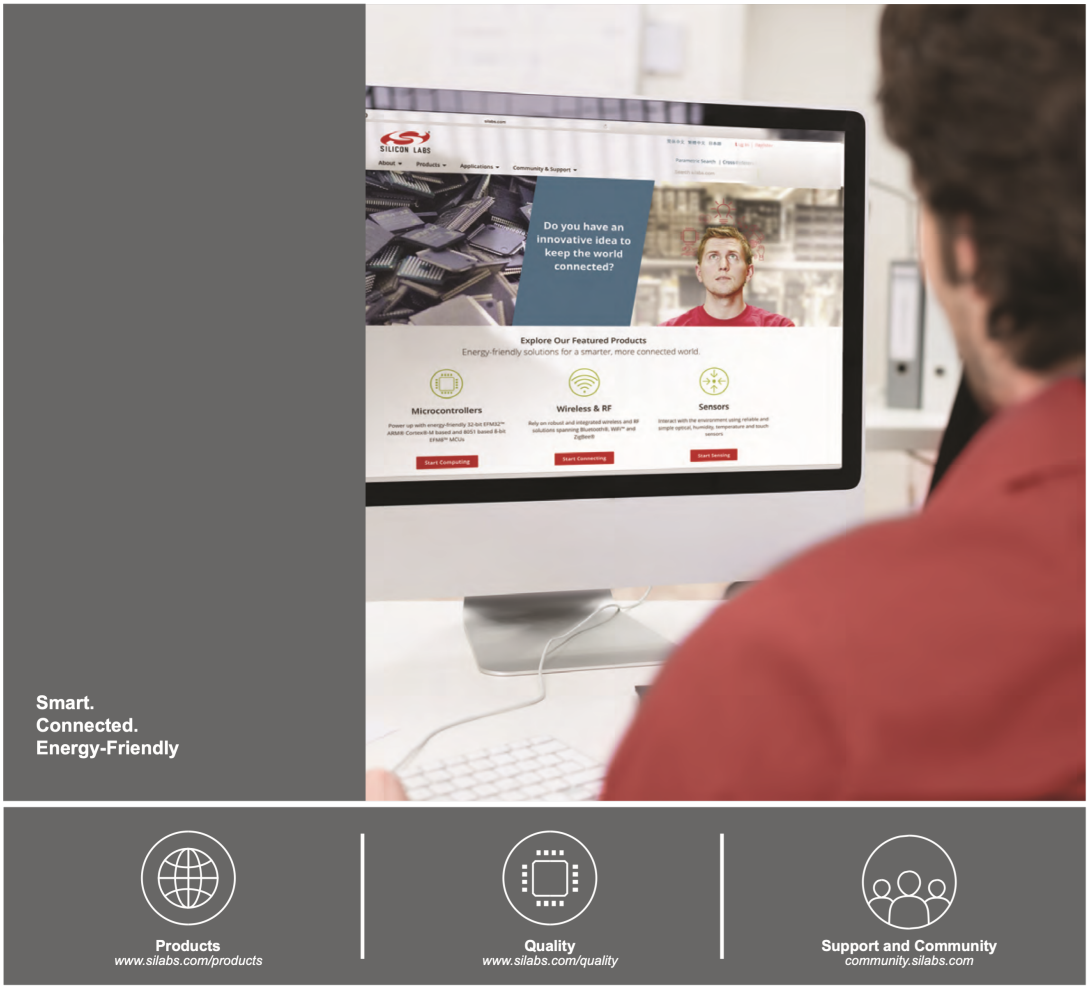
Qualification Data

NA



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