CoolGaN™ bidirectional switch 650 V G5 cycloconverter-based solar microinverter

About this document

Scope and purpose

This document provides a comprehensive functional description and guide for the REF_500W_CYCLO_BDSGAN solar microinverter reference design based on a cycloconverter topology. The circuit functionality is discussed in detail. The system implementation including converter architecture, control algorithms, and firmware is also described. Waveforms are shown under all operating conditions, and test measurement data is presented.

Intended audience

This application note is intended for design engineers, applications engineers, and students.

Infineon components featured

- OptiMOS™ 6 power MOSFET 80 V ISC014N08NM6, 1.45 mΩ N-channel in a 5 mm x 6 mm SuperSO8 package
- OptiMOS™ 6 power MOSFET 80 V ISC056N08NM6, 5.6 mΩ N-channel in a 5 x 6 mm SuperSO8 package
- CoolGaN™ bidirectional switch 650 V G5 IGLT65R055B2, 55 mΩ enhancement mode bidirectional GaN HEMT with GIT gate structure in top-side cooled PG-HDSOP-16 package
- EiceDRIVER™ 120 V 2EDL8034F5B, 3 A/4 A source/sink isolated high-side and low-side gate driver in SO-8 (PG-DSO-8) package
- EiceDRIVER™ 2EDR7259X 5 A/9 A source/sink dual-channel gate driver for CoolMOS™ and CoolGaN™
- PSOC™ Control C3 PSC3M5FDS2AFQ1, Arm® Cortex®-M33 32-bit MCU+FPU+DSP, 180 MHz, up to 256 KB flash/64 KB SRAM, real-time control

Keypoints

- Specifications for a high-efficiency microinverter design based on cycloinverter topology employing bidirectional GaN HEMT devices at the AC switching side
- Set the control algorithms, implement the firmware for the microinverter, design the PCB layout, and test the performance

About this product family

Product family

Infineon's CoolGaN™ solution offers unmatched quality that operates at higher switching speeds resulting in lower power losses, higher efficiency paving the way for smaller and lighter power supplies with the same power supplies with the same size but increased power capability.

Target applications

Solar microinverters

Important notice

"Evaluation Boards and Reference Boards" shall mean products embedded on a printed circuit board (PCB) for demonstration and/or evaluation purposes, which include, without limitation, demonstration, reference and evaluation boards, kits and design (collectively referred to as "Reference Board").

Environmental conditions have been considered in the design of the Evaluation Boards and Reference Boards provided by Infineon Technologies. The design of the Evaluation Boards and Reference Boards has been tested by Infineon Technologies only as described in this document. The design is not qualified in terms of safety requirements, manufacturing and operation over the entire operating temperature range or lifetime.

The Evaluation Boards and Reference Boards provided by Infineon Technologies are subject to functional testing only under typical load conditions. Evaluation Boards and Reference Boards are not subject to the same procedures as regular products regarding returned material analysis (RMA), process change notification (PCN) and product discontinuation (PD).

Evaluation Boards and Reference Boards are not commercialized products, and are solely intended for evaluation and testing purposes. In particular, they shall not be used for reliability testing or production. The Evaluation Boards and Reference Boards may therefore not comply with CE or similar standards (including but not limited to the EMC Directive 2004/EC/108 and the EMC Act) and may not fulfill other requirements of the country in which they are operated by the customer. The customer shall ensure that all Evaluation Boards and Reference Boards will be handled in a way which is compliant with the relevant requirements and standards of the country in which they are operated.

The Evaluation Boards and Reference Boards as well as the information provided in this document are addressed only to qualified and skilled technical staff, for laboratory usage, and shall be used and managed according to the terms and conditions set forth in this document and in other related documentation supplied with the respective Evaluation Board or Reference Board.

It is the responsibility of the customer's technical departments to evaluate the suitability of the Evaluation Boards and Reference Boards for the intended application, and to evaluate the completeness and correctness of the information provided in this document with respect to such application.

The customer is obliged to ensure that the use of the Evaluation Boards and Reference Boards does not cause any harm to persons or third-party property.

The Evaluation Boards and Reference Boards and any information in this document is provided "AS IS" without any warranty and liability and Infineon Technologies disclaims any warranties, express or implied, including but not limited to warranties of non-infringement of third-party rights and implied warranties of fitness for any purpose, or for merchantability.

Infineon Technologies shall not be responsible for any damages resulting from the use of the Evaluation Boards and Reference Boards and/or from any information provided in this document. The customer is obliged to defend, indemnify and hold Infineon Technologies harmless from and against any claims or damages arising out of or resulting from any use thereof.

Infineon Technologies reserves the right to modify this document and/or any information provided herein at any time without further notice.

Safety precautions

Note: *Please note the following warnings regarding the hazards associated with development systems*

Table 1 **Safety precautions**

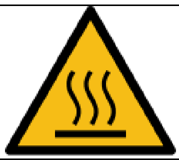
	**Warning:** *This reference design is intended for evaluation in a laboratory environment using a grid simulator and observing high voltage safety precautions. It is NOT intended for connection directly to the AC power grid and is not certified for this purpose! DO NOT CONNECT DIRECTLY TO THE AC POWER GRID!*
	**Warning**: *The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the system, wait at least ten minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with power electronics and trained in testing and evaluating such power boards should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *The reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

Table of contents

Table of contents

1 Introduction

1.1 Microinverter basics

Solar microinverters along with optimizers fall into the category of module-level power electronics (MLPE). These modules are attached underneath solar panels typically installed on a roof. Microinverters convert DC current converted from sunlight by solar panels[1], to AC output to be connected to the power grid. Devices that can transfer power to the grid are referred to as "grid tied". Microinverters differ from central and string inverters because, instead of receiving power from an array of PV panels, they operate at the panel level in a modular manner with their outputs connected in paralleled.

In a typical example, the Enphase IQ8+ microinverter is rated for a continuous output power of 290 VA[2] and an input power of 235 W to 440 W from a voltage of 16 V to 58 V. The advantage of microinverters and other MLPE devices such as power optimizers, is that the maximum power point can be utilized for each individual PV panel. In this way, shading of one panel in the array does not limit the power conversion ability of other panels receiving more sunlight as it would with series connected PV panels. Because of this, MLPE installations produce more solar energy.

Traditional string inverters are much larger and bulkier than microinverters, which are slightly larger than the junction box on a solar panel and typically weigh 2 lbs to 4 lbs.. A solar installation with microinverters is costlier overall than one using a string inverter.

Most solar microinverters are plug-and-play devices, meaning they can be connected and operated in a few easy steps or disconnected with minimal time and tools required. They usually include built-in MC4 connectors for quick and easy connection.

Microinverters are generally supported with remote monitoring technology so that the status of each device in the installation and hence the solar energy performance of each panel can be monitored with a smartphone application.

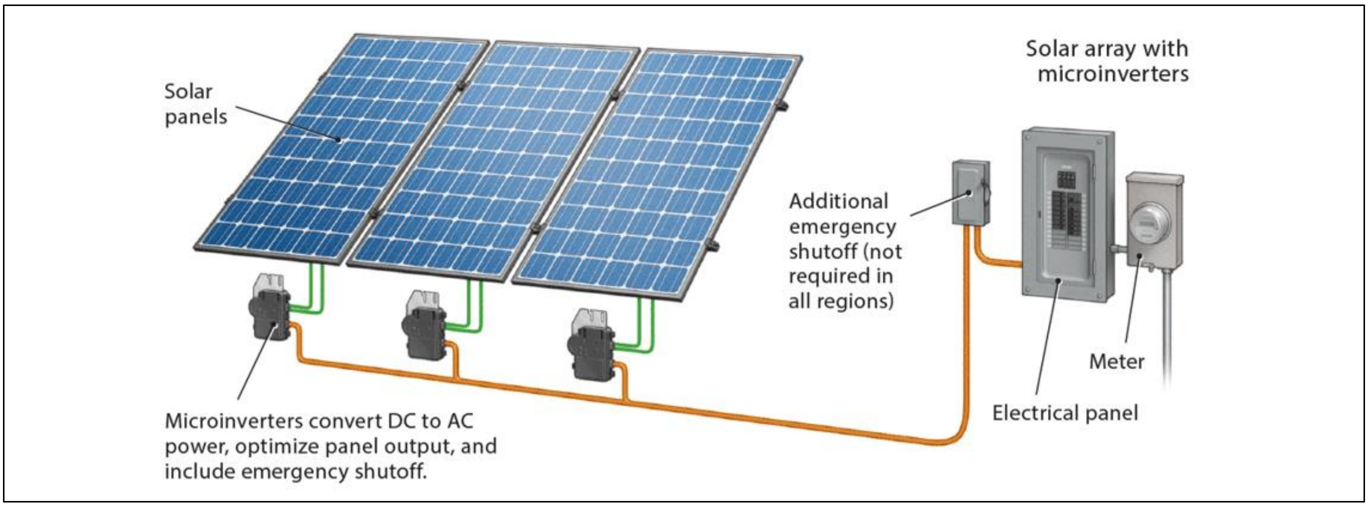


Figure 1 Solar installation using microinverters

[1] Also known as PV (photovoltaic) panels.

[2] The AC output rating in VA indicates that the microinverter can transfer active and reactive power to the grid.

1.2 Microinverter topologies

Microinverters are based on a two-stage architecture, the front-end stage is the MPPT block which converts PV panel voltage to a higher voltage- suitable for the back-end inverter stage to convert to AC to be tied to the grid.

1.2.1 Traditional microinverter topologies

Microinverter designs have traditionally used a DC to DC front-end stage to produce a high voltage DC bus voltage, which is then converted to line frequency sinusoidal AC by the back-end inverter stage.

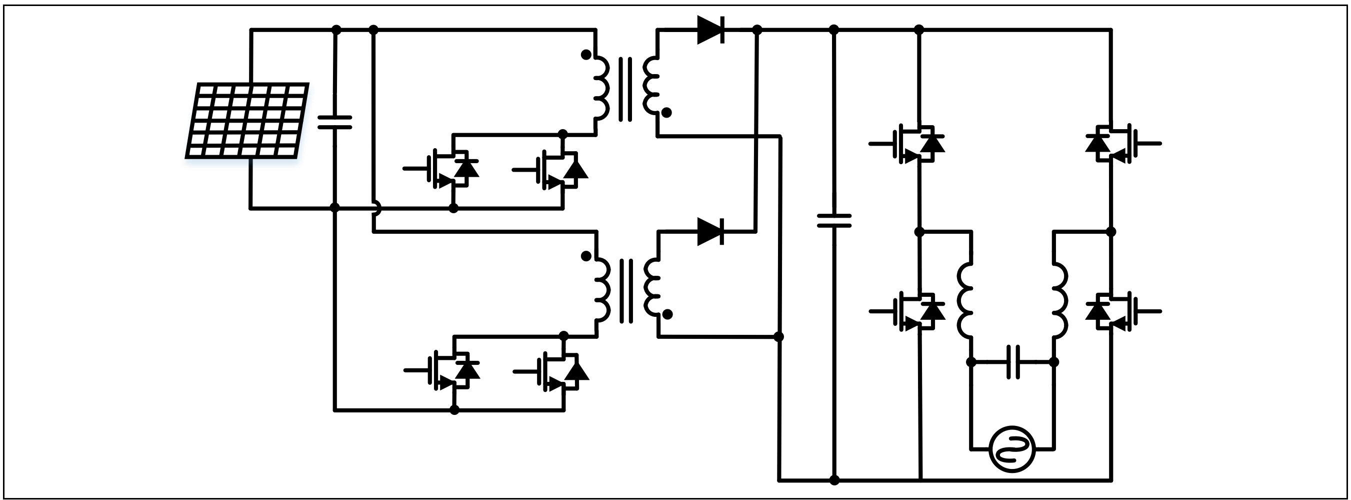


Figure 2 **Flyback + full-bridge type microinverter**

The voltage source flyback based MPPT followed by a full bridge inverter is less complicated but has lower efficiency than alternative design concepts. In the above example, efficiency is improved by using parallel flyback stages. A more popular current source flyback implementation is shown in the following figure.

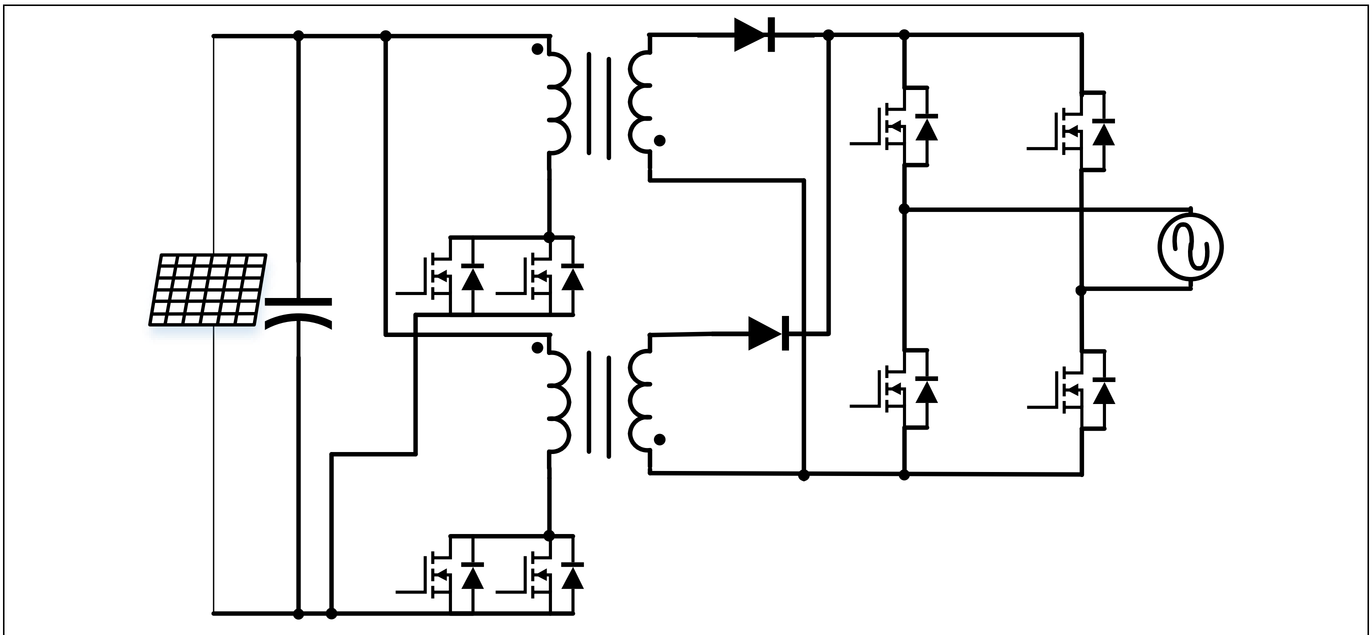


Figure 3 **Flyback + unfolding type microinverter**

The dual-active bridge offers better efficiency than the flyback by eliminating the rectifier diodes and using a direct energy transfer transformer based current source approach. The output bridge is used as a low frequency unfolding stage only. This design is more complex than the flyback but simpler than a cycloinverter.

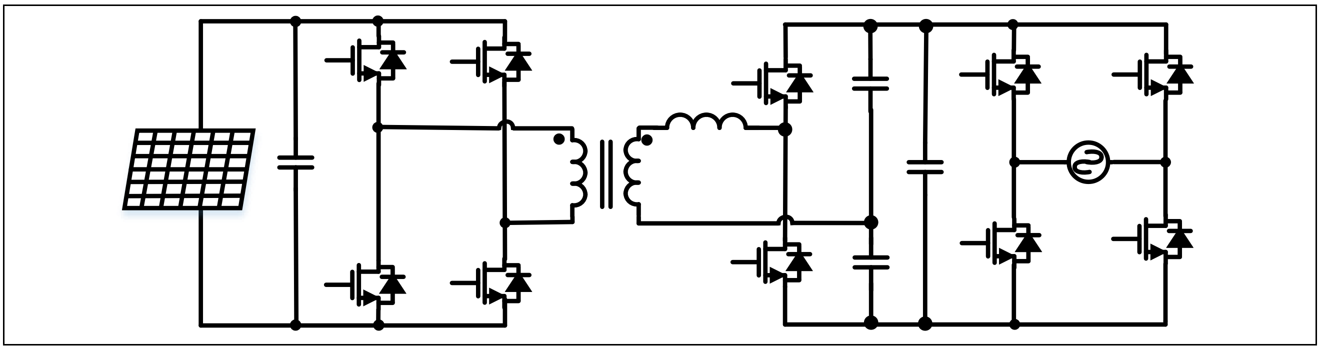


Figure 4 **Dual active bridge and unfolding type microinverter**

1.2.2 What is a cycloinverter?

A broad definition of a cycloinverter (also known as a cycloconverter) is a power conversion system, which converts AC electrical power directly from one frequency to another without the need for an intermediate DC link, hereby eliminating conduction losses from the rectifying diodes used in other topologies to improve efficiency. The cycloinverter is a resonant design able to operate with soft-switching over a wide operating range.

Infineon's REF_500W_CYCLO_BDSGAN reference design is based on a cycloinverter topology based on a full bridge primary stage, which employs a bidirectional switch. A detailed description of the topology and theory of operation is provided in Section 5.

Figure 5 **REF_500W_CYCLO_BDSGAN reference design board**

1.2.2.1 Benefits of bidirectional GaN

CoolGaN™ BDS 650 V G5 offers a significant improvement in system efficiency and power density compared to traditional back-to-back unidirectional solutions. The cycloinverter efficiency depends on achieving zero voltage switching (ZVS) over a wide range of line and load, which is explained in more detail in this document. Since C_{OSS} for GaN power switches is inherently much lower than for silicon MOSFET devices with much less variation over voltage, using GaN enables ZVS operation over a wider range with reduced dead-time, thereby enabling efficiency improvement.

GaN transistors operate laterally, which allows the monolithic integration of several devices on a single chip. Compact switches able to block high voltages in both polarities provides high-performance bidirectional switches in a single package offering significant space saving to offer an area/cost advantage over conventional realizations with vertical MOSFET switches by almost a factor of 4.

Infineon's CoolGaN™ GIT technology is based on a hybrid-drain HEMT with p-GaN gate resulting in a robust normally off power switch. To deal with the particularities of this concept, an innovative differential gate-drive concept has been implemented. The isolated gate drive circuit based on Infineon's EiceDRIVER™ 2EDR7259X provides negative V_{GS} voltage, which leads to safe off-states during switching transients. Additionally, it protects the GaN switch against spurious turn-on.

2 Specifications

2.1 Electrical characteristics

2.1.1 Input DC side

Table 1 Input operating parameters

Parameter	Value
PV module compatibility	60/66/72/78 cells
Minimum/Maximum input voltage	16/60 V
Minimum/Maximum Start-up voltage	22/58 V
Minimum/Maximum MPPT voltage	25/50 V
Maximum short-circuit DC input current	18 A

2.1.2 Output AC side

Table 2 Output operating conditions

Condition	Value
Maximum continuous output power	500 W
AC nominal (L-L) voltage	240 VRMS
AC (L-L) voltage operating range	185-276 VRMS
Maximum continuous output current	2.1 ARMS
Nominal line frequencies supported[1]	50/60 Hz
Total harmonic distortion of current	<5% for >50% load condition
Grid-tied power factor setting range	-0.8 to 1, +0.8 to 1
Off-grid mode minimum load	50 W

[1] The default line frequency setting is 60 Hz. A firmware parameter change is required for 50 Hz operation.

2.2 Mechanical specifications

2.3 Environment and cooling

Table 3 Ambient operating temperature

Condition	Description
Testing ambient	Room temperature (~25 °C)
Cooling	Natural convection – no fans Optional heatsink

2.3.1 Dimensions and weight

Table 4 Dimension and weight limits

Specification	Value
Enclosure	No enclosure provided
Dimensions (H x W x D)	190 mm x 145 mm x 35 mm
Weight	0.7 kg

Note: Size includes fully populated PCB and heatsink and excludes connectors and possible housing.

2.3.2 Input and output connectors

	MC4
Cable Cross-Section (mm^2)	2.5 - 10
Contact Material	Tin-platted copper
Rated Current	39 - 104A
Max. Voltage	1,000V
IP Index	IP65
Max. Temperature	105°C
Safety Class	II
Safety Mechanism	Plug lock
Locking/Unlocking Tool	Useful but not required

Figure 6 Connection system, DC side, MC4 connectors matching the PV panel output

These connectors are not supplied as part of the REF_500W_CYCLO_BDSGAN reference design kit but if needed can be attached to the board via ring terminals with sufficient current rating.

2.4 Efficiency requirements

Table 5 Efficiency requirements

Efficiency type	Requirement
Peak efficiency	> 97%
CEC weighted efficiency	> 96%

CEC weighted efficiency is calculated as in the following equation:

$$(0.04\ x\ Eff@10\%)\ +\ (0.05\ x\ Eff@20\%)\ +\ (0.12\ x\ Eff@30\%)\ +\ (0.21\ x\ Eff@50\%)\ +\ (0.53\ x\ Eff@75\%)\ +\ (0.05\ x\ Eff@100\%)$$

Equation 1

Efficiency is measured at Tamb = 25°C, Vin = 35 V, Vout = 240 V_{RMS} after at least 30-minutes operation.

2.5 Signal sensing and protections

Table 6 Fault protections

Signals	Sensing method	Protection
DC voltage	Resistor divider network	OV, UV
DC current	Current shunt resistor	OC
AC voltage	Resistor divider network	OV, UV, OF, UF
AC current	Hall current sensor	OC
Resonant current	Current transformer	OC
Temperature	Resistance temperature detector	OTP

Differential amplifier circuits based on operational amplifiers are used in most of the cases listed above to scale the measured signals appropriately for the MCU ADC inputs in the zero to 3.3 V range.

3 Control and communication

The control and communication is based on the Infineon PSOC™ Control C3 MCU.

3.1.1 Control functionality

The following supervision, protection, and performance measurement are implemented:

- System state machine
- MPPT incremental conductance algorithm
- Grid synchronization and grid tie operation
- Single Microinverter standalone operation
- Reactive power control
- Software protection for fault conditions detailed in the above table
- MPPT remove option to test with a regular current DC source at input
- Soft switching range > 50% @ rated power

3.1.2 Connectivity

- **Programmer/debugger type:** Segger J-Link supporting SWD interface
- **Programmer/debugger interface:** Arm® Serial Wire Debug (SWD) interface (P3)
- **Control interface:** UART1 serial port (P1)
  - **Baud rate:** 115200
  - **Flow control:** None
  - **Check bit:** None
  - **Stop bits:** 1
- **Graphical User Interface (GUI) tool:** Infineon Cyclo uInverter Commander

4 Schematics

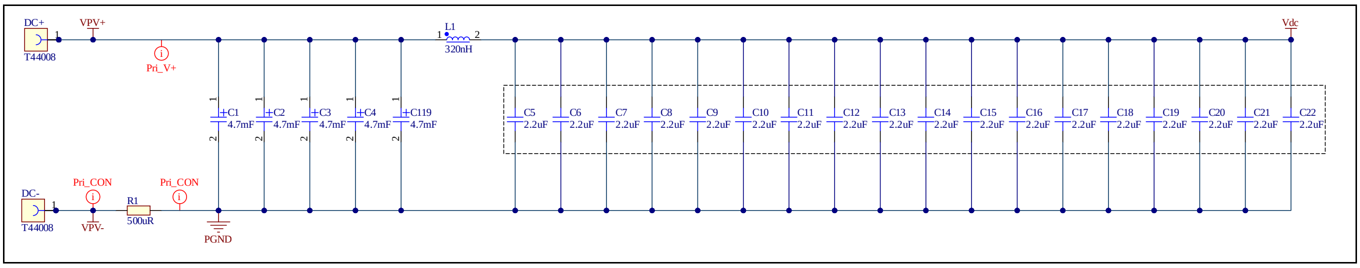


Figure 7 PV input section

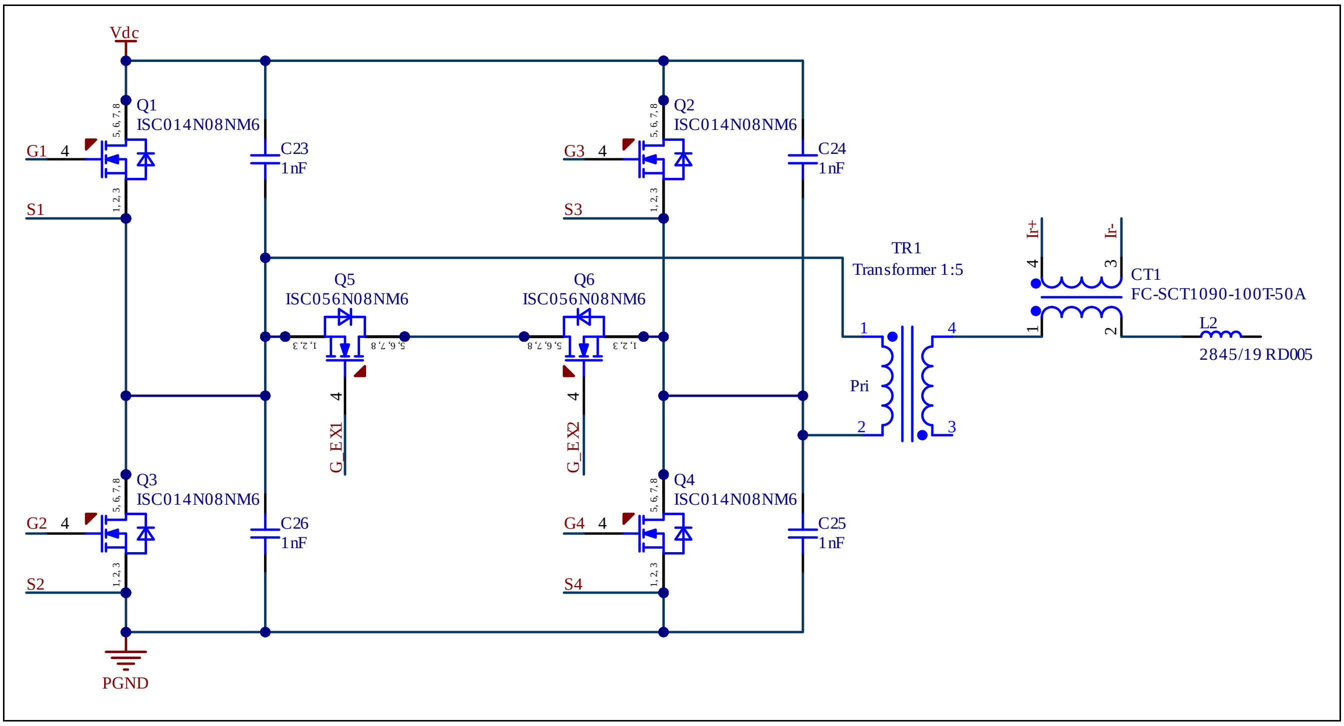


Figure 8 Primary side and step-up transformer

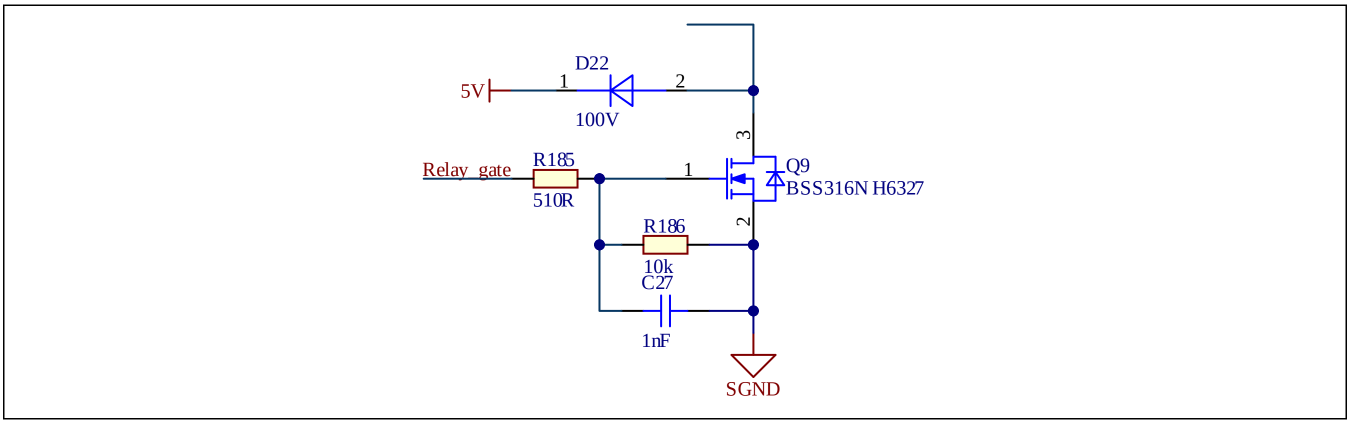


Figure 9 Relay drive circuit

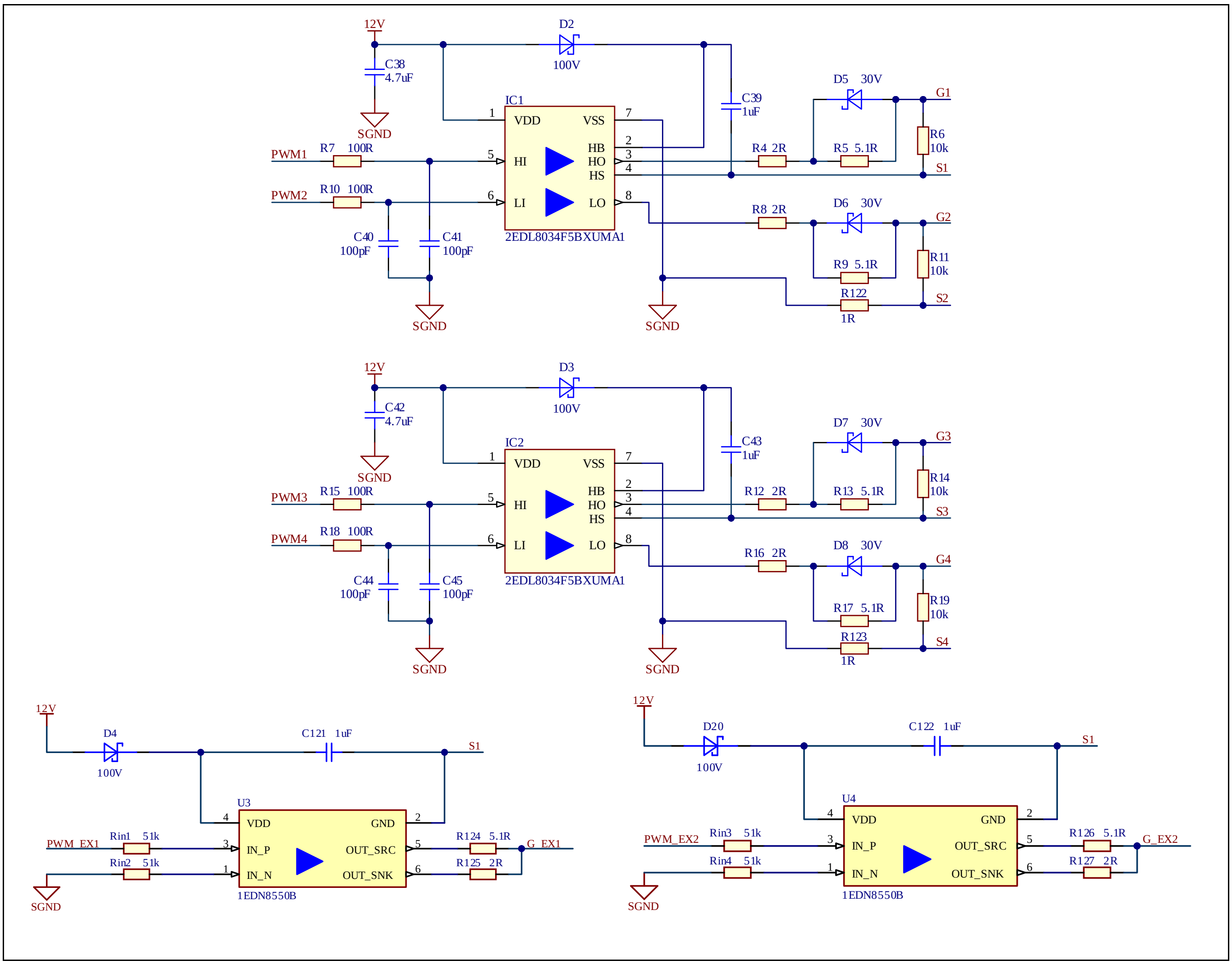


Figure 10 Primary side gate drivers

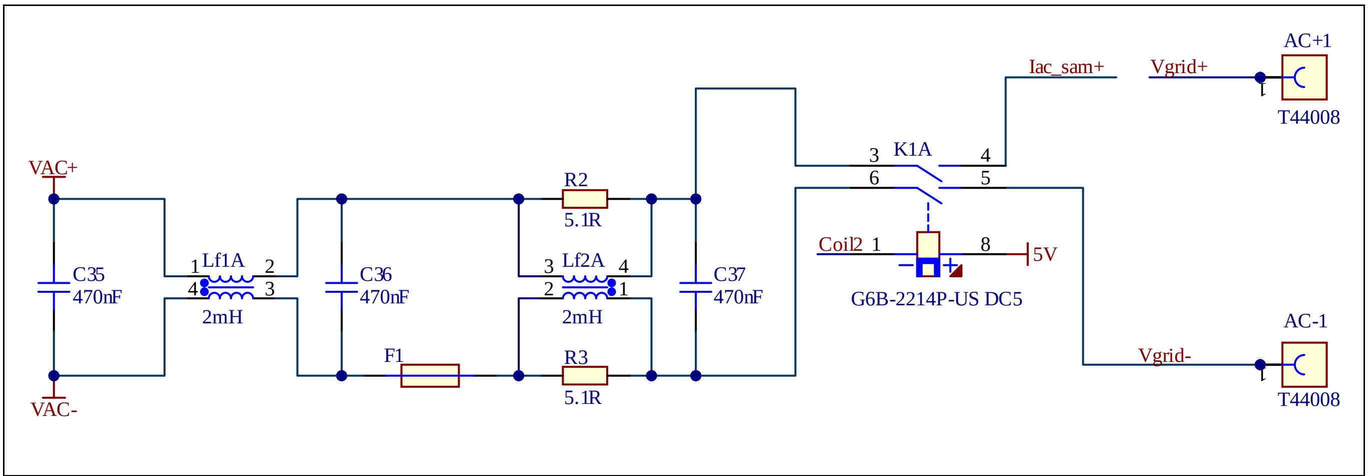


Figure 11 AC side, filter, and relay contacts

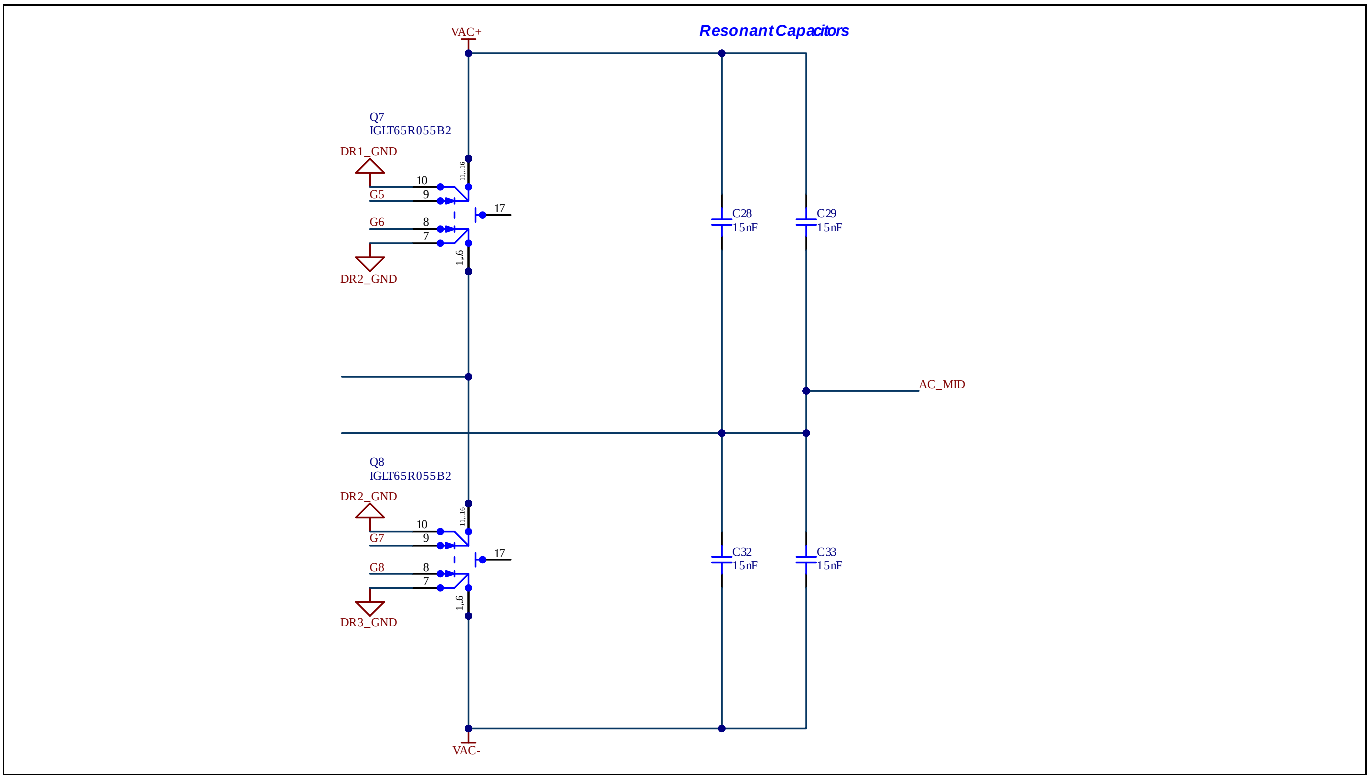


Figure 12 Secondary side

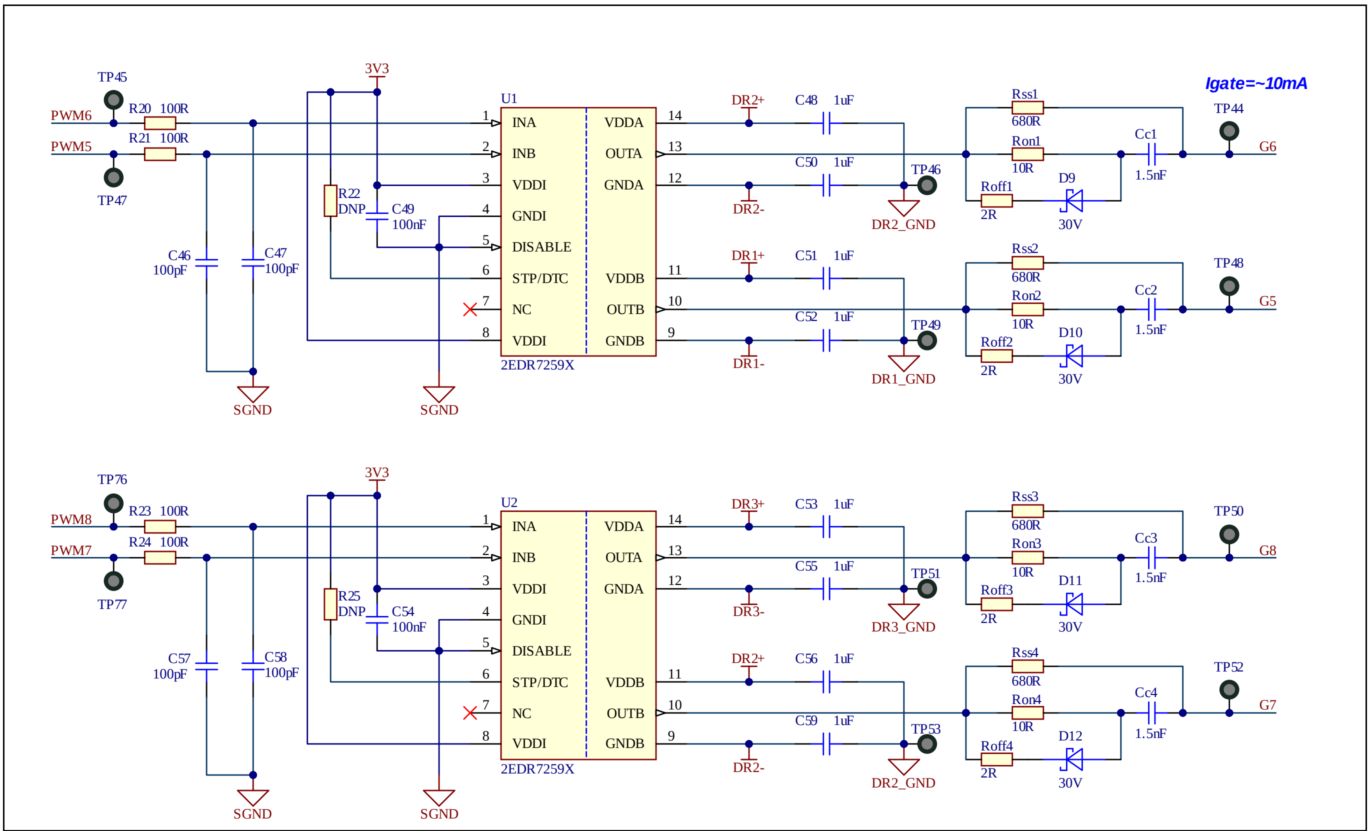


Figure 13 Secondary side gate drivers

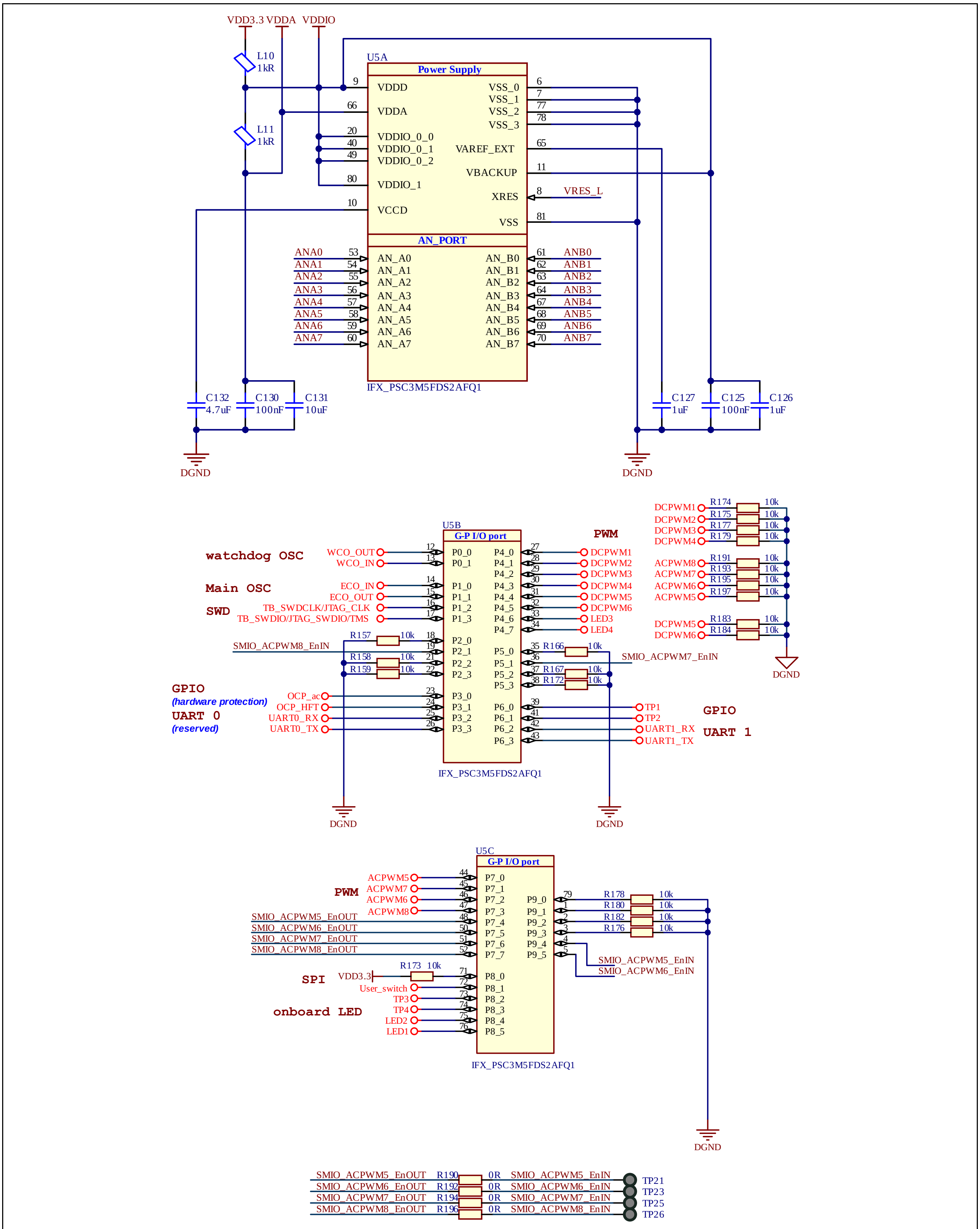


Figure 14 Microcontroller section

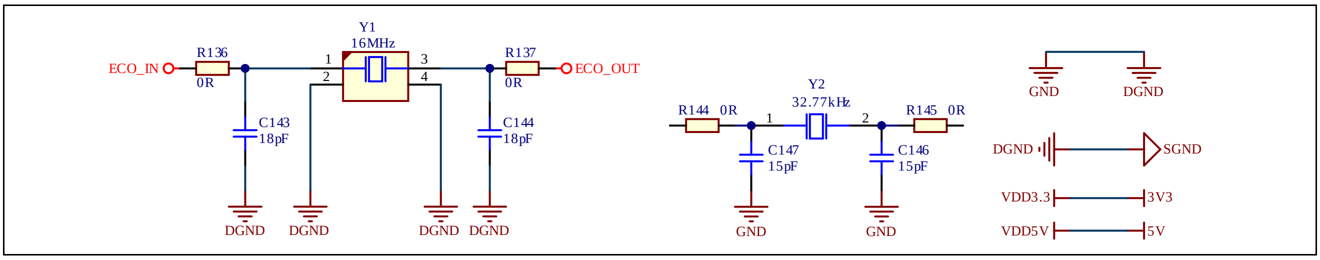


Figure 15 Oscillators, ground, and 3.3 V, 5 V connections

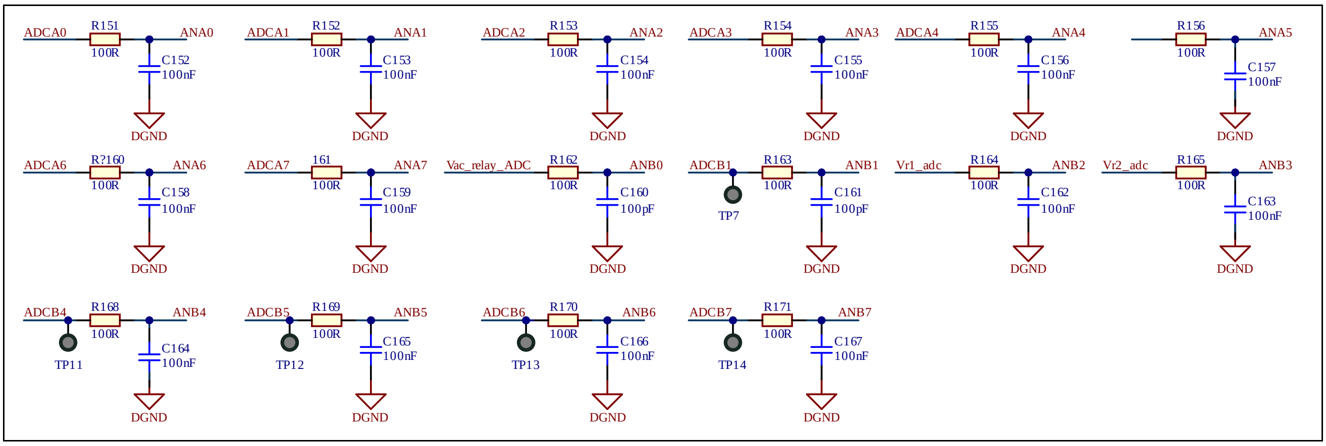


Figure 16 ADC input filtering

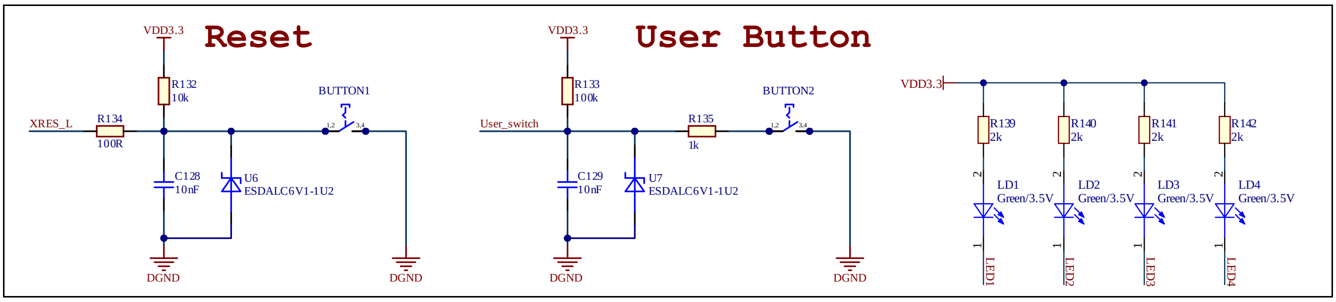


Figure 17 Reset and User buttons and LEDs

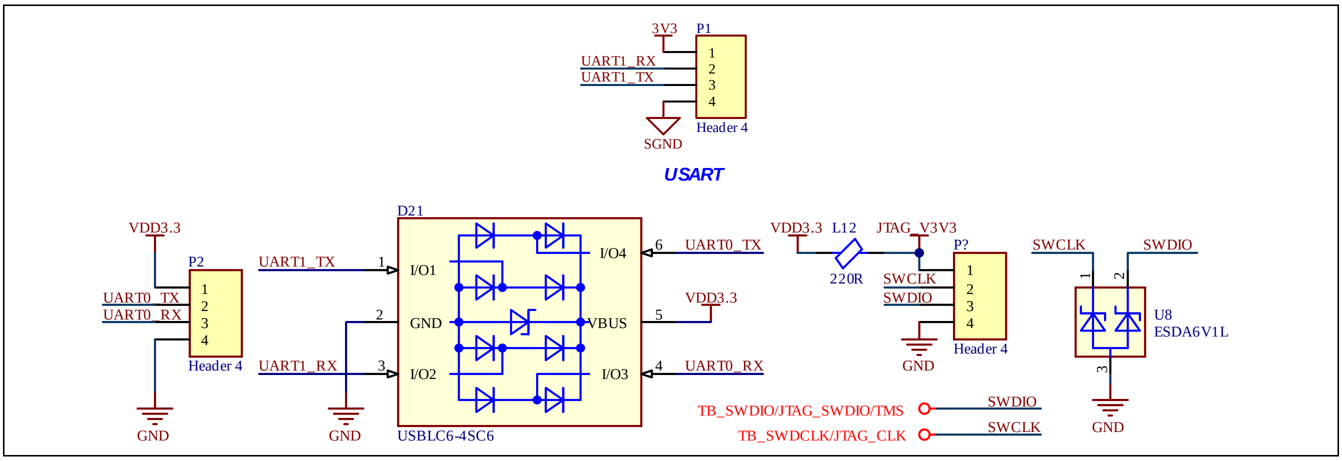


Figure 18 Communication

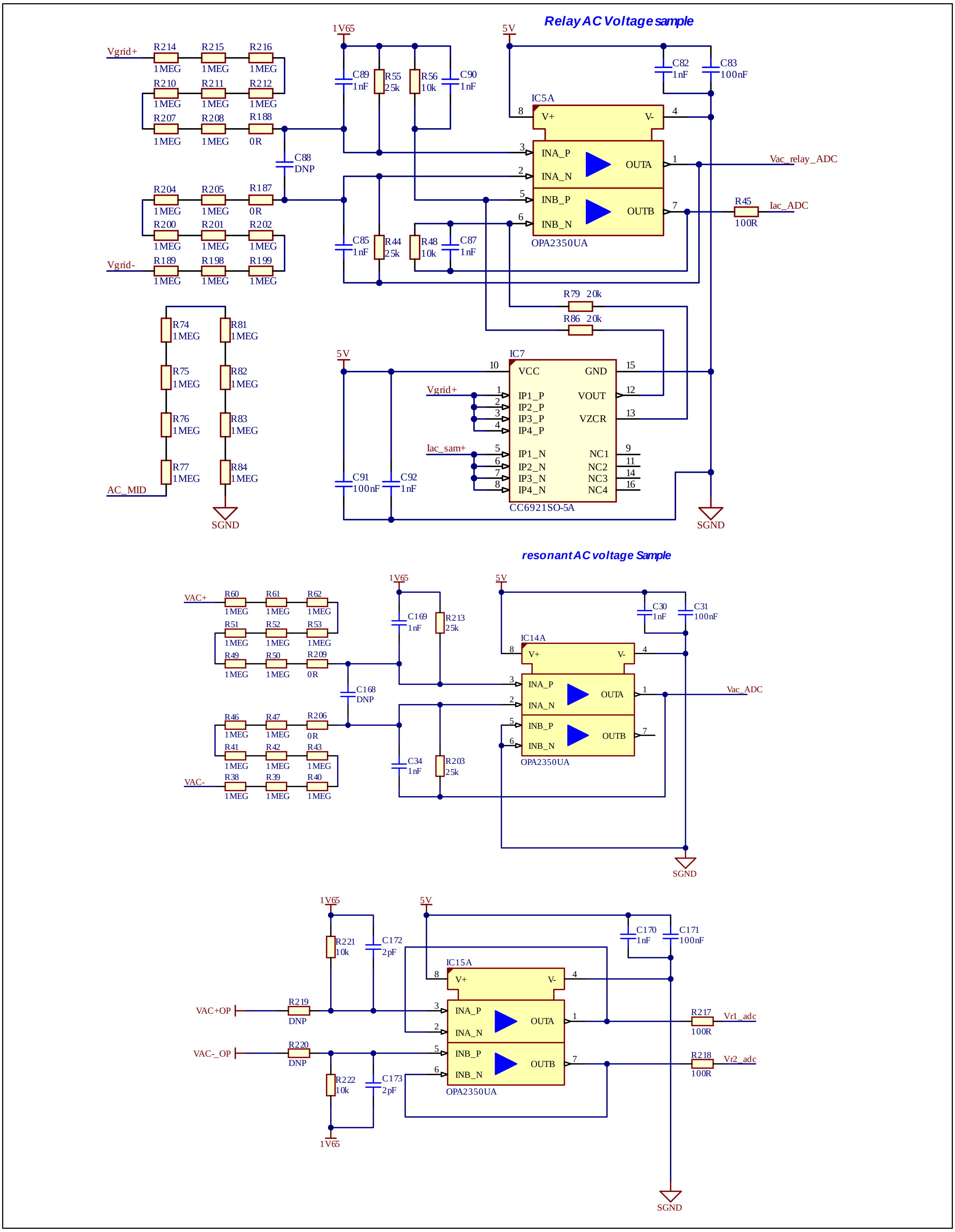


Figure 19 AC voltage sensing

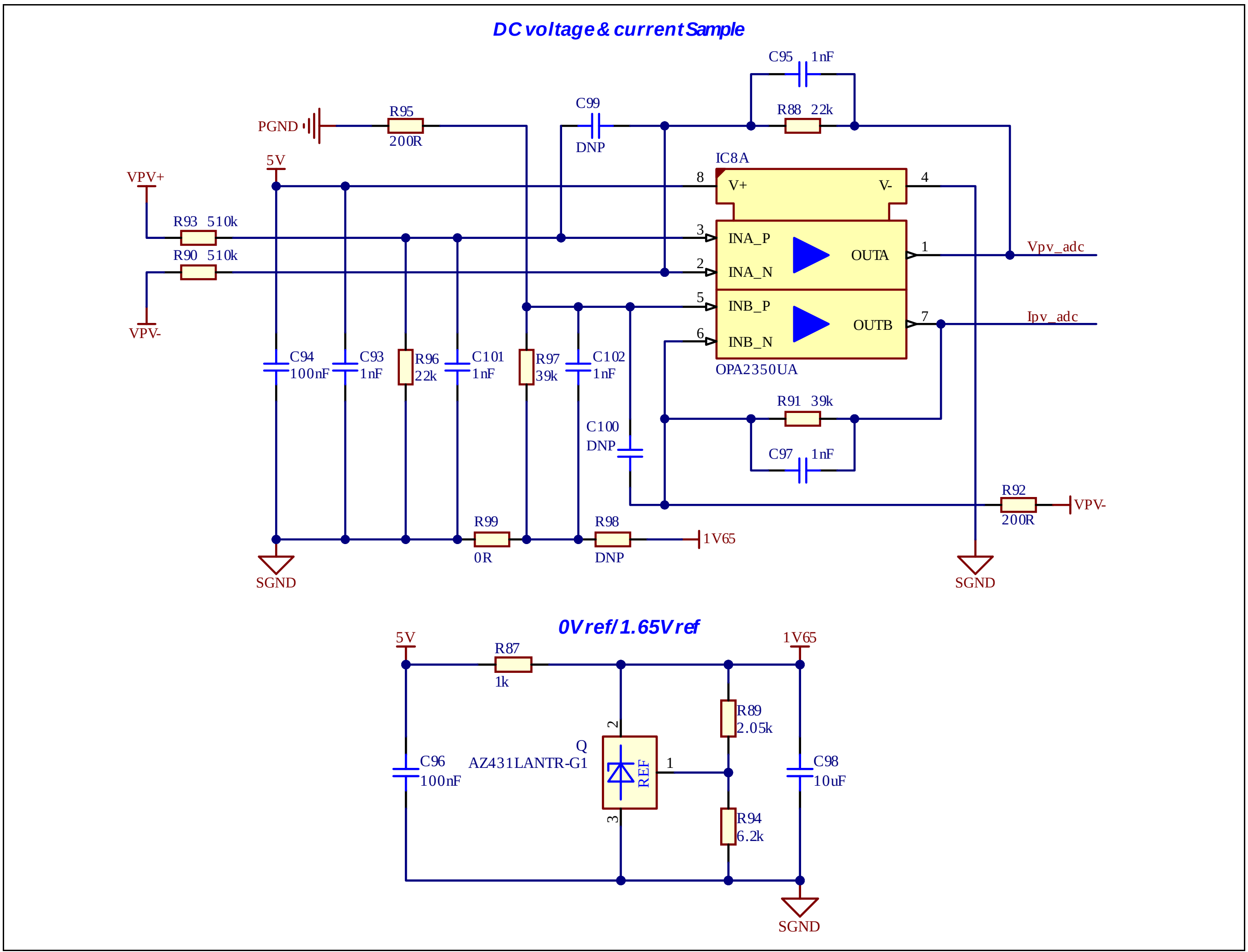


Figure 20 PV input DC voltage sensing

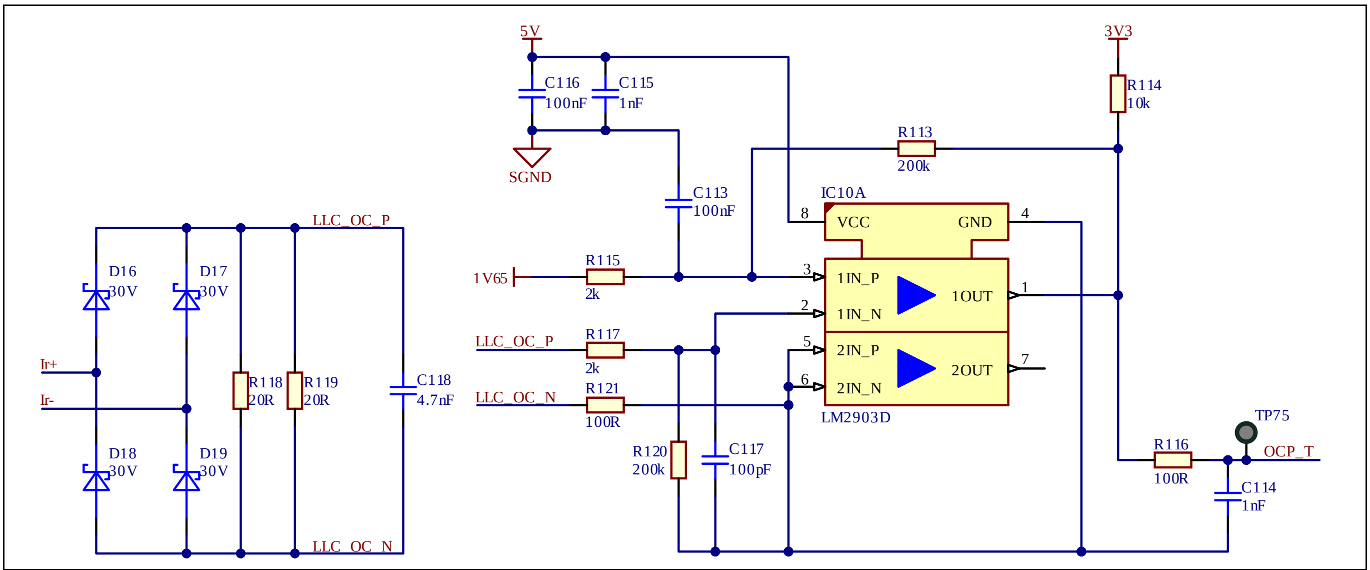


Figure 21 AC current sensing

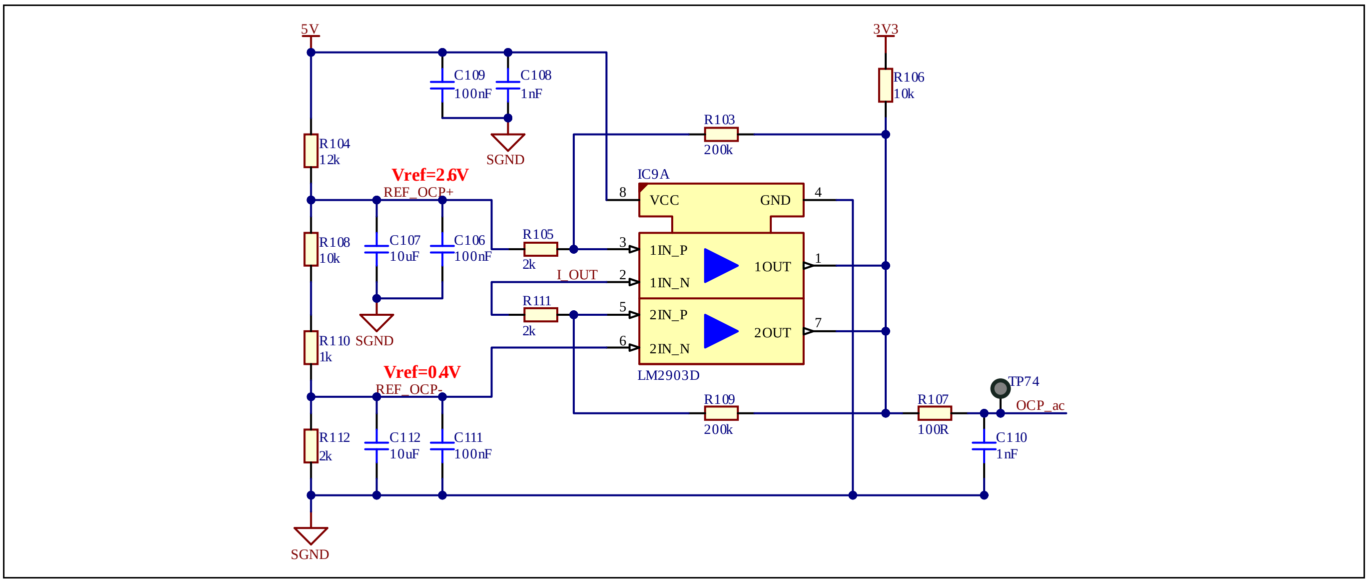


Figure 22 Overcurrent detection

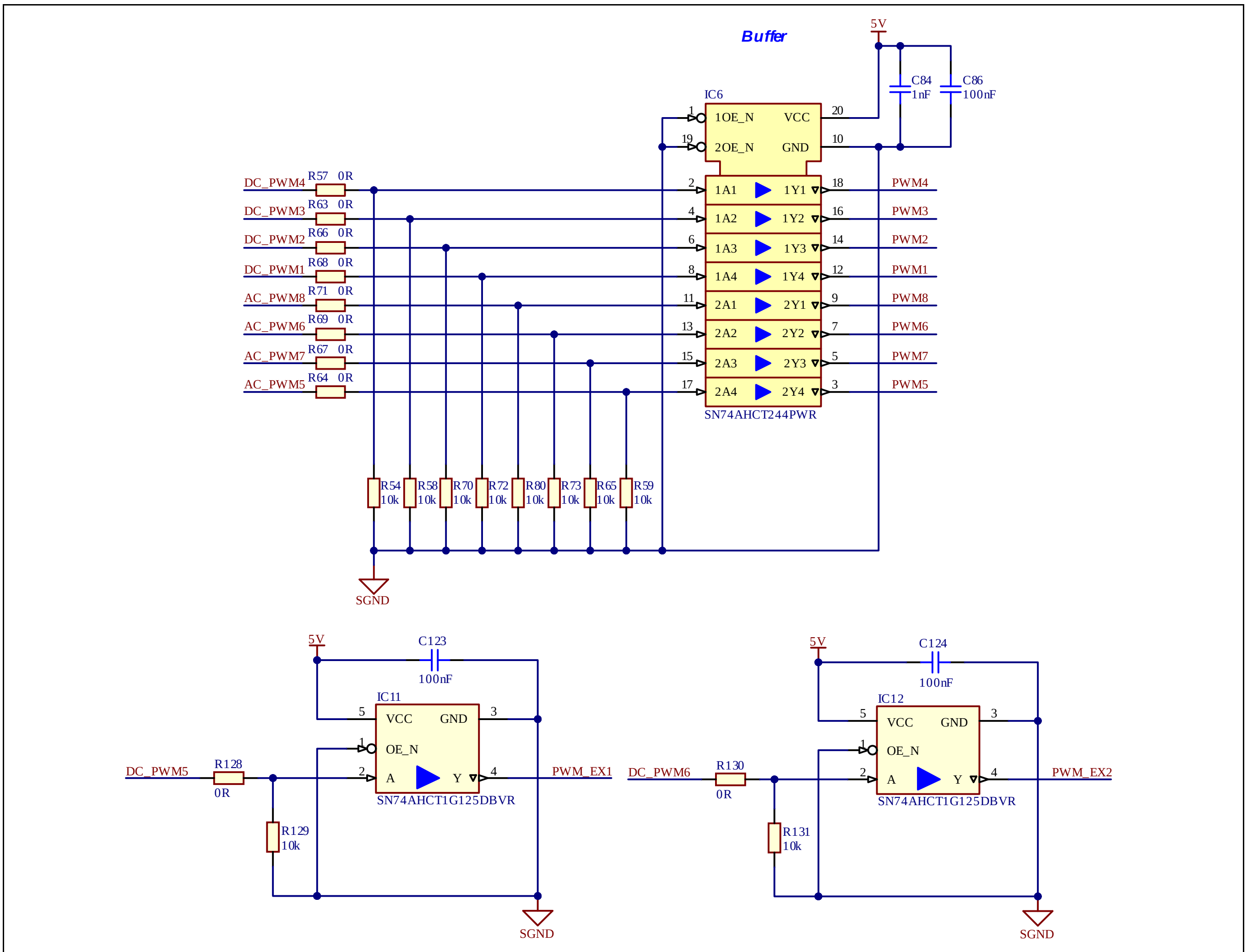


Figure 23 PWM buffer

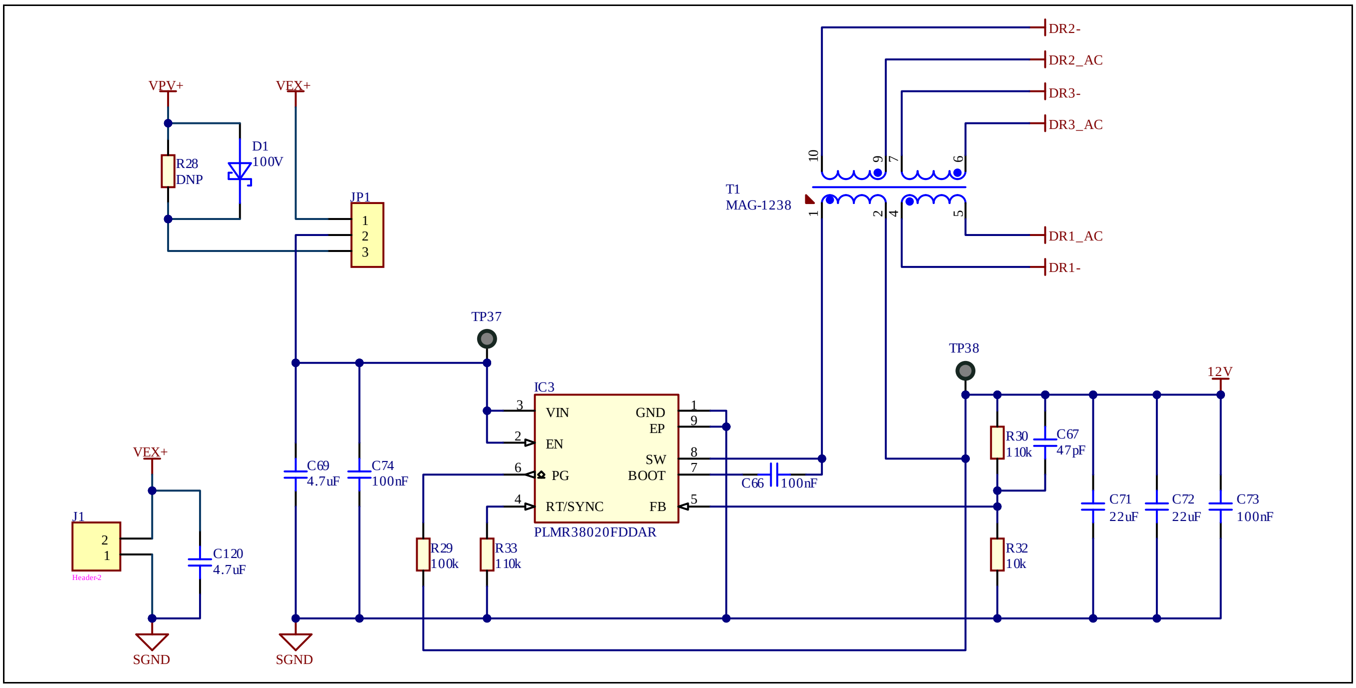


Figure 24 Auxiliary power supply primary side

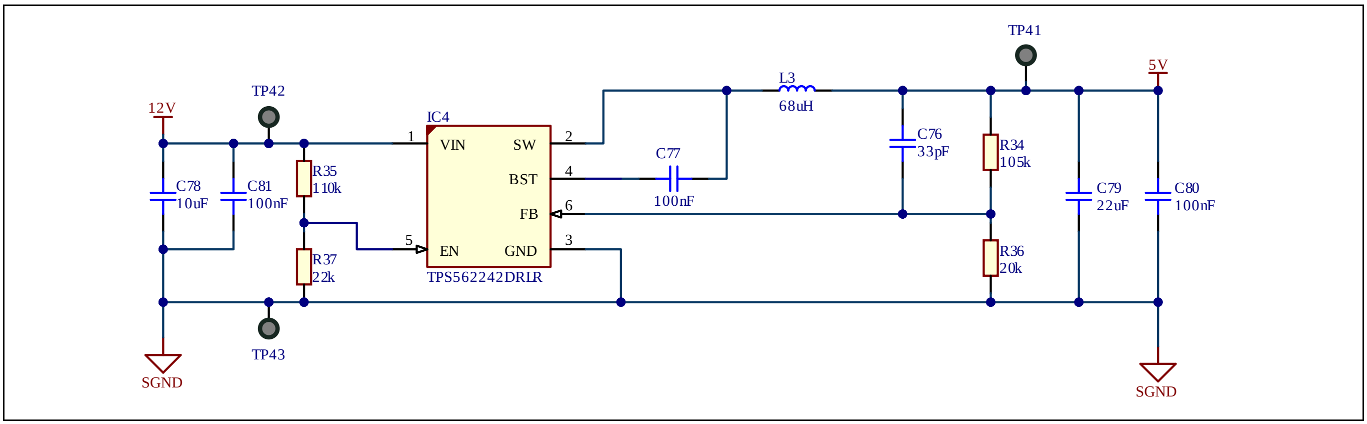


Figure 25 12 V to 5 V buck converter

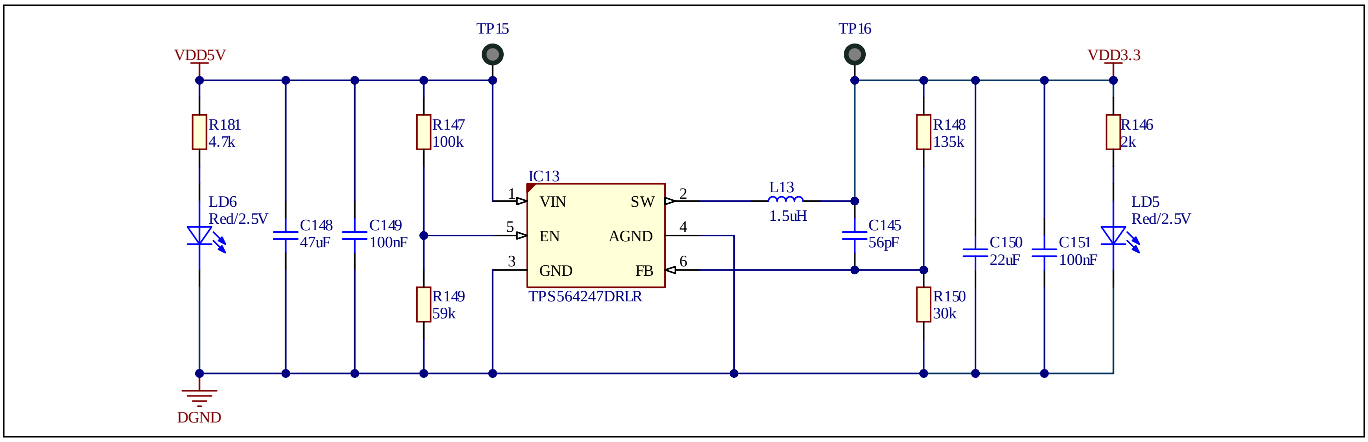


Figure 26 5 V to 3.3 V buck converter

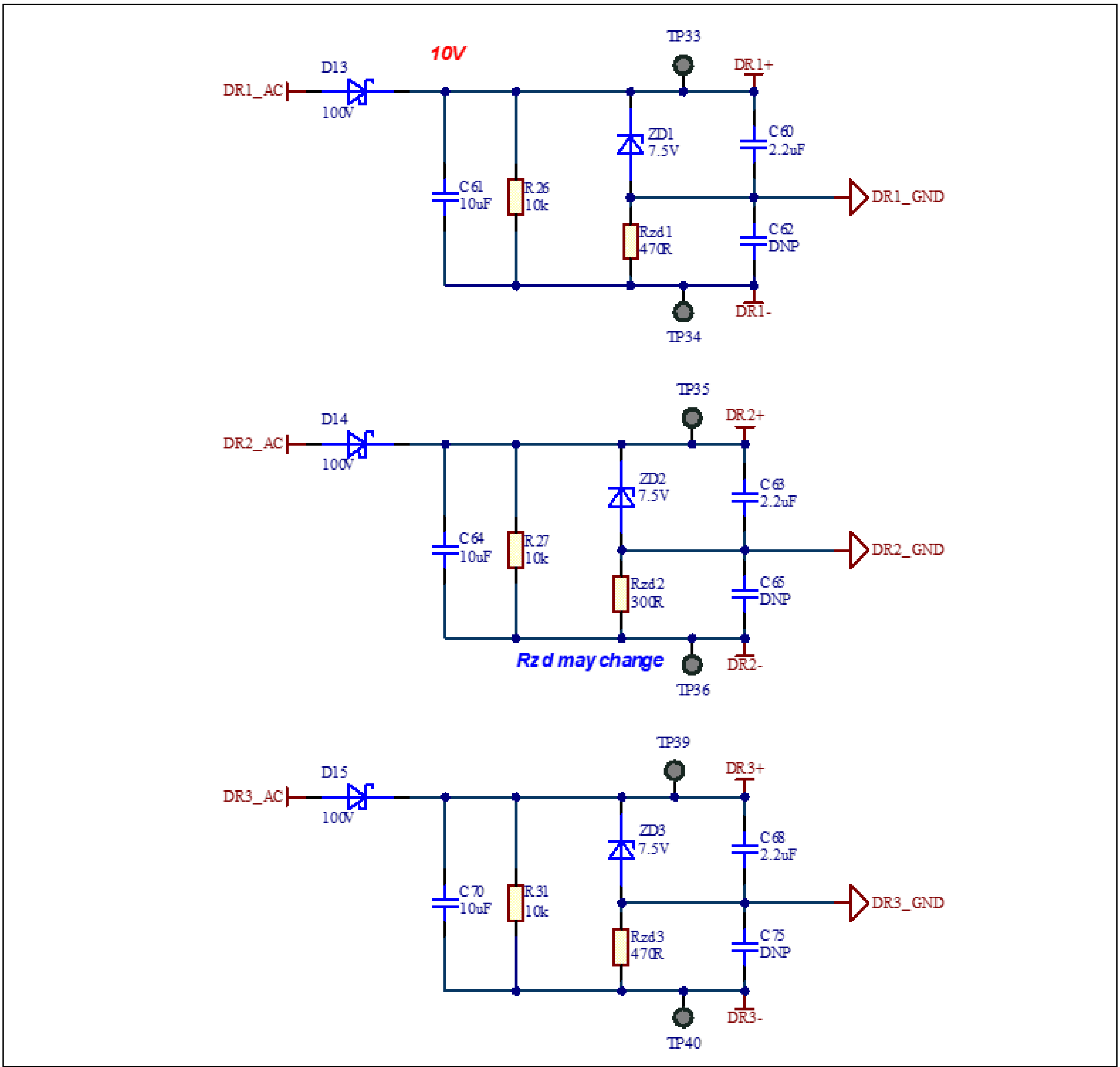


Figure 27 **Isolated power supplies**

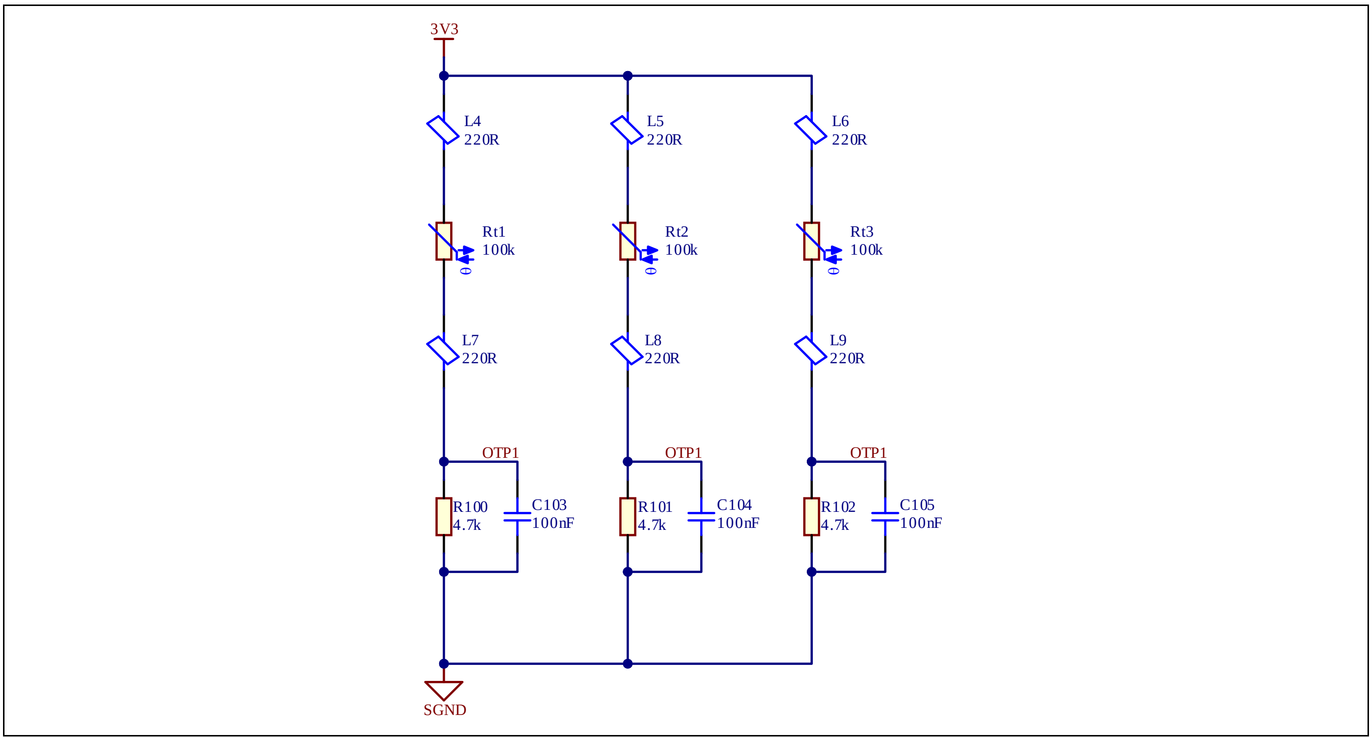


Figure 28 Temperature sensing

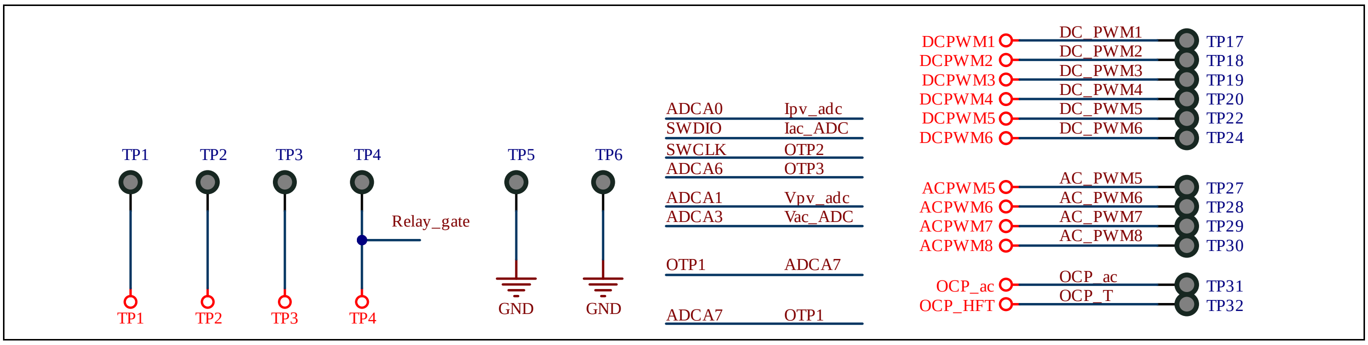


Figure 29 Test points

5 Hardware functional description

The REF_500W_CYCLO family of microinverter reference design boards is based on Infineon's proprietary cycloinverter topology, which is different from existing topologies and does not infringe any associated patents.

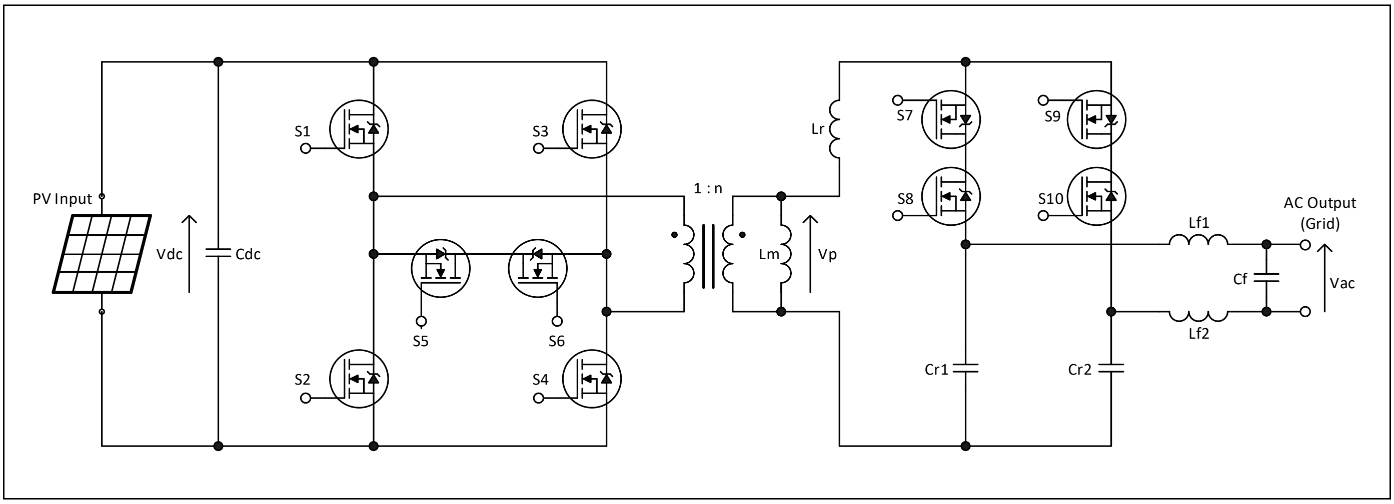


Figure 30 Infineon cycloinverter topology

This two-stage topology primary DC to AC full-bridge consists of S1, S2, S3, and S4 with an additional bidirectional switch formed by S5 and S6 that drives a step-up transformer. L_m represents the transformer magnetizing inductance and L_k represents the leakage inductance. The AC to AC cycloconverter secondary stage consists of a half-bridge formed with bidirectional switches S7-8 and S9-10, which are implemented using common drain bidirectional GaN devices integrated into a single package on the REF_500W_CYCLO_BDSGAN reference design. The transformer secondary is referenced to the mid-point of the two series capacitors Cr1 and Cr2. The output is connected to the AC grid via a filter represented by Lf1, Lf2 and Cf in the above figure. A more complex filter design is used in the REF_500W_CYCLO_BDSGAN design.

The system can be modeled by the following equivalent circuit:

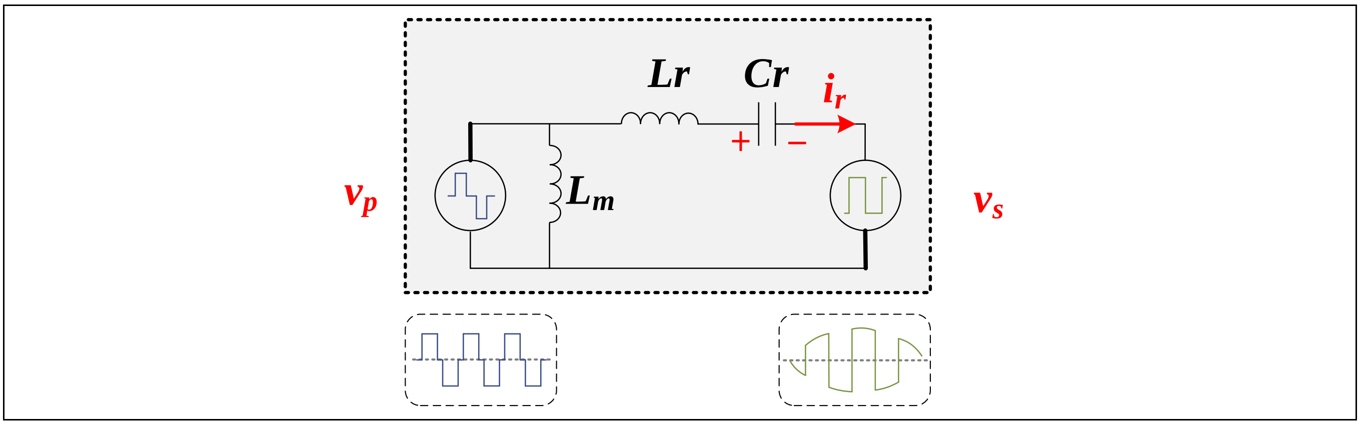


Figure 31 Cycloinverter circuit model

The secondary winding of the transformer is represented by a modulated AC source with resonant elements L_r and C_r, where L_r is equal to L_k and C_r is equal to Cr1 + Cr2, which are of equal value.

The voltage at the transformer secondary (V_p) is determined by the modulation of the primary stage and transformer turns ratio *n*. V_{dc} refers to the input voltage from the connected photovoltaic (PV) panels with DC bus capacitors C_{dc} required to absorb the low frequency ripple at twice the output grid frequency.

The secondary side of the cycloinverter can be described as a bi-polar voltage-doubler rectifier. Resonant current is transferred from the primary to the secondary with the transformer providing isolation and voltage step up. The positive portion of the current passes through one bidirectional HV switch to charge the corresponding capacitor and the negative portion passes through the other bidirectional switch to charge the other capacitor. The sum of the voltage across both of these capacitors passes to the AC grid through the filter network. The polarities alternate during the positive and negative half cycles of the AC grid.

5.1 Control scheme

The DC side consisting of S1 to S6 can provide three different voltage levels at the transformer primary v_p' +Vdc, 0 or -Vdc according to the switch states shown in the following figures:

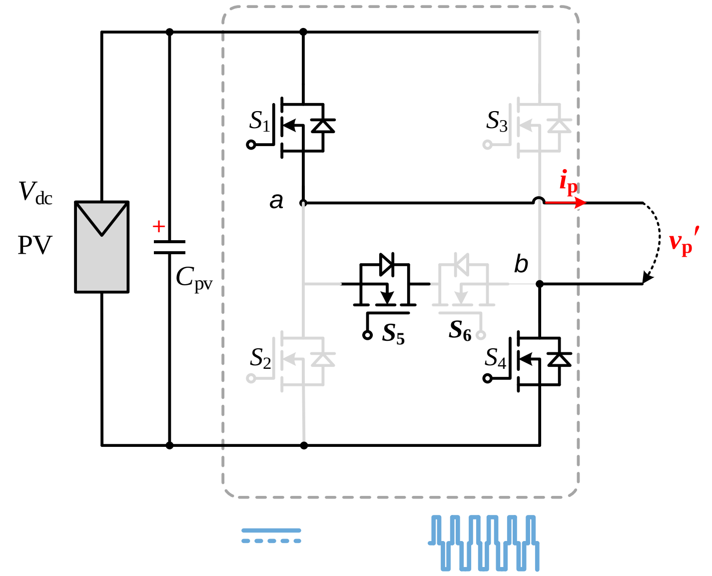


Figure 32 Vp' equal to +Vdc

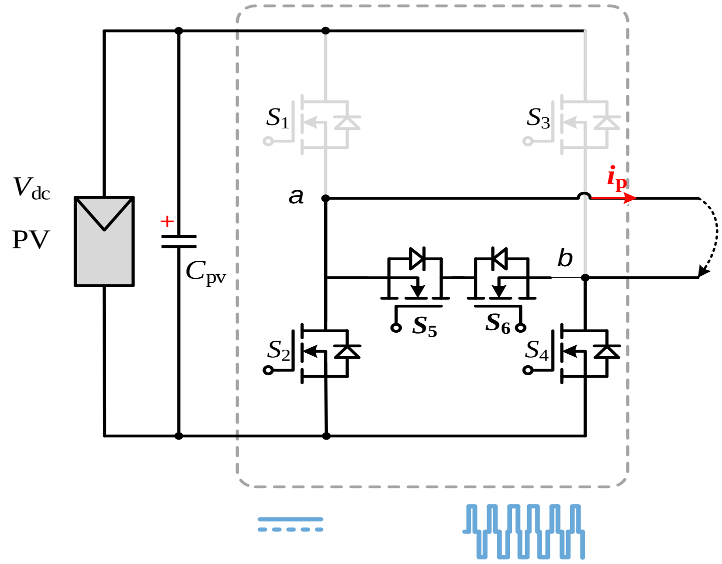


Figure 33 Vp' equal to zero

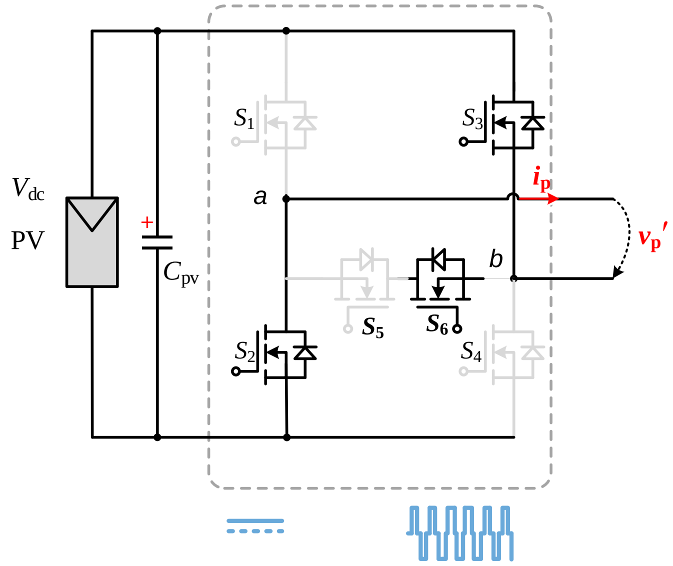


Figure 34 Vp' equal to -Vdc

The voltage V_P indicated in Figure 30 represents V_P' stepped up through the transformer with turns ratio n, therefore it can be equal to; $+nV_{dc}$, 0 or $-nV_{dc}$. The voltage V_s represents the secondary side resonant tank, which may be equal to $+|V_g|/2$ or $-|V_g|/2$ where V_g is the instantaneous voltage at the AC grid connection.

The control scheme used in the REF_500W_CYCLO_BDSGAN design includes three adjustable parameters, which are as follows:

- **f_S:** the switching frequency, for adjusting the impedance point in the resonant tank
- **D_1:** the inner phase shift ratio
- **D_δ:** the outer phase shift ratio

The value of D_2 is calculated with the formula:

$$D_2 = D_\delta + \frac{D_1}{2}$$

Equation 2

These signals are illustrated as follows:

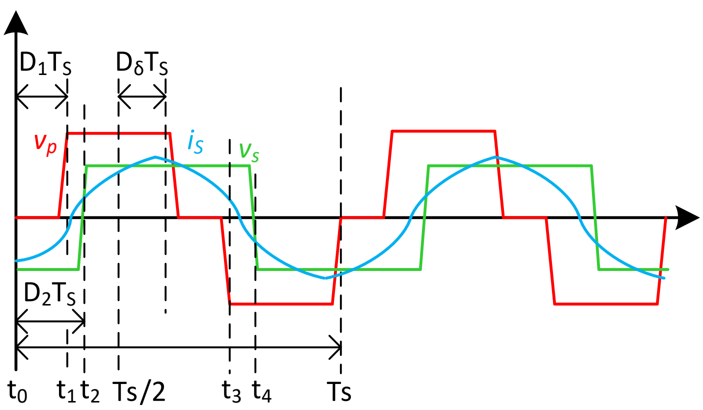


Figure 35 Operating waveforms

The time intervals t_1, t_2, and t_3 are calculated as:

$$\begin{cases} t_1 = D_1 T_s + \frac{(0.5 - D_1)}{2} T_s = \frac{D_1}{2} T_s + \frac{0.5}{2} T_s \\ t_2 = D_2 T_s + \frac{0.5}{2} T_s & \Rightarrow D_2 = D_\delta + \frac{D_1}{2} \\ t_2 = t_1 + D_\delta T_s \end{cases}$$

Equation 3

5.1.1 Switching states

The following six switching states are used in the PWM scheme of the cycloinverter during the positive AC grid half-cycle. The switching of S7+S8 and S9+S10 is swapped with S7+S8 on during the negative half-cycle:

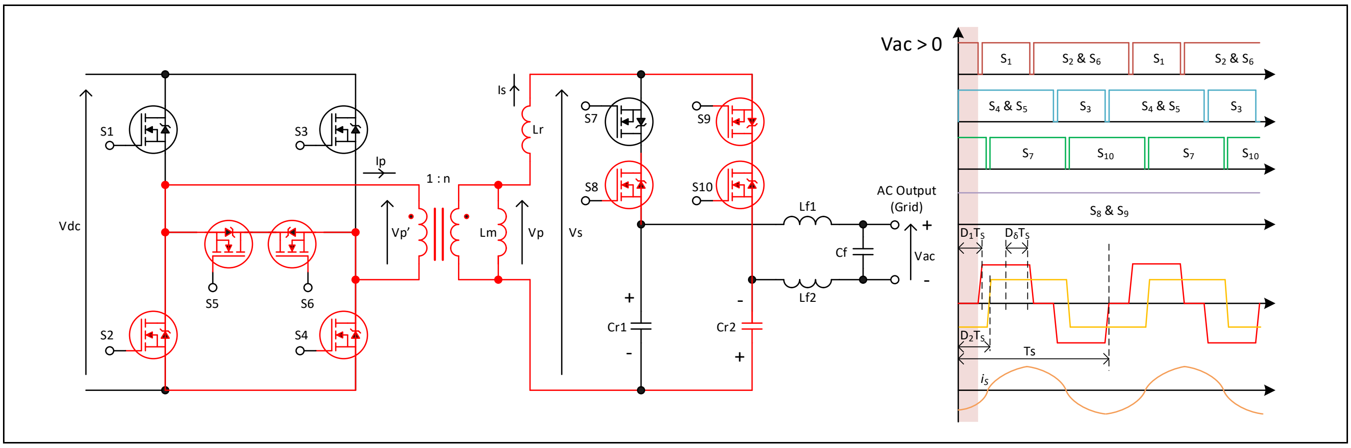


Figure 36 State 1

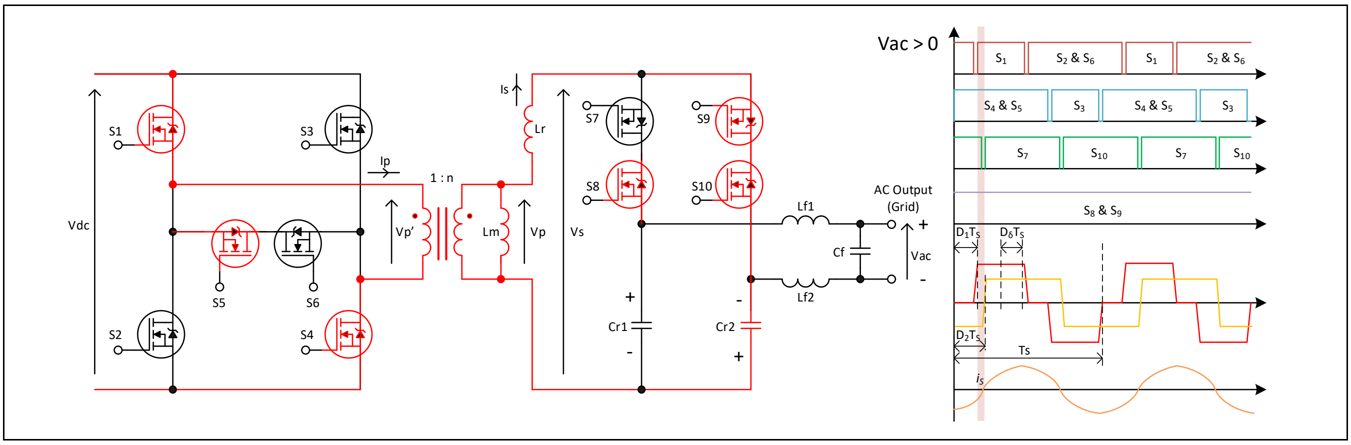


Figure 37 State 2

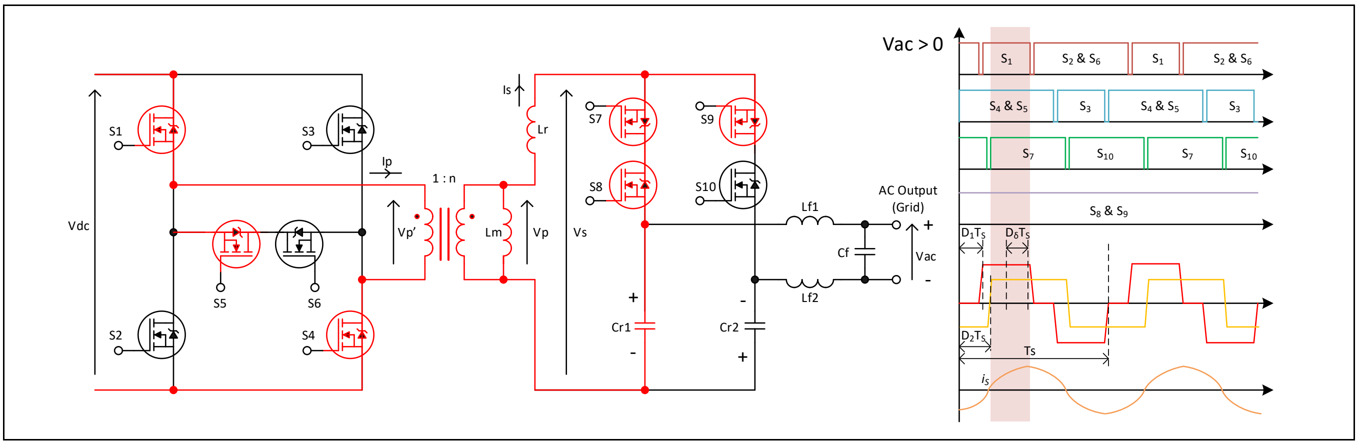


Figure 38 State 3

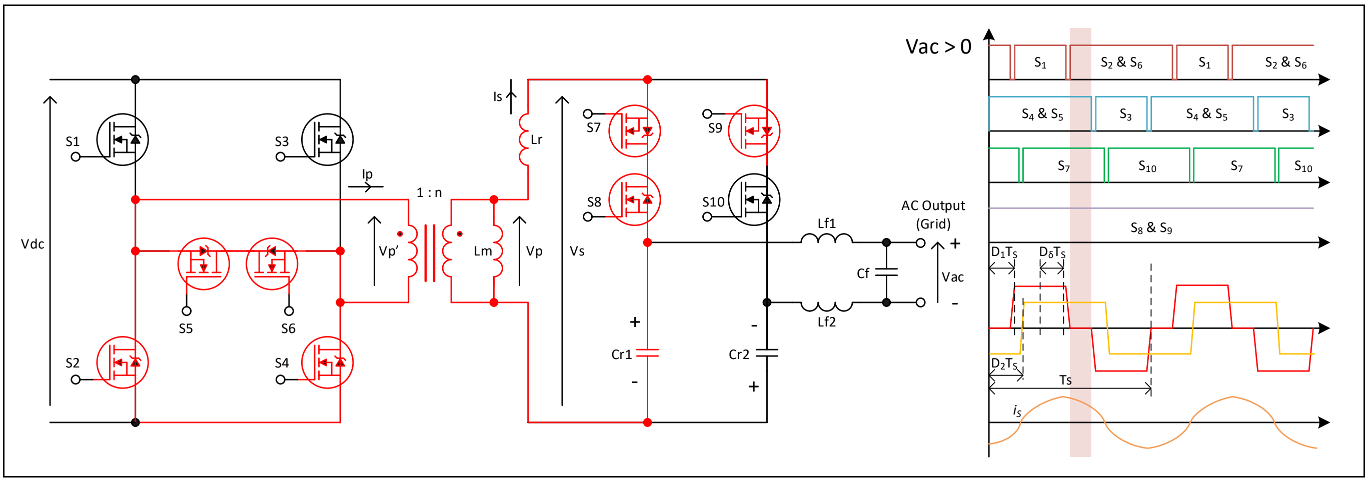


Figure 39 State 4

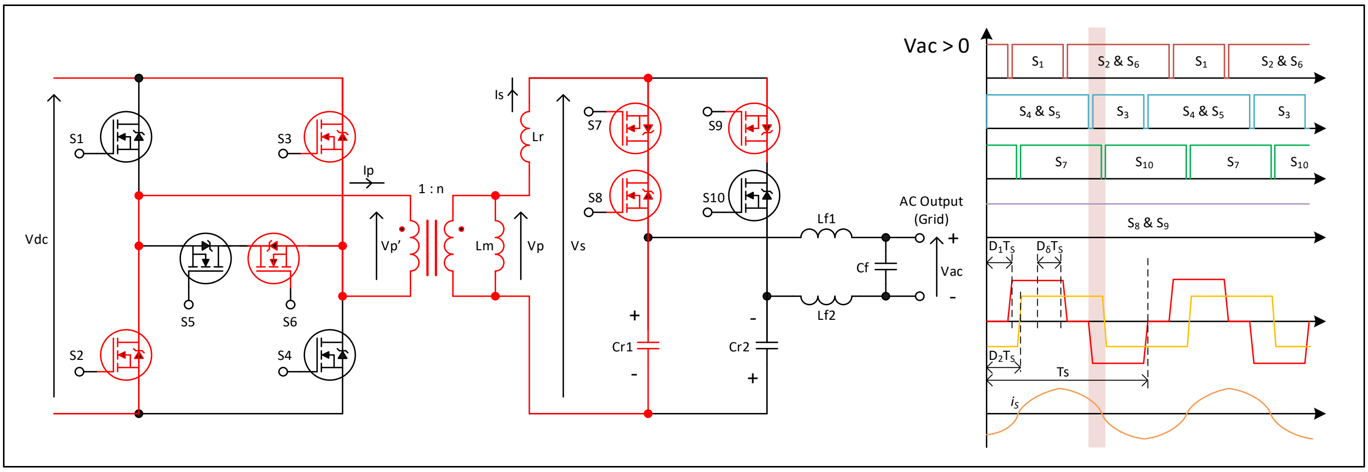


Figure 40 State 5

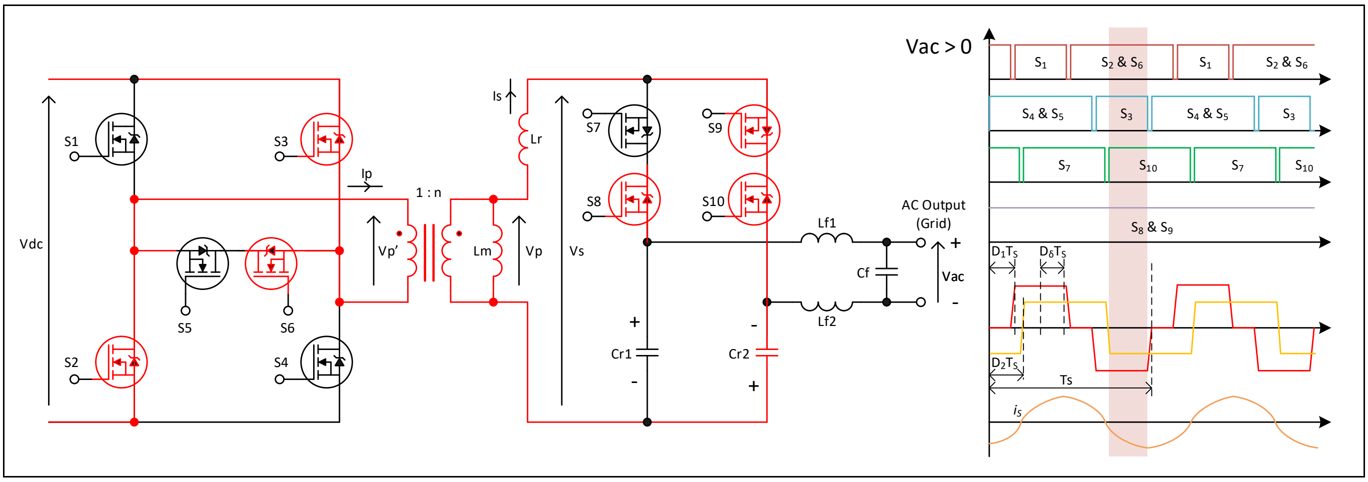


Figure 41 State 6

The states are summarized in the following table:

Table 7 Switching state summary Vac positive half-cycle (gate drives ON/OFF)

State	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	Vp	Vs	Vx
1	OFF	ON	OFF	ON	ON	ON	OFF	ON	ON	ON	0	-VCr2	-|Vac|/2
2	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	ON	Vdc	-VCr2	-|Vac|/2
3	ON	OFF	OFF	ON	ON	OFF	ON	ON	ON	OFF	Vdc	+VCr1	+|Vac|/2
4	OFF	ON	OFF	ON	ON	ON	ON	ON	ON	OFF	0	+VCr1	+|Vac|/2
5	OFF	ON	ON	OFF	OFF	ON	ON	ON	ON	OFF	-Vdc	+VCr1	+|Vac|/2
6	OFF	ON	ON	OFF	OFF	ON	OFF	ON	ON	ON	-Vdc	-VCr2	-|Vac|/2

Note: In the PWM scheme used here, S2 and S6 are always on and off at the same time as are S4 and S5.

S8 and S9 are on continuously during the AC grid positive half cycle while S7 and S10 are switching complementary to each other. During the negative grid half-cycle S7 and S10 are on continuously while S8 and S9 are switching.

The AC output voltage before the output filter is equal to the sum of the two capacitor voltages Vcr1 and Vcr2.

The operating conditions during different switching states are outlined in the following figures, which describe the energy transfer to the resonant capacitors C1 and C2, which supply the output to the grid. In a non-active state when all of the switches are off, the output voltage is equal to the sum of the voltages across C1 and C2 as follows:

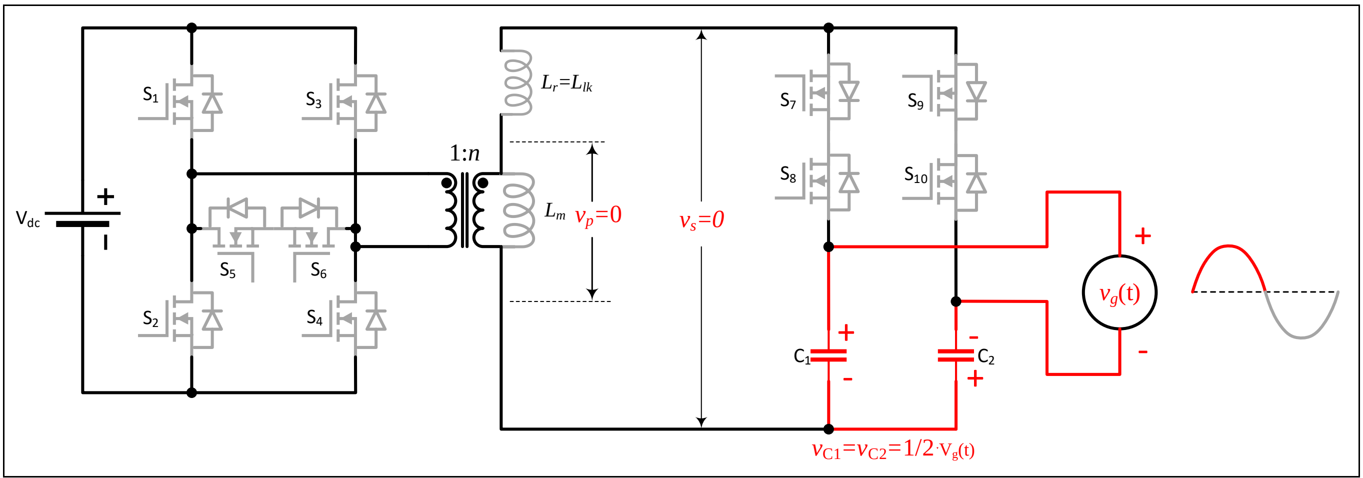


Figure 42 All switches OFF

The following diagrams describe the energy transfer taking place in the previously described switching states. The equations shown in each diagram describe the relationships between the voltages and currents in the capacitive and inductive elements.

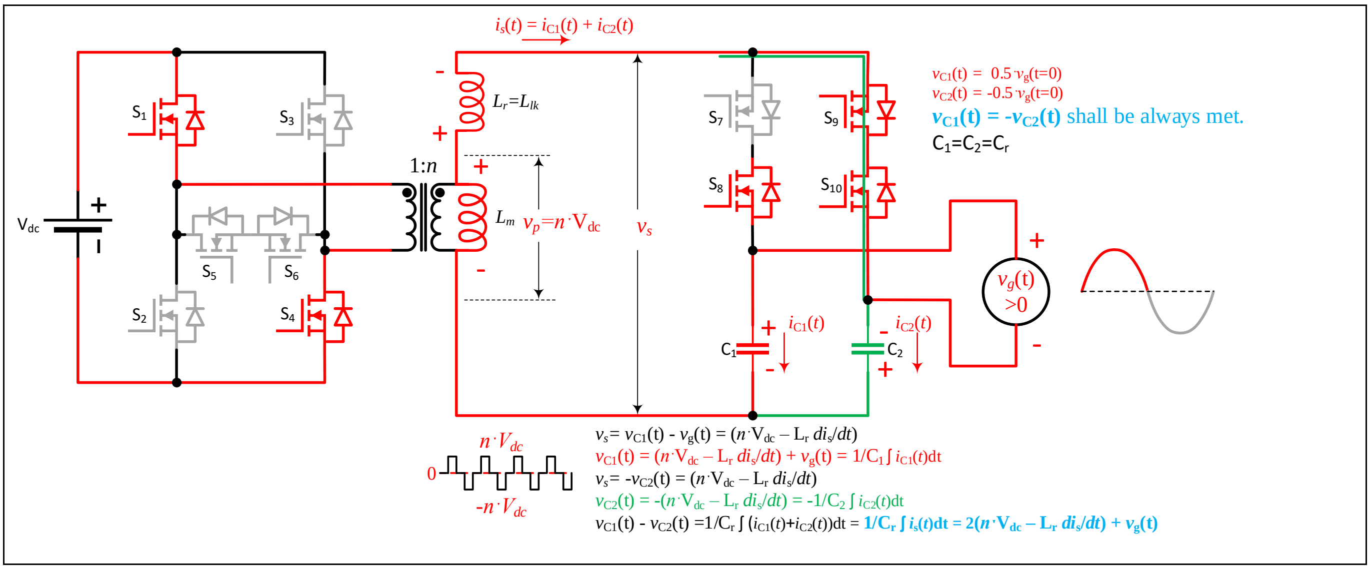


Figure 43 State 2

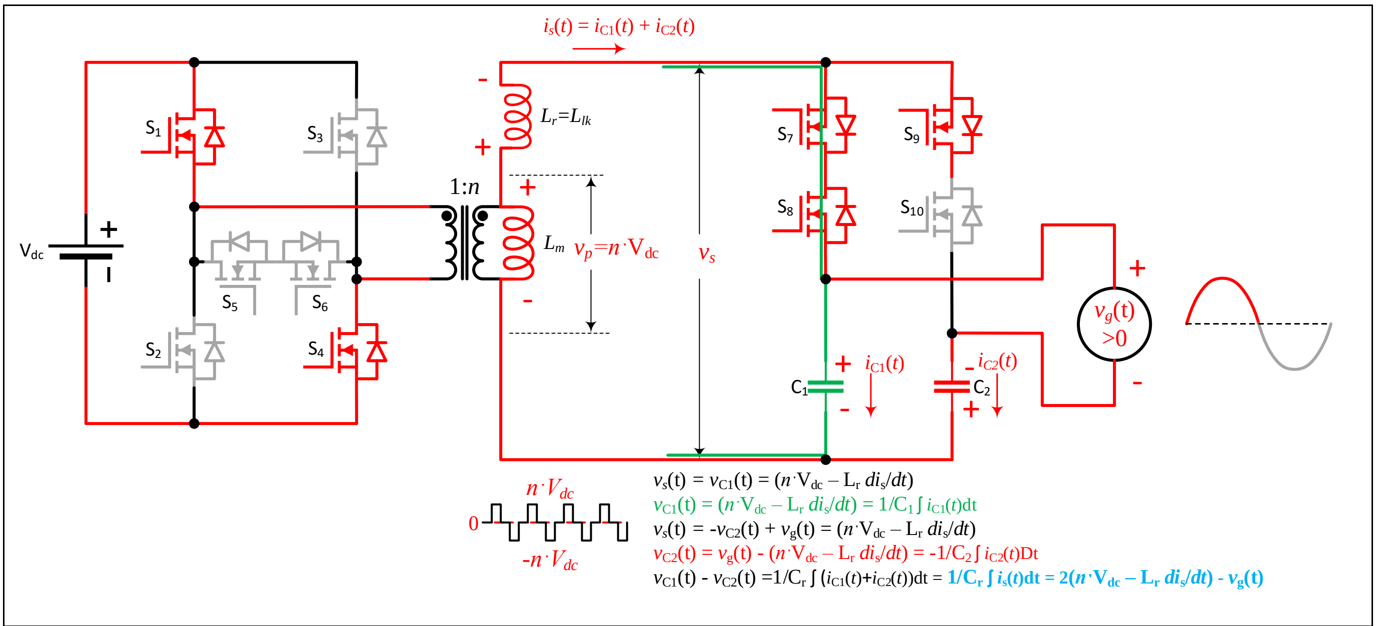


Figure 44 State 3

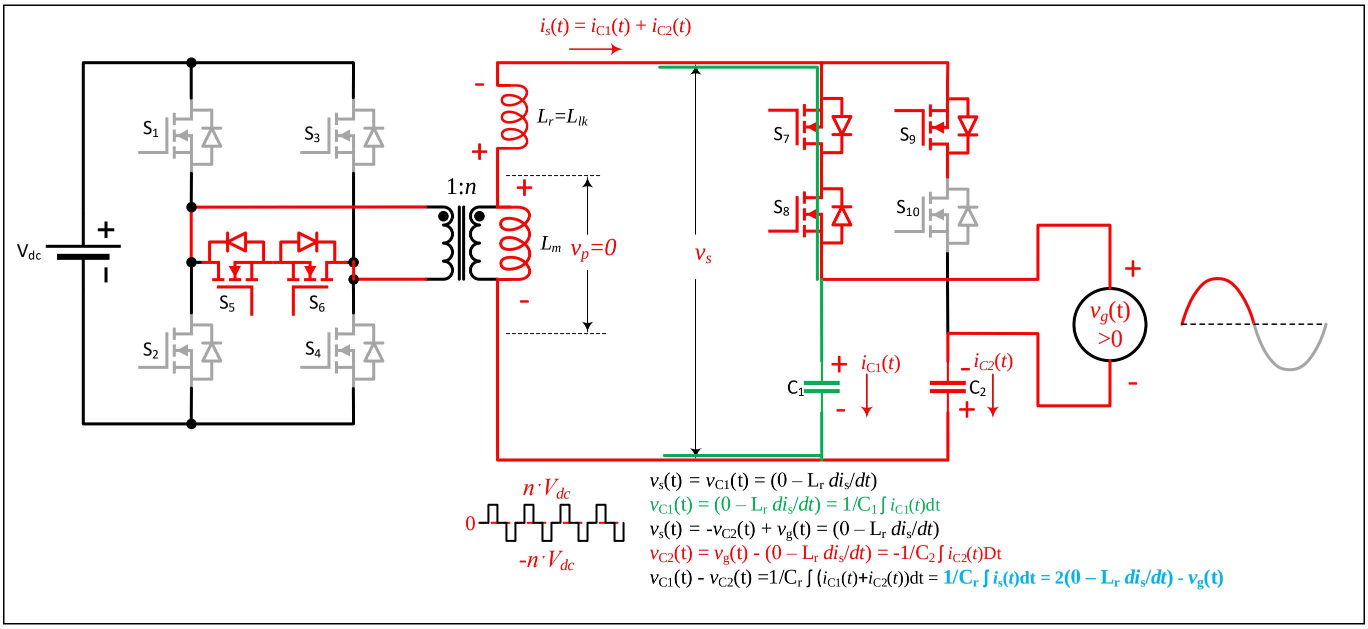


Figure 45 State 4

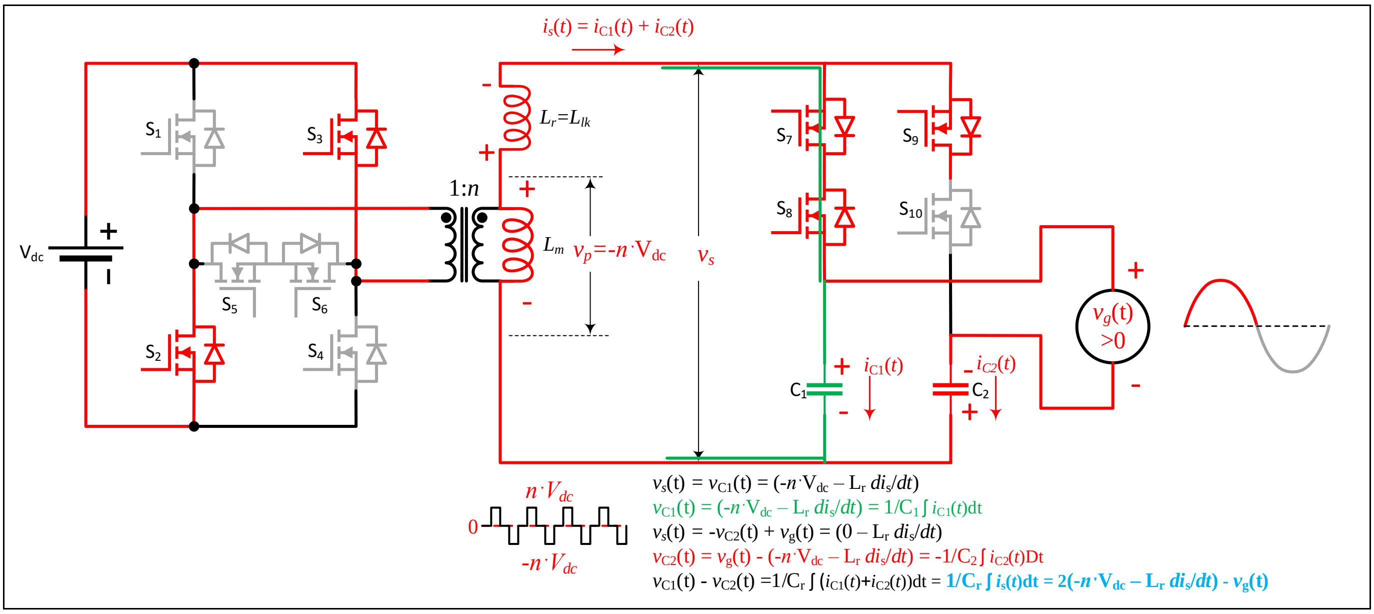


Figure 46 State 5

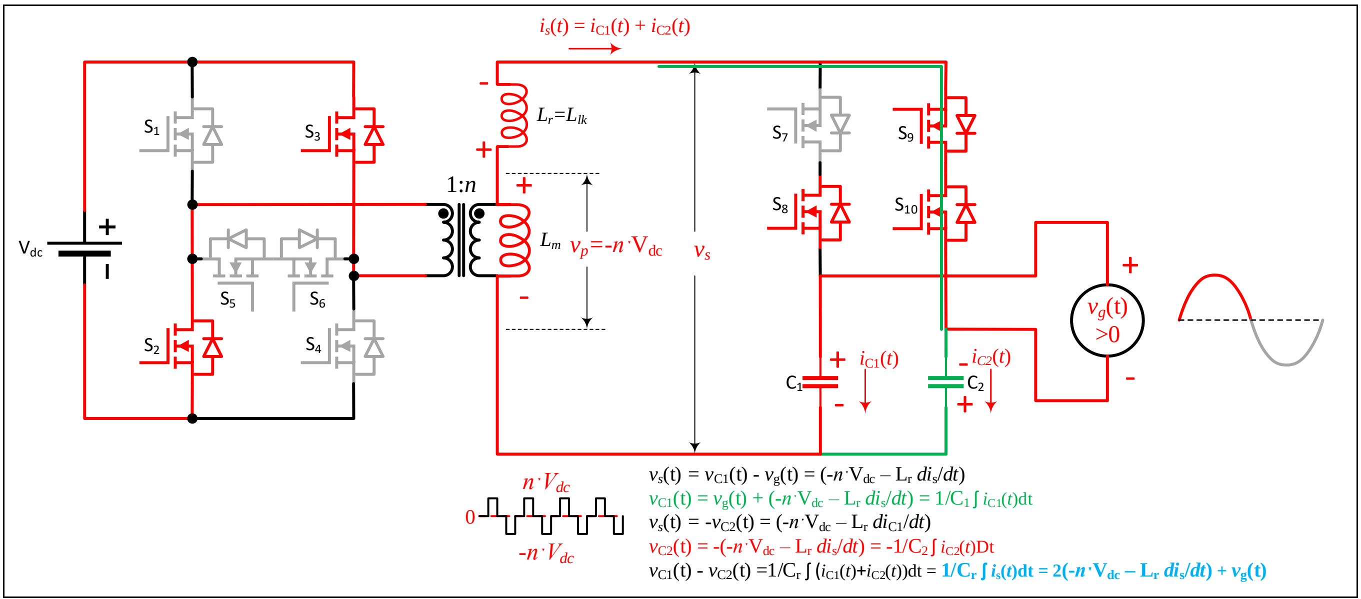


Figure 47 State 6

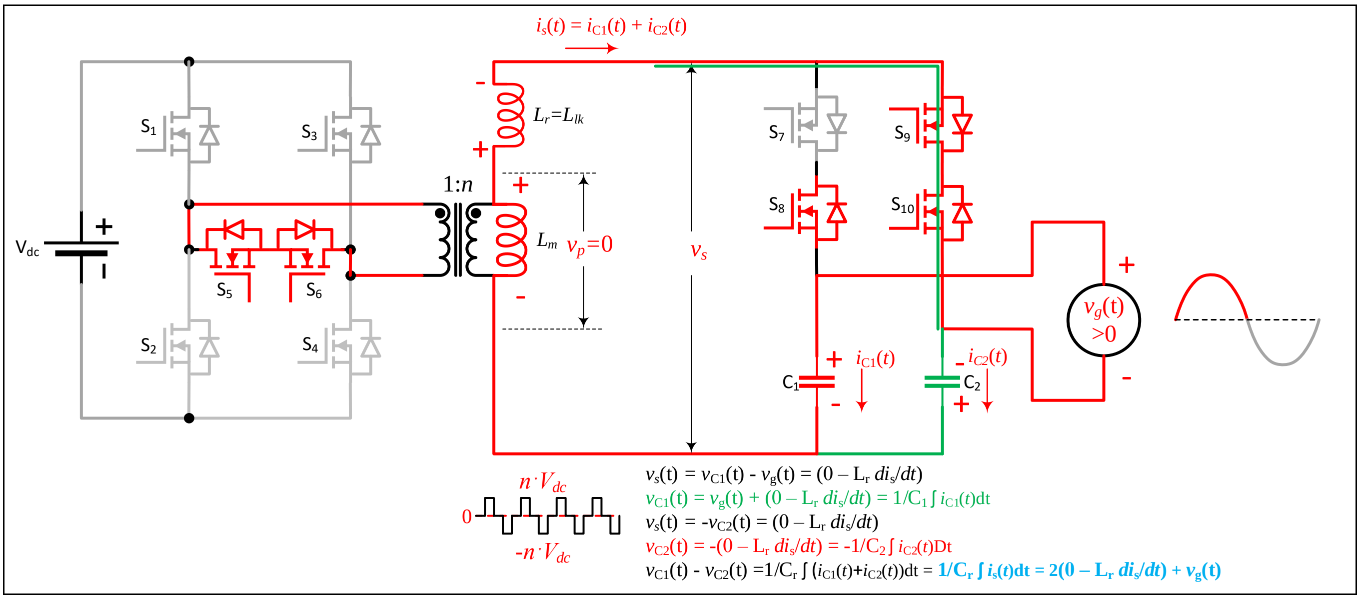


Figure 48 State 7

5.1.2 Soft switching (ZVS)

Zero Voltage Switching[1] (ZVS) is achieved to enable high efficiency in this converter. During state 1 the resonant current i_S is below zero and the V_{DS} of S1 is equal to V_{dc}. Commutation occurs during the dead-time between states 1 and 2 when the V_{DS} of S1 is discharged by the primary circulating current i_P until body diode conduction occurs, which enables ZVS of S1 to be achieved. In state 2 the resonant current transitions from negative to positive. When S10 switches off i_S charges the drain-source capacitance (C_{OSS}) of S10 also discharging the C_{OSS} of S7 causing the V_{DS} of S10 to rise and that of S7 to fall to enable ZVS switching once the body diode is conducting. In state 3, i_S charges the C_{OSS} of S1 and discharges the C_{OSS} of S2 and S6 until the body diodes of these two devices conduct and ZVS can be realized. ZVS switching is achieved for all switches in the different switching states provided there is sufficient load to produce enough resonant current. This is not the case at light load, which is why a burst mode function has been implemented to maintain high efficiency.

The ZVS constraint can be further explained by means of a phasor diagram:

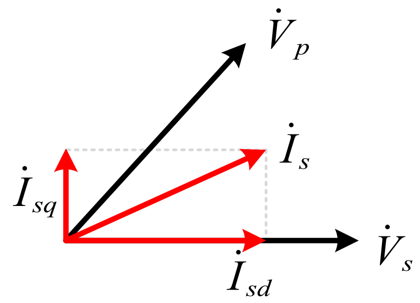


Figure 49 Phasor diagram of the resonant voltage and current fundamental components

The diagram shows the fundamental components of the primary voltage V_P' and secondary voltage V_S, which is the phase reference located on the real axis. The magnitude and phase angle of V_P' change with the change in inner and outer phase angles D_1 and D_δ. The resonant current I_S contains real and reactive components, which have been separated onto the real and imaginary axes. To achieve ZVS operation, a sufficiently large component of lagging reactive current I_{sq} is necessary, however this also increases the overall amplitude of I_S.

When I_S lags behind the V_P' by an angle of $\varphi_1/2$, the primary side lagging switches can achieve ZVS. When I_S leads V_S, the secondary side switches can realize soft switching. Therefore, when the current phase angle is in the middle of the original and secondary side voltage vectors, the soft switching of all switches can be realized, that is:

$$0 \le \angle \dot{I}_s \le \varphi_\delta - \frac{\varphi_1}{2}$$

Equation 4

Where, $\varphi_1 = 2\pi D_1$ and $\varphi_\delta = 2\pi D_\delta$

[1] Also referred to as h switching.

5.1.3 Frequency domain analysis

The resonant tank voltages according to Figure 30 can be expressed by Fourier transform for the harmonic components *k* are as:

$$v_p(t)=\sum_{k=1,3\cdots}^{N}\frac{4V_p}{k\pi}\cos\left(k\frac{\varphi_1}{2}\right)\sin\left(k\omega_s t+k\varphi_\delta\right)$$
$$v_s(t)=\sum_{k=1,3\cdots}^{N}\frac{2\left|v_g\right|}{k\pi}\sin\left(k\omega_s t\right)=\sum_{k=1,3\cdots}^{N}\frac{4mV_p}{k\pi}\sin\left(k\omega_s t\right)$$
$$m=\frac{\left|v_g\right|/2}{V_p},\varphi_1=2\pi D_1,\varphi_\delta=2\pi D_\delta,\omega_s=2\pi f_s$$

Equation 5

Where $\omega_S = 2\pi f_S$ is the switching frequency, v_g is the instantaneous grid voltage, and $V_p = nV_{dc}$, 4 therefore:

$$m=\frac{|v_g|}{2nV_{dc}}$$

Equation 6

For the period of the AC grid half cycle where m > 1, the converter is said to be working in *boost* mode and when m ≤ 1, it is said to be working in *buck* mode. The transformer turns ratio *n* therefore determines how much of each line half cycle is spent operating in each mode, which strongly influences the overall converter efficiency.

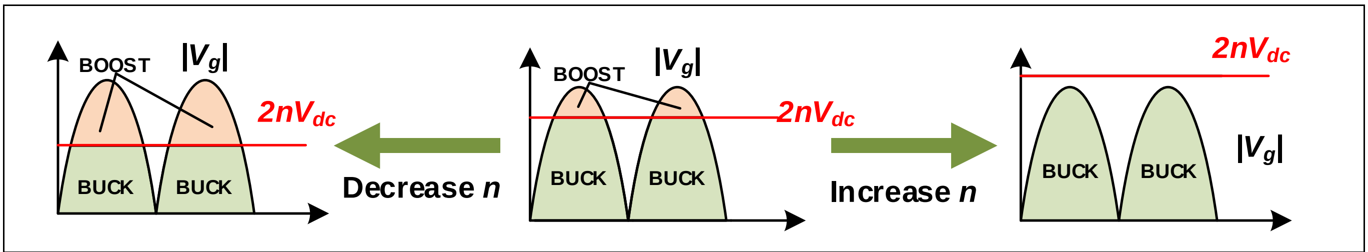


Figure 50 Buck and boost mode periods of operation according to transformer turns ratio

The resonant current is expressed as:

$$i_r(t)=\sum_{k=1,3\cdots}^{N}\frac{4V_p}{k\pi Z_r}\frac{\sqrt{A^2+B^2}}{\left(\frac{k\omega_s}{\omega_r}-\frac{\omega_r}{k\omega_s}\right)}\sin\left[k\omega_s t+\theta_V-\frac{\pi}{2}\right]$$

Equation 7

Where

$$Z_r = \sqrt{\frac{L_r}{C_r}}$$

Equation 8

$$A = \cos\left(\frac{\varphi_1}{2}\right)\sin(\varphi_\delta) \text{ and } B = \cos\left(\frac{\varphi_1}{2}\right)\cos(\varphi_\delta) - m$$

Equation 9

$$\theta_V = \text{arctan2}\left(\frac{A}{B}\right)$$

Equation 10

5.1.3.1 Transmission power and RMS resonant current

The power transmitted by the converter in one switching cycle can be calculated as:

$$P_{trans} = \frac{1}{T_s}\int_0^{T_s} v_s(t)\, i_r(t)\, dt = \sum_{k=1,3\cdots}^{N} \frac{8mV_p^2}{k^2\pi^2 Z_r} \frac{\sqrt{A^2+B^2}}{(\frac{k\omega_s}{\omega_r}-\frac{\omega_r}{k\omega_s})} \sin(\theta_V)$$
$$= \sum_{k=1,3\cdots}^{N} \frac{8mV_p^2}{k^2\pi^2 Z_r\left(\frac{k\omega_s}{\omega_r}-\frac{\omega_r}{k\omega_s}\right)} \cos\left(\frac{\varphi_1}{2}\right)\sin(\varphi_\delta)$$

Equation 11

Where $\omega_r = 2\pi f_r$ is the resonant frequency.

Considering the fundamental component only, the power transmitted by the transformer during one switching cycle is simplified to:

$$P_{trans}^1 = \frac{8mV_p^2}{\pi^2 Z_r\left(\frac{\omega_s}{\omega_r}-\frac{\omega_r}{\omega_s}\right)} \cos\left(\frac{\varphi_1}{2}\right) \sin(\varphi_\delta) = \frac{4nV_{dc}|v_g|}{\pi^2 Z_r\left(\frac{\omega_s}{\omega_r}-\frac{\omega_r}{\omega_s}\right)} \cos\left(\frac{\varphi_1}{2}\right) \sin(\varphi_\delta)$$

Equation 12

According to the expression for resonant current, the effective value of resonant current can be calculated as:

$$i_{r,rms} = \sqrt{\frac{1}{T_s}\int_0^{T_s}[i_r(t)]^2 dt} = \sqrt{\sum_{k=1,3\cdots}^{N}\left[\frac{2\sqrt{2}V_p}{k\pi Z_r}\frac{\sqrt{A^2+B^2}}{(\frac{k\omega_s}{\omega_r}-\frac{\omega_r}{k\omega_s})}\right]^2}$$

Equation 13

For the fundamental component, the effective value of the transformer secondary current is simplified to:

$${i_{r,rms}}^1 = \frac{2\sqrt{2}V_p}{\pi Z_r\left(\frac{\omega_s}{\omega_r}-\frac{\omega_r}{\omega_s}\right)} \sqrt{\left[\cos\left(\frac{\varphi_1}{2}\right)\sin(\varphi_\delta)\right]^2 + \left[\cos\left(\frac{\varphi_1}{2}\right)\cos(\varphi_\delta) - m\right]^2}$$

Equation 14

5.1.4 Modulation optimization

In the REF_500W_CYCLO_BDSGAN cyclo-microinverter, the resonant current magnitude is one of the key factors affecting the overall converter efficiency. An increase in the resonant current increases the conduction losses of the switching devices and the copper losses of the magnetic components leading to an efficiency reduction. Optimization of the resonant current is therefore an essential part of the control strategy.

5.1.4.1 Fixed-switching frequency analysis

Considering fixed-frequency operation, the P_{trans} and $i_{s,rms}$ calculations can be simplified to:

$$P_{trans} = \frac{4nV_{dc}\left|v_g\right|}{\pi^2 Z_r\left(\frac{f_s}{f_r}-\frac{f_r}{f_s}\right)}\cos\left(\frac{\varphi_1}{2}\right)\sin\left(\varphi_\delta\right)$$

$$i_{r,rms}{}^1 = \frac{2\sqrt{2}nV_{dc}}{\pi Z_r\left(\frac{f_s}{f_r}-\frac{f_r}{f_s}\right)}\sqrt{A^2+B^2}$$

$$= \frac{2\sqrt{2}nV_{dc}}{\pi Z_r\left(\frac{f_s}{f_r}-\frac{f_r}{f_s}\right)}\sqrt{\left[\cos\left(\frac{\varphi_1}{2}\right)\sin\left(\varphi_\delta\right)\right]^2+\left[\cos\left(\frac{\varphi_1}{2}\right)\cos\left(\varphi_\delta\right)-m\right]^2}$$

Equation 15

The transmission power reference is defined as:

$$P_N\left(V_{dc}, v_g, f_s\right) = \frac{4nV_{dc}\left|v_g\right|}{\pi^2 Z_r\left(\frac{f_s}{f_r}-\frac{f_r}{f_s}\right)}$$

Equation 16

When the inner phase shift angle is determined, the outer phase shift angle can be calculated from the above equation:

$$\varphi_\delta = arcsin\left[\frac{P_{trans}}{P_N\left(V_{dc},v_g,f_s\right)}\cdot\frac{1}{cos(\varphi_1/2)}\right] = arcsin\left[\frac{M_f\left(V_{dc},v_g,P_g,f_s\right)}{cos(\varphi_1/2)}\right]$$

Equation 17

$$M_f\left(V_{dc}, v_g, P_g, f_s\right) = \frac{P_{trans}}{P_N\left(V_{dc},v_g,f_s\right)}$$

Equation 18

The intermediate variable x = cos(ϕ1/2), therefore the following optimization problem can be solved:

$$\begin{aligned}\min\left(A^2+B^2\right) &= \min\left\{\left[\cos\left(\frac{\varphi_1}{2}\right)\sin\left(\varphi_\delta\right)\right]^2+\left[\cos\left(\frac{\varphi_1}{2}\right)\cos\left(\varphi_\delta\right)-m\right]^2\right\}\\ &= \min\left\{{M_f}^2+\left[x\cos\left(\arcsin\left[\frac{M_f}{x}\right]\right)-m\right]^2\right\}\\ &= \min\left\{{M_f}^2+\left[\sqrt{x^2-{M_f}^2}-m\right]^2\right\}\\ &= \min\left\{x^2+m^2-2m\sqrt{x^2-{M_f}^2}\right\}\\ &= \min\left\{f(x)\right\}\end{aligned}$$

Equation 19

Deriving f(x) and setting the derivative to zero gives:

$$\frac{\partial f(x)}{\partial x}=2x\left(1-\frac{m}{\sqrt{x^2-{M_f}^2}}\right)=0\Rightarrow x=\sqrt{{M_f}^2+m^2}$$

Equation 20

$$cos\left(\frac{\varphi_1}{2}\right)=x=\sqrt{{M_f}^2+m^2}\Rightarrow\varphi_1=2\cdot arccos\left(min\left\{\sqrt{{M_f}^2+m^2},1\right\}\right)$$

Equation 21

The inner and outer phase shift angle trajectories for the minimum RMS value of the resonant current can be obtained from these equations.

5.1.4.2 Variable switching frequency analysis

If switching frequency is variable over the working condition, it can be used to control the power transferred to the grid. The RMS value of resonant current is given by:

$$\left|\frac{{i_{r,rms}}^1}{i_g}\right|=\frac{\pi}{\sqrt{2}}\sqrt{\frac{A^2+B^2}{A^2}}=\frac{\pi}{\sqrt{2}}\sqrt{1+\frac{B^2}{A^2}}\Rightarrow\left|{i_{r,rms}}^1\right|=\frac{\pi|i_g|}{\sqrt{2}}\sqrt{1+\frac{B^2}{A^2}}\geq\frac{\pi|i_g|}{\sqrt{2}}$$

Equation 22

$|i_g|$ is the current passing between the microinverter and the grid, which is directly related to the transmitted power. When B = 0, the RMS value of the resonant current reaches a minimum value of $\pi|i_g|$ / 2. However, the condition B = 0 is only possible during buck mode. In Buck mode, B = 0 when the phase angle of resonant current θ_i is zero when the vector of resonant current is exactly parallel to the vector of the secondary voltage V_s. The phasor diagram is as follows:

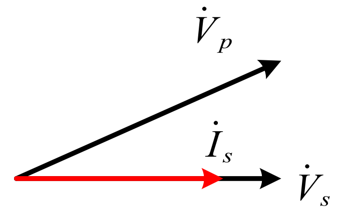


Figure 51 Phasor diagram when θi = 0

The vector diagram shows that when the phase of the resonant current and the phase of the secondary voltage are equal. The corresponding RMS value of the resonant current is at its minimum so the secondary switch can achieve zero current switching. However, this condition alone does not determine the value of the inner and outer phase shift angles. On this basis, if $\phi_\delta = \phi_1 / 2$ is specified, the zero-current switching of the primary-side switches can also be achieved. The corresponding inner and outer phase shift angle trajectory in buck mode is shown as follows:

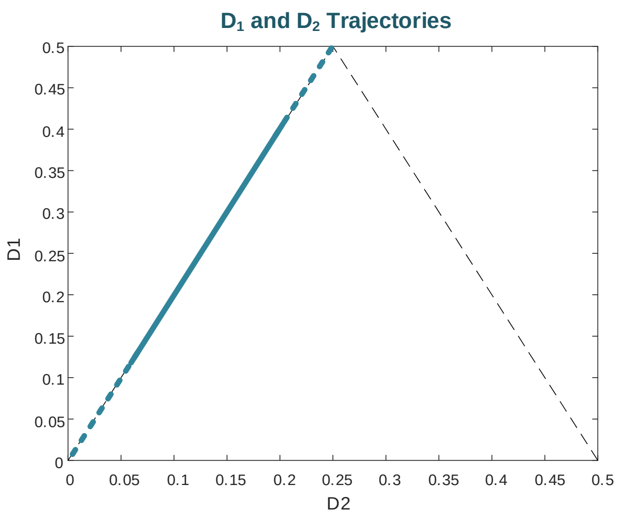


Figure 52 D1 and D2 trajectories in buck mode

In boost mode, the inner phase shift angle remains at zero. Defining the intermediate variable $x = \cos(\phi_\delta)$, the expressions of resonant current can be transformed to:

$$\left|i_{r,rms}{}^{1}\right| = \frac{\pi|i_g|}{\sqrt{2}}\sqrt{1+\frac{B^2}{A^2}} = \frac{\pi|i_g|}{\sqrt{2}}\sqrt{1+\frac{(cos\varphi_\delta - m)^2}{1-cos^2\varphi_\delta}} = \frac{\pi|i_g|}{\sqrt{2}}\sqrt{1+\frac{(x-m)^2}{1-x^2}} = \frac{\pi|i_g|}{\sqrt{2}}\sqrt{g(x)}$$

Equation 23

Where,

$$g(x) = 1 + \frac{(x-m)^2}{1-x^2}$$

Equation 24

Solving the derivative of g(x) at zero yields the maximum value:

$$\frac{\partial g(x)}{\partial x} = \frac{-2m(1-x^2)+2x(1-2mx+m^2)}{(1-x^2)^2} = \frac{-2(x-m)(mx-1)}{(1-x^2)^2} = 0 \Rightarrow x = \frac{1}{m}$$

Equation 25

$$cos\varphi_\delta = \frac{1}{m} \Rightarrow \varphi_\delta = arccos\left(\frac{1}{m}\right)$$

Equation 26

$$cos\varphi_\delta = \frac{1}{m} \Rightarrow \left|{i_{r,rms}}^1\right| = \frac{\pi|i_g|}{\sqrt{2}}\sqrt{1+\frac{\left(\frac{1}{m}-m\right)^2}{1-\frac{1}{m^2}}} = \frac{\pi m|i_g|}{\sqrt{2}}$$

Equation 27

The inner and outer phase shift angle trajectory in boost mode is shown here:

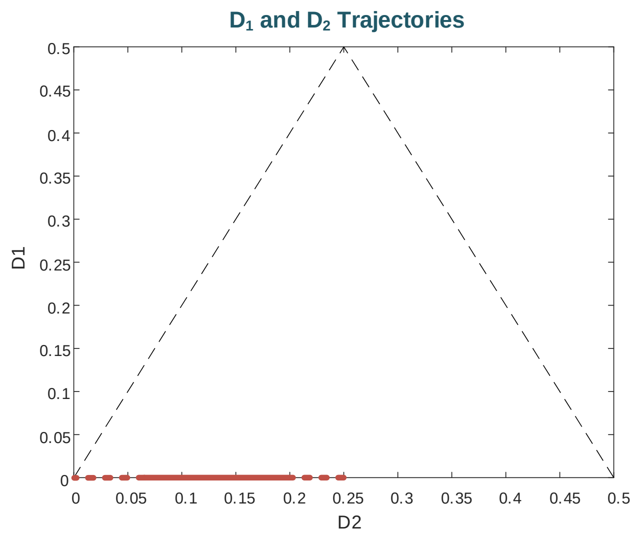


Figure 53 D₁ and D₂ trajectories in boost mode

It should be noted that when the voltage gain m = 1, the corresponding inner and outer phase shift angles D_1 and D_2 are both equal to 0. At this point, the switching frequency is equal to the resonant frequency, which is a non-permitted condition. In order to ensure the normal operation of the circuit, it is possible to limit the minimum switching frequency of the inverter operation so that the total internal and external phase shift angle trajectories are:

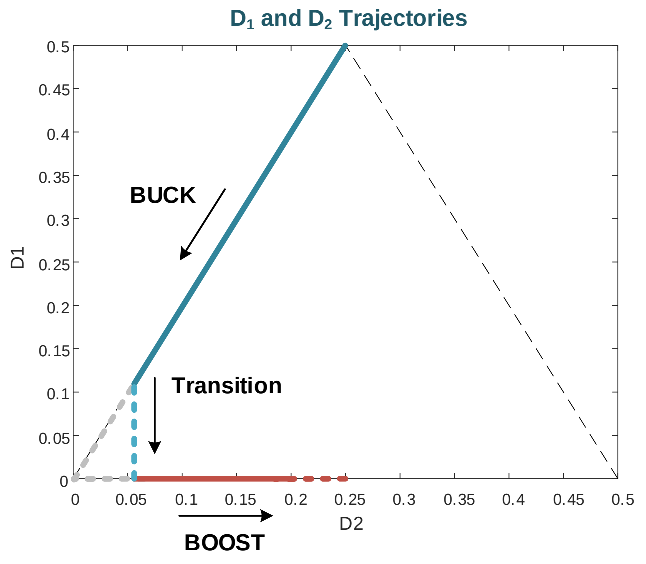


Figure 54 Overall D_1 and D_2 trajectories

5.1.4.3 ZVS optimization modulation

With the above modulation strategy, the switches of the primary-side leading-bridge arm can achieve ZVS zero voltage switch-on, and the primary-side lagging switches and the secondary-side switches can achieve ZCS zero current switch-on. The corresponding typical waveforms are shown in Figure 55:

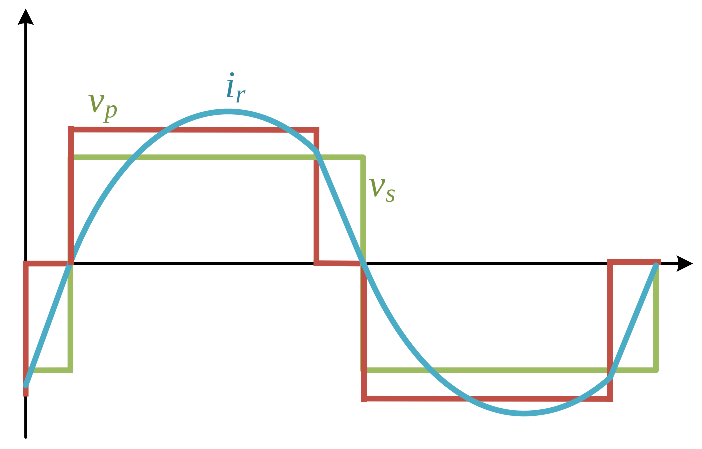


Figure 55 Waveforms under minimum RMS current modulation

To fully realize ZVS soft switching with lag switching on the primary side and over-switching on the secondary side, a small displacement Δϕ can be added to the outer phase shift angle D_δ so that the modified voltage-current waveforms are of the following form. The relationship between turn-on currents i_{lag} and i_{sec} with displacement Δϕ are:

$$i_{lag} + i_{sec} \approx \sqrt{2} i_{r,rms} \sin(\Delta\varphi) = \frac{4nV_{dc}\sin(\Delta\varphi)}{\pi Z_r\left(\frac{f_s}{f_r}-\frac{f_r}{f_s}\right)}\sqrt{\left[\cos\left(\frac{\varphi_1}{2}\right)\sin(\varphi_\delta)\right]^2 + \left[\cos\left(\frac{\varphi_1}{2}\right)\cos(\varphi_\delta) - m\right]^2}$$

Equation 28

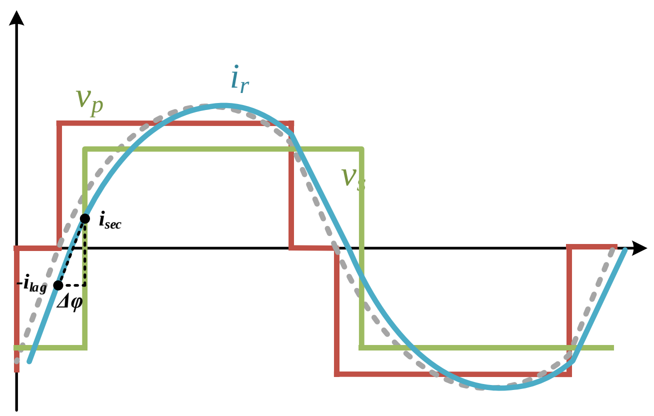


Figure 56 Waveforms with a small displacement added to Dδ

The displacement Δϕ is small, therefore, assume that the amount of change in the RMS value of the resonant current after the introduction of the displacement can be neglected and thus the above equation can be simplified as:

$$I_{zvs} \approx \sqrt{2} i_{r,rms} \, sin(\Delta\varphi) \approx \sqrt{2} \cdot sin(\Delta\varphi) \cdot \frac{\pi|i_g|}{\sqrt{2}} \cdot max\{1, m\} \approx \pi|i_g| \, tan(\Delta\varphi) \times max\{1, m\}$$

Equation 29

$$I_{zvs} = i_{lag} + i_{sec}$$

Equation 30

By setting I_{zvs} to an appropriate value the displacement Δϕ can be calculated and all switches can realize ZVS, while maintaining a low RMS value of the resonant current.

In boost mode the phasor diagram of minimum RMS current modulation is:

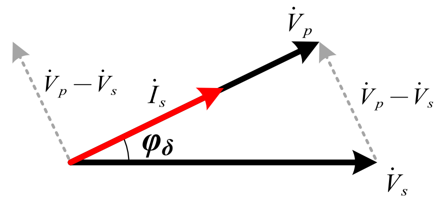


Figure 57 Phasor diagram in boost mode

This is because $cos(\phi_\delta) = 1/m = V_p/V_s$ and the vector $\dot{V}_p - \dot{V}_s$ is perpendicular to vector $\dot{V}_p$. Therefore, the vector of resonant current I_S is exactly parallel to the vector of the primary voltage V_p. The corresponding typical waveforms are shown below. In boost mode, the switches of the secondary-side switches can easily achieve ZVS, while all switches on the primary side are switching at zero current.

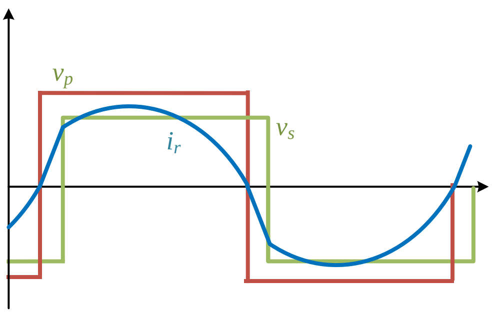


Figure 58 Waveforms of minimum RMS current modulation under boost mode

Similarly, a small displacement Δϕ can be added to the outer phase shift angle D_δ to help achieve full ZVS of all primary switches, so same modulation strategy as in buck mode can be used in boost mode.

The PWM control scheme driving the switches is shown below of a period of several AC line cycles:

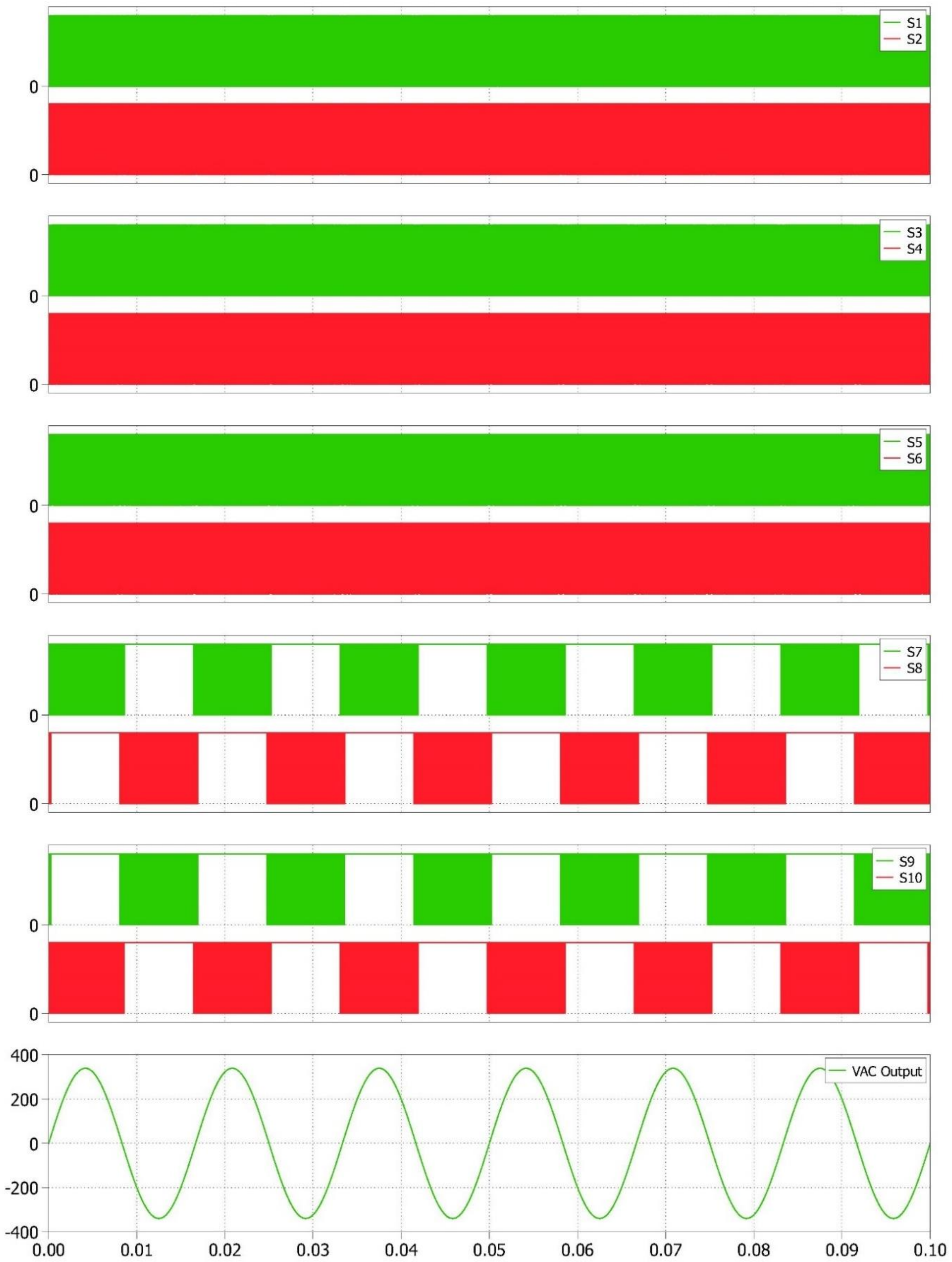


Figure 59 **Cycloinverter PWM scheme over several line cycles**

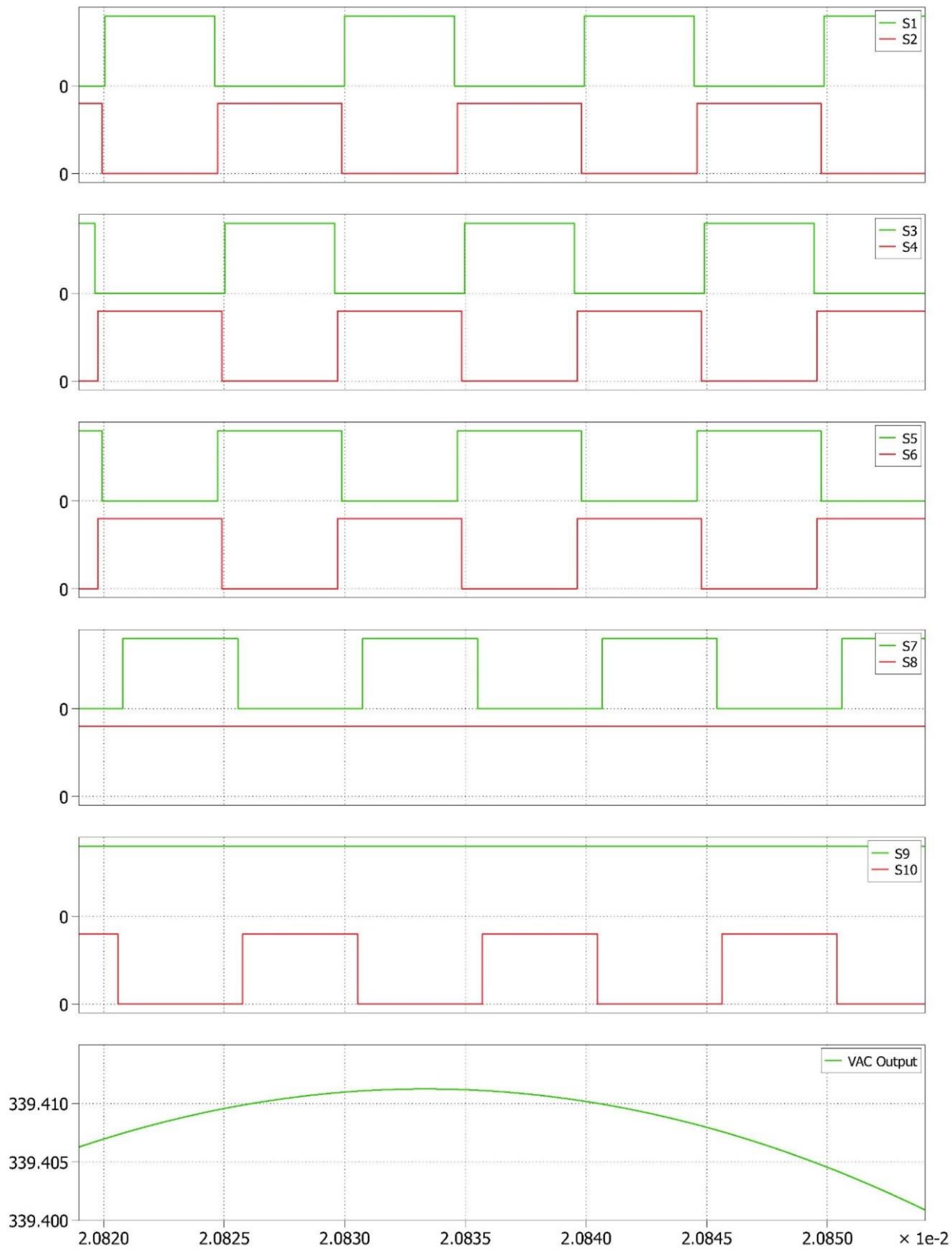


Figure 60 Cycloinverter PWM scheme at the switching frequency (at the positive AC output peak)

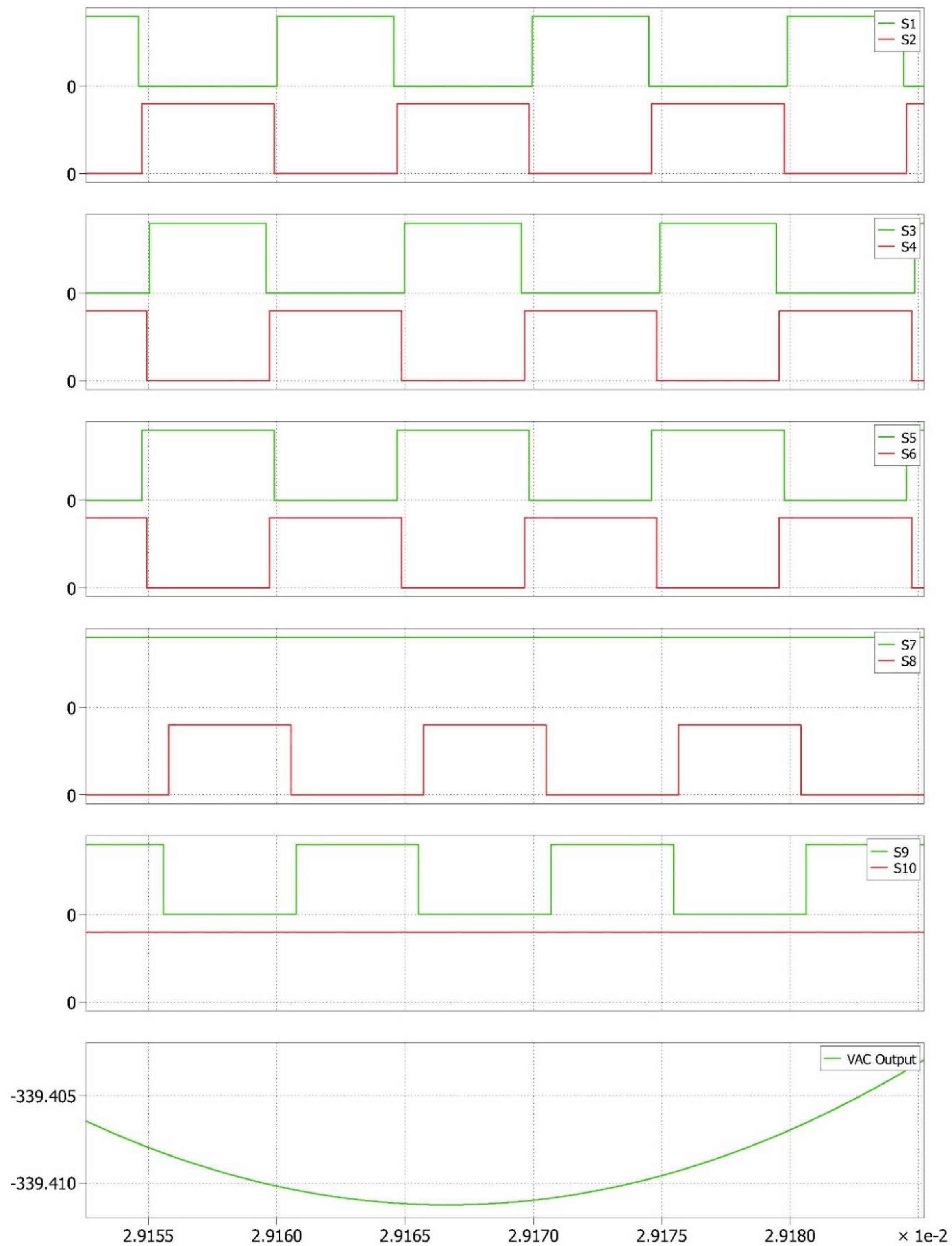


Figure 61 **Cycloinverter PWM scheme at the switching frequency (at the negative AC output peak)**

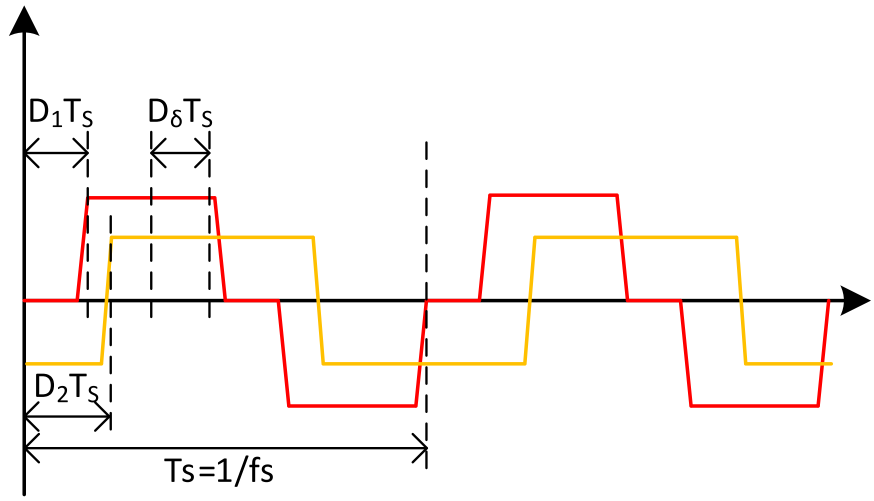


Figure 62 Modulation scheme

The switching frequency and duty cycles are varied over the period of the grid voltage half cycle to create a frequency and phase-locked sinusoidal current source at the grid connection whose amplitude and phase shift relative to the grid may be adjusted to transfer a defined AC power, which may include real and reactive components.

The reference designators in the following sections refer to the schematics (refer to Section 4), which differ from those used in the sections above.

5.2 Power stage and gate drivers

The DC input includes a bank of electrolytic capacitors C1, C2, C3, C4, and C119, required to absorb low frequency ripple at twice the AC grid frequency. This is necessary to achieve accurate and stable AC power and MPPT control. Capacitor sizing is based on the following calculation where a maximum allowable input voltage ripple of +/-5 percent is assumed, which is approximately +/-1.2 V under the worst-case minimum input voltage of 25 V.

$$C_{dc} = \frac{P_{PV}}{2\pi f_{ripple} V_{MPP} v_{ripple}} = \begin{cases} \dfrac{500W}{2\pi \cdot 120Hz \cdot 25V \cdot 1.2V} = 22.1mF \left(f_{AC} = 60Hz \right) \\ \dfrac{500W}{2\pi \cdot 100Hz \cdot 25V \cdot 1.2V} = 26.5mF \left(f_{AC} = 50Hz \right) \end{cases}$$

Equation 31

Since we have chosen to use five parallel capacitors, the value of each one should be 26.5 mF divided by 5, which equals 5300 µF. For convenience we have used the next lowest available value of 4700 µF.

The DC input also includes a high frequency EMI filter including eighteen parallel ceramic capacitors C5 to C22.

The primary side power stage consists of a full bridge with an additional bidirectional switch as shown in Figure 29. These switches are implemented with OptiMOS™ 6 power MOSFET 80 V parts in a 5 x 6 mm QFN package with a maximum $R_{DS(on)}$ of 1.45 mΩ. A heatsink is mounted to provide top-side cooling through a 1 mm thick thermal insulation material. The full bridge switches Q1, Q2, Q3, and Q4 are driven by non-isolated half-bridge gate drivers IC1 and IC2 referenced to the signal ground (SGND), which is connected at a single point to the power ground (PGND) connected to the DC input negative. The microcontroller U5 ground (DGND) is also referenced to the same primary side ground with proper separation of signal, digital, and power grounds implemented in the board layout.

The primary bidirectional switch comprising Q5 and Q6 uses OptiMOS™ 6 power MOSFET 80 V parts in 5 mm x 6 mm QFN package with a maximum $R_{DS(on)}$ of 5.6 mΩ with two single gate driver ICs with true differential inputs, U3 and U4, which are supplied from separate bootstrap circuits derived from the 12 V auxiliary supply.

The secondary side power stage consists of the two common-drain CoolGaN™ bidirectional switch 600 V Q7 and Q8 in TOLL packages with 55 mΩ typical $R_{SS(on)}$. Each of these devices is controlled by two separate gate drive circuits with different source potentials requiring two isolated gate drive circuits for each bidirectional switch. These are implemented by means of dual channel-isolated gate drivers U1 and U2 for which the input sides, which receive the PWM drive pulses from the microcontroller, are referenced to SGND. The outputs are all referenced to different potentials except for two that share the same ground, therefore requiring three separate floating voltage supplies.

The primary and secondary stages are linked through the transformer TR1, which provides a 1 to 5 step-up ratio. The secondary current passes through a current transformer CT1 to enable the current to be read by the microcontroller.

5.2.1 Transformer turns ratio selection

As discussed earlier, the turns ratio *n* of the main transformer is one of the most important parameters for design optimization in this topology because it affects the proportion of time in buck and boost mode operation during the AC line half cycle. Referring back to Figure 49, when the turns ratio is high, the circuit will operate in buck mode for a longer period or even continuously if the turns ratio is very high. Optimized modulation in buck mode allows the RMS secondary resonant current of the transformer to reach a theoretical minimum, however the corresponding large turns-ratio results in increased RMS primary current. Conversely, when the turns ratio is small the circuit operates in boost mode for longer. In this case, the current reflected from the secondary to the primary will be relatively small but the RMS value of the secondary resonant current will be higher compared to the buck mode.

Considering the difference in the RMS values of the current, the weighted sum of the RMS values of the primary and secondary currents is taken as the optimization objective, and the modulation strategy described earlier is selected, ignoring the transition phase when switching between buck and boost modes.

An optimization function *W* is used, which represents the conduction loss of the primary and secondary switches and is defined as:

$$W = {i_{p,rms}}^2 R_{on,pri} + {i_{s,rms}}^2 R_{on,sec} = {i_{s,rms}}^2 \left(n^2 R_{on,pri} + R_{on,sec}\right)$$

$$= {i_{s,rms}}^2 (0.00145 n^2 + 0.0042)$$

$$i_{s,rms} = \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} {i_r}^2(t) dt}$$

$$i_r(t) = \begin{cases} \frac{\pi \left| i_g(t) \right|}{\sqrt{2}}, m(t) < 1 \\ \frac{\pi m \left| i_g(t) \right|}{\sqrt{2}}, m(t) \geq 1 \end{cases}$$

Equation 32

At rated operating conditions V_{DC} = 35 V, V_{AC} = 240 V_{RMS}, P = 500 W, the optimization function W varies with turns ratio as shown:

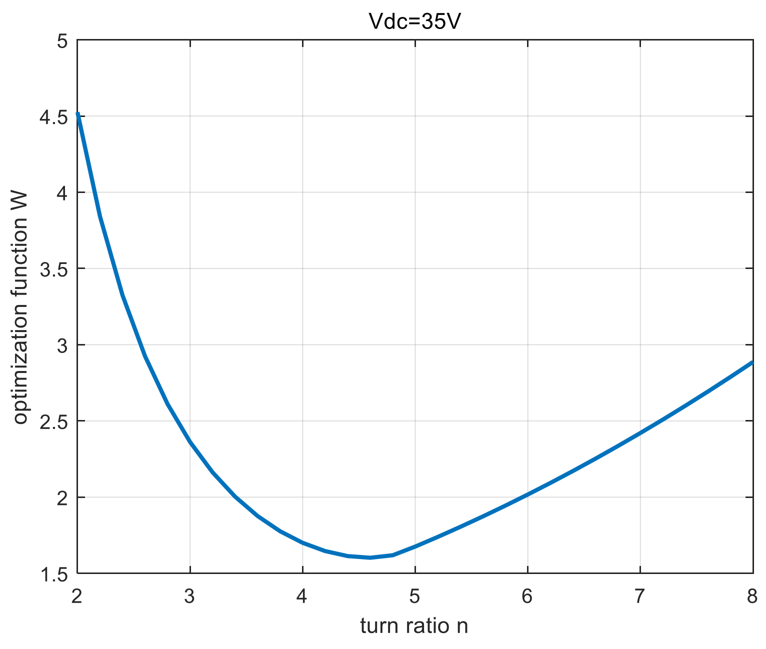


Figure 63 Optimization function used for selection of the turns-ratio *n*

Curves are plotted for different operating points, which are then averaged to find the optimum turns-ratio for the design:

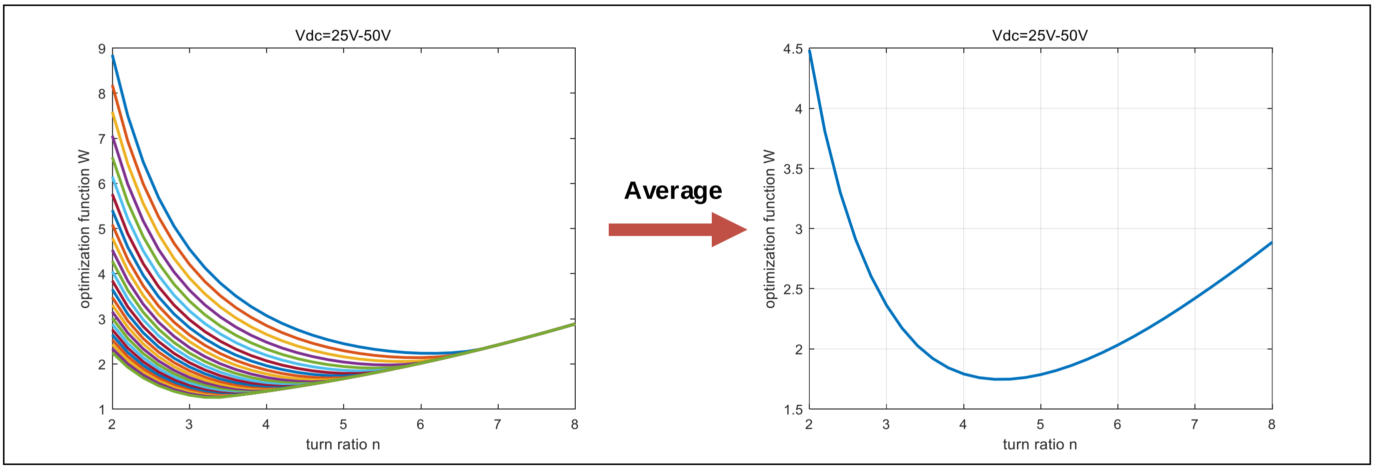


Figure 64 Optimization function averaged for multiple operating points

Based on the above analysis to achieve the lowest RMS resonant current, the selected transformer turns ratio is 1 to 5.

5.2.2 Resonant inductor and capacitor selection

The selection of resonant inductor and capacitor values is mainly related to the resonant frequency, resonant current and resonant voltage. The resonant parameters can be designed based on the current-voltage stress and transmitted power constraints. The expressions for the resonant current and resonant voltage of the microinverter are:

$$i_{r,rms}{}^{1} = \frac{2\sqrt{2}V_p}{\pi Z_r\left(\frac{\omega_s}{\omega_r}-\frac{\omega_r}{\omega_s}\right)}\sqrt{\left[\cos\left(\frac{\varphi_1}{2}\right)\sin\left(\varphi_\delta\right)\right]^2+\left[\cos\left(\frac{\varphi_1}{2}\right)\cos\left(\varphi_\delta\right)-m\right]^2}$$

$$v_{r,rms}^{1} = \frac{i_{r,rms}{}^{1}}{\omega_s C_r} = \frac{\omega_r Z_r}{\omega_s} i_{r,rms}{}^{1}$$

Equation 33

These should satisfy the following conditions:

$$i_{r,rms} \geq \frac{\pi\left|i_g\right|}{\sqrt{2}}\cdot\max\left\{1,m\right\}$$

$$v_{r,rms} = \frac{i_{r,rms}}{\omega_s C_r} \geq \frac{\omega_r Z_r}{\omega_s}\cdot\frac{\pi\left|i_g\right|}{\sqrt{2}}\cdot\max\left\{1,m\right\}$$

Equation 34

The true voltage-current value ratio is always larger than the estimated value, which adds some margin for design. The voltages of capacitors C1 and C2 each need to carry half of the grid voltage thus the capacitor voltage is expressed as:

$$V_{C1} = \frac{v_g(t)}{2} + v_r(t) \Rightarrow V_{C1,max} = \frac{V_{g,max}}{2} + \sqrt{2}v_{r,rms,max}$$

Equation 35

The peak AC voltage should never exceed the rated DC voltage of the MLCCs and the RMS voltage of the AC grid voltage should be limited to the rated DC voltage of the MLCC divided by two-root-two, as seen below:

$$V_{ac,peak} + V_{dc,bias} < V_{rated\ DC}$$

Equation 36

$$V_{ac,peak} < \frac{V_{rated\ DC}}{2} \Rightarrow V_{ac,rms} < \frac{V_{rated\ DC}}{2\sqrt{2}}$$

Equation 37

At 500 W at 240 V_{RMS} the peak grid current is close to 3 A. Considering a high AC line condition, the resonant current and voltage magnitudes are:

$$i_{r,rms,max} \approx \frac{\pi \left| i_{g,max} \right|}{\sqrt{2}} \cdot \frac{276 \cdot \sqrt{2}}{2 \cdot 25 \cdot 5} = 10.4A, \quad v_{r,rms} = \frac{\omega_r Z_r}{\omega_s} \cdot i_{r,rms,max} \approx 10.4 Z_r$$

$$v_{ac,rms} = v_{r,rms} = 10.4 Z_r, \quad v_{ac,peak} + V_{dc,bias} = \sqrt{2} v_{r,rms} + \frac{V_{g,max}}{2} = 14.7 Z_r + 195$$

Equation 38

The MLCC with a rated voltage of 1000 V is selected as the resonant capacitor and the calculation gives the constraint relationship of the resonant impedance as follows:

$$10.4 Z_r \le \frac{1000}{2\sqrt{2}} \Rightarrow Z_r \le 34$$

$$14.7 Z_r + 195 \le 1000 \Rightarrow Z_r \le 54.76$$

Equation 39

On the other hand, the microinverter also needs to satisfy power constraints and should have the ability to transmit sufficiently high power with the stable operating point should be in a reasonable interval. In the analysis, the operating point switching frequency range for maximum instantaneous power as [1.1f_r, 1.4f_r] at the above conditions.

$$P_{trans} = \frac{4nV_{dc} v_g}{\pi^2 Z_r \left(\frac{\omega_s}{\omega_r} - \frac{\omega_r}{\omega_s} \right)} \cos\left(\frac{\varphi_1}{2} \right) \sin\left(\varphi_\delta \right) \Rightarrow P_{\max} = \frac{4nV_{dc} v_g}{\pi^2 Z_r \left(\frac{\omega_s}{\omega_r} - \frac{\omega_r}{\omega_s} \right)} \Rightarrow i_{\max} = \frac{4nV_{dc}}{\pi^2 Z_r \left(\frac{\omega_s}{\omega_r} - \frac{\omega_r}{\omega_s} \right)}$$

$$i_{\max}(f_s = 1.1 f_r) = \frac{4nV_{dc}}{\pi^2 Z_r \left(1.1 - \frac{1}{1.1} \right)}, \quad i_{\max}(f_s = 1.4 f_r) = \frac{4nV_{dc}}{\pi^2 Z_r \left(1.4 - \frac{1}{1.4} \right)}$$

$$\Rightarrow 24.6 < Z_r < 88.5$$

Equation 40

The resonant inductor inductance is designed to be 60 µH integrated into the transformer, with the half-bridge capacitance at 30 nF. The resonant parameters of the circuit are as follows:

$$L_r = 60\mu H, C_r = 2C_1 = 60nF$$

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} = 83.9kHz, Z_r = \sqrt{\frac{L_r}{C_r}} = 31.6$$

Equation 41

5.3 Output filter and relay

The output from the secondary side is connected to the AC grid through the output filter and relay K1. The grid voltage is sensed directly at the output terminals and sampled by the microcontroller whether the relay is open or closed. This ensures that the system will be physically disconnected from the grid until the inverter has successfully synchronized to the voltage, frequency, and phase. The relay will be disengaged when a fault condition is detected.

High frequency components are removed by the two-stage output filter network, which consists of two common-mode inductors Lf1 and Lf2 with low DC resistance. These also include sufficient leakage inductance to filter out common and series mode noise. Filter capacitors C35, C36, and C37 are X2 safety rated metallized polypropylene film EMI suppression capacitors.

5.4 On board auxiliary power

The DC input feeds a fly-buck regulator based on IC3 that can operate from up to 80 V. This provides a non-isolated stable 12 V DC rail referenced to SGND as well as three floating 10 V outputs used to supply the secondary side switch gate drive circuits.

The 12 V rail supplies a second buck regulator based on IC4 to provide a stable 5 V rail, which in-turn feeds another buck stage based on IC13 to provide a stable 3.3 V rail.

These provide all of the voltage supplies needed to supply the control and gate drive circuitry.

5.5 Control and monitoring circuitry

The microcontroller U5 is a main line PSOC™ Control C3 MCU developed specifically for power conversion applications. It is based on real-time control Arm® Cortex® - M33 based core with 180 MHz clock frequency, 64 kB SRAM and 256 kB flash. Peripherals include 12-bit, 12-MSPS SAR ADC and 16 x 16-bit and 4 x 32-bit TCPWMs, 4-channel HRPWM with <100 ps resolution as well as UART interfaces for communication and an SPI programming/debugging interface. U5 is supplied from the 3.3 V rail.

PWM gate drive signals generated by U5 are converted from 3.3 V to 5 V via a digital buffers IC6, IC11, and IC12.

For analog AC measurements a stable 1.65 V offset is required, which is provided by Q. The output is buffered through IC15.

AC output voltage is sensed before the output filter through a differential amplifier based on IC14 and also at the grid connections through another differential amplifier based on IC5. A Hall effect current sensor IC7 is used to measure the AC output current. Amplification and offset is added through IC5.

DC input voltage is sensed via a differential amplifier based on IC3, which also provides another differential amplifier for sensing and amplifying the input current from the input shunt R1. All of the voltage and current signals are amplified or attenuated to the correct range required for the ADC inputs of U5. The resonant current measurement from the current transformer CT1 is used for over current protection. This is rectified through Schottky diodes D16-19 and amplified through IC10 to provide input to U5. An additional over current protection circuit monitors the AC grid output current from IC5 and triggers a shutdown through a dual comparator circuit IC9 if the amplitude exceeds upper and lower limits.

The system also includes three temperature sensors: Rt1, Rt2, and Rt3 placed at different points on the board to enable the firmware to monitor component temperature and shutdown in the event of overheating.

5.6 Control and firmware

5.7 Control algorithm

The control functionality of a microinverter combines MPPT for optimal harvesting of solar energy from connected PV panels, combined with AC power flow control for transferring power onto the AC grid. The REF_500W_CYCLO_BDSGAN reference design board can be operated in grid-tied mode to enable AC power transfer to a grid simulator or simple inverter mode driving a passive or AC electronic load. The unit operates with a PC-based GUI via a serial interface, which enables different operating modes and operating parameters to be selected.

During off-grid mode, the user sets the output voltage through the GUI. The unit will not operate with the relay disconnected if an AC voltage is present at the output terminals during this mode.

During grid-tied mode a grid simulator should be connected to the output terminals and set to the desired voltage and line frequency. The user set the target output current through the REF_500W_CYCLO_BDSGAN Cyclo microinverter commander GUI with the MPPT function turned OFF by default. MPPT will operate correctly only if the board is connected to a PV source or power supply which includes a PV emulation mode such as the Chroma 62150H-1000S used to perform the tests documented here.

Note: *The unit will shut down if no grid voltage is detected at the output during this mode.*

The individual control variables are derived mathematically by calculating the specific values of the internal and external phase shift angles and the switching frequency, given the amount of power the converter needs to transmit at that moment. In grid-tied operation, the output current can differ from the actual current due to the presence of dead zones, and errors in the resonance parameters can lead to inaccurate calculated control quantities. These practical factors affect the magnitude and THD of the output current and influence the quality of the waveform, hence the need for closed-loop control of the microinverter.

The closed-loop block diagram of the microinverter is shown in Figure 65, comprising a current closed-loop control and an optimized modulation algorithm. In the current closed-loop, the error value of the AC current is obtained by taking the difference between the measured AC current and the reference AC current. This error is then passed through a quasi-proportional resonant (QPR) controller to obtain the error Δi_{ac}, which also represents the difference between the commanded power and the actual power being transferred. Δi_{ac} and the reference current i_{ref} are added together to generate the corrected reference current value, $i'_{ac,ref}$. This correction is required to reduce iTHD in the output. In the optimized modulation block, the system samples the instantaneous input and output voltages. These values are used with the corrected reference current $i'_{ac,ref}$ to determine the required switching frequency f_{sw} with the inner phase shift angle D_1 and the outer phase shift angle D_2. These parameters are fed to the PWM generator to produce the gate drive pulses.

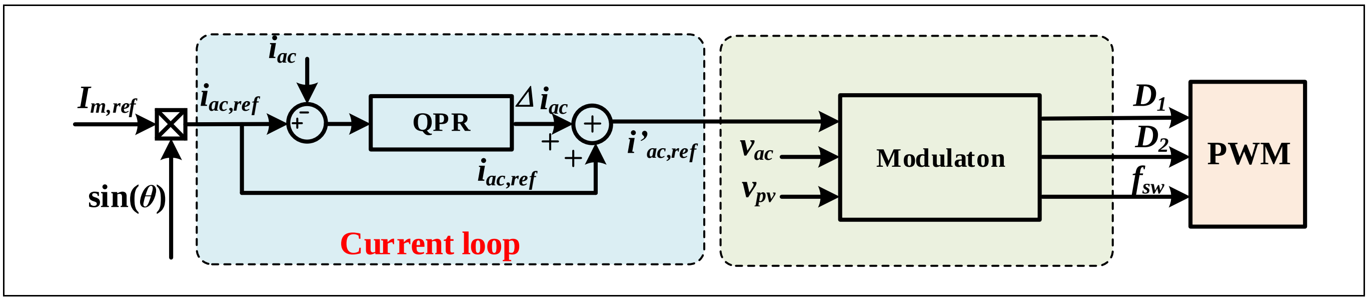


Figure 65 Control loop block diagram

The overall control framework consists of five components:

- MPPT controller
- Voltage loop controller
- SOGI-PLL phase-locked loop
- Feedforward controller
- Current loop controller

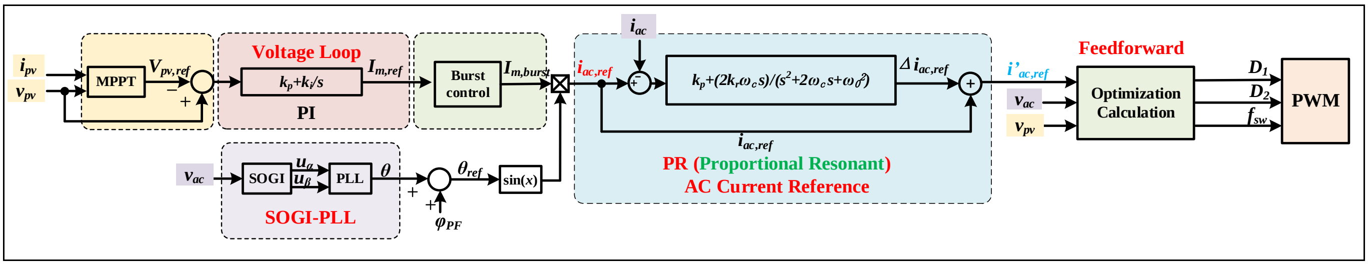


Figure 66 Overall control framework

The current control loop is based on a proportional resonant (PR) controller, which has a particular type of transfer function often used for the closed-loop control of systems with a sinusoidal behavior that includes both a proportional and a resonant term, which can be tuned independently.

Second-order Generalized Integrators (SOGI) for line frequency and phase synchronization in grid-tied inverters. The control structure o the SOGI-PLL is as follows:

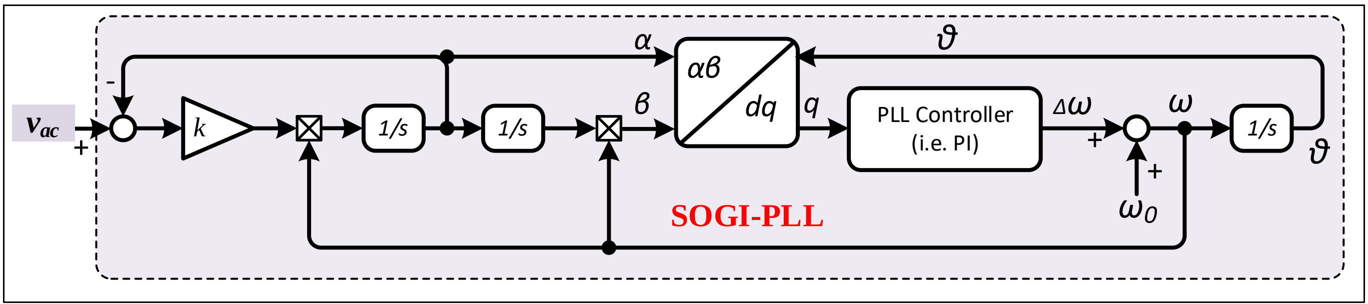


Figure 67 SOGI-PLL block diagram

The SOGI structure is composed of two filter types; first, a band-pass filter with zero-phase delay at the fundamental frequency for estimation of the AC grid voltage vα and secondly, a low pass filter with 90° phase delay to create a quadrature-shifted signal vβ. This enables the dq voltage signals to be calculated using the Park transform to provide inputs to a PI loop for PLL implementation.

5.7.1 MPPT control

The MPPT controller samples the PV terminal voltage v_{PV} and the PV output current i_{PV} at a sampling rate of 10 Hz, to provide average values with the ripple components averaged out. An incremental conductance algorithm is then used to generate the MPP reference voltage $V_{pv,ref}$. The difference between V_{pv} and $V_{pv,ref}$ is adjusted by the voltage loop controller to obtain the ac current magnitude reference value $I_{m,ref}$. The SOGI-PLL samples the AC voltage V_{ac} and generates the AC voltage phase angle θ. The combination of $I_{m,ref}$, θ and the given power factor angle ϕ_{PF} gives the AC current reference $i_{g,ref}$.

5.7.2 Feedforward control

The feedforward controller is used to improve the response speed of the microinverter, to extend the ZVS soft-switching range and to reduce the RMS resonant current. The switching frequency f_{sw}, inner phase shift angle D_1 and outer phase shift angle D_2 can then be calculated by the feedforward controller and current close-loop controller.

5.7.3 Burst mode control

To achieve ZVS variable switching frequency modulation is adopted. Generally, the switching frequency increases at lighter loads, which leads to higher turn-off losses. Moreover, considering the maximum frequency boundary, a hard switching condition is also possible resulting in efficiency reduction under light load conditions. To mitigate this, burst mode operation is introduced.

When burst mode is enabled, it operates when the power transfer is below a defined threshold of around 200 W and the power factor is unity. In burst mode, the inverter is periodically enabled and disabled at the grid AC voltage zero crossing point. When the inverter is disabled, there is no output current and energy is stored in the electrolytic capacitors. The inverter remains in an energy storage period for a number of AC grid voltage cycles, N_{off}. During the burst period, a burst current I_B is transferred to the grid in accordance with the energy stored in the input capacitors during the previous energy storage period. The inverter operates in the burst period for a number of AC grid voltage cycles, N_{on}. To transfer the same power the output current I_B must be greater than the output current during continuous mode I_{ref}.

Usually, the relationship of I_B and I_{ref} is:

$$I_B = \frac{N_{on} + N_{off}}{N_{on}} I_{ref}$$
$$I_{ref} = \frac{P_o}{V_{ac,rms}}$$

Equation 42

N_{on} is set to 1 (representing one complete AC grid cycle, i.e., two half cycles).

The burst mode current threshold I_{th} is defined as:

$$I_{th} = \frac{P_{th}}{V_{ac,rms}}$$

Equation 43

N_{off} can be any integer value; 1, 2, 3, etc. As the output power drops, N_{off} increases to maintain $I_B > I_{th}$.

$$I_B = (1 + N_{off}) I_{ref} > I_{th} \rightarrow 1 + N_{off} = \left\lceil \frac{I_{th}}{I_{ref}} \right\rceil (\text{Round up}) = \left\lfloor \frac{I_{th}}{I_{ref}} \right\rfloor + 1$$

Equation 44

The following diagram provides an illustration of equal power transfer in normal (continuous) operation where $I_B = i_{ref}$ and burst mode where $I_B = 2 \times I_{ref}$ and $N_{off} = 1$.

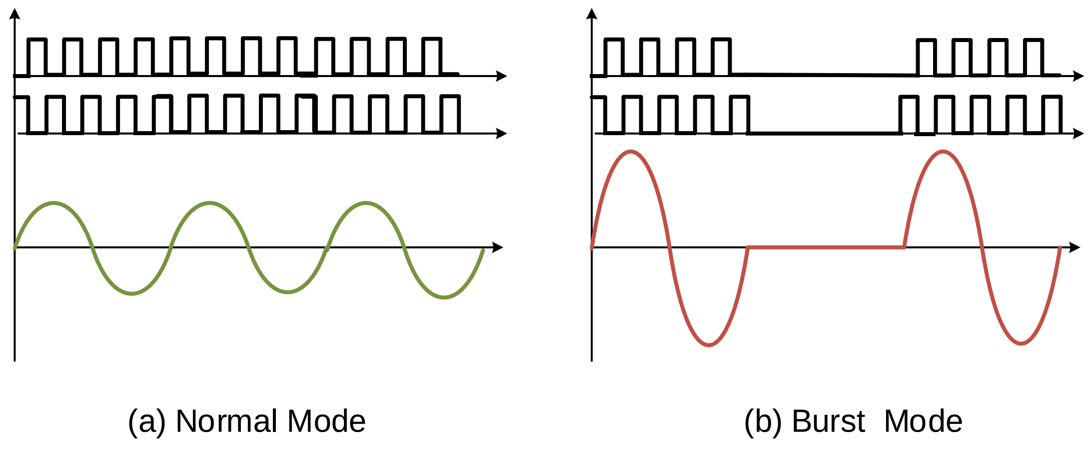


Figure 68 **Normal (continuous current) mode and burst mode operation**

Note that the efficiency measurement during burst mode is more challenging since the RMS current is not so easy to measure. A normal measurement even where the current is averaged over many samples may not provide an accurate result. This can be done only by determining the RMS current in a continuous state where the peak is equal to the peak in burst mode and then multiplying this current by $N_{on}/(N_{on}+N_{off})$ to obtain a true average RMS. For example, in the case shown in the above figure, the current would need to be set to twice the value in continuous mode to reach the same peak value as in burst mode. The RMS value could then be measured and divided by 2 to provide a result to use in calculating the true output power.

5.8 Firmware implementation

5.8.1 Overview

The firmware is built on the Eclipse IDE for ModusToolbox™. The *main.c* file is located in the project root directory with the header and other source files in the Source folder. The main function includes calls to the board and solution files that implement the system framework along with slow background tasks. The firmware structure uses multiple events triggered interrupts to execute control algorithms, communication, input sampling, status checks, fault protection, and other functions. A high-level flow chart is shown here:

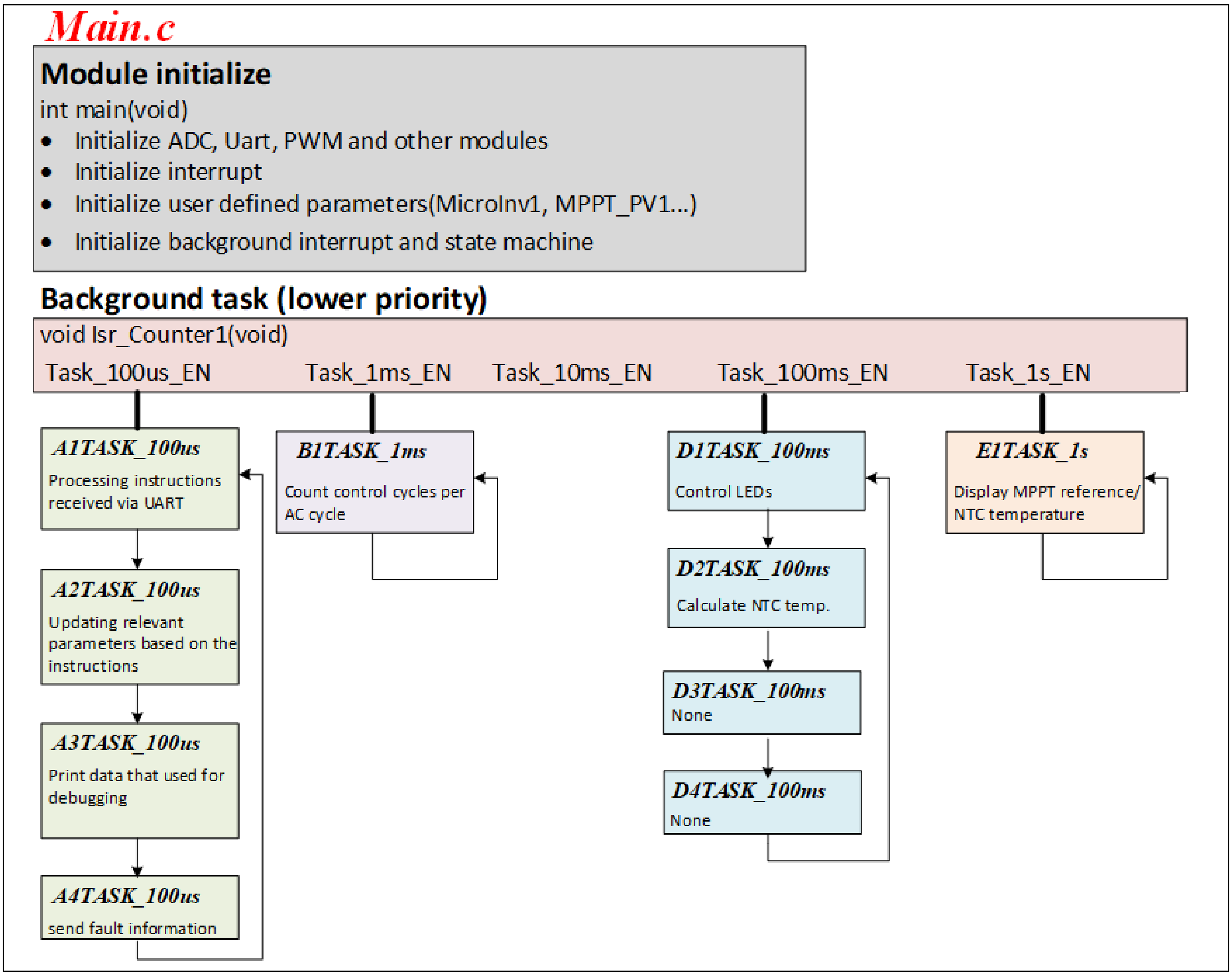


Figure 69 Main functions

The following table details the source and header files related to the different functions and peripherals.

Table 8 Source and header files

Source file	Header file	Functions supported
GlobalDef.c	GlobalDef.h	Macro and structure definitions
adc.c	adc.h	Initialization and data processing functions related to the ADC sampling module

Source file	Header file	Functions supported
User_gpio.c	User_gpio.h	I/O related initialization functions
User_pwm.c	User_pwm.h	PWM module initialization
User_uart.c	User_uart.h	UART communication-related initialization functions
User_closeloop.c	User_closeloop.h	Control algorithms used in closed-loop operations
User_init.c	User_init.h	Main control variable initialization
User_ISR.c	User_ISR.h	Interrupt service routines (ISRs) for ADC, PWM, GPIO, UART etc.
User_MPPT.c	User_PV.h	Maximum Power Point Tracking (MPPT) functions
User_sogi.c	User_sogi.h	SOGI-PLL phase-locked loop control
User_control.c	User_control.h	Main control code for the microinverter, including state machines for various operational modes, phase angle and frequency calculations, PWM control, fault handling, and more

5.8.2 Main.c and background tasks

The int main(void) function calls initialization functions such as cybsp_init(), User_uart_init(), and variable initialization functions such as Inverter_Init(). It enables the main loop and continuously calls (*Task_State_Ptr)() in the for(;;) infinite loop to poll five classes of time-multiplexed background functions from A0 to E0:

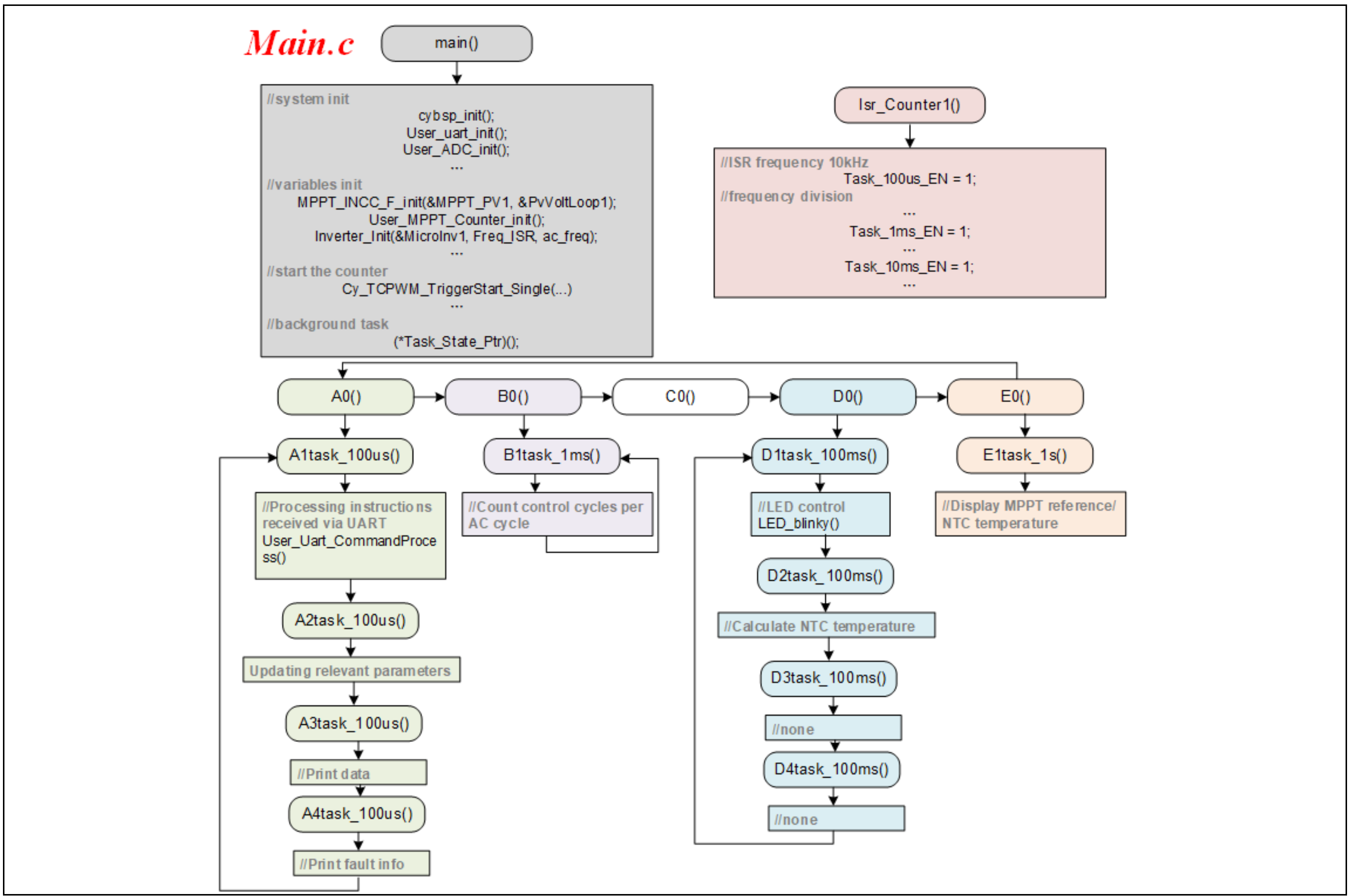


Figure 70 Main loop and timer driven processes

Additionally, there are five flags used to determine whether the background functions are executed: Task_100us_EN, Task_1ms_EN, etc. These flags are modified by the 10 kHz always-on interrupt program ISR_Counter. When a flag is activated, the corresponding background task is executed, such as A1task_100us(), A2task_100us(), etc., up to E1task_1s(). For example, the ISR_Counter interrupt function sets Task_100us_EN to 1, and (*Task_State_Ptr)() checks Task_100us_EN in A0(void) before executing (*A_Task_Ptr)(). Initially, A_Task_Ptr points to A1TASK_100us, and after executing this task, it points to A2TASK_100us, and so on in a loop.

Background tasks are executed in the for(;;) infinite loop in main(), and these tasks can be interrupted by other interrupt handling functions, having the lowest priority, making them suitable for handling tasks with lower real-time requirements. In this project, Atask is used to respond to communication commands; Btask calculates how many control cycles are contained in a single AC cycle based on the phase-locked loop frequency; Dtask controls the LED and calculates NTC temperature; and Etask is responsible for sending MPPT reference voltage and temperature.

5.8.3 Control ISR

The REF_500W_CYCLO_BDSGAN system has three control variables: inner and outer phase angles, and switching frequency, which are related to input and output voltage, power, grid phase, and other parameters. The Control ISR function is responsible for controlling the microinverter's operating state, calculating each control variable, and generating the appropriate PWM signals as illustrated below. The Control ISR has the highest control priority in the program.

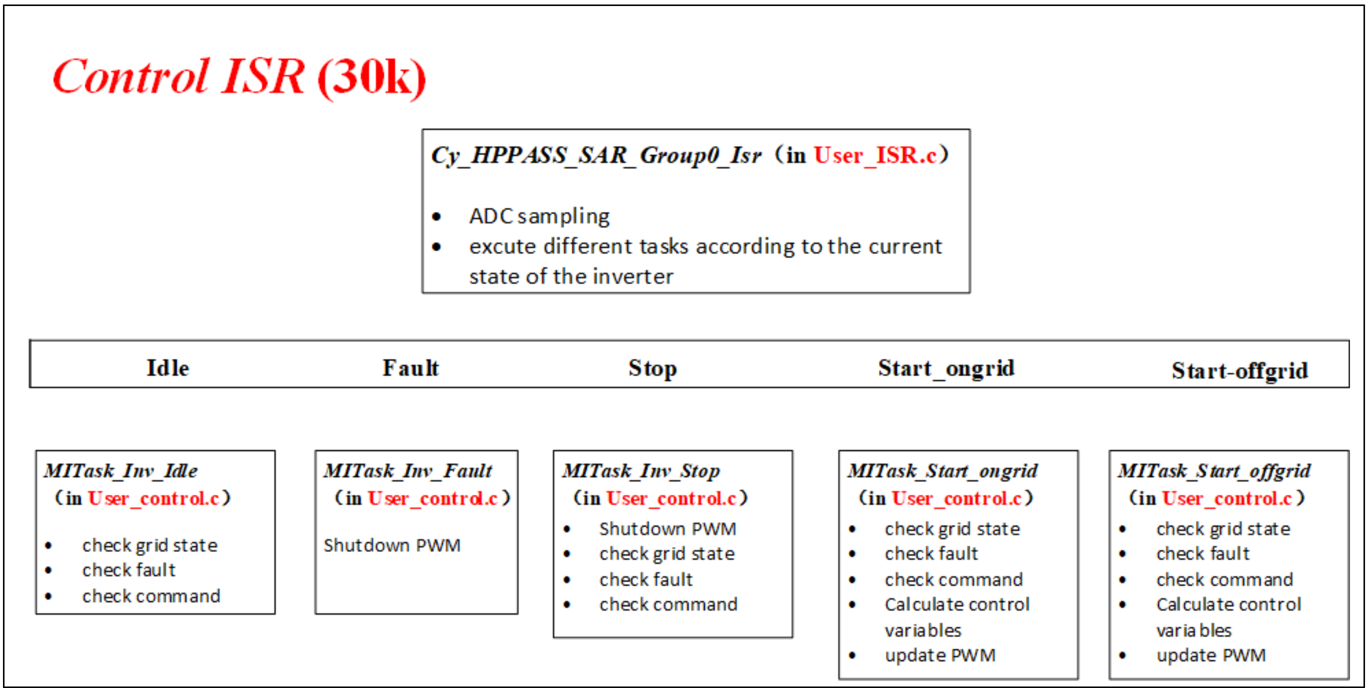


Figure 71 Control ISR operations

In this program, the entry point for the Control ISR is the ADC interrupt handling function Cy_HPPASS_SAR_Group0_Isr, located in User_ISR.c. The ADC is triggered by a 30kHz frequency PWMTri_ADC, and when sampling is complete, it triggers an interrupt then jumps to Cy_HPPASS_SAR_Group0_Isr. The flowchart for this process is as follows:

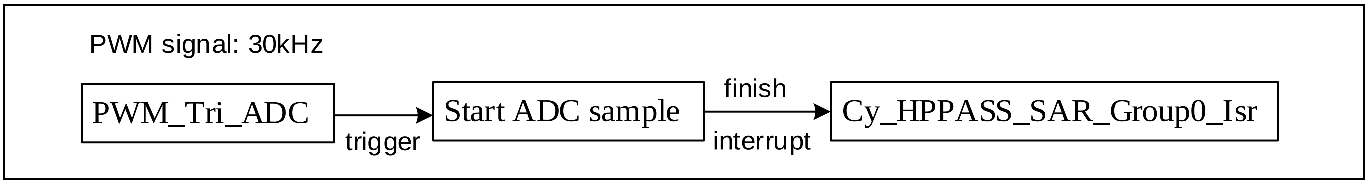


Figure 72 30 kHz process flow

Cy_HPPASS_SAR_Group0_Isr() first processes the ADC sampling data, converting the register values into actual sampled values. The system operates in the following states:

Table 9 System states

State	Description
Inv_Idle	Idle state, waiting for user commands
Inv_Fault	The unit has detected a fault and shut down, waiting for clear and reset
User_stop	The inverter is stopped by user command, waiting for re-start or reset command
Start_ongrid	Grid tied operation, the inverter is running
Start_offgrid	Off-grid operation, the inverter is running

After obtaining the corresponding sampled data, the control program jumps to execute different tasks based on the current inverter state. The functions for this part of the task are located in User_control.c.

Inv_Idle is the initial state after the processor powers on, during which all PWM signals are locked, and the converter stops running. The function executed in the Inv_Idle state is MITask_Inv_Idle(). In the idle state, it checks the grid status, fault status, and user commands. The grid status can be Grid_Undefined, Grid_Ongrid, or Grid_Offgrid. In the grid-connected operating state, the program detects the AC voltage at the port and closes the relay at the appropriate time; in the off-grid state, the relay only closes when there is no voltage at the port. The flow diagram for MITask_Inv_Idle() is shown in the following figure. In the idle state, the program may enter the Start_ongrid or Start_offgrid state based on control commands. If a fault is confirmed, it will also enter the Inv_Fault state.

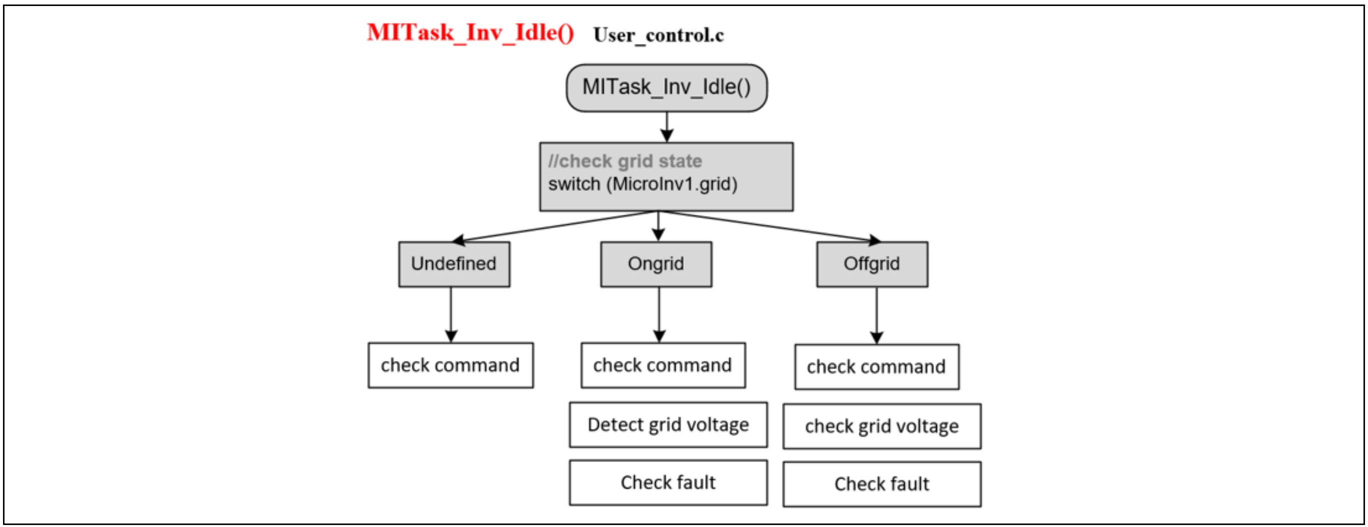


Figure 73 Initial idle state

When the program receives a power-on command, it can enter the Start_ongrid or Start_offgrid state based on the grid status control command, executing MITask_Start_ongrid() and MITask_Start_offgrid(), respectively, and the inverter begins to operate.

In the Start_ongrid state, the function executed is MITask_Start_ongrid(), corresponding to the flow diagram shown in the following figure.

First, the program executes the SOGI PLL phase-locked loop to synchronize with the grid voltage. It then checks for faults or whether a shutdown command has been received; if so, it executes specific procedures to shut down; otherwise, it continues to execute Control_OpenloopCalc_Ongrid() to calculate the inner and outer phase angles and switching frequency.

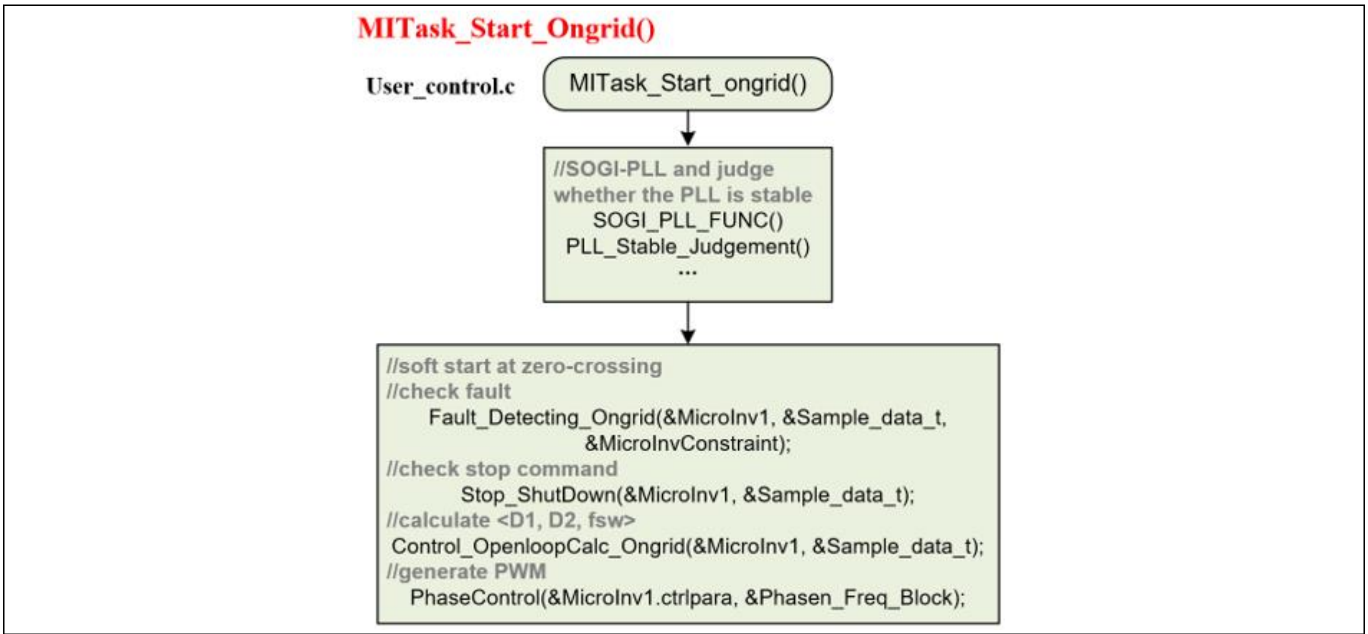


Figure 74 Connect to the grid

Control_OpenloopCalc_Ongrid() is used to calculate the inner and outer phase angles, as shown in the following flow diagram.

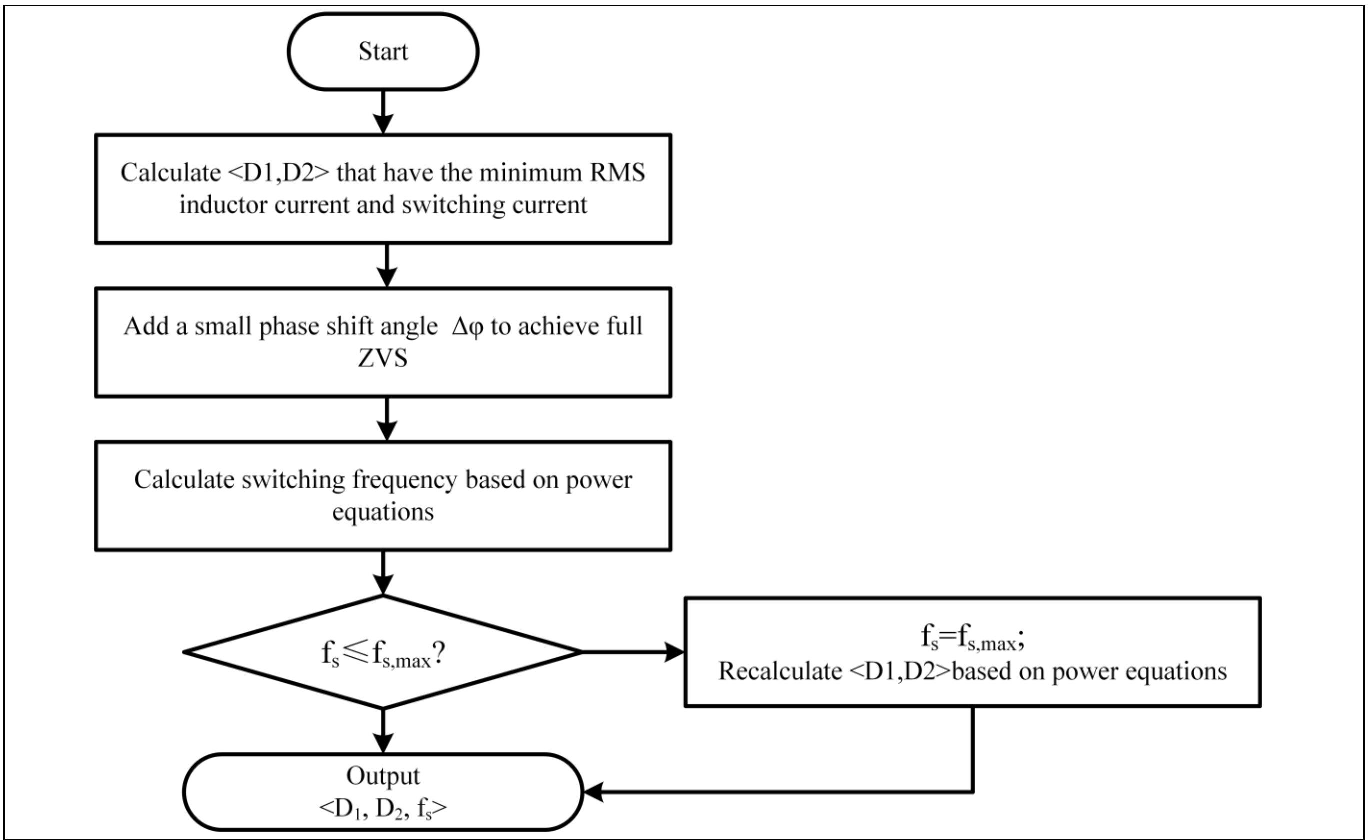


Figure 75 Calculating the inner and outer phase angles

PhaseControl() is responsible for generating PWM control signals. To generate the PWM signals for each switch, the comparison values 1 and 2 of the PWM module must be correctly configured, as shown in the following figure. For example, the comparison values 1 and 2 for the driving signal S1 should be:

$$0.5D\_1 \times PRD$$[1]

Equation 45

and

$$(0.5 - 0.5D\_1) \times PRD$$

Equation 46

respectively.

[1] PRD refers to the PWM cycle period, which defines the switching frequency.

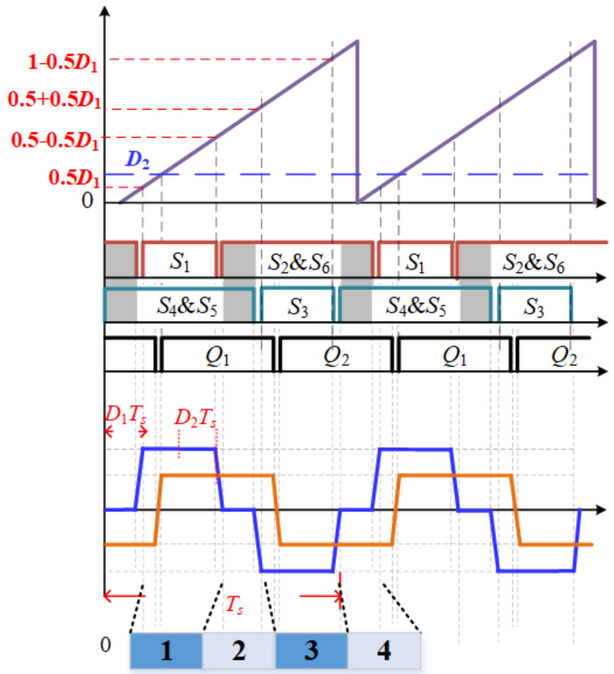


Figure 76 PWM encoding scheme

In the Start_offgrid state, the function executed is MITask_Start_offgrid(). In off-grid mode, there is no phase-locked loop; the grid phase is generated directly by the program, and the grid voltage is derived through PR closed-loop calculations. The system control flowchart under both grid-connected and off-grid conditions is shown in the following figure. The closed-loop programs for grid-connected and off-grid conditions are GridON_CurrentCloseLoop() and GridOFF_VoltageCloseLoop().

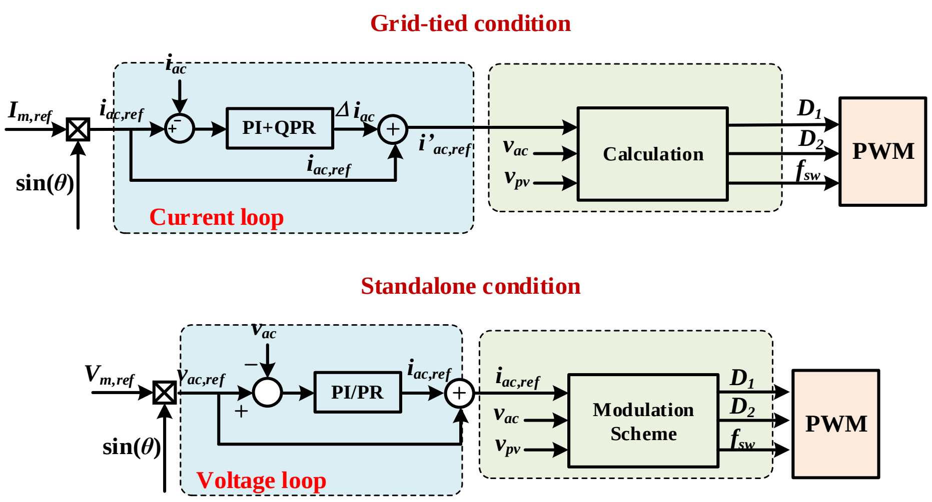


Figure 77 Control loop structures for grid tied and standalone operating modes

During the inverter's operation, when the processor receives a STOP command, it will execute Stop_ShutDown() to shut down the inverter. Although all switches in the primary side full-bridge circuit can be directly locked, due to the microinverter's secondary side having two sets of bidirectional switches, all switches cannot be locked directly; otherwise, the transformer current will lose its freewheeling path, resulting in high voltage across the switches, potentially damaging them.

Following the fault isolation method of a half-bridge DAB, the difference is that the common and cutoff switches on the secondary side need to switch logic based on the polarity of the grid voltage.

When the grid voltage is positive, lock the primary switches S1-S4, lock the secondary switches S6 and S8, and keep S5 and S7 conducting. After two control cycles, lock S5 and S7.

When the grid voltage is negative, lock the primary switches S1-S4, lock the secondary switches S5 and S7, and keep S6 and S8 conducting. After two control cycles, lock S6 and S8.

The flowchart for Stop_ShutDown() is shown in the following figure. After executing the shutdown command, the converter state will switch to User_stop.

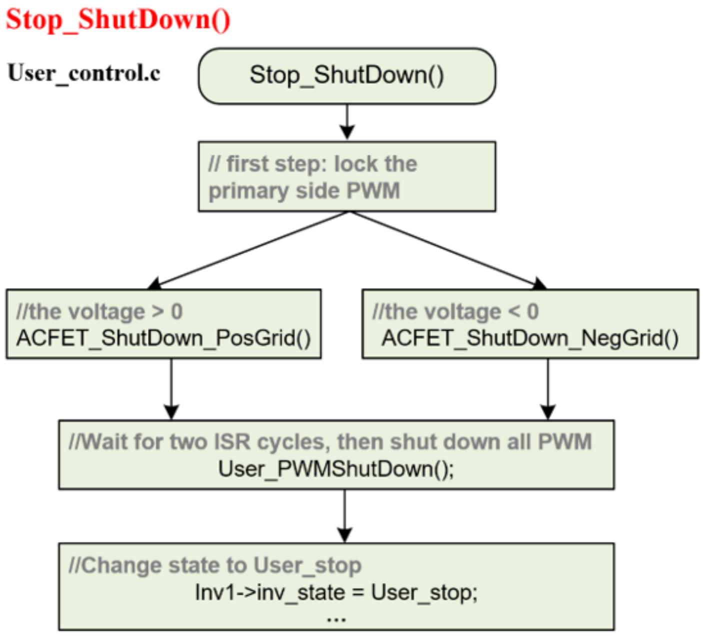


Figure 78 Inverter stop and shutdown functions

During the inverter's operation, when a fault is detected, the program will execute Fault_ShutDown() to shut down the inverter, and the locking process is consistent with the method described above. After executing the shutdown command, the converter state will switch to Inv_Fault.

In the User_stop state, the function executed is MITask_User_stop(). In this state, the inverter stops running, but upon receiving a Start command, it will re-enter the Start_ongrid or Start_offgrid state based on the grid status and execute the relevant commands.

In the Inv_Fault state, the function executed is MITask_Inv_Fault(). In this state, the inverter stops running, and upon receiving a Start command, it will not restart the inverter. The user must send the fault clearance command FaultClear@ before the controller allows the inverter to restart.

5.8.4 MPPT

The inverter has MPPT functionality based on an incremental conductance algorithm, which detects the slope of the P–V curve. The maximum power point is tracked using the instantaneous conductance I/V and the incremental conductance dI/dV. Depending on the relationship between the two values, the location of the operating point of the PV module in the P–V curve can be determined. The MPPT function is disabled by default and can be enabled by the user by sending the appropriate command through the serial interface. This is most easily done via the GUI tool.

The flow diagram for the MPPT function is shown in the following figure. In the program, the clock interrupt frequency of Timer_MPPT is configured to 480 Hz, with the interrupt handling function being ISR_MPPT_Task(). In ISR_MPPT_Task(), the program calls MPPT_PVVoltCheck() to check if the photovoltaic voltage is within the normal range and gradually updates the MPPT voltage setpoint through MPPT_SoftStart(). Every 60 Hz, the MPPT_PowerAvgCalc() function is executed to calculate the average voltage and current values. The MPPT algorithm MPPT_INCC_F_FUNC() is executed at a frequency of 2 Hz, and the voltage reference value modified by MPPT_SoftStart() is passed to the control program Control_OpenloopCalc_Ongrid() located in *User_control.c*, which updates the current reference value through Control_PvVoltLoop().

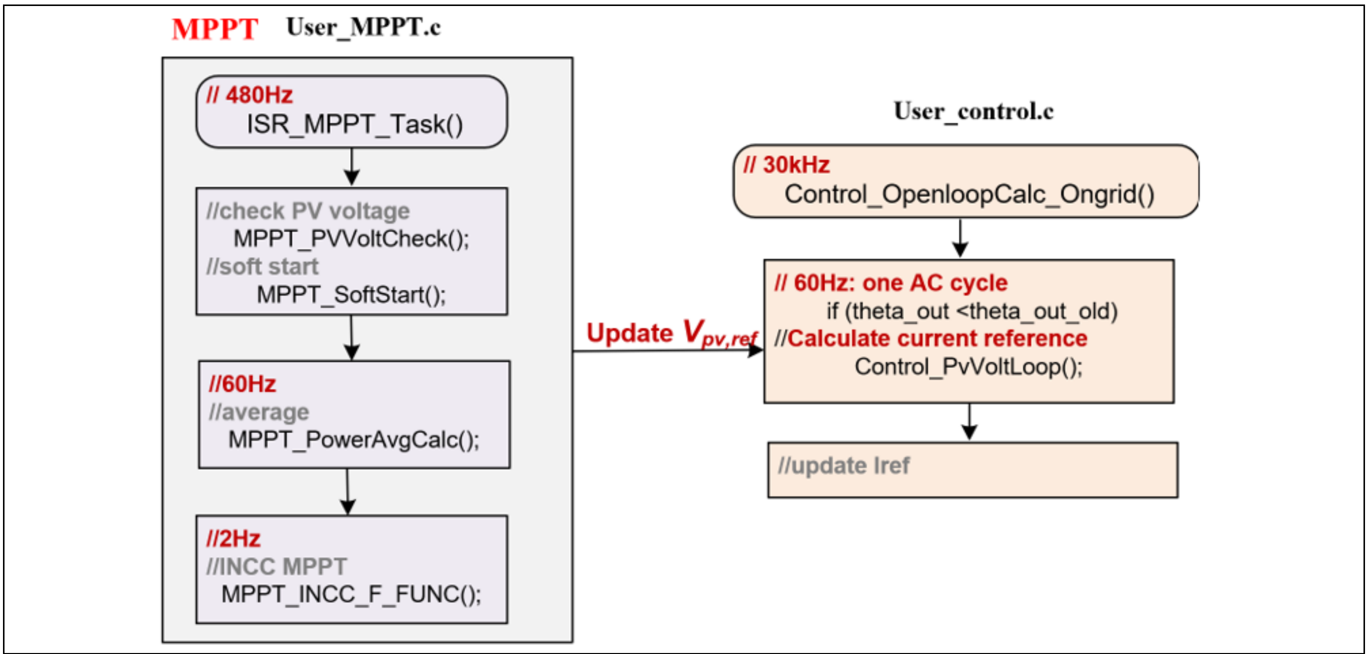


Figure 79 MPPT functions

5.8.5 Communication and command set

The UART function is configured in the program to realize the communication between the host computer and the converter. The flow diagram of the UART-related function and the program related to receiving commands is shown in the following figure. After receiving the command, UART_Interrupt_Callback() will take out the characters from the buffer, where @ is the command end identifier. After receiving a command, the function User_Uart_CommandProcess will be called in A1TASK_us() in the background function to process the received command.

The main command instructions and their related functions are shown in Table 10.

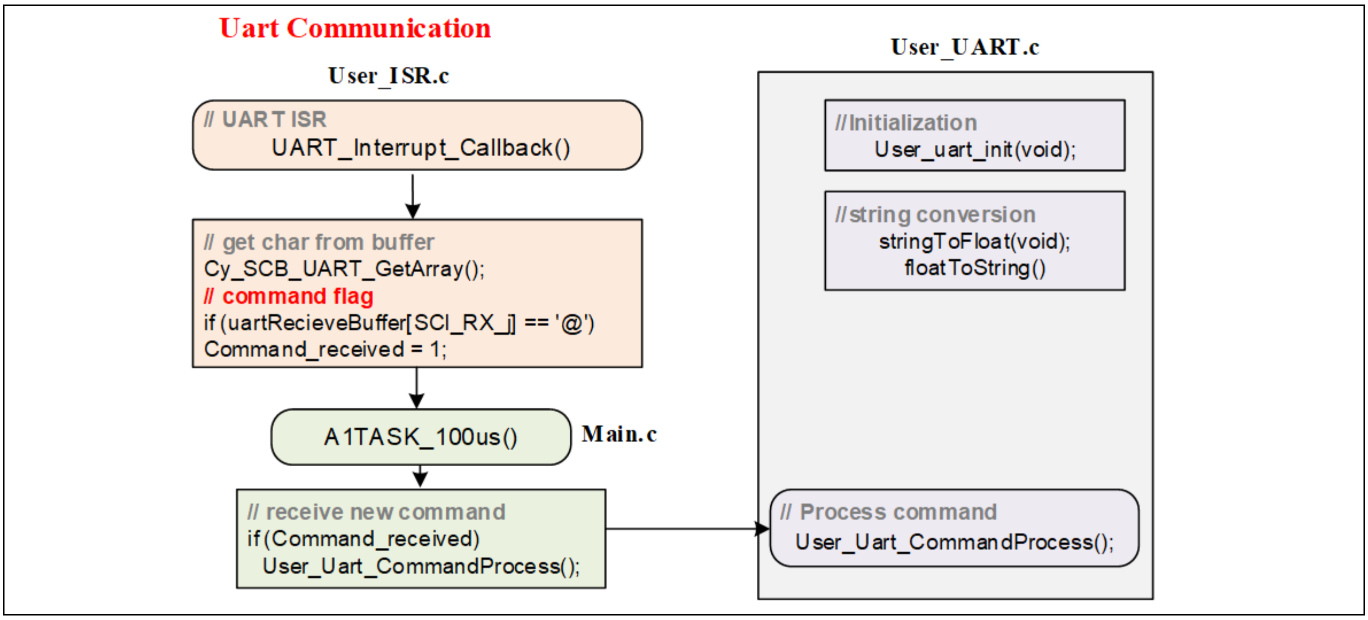


Figure 80 Communication functions

Table 10 System command set

No.	Command	Description
1	Grid_On@	Set the converter to grid-connected mode
2	Grid_Off@	Set the converter to off-grid mode
3	Start@	Start the converter
4	Stop@	Stop the converter
5	Reset@	Reset converter parameters
6	FaultClear@	Clear fault flag
7	VmoffX@	Set the off-grid output voltage amplitude to X. For example, Vmoff340@: Set the grid voltage amplitude to 340 V
8	ImonX@	Set the grid-connected output current amplitude to X. For example, Imon2.5@: Set the grid current amplitude to 2.5 A
9	PFonY@	Set the grid-connected power factor to Y. For example, PFon0.8@: Set the grid power factor to 0.8
10	BMEN@/ BMDS@	Enable/Disable Burst mode
11	MPPTEN@/ MPPTDIS@	Enable/Disable MPPT function

5.8.6 Protection

The protection logic framework in the program is shown in the following figure. The output current and transformer current are integrated with hardware detection protection circuits, and if their values exceed the normal range, they will trigger IO interrupts to set the corresponding fault flags high. The program also includes software protection, which evaluates ADC sampling values; if they exceed the normal range, the relevant fault flags will also be set high. Upon detecting hardware or software faults, the program will execute Fault_ShutDown() to shut down the inverter.

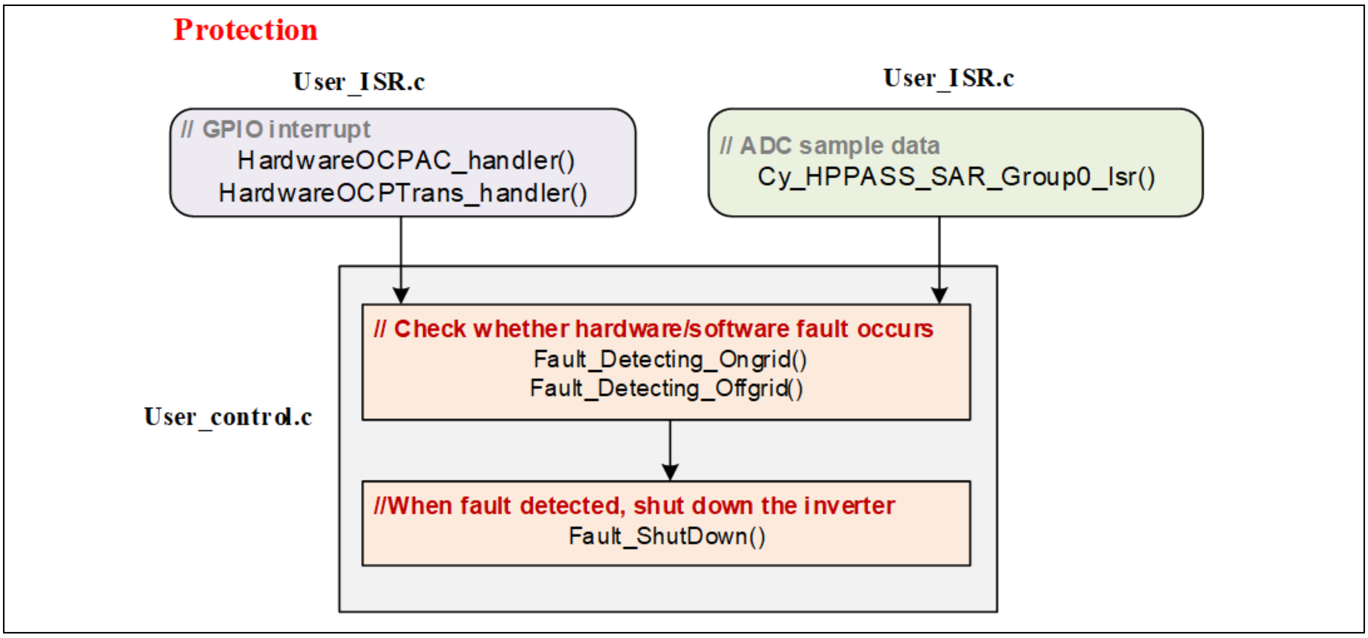


Figure 81 Protection functions

6 Test setup

6.1 Connections used for all tests

The REF_500W_CYCLO_BDSGAN board can be operated with a 24 V auxiliary power supply. This is recommended for initial tests and functionality checking where the unit may be operated from a very low DC input voltage (e.g., 5 V input with 30 V_{RMS} output setting).

For operation within the normal input range defined in Table 1, the 24 V supply is derived from the input via an on-board DC-DC converter. In this case the jumper JP1 should be connected between pins 2 and 3.

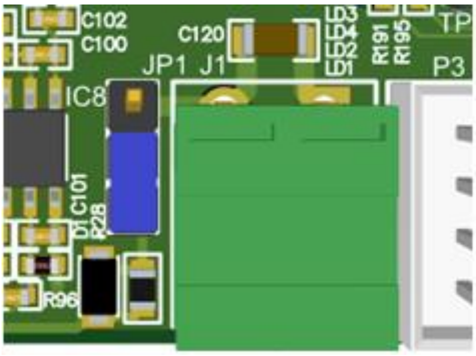


Figure 82 Operation with on-board 24 V auxiliary power

Attention: ***When carrying out efficiency measurements, the unit should be operated as described above and not with an external 24 V auxiliary supply.***

A power analyzer with a 64-sample averaging function was used for all efficiency measurements.

6.1.1 Auxiliary supply connections

A 24 V auxiliary power supply may be connected to J1 as shown in the following figure with positive at pin 2 and negative/GND at pin 1. Connection is made via a plug-in terminal block J1a. The jumper JP1 should be connected between pins 1 and 2 for auxiliary power operation and between pins 2 and 3 to operate directly from the main DC input.

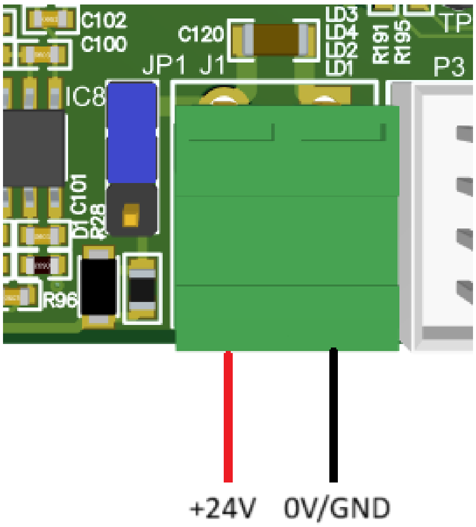


Figure 83 24 V auxiliary power connections and jumper setting

6.1.2 Connecting to the PC and GUI

The REF_500W_CYCLO_BDSGAN board requires the PC-based GUI for operation. This is connected via the UART1 port, which is connected to a PC via a serial interface. The serial interface may be tested with the auxiliary power supply connected before applying main DC (PV) input power or connecting to the AC outputs to the grid simulator. It is recommended to use an isolated USB/serial port adapter such as the Waveshare USB to RS485/RS232/TTL Converter shown here or a similar type.

Figure 84 Isolated USB serial interface

The TTL outputs RXD, TDX, and GND can be used to connect to P1 of the board via a suitable cable. The three required connections are; transmit data (TXD), receive date (RXD) and ground.

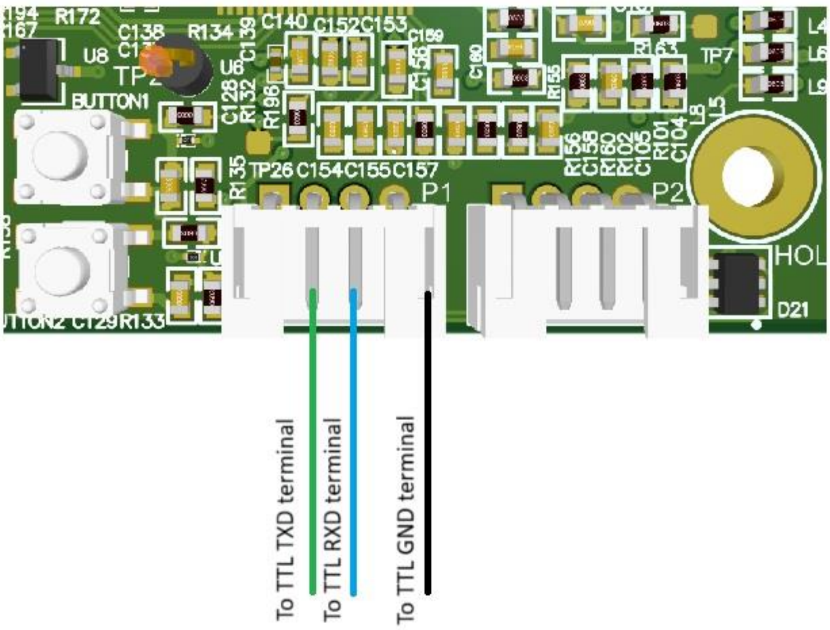


Figure 85 Serial port connections to the REF_500W_CYCLO_BDSGAN board

Note: It is recommended to test the serial interface with the GUI to verify correct operation, before proceeding further.

6.1.3 DC input supply connections

DC input power is connected to the terminals DC+ and DC-. For correct operation it is necessary to use a cable rated to carry 20 A or more with suitable ring or U terminals.

Figure 86 DC power connections

Additional sense leads are also attached to the terminals for voltage measurement.

6.2 Off-grid test setup

In off-grid mode, the cycloinverter produces a commanded constant voltage output. The output is connected to an AC electronic load, which is set to be purely resistive for testing at 100 W intervals from 100 to 500 W. Kelvin connections are required at the board terminals for accurate voltage measurement to allow accurate input and output power measurements required for efficiency calculations.

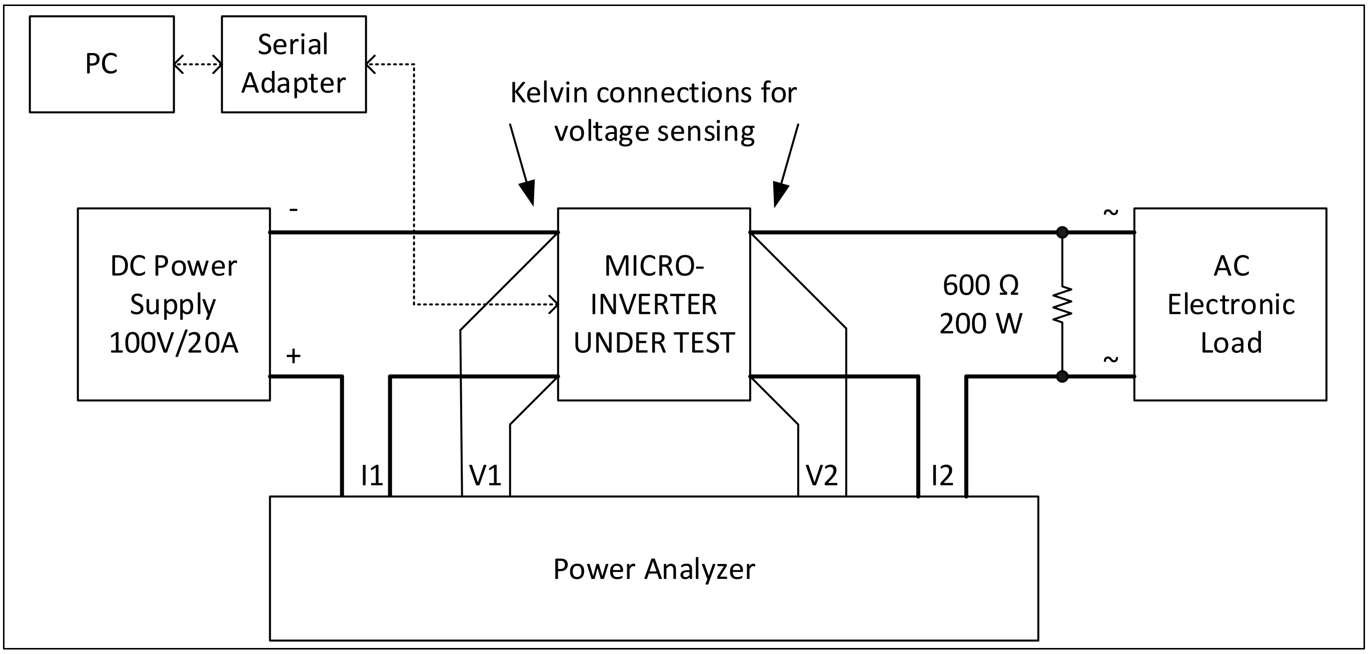


Figure 87 **Off-grid test setup**

A load 600 Ω resistor is used to provide a fixed load of approximately 100 W for a 240 V_{RMS} output. This resistor is rated at 200 W or more and is mounted to a heatsink. This resistor is necessary because the REF_500W_CYCLO_BDSGAN board requires a minimum load to operate and will shut down if operated with insufficient load. Additionally, the AC electronic load requires an AC voltage to be present before it is able to apply load. It may be necessary to disable the AC electronic load's automatic bandwidth adjustment (ABA) function in order to prevent it from shutting down when load is applied. The load is set to constant resistance mode with the following resistance settings used to provide power measurements at 100 W intervals:

Table 11 **AC electronic load settings for 240 VRMS constant resistance mode with 600 Ω external pre-loading resistor**

Target power (W)	Resistance setting (Ω)
100	Load OFF
200	554
300	282
400	189
500	143

6.3 On-grid test setup

For on-grid operation, the AC outputs from the board are connected to a grid simulator able to process AC power and transfer it safely back to the actual grid while enabling the voltage to be set to a defined level and frequency. On-grid operation can be in constant current or MPPT operating modes.

6.3.1 Grid simulator connections

The grid simulator is connected to the AC power terminals as follows:

Figure 88 AC power connections to the grid simulator

The AC cables should be rated for 300 V_{RMS} and at least 3 A_{RMS}. In Figure 88, two additional pairs of sensing cables have been added, one is for connection to the power analyzer and the other to connect to an HV differential oscilloscope probe.

The board with all connections is shown in the following figure with a current probe connected to measure the secondary side AC current coming from the transformer. A cable loop has been added to enable connection of the current probe, which may be replaced with a jumper between the two terminals of L2 if not required.

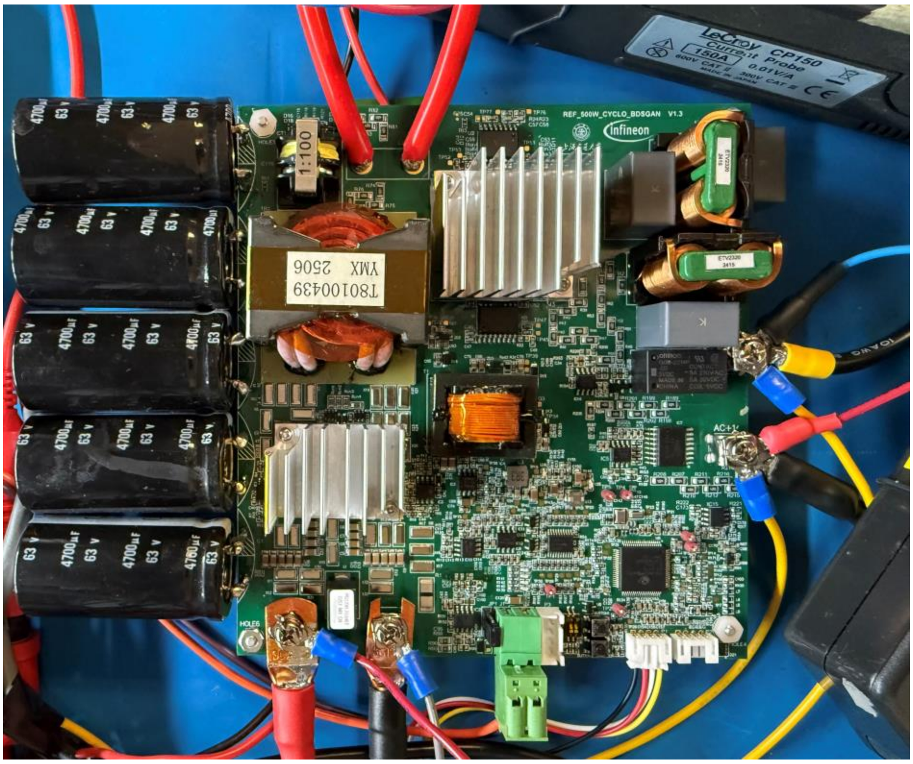


Figure 89 REF_500W_CYCLO_BDSGAN board with power and sensing connections

6.3.2 Constant output current mode

The default operating mode is a constant output current mode in which the AC RMS is set to a defined level via the PC-based GUI tool. The procedure is described in Section 7. The output voltage is determined by the grid voltage and the REF_500W_CYCLO_BDSGAN board operates as an AC current source to transfer the specified current onto the grid in a safe and stable manner. You can set the grid voltage and frequency via the grid simulator.

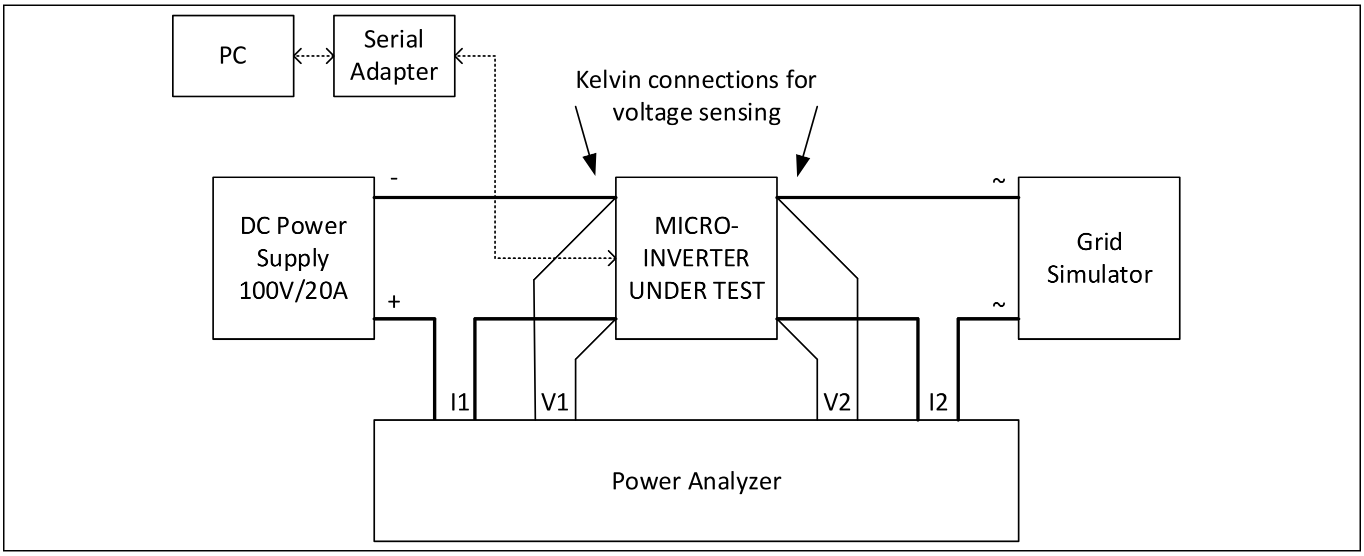


Figure 90 On-grid constant current mode test setup

6.3.3 MPPT mode

A PV emulator DC power source is required for operation in MPPT mode. These are typically operated with PC-based software that allows the user to set the desired maximum power point, which must be done in order for the REF_500W_CYCLO_BDSGAN board to operate correctly in MPPT mode.

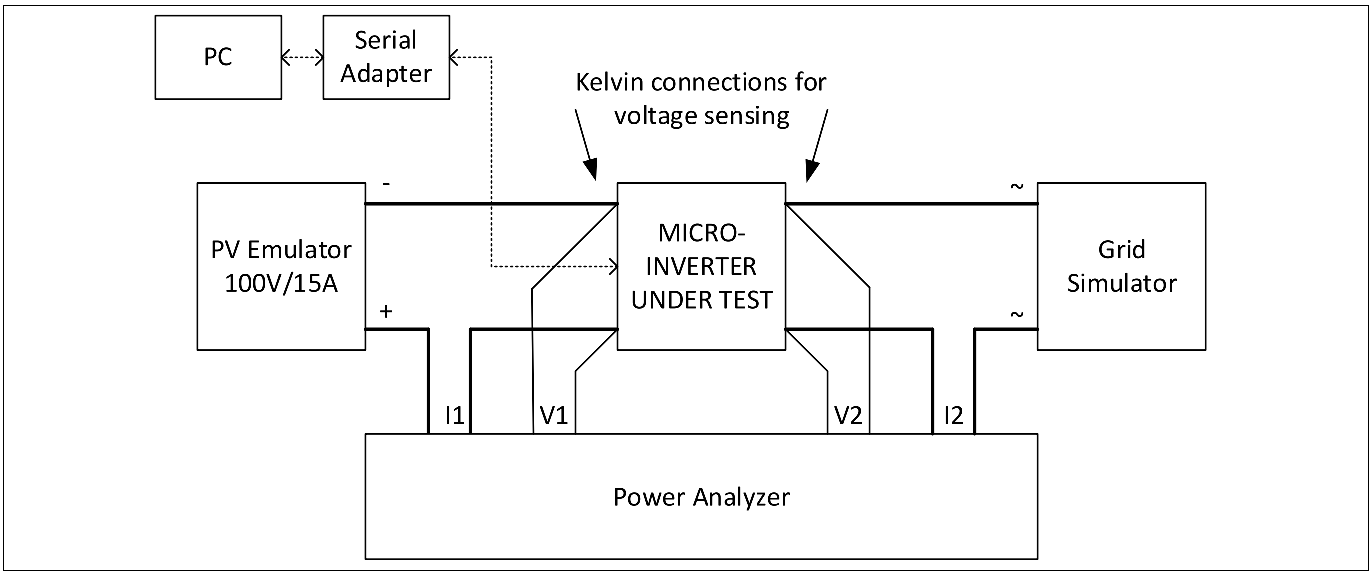


Figure 91 On grid MPPT mode test setup

The procedure will be explained in the following sections.

7 GUI tool and operation

The REF_500W_CYCLO_BDSGAN reference design board is operated via an ASCII-based operating system with a defined command set defined in Table 10. A PC-based tool is available from Infineon, which provides a user-friendly GUI for easy operation (refer to Section 3.1.2). Usage of the GUI is described in this section.

7.1.1 Basic functions

First install the GUI tool onto a PC and connect the PC to an isolated USB to serial port adapter as described in Section 6.1. Ensure the serial port adapter is shown in the Windows device drivers and note operating correctly, note the COM port. Select the COM port in the GUI tool and click the **CONNECT/DISCONNECT** button and check the "Port Connected" status is indicated:

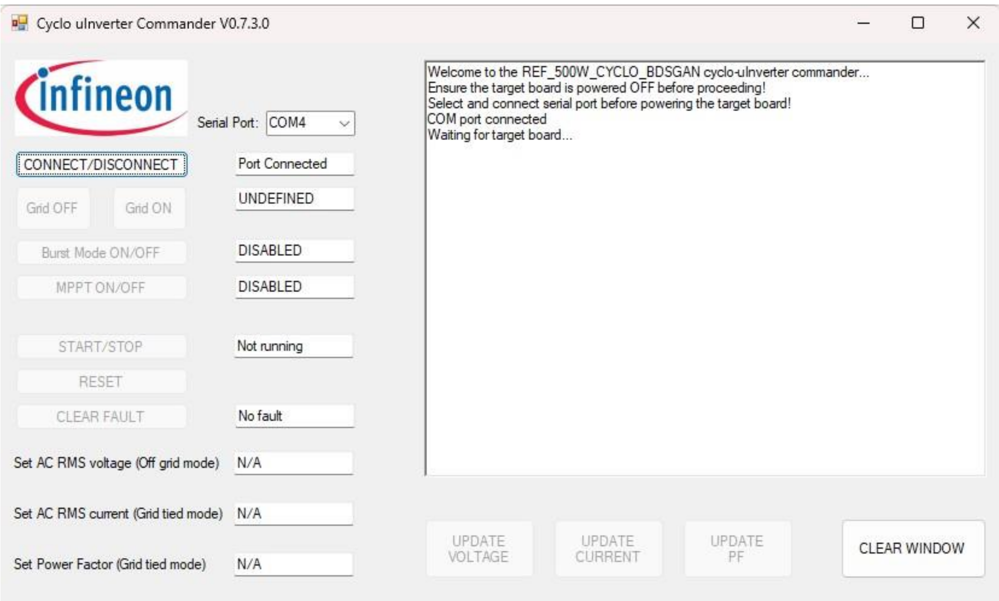


Figure 92 Setting the COM port

Connect the serial port adapter to the target board with the auxiliary power supply as shown in Section 6.1. Then switch on the auxiliary power supply and observe the GUI detection of the target board as shown in the following figure. The grid OFF and grid ON buttons will become enabled once the target board has been detected.

Observe that all ASCII messages transmitted from the GUI to the target board are displayed in the main GUI text window preceded by "TX:" and all text received from the target board is also displayed, which is preceded by "RX:" except for the start message shown below. The target board startup message contains three lines of text followed by "Target board detected!", which is indicated by the GUI when the preceding three lines have been received.

Attention: ***The REF_500W_CYCLO_BDSGAN board will not operate in off-grid mode and the relay will remain open if the unit is connected to an AC source such as a grid simulator if AC voltage is detected at the output terminals. Any attempt to apply AC voltage to the output terminals while operating on off-grid mode could damage the unit.***

The board will shut down immediately in startup in off-grid mode unless a passive load of at least 50 W is present at the output terminals.

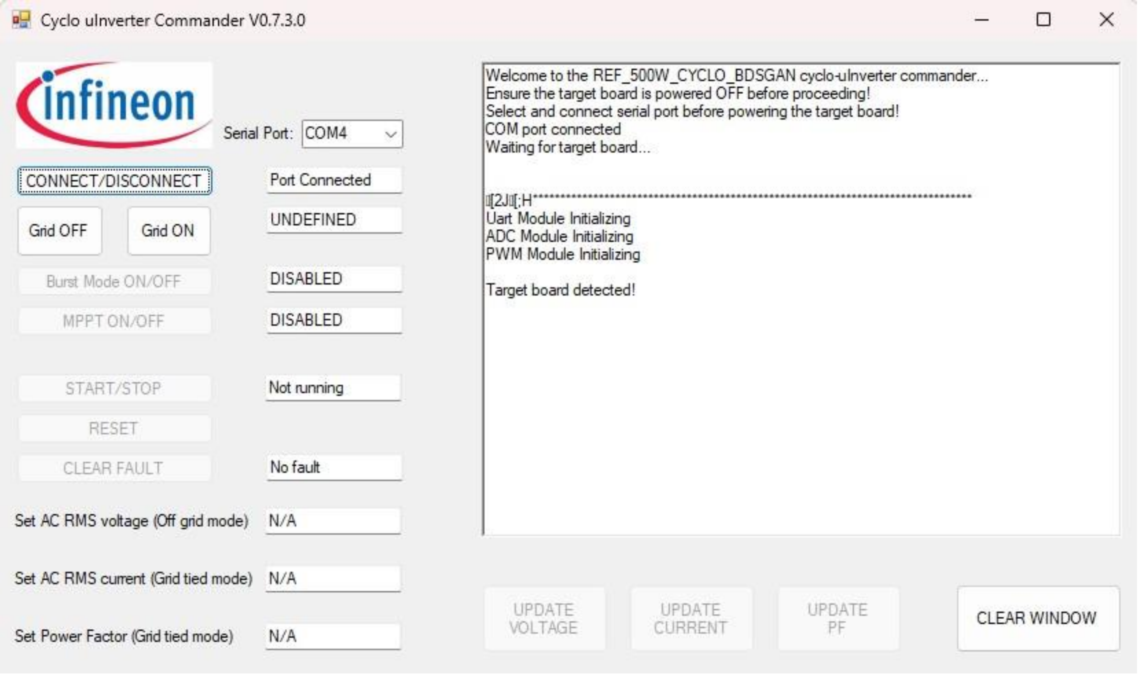


Figure 93 Target board detection

7.1.2 Off-grid operation

1. To operate the system in off-grid mode, click on the **Grid OFF** button and observe the grid mode status The grid **OFF** and **ON** buttons become disabled and the **UPDATE VOLTAGE** button becomes active
2. Ensure the main DC power is connected to the board with the appropriate voltage and current settings
3. Enter the required RMS output voltage in the **Set AC RMS voltage** box and then click on **UPDATE VOLTAGE** to send the voltage command to the target board
4. Click the **START/STOP** button to start the cycloinverter

Note: A 50 W minimum load must be connected to operate in off-grid mode otherwise the unit will shut down.

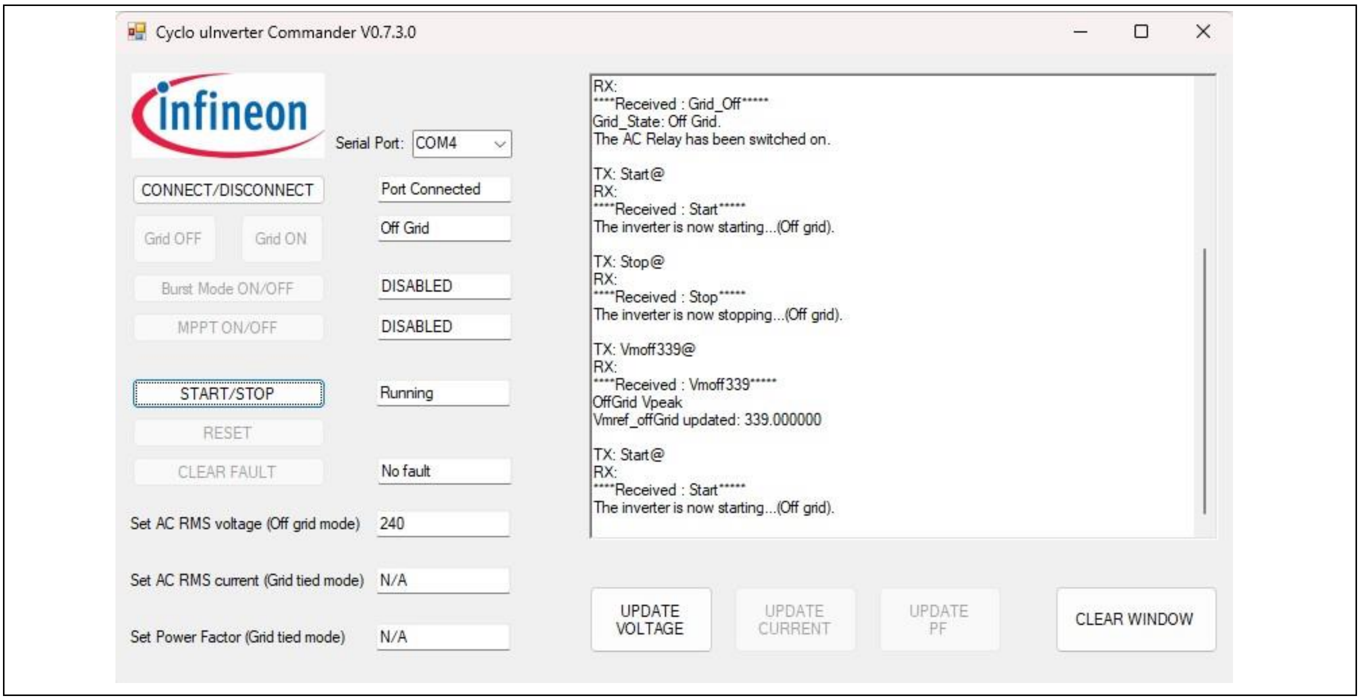


Figure 94 **Off-grid operation**

Note: *The GUI converts the RMS voltage to a peak voltage before sending the command as required by the target board firmware.*

5. To stop the inverter, click on the **START/STOP** button again.

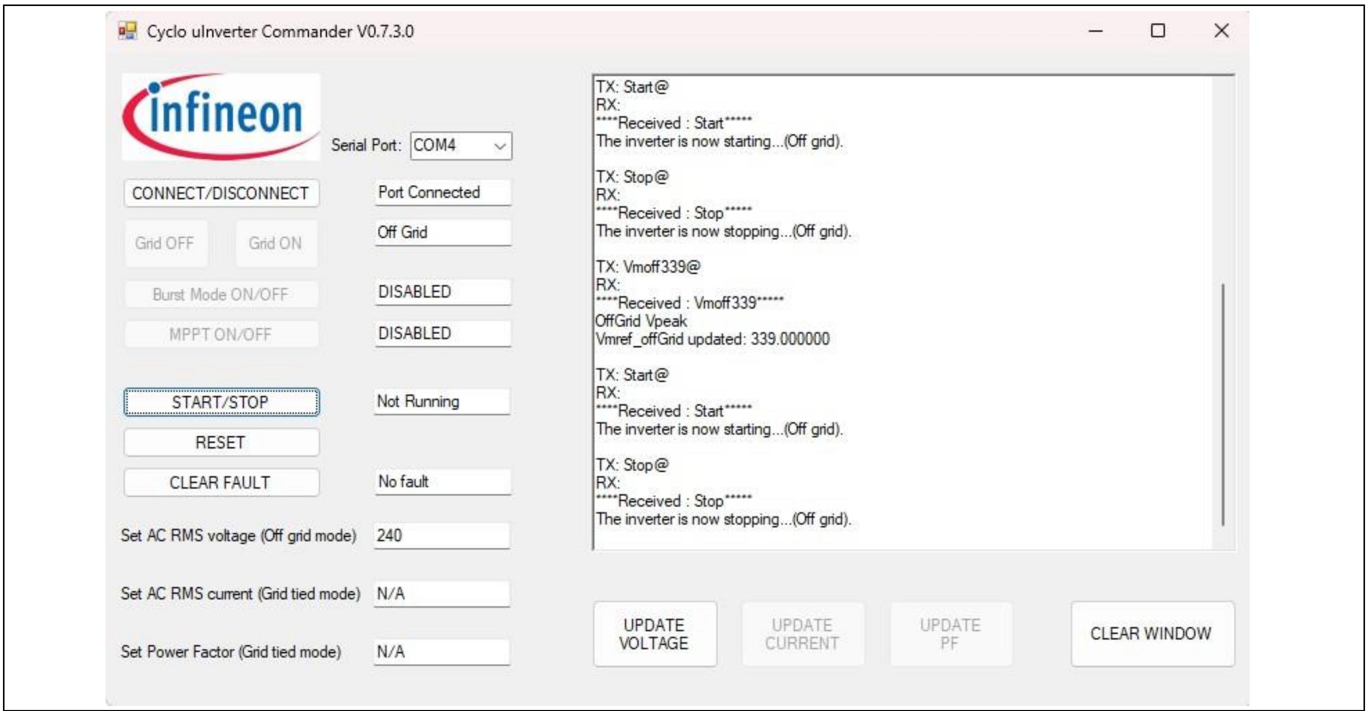


Figure 95 **Inverter stopped operation in off-grid mode**

In the event of an error causing the target board to stop running, an error message will appear in the main window and a fault status will be indicated. Click **FAULT CLEAR** button followed by the **RESET** button to return the target board to initial grid selection mode. In some cases, it may be necessary to power down and restart the target board.

7.1.3 On-grid (grid-tied) constant current operation

To operate in grid-tied mode, select the **Grid ON** button and observe the grid mode status. The grid **OFF** and **ON** buttons should then become disabled and the **UPDATE CURRENT** and **UPDATE PF** buttons become active. The REF_500W_CYCLO_BDSGAN board will attempt frequency and phase lock to the AC grid voltage. If this is not successfully completed within 10 seconds, the unit will reset to the mode selection state. For this reason, the grid simulator output should be enabled before selecting grid **ON** mode.

Ensure the main DC power is connected to the board with the appropriate voltage and current settings. The next step is to enter the required RMS output current in the **Set AC RMS current** box and then click on **UPDATE CURRENT** to send the current command to the target board. Click the **START/STOP** button to start the cyclonverter.

Note that the GUI converts the RMS current to a peak current before sending the command as required by the target board firmware.

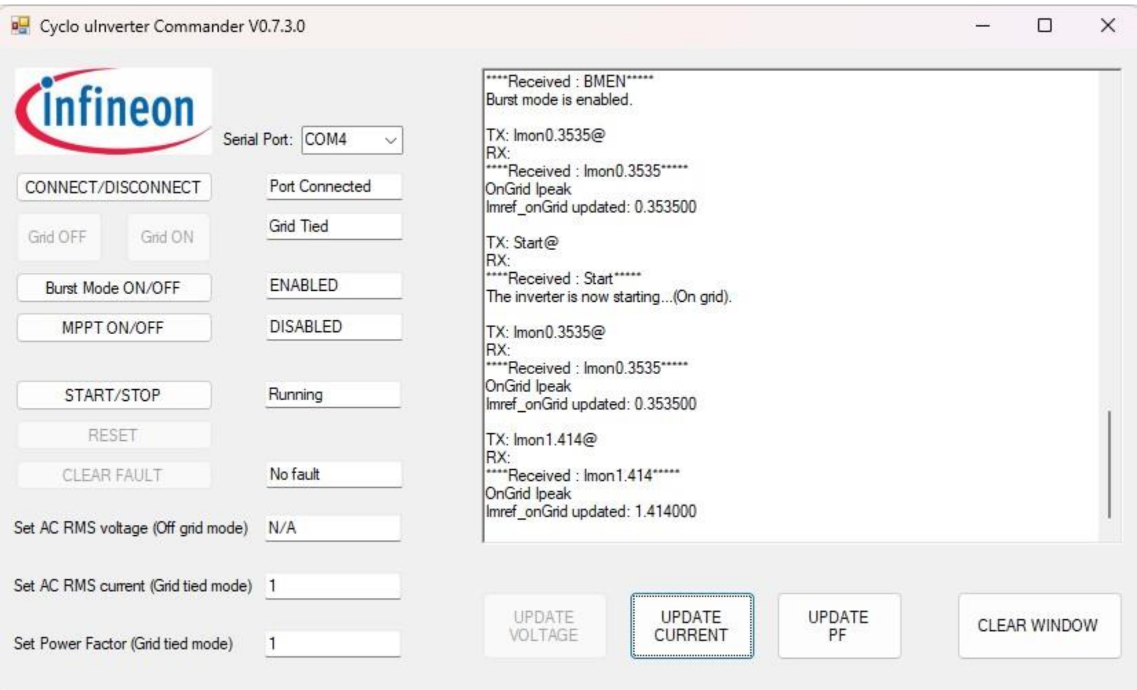


Figure 96 **Setting the output current for grid-tied operation**

The power factor may also be changed while operating in this mode. This is done by entering a power factor between in the range -0.8 to 1.0 to 0.8 in the set power factor box and click on **UPDATE PF**.

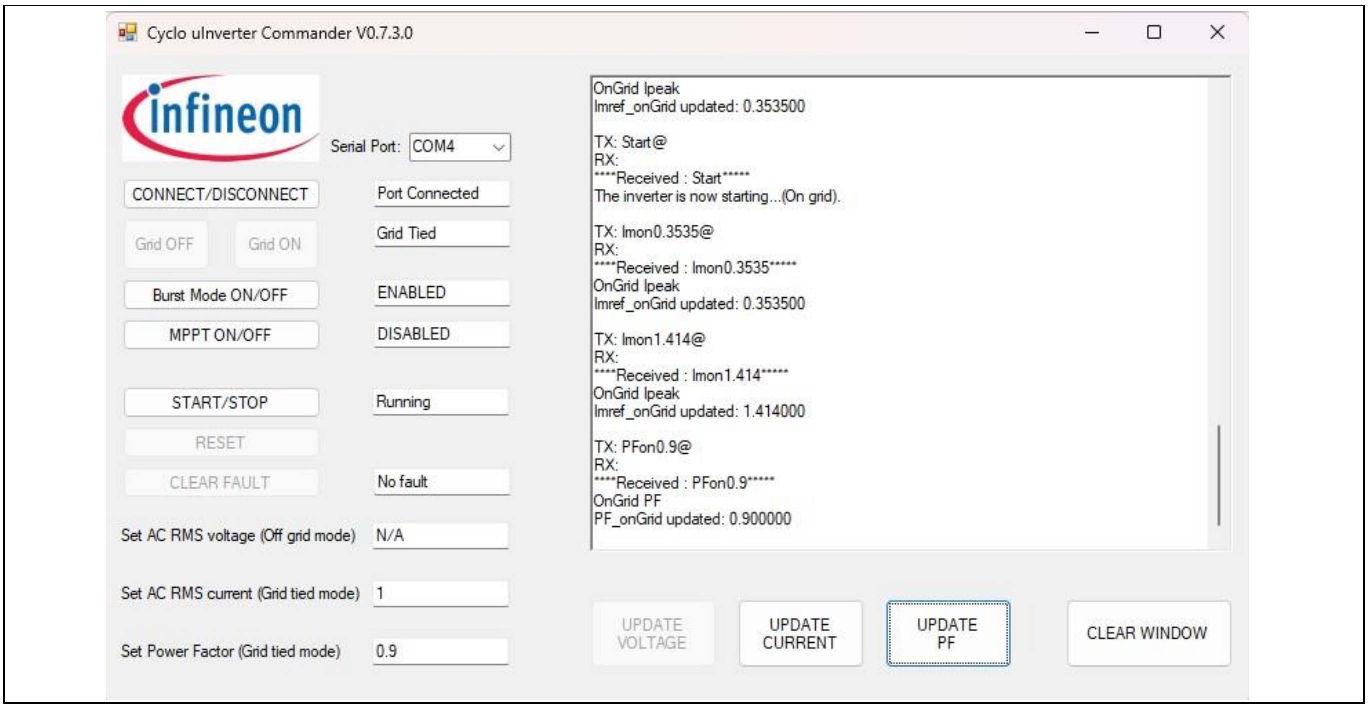


Figure 97 **Changing the power factor**

Burst mode, required to achieve light load efficiency, is inactive by default and can be enabled only when the power factor is set to unity (1.0). This is done by clicking the Burst Mode **ON/OFF** button and observing the bust mode status box. Burst mode may be enabled and disabled during operation.

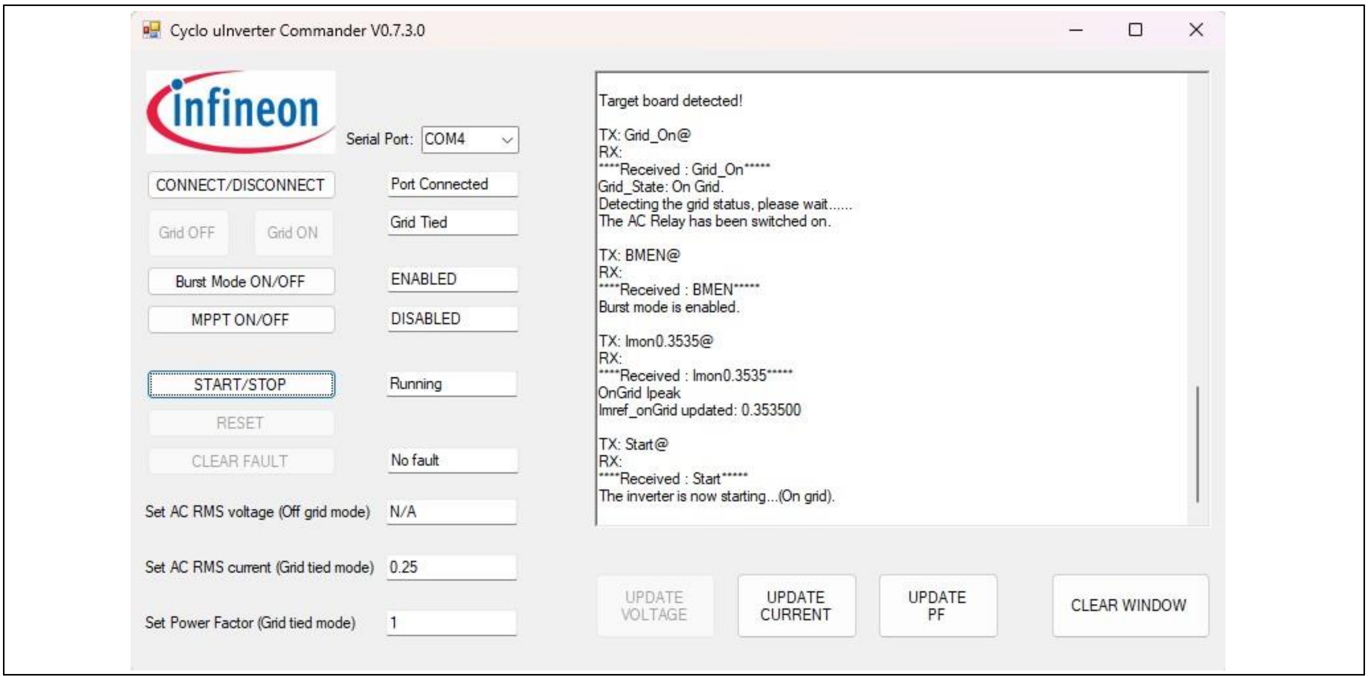


Figure 98 **Burst mode operation in on-grid mode**

The inverter is stopped by clicking the **START/STOP** button.

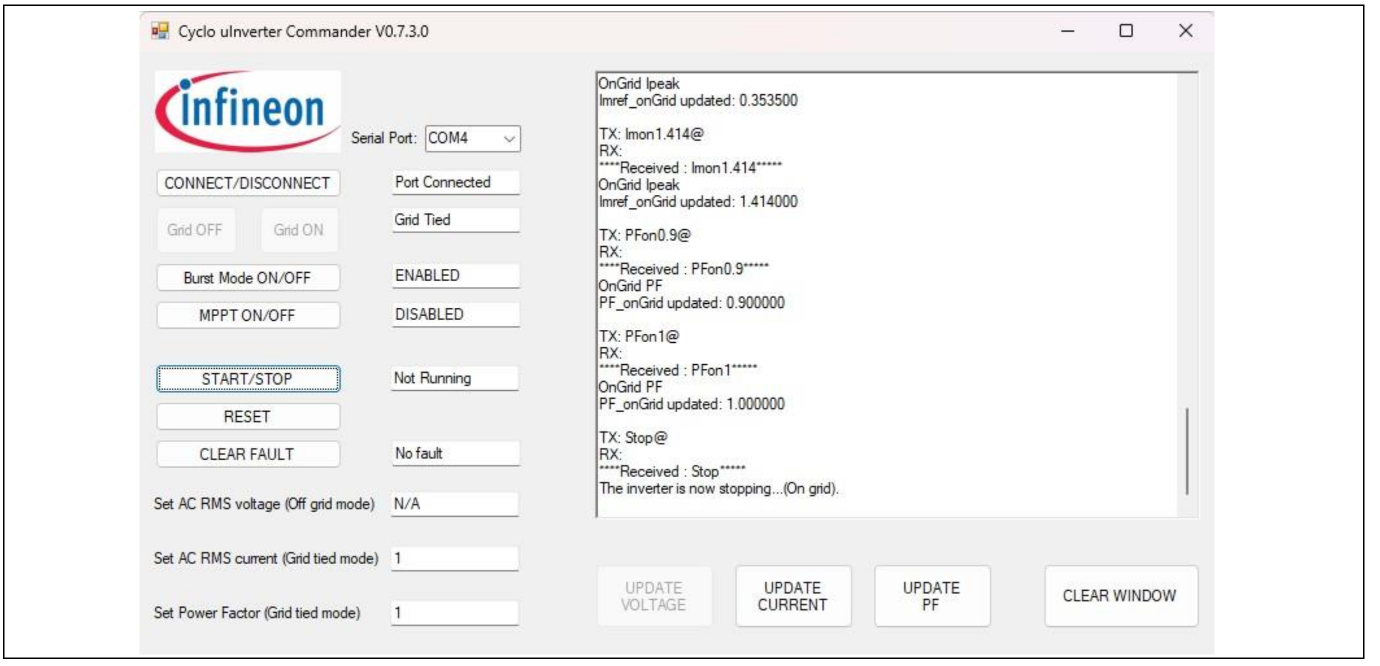


Figure 99 Inverter stopped operation in on-grid mode

MPPT operation is described in Section 11.1.3.

8 Bill of materials

8.1 Electrolytic capacitor board

Reference	Qty	Type	Value/rating	Manufacturer	Part number
C1, C2, C3, C4, C119	5	Capacitor	4.7 mF / 63 V / 20% / Aluminum electrolytic / D25 mm / L52 mm/ P10mm / Radial	Nichicon	LGY1J472MELA50
PCB	1	PCB	E-Caps / V1.0/ FR4 / 2 layers of 2oz. Cu / Green		

8.2 Main power board

Reference	Qty	Type	Value/rating	Manufacturer	Part number
AC-1, AC+1, DC-, DC+	4	Connector	0° (vertical) / Board-to-Cable	XFCN	T44008
BUTTON1, BUTTON2	2	Electro Mechanic	SWITCH TACTILE / SPST-NO / 0.05A / 12V	C&K	PTS647SM38SMTR 2LFS
C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22	18	Capacitor	2.2 uF / 100 V / 10% / X7R (EIA) / 1206 (3216)	Kyocera	12061C225KAT2A
C23, C24, C25, C26	4	Capacitor	1 nF / 100 V / 5% / COG-NPO / 0603 (1608)	MuRata	GRM1885C2A102JA 01D
C27	0	Capacitor	DO NOT POPULATE		
C88, C99, C100, C168	0	Capacitor	DO NOT POPULATE		
C30, C34, C82, C84, C85, C87, C89, C90, C92, C93, C95, C97, C101, C102, C108, C110, C114, C115, C169, C170	20	Capacitor	1 nF / 25 V / 5% / X7R (EIA) / 0603 (1608)	Yageo	CC0603JRX7R8BB1 02
C28, C29, C32, C33	4	Capacitor	15 nF / 1 kV / 5% / C0G (EIA) / NP0 / 1812 (4532)	Kemet	CKC18X153JDGACA UTO
C31, C49, C54, C66, C73, C77, C80, C81, C83, C86, C91, C94, C96, C103, C104, C105, C106, C109, C111,	40	Capacitor	100 nF / 25 V / 5% / X7R (EIA) / 0603 (1608)	Yageo	CC0603JRX7R8BB1 04

Reference	Qty	Type	Value/rating	Manufacturer	Part number
C113, C116, C123, C124, C149, C151, C152, C153, C154, C155, C156, C157, C158, C159, C162, C163, C164, C165, C166, C167, C171					
C125, C130, C133, C135, C137, C139, C141	7	Capacitor	100 nF / 25 V / 10% / X7R (EIA) / 0402 (1005)	Samsung	CL05B104KA5NNNC
C35, C36, C37	3	Capacitor	470 nF / 630 V / 10% / MKP (Metallized Polypropylene) / THT/Radial	Kemet	F862BY474K310ZV054
C38, C42, C132	3	Capacitor	4.7 uF / 25 V / 10% / X6S (EIA) / 0603 (1608)	MuRata	GRT188C81E475KE13D
C39, C43, C48, C50, C51, C52, C53, C55, C56, C59, C121, C122, C126, C127	14	Capacitor	1 uF / 25 V / 20% / X7R (EIA) / 0603 (1608)	TDK Corporation	C1608X7R1E105M080AB
C40, C41, C44, C45, C46, C47, C57, C58, C117, C160, C161	11	Capacitor	100pF / 25 V / 5% / C0G (EIA) / NP0 / 0603 (1608)	AVX	06033A101JAT2A
C60, C62, C63, C65, C68, C75	6	Capacitor	2.2 uF / 25 V / 20% / X7R (EIA) / 0805 (2012)	Kemet	C0805C225M3RACTU
C61, C64, C70, C78	4	Capacitor	10 uF / 25 V / 10% / X7S (EIA) / 0805 (2012)	MuRata	GRM21BC71E106KE11L
C67	1	Capacitor	47 pF / 100 V / 5% / C0G (EIA) / NP0 / 0603 (1608)	Kemet	C0603C470J1GACTU
C69, C120	2	Capacitor	4.7 uF / 100 V / 20% / X7R (EIA) / 1206 (3216)	MuRata	GRM31CZ72A475ME11K
C71, C72, C79	3	Capacitor	22 uF / 25 V / 20% / X5R (EIA) / 1206 (3216)	MuRata	GRM31CR61E226ME15
C74	1	Capacitor	100 nF / 100 V / 10% / X7R (EIA) / 0603 (1608)	Wurth Elektronik	885012206120
C76	1	Capacitor	33 pF / 50 V / 5% / C0G (EIA) / NP0 / 0603 (1608)	TDK Corporation	CGA3E2NP01H330J080AA
C98, C107, C112, C131, C134,	9	Capacitor	10 uF / 25 V / 20% / X5R (EIA) / 0603 (1608)	TDK Corporation	C1608X5R1E106M080AC

Reference	Qty	Type	Value/rating	Manufacturer	Part number
C136, C138, C140, C142					
C118	1	Capacitor	4.7 nF / 25 V / 5% / X7R (EIA) / 0603 (1608)	Yageo	CC0603JRX7R8BB472
C128, C129	2	Capacitor	10 nF / 50 V / 10% / X7R (EIA) / 0603 (1608)	Kemet	C0603C103K5RECAUTO
C143, C144	2	Capacitor	18 pF / 50 V / 2% / C0G (EIA) / NP0 / 0402 (1005)	MuRata	GCM1555C1H180GA16
C145	1	Capacitor	56 pF / 25 V / 2% / C0G (EIA) / NP0 / 0603 (1608)	MuRata	CC0603GRNPO9BN560
C146, C147	2	Capacitor	15 pF / 25 V / 5% / C0G (EIA) / NP0 / 0402 (1005)		0402N150J250CT
C148	1	Capacitor	47 uF / 10 V / 10% / X5R (EIA) / 1206 (3216)	MuRata	GRM31CR61A476KE15
C150	1	Capacitor	22 uF / 25 V / 20% / X7S (EIA) / 1206 (3216)	MuRata	GRM31CC71E226ME15L
C172, C173	2	Capacitor	2 pF / 50 V / 500 fF / X8G (Murata) / 0603 (1608)	MuRata	GCM1885G1H2R0DA16
Cc1, Cc2, Cc3, Cc4	4	Capacitor	1.5 nF / 25 V / 10% / X7R (EIA) / 0603 (1608)	MuRata	GCJ188R71E152KA01D
CT1	1	Transformer	1:100 / 50 A / DIP / Current Sense Transformers	FANGCHENG ELECTRON	FC-SCT1090-100T-50A
D1, D13, D14, D15	4	Diode	Schottky diode / PowerDI123	Diodes Incorporated	DFLS1100-7
D2, D3, D4, D20	4	Diode	Schottky diode / SOD-323F (SC-90)	Nexperia	BAT46WJ,115
D5, D6, D7, D8, D9, D10, D11, D12, D16, D17, D18, D19	12	Diode	Schottky diode / SC-79	Infineon Technologies	BAS3005A-02V
D21	1	Diode	TVS Diode / SOT-23-6	STMicroelectronics	USBLC6-4SC6
D22	1	Diode	Standard Diode / SOD-123	Diodes Incorporated	1N4148W-7-F
F1	1	Resistor	5A / 300V / THT / Radial	Littelfuse	36915000000
J1	1	Connector	TERM BLOCK HDR / 2POS / 5.08 mm	Würth Elektronik	691313510002
J1a	1	Connector	TERM BLOCK / PLUG / 2POS / 5.08 mm	Würth Elektronik	691351500002
JP1	1	Connector	Header / 2.54 mm / 3-pin / vertical	Amphenol ICC (FCI)	68001-203HLF

Reference	Qty	Type	Value/rating	Manufacturer	Part number
P1, P2	2	Connector	1x4P PH 4P Tin / -25°C~+85°C / 2 A / 2mm Brass Right-Angle Push-Pull	SHOU HAN	2.0-4P WZ-D
P3	1	Connector	1x4P / Vertical / 2.54 mm / shrouded / white	JST Sales America Inc.	B4B-XH-A
X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16, X17, X18, X19, X20, X21, X22, X23, X24, X25, X26, X27, X28, X29, X30, X31, X32, X33, X34, X35, X36, X37	37	Connector	H62 Brass / 5x2x0.6 mm Metal Products / SMT / Copper Sheet	STEIPU	STHW4-DU-HN050206
IC1, IC2	2	Integrated Circuit	Half-Bridge Gate Driver IC Non-Inverting / 8-VSON (4x4)	Texas Instruments	UCC27211AD
IC3	1	Integrated Circuit	4.2-V to 80-V, 2-A, synchronous buck with 40-µA IQ / HSOIC-8	Texas Instruments	PLMR38020FDDAR
IC4	1	Integrated Circuit	3-V to 17-V Input, 2-A, Synchronous Buck Converters / SOT-563	Texas Instruments	TPS562242DRLR
IC5, IC8, IC14, IC15	4	Integrated Circuit	CMOS Amplifier / 2 Circuit / Rail-to-Rail / 8-SOIC	Texas Instruments	OPA2350UA
IC6	1	Integrated Circuit	Buffer / Non-Inverting / 2 Element / 4 Bit per Element / 3-State Output / 20-TSSOP	Texas Instruments	SN74AHCT244PWR

Reference	Qty	Type	Value/rating	Manufacturer	Part number
IC7	1	Integrated Circuit	-5 A~5 A SOP-16-W Current Sensors ROHS	CrossChip Microsystems .Inc.	CC6921SO-5A
IC9, IC10	2	Integrated Circuit	Dual comparator / SOIC-8	Texas Instruments	LM2903D
IC11, IC12	2	Integrated Circuit	Buffer / Non-Inverting / 1 Element / 1 Bit per Element / 3-State Output / SOT-23-5	Texas Instruments	SN74AHCT1G125DBVR
IC13	1	Integrated Circuit	3-V to 16-V input voltage / 4-A FCCM mode / synchronous buck converter / SOT-563 package	Texas Instruments	TPS564247DRLR
K1	1	Electro Mechanic	General Purpose Relay / DPST-NO (2 Form A) / 5VDC Coil / Through Hole	Omron	G6B-2214P-US DC5
L1	1	Inductor	320 nH / Standard / SMD	Pulse Electronics	PG2290.321HLT
L2	1	Inductor	68 uH / Standard / SMD	Coilcraft	MSS1210-683MED
L3	1	Inductor	3.3 uH / Standard / SMD	TDK Corporation	SPM5030T-3R3M

Reference	Qty	Type	Value/rating	Manufacturer	Part number
L4, L5, L6, L7, L8, L9, L12	7	Inductor	220R / Ferrite Bead / 0603 (1608)	Wurth Elektronik	742863122
L10, L11	2	Inductor	1kR / Ferrite Bead / 0603 (1608)	MuRata	BLM18KG102SN1D
L13	1	Inductor	1.5 µH Shielded Drum Core / 3.6 A / 25.63mOhm Max / Nonstandard	TDK Corporation	SPM4030T-1R5M-HZ
LD1, LD2, LD3, LD4	4	Diode	CHIP LED / GREEN / 573NM / 45MCD / 0603	Wurth Elektronik	150060GS75000
LD5, LD6	2	Diode	CHIP LED / RED / 623NM / 180MCD / 0603	OSRAM Opto Semiconductors	LR Q976.01-P2R2-1
Lf1, Lf2	2	Inductor	4 mH / Custom / THT	Shenzhen Yamaxi Technology Co	TBD
Q	1	Integrated Circuit	VREF SHUNT ADJ / 0.5% / SOT23	Diodes Incorporated	AZ431LANTR-G1
Q1, Q2, Q3, Q4	4	Transistor FET	N-Channel Enhancement / 279A / 80V / PG-TSON-8-3	Infineon Technologies	ISC014N08NM6

Reference	Qty	Type	Value/rating	Manufacturer	Part number
Q5, Q6	2	Transistor FET	N-Channel Enhancement / 88A / 80V / PG-TSON-8-3	Infineon Technologies	ISC056N08NM6
Q7, Q8	2	Transistor FET	N-Channel Enhancement bidirectional / 600 V / GaN G5 / HDSOP-16	Infineon Technologies	IGLT65R055B2
Q9	1	Transistor FET	N-Channel Enhancement / 500 mW / 1.4 A / 30 V / PG-SOT23-3-5	Infineon Technologies	BSS316N H6327
R1	1	Resistor	500 uR / 1% / 3 / 2512 (6432)	Yageo	PA2512FKF7T0U5E
R2, R3	2	Resistor	5.1R / 5% / 0.33 / 1206 (3216)	KOA Speer Electronics Inc.	SG73P2BTTD5R1J
R4, R8, R12, R16, R125, R127, Roff1, Roff2, Roff3, Roff4	10	Resistor	2R / 0.1% / 0.063 / 0603 (1608)	TE Connectivity	CPF0603B2R0E1
R5, R9, R13, R17, R124, R126	6	Resistor	5.1R / 1% / 0.1 / 0603 (1608)	Vishay	CRCW06035R10FK
R6, R11, R14, R19, R26, R27, R31, R32, R48, R54, R56, R58, R59, R65, R70, R72, R73, R80, R106, R108, R114, R129, R131, R132, R157, R158,	49	Resistor	10k / 1% / 0.125 / 0603 (1608)	Stackpole Electronics	RNCP0603FTD10K0

Reference	Qty	Type	Value/rating	Manufacturer	Part number
R159, R166, R167, R172, R173, R174, R175, R176, R177, R178, R179, R180, R181, R182, R183, R184, R186, R191, R193, R195, R197, R221, R222					
R7, R10, R15, R18, R20, R21, R23, R24, R45, R107, R116, R121, R134, R151, R152, R153, R154, R155, R156, R160, R161, R162, R163, R164, R165, R168, R169, R170, R171, R217, R218	31	Resistor	100R / 1% / 0.1 / 0603 (1608)	ROHM Semiconductors	MCR03EZPFX1000
R22, R25	2	Resistor	DO NOT POPULATE		
R28	1	Resistor	DO NOT POPULATE		
R29, R133, R147	3	Resistor	100k / 1% / 0.1 / 0603 (1608)	Panasonic	ERJ-3EKF1003V
R30, R33, R35	3	Resistor	110k / 1% / 0.1 / 0603 (1608)	Vishay	CRCW0603110KFK

Reference	Qty	Type	Value/rating	Manufacturer	Part number
R34	1	Resistor	105k / 1% / 0.1 / 0603 (1608)	Vishay	CRCW0603105KFK
R36, R79, R86	3	Resistor	20k / 1% / 0.1 / 0603 (1608)	Vishay	CRCW060320K0FK
R37, R88, R96	3	Resistor	22k / 1% / 0.1 / 0603 (1608)	Vishay	CRCW060322K0FK
R38, R39, R40, R41, R42, R43, R46, R47, R49, R50, R51, R52, R53, R60, R61, R62, R74, R75, R76, R77, R81, R82, R83, R84, R189, R198, R199, R200, R201, R202, R204, R205, R207, R208, R210, R211, R212, R214, R215, R216	40	Resistor	1MEG / 1% / 0.25 / 1206 (3216)	Vishay	CRCW12061M00FK
R44, R55, R203, R213	4	Resistor	25k / 0.1% / 0.15 / 0603 (1608)	Vishay	PNM0603E2502BST 1
R57, R63, R64, R66, R67, R68, R69, R71, R99, R128, R130, R187, R188, R190, R192, R194, R196, R206, R209	19	Resistor	0R / 0603 (1608)	KOA Speer Electronics Inc.	RK73Z1JTTD

Reference	Qty	Type	Value/rating	Manufacturer	Part number
R136, R137, R144, R145	4	Resistor	0R / 0402 (1005)	KOA Speer Electronics Inc.	RK73Z1ETTP
R98	0	Resistor	DO NOT POPULATE		
R87, R110, R135	3	Resistor	1k / 1% / 0.1 / 0603 (1608)	Panasonic	ERJ3EKF1001V
R219, R220	2	Resistor	DO NOT POPULATE		
R89	1	Resistor	2.05k / 1% / 0.1 / 0603 (1608)	Vishay	CRCW06032K05FK
R90, R93	2	Resistor	510k / 1% / 0.125 / 0805 (2012)	Vishay	CRCW0805510KFK
R91, R97	2	Resistor	39k / 1% / 0.1 / 0603 (1608)	Vishay	CRCW060339K0FK
R92, R95	2	Resistor	200R / 1% / 0.1 / 0603 (1608)	Vishay	CRCW0603200RFK

Reference	Qty	Type	Value/rating	Manufacturer	Part number
R94	1	Resistor	6.2k / 1% / 0.1 / 0603 (1608)	Vishay	CRCW06036K20FK
R138, R143, R146	3	Resistor	4.7k / 1% / 0.25 / 0603 (1608)	Vishay	CRCW06034K70FKE AHP
R139, R140, R141, R142, R146	5	Resistor	2k / 1% / 0.1 / 0603 (1608	Vishay	CRCW06032K00FKE A
R103, R109, R113, R120	4	Resistor	200k / 1% / 0.1 / 0603 (1608)	Yageo	RC0603FR-07200KL
R104	1	Resistor	12k / 1% / 0.1 / 0603 (1608)	Stackpole Electronics	RMCF0603FT12K0
R105, R111, R112, R115, R117	5	Resistor	2k / 1% / 0.1 / 0603 (1608)	KOA Speer Electronics Inc.	RK73H1JTTD2001F
R118, R119	2	Resistor	20R / 1% / 0.25 / 1206 (3216)	Vishay	CRCW120620R0FK
R122, R123	2	Resistor	1R / 1% / 0.1 / 0603 (1608)	Panasonic	ERJ-3RQF1R0V

Reference	Qty	Type	Value/rating	Manufacturer	Part number
R148	1	Resistor	135k / 0.1% / 0.1 / 0603 (1608)	Yageo	RT0603BRD07135KL
R149	1	Resistor	59k / 1% / 0.1 / 0603 (1608)	Vishay	CRCW060359K0FK
R100, R101, R102, R150	4	Resistor	30k / 1% / 0.1 / 0603 (1608)	Vishay	CRCW060330K0FK
R185	1	Resistor	510R / 1% / 0.1 / 0603 (1608)	Yageo	RC0603FR-07510RL
Rin1, Rin2, Rin3, Rin4	4	Resistor	51k / 1% / 0.125 / 0805 (2012)	Vishay	CRCW080551K0FK
Ron1, Ron2, Ron3, Ron4	4	Resistor	10R / 1% / 0.1 / 0603 (1608)	ROHM Semiconductors	MCR03EZPFX10R0
Rss1, Rss2, Rss3, Rss4	4	Resistor	680R / 0.1% / 0.1 / 0603 (1608)	Yageo	RE0603BRE07680RL
Rt1, Rt2, Rt3	3	Resistor	NTC/ 100k / 0603 (1608)	Shenzhen Sunlord Electronics Co., Ltd.	SDNT1608X104F3950FTF

Reference	Qty	Type	Value/rating	Manufacturer	Part number
Rzd1, Rzd3	2	Resistor	470R / 1% / 0.5 / 0805 (2012)	Panasonic	ERJ-P06F4700V
Rzd2	1	Resistor	300R / 1% / 0.5 / 0805 (2012)	Panasonic	ERJ-P06F3000V
S1	1	Electro Mechanic	2Bit SPST Black Flat toggle / slotted / SMD-4P / 4.1x5.4mm / DIP	Dongguan KINGTEK	DSHP02TSGET
T1	1	Transformer	Buck with isolated windings (SJTU MAG-1238)	Shenzhen Yamaxi Technology Co	TBD
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35, TP36, TP37, TP38, TP39, TP40, TP41, TP42, TP43, TP44, TP45, TP46, TP47, TP48, TP49, TP50, TP51, TP52, TP53, TP74, TP75, TP76, TP77	54	Connector	PC TEST POINT MINIATURE / WHITE	Keystone Electronics	5002

Reference	Qty	Type	Value/rating	Manufacturer	Part number
TR1	1	Transformer	Resonant step-up transformer / 1 : 5	Shenzhen Yamaxi Technology Co	TBD
U1, U2	2	Integrated Circuit	DGTL ISO / 5.7KV / 2CH / GT DVR / DSO14	Infineon Technologies	2EDR7259X
U3, U4	2	Integrated Circuit	GATE DRVR / HIGH-SIDE / SOT23-6	Infineon Technologies	1EDN8550B
U5	1	Microcontroller	ARM Cortex-M33 / 3.6V - 1.71V / PG-LQFP-80-3	Infineon Technologies	PSC3M5FDS2AFQ1
U6, U7	2	Diode	TVS Diode / 6.1V / ST0201	STMicroelectronics	ESDALC6V1-1U2
U8	1	Diode	TVS Diode / 6.1V / SOT-23-3	STMicroelectronics	ESDA6V1L
Y1	1	Clock	CRYSTAL 16.0000MHZ / 8PF / SMD	Nihon Dempa Kogyo	NX3225SA-16.000MHZ-STD-CSR-1
Y2	1	Clock	CRYSTAL 32.7680KHZ / 12.5PF / SMD	CTS Electronic Component	TFA322PH327KR

Reference	Qty	Type	Value/rating	Manufacturer	Part number
ZD1, ZD2, ZD3	3	Diode	Zener Diode / 7.5V / 500mW / SOD-123	Diodes Incorporated	MMSZ5236B-7-F
M1, M2, M3, M4	4	Fastner	Nut / M2 x 0.5 / patch round	Sinhoo	SMTSO2005CTJ
HSK1	1	Heatsink	Custom REF_500W_CYCLO_BDSGAN_HSK1	PT Heatsink	H007242
HSK2	1	Heatsink	Custom REF_500W_CYCLO_BDSGAN_HSK2	PT Heatsink	H007243
	1	Insulator	30mm Width 50m Long Single Sided Strong Self-Adhesive Mylar Tape Yellow	Uxcell	a17072400ux0845
	1	Insulator	Tflex HD720 18x18in cut pieces	Laird	A17536-02
	4	Fastner	Screw / M2 x 8 / pan head	APM Hexseal	RM2X8MM 2701
	4	Fastner	HEX STANDOFF / #4-40 / SS / 1/2"	Keystone Electronics	2088

Reference	Qty	Type	Value/rating	Manufacturer	Part number
	4	Fastner	HEX NUT / 1/4" / STEEL / #4-40	Keystone Electronics	9600
PCB	1	PCB	V1.4 / FR4 / 6 layers of 2oz Cu / Green		

8.3 Heatsink drawings

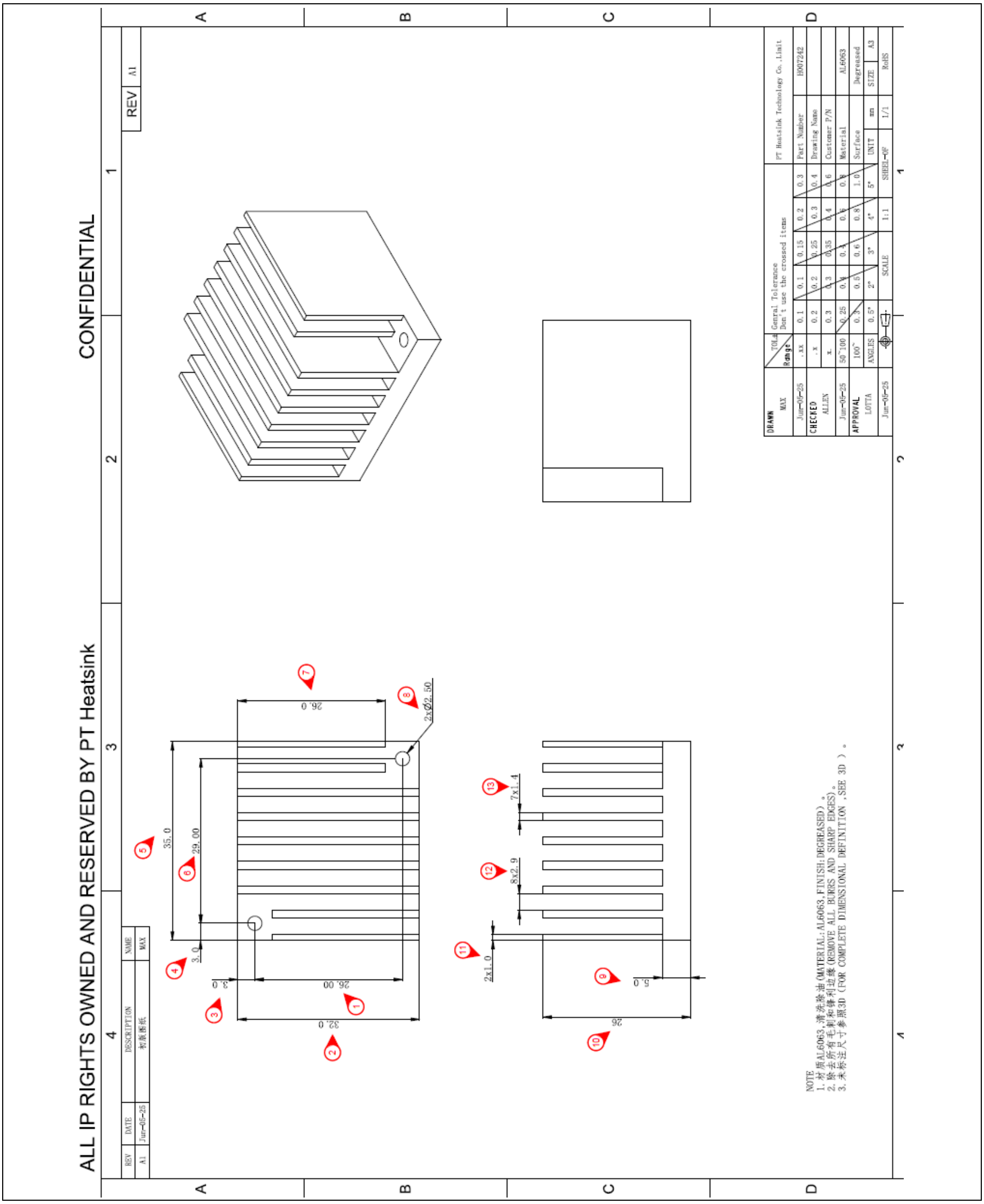


Figure 100 Heatsink REF_500W_CYCLO_BDSGAN_HSK1 (H007242)

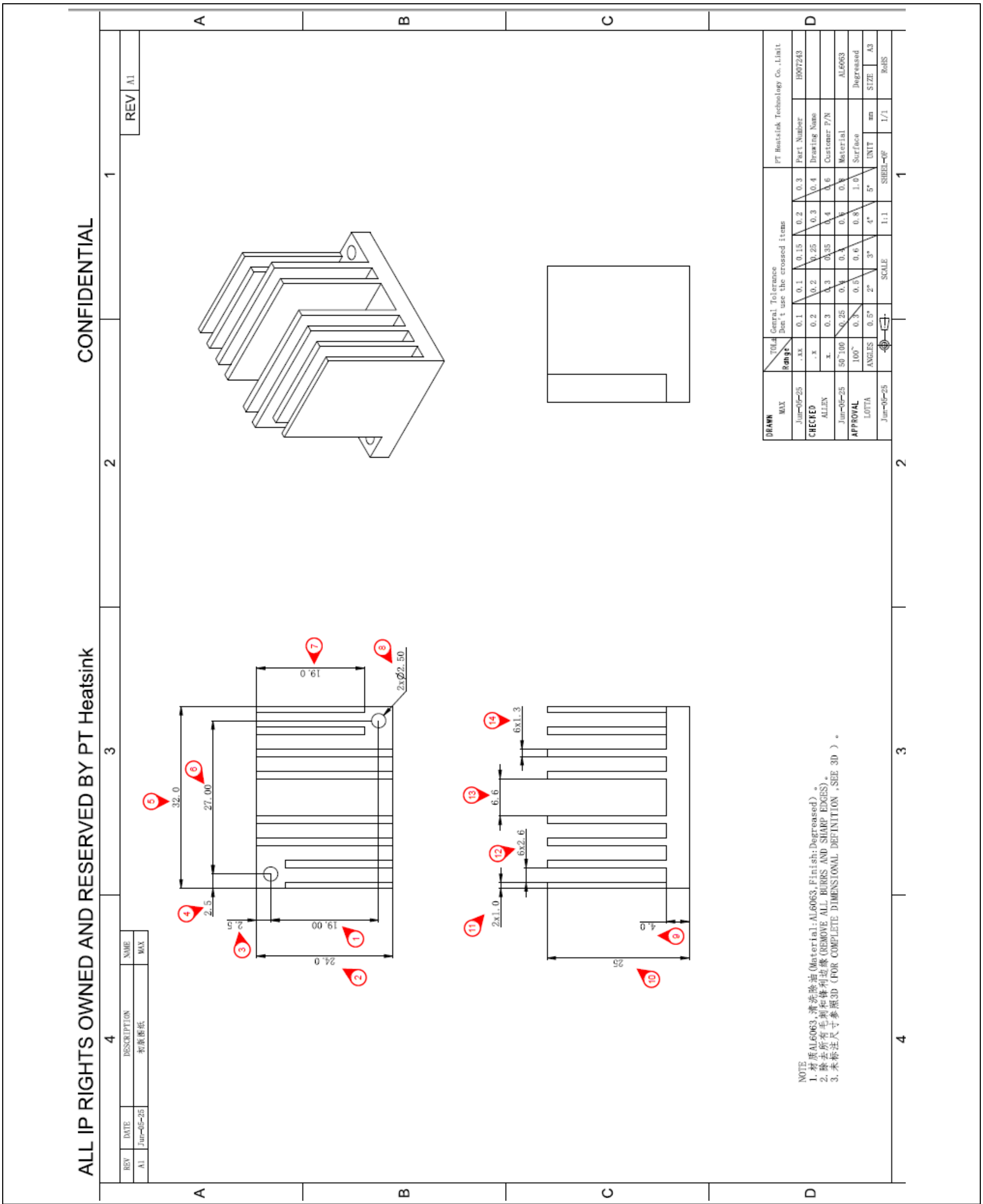


Figure 101 Heatsink REF_500W_CYCLO_BDSGAN_HSK2 (H007243)

9 Transformer and inductor specifications

9.1 Step-up transformer (TR1)

The step-up transformer is a custom-made part designed to provide isolation with a 1:5 step-up ratio from the DC primary side to the grid tied AC side. It is designed to integrate a defined leakage inductance required to create the resonant tank. The core material is PC96 or equivalent ferrite with PQ4035 geometry modified by grinding to reduce the overall height from 35 mm to between 30 mm and 32 mm.

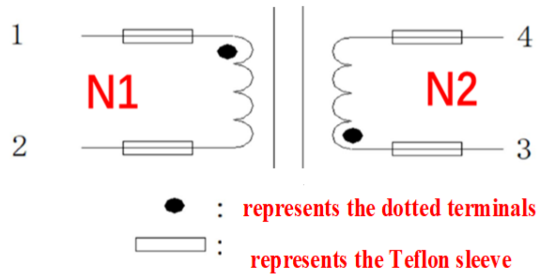


Figure 102 **Transformer format**

A magnetic insert made from the same PC96 material as the cores is placed between the windings N1 and N2.

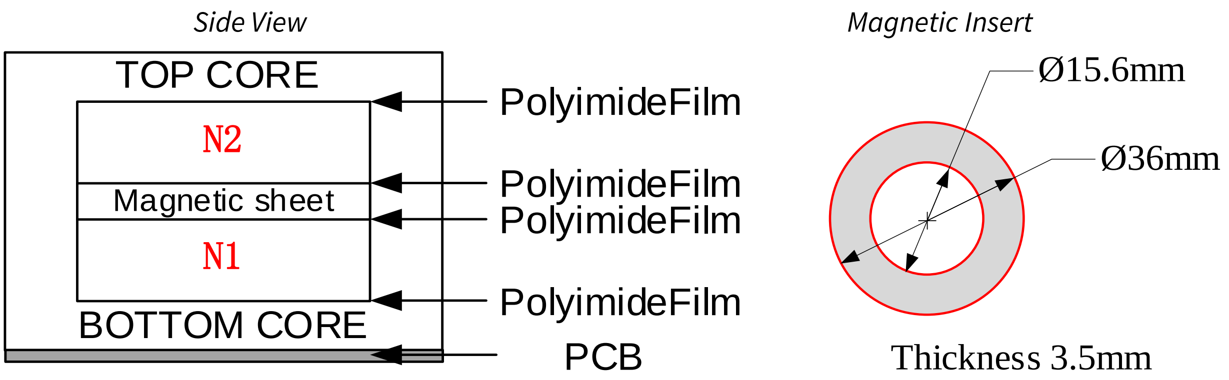


Figure 103 **Transformer structure**

The transformer is attached to a base made from FR4 PCB material according to the dimensions shown in the following diagram:

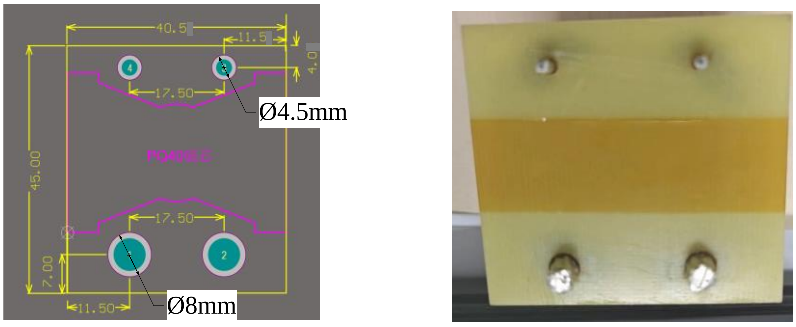


Figure 104 **Base and hole dimensions and picture showing protruding stripped wire terminations**

Winding details and test parameters are as follows:

Table 12 Transformer winding specifications

Winding	Start pin	Finish pin	Turns	Wire type	Winding notes
N1	1	2	3	Film-wrapped around Litz wire, 0.06 mm, 1100 strands x 2 parallel	Wound densely according to Figure 65
N2	3	4	15	Film-wrapped around Litz wire, 0.06 mm x 450 strands	Wound densely according to Figure 65

Table 13 Transformer test parameters

Parameter	Unit	Measurement point	Value	Test Condition
Inductance	µH	Pin 3 to pin 4	≥ 500	100 kHz, $1V_{RMS}$
Leakage Inductance	µH	Pin 3 to pin 4	59 to 61[1]	Pins 1 and 2 are shorted 100 kHz, $1V_{RMS}$
Dielectric strength	V_{RMS}	Pin 1 to pin 3 Pin 1 to core Pin 3 to core	1500	5 mA, 60 s

Leakage inductance is a critical parameter in this design and therefore, each core must me adjusted to provide a value within the specification above, which has a tolerance of less than 2 percent. The leakage inductance is reduced by grinding down the cores a little at a time and measuring the leakage inductance until the target specification is met. The core total core height should not be reduced below 30 mm. If the target leakage inductance is not achieved, the outer diameter of the magnetic sheet may also be reduced, which also serves to reduce leakage inductance. The finished transformer is shown in the following figure.

Figure 105 Integrated transformer viewed from both sides

[1] Values outside of this range may require some fine tuning of firmware parameters to achieve optimal efficiency.

9.2 Filter inductors (Lf1 and Lf2)

The filter inductors are common mode chokes custom-made as described in the following diagrams.

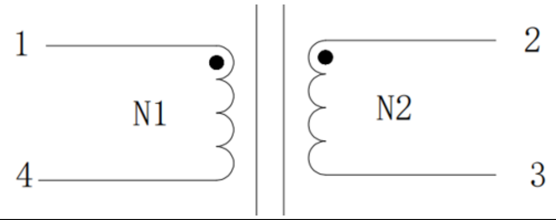


Figure 106 Common mode filter format

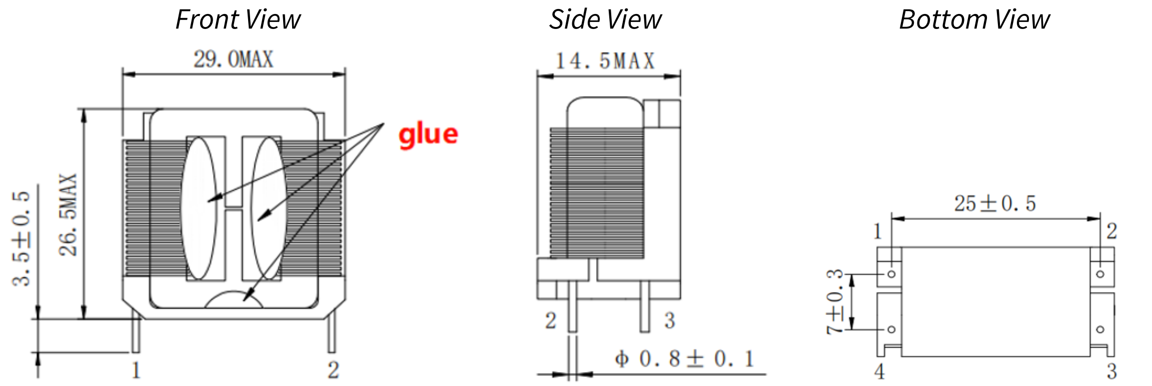
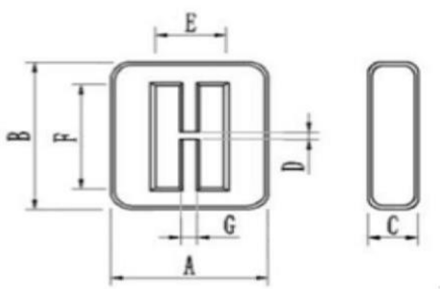


Figure 107 Filter inductor illustration and dimensions

The cores are ETV2320 shape made from M10K high permeability magnetic steel material:



	Product Dimensions	Post-Coating Dimensions
A	20. 5±0. 4	20. 9±0. 4
B	23. 3±0. 4	23. 7±0. 4
C	6. 2±0. 25	6. 6±0. 25
D	1. 4±0. 2	1. 0±0. 2
E	9. 8±0. 4	9. 0 min
F	17. 5±0. 5	16. 5 min
G	2. 25±0. 3	2. 55±0. 3

Figure 108 Filter inductor ETV2320 cores

The cores are glued together using H907 epoxy (UL number E304477).

The bobbin is made from plastic material T375HF rated to 150°C (UL number E39481).

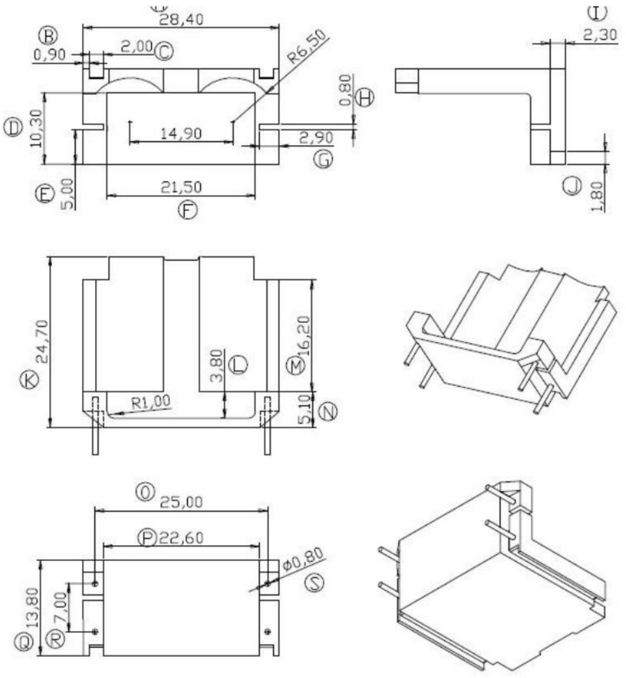


Figure 109 Bobbin details and dimensions

Table 14 Filter inductor winding specifications

Winding	Start pin	Finish pin	Turns	Wire type	Winding notes
N1	1	4	31	SFT - UEWH Φ0.4 x 1.8	Tightly wound
N2	2	3	31	SFT - UEWH Φ0.4 x 1.8	Tightly wound

Flat wire is used with insulation rated to 180°C (UL number E318511).

Table 15 Transformer test parameters

Parameter	Unit	Measurement point	Value	Test condition
Inductance	mH	Pins 1 to 4 and 2 to 3	≥ 4	100 kHz, 1 V_{RMS}
Leakage Inductance	µH	Pins 1 to 4 Pins 2 to 3	85 +/- 20%	Pins 2 and 3 are shorted Pins 1 and 4 are shorted 100 kHz, 1 V_{RMS}
DC Resistance	mΩ	Pins 1 to 4 and 2 to 3	25 +/- 12%	25°C
Dielectric strength	V_{RMS}	Pin 1 to pin 2	1000	5 mA, 60 s
Dielectric strength	V_{RMS}	Pin 1 to core Pin 2 to core	1000	5 mA, 60 s
Insulation Resistance	MΩ	Pin 1 to core Pin 2 to core	> 100	500 V_{DC}, 60 s

9.3 Auxiliary power inductor (T1)

The auxiliary power supply uses a multi-winding inductor custom-made according to the details given in the following figure.

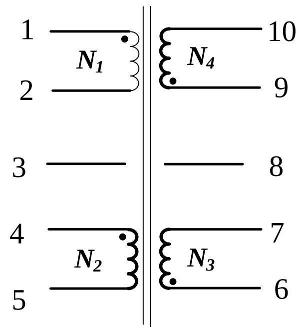


Figure 110 Auxiliary power inductor format

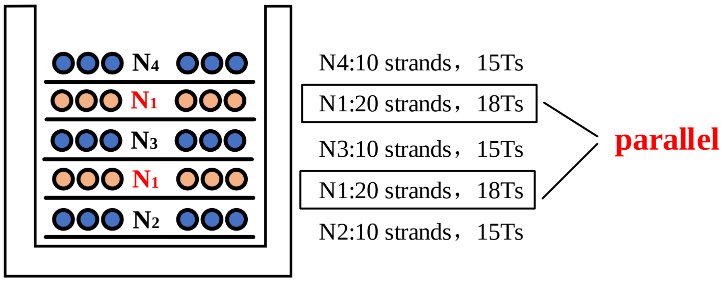
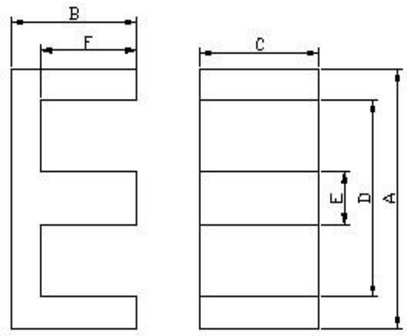


Figure 111 Auxiliary power inductor winding stack-up

The cores are standard EE25 size made from PC95 material with the center post ground to create an air gap to provide the correct A_L value.



Mold Type	Product Model	Dimensions(mm)					
		A	B	C	D	E	F
EE2520	EE25/20/6.4	25.0±0.5	10.0±0.3	6.4±0.3	18.0min	6.4±0.3	6.8±0.3

Figure 112 Filter inductor cores

The bobbin is a horizontal single section type as shown in Figure 113.

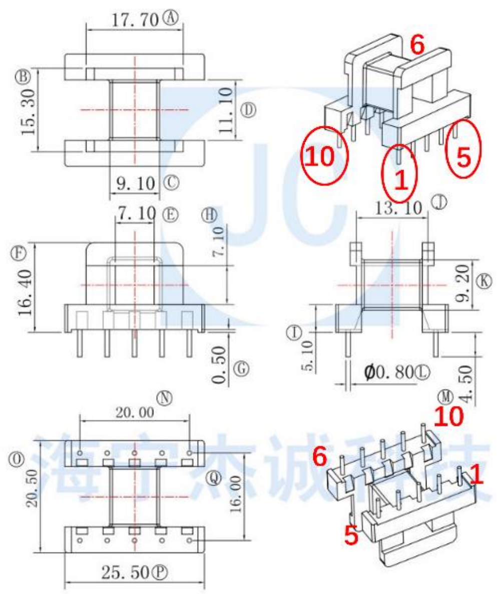


Figure 113 Bobbin details and dimensions

Table 16 Auxiliary power inductor winding specifications

Winding	Start pin	Finish pin	Turns	Wire type	Winding notes
N1	1	2	18	Ø0.1 mm Litz, 2 x 20 strands	
Three layers of insulating tape					
N2	4	5	15	Ø0.1 mm Litz, 10 strands	
Three layers of insulating tape					
N3	6	7	15	Ø0.1 mm Litz, 10 strands	
Three layers of insulating tape					
N4	9	10	15	Ø0.1 mm Litz, 10 strands	

Table 17 Auxiliary power inductor test parameters

Parameter	Unit	Measurement point	Value	Test condition
Inductance	µH	Pins 1 to 2	100 +/-15%	100 kHz, 1 V_{RMS}
DC Resistance	mΩ	Pins 1 to 2	< 100 mΩ	25°C
Dielectric strength	V_{RMS}	Pin 1 to pin 4 Pin 1 to pin 6 Pin 1 to pin 9	1500	50 Hz, 3 mA, 60 s
Insulation Resistance	MΩ	Pin 1 to core Pin 4 to core Pin 6 to core Pin 9 to core	> 100	500 V_{DC}, 60 s

10 PCB layout design

The main PCB is fabricated on 6-layer FR4 material using 2 oz. copper on all layers with all components mounted on the top side.

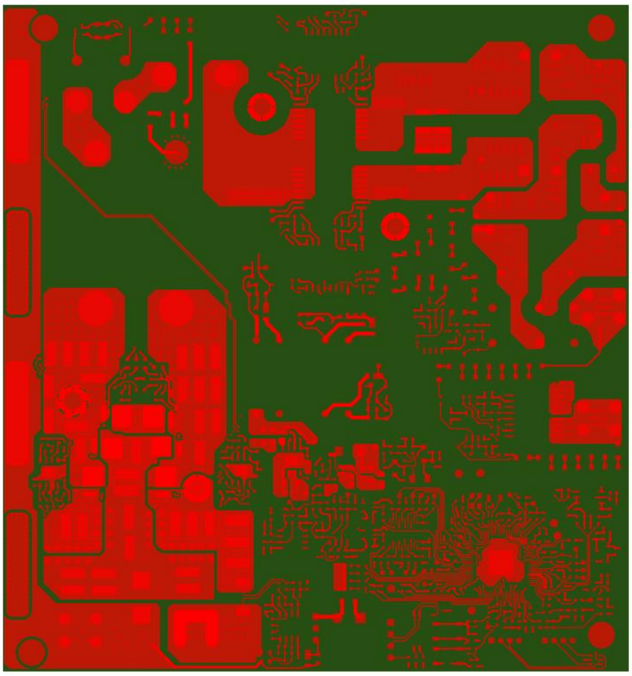


Figure 114 Top layer copper

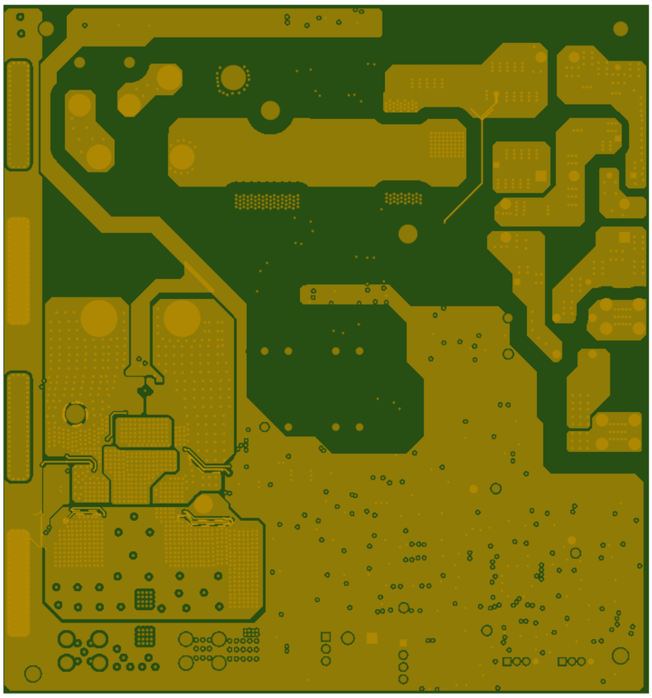


Figure 115 First inner layer copper

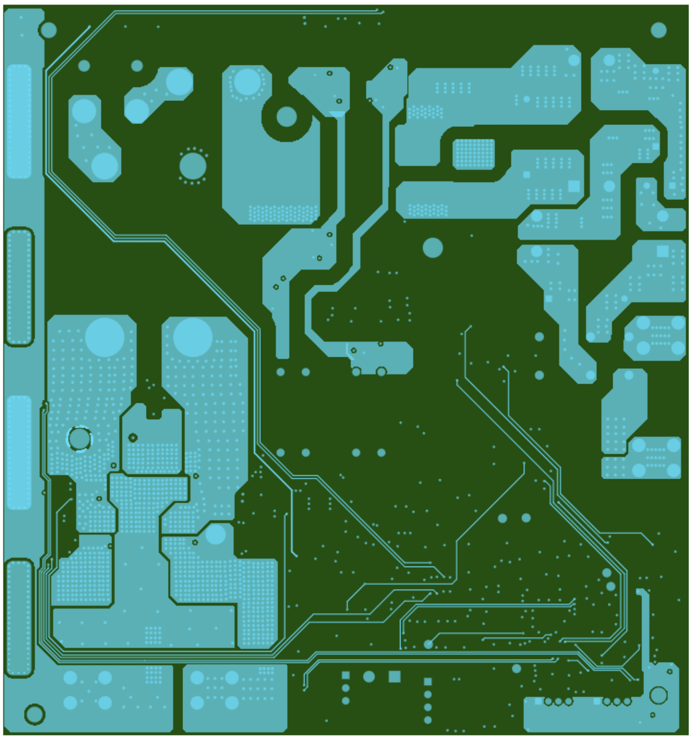


Figure 116 Second inner layer copper

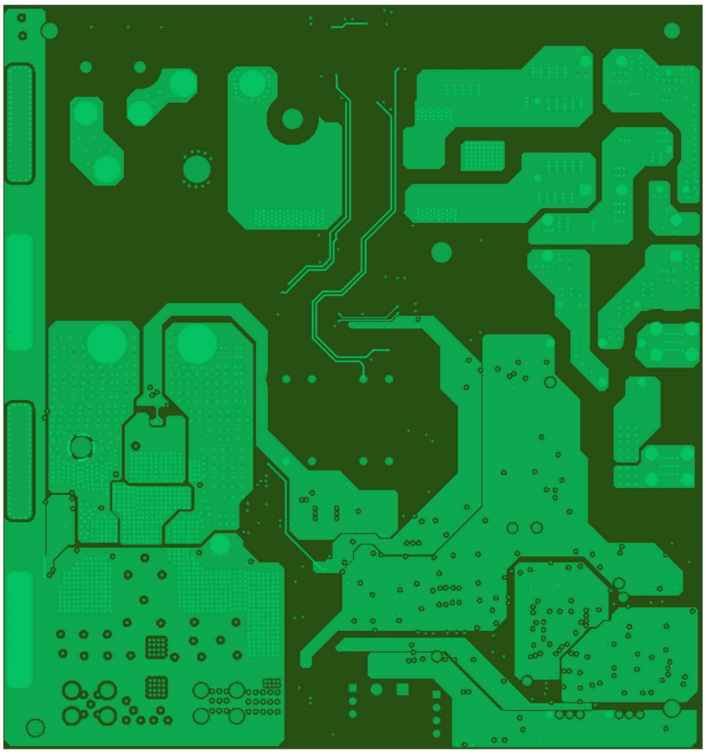


Figure 117 Third inner layer copper

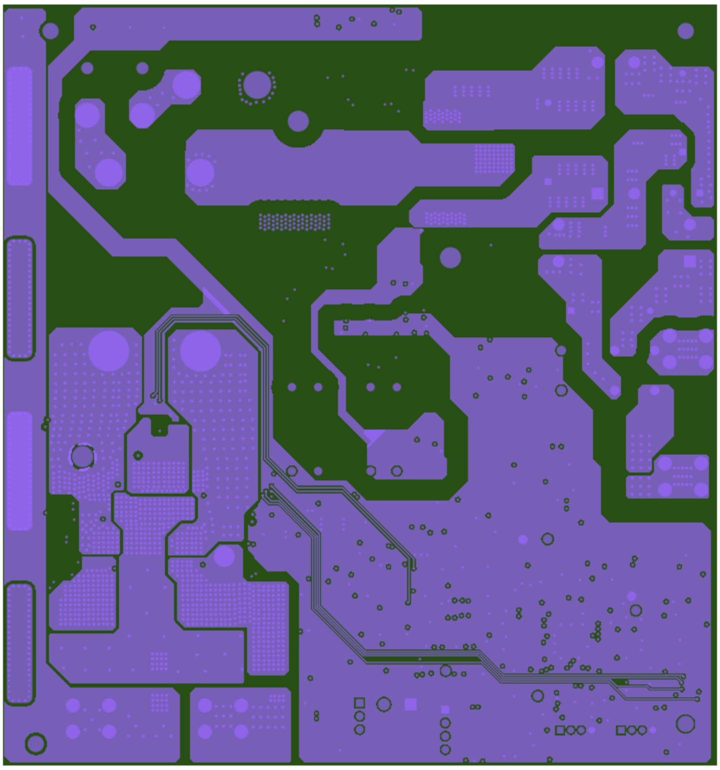


Figure 118 Fourth inner layer copper

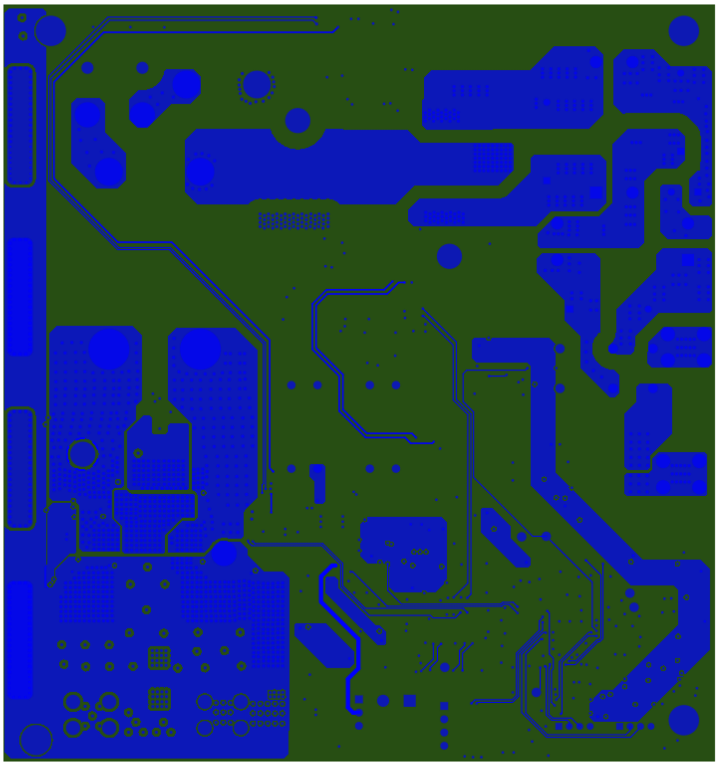


Figure 119 Bottom layer copper

The layer composition is as follows:

Table 18 Layer organization

Layer	Power planes	Signal traces	Comment
L1 (top)	DC+ input terminal DC- input current shunt Electrolytic capacitor connections Primary switches Main transformer Secondary switches Output filter and terminals	MCU connections Sensing amplifiers and other low control circuitry	The majority of the signal connections are located on this layer
L2 (inner)	DC- power plane Primary ground plane Primary switches Main transformer Output filter and terminals	VAC- sensing	No other signal traces on this layer
L3 (inner)	DC+ input terminal DC- input current shunt Primary switches Main transformer Output filter and terminals		Some parallel signal sensing traces some miscellaneous signal traces
L4 (inner)	Auxiliary power and voltage reference planes Primary switches Main transformer Output filter and terminals		Some parallel signal sensing traces some miscellaneous signal traces
L5 (inner)	DC+ input terminal DC- input current shunt Primary switches Main transformer Output filter and terminals Large primary ground plane		Some parallel signal sensing traces some miscellaneous signal traces
L6 (bottom)	DC- power plane Primary ground plane Primary switches Main transformer Output filter and terminals		Some parallel signal sensing traces some miscellaneous signal traces

In general, the board has been designed to provide the maximum sized possible power planes duplicated on different layers to minimize conduction losses. Sensitive signal sensing traces and other PWM signals are carried along parallel traces to minimize inductance and surrounded by ground plane as much as possible.

10.1 Electrolytic capacitor board

The DC input electrolytic capacitors are mounted on a separate daughter card, which is inserted into slotted pads on the main board to provide a secure mechanical and electrical connection. This mounting method has been implemented because the capacitors are physically large with short snap-in type terminals.

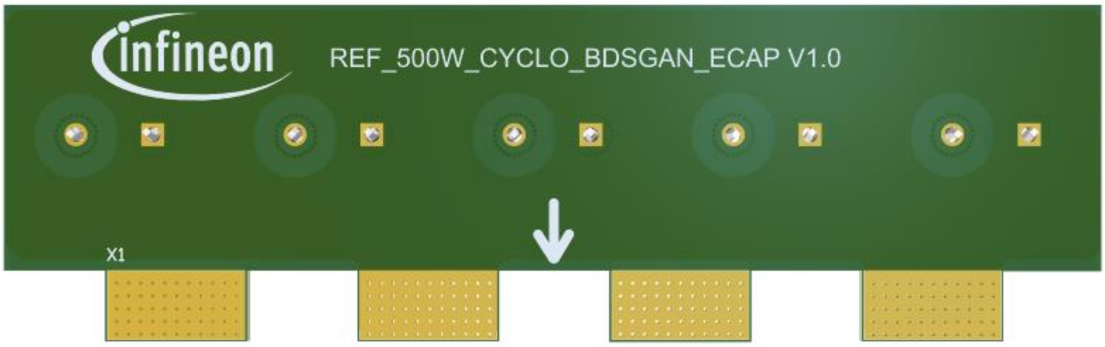


Figure 120 Electrolytic capacitor board front

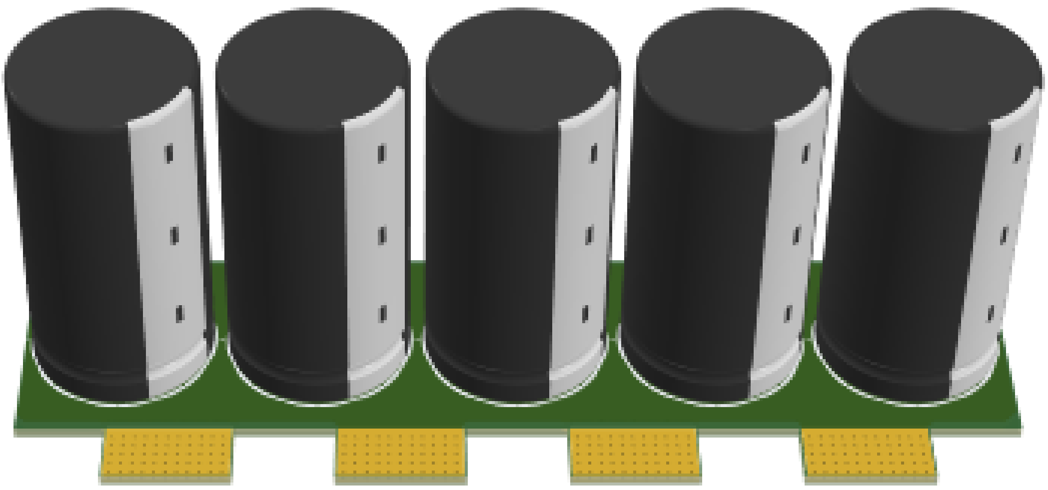


Figure 121 Electrolytic capacitor board back

11 Test results

11.1 Power and efficiency measurements

All measurements have been averaged over 64 samples to remove fluctuations due to ripple to provide stable and repeatable results.

11.1.1 Off-grid operation

The following measurements were made for off-grid operation at 240 V_{RMS} 60 Hz:

Table 19 Test measurements – off grid operation

DC Input voltage	DC input current	Input power	AC Output RMS voltage	AC Output RMS current	Power Factor	Output power	Efficiency	iTHD
36.021	3.5996	105.74	239.16	0.40606	0.999	97.1	91.83%	2.6%
35.968	7.121	205.82	238.73	0.8329	0.999	198.85	96.61%	2.8%
35.914	10.624	304.95	238.23	1.2471	0.999	296.82	97.33%	2.3%
35.864	14.087	403.7	237.75	1.6561	0.999	393.47	97.47%	1.8%
35.812	17.43	500.3	237.26	2.0539	1	487.07	97.36%	1.4%

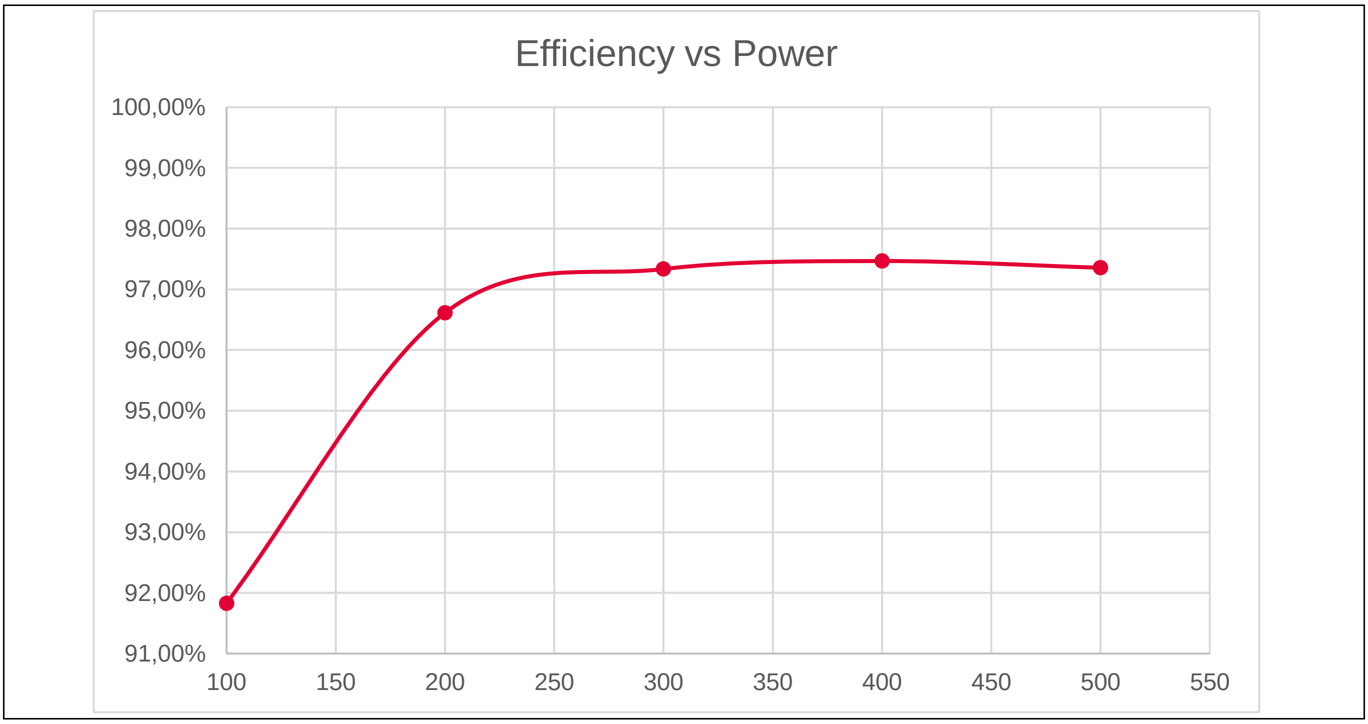


Figure 122 Off-grid operation efficiency curve

11.1.1.1 Voltage and current harmonics

The following measurements of harmonic content of the voltage and current outputs from the fundamental to the 40th harmonic indicating low THD with the majority of harmonic content in the odd harmonics:

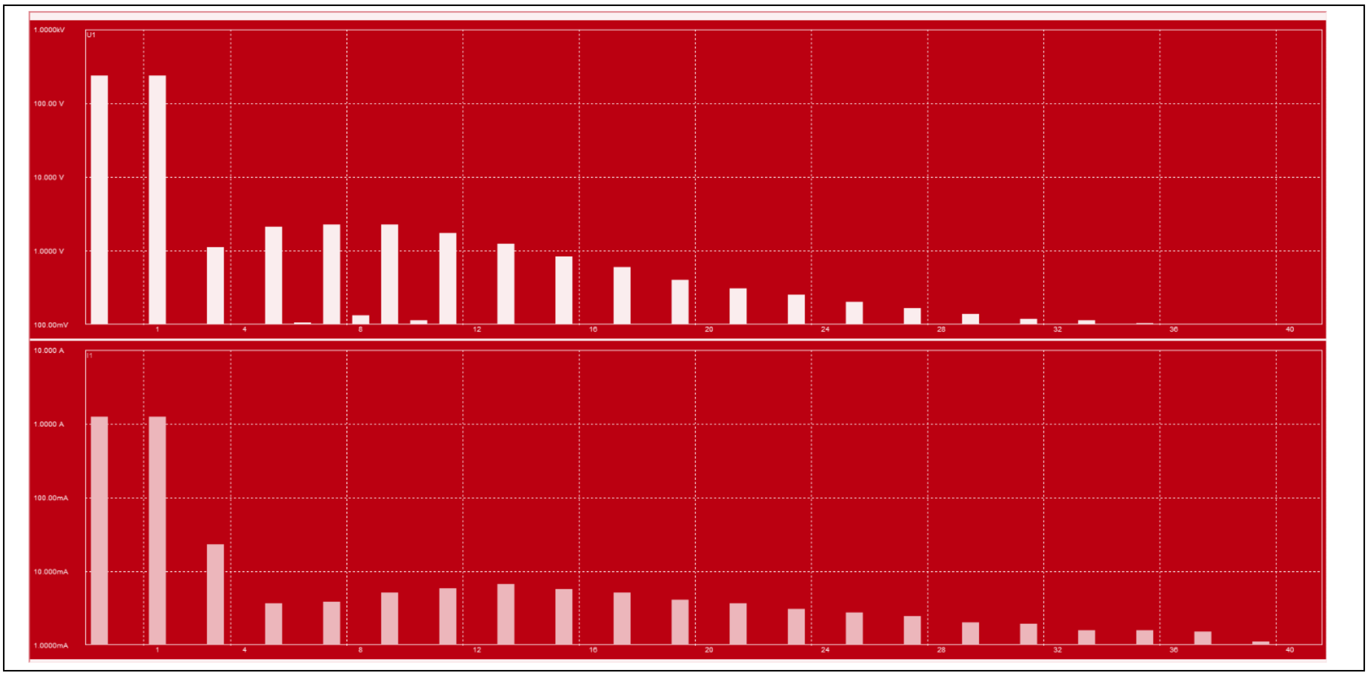


Figure 123 Voltage (top) and current (bottom) harmonic content at 300 W output

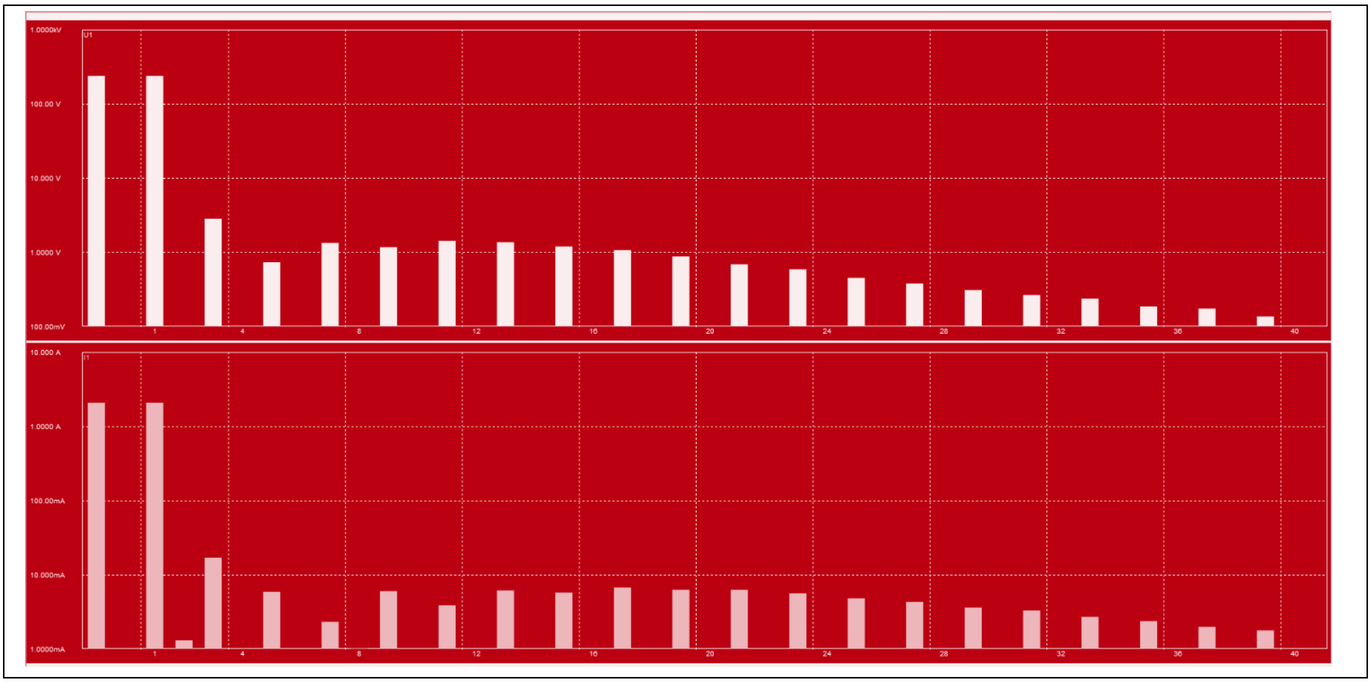


Figure 124 Voltage (top) and current (bottom) harmonic content at 500 W output

11.1.2 On-grid operation with burst mode enabled

The following measurements were made for on-grid operation at 240 V_{RMS} 60 Hz with burst mode enabled.

Table 20 Test measurements – on-grid operation (burst mode enabled)

DC Input voltage	DC input current	Input power	AC Output RMS voltage	AC Output RMS current	Power Factor	Output power	Efficiency
36.042	4.244	63.300	240.160	0.498	0.475	57.400	90.68%
36.015	5.901	124.150	240.160	0.693	0.689	118.400	95.37%
35.983	8.826	180.700	240.280	1.014	0.705	175.000	96.85%
35.946	8.549	247.570	240.380	1.001	0.997	239.730	96.83%
35.912	10.676	308.190	240.470	1.250	0.998	299.710	97.25%
35.881	12.830	369.300	240.570	1.498	0.998	359.680	97.40%
35.847	14.950	429.800	240.650	1.743	0.998	418.500	97.37%
35.816	17.046	488.700	240.730	1.979	0.998	475.480	97.29%

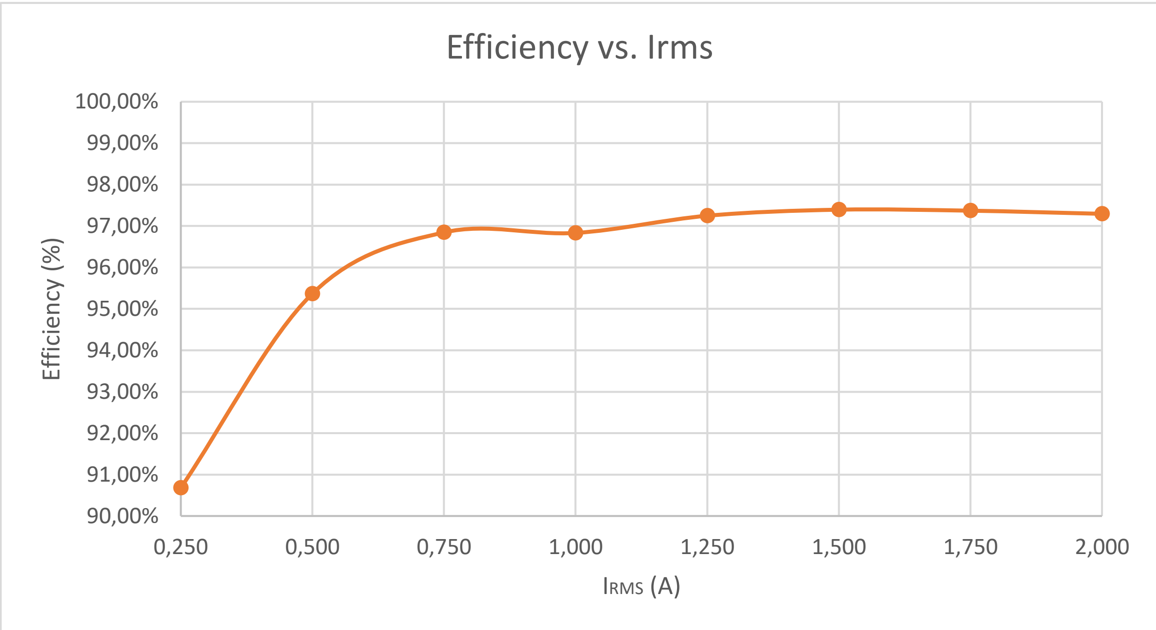


Figure 125 On-grid operation with burst mode enabled efficiency curve

The **peak efficiency is 97.4 percent**, measured at 1.5 A_{RMS} output current corresponding to approximately 360 W, which is 72 percent of the maximum rated load.

The results shown here are for a fully optimized board including fine tuning of firmware parameters. Results may vary depending on component tolerances.

11.1.2.1 CEC weighted efficiency measurements and calculation

The following measurements were made for on-grid operation at 240 V_{RMS} 60 Hz with burst mode enabled. Measurements are made for specific load levels defined for the CEC weighted efficiency formula. CEC measurements – on-grid operation (burst mode enabled) CEC.

Table 21 CEC weighted efficiency measurements and calculation

Load	DC input voltage	DC input current	Input power	AC output RMS voltage	AC output RMS current	Power factor	Output power	Efficiency
5%	36.060	2.860	31.200	240.370	0.336	0.303	24.420	78.269%
10%	36.048	4.030	55.050	240.180	0.472	0.428	48.830	88.701%
20%	36.023	6.086	103.520	240.340	0.710	0.570	97.500	94.185%
30%	36.000	7.263	146.800	240.200	0.850	0.694	141.600	96.458%
50%	35.942	8.893	257.620	240.350	1.041	0.997	249.720	96.933%
75%	35.871	13.379	384.800	240.590	1.561	0.998	374.710	97.378%
100%	35.806	17.748	508.300	240.760	2.057	0.998	494.340	97.254%

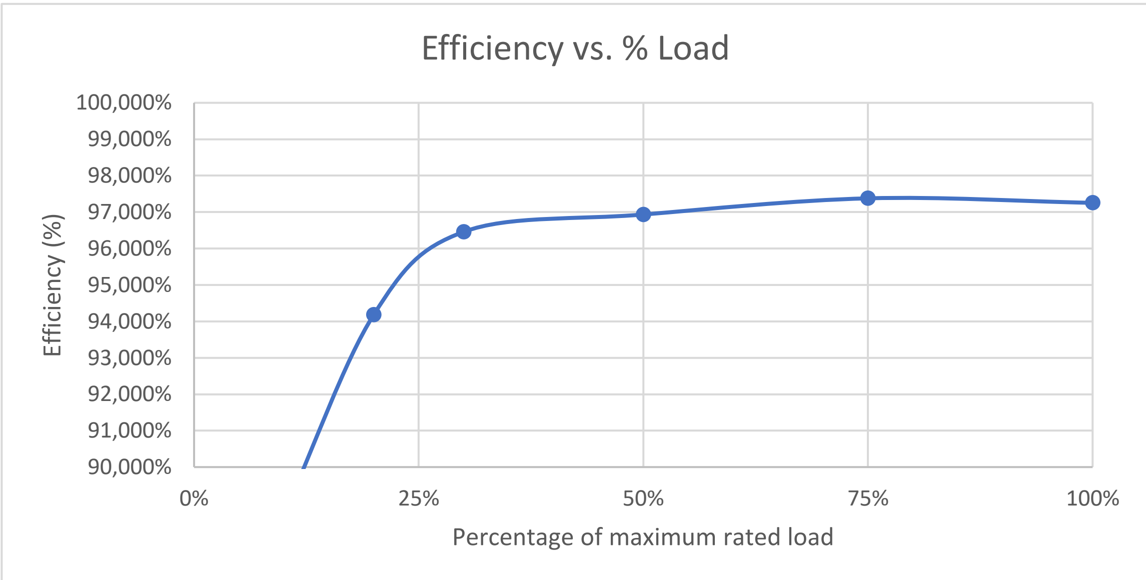


Figure 126 On grid operation with burst mode enabled efficiency curve

CEC weighted efficiency is calculated as follows:

$$EFF_{CECW} = (0.04 \times Eff@10\%) + (0.05 \times Eff@20\%) + (0.12 \times Eff@30\%) + (0.21 \times Eff@50\%) + (0.53 \times Eff@75\%) + (0.05 \times Eff@100\%)$$

$$\mathbf{EFF_{CECW} = 96.7\%}$$

Equation 47

European weighted efficiency is calculated as follows:

$$EFF_{EU} = (0.03 \times Eff@5\%) + (0.06 \times Eff@10\%) + (0.13 \times Eff@20\%) + (0.1 \times Eff@30\%) + (0.48 \times Eff@50\%) + (0.2 \times Eff@100\%)$$

$$\mathbf{EFF_{EU} = 95.5\%}$$

Equation 48

11.1.3 MPPT efficiency

The MPPT function of the REF_500W_CYCLO_BDSGAN board is tested by connecting the DC inputs to a Chroma 62150H-1000S PV array simulator and the GUI to setting Grid ON mode and clicking the **MPPT ON/OFF** button to enable it instead of setting a defined output current. The AC grid simulator voltage is set to 240 V_{RMS} and switched on before pressing the **START/STOP** button to begin operation.

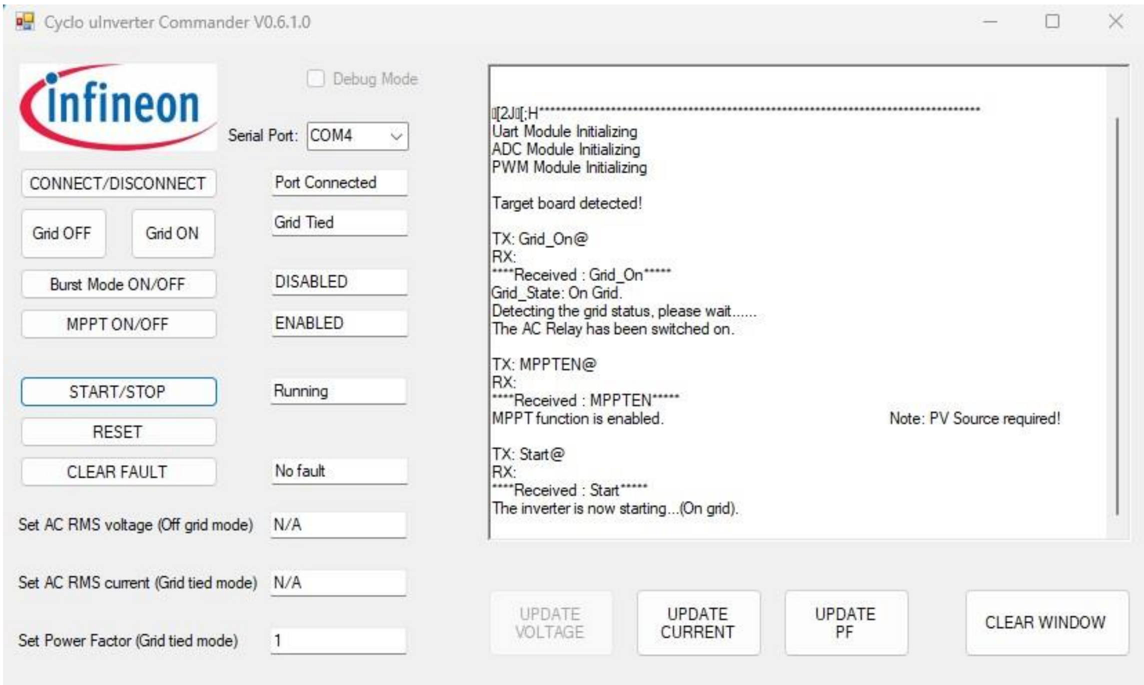


Figure 127 Setting MPPT mode for grid tied operation

Tests were performed at three different power levels at various input voltages:

Table 22 MPPT efficiency measurements at different input voltages and loads

DC input voltage	25% rated load	50% rated load	75% rated load
30	99.32%	99.52%	99.69%
35	98.57%	99.88%	99.89%
40	97.46%	99.93%	99.90%
45	96.76%	99.89%	99.91%
50	96.05%	99.99%	99.99%

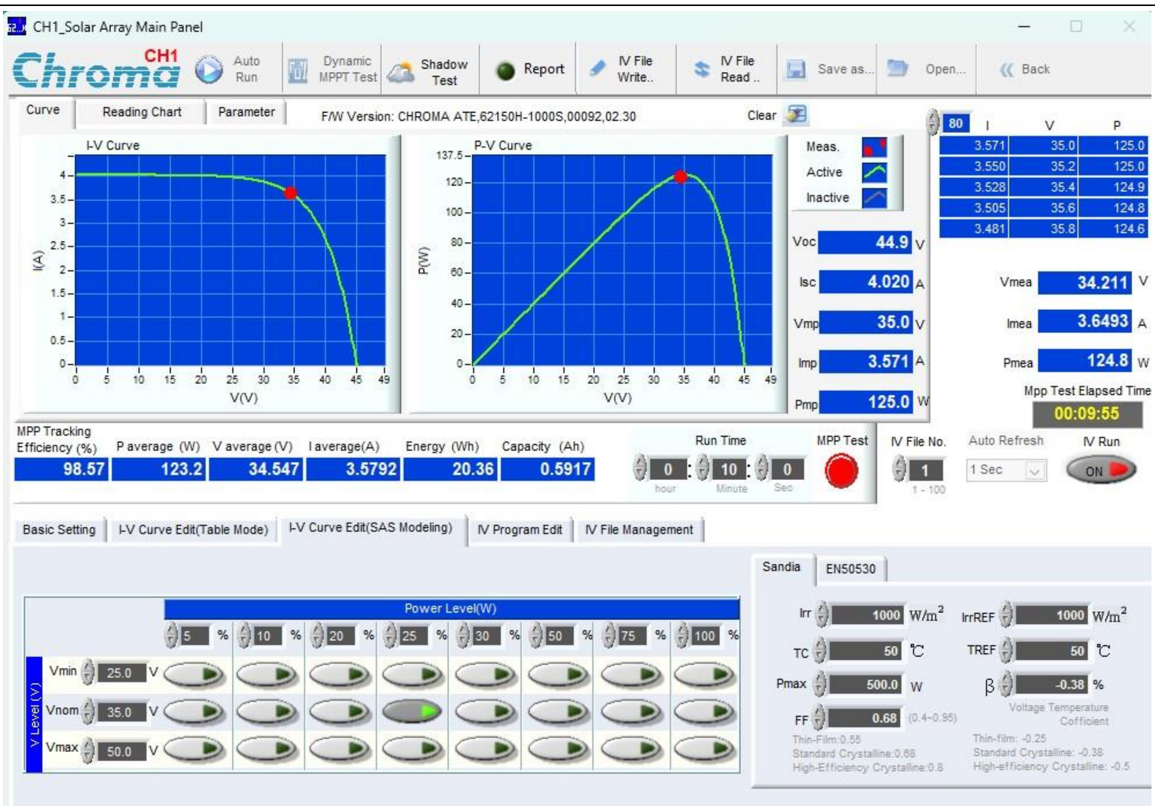


Figure 128 Operating point 35V input, 25% load

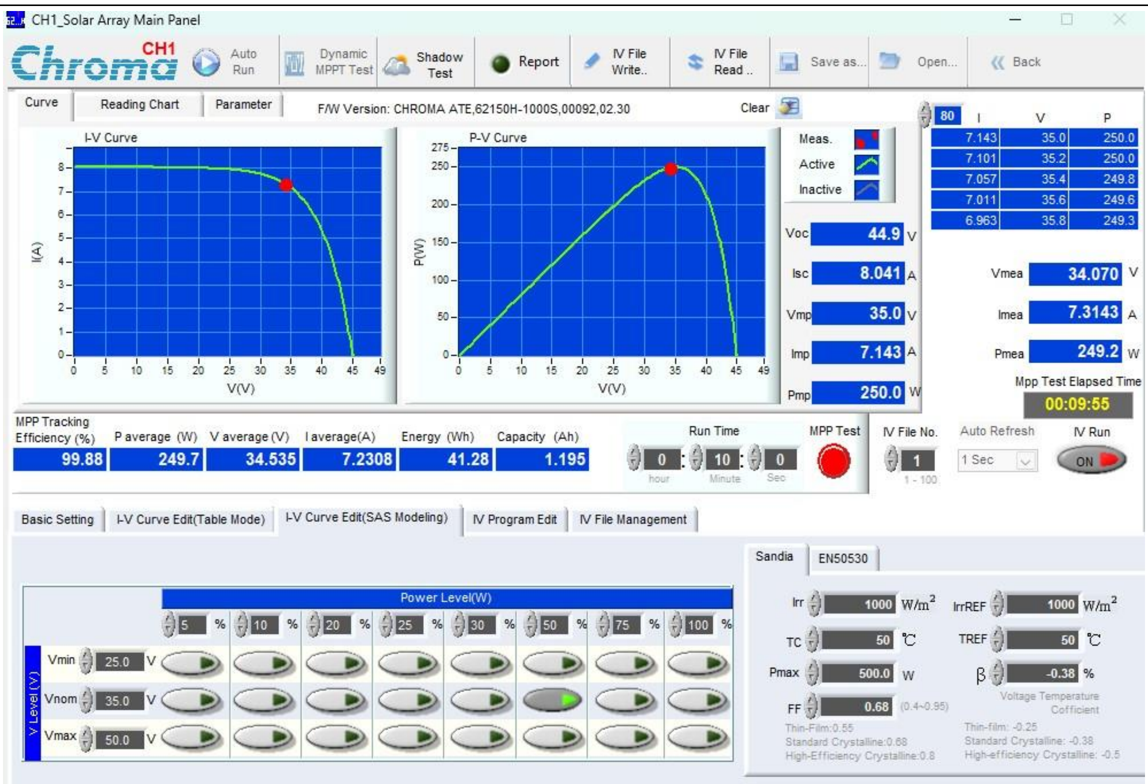


Figure 129 Operating point 35V input, 50% load

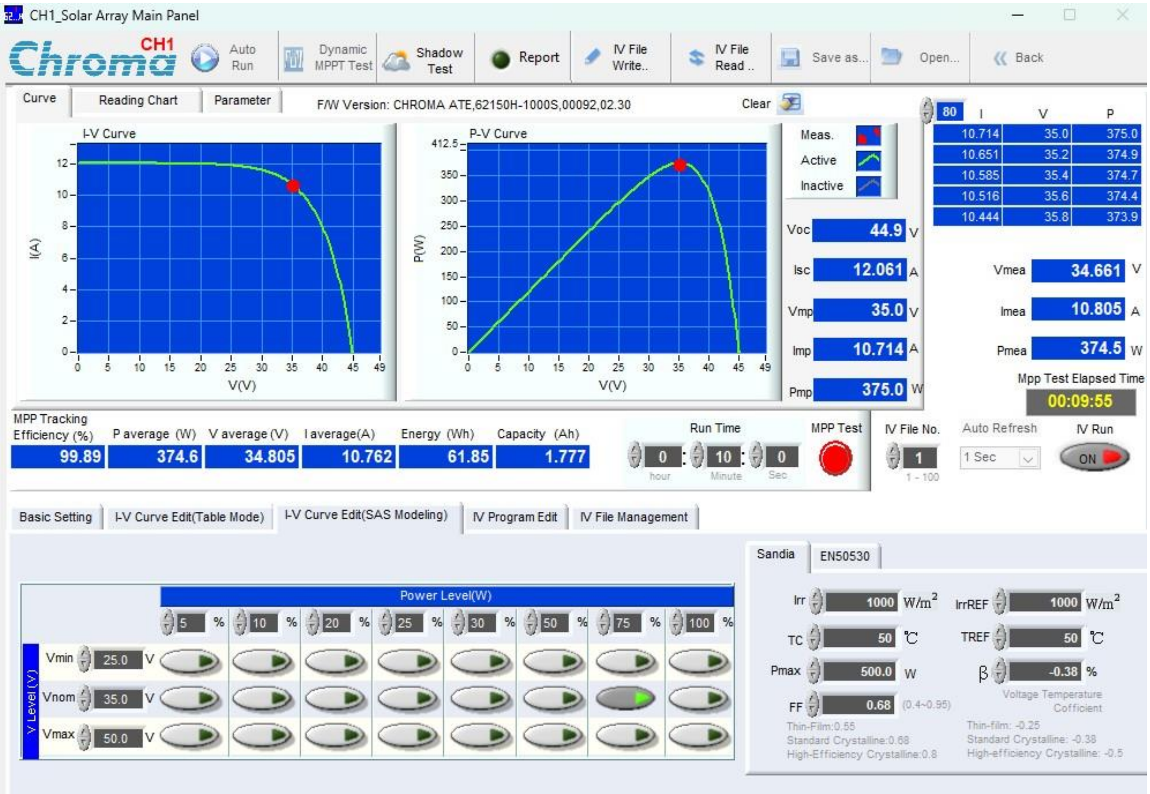


Figure 130 Operating point 35V input, 75% load

11.2 Thermal measurements

The following thermal image was captured after 30 minutes of operation at maximum load with no forced air cooling:

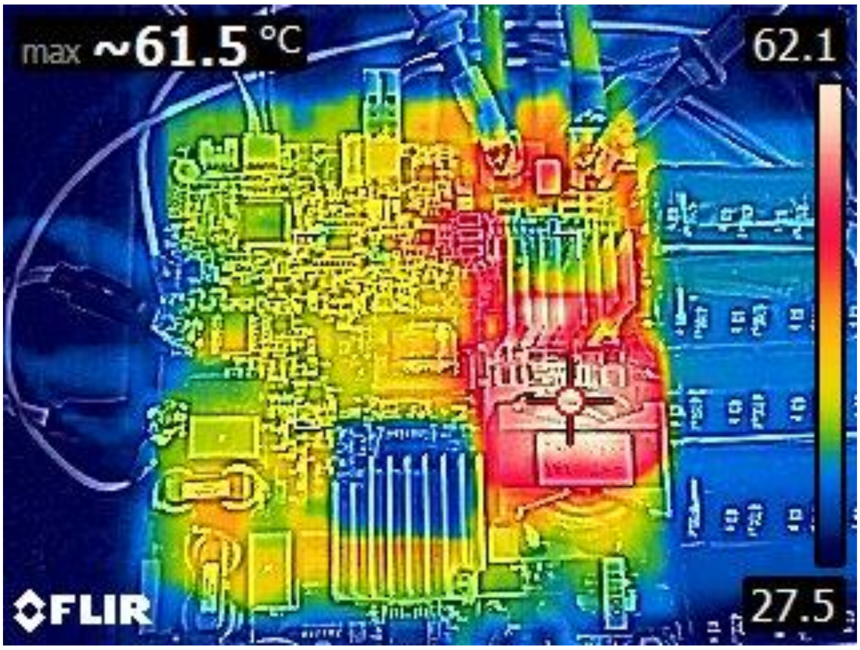


Figure 131 REF_500W_CYCLO_BDSGAN thermal image

It can be seen that the maximum temperature on the board is around 62 degrees Celsius, measured at the main transformer and that the bidirectional GaN switches reach a similar temperature.

11.3 Operating waveforms

Measurements are taken at 35 V input and 240 V_{RMS} output.

11.3.1 Off-grid operation

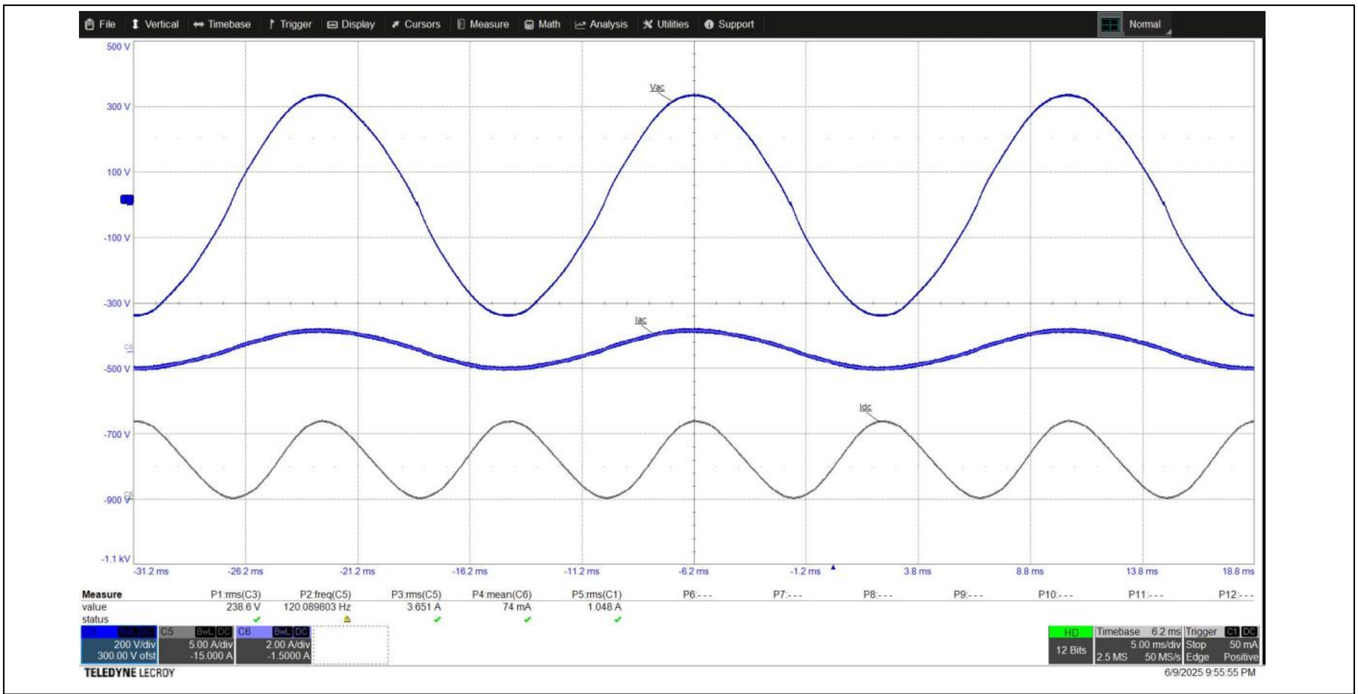


Figure 132 Load 100 W - output voltage (blue), output current (purple), DC input current (gray)

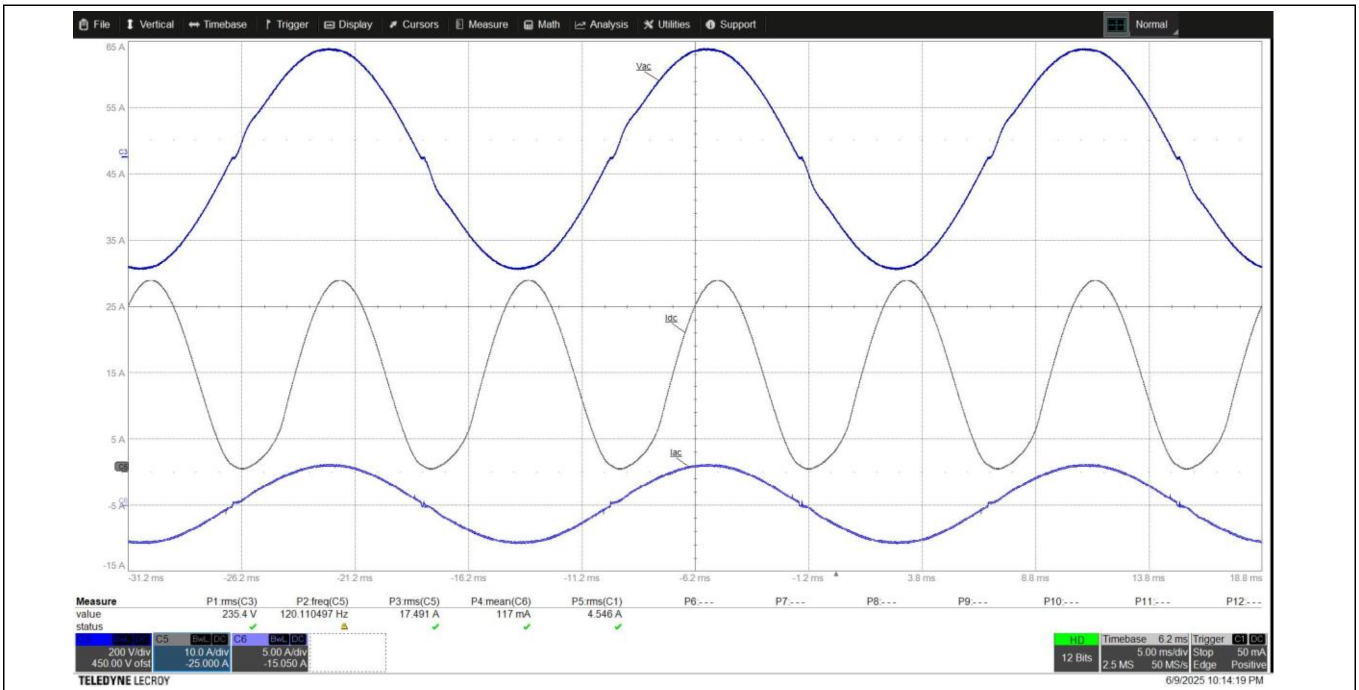


Figure 133 Load 500 W - output voltage (blue), output current (purple), DC input current (gray)

11.3.2 On-grid operation

Measurements are taken at 240 V_{RMS} output.

11.3.2.1 Input 35 VDC

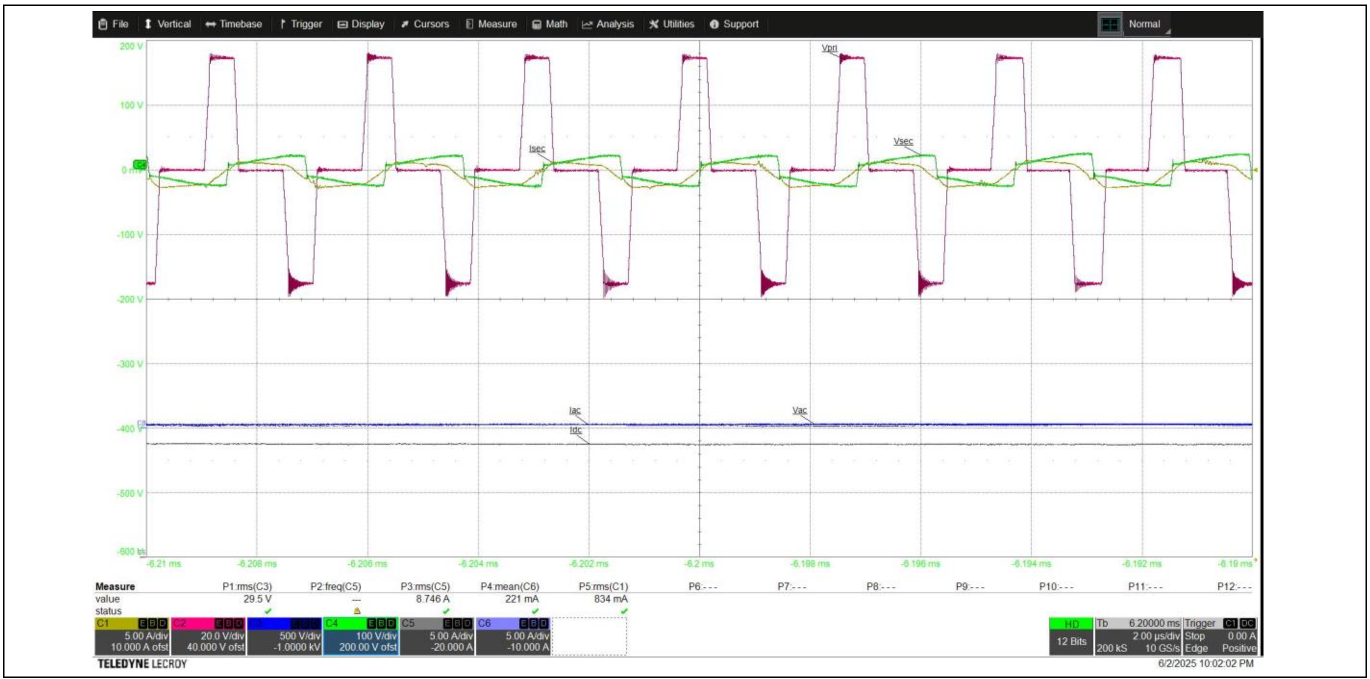


Figure 134 Output 1.0 A_{RMS} - primary voltage (red), secondary voltage (green), resonant current (yellow)

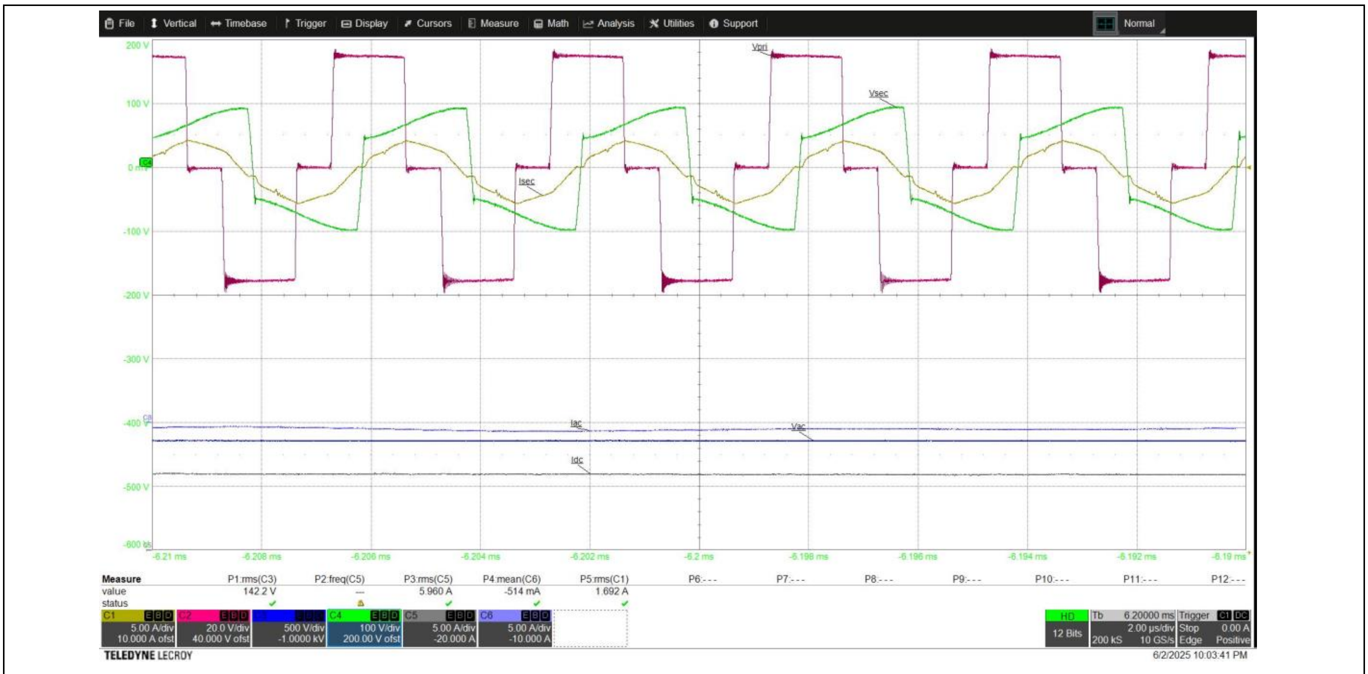


Figure 135 Output 1.0 A_{RMS} - primary voltage (red), secondary voltage (green), resonant current (yellow)

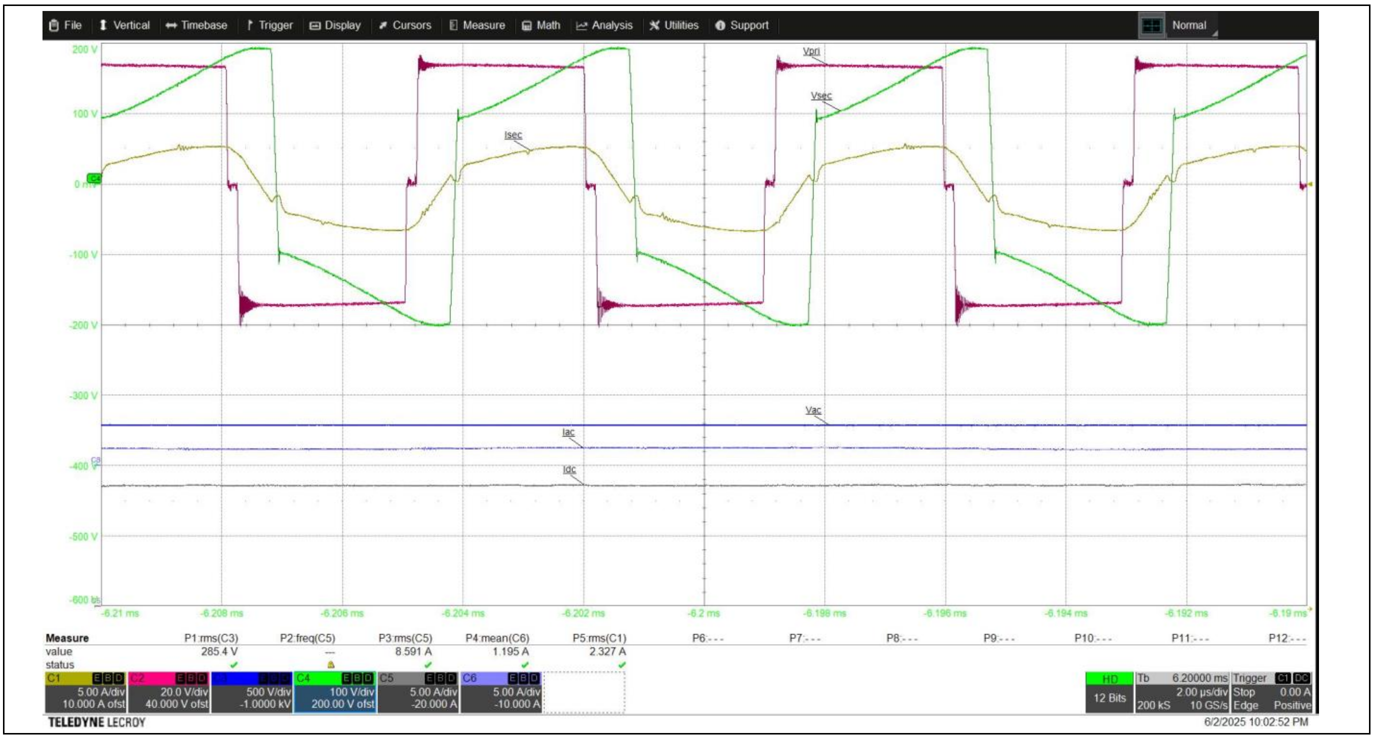


Figure 136 **Output 1.0 A_{RMS} - primary voltage (red), secondary voltage (green), resonant current (yellow)**

Figure 137 **Output 2.0 A_{RMS} - primary voltage (red), secondary voltage (green), resonant current (yellow)**

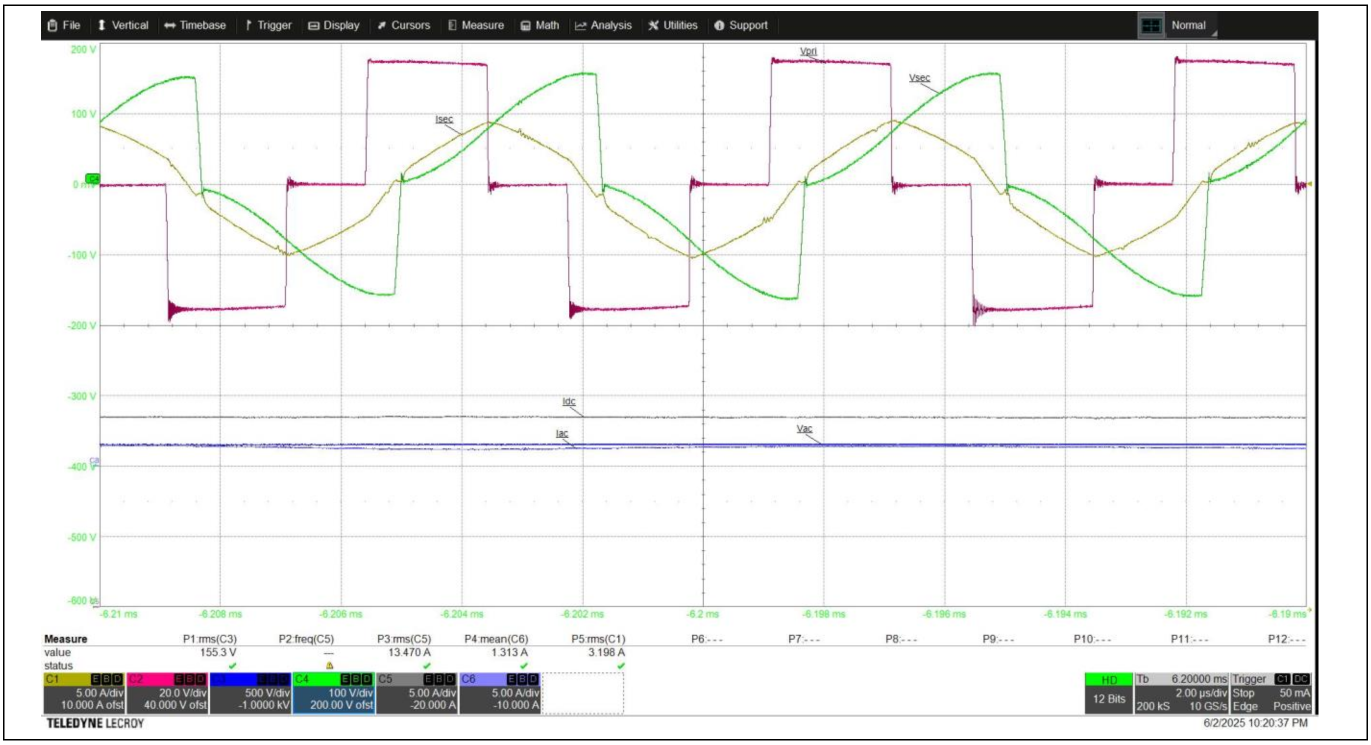


Figure 138 **Output 2.0 A_{RMS} - primary voltage (red), secondary voltage (green), resonant current (yellow)**

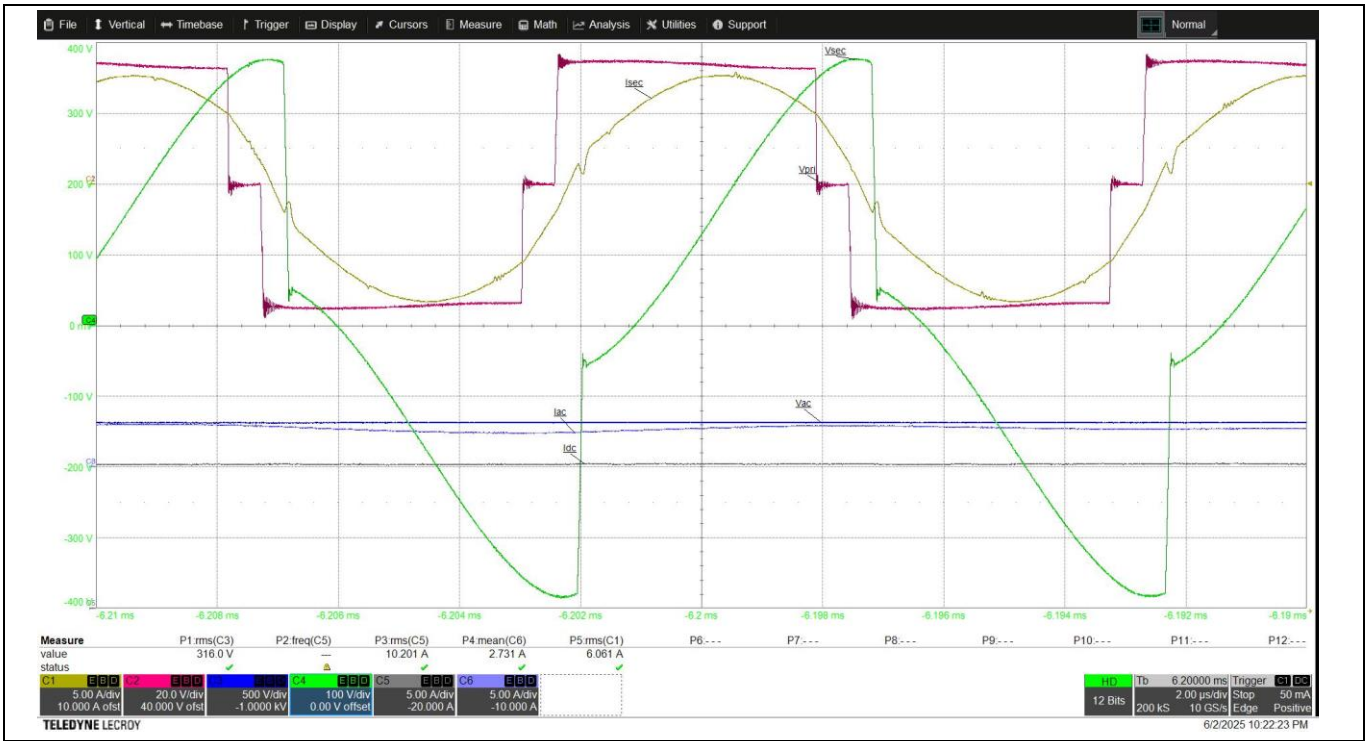


Figure 139 **Output 2.0 A_{RMS} - primary voltage (red), secondary voltage (green), resonant current (yellow)**

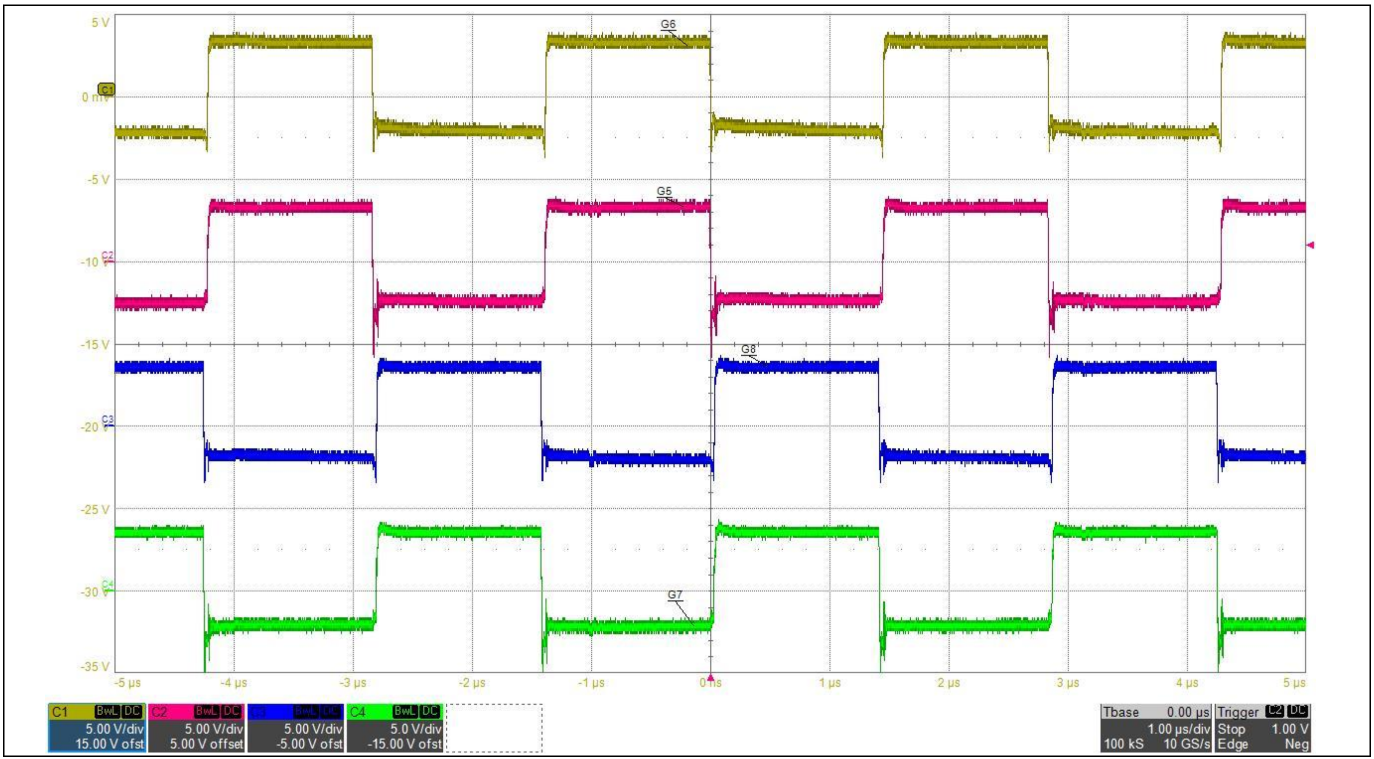


Figure 140 Bi-directional GaN V_{GS} gate drive voltages – Q7-G6 (yellow), Q7-G5 (red), Q8-G8 (blue), Q8-G7 (green)

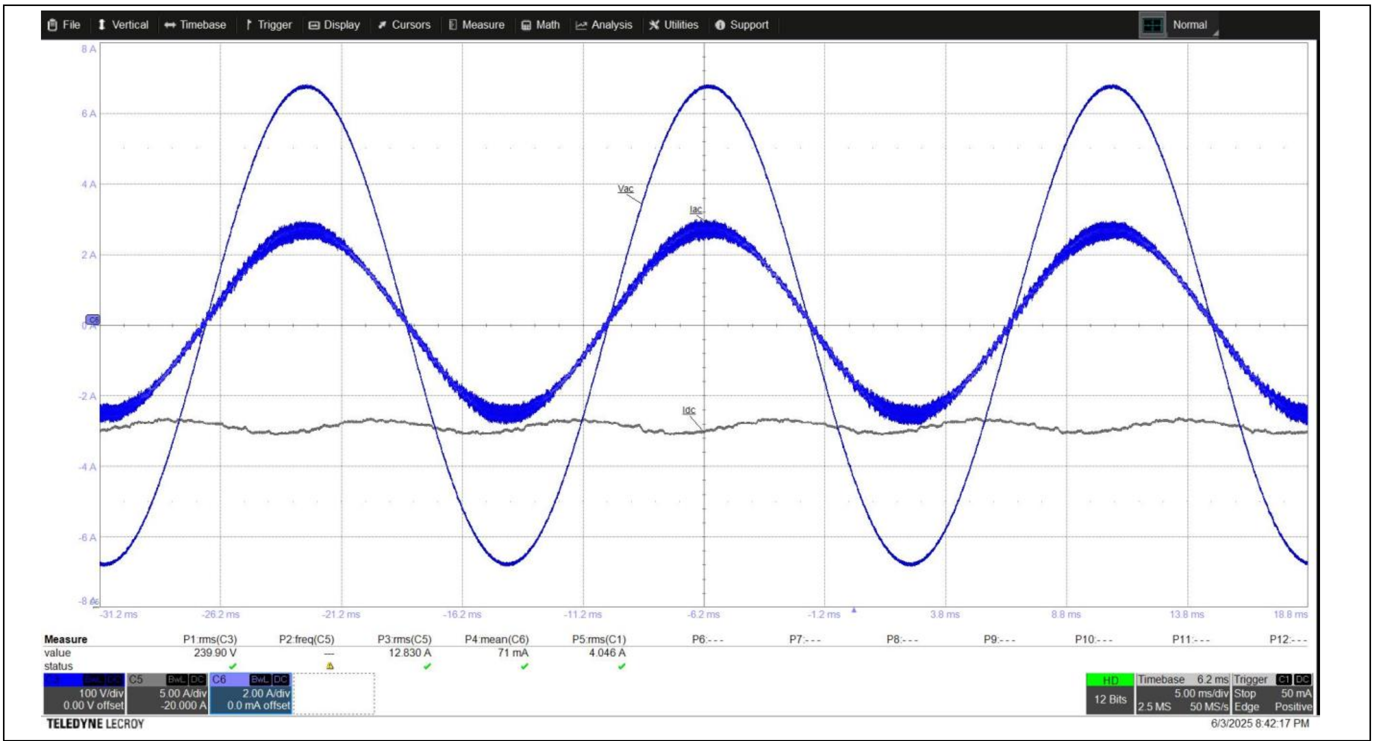


Figure 141 Load 450 W, PF 1.0 - output voltage (blue), output current (purple), DC input current (gray)

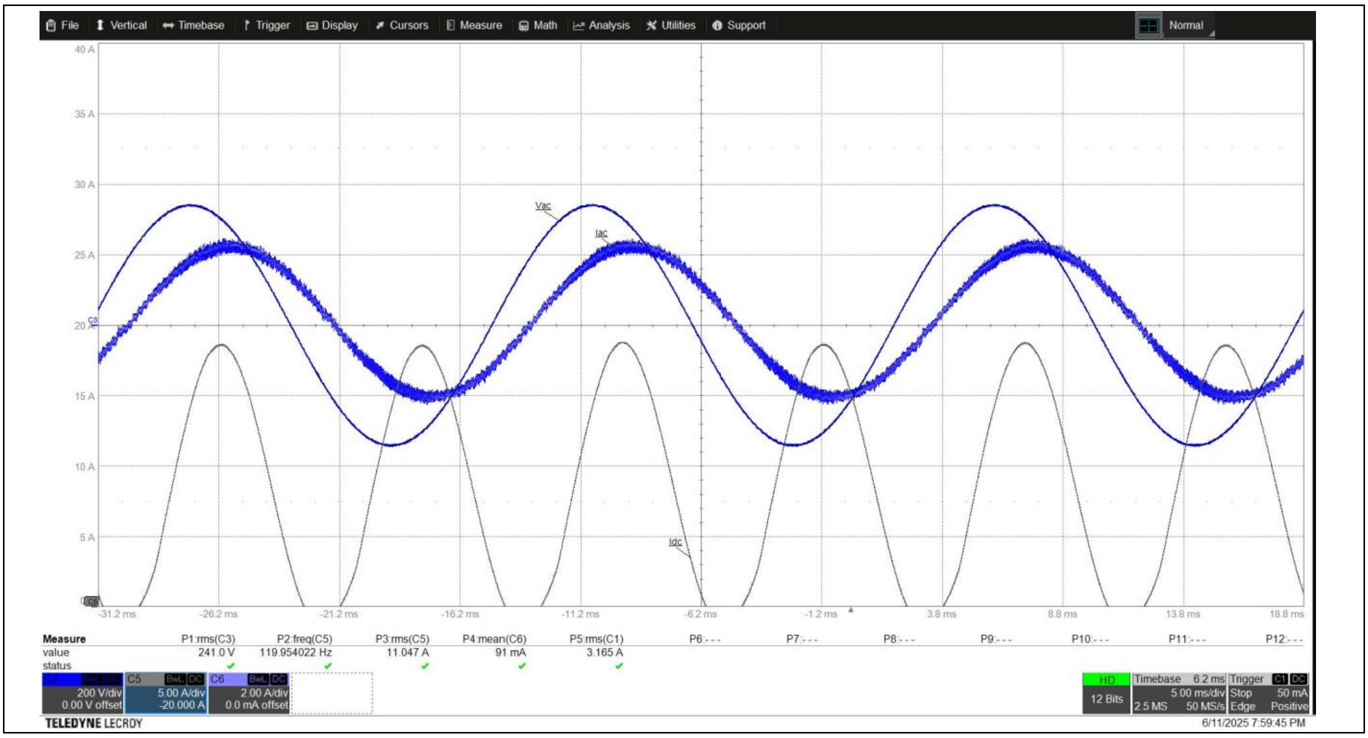


Figure 142 **Load 1.5 A_{RMS}, PF 0.8 (lagging) - output voltage (blue), output current (purple), DC input current (gray)**

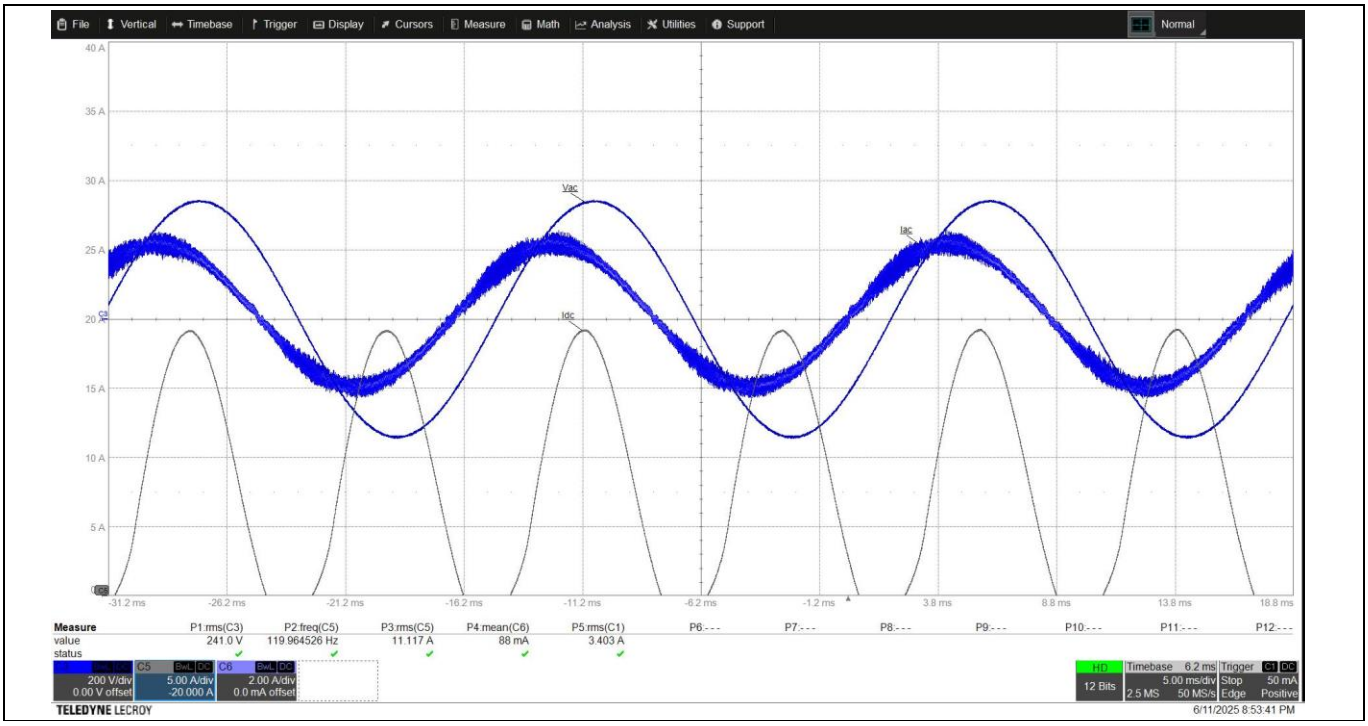


Figure 143 **Load 1.5 A_{RMS}, PF -0.8 (leading) - output voltage (blue), output current (purple), DC input current (gray)**

11.3.2.2 Input 50 VDC

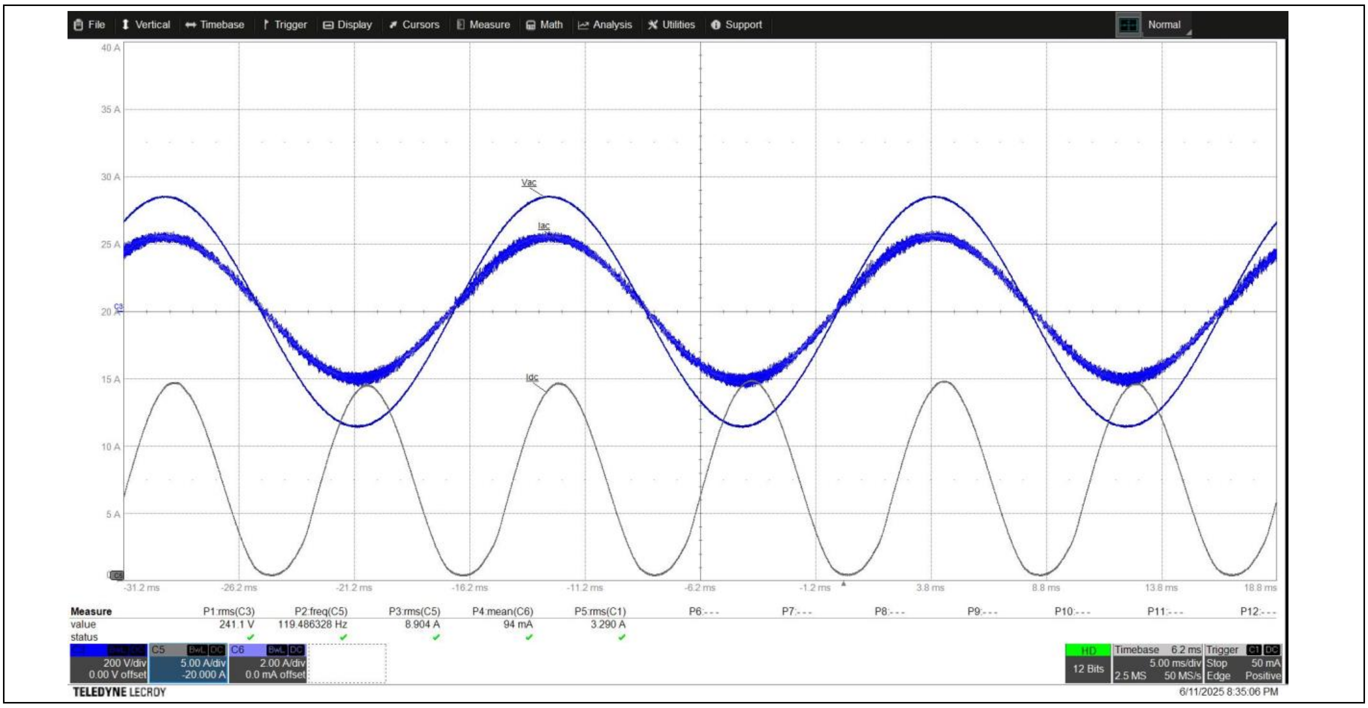


Figure 144 Load 1.5 A_{RMS}, PF 1.0 - output voltage (blue), output current (purple), DC input current (gray)

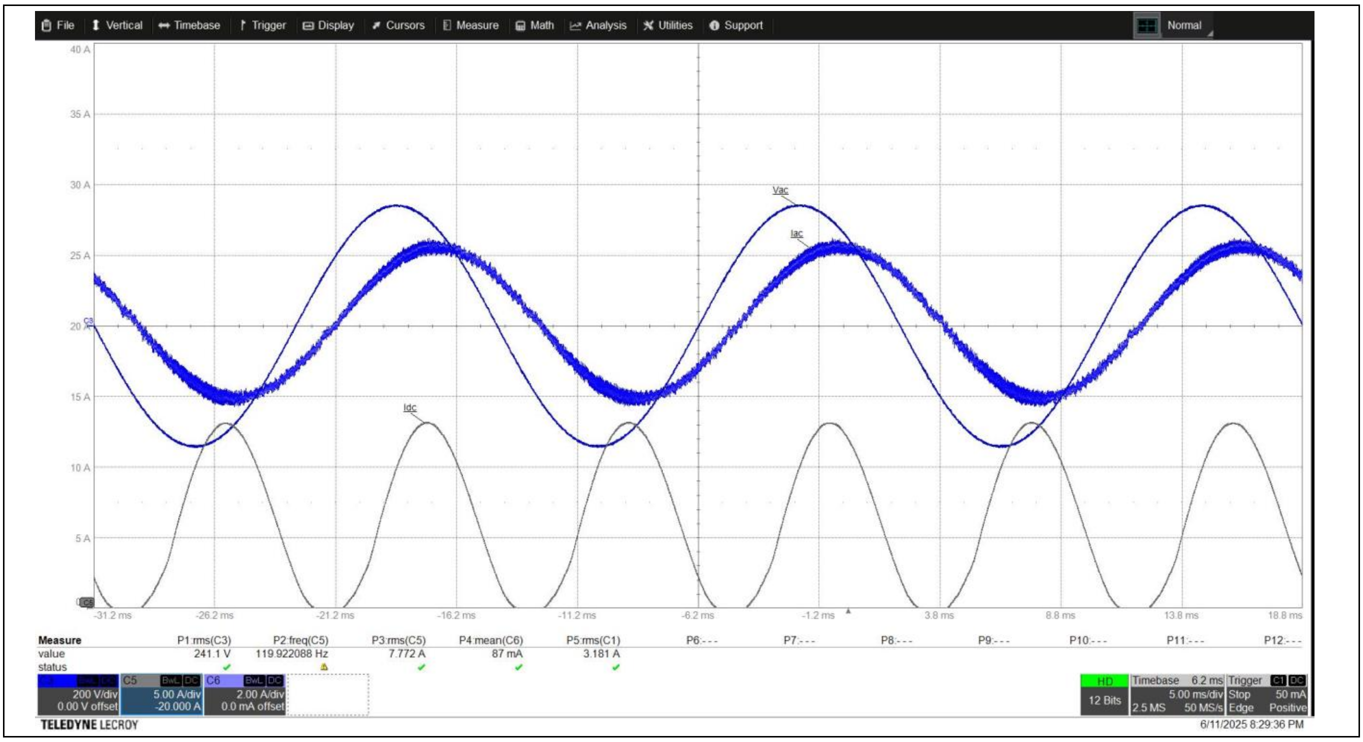


Figure 145 Load 1.5 A_{RMS}, PF 0.8 (lagging) - output voltage (blue), output current (purple), DC input current (gray)

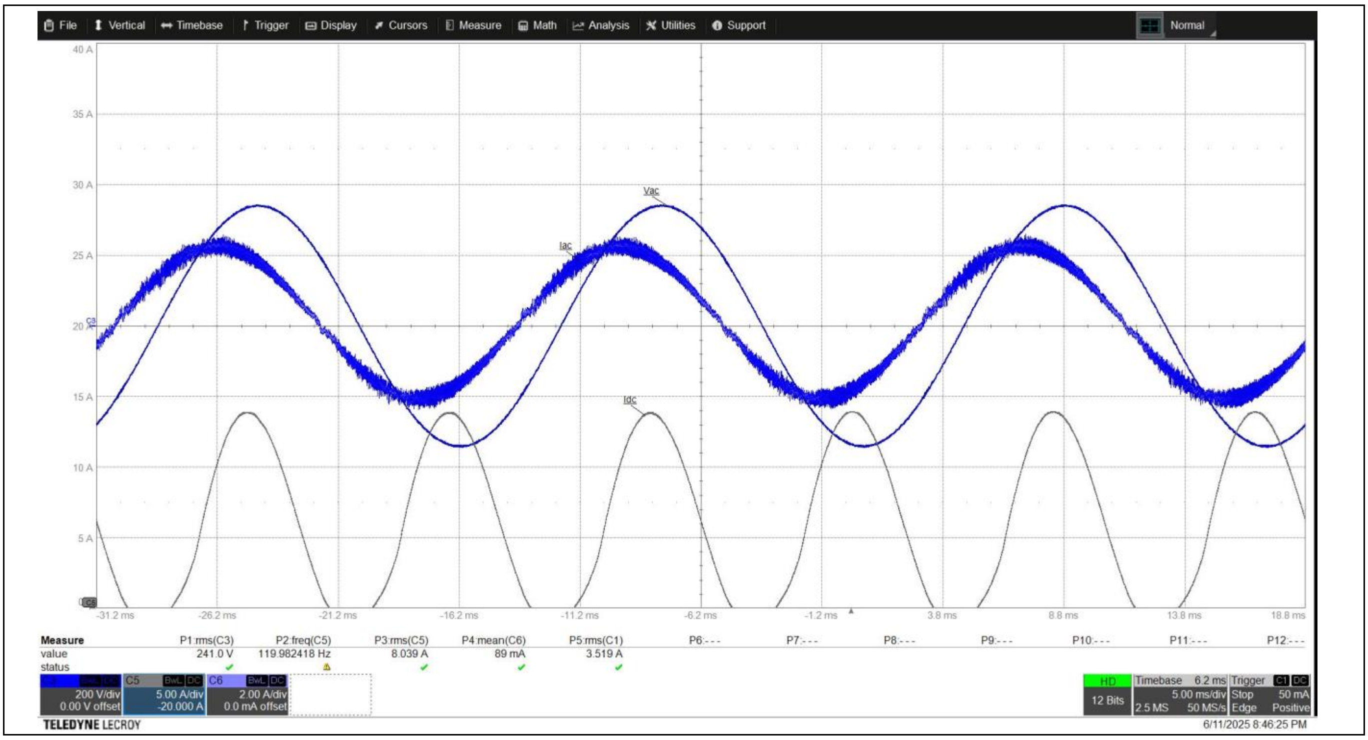


Figure 146 Load 1.5 A_{RMS}, PF -0.8 (leading) - output voltage (blue), output current (purple), DC input current (gray)

11.3.3 On-grid operation in burst mode

When burst mode is enabled through the GUI, the operating waveforms at light load can be seen as follows:

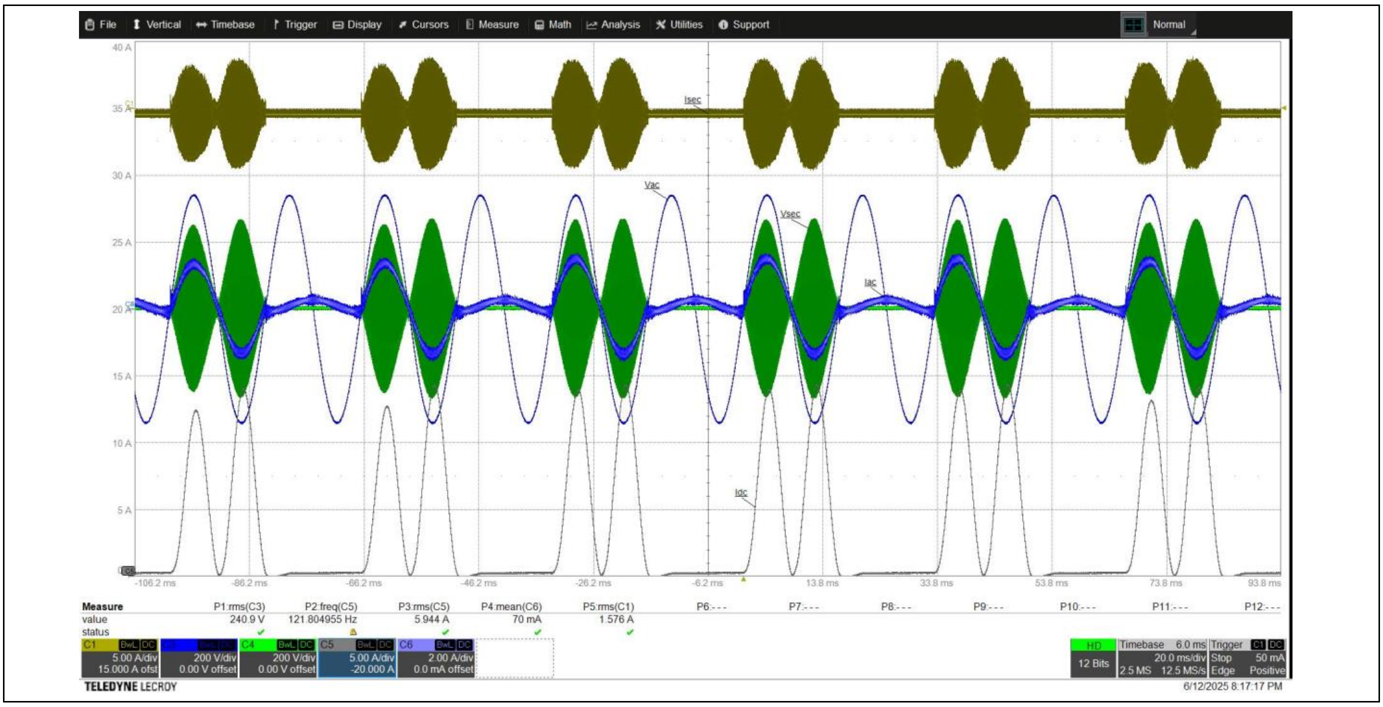


Figure 147 Load 0.5 A_{RMS}, PF 1.0 - grid voltage (blue), output current (purple), DC input current (gray), secondary voltage (green), secondary current (brown)

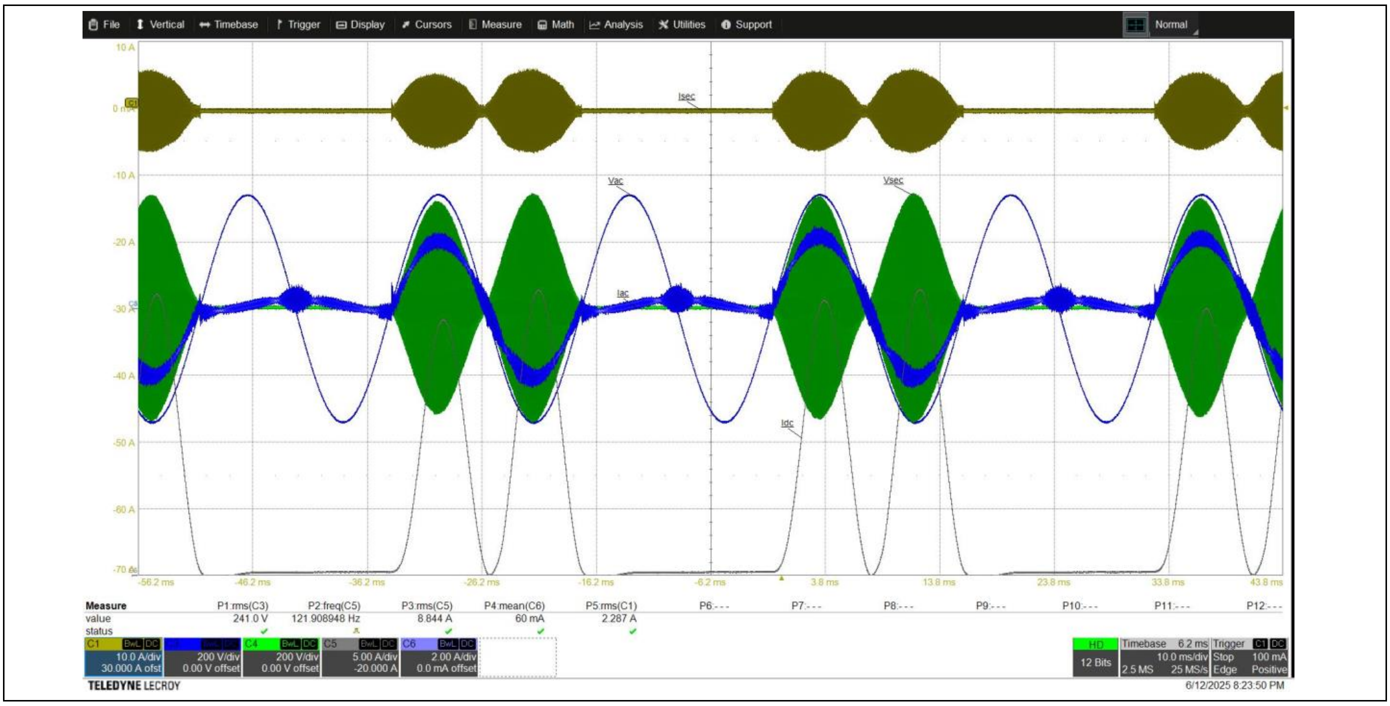


Figure 148 Load 0.75 A_{RMS}, PF 1.0 - grid voltage (blue), output current (purple), DC input current (gray), secondary voltage (green), secondary current (brown)

12 Conclusion

The REF_500W_CYCLO_BDSGAN reference design meets the design objectives. Control of the cyclo-microinverter board is realized through the dedicated GUI tool, which has been used to demonstrate the different operating modes. The test results demonstrate a peak efficiency greater than 97 percent and a CEC-weighted efficiency of 96.7 percent. The AC current THD is well below the 5 percent maximum limit for operation from 50 to 100 percent of full rated load. The component temperature reaches no more than 65 degrees Celsius at maximum load in an ambient temperature of approximately 20 degrees after more than 30 minutes of operation where thermal equilibrium has been reached.

Excellent performance has been achieved by maintaining ZVS over a wide operating range, which is made possible in part due to the benefits of HV GaN with its low and voltage stable C_{OSS} combined with low conduction losses. This is further aided by the OptiMOS™ 6 power MOSFETs used in the primary side based on Infineon's thin wafer technology enabling >24% lower $R_{DS(on)}$ and ~40% improved $FOM_{Qg} \times R_{DS(on)}$ and $FOM_{Qgd} \times R_{DS(on)}$ compared against the previous generation.

Burst mode operation has also been demonstrated at low output conditions, which can be enabled to maintain high efficiency during periods of reduced sunlight.

The control implementation based on the PSOC™ Control C3 MCU with Infineon’s firmware solution has demonstrated stable, accurate and reliable operation over a wide range of line, load and power factor conditions with protection against fault conditions successfully implemented. MPPT efficiency is measured at higher than 99 percent for loads above 50% over a wide input voltage range.

The output current and power factor can be changed while the unit is operating in grid tied mode using the Infineon PC based GUI tool without causing any fault or damage to the system. It is also possible to change the DC input voltage and AC line voltage during operation without causing any disruption.

The protection schemes implemented enable the unit to shut down safely if a fault condition or unexpected disconnect occurs.

In conclusion, the REF_500W_CYCLO_BDSGAN offers a reliability, high-efficiency solution based on a cycloinverter topology, with performance comparable to state-of-the-art microinverters currently in the market.

13 Related resources

- CoolGaN™ GaN bidirectional switches webpage
- CoolGaN™ GaN developer community
- OptiMOS™ 6 power MOSFET 80 V webpage
- MOSFET (Si/SiC) developer community
- PSOC™ Control C3 Main Line MCUs webpage
- PSOC™ Control C3 developer community

References

[1] Infineon Technologies AG: *Considerations and guidelines for using high-voltage CoolGaN™ switches in power systems,* Available online

[2] Infineon *Technologies AG: CoolGaN™ Bidirectional* switch *650 V G5: Fundamentals and design considerations,* Available online

[3] Imperix: *Proportional resonant controller (TN110)*; Available online

[4] Imperix: *SOGI PLL (TN104)*; Available online

[5] Infineon Technologies: *PSOC™ Control C3 - PSC3P5xD, PSC3M5xD datasheet*; Available online

[6] Infineon Technologies: *CoolGaN™ BDS 650 V G5 datasheet*; Available online

[7] Infineon Technologies: *ISC014N08NM6 datasheet*; Available online

[8] Infineon Technologies: *EiceDRIVER™ 1EDNx550 datasheet*; Available online

[9] Infineon Technologies: *EiceDRIVER™ 2EDL803X datasheet*; Available online

[10] Infineon Technologies: *EiceDRIVER™ 2EDR8259H, 2EDRx259X, 2EDRx258X datsheet*; Available online

Revision history

Document revision	Date	Description of changes
V 1.0	2025-08-19	Initial release
V 1.1	2025-09-18	Correction to figures 10 and 13

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2025-09-18

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

AN211819