Customer Information Notification

202603012I : PCA9617A Datasheet Update

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Issue Date: Jun 05, 2026 **Effective Date:** Jun 08, 2026

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Management summary

NXP Semiconductor announces a PCA9617 datasheet update update

Change Category

[ ]Wafer Fab Process	[ ]Assembly Process	[ ]Product Marking	[ ]Test Process	[ ]Design
[ ]Wafer Fab Materials	[ ]Assembly Materials	[ ]Mechanical Specification	[ ]Test Equipment	[ ]Errata
[ ]Wafer Fab Location	[ ]Assembly Location	[ ]Packing/Shipping/Labeling	[ ]Test Location	[ ]Electrical spec./Test coverage
[ ]Firmware	[X]Other: Datasheet			

Notification Overview

Description

PCA9617A Rev. 1.1: https://www.nxp.com/docs/en/data-sheet/PCA9617A.pdf

The datasheet was updated to correct the placement of footnotes in Table 5.
There is no change in part or part performance.

Reason

The footnote [2] was added to both VCC(A) and VCC(B) parameters to clearly indicate the intended reference and avoid potential misinterpretation.

Identification of Affected Products

Product identification does not change

Anticipated Impact on Form, Fit, Function, Reliability or Quality

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No Impact on form, fit, function, reliability or quality

Data Sheet Revision

A new data sheet will be issued

Additional information

Additional documents: view online

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PCA9617A

Level Translating Fm+ I^2C-bus Repeater

Rev. 1.1 — 16 March 2026 **Product data sheet**

1 General description

The PCA9617A is a CMOS-integrated circuit that provides level shifting between low voltage (0.8 V to 5.5 V) and higher voltage (2.2 V to 5.5 V) Fast-mode Plus I^2C-bus or SMBus applications. While retaining all the operating modes and features of the I^2C-bus system during the level shifts, it also permits extension of the I^2C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, therefore enabling two buses of 540 pF at 1 MHz or up to 4000 pF at lower speeds. Using the PCA9617A enables the system designer to isolate two halves of a bus for both voltage and capacitance. The SDA and SCL pins are overvoltage tolerant and are high-impedance when the PCA9617A is unpowered.

The 2.2 V to 5.5 V bus port B drivers have the static level offset, while the adjustable voltage bus port A drivers eliminate the static offset voltage. It results in a LOW on the port B translating into a nearly 0 V LOW on the port A, which accommodates the smaller voltage swings of lower voltage logic.

The static offset design of the port B PCA9617A I/O drivers prevents them from being connected to the static or incremented offset of other bus buffers. Port A of two or more PCA9617As can be connected, however, to allow a star topography with port A on the common bus. Port A can then be connected directly to any other buffer with static or incremented offset outputs. Multiple PCA9617As can be connected in series, port A to port B, with no build-up in offset voltage with only time of flight delays to consider.

The PCA9617A drivers are kept disabled unless $V_{CC(A)}$ is above 0.8 V and $V_{CC(B)}$ is above 2.2 V. The EN pin is referenced to $V_{CC(B)}$ and can also be used to turn the drivers on and off under system control.

Note: *Only change the state of enable pin when the bus is idle.*

The output pulldown on the port B internal buffer LOW is set for approximately 0.55 V, while the input threshold of the internal buffer is set about 90 mV lower (0.45 V). When the port B I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. It prevents a latching condition from occurring. The output pulldown on port A drives a hard LOW. The input level is set at $0.35V_{CC(A)}$ to accommodate the need for a lower LOW level in systems where the low voltage side supply voltage is as low as 0.8 V.

2 Features and benefits

- A two-channel, bidirectional buffer isolates capacitance, allowing 540 pF on either side of the device at 1 MHz and up to 4000 pF at lower speeds
- Voltage level translation from 0.8 V to 5.5 V and from 2.2 V to 5.5 V
- Footprint and functional replacement for PCA9517A at Fast-mode speeds
- Port A operating supply voltage range of 0.8 V to 5.5 V with normal levels
- Port B operating supply voltage range of 2.2 V to 5.5 V with static offset level
- 5 V tolerant I^2C-bus and enable pins
- 0 Hz to 1000 kHz clock frequency (the maximum system operating frequency can be less than 1000 kHz because of the delays added by the repeater)
- Active HIGH repeater enables input referenced to $V_{CC(B)}$
- Open-drain input/outputs
- Latching free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates Standard-mode, Fast-mode and Fast-mode Plus I^2C-bus devices, SMBus (standard and high power mode), PMBus, and multiple controllers
- Powered-off high-impedance I^2C-bus pins
- ESD protection exceeds 5500 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78, which exceeds 100 mA
- Packages offered: TSSOP8 and HWSON8

3 Ordering information

Table 1 describes the ordering information for PCA9617A.

Table 1. Ordering information

T_{amb} = -40 °C to +85 °C.

Type number	Topside mark	Package		
		Name	Description	Version
PCA9617ADP	P617A	TSSOP8[1]	Plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCA9617ATP	P7A	HWSON8	Plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 2 × 3 × 0.8 mm	SOT1069-2

[1] Also known as MSOP8.

3.1 Ordering options

Table 2 describes the ordering options for PCA9617A.

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCA9617ADP	PCA9617ADPJ	TSSOP8	Reel 13" Q1/T1 *standard mark SMD	2500	T_{amb} = -40 °C to +85 °C
PCA9617ATP	PCA9617ATPZ	HWSON8	Reel 7" Q2/T3 *standard mark	4000	T_{amb} = -40 °C to +85 °C

4 Functional diagram

Figure 1 shows the functional diagram of PCA9617A.

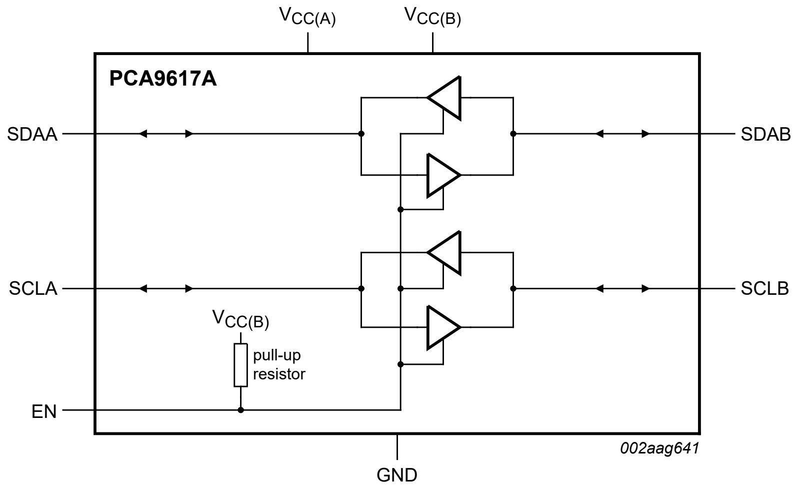


Figure 1. Functional diagram of PCA9617A

5 Pinning information

This section provides the pin configuration and description of TSSOP8 and HWSON8 packages.

5.1 Pinning

Figure 2 and Figure 3 show the pinning for TSSOP8 and HWSON8 packages, respectively.

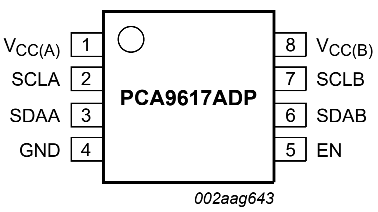


Figure 2. Pin configuration for TSSOP8 (MSOP8)

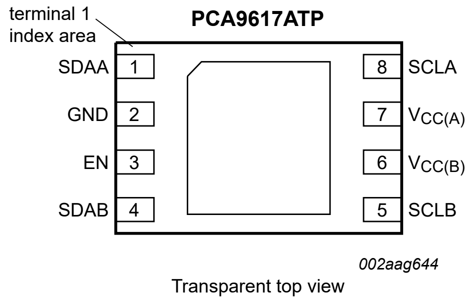


Figure 3. Pin configuration for HWSON8

5.2 Pin description

Table 3 provides detailed description of various pins on PCA9617A.

Table 3. Pin description

Symbol	Pin		Description
	TSSOP8	HWSON8	
$V_{CC(A)}$	1	7	Port A supply voltage (0.8 V to 5.5 V)
SCLA	2	8	Serial clock port A bus
SDAA	3	1	Serial data port A bus
GND	4	2[1]	Supply ground (0 V)
EN	5	3	Active HIGH repeater enable input
SDAB	6	4	Serial data port B bus
SCLB	7	5	Serial clock port B bus
$V_{CC(B)}$	8	6	Port B supply voltage (2.2 V to 5.5 V)

[1] HWSON8 package die supply ground is connected to both GND pin and exposed center pad. GND pin must be connected to the supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad must be soldered to the board using a corresponding thermal pad on the board. For proper head conduction through the board, thermal vias must be incorporated in the printed-circuit board in the thermal pad region.

6 Functional description

Refer to Figure 1.

The PCA9617A enables I^2C-bus or SMBus translation down to $V_{CC(A)}$ as low as 0.8 V without degradation of system performance. The PCA9617A contains two bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage (as low as 0.8 V) and a 2.5 V, 3.3 V, or 5 V I^2C-bus or SMBus. All inputs and I/Os are overvoltage tolerant to 5.5 V even when the device is unpowered ($V_{CC(B)}$ and/or $V_{CC(A)}$ = 0 V). The PCA9617A includes a power up circuit that keeps the output drivers turned off until $V_{CC(B)}$ is above 2.2 V and until after the internal reference circuits have settled ~400 μs, and the $V_{CC(A)}$ is above 0.8 V. $V_{CC(B)}$ and $V_{CC(A)}$ can be applied in any sequence at power up. After power up and with the enable (EN) HIGH, a LOW level on port A (below 0.3$V_{CC(A)}$) turns on the corresponding port B driver (either SDA or SCL) and drives port B down to about 0.55 V. When port A rises above 0.3$V_{CC(A)}$, the port B pulldown driver is turned off and the external pullup resistor pulls the pin HIGH. When port B falls first and goes below 0.4 V, the port A driver is turned on and port A pulls down to ~0 V. The port A pulldown is not enabled unless the port B voltage goes below 0.4 V. If the port B low voltage goes below 0.4 V, the port B pulldown driver is enabled and port B can only rise to 0.55 V until port A rises above 0.3$V_{CC(A)}$. Now, port B continues to rise, being pulled up by the external pullup resistor. The $V_{CC(A)}$ is only used to provide the 0.35$V_{CC(A)}$ reference to the port A input comparators and for the power good detect circuit. The PCA9617A includes a $V_{CC(A)}$ overvoltage disable that turns off the channel when 0.4$V_{CC(A)}$ + 0.8 V > $V_{CC(B)}$. The PCA9617A logic and all I/Os are powered by the $V_{CC(B)}$ pin.

6.1 Enable

The EN pin is active HIGH with thresholds referenced to $V_{CC(B)}$ and an internal pullup to $V_{CC(B)}$ that maintains the device active unless the user selects to disable the repeater to isolate a badly behaved target on power up until after the system power up reset. It must never change state during an I^2C-bus operation because disabling during a bus operation hangs the bus and enabling part way through a bus cycle can confuse the I^2C-bus parts being enabled. The enable does not switch the internal reference circuits so the ~400 μs delay is only seen when $V_{CC(B)}$ comes up.

The enable pin only changes state when the global bus and the repeater port are in an idle state to prevent system failures.

6.2 I^2C-bus systems

As with the standard I^2C-bus system, pullup resistors are required to provide the logic HIGH levels on the buffered bus (the standard open-collector configuration of I^2C-bus). The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. This part is designed to work with Standard mode, Fast-mode, and Fast-mode Plus I^2C-bus devices in addition to SMBus devices. Standard mode and Fast-mode I^2C-bus devices only specify 3 mA output drive, which limits the termination current to 3 mA in a generic I^2C-bus system where Standard-mode devices, Fast-mode devices, and multiple controllers are possible. When only Fast-mode Plus devices are used with 30 mA at 5 V drive strength, the lower value pullup resistors can be used. The B-side RC cannot be less than 67.5 ns because shorter RCs increase the turnaround bounce when the B-side transitions from being externally driven to pulled down by its offset buffer.

For additional information on sizing resistors and precautions while using more than one PCA9617A in a system or using PCA9617A with other bus buffers, refer *“I2C/SMBus Repeaters, Hubs, and Expanders”* [AN255].

7 Application design-in information

A typical application is shown in Figure 4. In this example, the system controller is running on a 3.3 V I²C-bus while the target is connected to a 1.2 V bus. Both buses run at 1000 kHz. Controller devices can be placed on either bus.

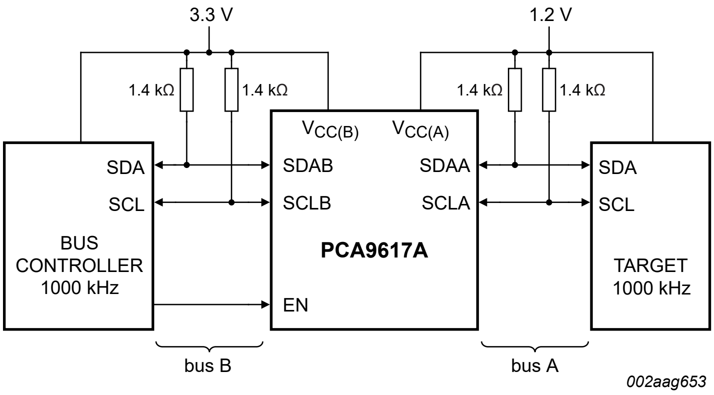


Figure 4. Typical application

The PCA9617A is 5 V tolerant. Therefore, it does not require any additional circuitry to translate between 0.8 V to 5.5 V bus voltages and 2.2 V to 5.5 V bus voltages.

When port A of the PCA9617A is pulled LOW by a driver on the I²C-bus, a comparator detects the falling edge when it goes below $0.3V_{CC(A)}$ and causes the internal driver on port B to turn on, causing port B to pull down to about 0.5 V. When port B of the PCA9617A falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on port A to turn on and pull the port A pin down to the ground. To illustrate what is seen in a typical application, refer to Figure 8 and Figure 9. If the bus controller in Figure 4 is to write to the target through the PCA9617A, waveforms shown in Figure 8 are observed on the A bus. This looks like a normal I²C-bus transmission except that the HIGH level can be as low as 0.8 V, and the turn-on and turn-off of the acknowledge signals are slightly delayed.

The internal comparator requires that $0.4 \times V_{CC(A)}$ is less than or equal to $V_{CC(B)}$ - 0.8 V for the device to operate. Since A port is 5 V tolerant, the $V_{CC(A)}$ can be lowered to support device spectrum while still supporting 5 V signals on the A port.

On the B bus side of PCA9617A, the clock and data lines have a positive offset from ground equal to the V_{OL} of the PCA9617A. After the eighth clock pulse, the data line is pulled to V_{OL} of the target device, which is very close to the ground in this example. At the end of the acknowledge, the level rises only to the LOW level set by the driver in the PCA9617A for a short delay while the A bus side rises above $0.3V_{CC(A)}$ then it continues HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the B bus side at the input of the PCA9617A (V_{IL}) is at or below 0.4 V to be recognized by the PCA9617A and then transmitted to the A bus side.

Multiple PCA9617A port A sides can be connected in a star configuration (Figure 5), allowing all nodes to communicate with each other.

Multiple PCA9617As can be connected in series (Figure 6) as long as port A is connected to port B. I²C-bus target devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

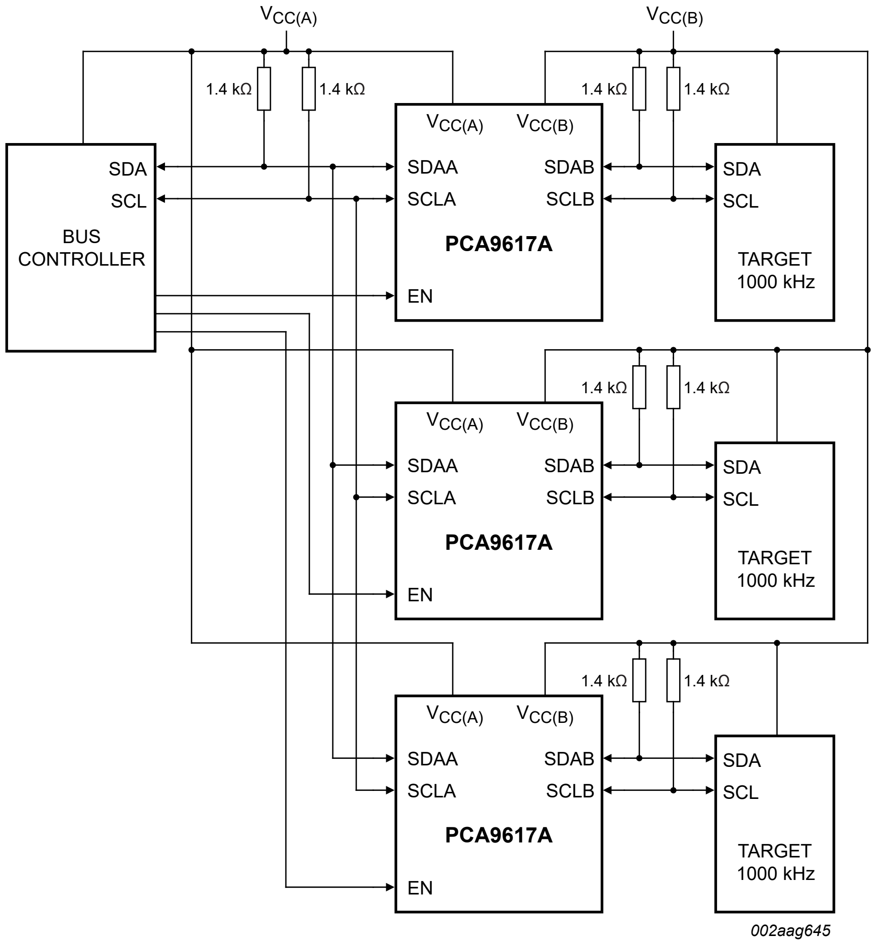
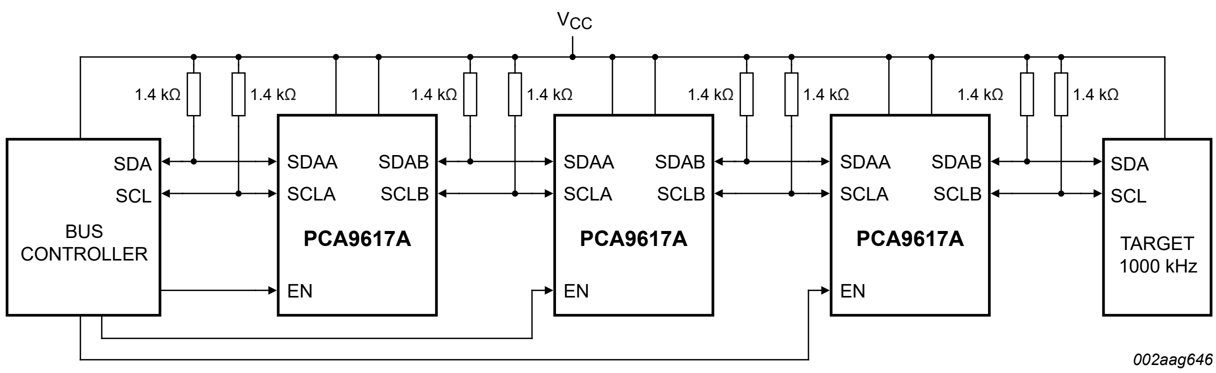
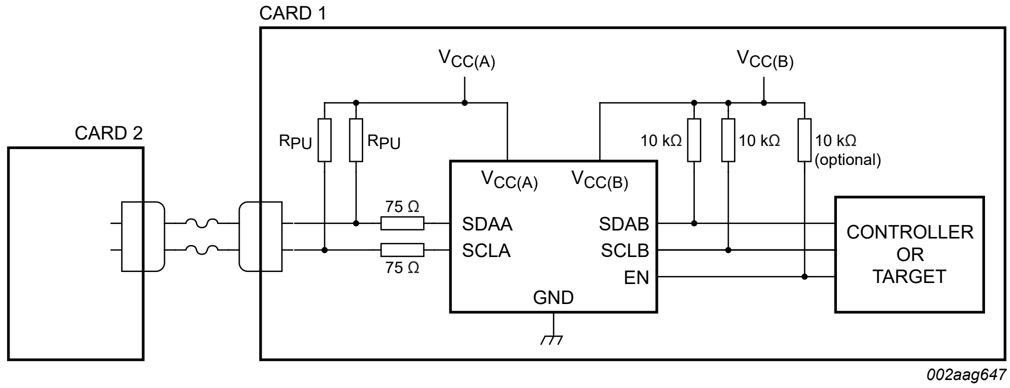


Figure 5. Typical star application



Decoupling capacitors is not shown for simplicity, but they are required. It is especially important that the decoupling for the PCA9617A $V_{CC(B)}$ is close to the $V_{CC(B)}$ pin.

Figure 6. Typical series application



Decoupling capacitors is not shown for simplicity, but they are required. It is especially important that the decoupling for the PCA9617A $V_{CC(B)}$ is close to the $V_{CC(B)}$ pin.

Figure 7. Typical application of PCA9617A driving a short cable

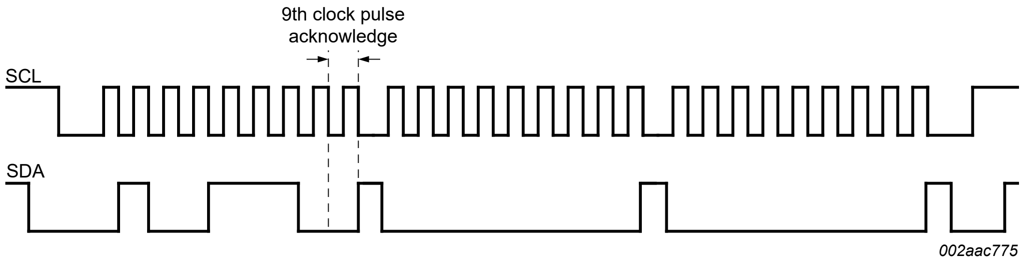


Figure 8. Bus A (0.8 V to 5.5 V bus) waveform

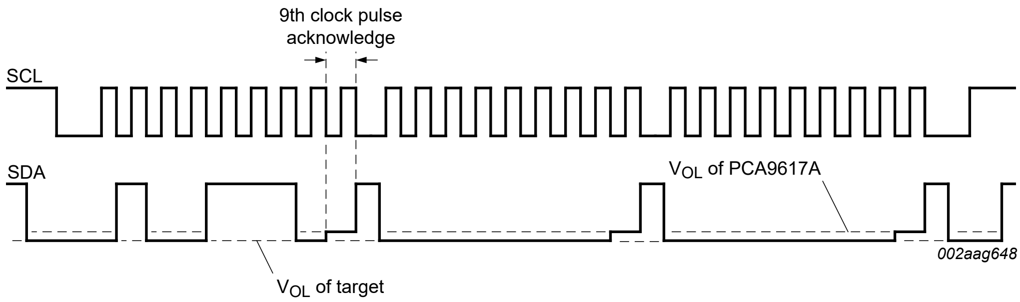


Figure 9. Bus B (2.2 V to 5.5 V) waveform

8 Limiting values

Table 4 describes the limiting values of PCA9617A.

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(B)}$	Supply voltage port B		-0.5	+7	V
$V_{CC(A)}$	Supply voltage port A	Adjustable	-0.5	+7	V
$V_{I/O}$	Voltage on an input/output pin	Port A and port B; enable pin (EN)	-0.5	+7	V
$I_{I/O}$	Input/output current	Port A; port B	-	50	mA
I_I	Input current	EN, $V_{CC(A)}$, $V_{CC(B)}$, GND	-	50	mA
P_{tot}	Total power dissipation		-	100	mW
T_{stg}	Storage temperature		-55	+125	°C
T_{amb}	Ambient temperature	Operating in free air	-40	+85	°C
T_j	Junction temperature		-	+125	°C

9 Static characteristics

This section describes the static characteristics of PCA9617A.

Table 5. Static characteristics

$V_{CC(A)}$ = 0.8 V to 5.5 V[1]; $V_{CC(B)}$ = 2.2 V to 5.5 V; GND = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified. Typical values measured with $V_{CC(A)}$ = 0.95 V and $V_{CC(B)}$ = 2.5 V at 25 °C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
$V_{CC(B)}$	Supply voltage port B	[2]	2.2	-	5.5	V
$V_{CC(A)}$	Supply voltage port A	[2] [3]	0.8	-	5.5	V
$I_{CC(A)}$	Supply current port A	$V_{CC(A)}$ = 0.95 V	-	-	8	μA
		$V_{CC(A)}$ = 5.5 V	-	-	50	μA
$I_{CCH(B)}$	Port B HIGH-level supply current	$V_{CC(B)}$ = 5.5 V; SDAn = SCLn = $V_{CC(n)}$	-	1.5	2.5	mA
$I_{CCL(B)}$	Port B LOW-level supply current	$V_{CC(B)}$ = 5.5 V; one SDA and one SCL = GND; other SDA and SCL open (with pullup resistors)	-	1.7	2.9	mA
Input and output SDAB and SCLB						
V_{IH}	HIGH-level input voltage		0.7$V_{CC(B)}$	-	5.5	V
V_{IL}	LOW-level input voltage		-0.5	-	+0.4	V
V_{IK}	Input clamping voltage	I_I = -18 mA	-1.2	-	-0.3	V
I_{LI}	Input leakage current	V_I = 5.5 V	-	-	±1	μA
I_{IL}	LOW-level input current	SDA, SCL; V_I = 0.2 V	-	-	10	μA
V_{OL}	LOW-level output voltage	I_{OL} = 150 μA at $V_{CC(B)}$ = 2.2 V [4]	0.47	-	-	V
		I_{OL} = 13 mA at $V_{CC(B)}$ = 2.2 V [5]	-	0.54	0.60	V
V_{OL}-V_{IL}	Difference between LOW-level output and LOW-level input voltage	V_{OL} at I_{OL} = 1 mA; guaranteed by design	60	90	160	mV
C_{io}	Input/output capacitance	V_I = 3 V or 0 V; $V_{CC(B)}$ = 3.3 V; EN = LOW	-	7	10	pF
		V_I = 3 V or 0 V; V_{CC} = 0 V	-	7	10	pF
Input and output SDAA and SCLA						
V_{IH}	HIGH-level input voltage		0.7$V_{CC(A)}$	-	5.5	V
V_{IL}	LOW-level input voltage	[6]	-0.5	-	+0.25$V_{CC(A)}$[7]	V
V_{IK}	Input clamping voltage	I_I = -18 mA	-1.2	-	-0.3	V
I_{LI}	Input leakage current	V_I = 5.5 V	-	-	±1	μA
I_{IL}	LOW-level input current	SDA, SCL; V_I = 0.2 V	-	-	10	μA
V_{OL}	LOW-level output voltage	I_{OL} = 13 mA; $V_{CC(B)}$ = 2.2 V	-	0.1	0.2	V
C_{io}	Input/output capacitance	V_I = 3 V or 0 V; V_{CC} = 3.3 V; EN = LOW	-	7	10	pF

Table 5. Static characteristics*...continued*

$V_{CC(A)}$ = 0.8 V to 5.5 V[1]; $V_{CC(B)}$ = 2.2 V to 5.5 V; GND = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified. Typical values measured with $V_{CC(A)}$ = 0.95 V and $V_{CC(B)}$ = 2.5 V at 25 °C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		V_I = 3 V or 0 V; V_{CC} = 0 V	-	7	10	pF
Enable						
V_{IL}	LOW-level input voltage		-0.5	-	+0.3$V_{CC(B)}$	V
V_{IH}	HIGH-level input voltage		0.7$V_{CC(B)}$	-	5.5	V
$I_{IL(EN)}$	LOW-level input current on pin EN	V_I = 0.2 V, EN; $V_{CC(B)}$ = 2.2 V	-18	-7	-4	μA
I_{LI}	Input leakage current		-1	-	+1	μA
C_i	Input capacitance	V_I = $V_{CC(B)}$	-	6	7	pF

[1] $V_{CC(A)}$ may be as high as 5.5 V for overvoltage tolerance but 0.4 $V_{CC(A)}$ + 0.8 V ≤ $V_{CC(B)}$ for the channels to be enabled and functional normally.
[2] Power supply decoupling capacitors must be present for both $V_{CC(A)}$ and $V_{CC(B)}$. The 0.1 μF decoupling for $V_{CC(B)}$ must be located near the $V_{CC(B)}$ pin.
[3] For part to function, 0.4 × $V_{CC(A)}$ must be equal or less than $V_{CC(B)}$ - 0.8 V. The voltage on the A port can still be up to 5.5 V without damage to the pins.
[4] Pullup must result in I_{OL} ≥ 150 μA.
[5] Guaranteed by design and characterization.
[6] V_{IL} for port A with envelope noise must be below 0.3$V_{CC(A)}$ for stable performance.
[7] When $V_{CC(A)}$ is less than 1 V, care is required to make certain that the system ground offset and noise are minimized such that there is a reasonable difference between the V_{IL} present at the PCA9617A A-side input and the 0.25$V_{CC(A)}$ input threshold.

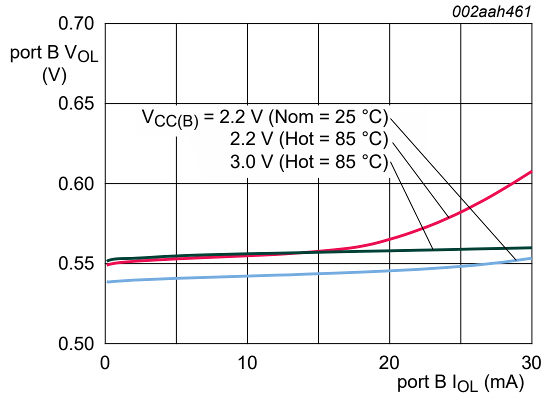


Figure 10. Port B V_{OL} versus I_{OL}

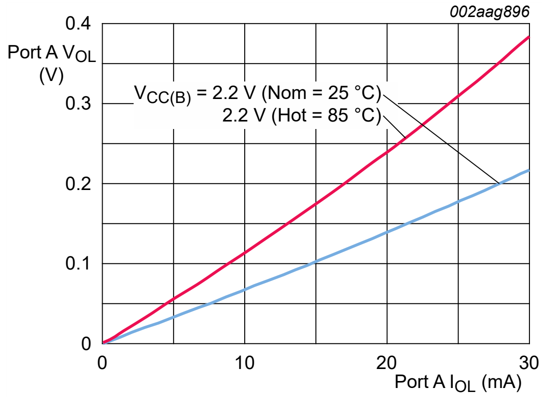
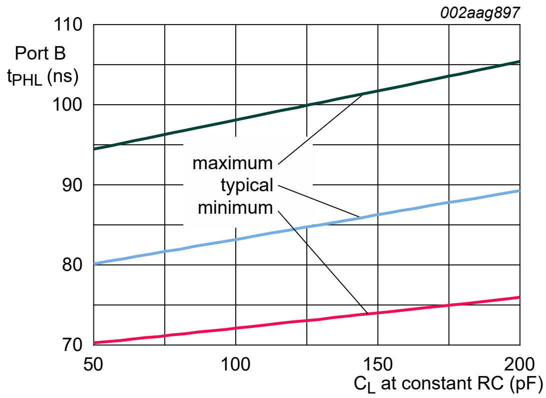


Figure 11. Port A V_{OL} versus I_{OL}



RC = 67.5 ns, $V_{CC(A)}$ = 0.95 V, $V_{CC(B)}$ = 2.5 V, and T_{amb} = 25 °C.

Figure 12. Nominal port B t_{PHL} with load capacitance at constant RC

10 Dynamic characteristics

Table 6 describes the dynamic characteristics of PCA9617A.

Table 6. Dynamic characteristics

$V_{CC(A)}$ = 0.8 V to 5.5 V[1]; $V_{CC(B)}$ = 2.2 V to 5.5 V; GND = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified. Typical values measured with $V_{CC(A)}$ = 0.95 V and $V_{CC(B)}$ = 2.5 V at 25 °C, unless otherwise noted[2][3]

Symbol	Parameter	Conditions	Min	Typ[4]	Max	Unit
t_{PLH}	LOW to HIGH propagation delay	Port B to port A; Figure 15	-42	-65	-103	ns
t_{PLH2}	LOW to HIGH propagation delay 2	Port B to port A; Figure 15 [5]	67	94	130	ns
t_{PHL}	HIGH to LOW propagation delay	Port B to port A; Figure 13	46	76	152	ns
t_{TLH}	LOW to HIGH output transition time	Port A; Figure 13 [6]	-	60	-	ns
SR_f	Falling slew rate	Port A; 0.7$V_{CC(A)}$ to 0.3$V_{CC(A)}$	0.022	0.037	0.11	V/ns
t_{PLH}	LOW to HIGH propagation delay	Port A to port B; Figure 14 [7]	40	60	102	ns
t_{PHL}	HIGH to LOW propagation delay	Port A to port B; Figure 14 [7]	63	80	173	ns
t_{TLH}	LOW to HIGH output Transition time	Port B; Figure 14 [6]	-	60	-	ns
SR_f	Falling slew rate	Port B; 0.7$V_{CC(B)}$ to 0.3 $V_{CC(B)}$	0.029	0.056	0.09	V/ns
t_{en}	Enable time	Quiescent - 0.3 V; EN HIGH to enable; Figure 16 [8]	-	-	100	ns
t_{dis}	Disable time	Quiescent + 0.3 V; EN LOW to disable; Figure 16 [8]	-	-	100	ns

[1] 0.4$V_{CC(A)}$ + 0.8 V ≤ $V_{CC(B)}$ for the channels to be enabled and function normally.
[2] Times are specified with loads of 1.35 kΩ pull-up resistance and 50 pF load capacitance on port A and port B, and a falling edge slew rate of 0.05 V/ns input signals.
[3] Pullup voltages are $V_{CC(A)}$ on port A and $V_{CC(B)}$ on port B.
[4] Typical values were measured with $V_{CC(A)}$ = 0.95 V, $V_{CC(B)}$ = 2.5 V at T_{amb} = 25 °C, unless otherwise noted.
[5] The t_{PLH2} delay data from port B to port A is measured at 0.45 V on port B to 0.5$V_{CC(A)}$ on port A.
[6] The t_{TLH} of the bus is determined by the pullup resistance (1.35 kΩ) and the total capacitance (50 pF).
[7] The proportional delay data from port A to port B is measured at 0.5$V_{CC(A)}$ on port A to 0.5$V_{CC(B)}$ on port B.
[8] The enable pin, EN, must only change state when the global bus and the repeater port are in an idle state.

10.1 AC waveforms

Figures below depict the AC waveforms associated with PCA9617A.

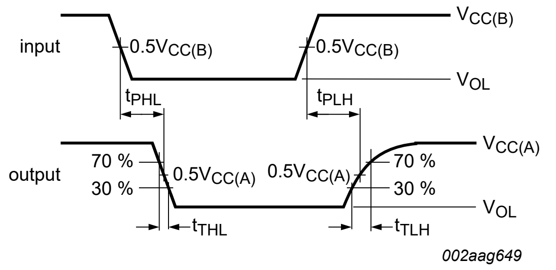


Figure 13. Propagation delay and transition times; port B to port A

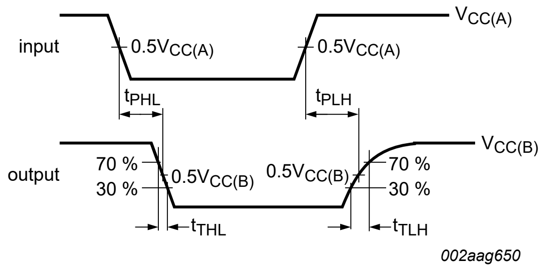


Figure 14. Propagation delay and transition times; port A to port B

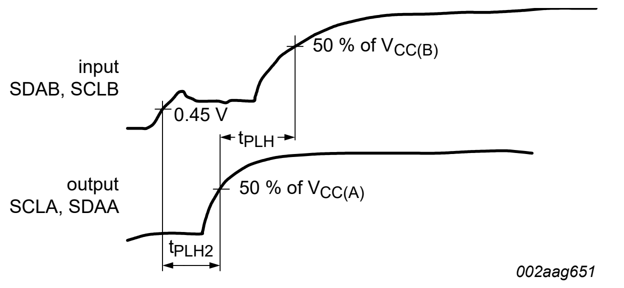


Figure 15. Propagation delay

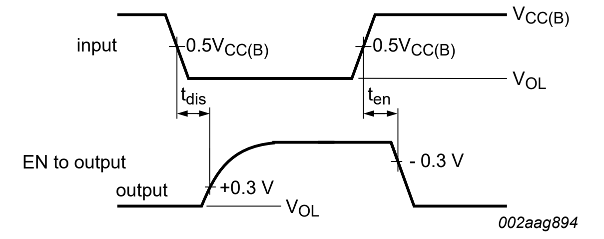
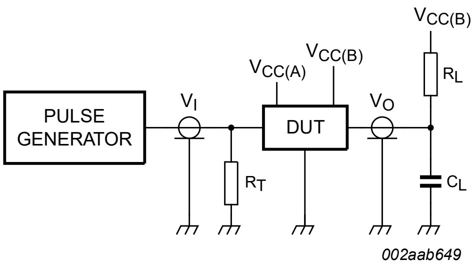


Figure 16. Enable and disable times

11 Test information

Figure 17 describes testing information associated with PCA9617A.



R_L = load resistor; 1.35 kΩ on port A and port B

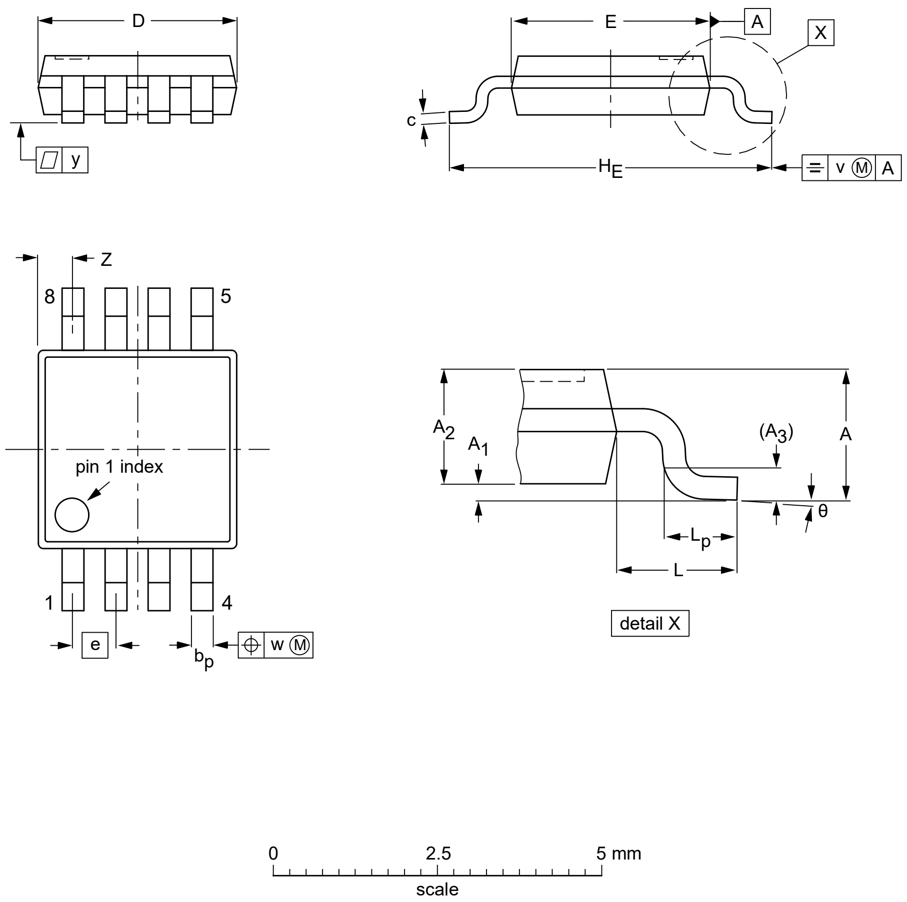
C_L = load capacitance; includes jig and probe capacitance (50 pF)

R_T = termination resistance; must be equal to Z_o of pulse generators.

Figure 17. Test circuit for open-drain outputs

12 Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

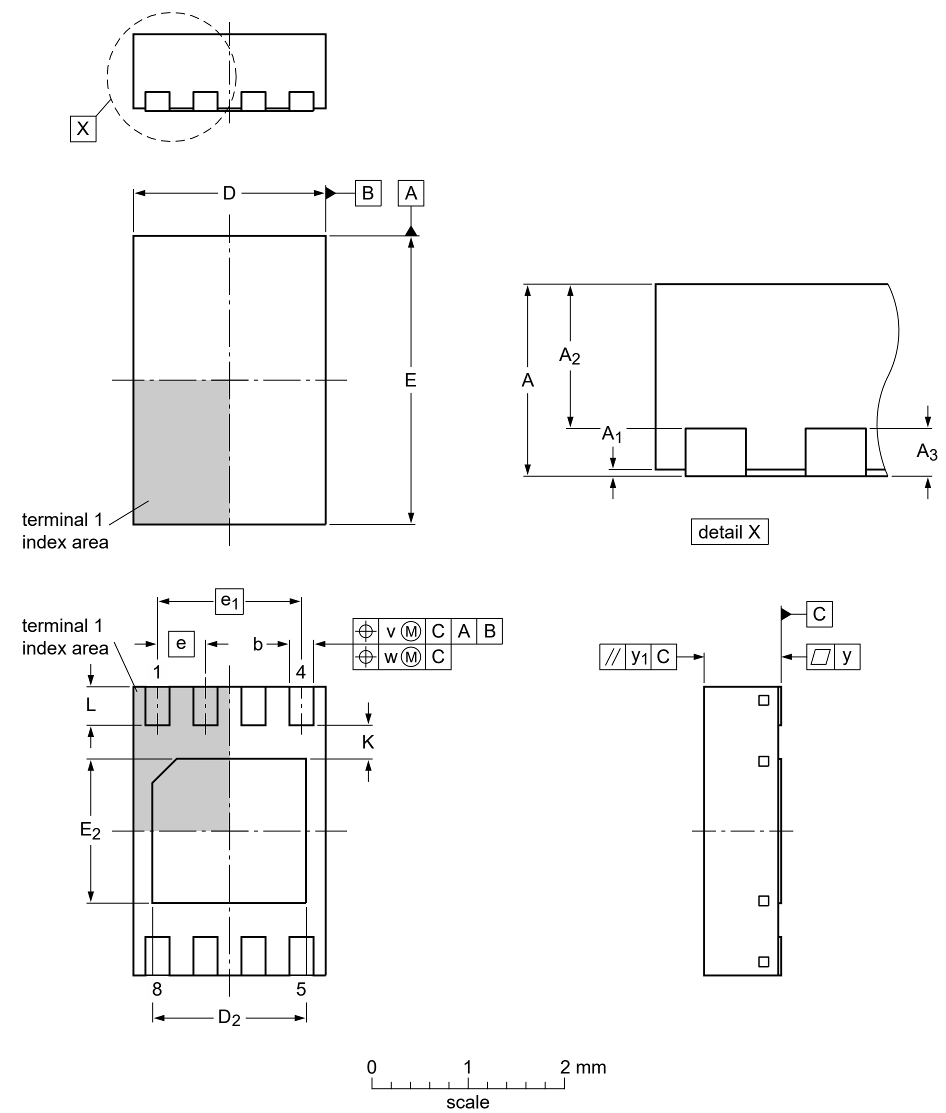
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Figure 18. Package outline SOT505-1 (TSSOP8)

HWSON8: plastic thermal enhanced very very thin small outline package; no leads; 8 terminals; body 2 x 3 x 0.75 mm **SOT1069-2**



Dimensions

Unit		A(1)	A_1	A_2	A_3	b	D(1)	D_2	E(1)	E_2	e	e_1	K	L	v	w	y	y_1
mm	max	0.80	0.05	0.65		0.30	2.1	1.6	3.1	1.6			0.40	0.45				
	nom	0.75	0.02	0.55	0.2	0.25	2.0	1.5	3.0	1.5	0.5	1.5	0.35	0.40	0.1	0.05	0.05	0.05
	min	0.70	0.00	0.45		0.18	1.9	1.4	2.9	1.4			0.30	0.35				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1069-2_po

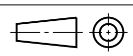
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1069-2	- - -	MO-229	- - -			~~09-11-18~~ 12-04-18

Figure 19. Package outline SOT1069-2 (HWSON8)

13 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 20) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 7 and Table 8

Table 7. SnPb eutectic process (from J-STD-020D)

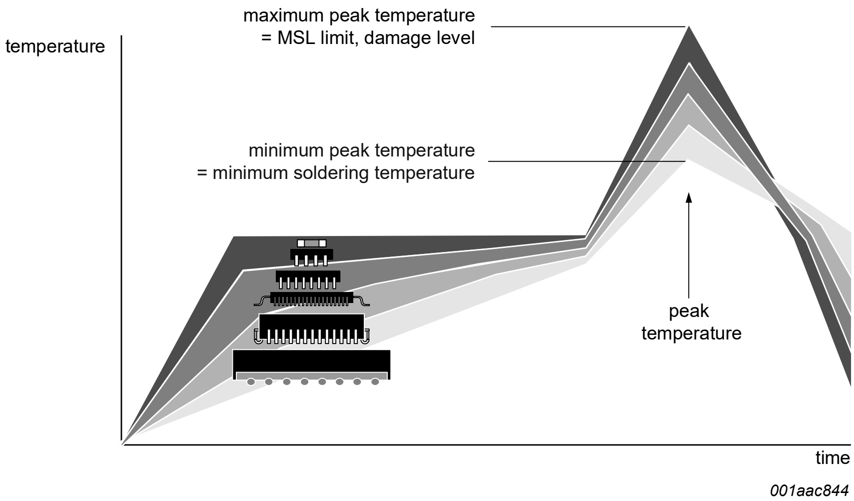
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 8. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 20.



MSL: Moisture Sensitivity Level

Figure 20. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

14 Soldering: PCB footprints

This section provides PCB footprint figures for soldering the PCA9617A.

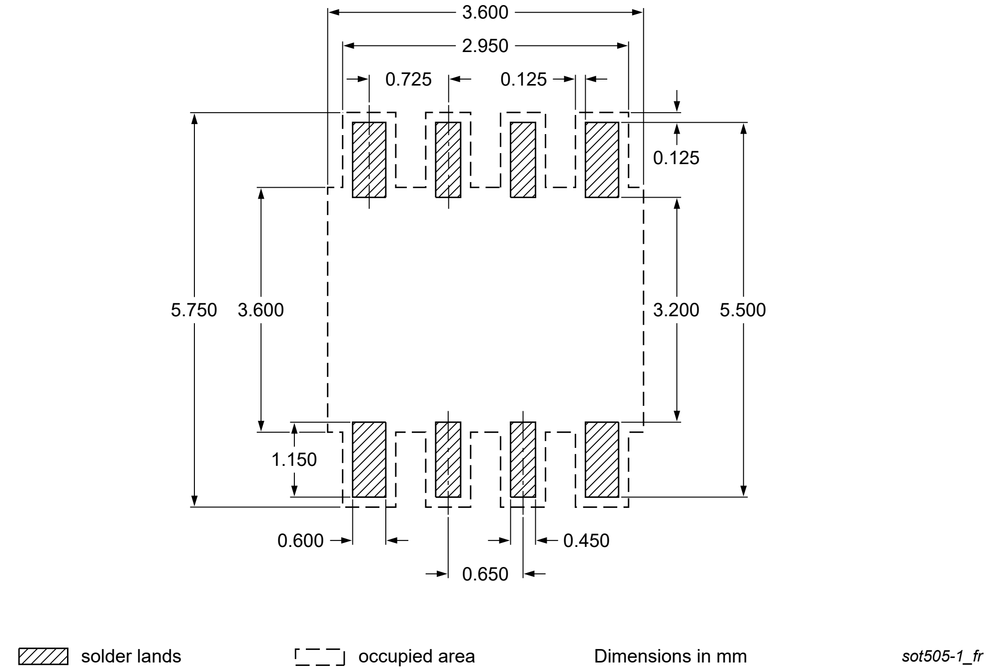
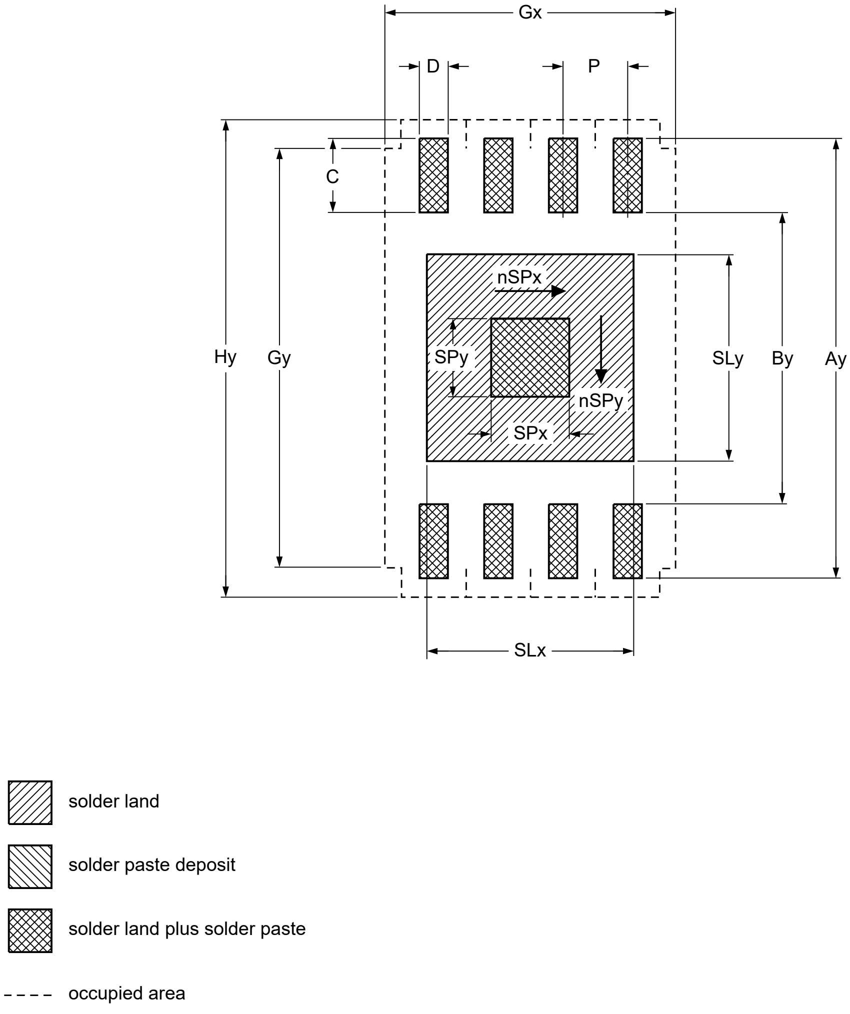


Figure 21. PCB footprint for SOT505-1 (TSSOP8); reflow soldering

Footprint information for reflow soldering of HWSON8 package **SOT1069-2**



DIMENSIONS in mm

P	Ay	By	C	D	SLx	SLy	SPx	SPy	Gx	Gy	Hy	nSPx	nSPy
0.5	3.45	2.2	0.625	0.25	1.6	1.6	0.6	0.6	2.25	3.25	3.7	1	1

Issue date ~~12-02-09~~ 12-02-22

sot1069-2_fr

Figure 22. PCB footprint for SOT1069-2 (HWSON8); reflow soldering

15 Acronyms

Table 9 describes acronyms used in this document.

Table 9. Acronyms

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
PMBus	Power Management Bus
RC	Resistor-Capacitor network
SMBus	System Management Bus

16 Revision history

Table 10 summarizes revisions to this document.

Table 10. Revision history

Document ID	Release date	Description
PCA9617A v.1.1	16 March 2026	Updated per CIN #202603012I: • Updated footnotes' placement in Table 5 • Editorial fixes
PCA9617A v.1.0	20 March 2013	• Initial public release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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