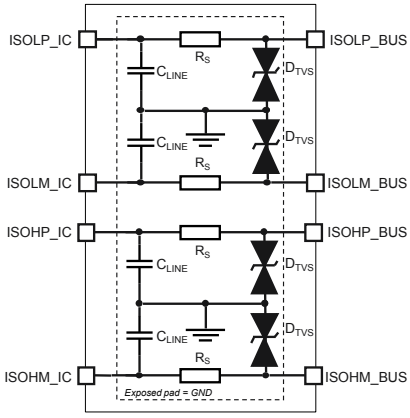
EMIF04-0410M8Y

Datasheet

Automotive isolated communication port interface for L9965

QFN-8L 2 x 1.5 x 0.75 mm



Product status link
EMIF04-0410M8Y

Features

- AEC-Q101 qualified
- Optimized for STM L9965 BMS IC
- Compatible with capacitive and inductive isolation
- One single device for ISOH and ISOL
- Embedded EOS and ESD protection
- Breakdown voltage, V_{BR} min = 18 V
- QFN package 2.0 mm x 1.5 mm 8 leads with exposed pad
- Bidirectional ESD protection devices
- Low leakage current
- ECOPACK2 RoHS compliant component
- **Complies with the following standards**:
  - J-STD-020 MSL level 1 and UL94, V0
  - IPC7531 footprint and JEDEC registered package
- **Complies with ISO 10605 / IEC 61000-4-2 - C = 150 pF, R = 330 Ω, exceeds level 4**:
  - ±25 kV (air discharge)
  - ±12 kV (contact discharge)
- **Complies with ISO 10605 - C = 330 pF, R = 330 Ω**:
  - ±25 kV (air discharge)
  - ±8 kV (contact discharge)
- **Complies with ISO 7637-3**:
  - Pulse 3a : -150 V
  - Pulse 3b : +150 V
  - Pulse 2a: +/-85 V

Application

Where EMI filtering in ESD sensitive equipment is required:

- Battery management system

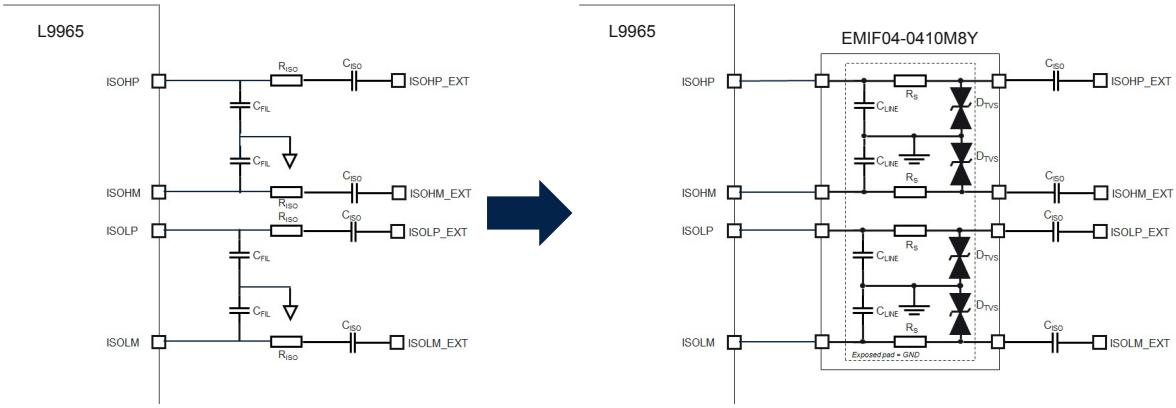
Description

The EMIF04-0410M8Y provides, in one single device, the vertical interface for the isolated communication port of the L9965 compatible with both capacitive and inductive capacitance isolation.

It is housed in QFN package and provides a superior protection level.

1 Application block diagram

Figure 1. Discret filter integrated on EMIF04-0410M8Y with the addition of protection



2 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	ISO 10605 - C = 150 pF, R = 330 Ω: BUS pins Contact discharge Air discharge	 ±12 ±25	kV
		ISO 10605 - C = 330 pF, R = 330 Ω: BUS pins Contact discharge Air discharge	 ±8 ±25	
		HBM (human body model) - MIL STD 883C (C = 100 pF, R = 1.5 kΩ) IC pins	±8	
I_{PP}	Peak pulse current (8/20 µs) BUS pins		2	A
T_j	Operating junction temperature range		-55 to +150	°C
T_{stg}	Storage temperature range		-55 to +150	°C

Figure 2. Electrical characteristics (definitions)

Symbol		Parameter
V_{BR}	=	Breakdown voltage
V_{CL}	=	Clamping voltage
I_{RM}	=	Leakage current @V_{RM}
V_{RM}	=	Stand-off voltage
I_{PP}	=	Peak pulse current
R_D	=	Dynamic resistance
I_R	=	Breakdown current

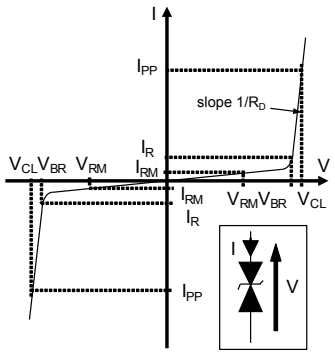


Table 2. Electrical characteristics (T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	Breakdown voltage	I_R = 1 mA	18			V
I_{RM}	Leakage current	V_{RM} = 5 V			50	nA
R_S	Serial resistor	I_{RS} = 10 mA	36	40	44	Ω
C_{LINE}	Line capacitance	V_{LINE} = 0 V, f = 1 MHz, V_{osc} = 30 mV	90	100	110	pF
V_{CL}(1)	Clamping voltage	ISO 10605 / IEC 61000-4-2 – C = 150 pF, R = 330 Ω + 8 kV contact discharge, measured at 30 ns on the IC side (pin 1 to pin 4)		26.4		V
		TLP, pulse duration 100 ns, 16 A on V_{BUS} side (pin 5 to pin 8)		48.6		
		8/20 µs waveform, I_{PP} = 2 A on V_{BUS} side (pin 5 to pin 8)			31	
R_D(1)	Dynamic resistance	TLP - pulse duration 100 ns I_{PP} [1 A – 16 A] on V_{BUS} side (pin 5 to pin 8)		1.57		Ω

1. *Evaluated By Characterization – Not tested in production.*

2.1 Characteristics curves

Figure 3. Leakage current versus junction temperature

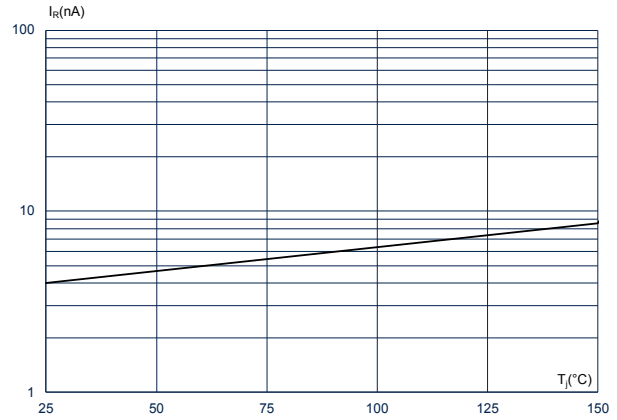


Figure 4. Single-line attenuation S_{21} (dB)

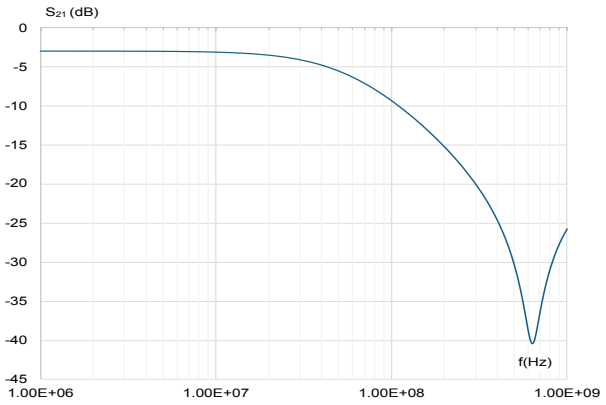


Figure 5. Line capacitance versus applied voltage

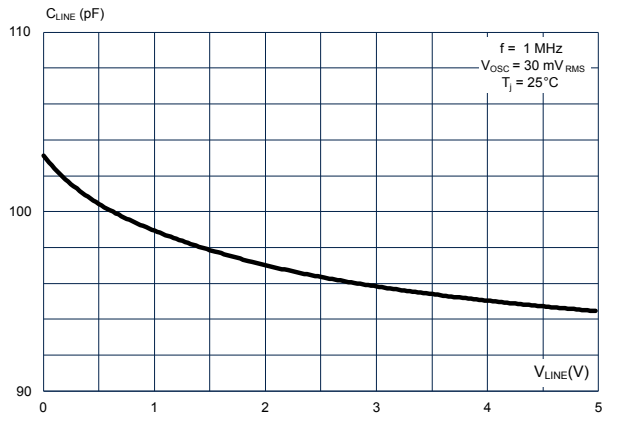


Figure 6. TLP characteristic

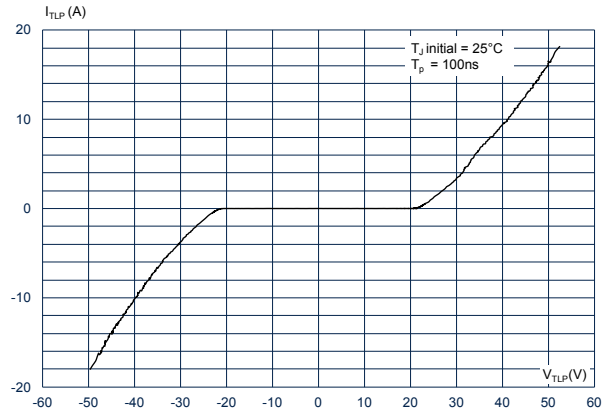


Figure 7. Response to ISO 10605 - C = 150 pF, R = 330 Ω (-8 kV contact) measured at the IC side pin

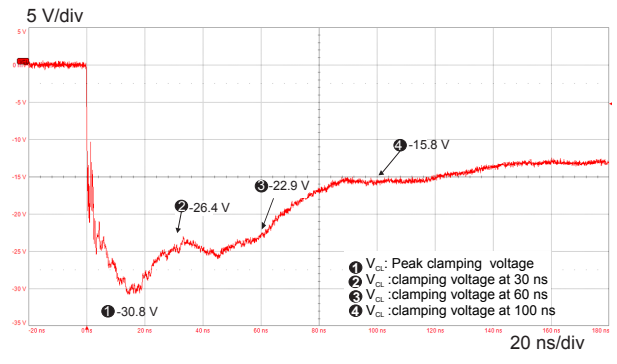


Figure 8. Response to ISO 10605 - C = 150 pF, R = 330 Ω (+8 kV contact) measured at the IC side pin

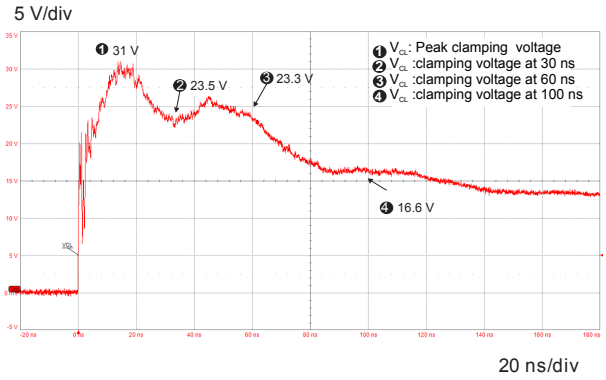


Figure 9. Response to ISO 7637-3 Pulse 3a: -150 V, measured at the IC side pin

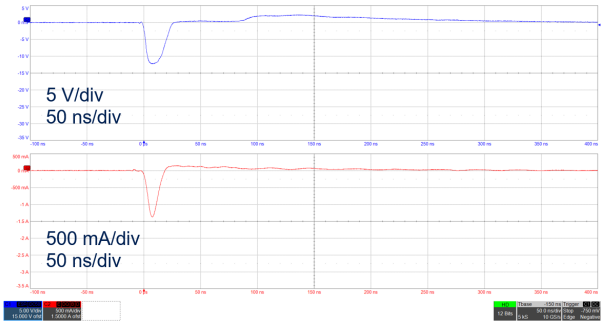


Figure 10. Response to ISO 7637-3 Pulse 3b +150 V, measured at the IC side pin

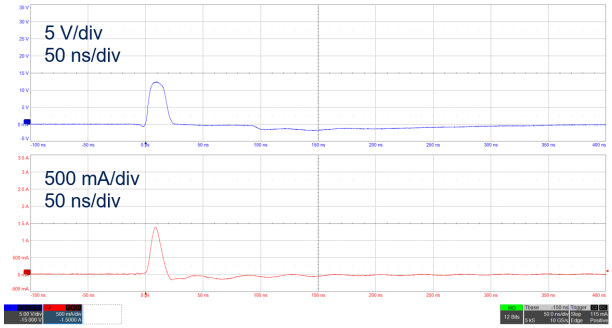


Figure 11. Response to ISO 7637-3 Pulse 2a: -85 V, measured at the IC side pin

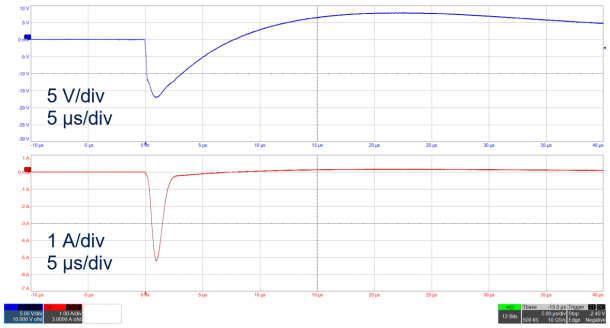
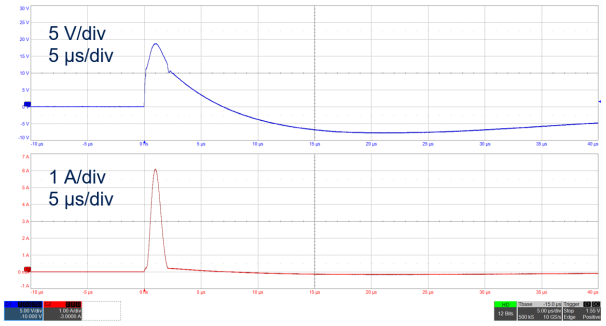


Figure 12. Response to ISO 7637-3 Pulse 2a: +85 V, measured at the IC side pin



3 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 Package information

Figure 13. QFN-8L package outline

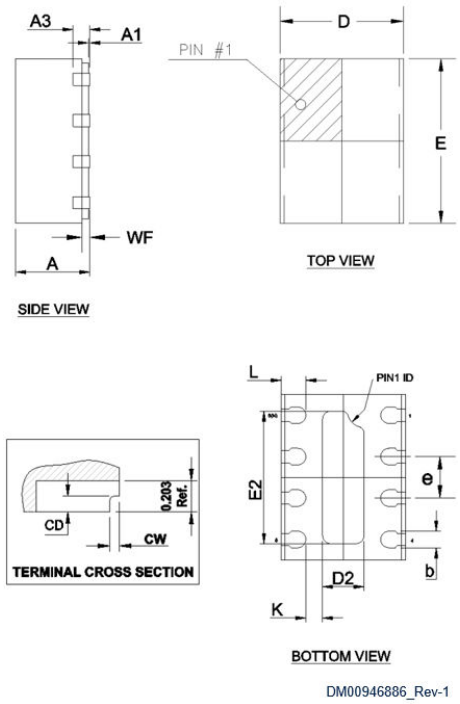


Table 3. QFN-8L package mechanical data

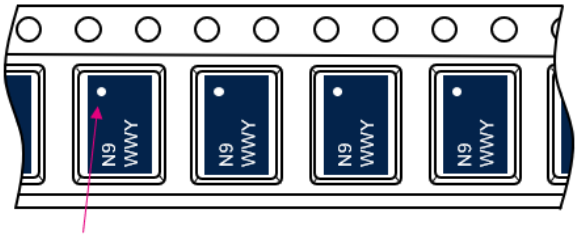
Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203	
b	0.15	0.20	0.25
D	1.45	1.50	1.55
E	1.95	2.00	2.05
e		0.50	
D2	0.40	0.50	0.60
E2	1.50	1.60	1.70
K	0.20		
L	0.20	0.30	0.40
CD	0.10		
CW	0.02	0.05	0.08
WF	0.10		

Figure 14. **Marking**

N9: Marking
Y : Year
WW : Week

Dot indicates pin 1

Figure 15. **Package orientation in reel**



Pin 1 located according to EIA-481

Note: Pocket dimensions are not on scale.
Only pin 1 mark must be used to orient the component for its placement on a PCB.

Figure 16. **7" reel dimension values (mm)**

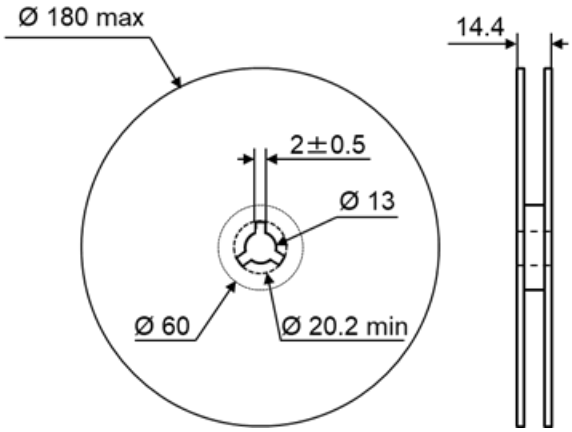


Figure 17. **Tape and reel orientation**

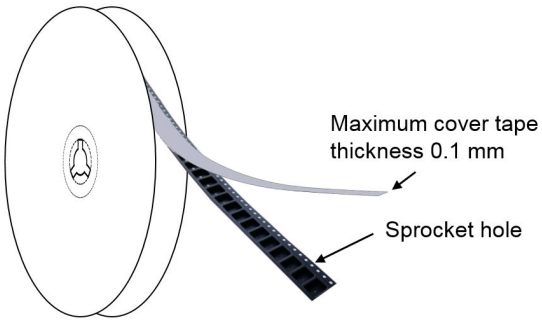


Figure 18. **Inner box dimensions (mm)**

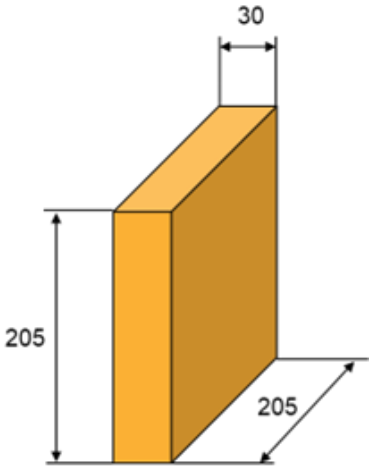


Figure 19. Tape and reel outline

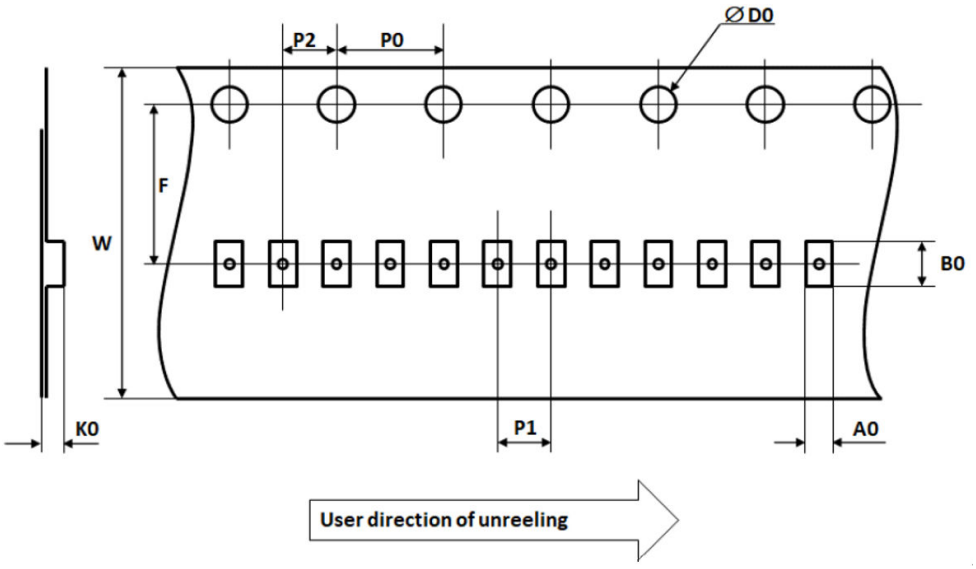
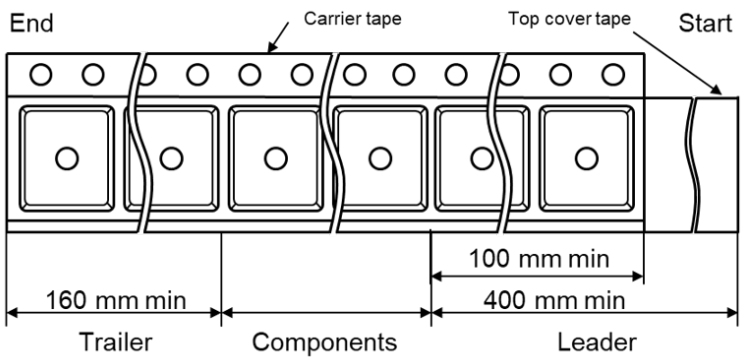


Table 4. Tape and reel mechanical data

Ref	Dimensions		
	Millimeters		
	Min	Typ	Max
A0	0.34	0.37	0.40
B0	0.79	0.82	0.85
D0	1.40	1.50	1.60
F	3.45	3.50	3.55
K0	0.24	0.27	0.30
P0	3.90	4.00	4.10
P1	1.95	2.00	2.05
P2	1.95	2.00	2.05
W	7.90	8.00	8.30

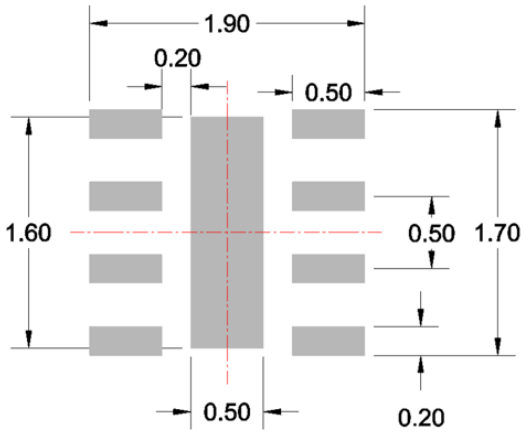
Figure 20. Tape leader and trailer dimensions



4 Recommendation PCB assembly

4.1 Footprint

Figure 21. **Recommended footprint in mm**



4.2 Stencil opening design

- Stencil opening thickness: 75 µm / 3 mils
- Stencil opening ratio: 90%

Figure 22. **Stencil opening recommendations in mm**

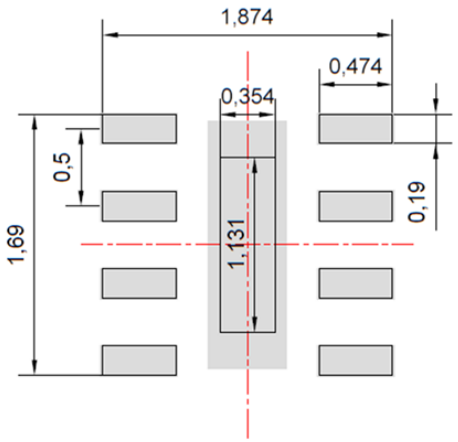
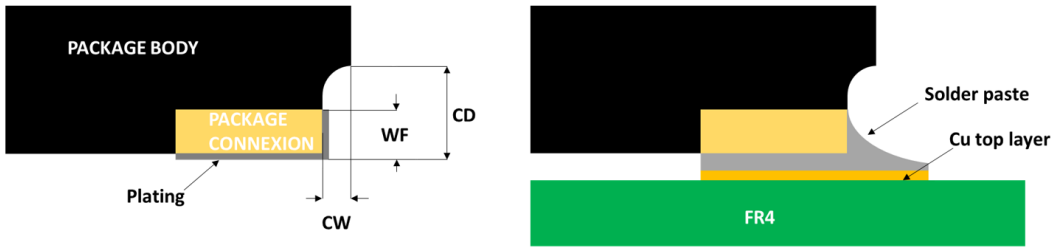


Figure 23. **Wettable flank profile**



Note: You can find the wettable flank values in Table 3.

4.3 Solder paste

1. Halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Tack force high enough to resist component displacement during PCB movement.
4. Particles size 20-38 µm per IPCJ STD-005.

4.4 Placement

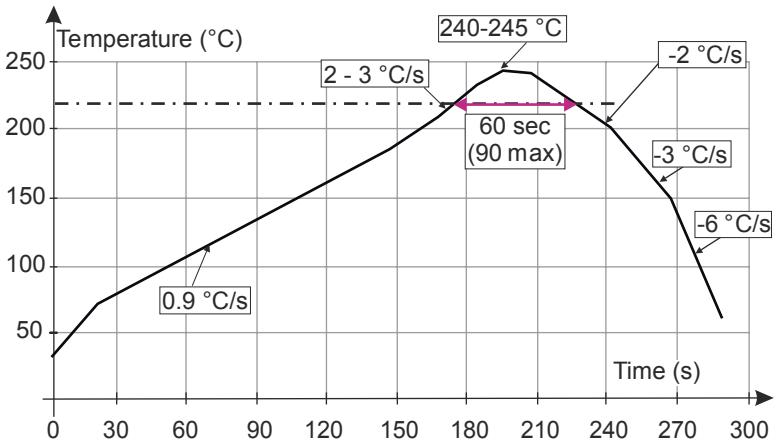
1. It is recommended to use leads recognition instead of package outline for accurate placement on footprint with adequate resolution tool.
2. Tolerance of ±50 µm is recommended.
3. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
4. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.5 PCB design preference

1. Any via around or inside the footprint area must be closed to avoid solderpaste migration in the via.
2. Position and dimensions of the tracks should be well balanced. A symmetrical layout is recommended to prevent assembly troubles.

4.6 Reflow profile

Figure 24. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. O_2 rate inside the oven must be below 500 ppm. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

5 Ordering information

Table 5. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
EMIF04-0410M8Y	N9[1]	QFN-8L	7 mg	3000	Tape and reel

1. *The marking can be rotated by 90° to differentiate assembly location*

Revision history

Table 6. **Document revision history**

Date	Revision	Changes
16-Apr-2026	1	Initial release.
08-Jun-2026	2	Added Section 1: Application block diagram.

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