EVQ4232A-VE-00A

36V,6A Buck-Boost Converter with Four Integrated MOSFETs and I²C Interface Evaluation Board, AEC-Q100 Qualified

DESCRIPTION

The EVQ4232A-VE-00A is an evaluation board designed to demonstrate the capabilities of the MPQ4232A, a synchronous, four-switch, buck-boost converter with integrated MOSFETs. The device can deliver up to 6A of output current (I_{OUT}) and achieve excellent efficiency across a certain input supply voltage (V_{IN}) range.

The MPQ4232A is designed for USB power delivery (PD) and wireless charging applications. It can work well with an external PD controller or wireless charging controller via the I²C interface.

The MPQ4232A is available in a small QFN-19 (4mmx5mm) package with wettable flanks. It is recommended to read the MPQ4232A datasheet prior to making any changes to the EVQ4232A-VE-00A.

PERFORMANCE SUMMARY

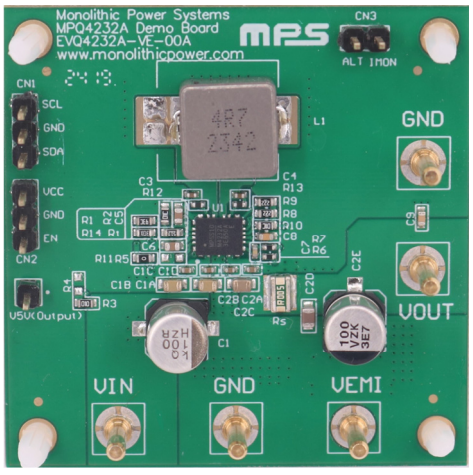
Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V_{IN}) range		4V to 36V
Output voltage (V_{OUT}) (1)	V_{IN} = 4V to 36V, I_{OUT} = 0A to 6A	V_{OUT} = 5V
Maximum output current (I_{OUT}) (2)	V_{IN} = 4V to 36V	6A
Typical efficiency	V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A	95.58%
Peak efficiency	V_{IN} = 12V, V_{OUT} = 15V, I_{OUT} = 1.5A	98.28%
Switching frequency (f_{SW})		400kHz

Notes:

1) V_{OUT} can be adjusted via the I²C or feedback (FB) resistor (R_{FB}).
2) The default over-current (OC) limit is 5.4A. To support a 6A I_{OUT}, the OC limit can be set to 6A via the I²C or by shorting the current-sense (CS) resistor (R_{CS}).

EVQ4232A-VE-00A EVALUATION BOARD



LxWxH (50mmx50mmx16mm)
4 Layers (2oz, 1oz, 1oz, and 2oz)

Board Number	MPS IC Number
EVQ4232A-VE-00A	MPQ4232AGVE-0000-AEC1

QUICK START GUIDE

The EVQ4232A-VE-00A evaluation board is easy to set up and use to evaluate the performance of the MPQ4232A. For proper measurement equipment set-up, refer to Figure 1 and follow the steps below:

1. Preset the power supply (V_{IN}) to 12V, then turn off the power supply.
2. Connect the power supply terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND
3. Connect the electronic load to:
   a. Positive (+): VOUT
   b. Negative (-): GND
4. After making the connections, turn on the power supply.
5. Once the power supply is on, the output voltage (V_{OUT}) should start up automatically.
6. To modify the MPQ4232A's register settings, connect the EVQ4232A-VE-00A to the USB-to-I²C communication kit (EVKT-USBI2C-02). Use Virtual Bench Pro 4.0 GUI to read and write the I²C registers. The EVKT-USBI2C-02 and Virtual Bench Pro 4.0 GUI are available on the MPS website.
7. If the MPQ4232A's silicon die temperature exceeds 165°C, over-temperature protection (OTP) is triggered and the entire chip shuts down. Once the temperature drops below 145°C, the chip is enabled again and resumes normal operation.
8. Figure 1 shows the measurement equipment set-up.

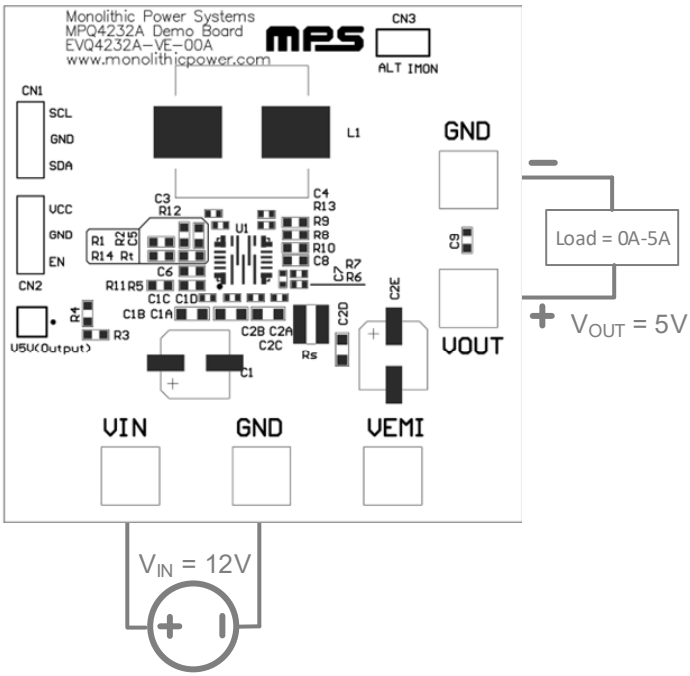


Figure 1: Measurement Equipment Set-Up

MPQ4232AGVE-0000-AEC1 DEFAULT CONFIGURATIONS

OTP Items	Description	Default Value
OPERATION	The MPQ4232A is on or off by default.	0: Off (2)
VOUT_COMMAND	V_{OUT}, voltage reference (V_{REF}) = 0.5V	5V
DITHER_ENABLE	Enables frequency spread spectrum (FSS).	1: Enabled
FREQ	Sets the switching frequency (f_{SW}).	01: 400kHz
PFM/PWM_MODE	Selects automatic pulse-frequency modulation (PFM) or pulse-width modulation (PWM) mode, or forced PWM mode.	01: Forced PWM mode
OUTPUT_OVP_EN	Enables output over-voltage protection (OVP).	1: Enabled
OUTPUT_DISCHARGE_EN	Enables output discharge during the V_{IN}, I²C, or EN disabled period.	1: Enabled
RSENS	Selects R_{SENS}.	0: 5mΩ
LDC_DISABLE	Enables line drop compensation.	0: Enables line drop compensation
CONSTANT_CURRENT_LIMIT	Sets the output current (I_{OUT}) limit.	5.4A
LINE_DROP_COMPENSATION	Sets V_{OUT} compensation vs. I_{OUT}.	00: No compensation
SWITCHING_CURRENT_LIMIT	Sets the switch B (SWB) valley current limit and the switch C (SWC) peak current limit.	01: SWC peak 12A, SWB valley 8.7A
CC_ADJ	Adjusts the constant-current (CC) limit vs. V_{OUT} gain.	0: Does not add 50mA to the CC limit
SLEW_RATE_RISE	Sets the V_{REF} adjusted rising slew rate. The V_{OUT} slew rate can be calculated with the following equation: V_{OUT} Slew Rate = V_{REF} Slew Rate x Feedback Ratio Where the feedback ratio is 10.	01: 0.16mV/μs
SLEW_RATE_FALL	Sets the V_{REF} adjusted falling slew rate. The V_{OUT} slew rate can be calculated with the following equation: V_{OUT} Slew Rate = V_{REF} Slew Rate x Feedback Ratio Where the feedback ratio is 10.	10: 0.1mV/μs
FREQ_MODE	Sets the frequency mode under buck-boost conditions.	1: Maintains the same frequency as in buck and boost mode
CC_BLANK_TIMER	Sets the blanking time before the MPQ4232A enters CC mode.	01: 2ms
HICCUP_EN	Enables hiccup mode during a current limit event.	1: Enabled
OT_WARNING	Enables the over-temperature (OT) warning.	135°C
I2C_ADDRESS	Sets the I²C slave address.	00111: 07h
VOUT_MSK	Masks ALT pin indication.	1: Masked
IOUT/POUT_MSK		0: Not masked
VIN_MSK		1: Masked
TEMP_MSK		1: Masked
PG_MSK		11: The ALT pin does not indicate any PG edge changes
RESERVED		1: Masked
UNKNOWN_MSK		1: Masked

Note:

3) Pull the ADDR pin voltage above 57% of V_{CC} to enable V_{OUT}.

EVALUATION BOARD SCHEMATIC

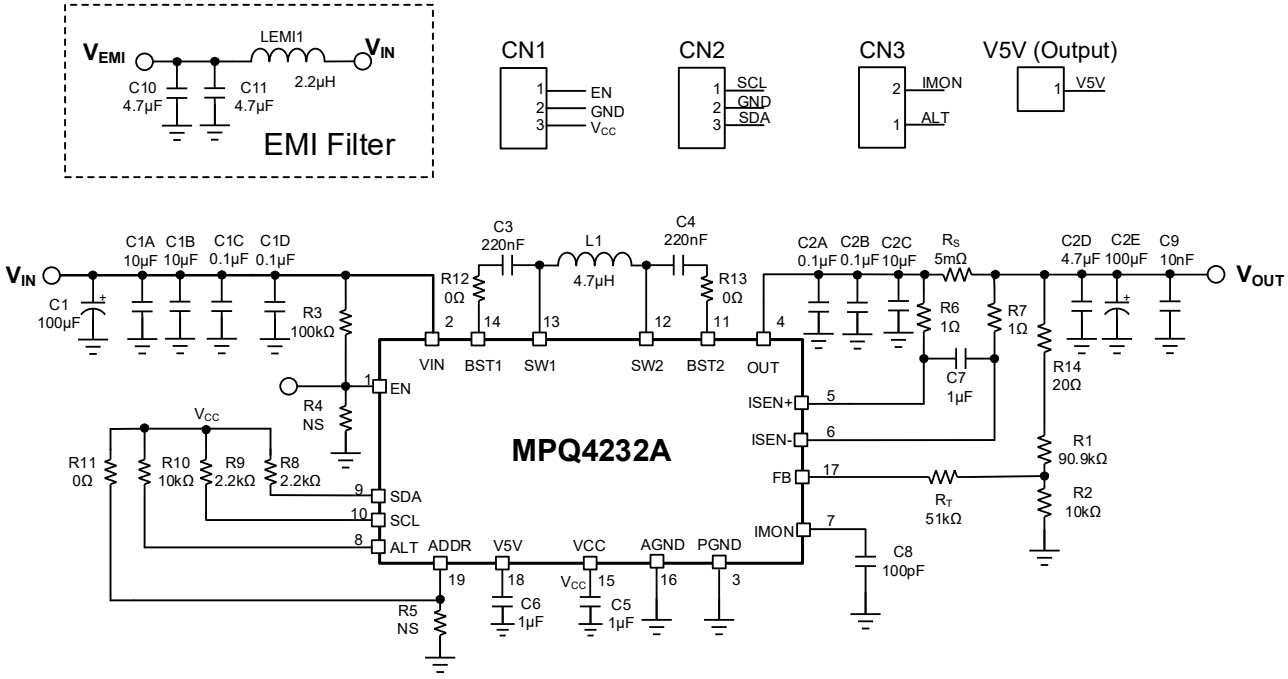


Figure 2: Evaluation Board Schematic (V_{IN} = 5V to 20V, Default f_{SW} = 400kHz, Default V_{OUT} = 5V) (3) (4kH)

Notes:

4) ADDR sets the I²C address and I2C_EN status. I2C_EN is the logic or result of the OPERATION bit and ADDR status. When ADDR is connected to V_{CC}, I2C_EN is on. Once V_{IN} and V_{EN} exceed their respective UVLO thresholds, V_{OUT} starts up automatically. When ADDR is connected to GND, I2C_EN is off. Once V_{IN} and V_{EN} exceed their respective UVLO thresholds, V_{OUT} does not start up until 1 is written to the OPERATION bit.
5) The V5V pin outputs 5V and can supply the external MCU with a 60mA capability.

EVQ4232A-VE-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C1	100µF	Aluminum electrolytic capacitor, 50V	SMD	Nippon Chemic-Con	EMZR500ARA101MF80G
2	C1A, C1B	10µF	Ceramic capacitor, 50V, X5R	0805	Murata	GRM21BR61H106KE43L
4	C1C, C1D, C2A, C2B	0.1µF	Ceramic capacitor, 50V, X7R	0402	Murata	GRM155R71H104ME14D
1	C2C	10µF	Ceramic capacitor, 25V, X7S	0805	Murata	GRM21BC71E106KE11L
1	C2D	4.7µF	Ceramic capacitor, 25V, X7R	0805	Murata	GRM21BC71E475KE11L
1	C2E	100µF	Aluminum capacitor, 35V, ±20%, ESR = 35mΩ	SMD	Panasonic	EEHZK1V101XP
2	C3, C4	220nF	Ceramic capacitor, 16V, X7R	0402	Murata	GRM155R71C224KA12D
2	C5, C6	1µF	Ceramic capacitor, 16V, X5R	0603	Murata	GRM185R61C105KE44D
1	C7	1µF	Ceramic capacitor, 10V, X5R	0402	Wurth	885012105012
1	C8	100pF	Ceramic capacitor, 50V, X7R	0603	Wurth	885012206077
1	C9	10nF	Ceramic capacitor, 50V, X7R	0603	Wurth	885012206089
2	C10, C11	4.7µF	Ceramic capacitor, 50V, X7R	0805	TDK	CGA4J1X7R1H475K
1	R1	90.9kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0790K9L
2	R2, R10	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
1	RT	51kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0751KL
1	R3	100kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07100KL
0	R4, R5	NS				
2	R6, R7	1Ω	Film resistor, 1%	0402	Yageo	RC0402FR-071RL
2	R8, R9	2.2kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-072K2L
1	R11	0Ω	Film resistor, 1%	0603	Yageo	RC0603FR-070RL
2	R12, R13	0Ω	Film resistor, 1%	0402	Yageo	RC0402FR-070RL
1	R14	20Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0720RL
1	Rs	5mΩ	Current-sense resistor, long side, 1%, 1W	L1508	Susumu	RL3720WT-R005-F
1	L1	4.7µH	Inductor, R_{DC} = 8mΩ, I_{SAT} = 13A	SMD	Superworld	PIAQ1005S4R7MN
1	LEMI1	2.2µH	Inductor, R_{DC} = 14.5mΩ, I_{SAT} = 9.2A	5030	Coilcraft	XAL5030-222ME
2	CN1, CN2	2.54mm	Through-hole connector header, 1 x 3-pin, straight	DIP	Wurth	61300311121

EVQ4232A-VE-00A BILL OF MATERIALS *(continued)*

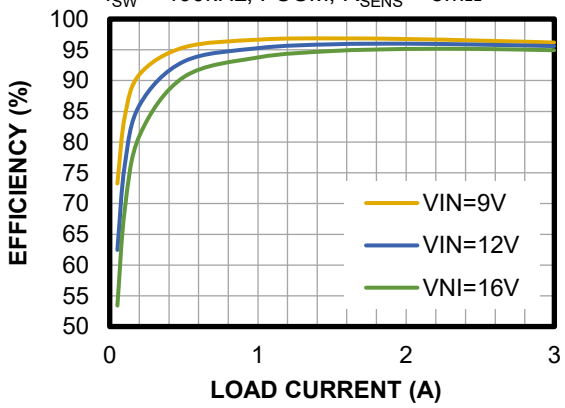
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	CN3	2.54mm	Through-hole connector header, 1 x 2-pin, straight	DIP	Wurth	61300211121
1	V5V	2.54mm	Through-hole connector header, 1 x 1-pin, straight	DIP	Wurth	61300111121
5	GND x 2, VIN, VEMI, VOUT	2mm	Copper pin, 1-pin	DIP	Any	
1	U1	MPQ4232A-AEC1	6A buck-boost converter with four integrated MOSFETs and I²C interface, AEC-Q100 qualified	QFN-19 (4mmx 5mm)	MPS	MPQ4232AGVE-0000-AEC1

EVB TEST RESULTS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

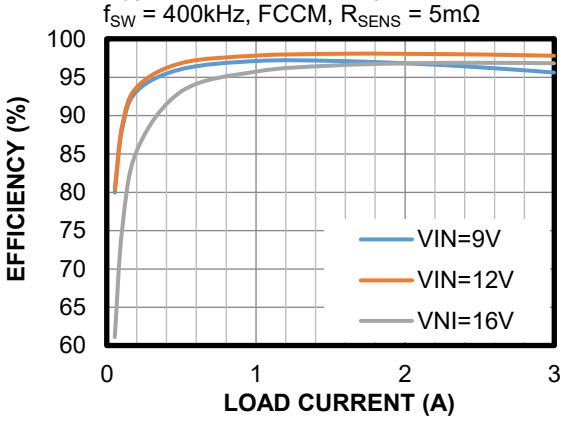
Efficiency vs. Load Current

V_{OUT} = 5V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 400kHz, FCCM, R_{SENS} = 5mΩ



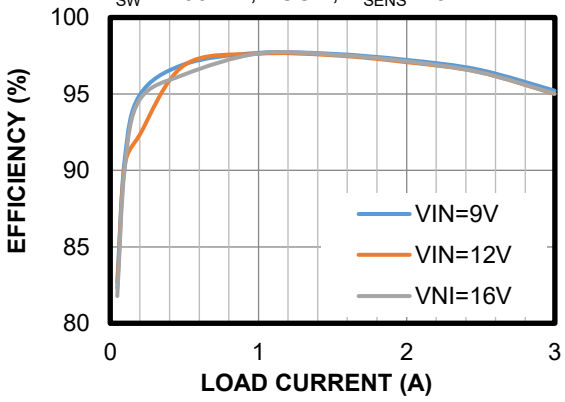
Efficiency vs. Load Current

V_{OUT} = 9V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 400kHz, FCCM, R_{SENS} = 5mΩ



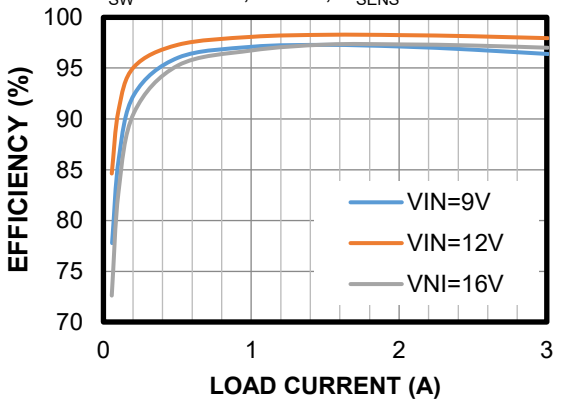
Efficiency vs. Load Current

V_{OUT} = 12V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 400kHz, FCCM, R_{SENS} = 5mΩ



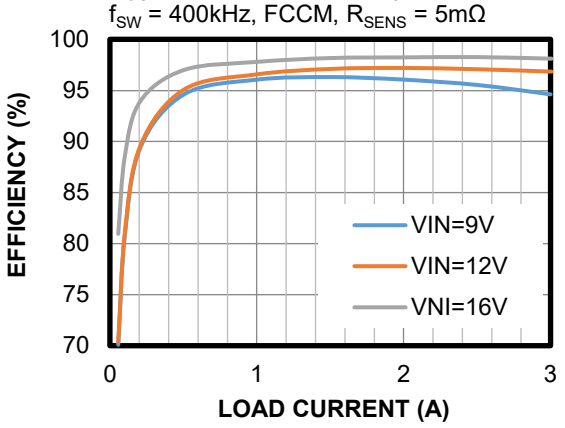
Efficiency vs. Load Current

V_{OUT} = 15V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 400kHz, FCCM, R_{SENS} = 5mΩ



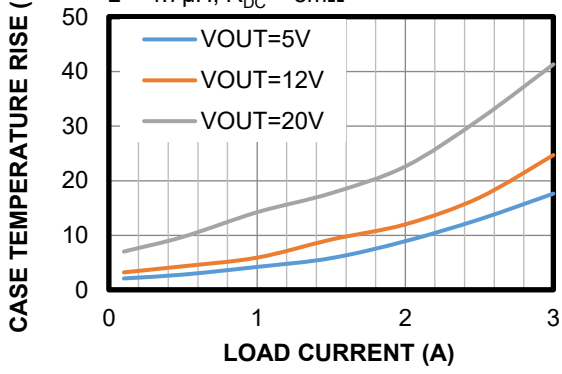
Efficiency vs. Load Current

V_{OUT} = 20V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 400kHz, FCCM, R_{SENS} = 5mΩ



Case Temperature Rise vs. Load Current

V_{IN} = 12V, V_{OUT} = 5V/12V/20V, f_{SW} = 400kHz, 5cmx5cm board, L = 4.7µH, R_{DC} = 8mΩ



PCB LAYOUT

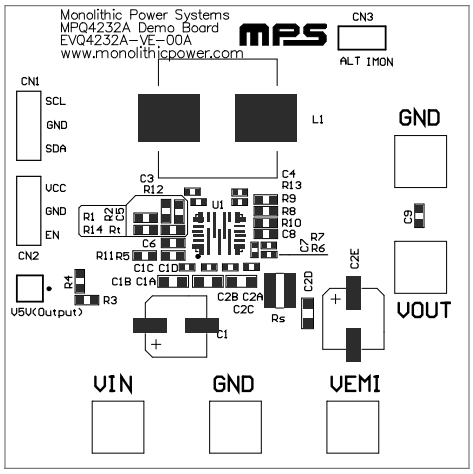


Figure 3: Top Silk

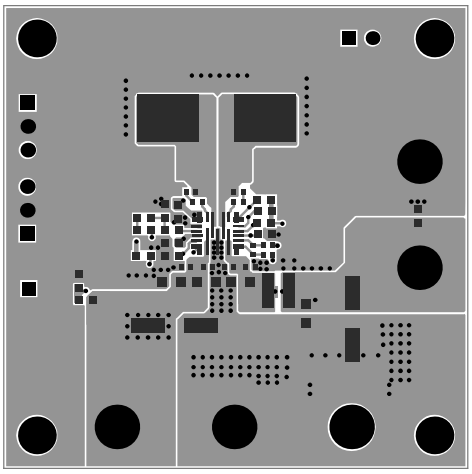


Figure 4: Top Layer

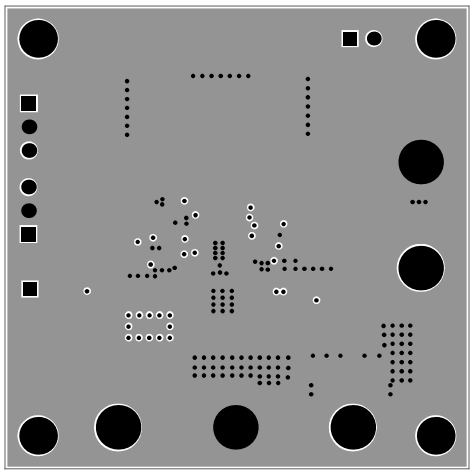


Figure 5: Mid-Layer 1

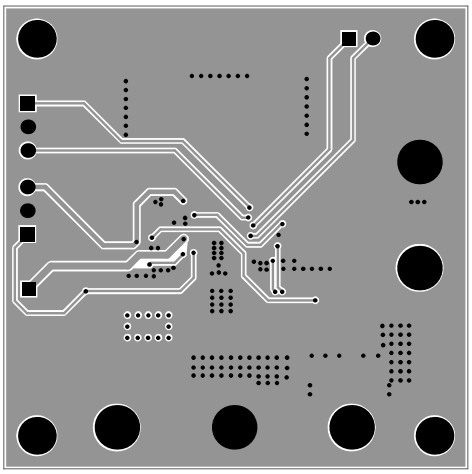


Figure 6: Mid-Layer 2

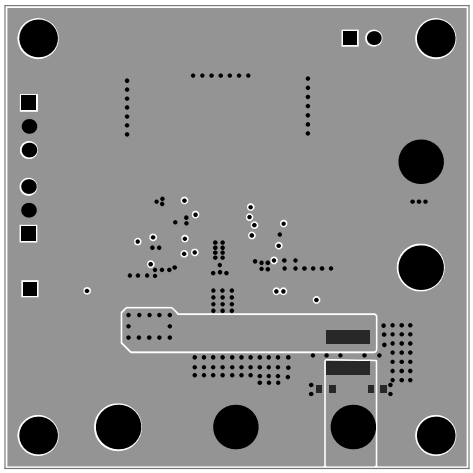


Figure 7: Bottom Layer

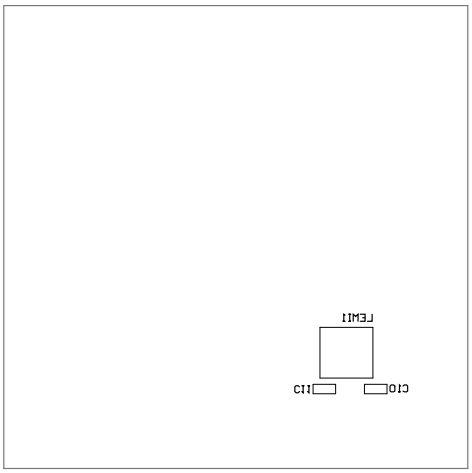


Figure 8: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/5/2025	Initial Release	-