EVQ70700FS-UT-00A

MPSafe™ ASIL-D, 5.5V PMIC for SoCs with 5 LDOs, 4 GPIOs, and 2 Voltage Monitors Evaluation Board, AEC-Q100 Qualified

DESCRIPTION

The EVQ70700FS-UT-00A is an evaluation board designed to demonstrate the capabilities of the MPQ70700FS, a functional safety power management IC (PMIC) designed to power a variety of systems-on-chip (SoCs) or safety MCUs with a requirement for multiple low-dropout regulators (LDOs).

The MPQ70700FS integrates five linear LDOs to provide up to 400mA of load current (I_{LOAD}) per channel. Three independent voltage inputs allow different input voltage (V_{IN}) levels to optimize dropout for their respective outputs. The four GPIO pins can be used for power sequencing, and two voltage monitors — including one differential monitor — monitor two external voltage rails.

Protection features include under-voltage lockout (UVLO), over-current protection (OCP), under-voltage protection (UVP), over-voltage protection (OVP), and thermal shutdown.

Safety mechanisms such as a built-in self-testing (BIST) provide high diagnostic coverage, which help the system achieve its target ASIL rating. It is developed under MPS's advanced MPSafe™ Functional Safety Product Development process, which has been independently certified to meet ISO 26262 guidelines.

The I^2C interface with packet error checking (PEC) and an integrated one-time programmable (OTP) memory support configurability.

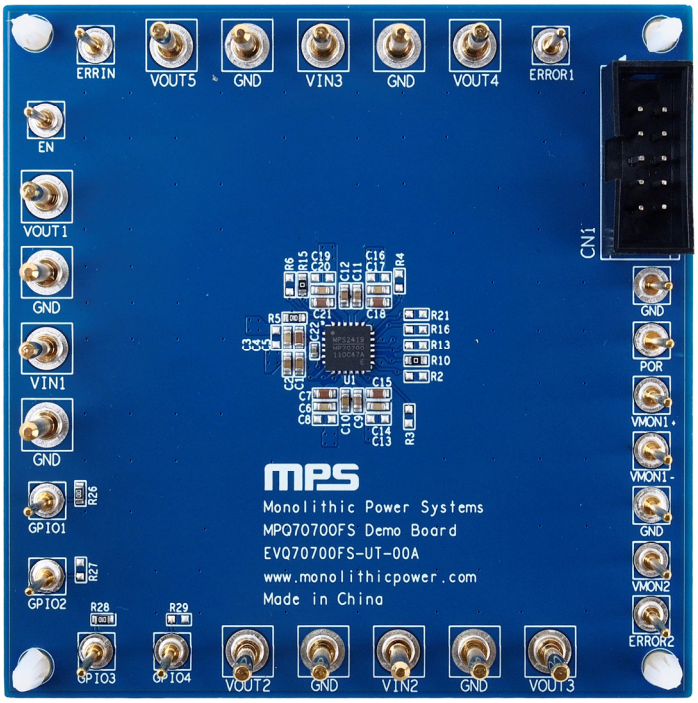
The EVQ70700FS-UT-00A is a fully assembled and tested evaluation board. The MPQ70700FS is available in a TQFN-24 (5mmx5mm) package with wettable flanks. It is available in AEC-Q100 Grade 1.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V_{IN}) range		3.5V to 5.5V
LDO 1 output voltage (V_{OUT1})	V_{IN} = 3.5V to 5.5V, I_{OUT1} = 0.1mA to 400mA	3.3V
LDO 1 maximum output current (I_{OUT1})	V_{IN} = 3.5V to 5.5V, V_{OUT1} = 3.3V	400mA
LDO 2 output voltage (V_{OUT2})	V_{IN} = 3.5V to 5.5V, I_{OUT2} = 0.1mA to 400mA	0.75V
LDO 2 maximum output current (I_{OUT2})	V_{IN} = 3.5V to 5.5V, V_{OUT2} = 0.75V	400mA
LDO 3 output voltage (V_{OUT3})	V_{IN} = 3.5V to 5.5V, I_{OUT3} = 0.1mA to 400mA	1.8V
LDO 3 maximum output current (I_{OUT3})	V_{IN} = 3.5V to 5.5V, V_{OUT3} = 1.8V	400mA
LDO 4 output voltage (V_{OUT4})	V_{IN} = 3.5V to 5.5V, I_{OUT4} = 0.1mA to 400mA	0.75V
LDO 4 maximum output current (I_{OUT4})	V_{IN} = 3.5V to 5.5V, V_{OUT4} = 0.75V	400mA
LDO 5 output voltage (V_{OUT5})	V_{IN} = 3.5V to 5.5V, I_{OUT5} = 0.1mA to 400mA	1.8V
LDO 5 maximum output current (I_{OUT5})	V_{IN} = 3.5V to 5.5V, V_{OUT5} = 1.8V	400mA

EVQ70700FS-UT-00A EVALUATION BOARD



LxWxH (7.6cmx7.6cmx1cm)

Board Number	MPS IC Number
EVQ70700FS-UT-00A	MPQ70700FSGUTE-0001AEC1

QUICK START GUIDE

The EVQ70700FS-UT-00A evaluation board is easy to set up and use to evaluate the MPQ70700FS's performance. For the proper measurement equipment set-up, refer to Figure 2 on page 4 and follow the steps below:

1. Preset the power supply (V_{IN}) between 3.5V and 5.5V, then turn off the power supply.
2. Set the load current (I_{LOAD}) for each channel (I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.1mA to 400mA). Electronic loads represent a negative impedance to the converter, and setting the current too high can trigger hiccup mode.
3. If longer cables (>0.5m total) are used between the source and the evaluation board, place a damping capacitor at the input terminals.
4. Connect the power supply terminals to:
   a. Positive (+): VIN1
   b. Negative (-): GND
5. Connect the load terminals to:
   a. Positive (+) channel: VOUT1, VOUT2, VOUT3, VOUT4, and/or VOUT5
   b. Negative (-) channel: GND
6. After making the connections, turn on the power supply. The MPQ70700FS should start up automatically.(1)
7. To use the enable (EN) function, apply a digital input to the EN pin. Pull EN above 1.23V to turn the regulator on; pull EN below 0.44V to turn it off. If the enable function is not used, EN can be connected to the VIN pin through a 100kΩ resistor.
8. Evaluate the MPQ70700FS using the I²C digital interface by following the steps below:
   a. Download and install the software Virtual Bench Pro 4.0 (VBP 4.0) from the MPS website. The MPQ70700FS GUI is embedded in VBP 4.0.
   b. Connect the EVKT-USBI2C-02 to CN1 with a ribbon cable, then connect the EVKT-USBI2C-02 to the computer with a USB cable. The EVKT-USBI2C-02 (including the ribbon cable) is included with product evaluation kits, or can be purchased separately from the MPS website.
   c. Using the MPQ70700FS GUI, scan for the evaluation board address, which is 08h by default.
   d. Evaluate the device using the MPQ70700FS GUI, such as the turn-on delay and soft-start time (t_{SS}). Figure 1 shows the I²C evaluation kit set-up.

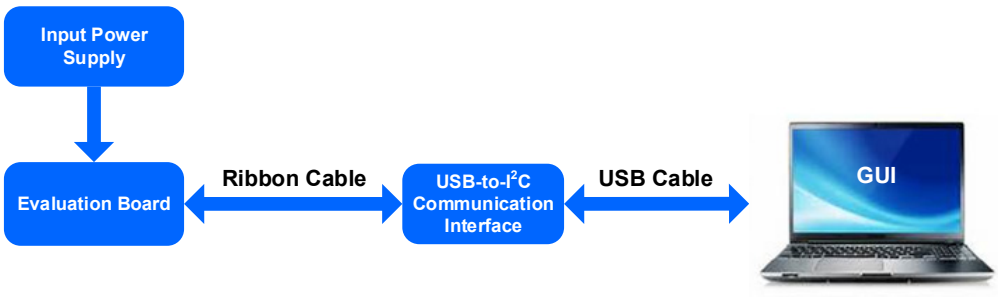


Figure 1: I²C Evaluation Kit Set-Up

Note:

1) The EN voltage (V_{EN}) should exceed the maximum enable rising threshold indicated in the Electric Characteristic table section of the MPQ70700FS datasheet.

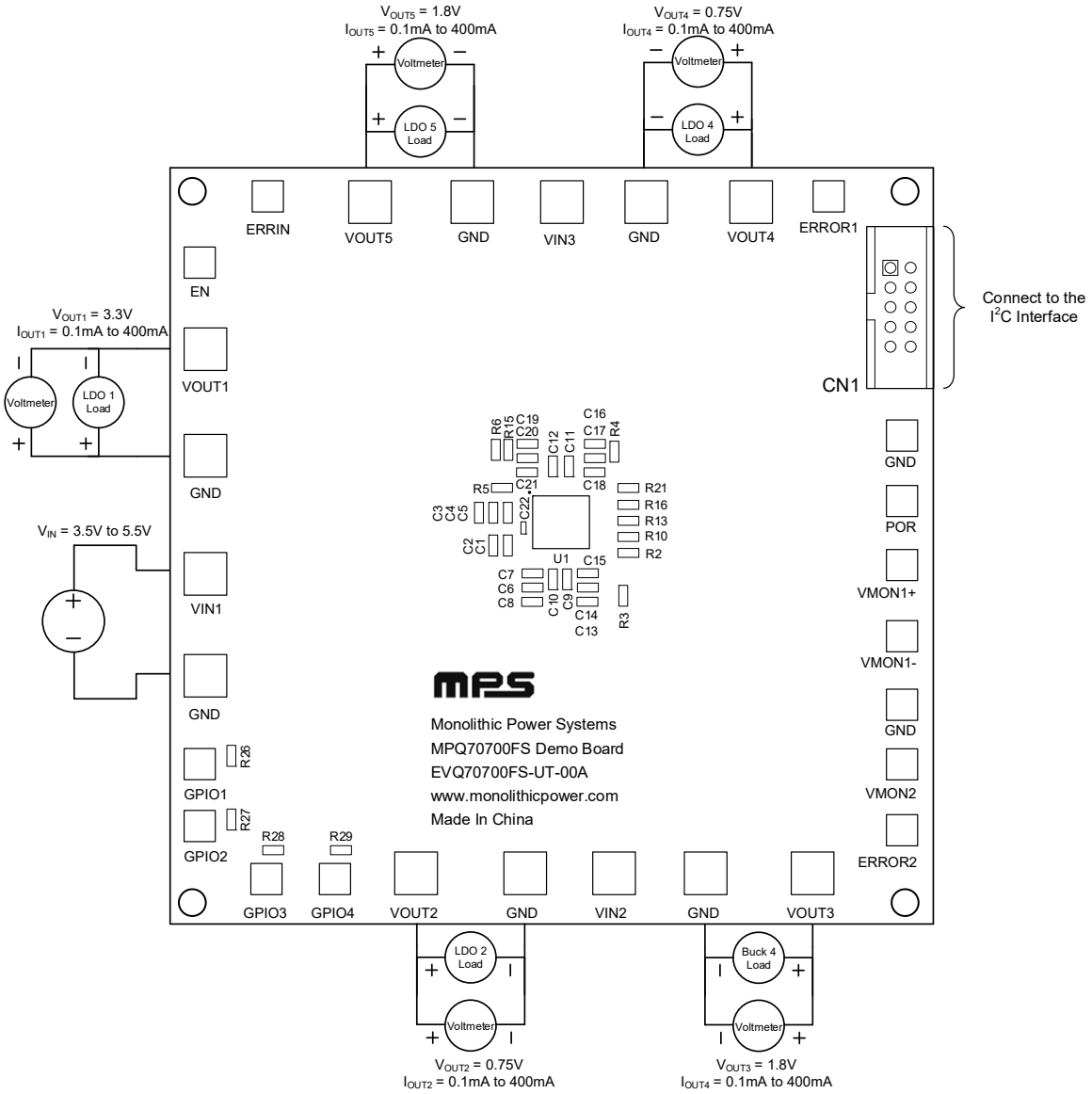


Figure 2: Measurement Equipment Set-Up

MPQ70700FS-0001 DEFAULT REGISTER VALUES

Register	Page	Register Name	Register Value	Description
00h	0	DEVICE_REV	00h	Returns device revision information.
09h	0	FAULT_ ENABLE_ INTERNAL	27h	• Any runtime cyclic redundancy check (RTCRC), register write (REG_WR) check, and/or bandgap (BG) check fault pulls ERRO1 low and is recorded to the fault registers • A state machine error and/or non-LBIST register (NBVM) double-check fault does not pull ERRO1 low and is not recorded to the fault registers
0Ah	0	FAULT_ ENABLE_SYS	0Bh	• Any I^2C packet error checking (PEC), thermal shutdown (TSD), and/or thermal warning (TWN) fault pulls ERRO1 low and is recorded to the fault registers • A watchdog failure does not pull ERRO2 low and is not recorded to the fault registers
0Bh	0	FAULT_ ENABLE_ CHANNELS1	3Fh	• Any VIN1 over-voltage protection (OVP) and/or LDO OVP fault pulls ERRO1 low and is recorded to the fault registers • A VMON1/2 OVP fault does not pull ERRO1 low and is not recorded to the fault registers
0Ch	0	FAULT_ ENABLE_ CHANNELS2	3Fh	• Any VIN2 OVP and/or LDO under-voltage protection (UVP) fault pulls ERRO1 low and is recorded to the fault registers • A VMON1/2 UVP fault does not pull ERRO1 low and is not recorded to the fault registers
0Dh	0	FAULT_ ENABLE_ CHANNELS3	1Fh	• Any LDO over-current protection (OCP) fault pulls ERRO1 low and is recorded to the fault registers • A VIN3 OVP fault does not pull ERRO1 low and is not recorded to the fault registers
0Eh	0	FAULT_ ENABLE_TEST	03h	• Any OTP single error correction (SEC) and/or analog built-in self-test (ABIST) fault pulls ERRO1 low and is recorded to the fault registers
0Fh	0	FAULT_ REACTION_ GUP1	02h	• TSD causes the state machine to enter a failsafe state • TWN causes the state machine to enter a fail-recovery state
10h	0	FAULT_ REACTION_ GUP2	FFh	Any VMON1/2 OVP, VIN1 OVP, and/or LDO OVP fault causes the state machine to enter a failsafe state.
11h	0	FAULT_ REACTION_ GUP3	FFh	Any VMON1/2 UVP, VIN2 OVP, and/or LDO UVP fault causes the state machine to enter a failsafe state.
12h	0	FAULT_ REACTION_ GUP4	3Fh	Any VIN3 OVP and/or LDO OCP fault causes the state machine to enter a failsafe state.
13h	0	FAULT_ REACTION_ GUP_ INTERNAL	1Fh	Any NBVM, REG_WR, clock, BG, and/or RTCRC fault causes the state machine to enter a failsafe state.
14h	0	ERR_MODE	40h	• ERRIN_MODE = active low • ERRIN_DLY = 0ms • ERRO_DLY = 0ms
17h	0	EN2_GROUP	00h	• The GPIO2/3/4 output cannot be controlled by EN2 • The LDO1/2/3/4/5 output cannot be controlled by EN2
18h	0	CHANNEL_EN	1Fh	• The default LDO1/2/3/4/5 output status is enabled.

MPQ70700FS-0001 DEFAULT REGISTER VALUES *(continued)*

Register	Page	Register Name	Register Value	Description
19h	0	TEST_CFG	0Fh	• AT_REOV = enabled AT_POR = enabled
1Ah	0	DLY_RCOV_CFG	4Fh	• RETRY_CFG_RCOV = 3 times • DLY_RCOV = 2.048ms
1Bh	0	GPIO_CFG	0Ah	• GPIO1/3 = input • GPIO2/4 = input
1Ch	0	TIME_SLOT	10h	TIME_SLOT = 500µs
1Dh	0	SEQ_GPIO1	00h	• GPIO1 output turn-on delay = TIME_SLOT x 0 • GPIO1 output turn-off delay = TIME_SLOT x (15 - 0)
1Eh	0	SEQ_GPIO2	50h	• GPIO2 output turn-on delay = TIME_SLOT x 5 • GPIO3 output turn-off delay = TIME_SLOT x (15 - 0)
1Fh	0	SEQ_GPIO3	00h	• GPIO3 output turn-on delay = TIME_SLOT x 0 • GPIO3 output turn-off delay = TIME_SLOT x (15 - 0)
20h	0	SEQ_GPIO4	80h	• GPIO4 output turn-on delay = TIME_SLOT x 8 • GPIO4 output turn-off delay = TIME_SLOT x (15 - 0)
21h	0	VREF_LDO1	6Eh	Sets the LDO1 output (V_{OUT1}) to 3.3V when GPIO3 is the output.
22h	0	SETUP_LDO1	13h	• Sets the LDO1 soft-start (SS) rising slew rate to 2.5mV/µs. • Sets the LDO1 over-voltage (OV), under-voltage (UV), and power-on reset (POR) thresholds when GPIO3 is the input. Refer to the MPQ70700FS datasheet for details. • LDO1 output discharge = enabled
23h	0	SEQ_LDO1	18h	• LDO1 output turn-on delay = TIME_SLOT x 1 • LDO1 output turn-off delay = TIME_SLOT x (15 – 8)
24h	0	VREF_LDO2	14h	Sets the LDO2 output (V_{OUT2}) to 0.75V.
25h	0	SETUP_LDO2	11h	• Sets the LDO2 SS rising slew rate to 2.5mV/µs • LDO2 output discharge = enabled
26h	0	SEQ_LDO2	5Ch	• LDO2 output turn-on delay = TIME_SLOT x 5 • LDO2 output turn-off delay = TIME_SLOT x (15 - 12)
27h	0	VREF_LDO3	50h	Sets the LDO3 output (V_{OUT3}) to 1.8V.
28h	0	SETUP_LDO3	11h	• Sets the LDO3 SS rising slew rate to 2.5mV/µs • LDO3 output discharge = enabled
29h	0	SEQ_LDO3	8Fh	• LDO2 output turn-on delay = TIME_SLOT x 8 • LDO2 output turn-off delay = TIME_SLOT x (15 - 15)
2Ah	0	VREF_LDO4	14h	Sets the LDO4 output (V_{OUT4}) to 0.75V.
2Bh	0	SETUP_LDO4	11h	• Sets the LDO4 SS rising slew rate to 2.5mV/µs • LDO4 output discharge = enabled
2Ch	0	SEQ_LDO4	8Fh	• LDO4 output turn-on delay = TIME_SLOT x 8 • LDO4 output turn-off delay = TIME_SLOT x (15 - 15)
2Dh	0	VREF_LDO5	50h	Sets the LDO5 output (V_{OUT5}) to 1.8V.
2Eh	0	SETUP_LDO5	11h	• Sets the LDO5 SS rising slew rate to 2.5mV/µs • LDO5 output discharge = enabled
2Fh	0	SEQ_LDO5	6Dh	• LDO5 output turn-on delay = TIME_SLOT x 6 • LDO5 output turn-off delay = TIME_SLOT x (15 - 13)
30h	0	POR1_CTL_CTH	CEh	Sets LDO1's POR threshold voltage to 3.025V when GPIO3 is the output.
31h	0	POR2_CTL_CTH	12h	Sets LDO2's POR threshold voltage to 0.675V.

MPQ70700FS-0001 DEFAULT REGISTER VALUES *(continued)*

Register	Page	Register Name	Register Value	Description
32h	0	POR3_CTL_CTH	5Eh	Sets LDO3's POR threshold voltage to 1.625V.
33h	0	POR4_CTL_CTH	12h	Sets LDO4's POR threshold voltage to 0.675V.
34h	0	POR5_CTL_CTH	5Eh	Sets LDO5's POR threshold voltage to 1.625V.
35h	0	POR_CTL_DLY	9Bh	Sets POR_DLY to 19.968ms.
36h	0	MON1_OV_VTH	FFh	Sets the VMON1 OV threshold to 3.6375V.
37h	0	MON1_UV_VTH	00h	Sets the VMON1 UV threshold to 0.45V.
38h	0	MON1_MODE	00h	• VMON1 = disabled • Any VMON1 OV or UV faults are not detected when the device is in an idle, active, or sleep state • Sets the VMON1 OV/UV fault debounce time to 10µs
39h	0	MON2_OV_VTH	FFh	Sets the VMON2 OV threshold to 3.6375V.
3Ah	0	MON2_UV_VTH	00h	Sets the VMON2 UV threshold to 0.45V.
3Bh	0	MON2_MODE	00h	• VMON2 = disabled • Any VMON2 OV or UV faults are not detected when the device is in an idle, active, or sleep state • Set the VMON2 OV/UV fault debounce time to 10µs
3Ch	0	LDO1_OV_VTH	FBh	Sets the LDO1 OV threshold to 3.5875V when GPIO3 is the output.
3Dh	0	LDO1_UV_VTH	D5h	Sets the LDO1 UV threshold to 3.1125V when GPIO3 is the output.
3Eh	0	LDO1_MODE	00h	• Sets all LDO OC fault debounce times to 10µs • Sets the LDO1 OV/UV fault debounce time to 10µs
3Fh	0	LDO2_OV_VTH	1Ch	Sets the LDO2 OV threshold to 0.8V.
40h	0	LDO2_UV_VTH	14h	Sets the LDO2 UV threshold to 0.7V.
41h	0	LDO2_MODE	00h	Sets the LDO2 OV/UV fault debounce time to 10µs.
42h	0	LDO3_OV_VTH	77h	Sets the LDO3 OV threshold to 1.9375V.
43h	0	LDO3_UV_VTH	66h	Sets the LDO3 UV threshold to 1.725V.
44h	0	LDO3_MODE	00h	Sets the LDO3 OV/UV fault debounce time to 10µs.
45h	0	LDO4_OV_VTH	1Ch	Sets the LDO4 OV threshold to 0.8V.
46h	0	LDO4_UV_VTH	14h	Sets the LDO4 UV threshold to 0.7V.
47h	0	LDO4_MODE	00h	Sets the LDO4 OV/UV fault debounce time to 10µs.
48h	0	LDO5_OV_VTH	77h	Sets the LDO5 OV threshold to 1.9375V.
49h	0	LDO5_UV_VTH	66h	Sets the LDO5 UV threshold to 1.725V.
4Ah	0	LDO5_MODE	00h	Sets the LDO5 OV/UV fault debounce time to 10µs.
4Bh	0	WDT_CFG	73h	• A watchdog failure does not pull POR low • Watchdog mode is Q&A mode • The watchdog fault limit is set to 8 and watchdog is enabled • Watchdog is disabled when the device is in a sleep, sleep in, or sleep out state. • Watchdog delay = 4 x (open window time + closed window time)
4Ch	0	WDT_CLOSE	09h	Closed window time = 10ms
4Dh	0	WDT_OPEN	09h	Open window time = 10ms

MPQ70700FS-0001 DEFAULT REGISTER VALUES *(continued)*

Register	Page	Register Name	Register Value	Description
51h	0	I2C_ADDRESS	08h	Sets the I²C address to 0x08. Connect the ADDR pin to GND.
52h	0	I2C_CONFIG	01h	I²C PEC function = enabled

EVALUATION BOARD SCHEMATIC

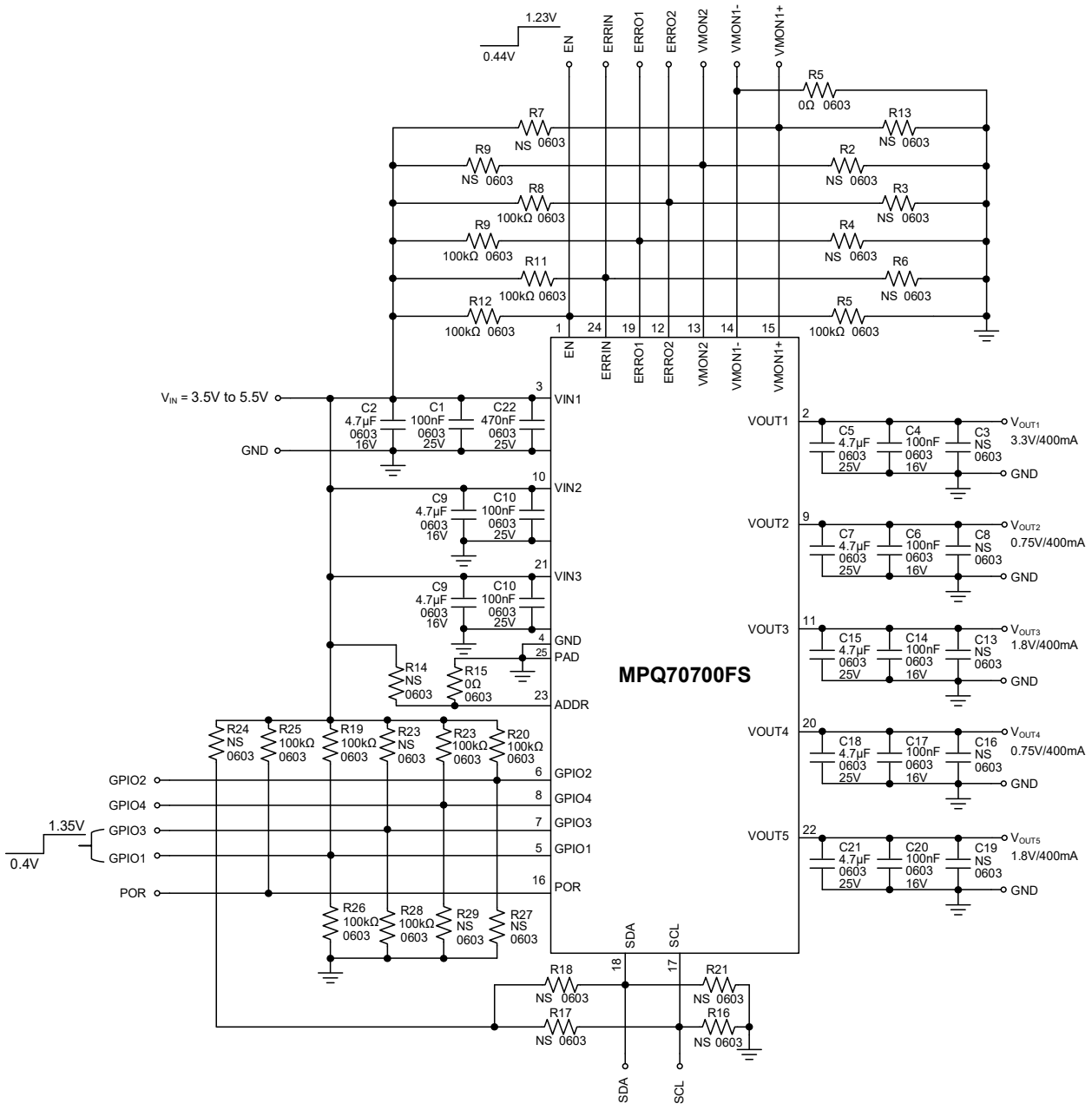
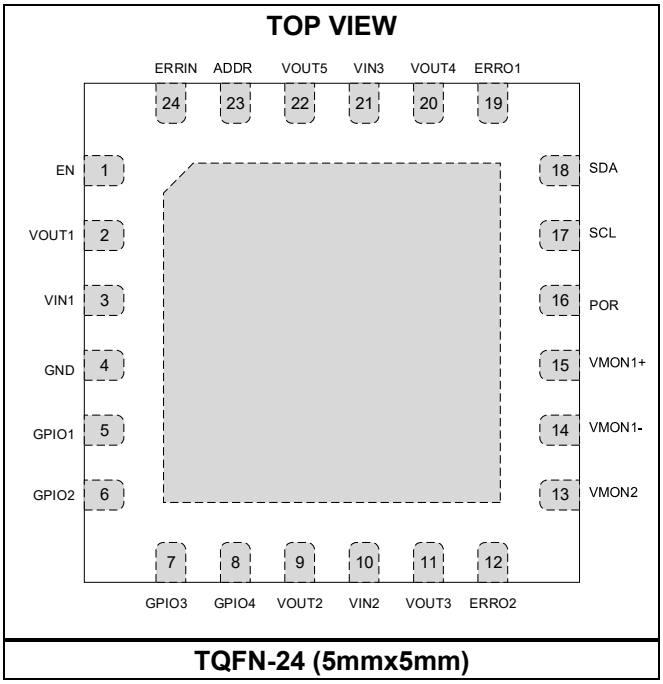


Figure 3: Evaluation Board Schematic

EVALUATION BOARD SCHEMATIC *(continued)*

PACKAGE REFERENCE



TQFN-24 (5mmx5mm)

EVQ70700FS-UT-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	CN1	2.54mm	2-row, 10-pin I²C interface connector	DIP	Custom (2)	
3	C2, C9, C11	4.7µF	Capacitor, 16V, X5R	0603	Murata	GRM188R61C475KE11D
3	C1, C10, C12	100nF	Capacitor, 25V, X7R	0603	Murata	GCJ188R71E104KA12D
5	C4, C6, C14, C17, C20	100nF	Capacitor, 16V, X7R	0603	Murata	GRM188R71C104KA01D
5	C5, C7, C15, C18, C21	4.7µF	Capacitor, 25V, X5R	0603	Murata	GRM188R61E475KE11D
5	C3, C8, C13, C16, C19	NS				
1	C22	470nF	Capacitor, 25V, X5R	0402	Murata	GRM155R61E474KE01D
14	VOUT1, VIN1, GND, VOUT2, VIN2, GND, VOUT3, VIN3, GND, VOUT4, VOUT5, GND, GND, GND	2mm	Golden pin	DIP	Custom (2)	
14	VMON1, POR, GPIO1, GND, ERRO1, ERRIN, EN, GPIO2, ERRO2, GPIO3, GND3, GPIO4, GND, VMON1-, VMON1+	1mm	Golden pin	DIP	Custom (2)	
11	R5, R8, R9, R11, R12, R19, R20, R23, R25, R26, R28	100kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07100KL
16	R1, R2, R3, R4, R6, R7, R13, R14, R16, R17, R18, R21, R22, R24, R27, R29	NS				
2	R10, R15	0Ω	Film resistor, 1%	0603	Yageo	RC0603FR-070RL
1	U1	MPQ70700FS-AEC1	MPSafe™ ASIL-D, 5.5V PMIC, AEC-Q100	TQFN-15 (2.5mmx 3.5mm)	MPS	MPQ70700FSGUTE-0001AEC1

Note:

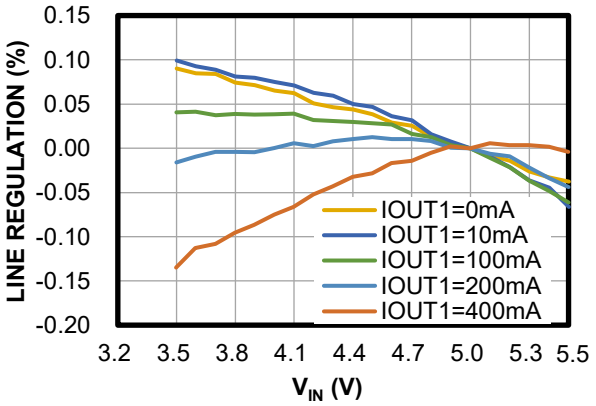
2) MPS custom-produces these pins. Contact an MPS FAE for more information.

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

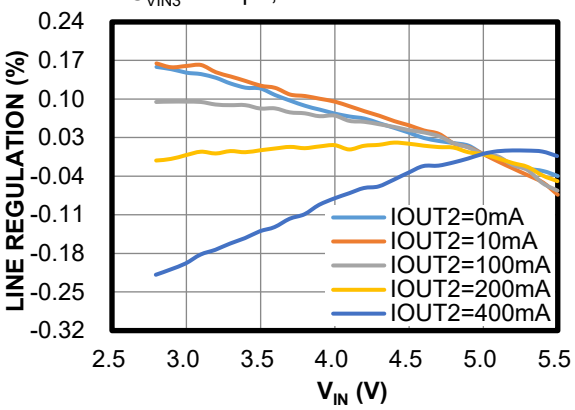
Line Regulation (LDO 1)

V_{OUT1} = 3.3V, C_{OUT1} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



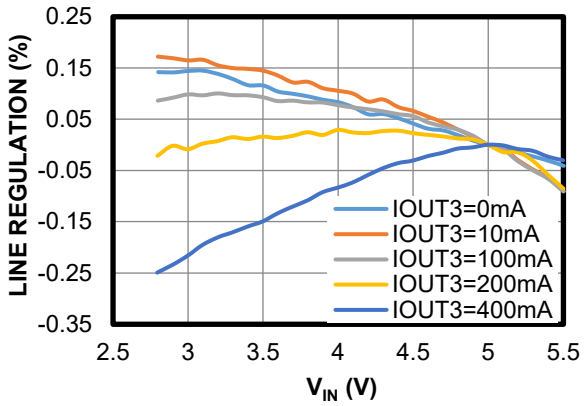
Line Regulation (LDO 2)

V_{OUT2} = 0.75V, C_{OUT1} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



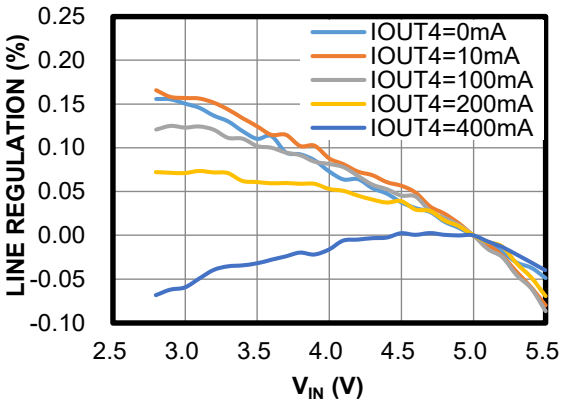
Line Regulation (LDO 3)

V_{OUT3} = 1.8V, C_{OUT3} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



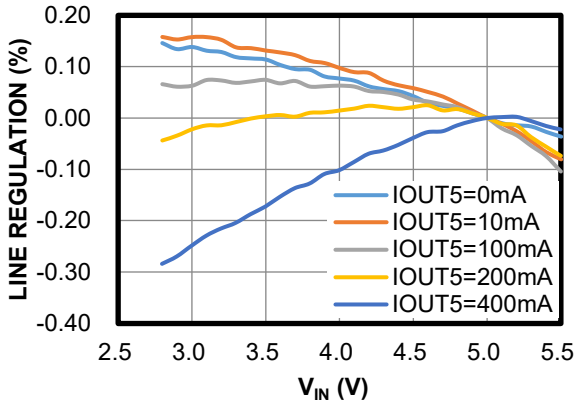
Line Regulation (LDO 4)

V_{OUT4} = 0.75V, C_{OUT4} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



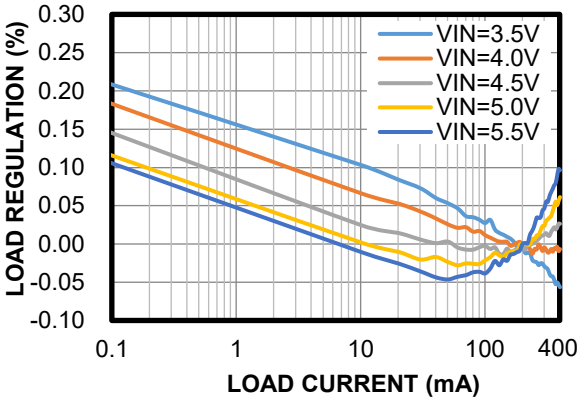
Line Regulation (LDO 5)

V_{OUT5} = 0.75V, C_{OUT5} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



Load Regulation (LDO 1)

V_{OUT1} = 3.3V, C_{OUT1} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled

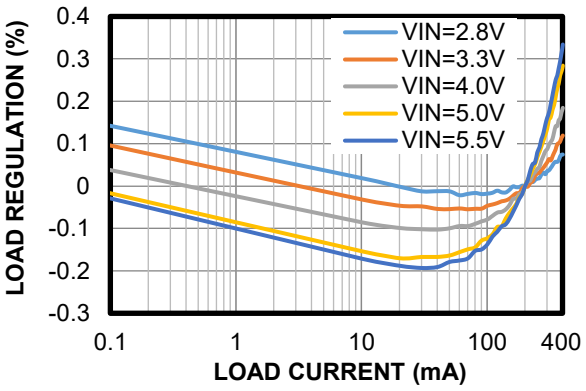


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

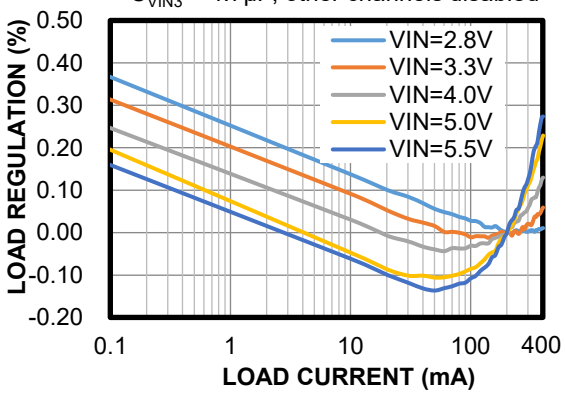
Load Regulation (LDO 2)

V_{OUT2} = 0.75V, C_{OUT2} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



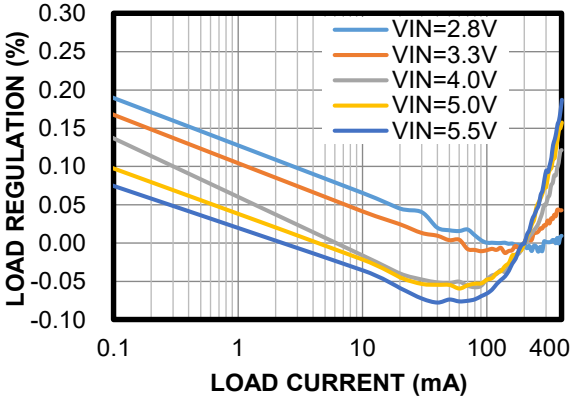
Load Regulation (LDO 3)

V_{OUT3} = 1.8V, C_{OUT3} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



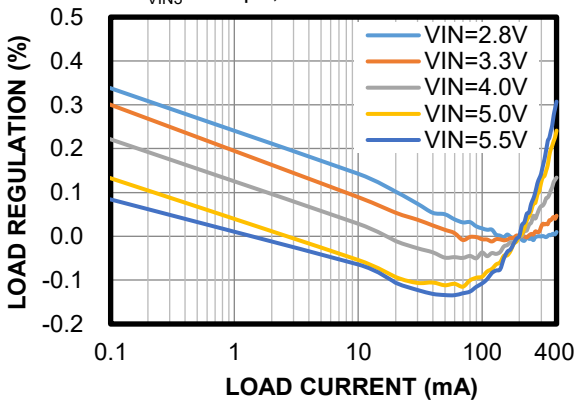
Load Regulation (LDO 4)

V_{OUT4} = 0.75V, C_{OUT4} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



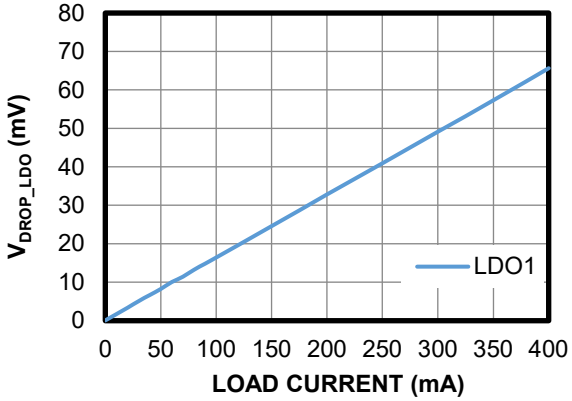
Load Regulation (LDO 5)

V_{OUT5} = 1.8V, C_{OUT5} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



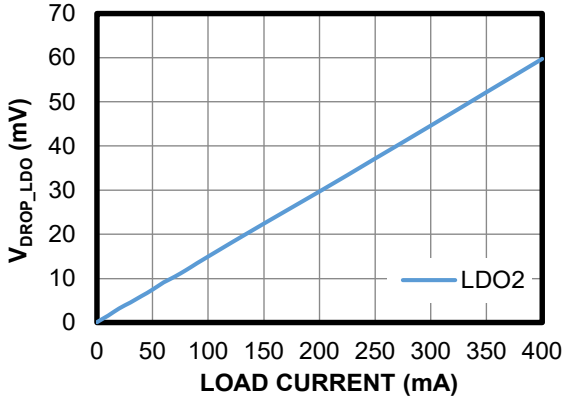
Load Dropout Voltage (LDO1)

V_{IN} = 3.2V, V_{OUT1} = 3.3V, C_{OUT1} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



Load Dropout Voltage (LDO2)

V_{IN} = 3.2V, V_{OUT2} = 3.3V, C_{OUT2} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled

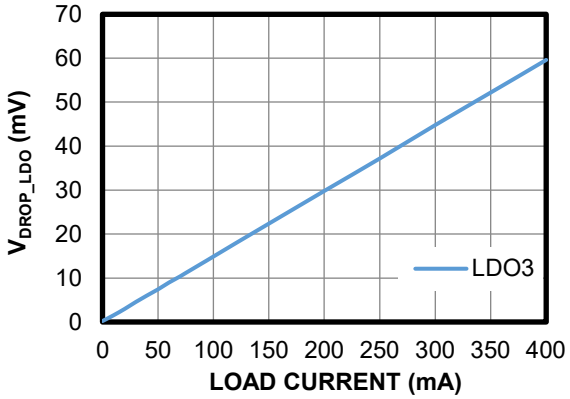


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

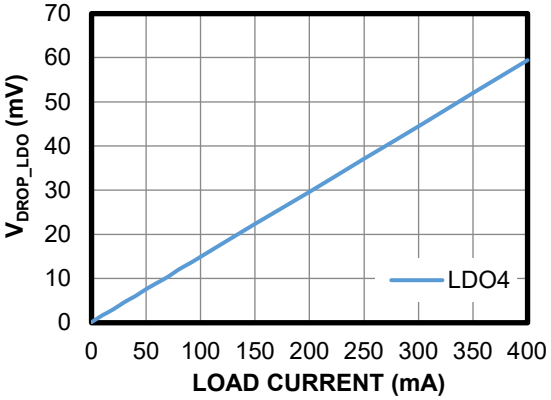
Load Dropout Voltage (LDO3)

V_{IN} = 3.2V, V_{OUT3} = 3.3V, C_{OUT3} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



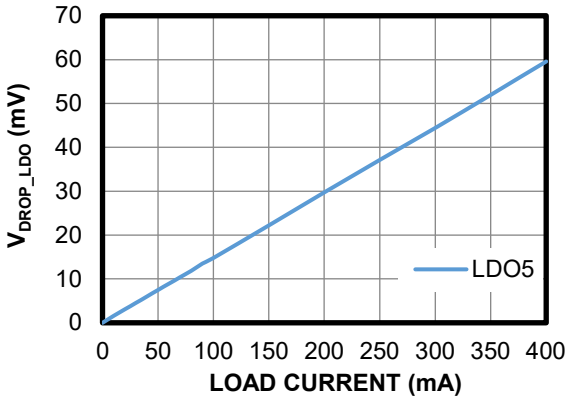
Load Dropout Voltage (LDO4)

V_{IN} = 3.2V, V_{OUT4} = 3.3V, C_{OUT4} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



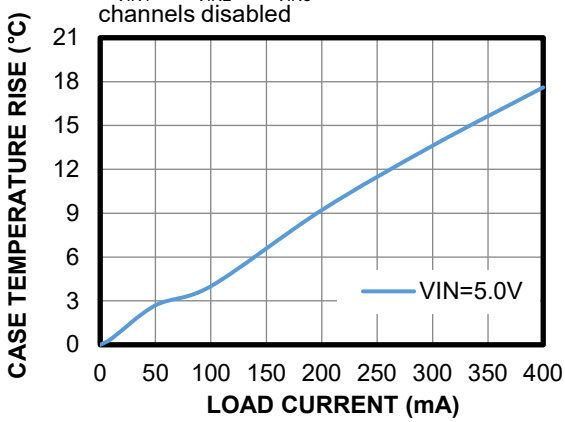
Load Dropout Voltage (LDO5)

V_{IN} = 3.2V, V_{OUT5} = 3.3V, C_{OUT5} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



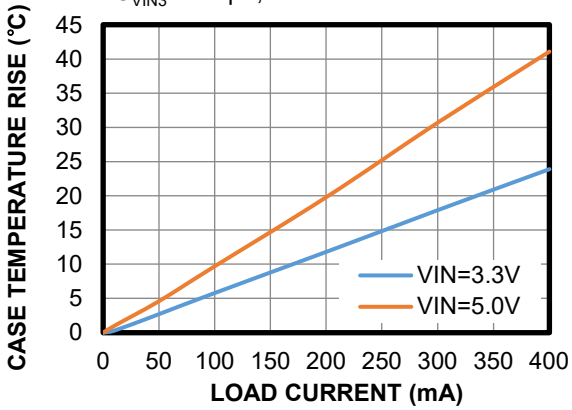
Case Temperature Rise (LDO1)

V_{IN} = 5V, V_{OUT1} = 3.3V, C_{OUT1} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



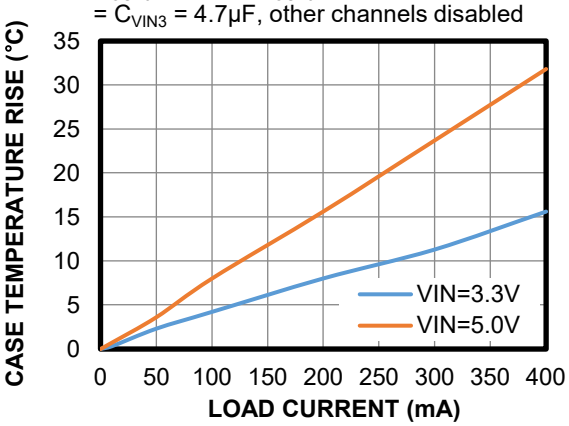
Case Temperature Rise (LDO2)

V_{OUT2} = 0.75V, C_{OUT2} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



Case Temperature Rise (LDO3)

V_{OUT3} = 0.75V, C_{OUT3} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled

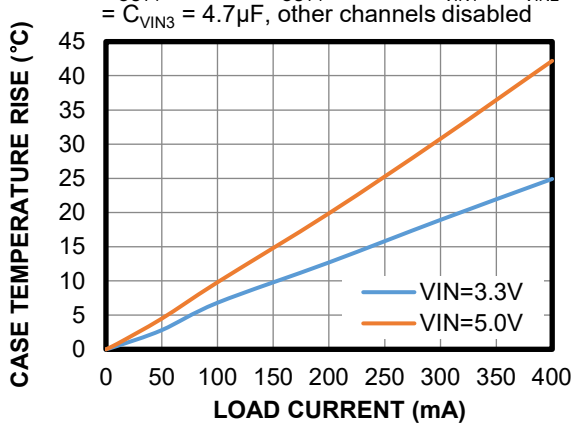


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

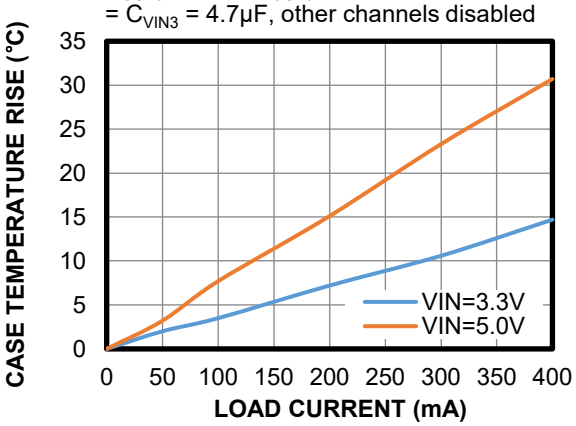
Case Temperature Rise (LDO4)

V_{OUT4} = 0.75V, C_{OUT4} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



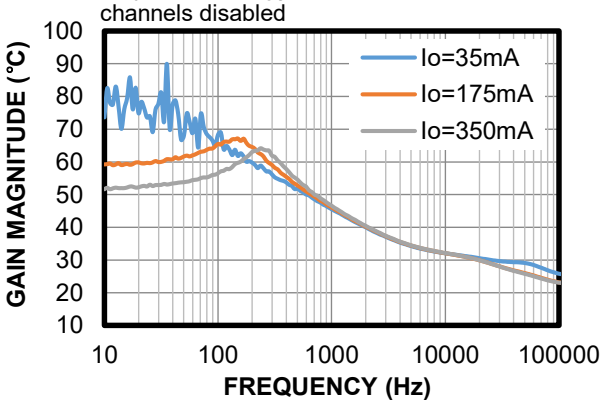
Case Temperature Rise (LDO5)

V_{OUT5} = 1.8V, C_{OUT5} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



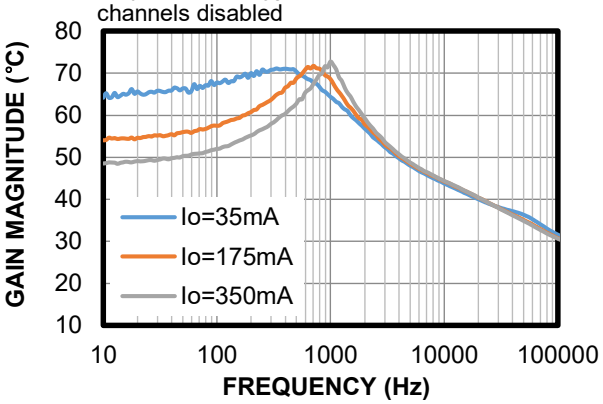
LDO1 PSRR

$V_{IN1/3}$ = 3.3V + sine ripple, V_{IN2} = 3.3V, V_{OUT1} = 1.8V, C_{IN1} = 2 x 100nF, C_{IN2} = 100nF, C_{IN3} = 100nF, C_{OUT1} = 4.7µF + 100nF, other channels disabled



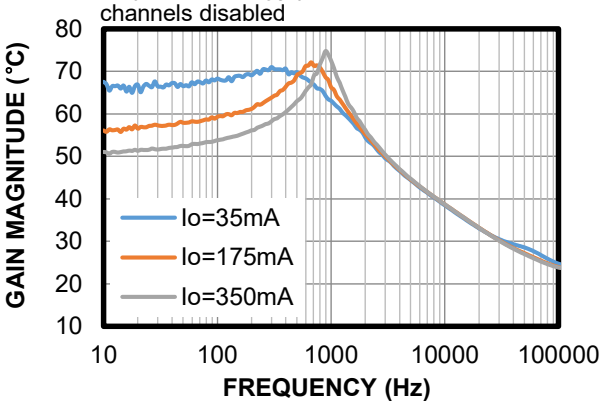
LDO2 PSRR

$V_{IN1/3}$ = 3.3V, V_{IN2} = 3.3V + sine ripple, V_{OUT2} = 1.8V, C_{IN1} = 100nF, C_{IN2} = 3 x 220nF, C_{IN3} = 100nF, C_{OUT2} = 4.7µF + 100nF, other channels disabled



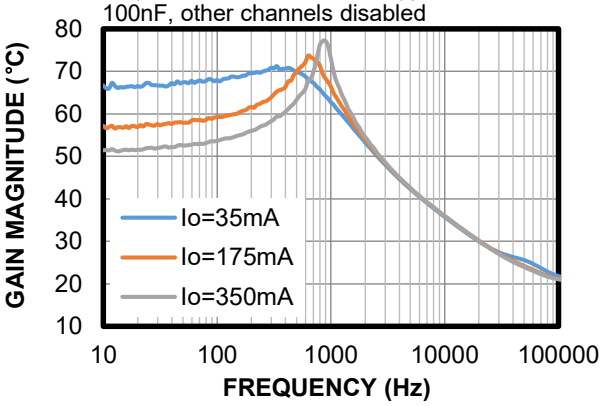
LDO3 PSRR

$V_{IN1/3}$ = 3.3V, V_{IN2} = 3.3V + sine ripple, V_{OUT3} = 1.8V, C_{IN1} = 100nF, C_{IN2} = 3 x 220nF, C_{IN3} = 100nF, C_{OUT3} = 4.7µF + 100nF, other channels disabled



LDO4 PSRR

$V_{IN1/2}$ = 3.3V, V_{IN3} = 3.3V + sine ripple, V_{OUT4} = 1.8V, C_{IN1} = 100nF, C_{IN2} = 100nF, C_{IN3} = 2 x 100nF + 220nF, C_{OUT4} = 4.7µF + 100nF, other channels disabled

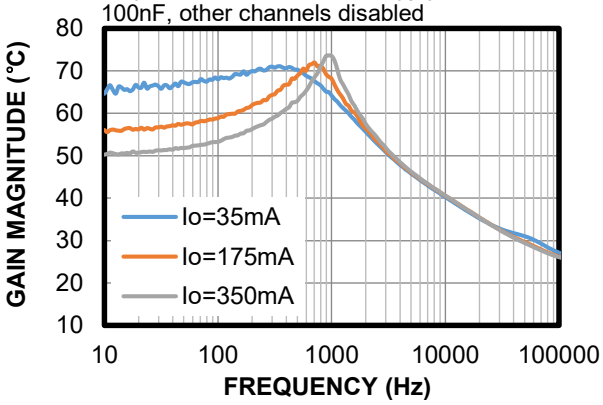


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

LDO5 PSRR

$V_{IN1/2}$ = 3.3V, V_{IN3} = 3.3V + sine ripple, V_{OUT5} = 1.8V, C_{IN1} = 100nF, C_{IN2} = 100nF, C_{IN3} = 2 x 100nF + 220nF, C_{OUT5} = 4.7µF + 100nF, other channels disabled

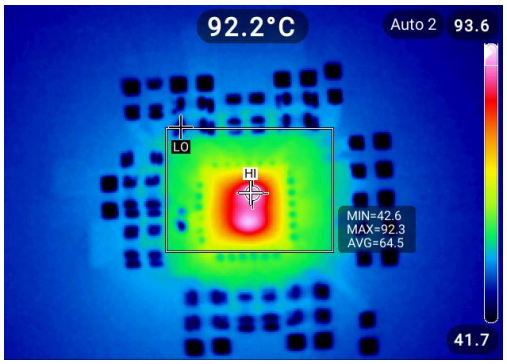


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

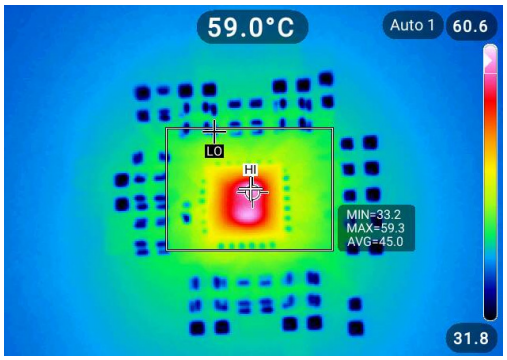
Thermal Performance

V_{IN} = 3.5V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 400mA, no forced airflow, T_A = 25.4°C, T_{CASE} = 92.2°C



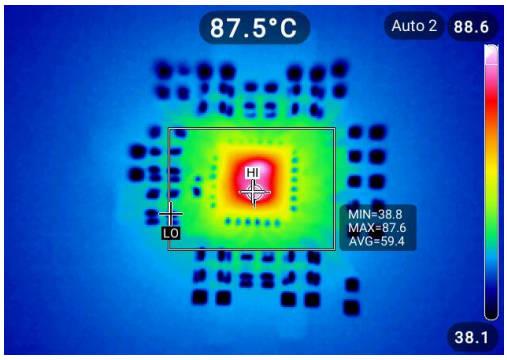
Thermal Performance

V_{IN} = 3.5V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 200mA, no forced airflow, T_A = 25.4°C, T_{CASE} = 59.3°C



Thermal Performance

V_{IN} = 5V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 200mA, no forced airflow, T_A = 25.4°C, T_{CASE} = 87.6°C

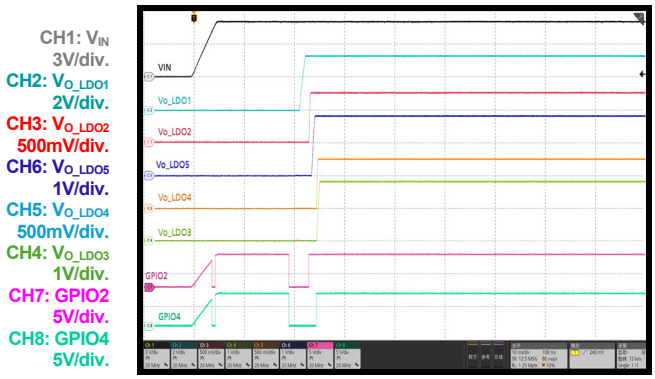


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

Start-Up through VIN

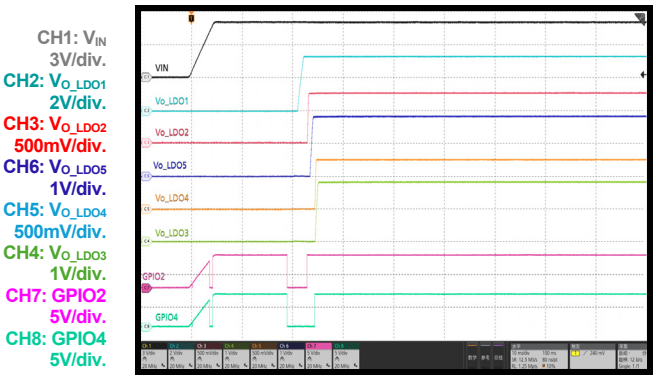
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A



10ms/div.

Start-Up through VIN

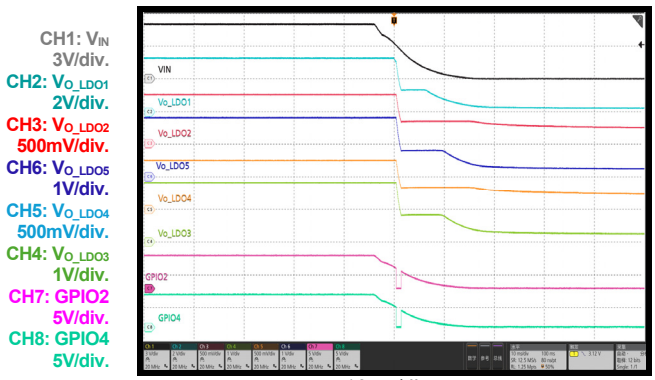
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A



10ms/div.

Shutdown through VIN

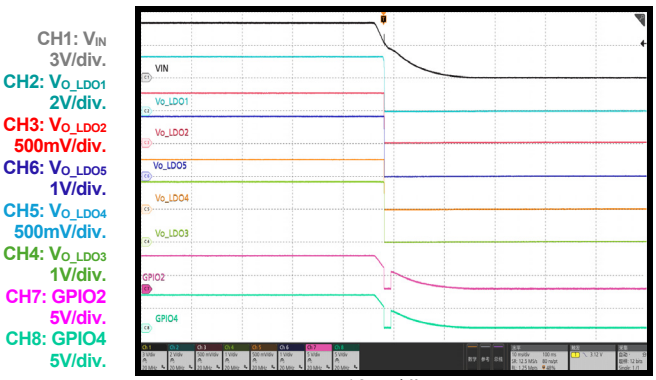
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A



10ms/div.

Shutdown through VIN

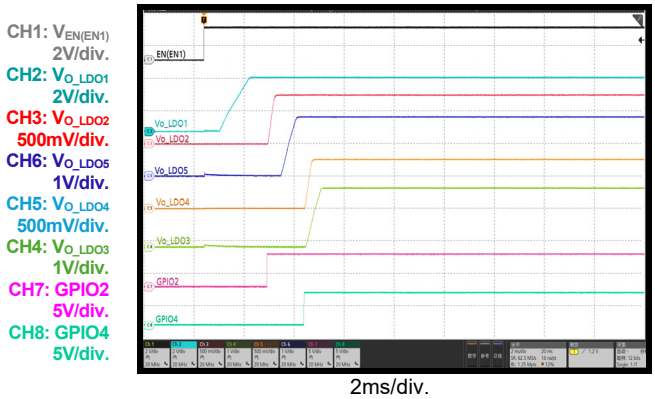
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A



10ms/div.

Start-Up through EN (EN1)

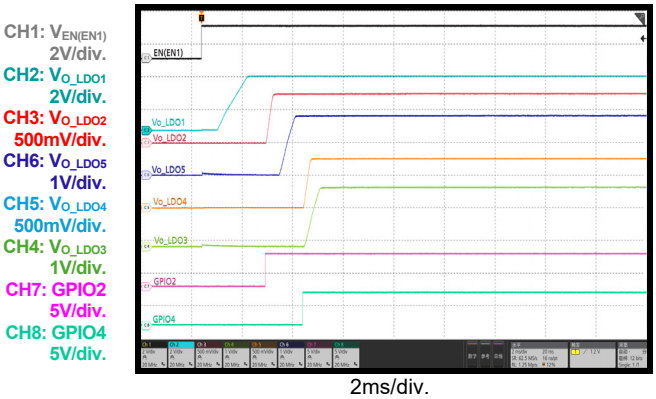
$V_{GPIO1(EN2)}$ = 5V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A



2ms/div.

Start-Up through EN (EN1)

$V_{GPIO1(EN2)}$ = 5V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A



2ms/div.

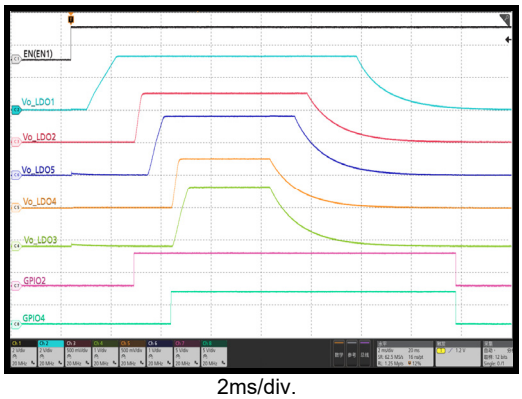
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

Start-Up through EN (EN1)

$V_{GPIO1(EN2)}$ = 0V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

CH1: $V_{EN(EN1)}$ 2V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.

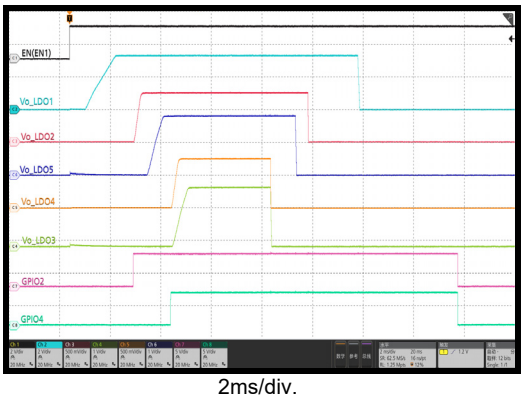


2ms/div.

Start-Up through EN (EN1)

$V_{GPIO1(EN2)}$ = 0V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

CH1: $V_{EN(EN1)}$ 2V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.

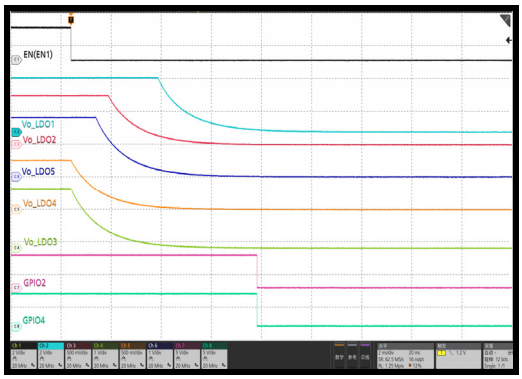


2ms/div.

Shutdown through EN (EN1)

$V_{GPIO1(EN2)}$ = 5V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

CH1: $V_{EN(EN1)}$ 2V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.

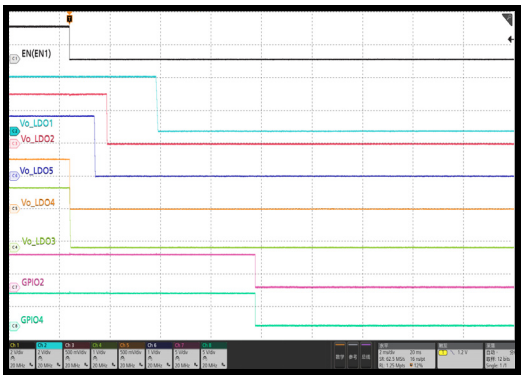


2ms/div.

Shutdown through EN (EN1)

$V_{GPIO1(EN2)}$ = 5V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

CH1: $V_{EN(EN1)}$ 2V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.

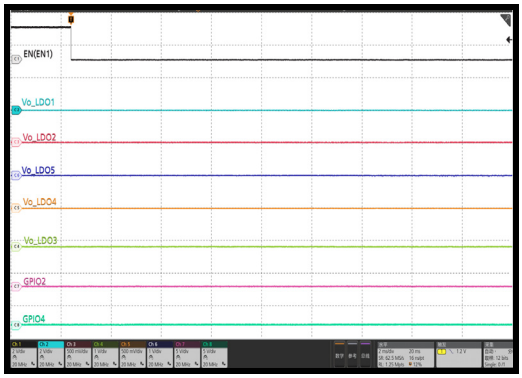


2ms/div.

Shutdown through EN (EN1)

$V_{GPIO1(EN2)}$ = 0V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

CH1: $V_{EN(EN1)}$ 2V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.

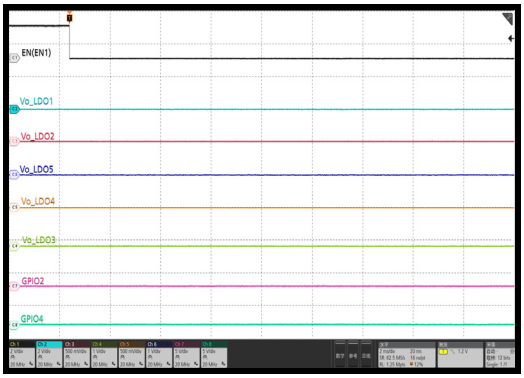


2ms/div.

Shutdown through EN (EN1)

$V_{GPIO1(EN2)}$ = 0V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

CH1: $V_{EN(EN1)}$ 2V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.



2ms/div.

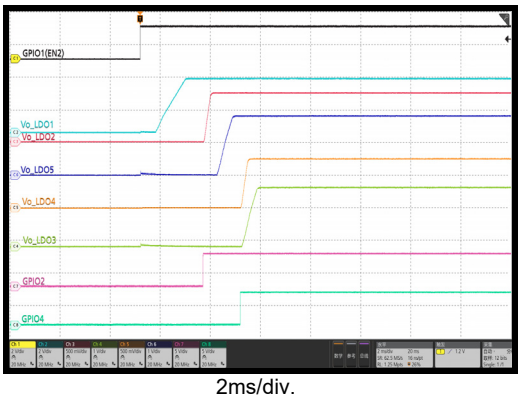
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

Start-Up through GPIO1 (EN2)

$V_{EN(EN1)}$ = 5V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

CH1: $V_{GPO1(EN2)}$ 2V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.

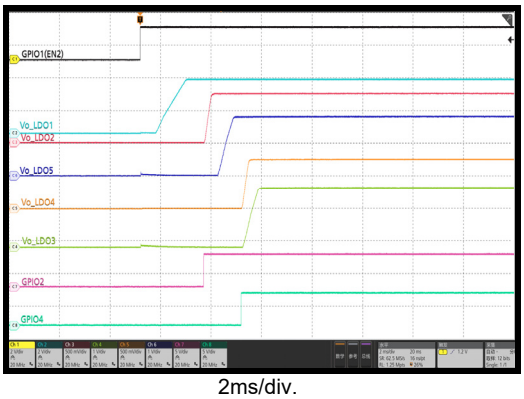


2ms/div.

Start-Up through GPIO1 (EN2)

$V_{EN(EN1)}$ = 5V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

CH1: $V_{GPO1(EN2)}$ 2V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.

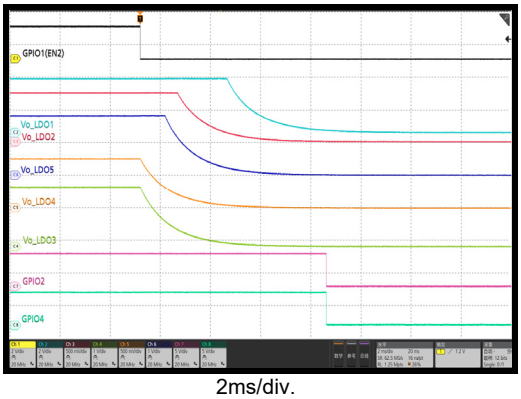


2ms/div.

Shutdown through GPIO1 (EN2)

$V_{EN(EN1)}$ = 5V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

CH1: $V_{GPO1(EN2)}$ 2V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.

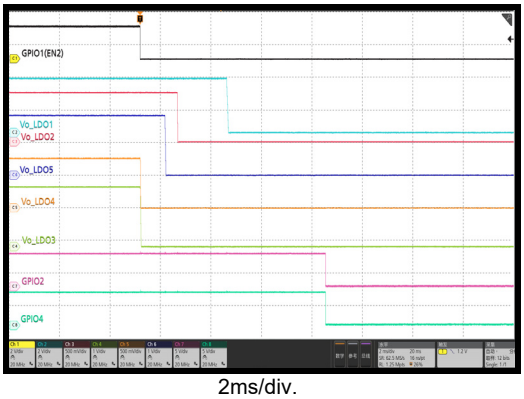


2ms/div.

Shutdown through GPIO1 (EN2)

$V_{EN(EN1)}$ = 5V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

CH1: $V_{GPO1(EN2)}$ 2V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.

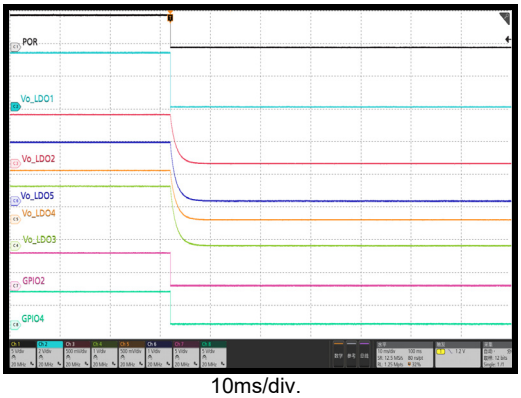


2ms/div.

SCP Entry (LDO1)

Configured part enters failsafe after LDO1 SCP entry, I_{OUT1} = 0A to SCP, other I_{OUT} = 0A

CH1: V_{POR} 2V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.

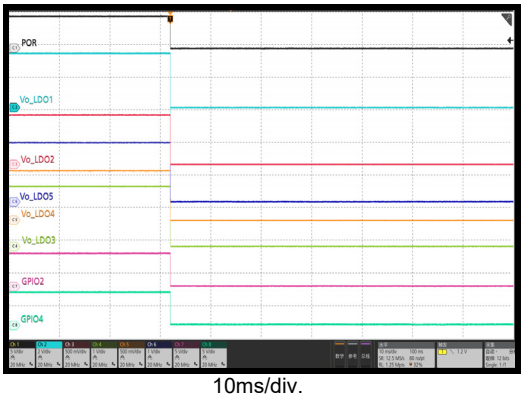


10ms/div.

SCP Entry (LDO1)

Configured part enters failsafe after LDO1 SCP entry, I_{OUT1} = 0.4A to SCP, other I_{OUT} = 0.4A

CH1: V_{POR} 2V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.



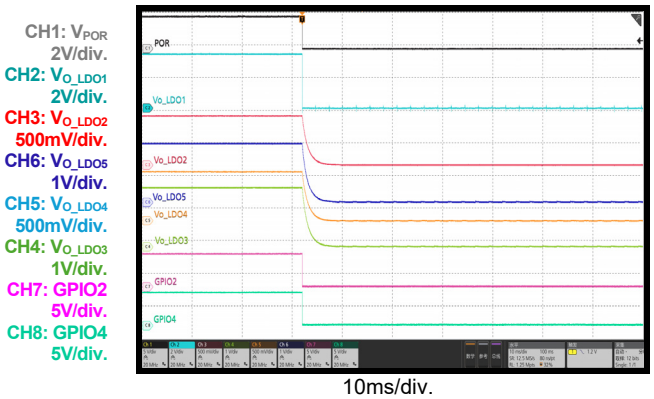
10ms/div.

EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted .

SCP Entry (LDO1)

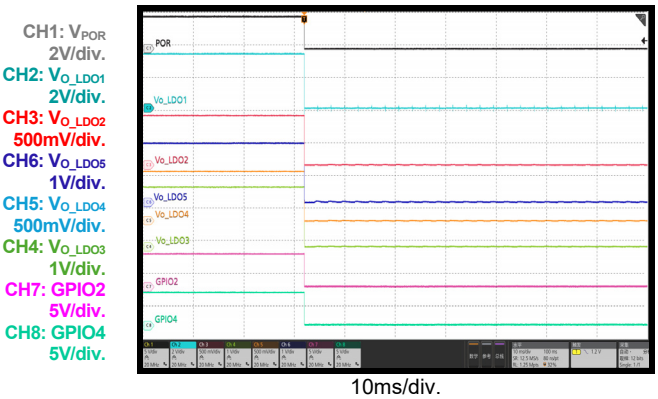
Configured part enters fail-recovery after LDO1 SCP entry, I_{OUT1} = 0A to SCP, other I_{OUT} = 0A



10ms/div.

SCP Entry (LDO1)

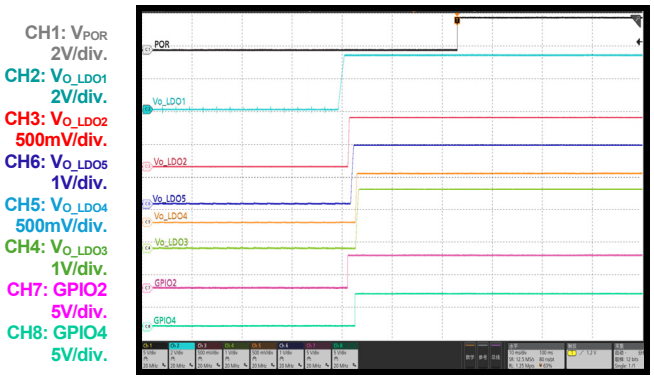
Configured part enters fail-recovery after LDO1 SCP entry, I_{OUT1} = 0.4A to SCP, other I_{OUT} = 0.4A



10ms/div.

SCP Recovery (LDO1)

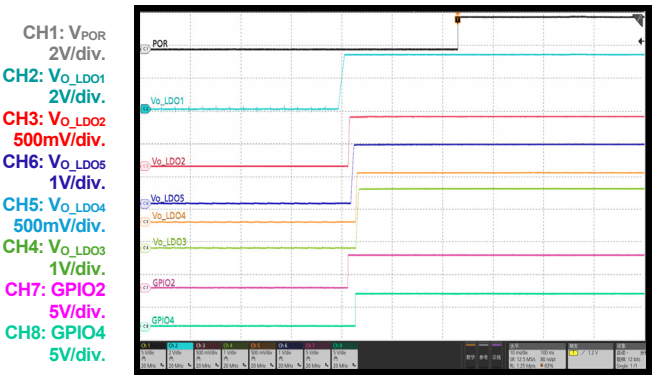
Configured part enters fail-recovery after LDO1 SCP entry, I_{OUT1} = SCP to 0A, other I_{OUT} = 0A



10ms/div.

SCP Recovery (LDO1)

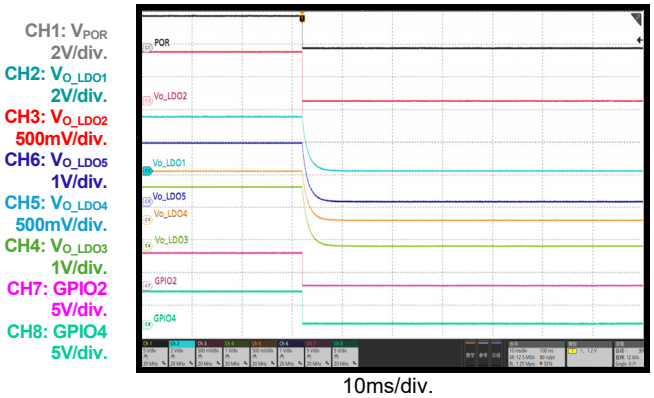
Configured part enters fail-recovery after LDO1 SCP entry, I_{OUT1} = SCP to 0.4A, other I_{OUT} = 0.4A



10ms/div.

SCP Entry (LDO2)

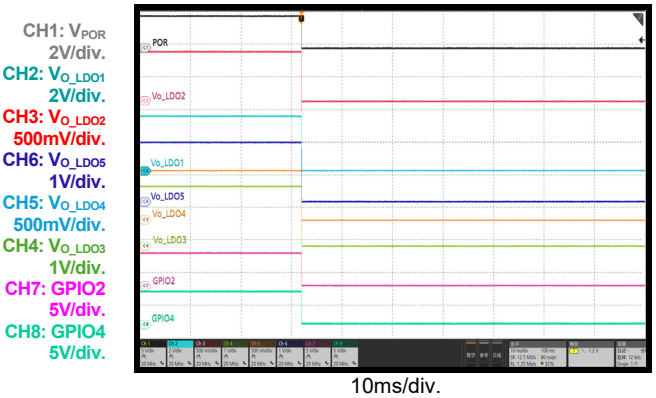
Configured part enters failsafe after LDO2 SCP entry, I_{OUT2} = 0A to SCP, other I_{OUT} = 0A



10ms/div.

SCP Entry (LDO2)

Configured part enters failsafe after LDO2 SCP entry, I_{OUT2} = 0.4A to SCP, other I_{OUT} = 0.4A



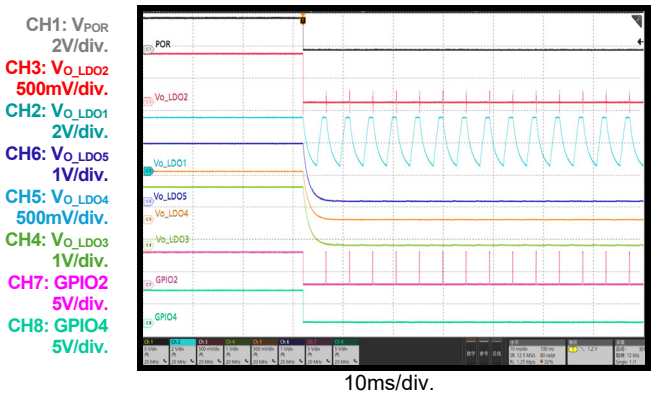
10ms/div.

EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

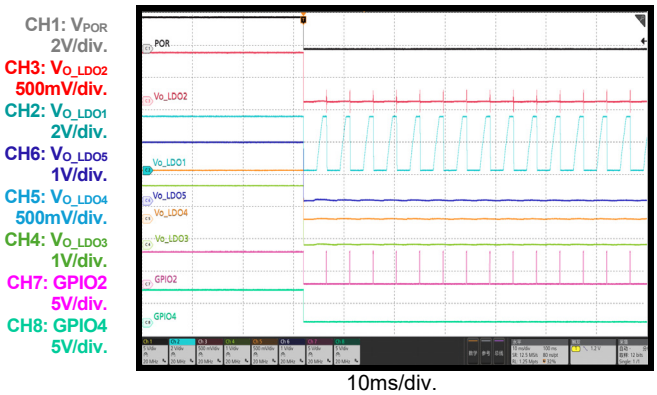
SCP Entry (LDO2)

Configured part enters fail-recovery after LDO2 SCP entry, I_{OUT2} = 0A to SCP, other I_{OUT} = 0A



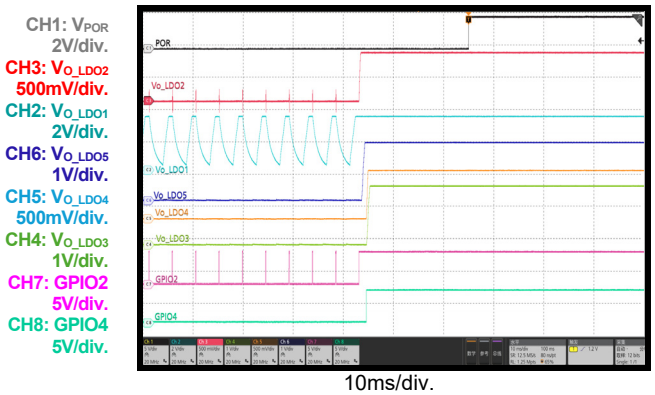
SCP Entry (LDO2)

Configured part enters fail-recovery after LDO2 SCP entry, I_{OUT2} = 0.4A to SCP, other I_{OUT} = 0.4A



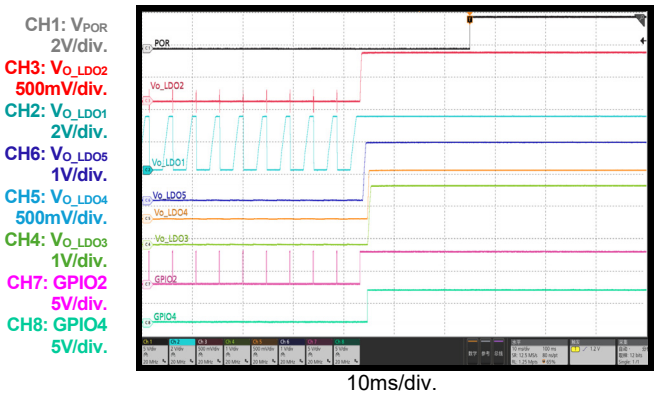
SCP Recovery (LDO2)

Configured part enters fail-recovery after LDO2 SCP entry, I_{OUT2} = 0A to SCP, other I_{OUT} = 0A



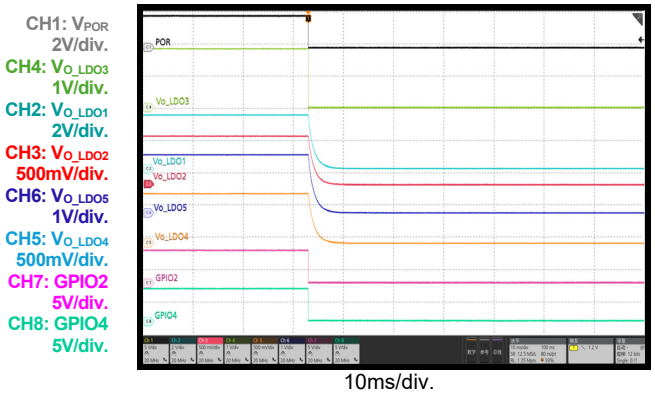
SCP Recovery (LDO2)

Configured part enters fail-recovery after LDO2 SCP entry, I_{OUT2} = 0.4A to SCP, other I_{OUT} = 0.4A



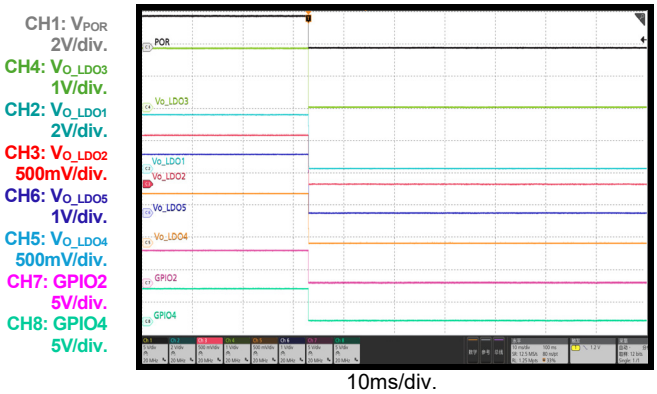
SCP Entry (LDO3)

Configured part enters failsafe after LDO3 SCP entry, I_{OUT3} = 0A to SCP, other I_{OUT} = 0A



SCP Entry (LDO3)

Configured part enters failsafe after LDO3 SCP entry, I_{OUT3} = 0.4A to SCP, other I_{OUT} = 0.4A



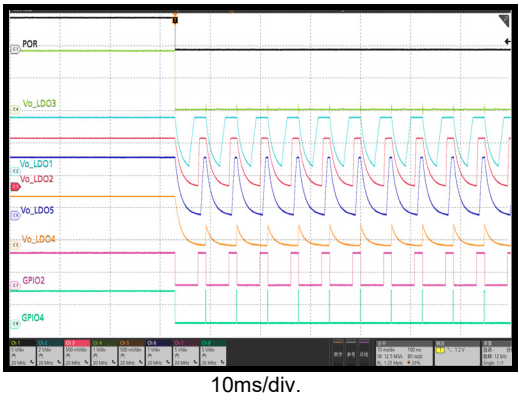
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

SCP Entry (LDO3)

Configured part enters fail-recovery after LDO3 SCP entry, I_{OUT3} = 0A to SCP, other I_{OUT}= 0A

CH1: V_{POR} 2V/div.
CH4: V_{O_LDO3} 1V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.

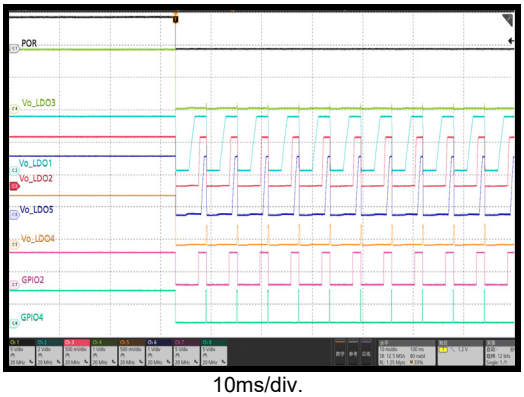


10ms/div.

SCP Entry (LDO3)

Configured part enters fail-recovery after LDO3 SCP entry, I_{OUT3} = 0.4A to SCP, other I_{OUT} = 0.4A

CH1: V_{POR} 2V/div.
CH4: V_{O_LDO3} 1V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.

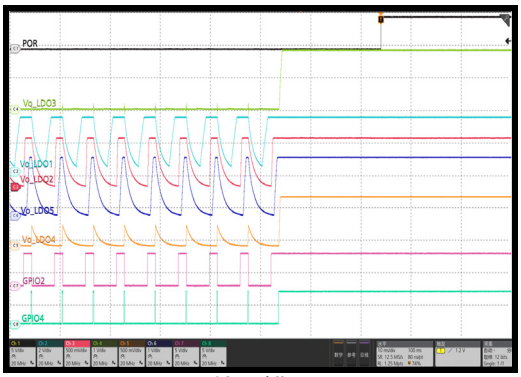


10ms/div.

SCP Recovery (LDO3)

Configured part enters fail-recovery after LDO3 SCP entry, I_{OUT3} = 0A to SCP, other I_{OUT} = 0A

CH1: V_{POR} 2V/div.
CH4: V_{O_LDO3} 1V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.

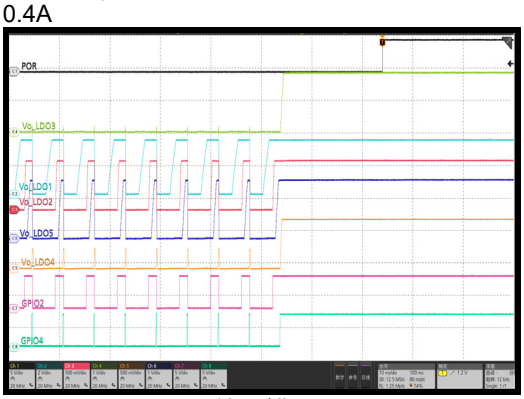


10ms/div.

SCP Recovery (LDO3)

Configured part enters fail-recovery after LDO3 SCP entry, I_{OUT3} = 0.4A to SCP, other I_{OUT} = 0.4A

CH1: V_{POR} 2V/div.
CH4: V_{O_LDO3} 1V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.

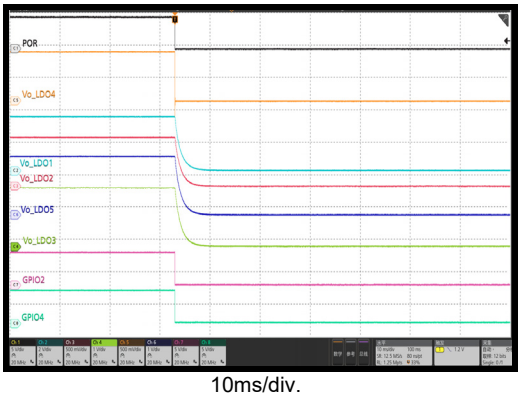


10ms/div.

SCP Entry (LDO4)

Configured part enters failsafe after LDO4 SCP entry, I_{OUT4} = 0A to SCP, other I_{OUT} = 0A

CH1: V_{POR} 2V/div.
CH5: V_{O_LDO4} 500mV/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH6: V_{O_LDO5} 1V/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.

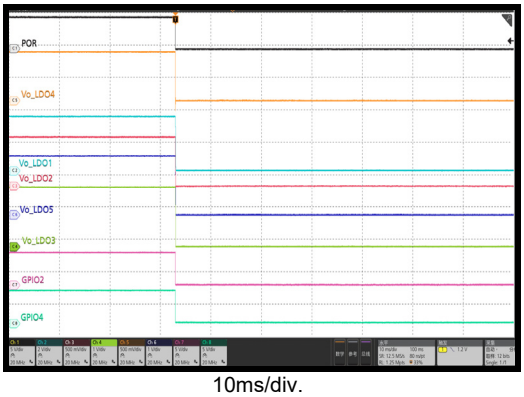


10ms/div.

SCP Entry (LDO4)

Configured part enters failsafe after LDO4 SCP entry, I_{OUT4} = 0.4A to SCP, other I_{OUT} = 0.4A

CH1: V_{POR} 2V/div.
CH5: V_{O_LDO4} 500mV/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH6: V_{O_LDO5} 1V/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.



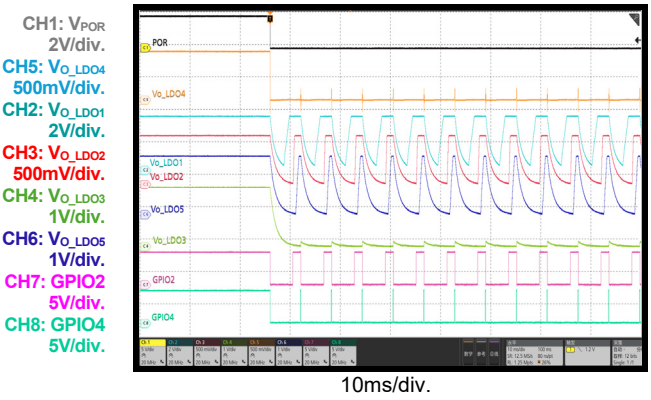
10ms/div.

EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

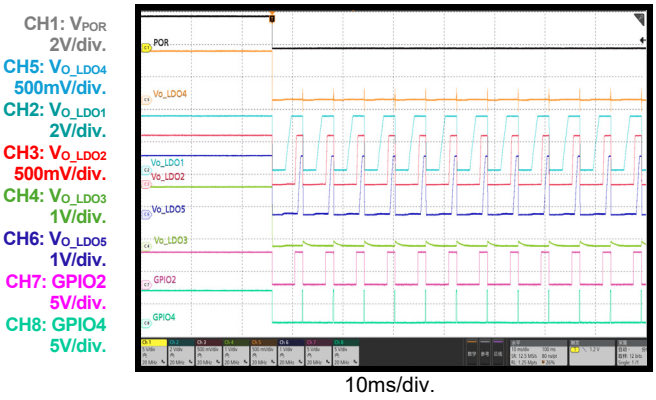
SCP Entry (LDO4)

Configured part enters fail-recovery after LDO4 SCP entry, I_{OUT4} = 0A to SCP, other I_{OUT} = 0A



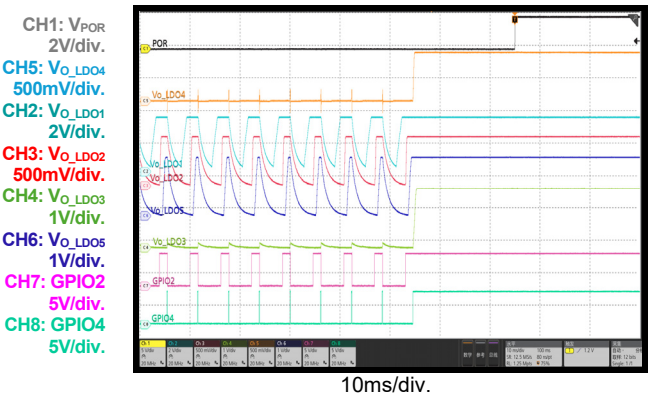
SCP Entry (LDO4)

Configured part enters fail-recovery after LDO4 SCP entry, I_{OUT4} = 0.4A to SCP, other I_{OUT} = 0.4A



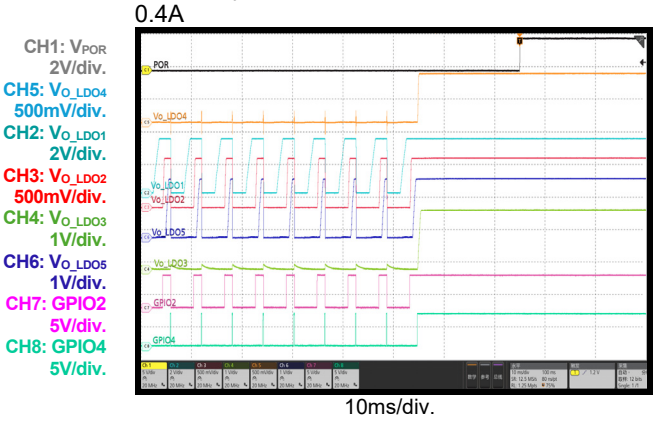
SCP Recovery (LDO4)

Configured part enters fail-recovery after LDO4 SCP entry, I_{OUT4} = 0A to SCP, other I_{OUT} = 0A



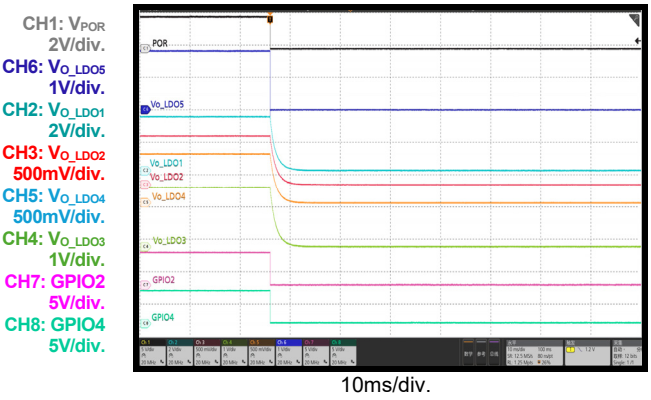
SCP Recovery (LDO4)

Configured part enters fail-recovery after LDO4 SCP entry, I_{OUT4} = 0.4A to SCP, other I_{OUT} = 0.4A



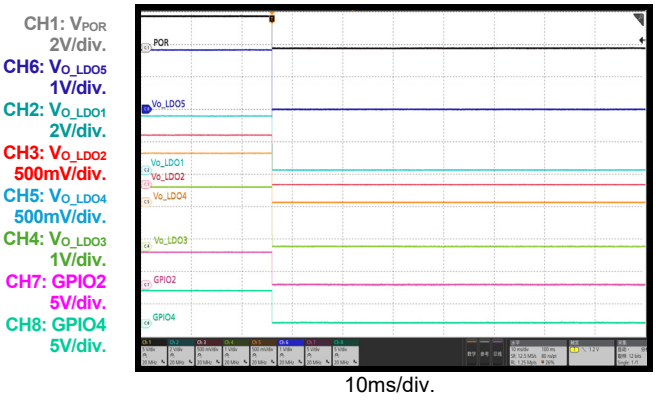
SCP Entry (LDO5)

Configured part enters failsafe after LDO5 SCP entry, I_{OUT5} = 0A to SCP, other I_{OUT} = 0A



SCP Entry (LDO5)

Configured part enters failsafe after LDO5 SCP entry, I_{OUT5} = 0.4A to SCP, other I_{OUT} = 0.4A

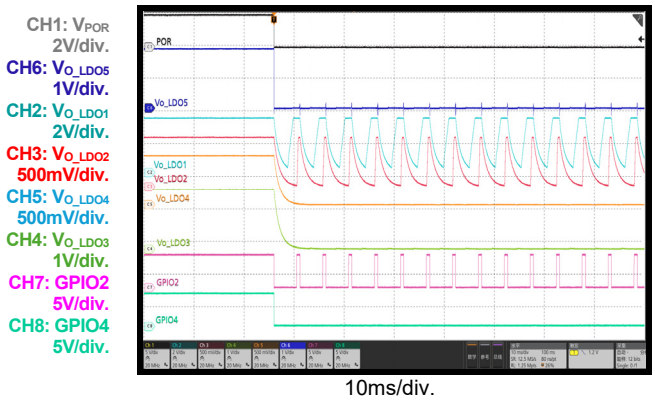


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

SCP Entry (LDO5)

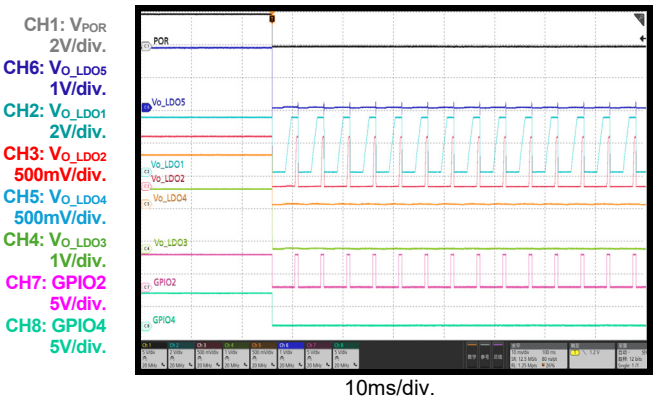
Configured part enters fail-recovery after LDO5 SCP entry, I_{OUT5} = 0A to SCP, other I_{OUT} = 0A



10ms/div.

SCP Entry (LDO5)

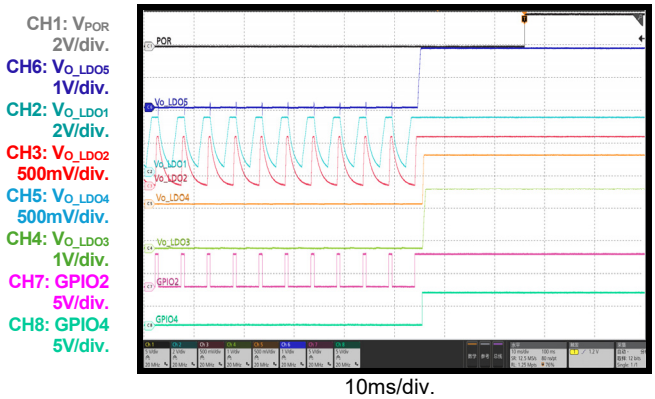
Configured part enters fail-recovery after LDO5 SCP entry, I_{OUT5} = 0.4A to SCP, other I_{OUT} = 0.4A



10ms/div.

SCP Recovery (LDO5)

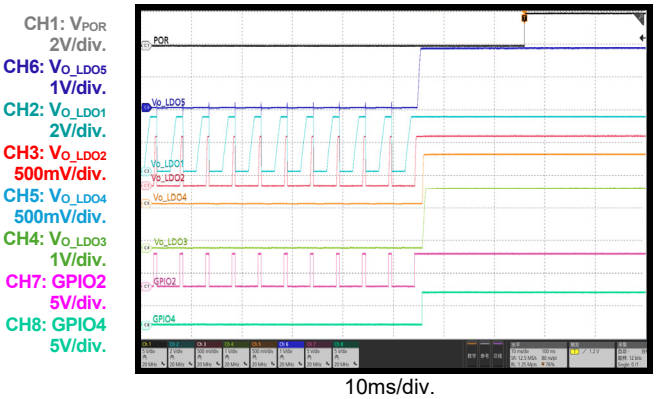
Configured part enters fail-recovery after LDO5 SCP entry, I_{OUT5} = 0A to SCP, other I_{OUT} = 0A



10ms/div.

SCP Recovery (LDO5)

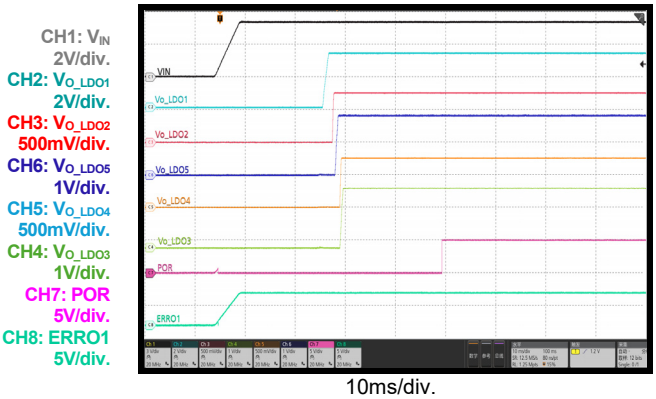
Configured part enters fail-recovery after LDO5 SCP entry, I_{OUT5} = 0.4A to SCP, other I_{OUT} = 0.4A



10ms/div.

Start-Up through VIN (POR and ERRO1)

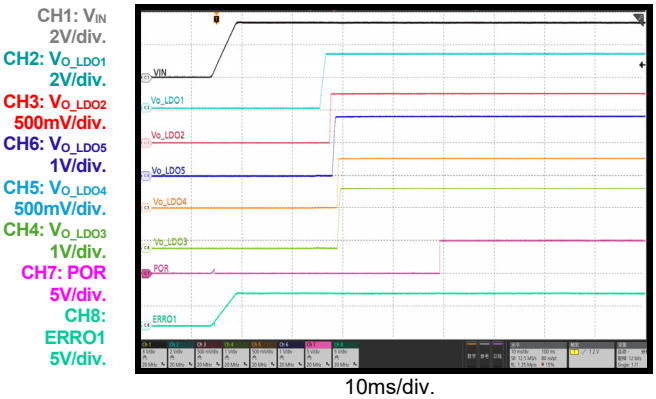
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A



10ms/div.

Start-Up through VIN (POR and ERRO1)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A



10ms/div.

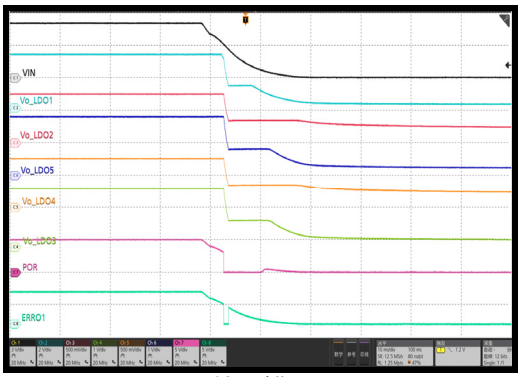
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

Shutdown through VIN (POR and ERRO1)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

CH1: V_{IN} 2V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.

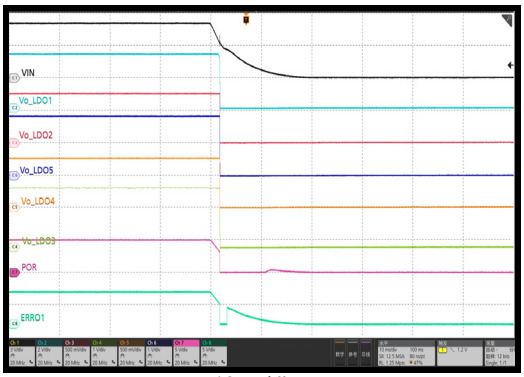


10ms/div.

Shutdown through VIN (POR and ERRO1)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

CH1: V_{IN} 2V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.

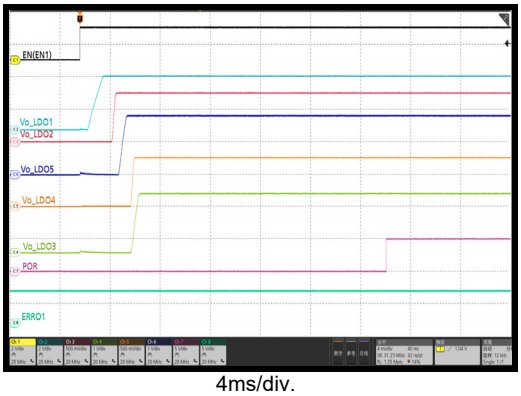


10ms/div.

Start-Up through EN (EN1) (POR and ERRO1)

$V_{GPIO1(EN2)}$ = 5V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

CH1: $V_{EN(EN1)}$ 2V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.

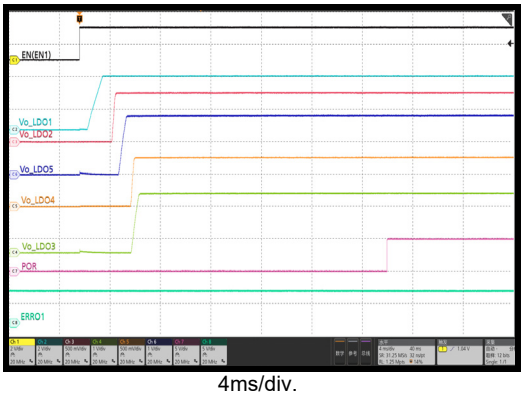


4ms/div.

Start-Up through EN (EN1) (POR and ERRO1)

$V_{GPIO1(EN2)}$ = 5V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

CH1: $V_{EN(EN1)}$ 2V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.

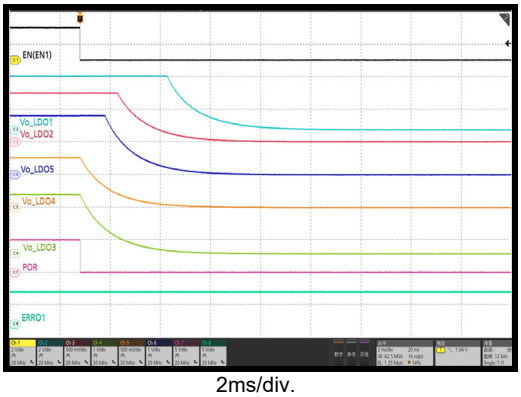


4ms/div.

Shutdown through EN (EN1) (POR and ERRO1)

$V_{GPIO1(EN2)}$ = 5V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

CH1: $V_{EN(EN1)}$ 2V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.

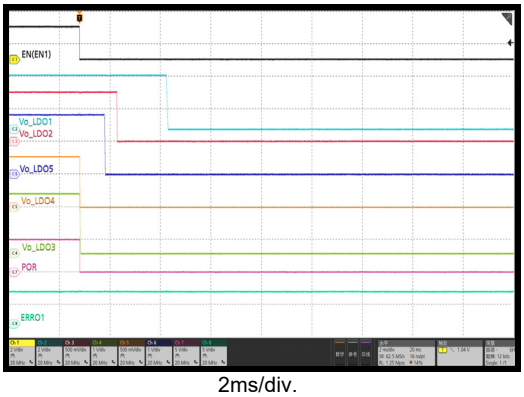


2ms/div.

Shutdown through EN (EN1) (POR and ERRO1)

$V_{GPIO1(EN2)}$ = 5V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

CH1: $V_{EN(EN1)}$ 2V/div.
CH2: V_{O_LDO1} 2V/div.
CH3: V_{O_LDO2} 500mV/div.
CH6: V_{O_LDO5} 1V/div.
CH5: V_{O_LDO4} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.



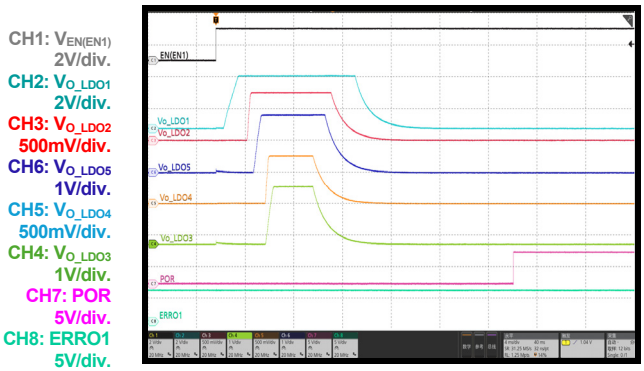
2ms/div.

EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

Start-Up through EN (EN1) (POR and ERRO1)

$V_{GPIO1(EN2)}$ = 0V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A



4ms/div.

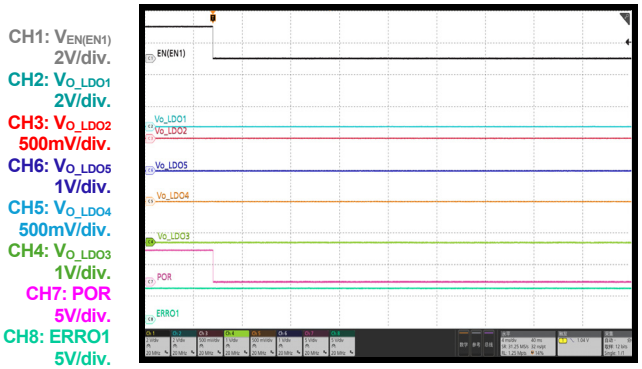
Start-Up through EN (EN1) (POR and ERRO1)

$V_{GPIO1(EN2)}$ = 0V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

4ms/div.

Shutdown through EN (EN1) (POR and ERRO1)

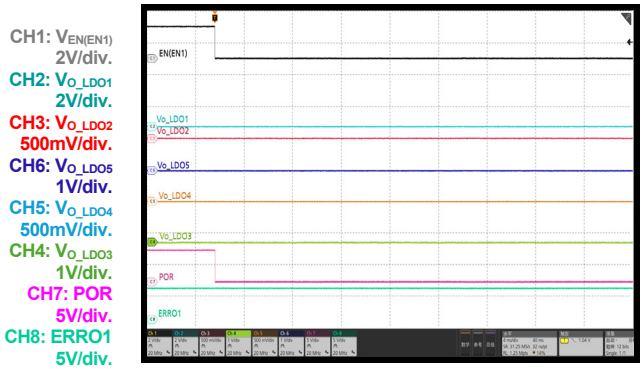
$V_{GPIO1(EN2)}$ = 0V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A



4ms/div.

Shutdown through EN (EN1) (POR and ERRO1)

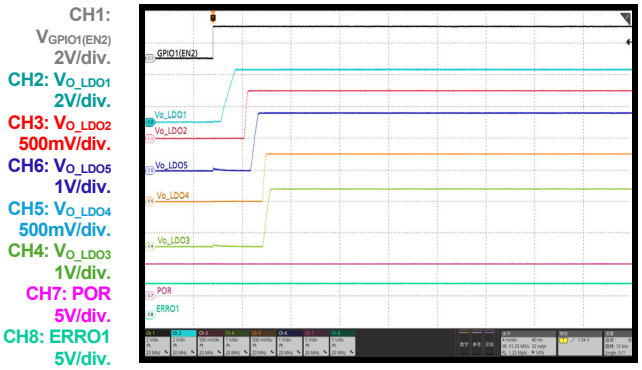
$V_{GPIO1(EN2)}$ = 0V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A



4ms/div.

Start-Up through GPIO1 (EN2) (POR and ERRO1)

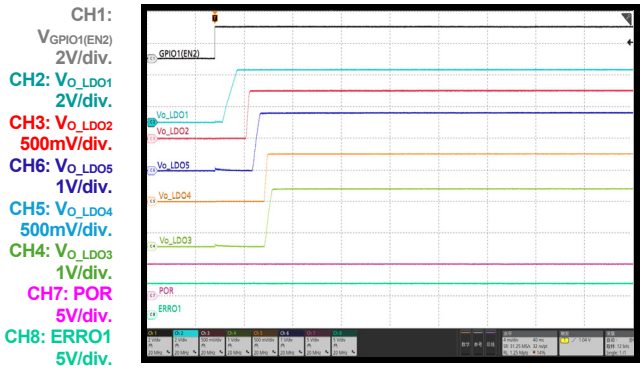
$V_{EN(EN1)}$ = 5V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A



4ms/div.

Start-Up through GPIO1 (EN2) (POR and ERRO1)

$V_{EN(EN1)}$ = 5V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A



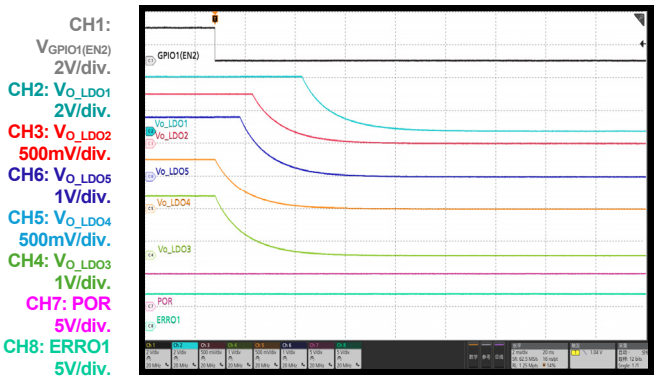
4ms/div.

EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

Shutdown through GPIO1 (EN2) (POR and ERRO1)

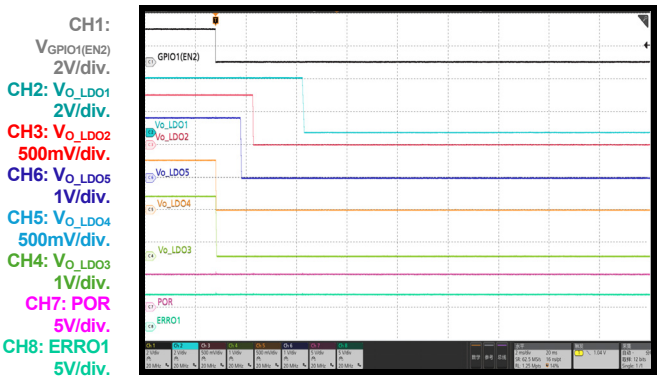
$V_{EN(EN1)}$ = 5V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A



2ms/div.

V Shutdown through GPIO1 (EN2) (POR and ERRO1)

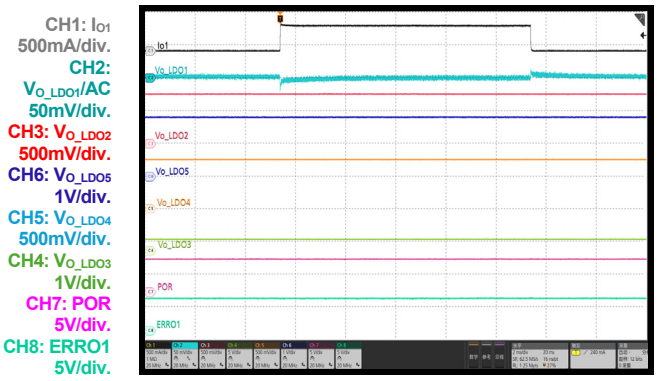
$V_{EN(EN1)}$ = 5V, I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A



2ms/div.

Load Transient (LDO1)

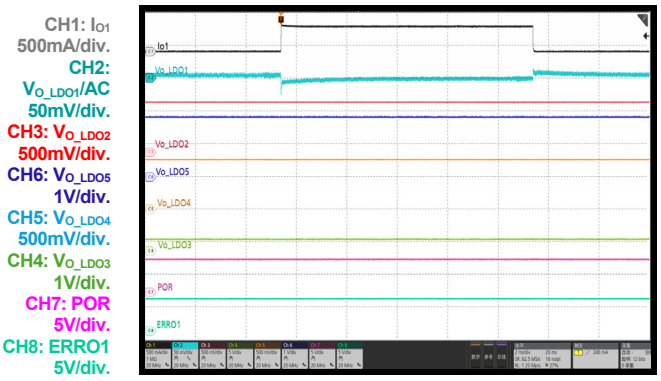
I_{OUT1} = 0A to 0.4A, 2A/µs slew rate, I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A



2ms/div.

Load Transient (LDO1)

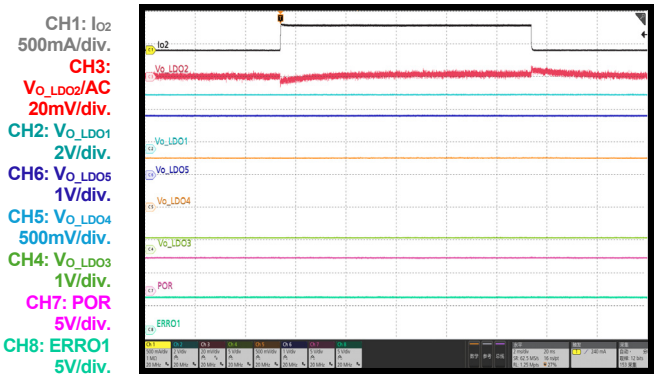
I_{OUT1} = 0A to 0.4A, 2A/µs slew rate, I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A



2ms/div.

Load Transient (LDO2)

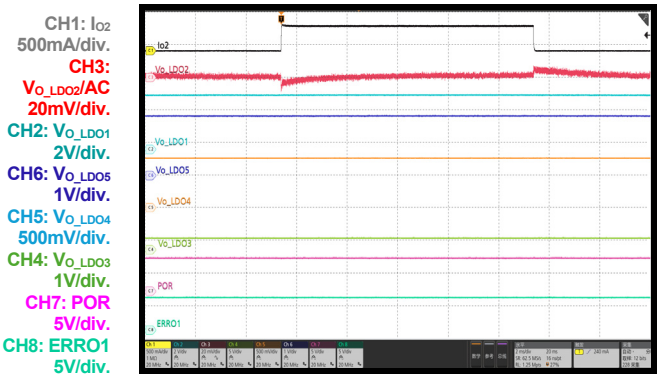
I_{OUT2} = 0A to 0.4A, 2A/µs slew rate, I_{OUT1} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A



2ms/div.

Load Transient (LDO2)

I_{OUT2} = 0A to 0.4A, 2A/µs slew rate, I_{OUT1} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A



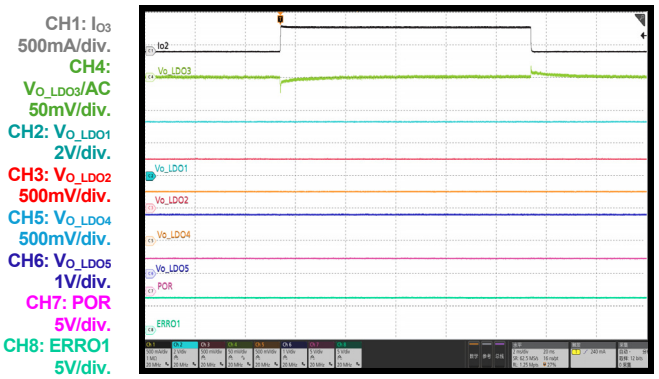
2ms/div.

EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

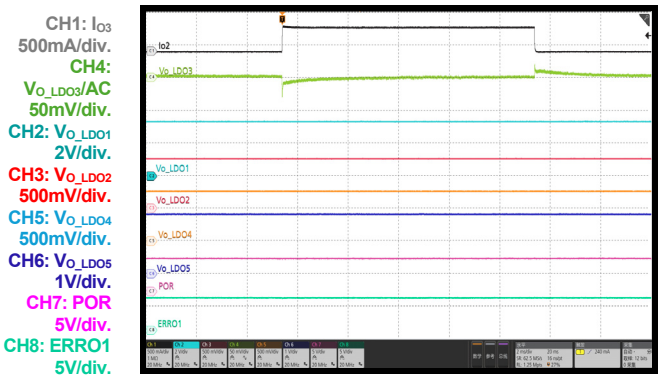
Load Transient (LDO3)

I_{OUT3} = 0A to 0.4A, 2A/µs slew rate,
I_{OUT1} = I_{OUT2} = I_{OUT4} = I_{OUT5} = 0A



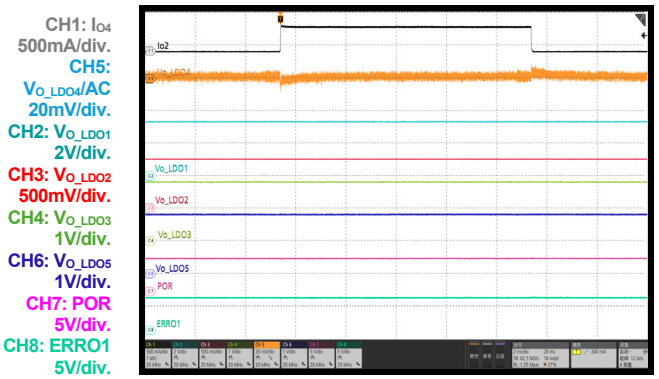
Load Transient (LDO3)

I_{OUT3} = 0A to 0.4A, 2A/µs slew rate,
I_{OUT1} = I_{OUT2} = I_{OUT4} = I_{OUT5} = 0.4A



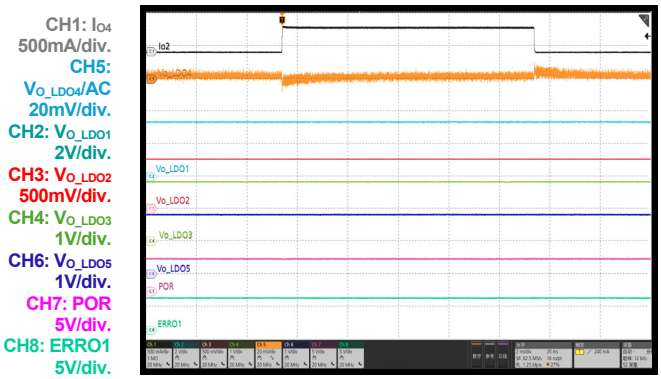
Load Transient (LDO4)

I_{OUT4} = 0A to 0.4A, 2A/µs slew rate,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT5} = 0A



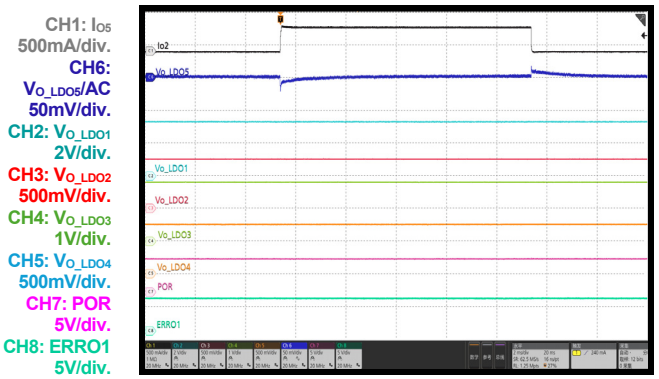
Load Transient (LDO4)

I_{OUT4} = 0A to 0.4A, 2A/µs slew rate,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT5} = 0.4A



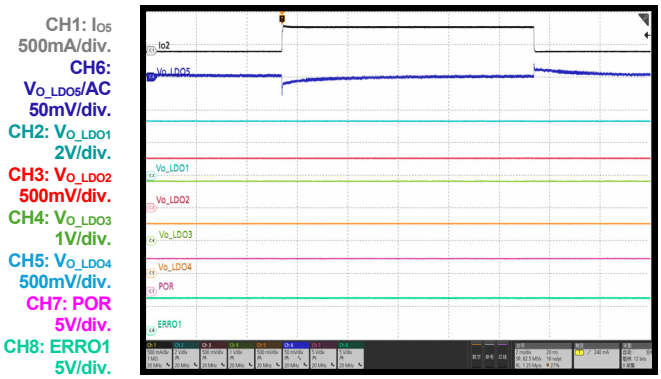
Load Transient (LDO5)

I_{OUT5} = 0A to 0.4A, 2A/µs slew rate,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = 0A



Load Transient (LDO5)

I_{OUT5} = 0A to 0.4A, 2A/µs slew rate,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = 0.4A



PCB LAYOUT (4)

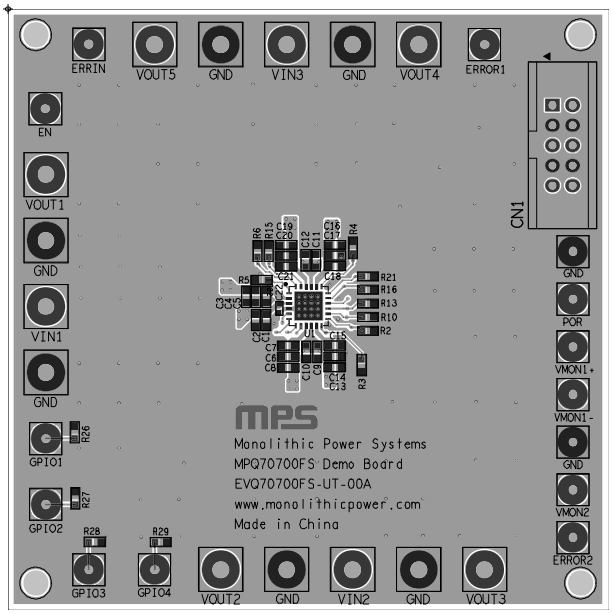


Figure 4: Top Silk and Top Layer

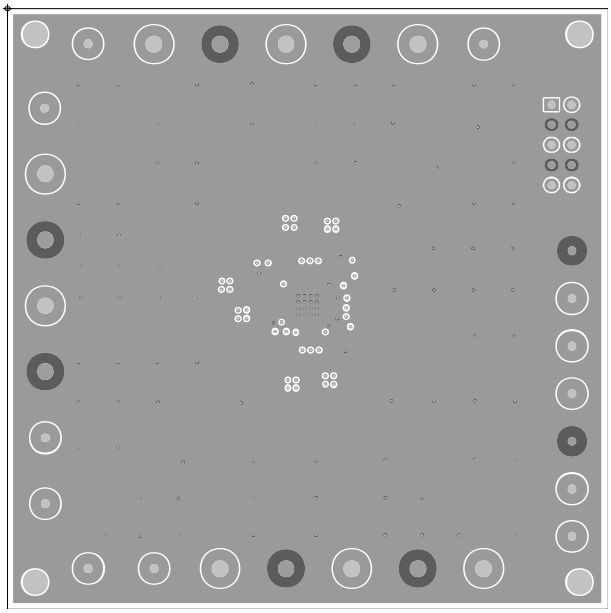


Figure 5: Mid-Layer 1

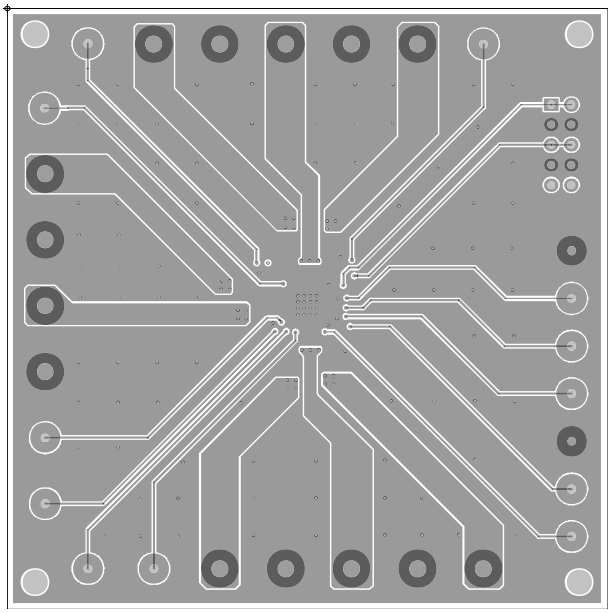


Figure 6: Mid-Layer 2

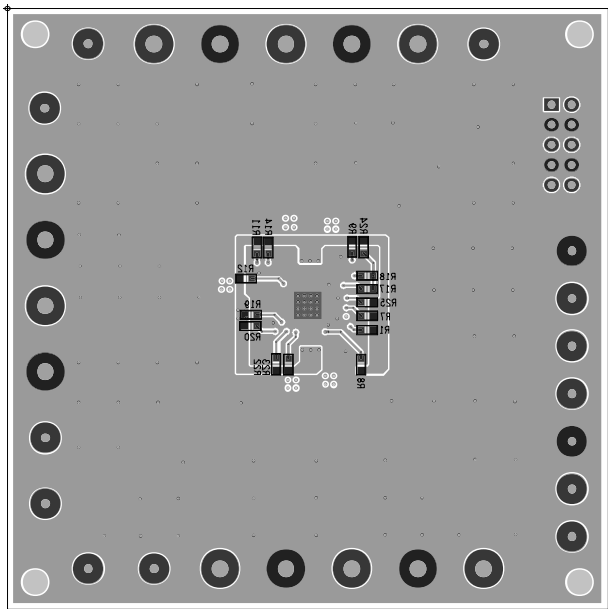


Figure 7: Bottom Layer and Bottom Silk

Note:

3) The EVQ70700FS-UT-00A is a 4-layer PCB with a 2oz copper thickness PCB (7.6cmx7.6cm).

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/11/2025	Initial Release	-