MPQ70700FS

MPSafe™, ASIL-D, 5.5V PMIC with 5 LDOs, 4 GPIOs, and 2 Voltage Monitors for SoCs, AEC-Q100 Qualified

DESCRIPTION

The MPQ70700FS is a functional safety power management IC designed to power a variety of system-on-chips (SoCs) or safety microcontroller units (MCUs) that require multiple low-dropout (LDO) regulators.

Five LDO linear regulators can provide up to 400mA of load current (I_{LOAD}) per channel. Three independent voltage inputs allow different input voltage (V_{IN}) levels to optimize dropout for their respective outputs. The MPQ70700FS provides four GPIO pins that can be used for power sequencing, as well as two voltage monitors, including one differential monitor to monitor two external voltage rails.

Protection features include under-voltage lockout (UVLO), over-current protection (OCP), under-voltage protection (UVP), over-voltage protection (OVP), and thermal shutdown.

Safety mechanisms such as a built-in self-testing (BIST) provide high diagnostic coverage, which help the system achieve its target ASIL rating. The MPQ70700FS is developed under MPS's advanced MPSafe™ Functional Safety Product Development process, which has been independently certified to meet ISO 26262 guidelines.

The I^2C interface with packet error checking (PEC) and integrated one-time programmable (OTP) memory allow for configurability.

The MPQ70700FS is available in a TQFN-25 (5mmx5mm) package with wettable flanks, and is available in AEC-Q100 Grade 1.

FEATURES

- Designed for Automotive Applications
  - 2.8V to 5.5V Operating Input Voltage (V_{INx}) (where x = 1 to 3)
  - -40°C to +150°C Operating Junction Temperature (T_J)
  - Available in AEC-Q100 Grade 1
  - Available in a TQFN-24 (5mmx5mm) Package
  - Available with Wettable Flanks

FEATURES

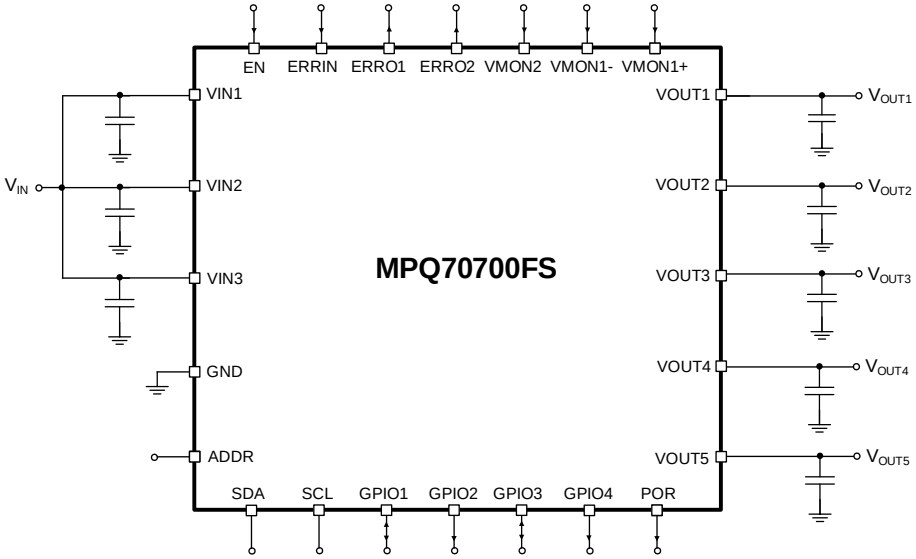
- High Integration Reduces Board Size
  - x5 400mA LDOs
  - x4 GPIOs
    - x2 General-Purpose Input/Output
    - x2 General-Purpose Outputs
    - x2 Voltage Monitors
    - x1 Differential Monitor
    - x1 Single-Ended Monitor
- Comprehensive Protection Features
  - OVP and UVP
  - Over-Current Protection (OCP)
  - Thermal Shutdown Protection
  - Power-On Reset (POR) and Error Indicator
  - Error Signal Input Detection
  - I^2C Interface with PEC
- Configurability for Flexibility
  - Multi-Page OTP Memory
  - Adjustable Output Voltage (V_{OUT}) via Registers
  - Configurable Sequencing
- Functional Safety
  - ISO 26262 ASIL-D Hardware Capable
  - Built-In Self-Testing (BIST)
  - Over-Voltage (OV) and Under-Voltage (UV) Monitor
  - Clock Monitor
  - Window and Q&A Watchdog Timer
  - Protected Registers
  - Documents Available for ISO 26262 System Design
  - Failure Modes Effects and Diagnostic Analysis (FMEDA)
  - Safety Manual

MPSafe™ Developed for Functional Safety Applications: ISO 26262 Compliant

APPLICATIONS

- Automotive Advanced Driver-Assistance System (ADAS) System-on-Chips (SoCs)
- Safety Microcontroller Units (MCUs)
- General-Purpose Secondary Regulation

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating***
MPQ70700FSGUTE-xxxxAEC1**,****	TQFN-24 (5mmx5mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ70700FSGUTE-xxxxAEC1-Z).

** “xxxx” is the configuration code identifier for the register settings stored in the OTP register. The default code is “0001”. Contact an MPS FAE to create this unique number.

*** Moisture Sensitivity Level Rating

**** Wettable Flanks

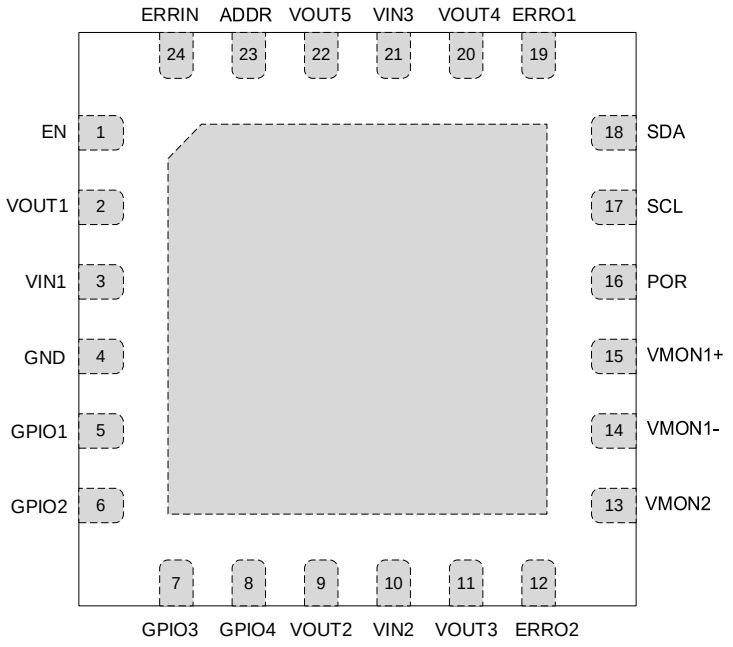
TOP MARKING

MPSYYWW
MP70700
LLLLLLL
E

MPS: MPS prefix
YY: Year code
WW: Week code
MP70700: Part number
LLLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE

TOP VIEW



TQFN-24 (5mmx5mm)

PIN FUNCTIONS

Pin #	Name	Type	Description
1	EN	I	**Power management IC (PMIC) enable.** EN is the input pin that controls power-up or power-down on the channels. If the EN pin voltage (V_{EN}) exceeds 1.3V, then all the low-dropout (LDO) regulators (LDO1, LDO2, LDO3, LDO4, and LDO5) and the GPIO pins (GPIO1, GPIO2, GPIO3, and GPIO4) initiate the power-up sequence. If V_{EN} drops below 0.4V, then the MPQ70700 enters the power-down sequence.
2	VOUT1	PWR	**LDO1 output.** The VOUT1 pin is powered by the LDO1 and internal circuit supply input voltage (V_{IN1}). See the VREF_LDO1 (21h) command on page 87 for the LDO1 output voltage (V_{OUT1}) setting. A 4.7µF ceramic capacitor is recommended for the output. If VOUT1 is not used, disable LDO1 via the CHANNEL_EN (18h) command, then float the pin.
3	VIN1	PWR	**LDO1 and internal circuit supply input voltage.** The three VIN pins (VIN1, VIN2, and VIN3) are not connected together internally. For functional safety, all VIN pins must start up at the same time and test safety-related functions. The MPQ70700FS operates from a 2.8V to 5.5V input rail. A 470nF ceramic capacitor (0402) must be placed as close as possible between the VIN1 and GND pins to decouple the input rail. Meanwhile, place a 1µF to 10µF ceramic capacitor between the VIN1 pin and ground. VIN1 is the main input of the PMIC, supply for LDO1, and the internal circuit. If V_{IN1}, V_{IN2}, and V_{IN3} exceed their respective under-voltage lockout (UVLO) thresholds, then the MPQ70700FS can work normally. It is recommended to connect all the VIN pins using a wide PCB trace if there is no special input requirement.
4	GND	GND	**Power ground.** Connect the GND pin to power ground using a single trace.
5	GPIO1	I/O	**General-purpose input/output (I/O) 1.** GPIO1 is an open-drain pin, and can be configured as an input pin or output pin via the GPIO_CFG (1Bh) command. Input: If configured as an input pin, GPIO1 can enable the LDOs' output voltage (V_{OUTx}) (where x = 1 to 5) channels and other GPIO outputs (where GPIO2, GPIO3, and GPIO4 are the output pins) via the EN2_GROUP (17h) command. In sleep mode, when the GPIO1 input voltage (V_{GPIO1}) exceeds 1.3V, the controller's LDO regulators (LDO1, LDO2, LDO3, LDO4, and LDO5) and other GPIO outputs (where GPIO2, GPIO3, and GPIO4 are the output pins) initiate the sleep mode exit sequence. In active state, when V_{GPIO1} drops below 0.4V, the controller's LDO regulators and GPIO pins initiate the sleep mode entry sequence. Output: If configured as an output pin, a pull-up resistor (e.g. 100kΩ) must be added between the GPIO1 pin and a power supply (e.g. V_{OUT1}). GPIO1 is used as the sequencer output, and configures the power-up and power-down timing sequences via the SEQ_GPIO1 (1Dh) command. If not used, configure GPIO1 as the output and connect the pin to ground.
6	GPIO2	O	**General-purpose output 2.** GPIO2 is an open-drain pin. It is used as the sequencer output, and configures the power-up and power-down timing sequences via the SEQ_GPIO2 (1Eh) command. GPIO2 should be connected to a power supply (e.g. V_{OUT1}) via a resistor (e.g. 100kΩ). If it is not used, connect the pin to ground.
7	GPIO3	I/O	**General-purpose I/O 3.** GPIO3 is an open-drain pin, and can be configured as an input pin or output pin via the GPIO_CFG (1Bh) command. Input: If configured as an input pin, then GPIO3's input voltage controls V_{OUT1}. V_{OUT1} is 3.3V when GPIO3 is pulled down below 0.4V, and V_{OUT1} is 1.8V when the GPIO3 pin voltage (V_{GPIO3}) exceeds 1.3V. Output: If configured as an output pin, GPIO3 is used as the sequencer output, and configures the power-up and power-down timing sequences via the SEQ_GPIO3 (1Fh) command. GPIO3 should be connected to a power supply (e.g. V_{OUT1}) via a resistor (e.g. 100kΩ). If not used, configure GPIO3 as the output and connect the pin to ground.

PIN FUNCTIONS *(continued)*

Pin #	Name	Type	Description
8	GPIO4	O	**General-purpose output 4.** GPIO4 is an open-drain pin. It is used as the sequencer output, and configures the power-up and power-down timing sequences via the SEQ_GPIO4 (1Fh) command. GPIO4 should be connected to a power supply (e.g. V_{OUT1}) via a resistor (e.g. 100kΩ). If it is not used, connect the pin to ground.
9	VOUT2	PWR	**LDO2 output.** The VOUT2 pin is powered by the LDO2 and LDO3 supply voltage input voltage (V_{IN2}). See the VREF_LDO2 (24h) command on page 89 for the LDO2 output voltage (V_{OUT2}) setting. A 4.7µF ceramic capacitor is recommended for the output. If VOUT2 is not used, disable LDO2 via the CHANNEL_EN (18h) command, then float the pin.
10	VIN2	PWR	**LDO2 and LDO3 supply input voltage.** The three VIN pins (VIN1, VIN2, and VIN3) are not connected together internally. For functional safety, all VIN pins must start up at the same time and test safety-related functions. The MPQ70700 operates from a 2.8V to 5.5V input rail, and requires a ceramic capacitor to decouple the input rail. In addition, place a 1µF to 10µF ceramic capacitor between the VIN2 pin and ground. VIN2 can be used separately from VIN1, but all VIN pins must power up at the same time. It is recommended to connect all VIN pins using a wide PCB trace if there is no special input requirement.
11	VOUT3	PWR	**LDO3 output.** The VOUT3 pin is powered by V_{IN2}. See the VREF_LDO3 (27h) command on page 90 for the LDO3 output voltage (V_{OUT3}) setting. A 4.7µF ceramic capacitor is recommended for the output. If VOUT3 is not used, disable LDO3 via the CHANNEL_EN (18h) command, then float the pin.
12	ERRO2	O	**Open-drain error output 2.** An external pull-up resistor (e.g. 100kΩ) is required to connect the ERRO2 pin to power supply rail (e.g. V_{IN1}). This pin asserts active low if a related error occurs. If ERRO2 is not used, then connect this pin to ground.
13	VMON2	I	**Monitor input 2.** The VMON2 pin can be enabled via the MON2_MODE (3Bh) command. VMON2 can monitor over-voltage (OV) and under-voltage (UV) conditions for external voltages with a configurable threshold. The monitor OV and UV thresholds can be set via the MON2_OV_VTH (39h) and MON2_UV_VTH (3Ah) commands, respectively. If VMON2 is not used, disable the pin, then connect it to ground.
14	VMON1-	I	**Differential monitor negative input 1.** The VMON1- pin sets the negative input of the differential voltage, and can be enabled via the MON1_MODE (38h) command. The VMON1- pin voltage (V_{MON1-}) must be below 0.3V. The differential monitor input voltage 1 (V_{MON1}) can monitor OV and UV conditions for external voltages with a configurable threshold. The monitor OV and UV thresholds can be set via the MON1_OV_VTH (36h) and MON1_UV_VTH (37h) commands, respectively. If VMON1- is not used, disable the pin, then connect it to ground.
15	VMON1+	I	**Differential monitor positive input 1.** The VMON1+ pin sets the positive input of the differential voltage, and can be enabled via the MON1_MODE (38h) command. V_{MON1} can monitor OV and UV conditions for external voltages with a configurable threshold. The monitor OV and UV thresholds can be set via the MON1_OV_VTH (36h) and MON1_UV_VTH (37h) commands, respectively. If VMON1+ is not used, disable the pin, then connect it to ground.

PIN FUNCTIONS *(continued)*

Pin #	Name	Type	Description
16	POR	O	**Power-on reset (POR).** The POR pin is an open-drain error output. An external pull-up resistor (e.g. 100kΩ) is required to connect this pin to a power supply rail (e.g. V_{IN1}). POR is active low by default. After all LDOs' V_{OUTx} exceed the respective POR thresholds, POR must remain asserted low within the POR delay time (t_{POR_DELAY}), which is set via the POR_CTL_DLY (35h) command, before POR reasserts (low to high transition). The POR threshold can be set via the PORx_CTL_CTH commands (where x = 1 to 5) (30h to 34h) for each LDO. If a watchdog failure occurs, then POR inserts a low pulse configured via the WDT_CFG (4Bh) command and holds for a set time (t_{POR_DELAY}) before recovering high. If POR is not used, then connect this pin to ground.
17	SCL	I	**I²C interface clock input.** An external pull-up resistor (e.g. 100kΩ) is required to connect the SCL pin to a 3.3V power supply rail. If SCL is not used, then connect this pin to ground.
18	SDA	I/O	**I²C interface data I/O.** An external pull-up resistor (e.g. 100kΩ) is required to connect the SDA pin to a 3.3V power supply rail. If SDA is not used, then connect this pin to ground.
19	ERRO1	O	**Open-drain error output 1.** An external pull-up resistor (e.g. 100kΩ) is required to connect the ERRO1 pin to the power supply rail (e.g. V_{IN1}). ERRO1 asserts active low if a related error occurs. If ERRO1 is not used, then connect this pin to ground.
20	VOUT4	PWR	**LDO4 output.** The VOUT4 pin is powered by the LDO4 and LDO5 supply input voltage (V_{IN3}). See the VREF_LDO4 (2Ah) command for the LDO4 output voltage (V_{OUT4}) setting. A 4.7µF ceramic capacitor is recommended for the output. If VOUT4 is not used, disable LDO4 via the CHANNEL_EN (18h) command, then float this pin.
21	VIN3	PWR	**LDO4 and LDO5 supply input voltage.** The three VIN pins (VIN1, VIN2, and VIN3) are not connected together internally. For functional safety, all VIN pins must start up at the same time and test safety-related functions. The MPQ70700FS operates from a 2.8V to 5.5V input rail, and requires a ceramic capacitor to decouple the input rail. In addition, place a 1µF to 10µF ceramic capacitor between the VIN2 pin and ground. VIN3 can be used to separately from VIN1, but all the VIN pins must start up at the same time. It is recommended to connect all VIN pins using a wide PCB trace if there is no special input requirement.
22	VOUT5	PWR	**LDO5 output.** The VOUT5 pin is powered by V_{IN3}. See the VREF_LDO5 (2Dh) command on page 93 for the LDO5 output voltage (V_{OUT5}) setting. A 4.7µF ceramic capacitor is recommended for the output. If VOUT5 is not used, disable LDO4 via the CHANNEL_EN (18h) command, then float this pin.
23	ADDR	PWR	**I²C address setting.** The MPQ70700FS provides a 7-bit I²C address from 0x00 to 0x7F. The low 2 least significant bit (2LSB) I²C address is determined using different external ADDR resistors connected to ground or VIN1. See the I2C_ADDRESS_PIN bits (51h, bits[1:0]) on page 105 for more details. The high 5LSB I²C address is set via the I2C_ADDRESS_NVM bits (51h, bits[6:2]).
24	ERRIN	I	**Error input.** ERRIN is an open-drain pin. The MPQ70700FS provides an error input function. If the error input signal is configured as a low valid signal and the ERRIN pin voltage (V_{ERRIN}) drops below 0.4V, then the ERRO2 and POR pins are asserted after the ERRIN delay time. If the error input signal is configured as a high valid signal and V_{ERRIN} exceeds 1.3V, then the ERRO2 and POR pins are asserted after the ERRIN delay time. The error signal's active status can be configured low or high via the ERR_MODE (14h) command. The ERRIN delay time is also configured via the ERR_MODE command. If ERRIN is not used, then configure this pin active high, then connect it to ground.
-	Exposed pad	-	**Exposed thermal power pad.** Connect the exposed pad (EP) to the ground plane for optimal heat dissipation. Do not use EP as the primary electrical ground connection.

ABSOLUTE MAXIMUM RATINGS (1)

All pins .....-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2) (7)
TQFN-24 (5mmx5mm)..... 5.48W
Operating junction temperature (T_J).....150°C
Lead temperature.....260°C
Storage temperature.....-65°C to +150°C

ESD Ratings

Human body model (HBM).....Class 2 (4)
Charged-device model (CDM).....Class C2b (5)

Recommended Operating Conditions

Supply voltage (V_{INx}) .....2.8V to 5.5V
Output voltage (V_{LDOx}).....0.5V to 3.6V
Operating junction temp (T_J)……...
……-40°C to +150°C (3)

Thermal Resistance θ_{JA} θ_{JC}

TQFN-24 (5mmx5mm)
JESD51-7.....28.1…3.1…°C/W (6)
EVQ70700FS-UT-00A.....22.8.....…°C/W (7)

Ψ_{JT}

JESD51-7.....0.9…°C/W (6)
EVQ70700FS-UT-00A.....3.…°C/W (7)

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation may generate excessive die temperature, which can cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) T_J is between -40°C to -15°C. V_{INx} is not recommended to exceed 5V from the off state to normal idle state.
4) Per AEC-Q100-002.
5) Per AEC-Q100-011.
6) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The θ_{JC} value shows the thermal resistance from the junction-to-case bottom. The Ψ_{JT} value shows the thermal characterization parameter from junction-to-case.
7) Measured on an MPS standard EVQ70700FS-UT-00A, a 2oz copper, 4-layer PCB (7.6cmx7.6cm). The Ψ_{JT} value shows the thermal characterization parameter from junction-to-case.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage						
LDO1 and internal circuit supply voltage input voltage (V_{IN1}) under-voltage lockout (UVLO) rising threshold	V_{IN1_UVLO}		2.6	2.8	3	V
V_{IN1} UVLO hysteresis	$V_{IN1\_UVLO\_HYS}$			200		mV
Input voltage (V_{INx}) (where x = 1 to 3) over-voltage (OV) rising threshold	$V_{INx\_OV\_R}$		5.55	5.75	5.95	V
V_{INx} OV falling threshold	$V_{INx\_OV\_F}$		5.5	5.7	5.9	V
VIN1/2/3 shutdown current	$I_{Q\_OFF\_WIIC}$	EN1 = 0V, EN2 = 0V, I²C enabled, all LDOs enabled, I_{OUT} = 0A, VMON1/2 disabled			180	µA
	$I_{Q\_OFF\_NIIC}$	EN1 = 0V, EN2 = 0V, I²C disabled, all LDOs enabled, I_{OUT} = 0A, VMON1/2 disabled			150	µA
VIN1/2/3 quiescent current	I_{Q_ON}	EN1 = 2V, EN2 = 2V, all LDOs enabled, I_{OUT} = 0, T_J = 25°C			3	mA
Penta Linear Regulator (LDO1, LDO2, LDO3, LDO4, and LDO5)						
LDOx (where x = 1 to 5) output voltage range (8) (9)	V_{OUTx_RANGE}	MODE0,12.5mV/step	0.5		1.0375	V
		MODE1, 50mV/step	1		3.6	V
LDOx output voltage accuracy (10)	V_{OUTx_ACC}	Relative to the VREF_LDOx bits (where x = 1 to 5) (21h, 24h, 27h, 2Ah, and 2Dh, bits[5:0]), V_{INx} = 5V, V_{OUTx} > 0.75V, I_{OUTx} = 0.1mA - 400mA	-2.5		+2.5	%
		V_{INx} = 5V, V_{OUTx} < 0.75V, I_{OUTx} = 0.1mA - 400mA	-18.75		+18.75	mV
LDOx output current limit	I_{OUTx_LIMIT}	V_{INx} = 5V	420	500	580	mA
LDOx over-current protection (OCP) debounce time range (8) (9)	$t_{LDOx\_OC\_DEB}$		10		80	µs
LDOx OCP debounce time accuracy (8)	$t_{LDOx\_OC\_DEB\_ACC}$	Relative to the LDO_OC_DEBOUNCE bits (3Eh, bits[3:2])	-10		+10	%
LDOx soft-start (SS) rising slew rate voltage range (8) (9)	V_{OUTx_SS}	C_{OUTx} = 4.7µF, from 10% x V_{OUTx} to 90% x V_{OUTx}	0.625		66.6	mV/µs
LDOx SS rising slew rate accuracy (10)	$V_{OUTx\_SS\_ACC}$	Relative to LDOx_SS_SLEW_RATE bits (where x = 1 to 5) (22h, 25h, 28h, 2Bh, and 2Eh, bits[5:3])	-15		+15	%
LDOx dropout voltage	V_{DROP_LDOx}	V_{INx} = 3.2V, V_{OUTx} = 3.3V, I_{OUTx} = 400mA		60	100	mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
LDO1 PSRR performance under 1kHz noise input signal (8) (10)	$PSRR_{1K\_LDO1}$	$V_{IN1/2/3}$ is powered separately and independently, $V_{IN1/2/3}$ = 3.3V, V_{OUT1} = 1.8V, I_{OUT1} = 10mA to 350mA, C_{IN1} = 100nF x2, $C_{IN2/3}$ = 100nF, C_{OUT1} = 4.7µF + 100nF, f_{SW} = 1kHz	40			dB
LDO2 and LDO3 PSRR performance under 1kHz noise input signal (8) (10)	$PSRR_{1K\_LDO2/3}$	$V_{IN1/2/3}$ is powered separately and independently, V_{IN2} = 3.3V, V_{OUTx} = 1.8V, I_{OUTx} = 10mA to 350mA, C_{IN2} = 220nF x3, $C_{IN1/3}$ = 100nF, C_{OUTx} = 4.7µF + 100nF, f_{SW} = 1kHz	60			dB
LDO4 and LDO5 PSRR performance under 1kHz noise input signal (8) (10)	$PSRR_{1K\_LDO4/5}$	$V_{IN1/2/3}$ is powered separately and independently, V_{IN3} = 3.3V, V_{OUTx} = 1.8V, I_{OUTx} = 10mA to 350mA, C_{IN3} = 220nF x3, $C_{IN1/2}$ = 100nF, C_{OUTx} = 4.7µF + 100nF, f_{SW} = 1kHz	60			dB
Line regulation (11)		Relative to the VREF_LDOx bits, V_{IN} = 2.8V to 5V, I_{OUT} = 10mA	-1		+1	%/V
Output discharge resistance	$R_{DISCHARGE}$	LDOx output discharge function is enabled		120		Ω
LDO over-voltage protection (OVP) and under-voltage protection (UVP) debounce time range (8) (9)	t_{LDO_OVP/UVP_DEB}		10		80	µs
LDO OVP and UVP debounce time accuracy (8)	t_{LDO_OV/UV_DEB_ACC}	Relative to the LDOx_DEBOUNCE bits (where x = 1 to 5) (3Eh, 41h, 44h, 47h, and 4Ah, bits[1:0])	-10		+10	%
Dual General-Purpose Input/Output (GPIO1 and GPIO3)						
GPIO1/3 input high	$V_{IH\_GPIO1/3}$		1.35			V
GPIO1/3 input low	$V_{IL\_GPIO1/3}$				0.4	V
GPIO1/3 output low	$V_{OL\_GPIO1/3}$				0.1	V
GPIO1/3 leakage current	$I_{GPIO1/3\_LKG}$	$V_{GPIO1/3}$ = 5V			150	nA
Dual General-Purpose Output (GPIO2 and GPIO4)						
GPIO2/4 output low	$V_{OL\_GPIO2/4}$				0.1	V
GPIO2/4 leakage current	$I_{GPIO2/4\_LKG}$	$V_{GPIO2/4}$ = 5V			150	nA
Two Voltage Monitors (Differential VMON1 and Independent VMON2)						
VMONx (where x = 1 or 2) OV rising threshold range (8) (9)	V_{MONx_OV}		0.45		3.6375	V
VMONx UV falling threshold range (8) (9)	V_{MONx_UV}		0.45		3.6375	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VMONx OVP and UVP threshold accuracy (10)	V_{MONx_ACC}	Relative to the MONx_OV_VTH (where x = 1 to 2) (36h and 39h) and MONx_UV_VTH (where x = 1 to 2) (37h and 3Ah) commands, $V_{MONx\_OV/UV}$ > 1V	-5		+5	%
		$V_{MONx\_OV/UV}$ < 1V	-50		+50	mV
VMONx OVP and UVP debounce time range (8) (9)	$t_{VMONx\_OVUV\_DEB}$		10		80	µs
VMONx OVP and UVP debounce time accuracy (8)		Relative to the MONx_DEBOUNCE bits (where x = 1 to 2) (38h and 3Bh bits[1:0]) and MONx_MODE commands (where x = 1 to 2) (38h and 3Bh)	-10		+10	%
VMON2, VMON1-, and VMON1+ pin impedance	R_{VMON}	V_{MON} = 5V	1			MΩ
Time Slot						
Sequence time slot range (8) (9)	t_{SLOT_RANGE}		100		6475	µs
Sequence time slot accuracy (8)	t_{SLOT_ACC}	Relative to the TIME_SLOT (1Ch) command	-10		+10	%
Thermal Protection						
Thermal warning	T_{TW}		110	130	150	°C
Thermal warning hysteresis	T_{TW_HYS}			15		°C
Thermal shutdown	T_{TSD}		152	172	192	°C
Thermal shutdown hysteresis	T_{TSD_HYS}			15		°C
Low-Dropout (LDO) Output Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP)						
LDOx output OV rising threshold range (8) (9)	$V_{OUTx\_OV\_RISING}$		0.45		3.6375	V
LDOx output OV rising threshold accuracy (10)	$V_{OUxT\_OV\_ACC}$	Relative to the LDOx_OV_VTH commands (where x = 1 to 5) (3Ch, 3Fh, 42h, 45h, and 48h), $V_{OUTx\_OV\_RISING}$ > 1V	-5		+5	%
		$V_{OUTx\_OV\_RISING}$ < 1V	-50		+50	mV
LDOx output OV hysteresis	$V_{OUTx\_OV\_HYS}$				40	mV
LDOx output UV falling threshold range (8) (9)	$V_{OUTx\_UV\_FALLING}$		0.45		3.6375	V
LDOx output UV falling threshold accuracy (10)	$V_{OUTx\_UV\_ACC}$	Relative to the LDOx_UV_VTH commands (where x = 1 to 5) (3Dh, 40h, 43h, 46h, and 49h), $V_{OUTx\_UV\_FALLING}$ > 1V	-5		+5	%
		$V_{OUTx\_UV\_FALLING}$ < 1V	-50		+50	mV
LDOx output UV hysteresis	$V_{OUTx\_UV\_HYS}$				40	mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
LDOx OVP and UVP debounce time range (8) (9)	t_{LDOx_OV/UV_DEB}		10		80	µs
LDOx OVP and UVP debounce time accuracy (8)		Relative to the LDOx_DEBOUNCE bits	-10		+10	%
Fail-Recovery Delay Time						
Fail-recovery delay time (8) (9)	$t_{FAIL\_REC\_DLY}$	Transition from fail-recovery state entry to the next state	0.128		8.192	ms
Fail-recovery delay time accuracy (8)		Relative to the DLY_RCOV bits (1Ah, bits[5:0])	-10		+10	%
Enable (EN)						
EN rising threshold	$V_{IH\_EN\_R}$	Level-sensitive input	1.13	1.23	1.33	V
EN falling threshold	$V_{IL\_EN\_F}$	Level-sensitive input	0.4	0.44	0.48	V
EN threshold hysteresis				790		mV
EN input current	I_{EN}	V_{EN} = 2V			200	nA
Built-In Self-Testing (BIST)						
Power-on reset (POR) to ready with built-in self-testing (BIST)	t_{CFG_WB}	Includes pre-loaded one-time programmable (OTP) memory with error correction code (ECC), BIST, reload OTP with ECC			20	ms
POR to ready without BIST (8)	t_{CFG_NB}	Includes pre-loaded OTP with ECC			5	ms
BIST time (8)		AT_POR (19h, bits[1:0]) = 1 or AT_SHDN (19h, bit[4]) = 1			15	ms
Power-On Reset (POR)						
POR delay time range (8) (9)	$t_{POR\_DLY\_RANGE}$		0.128		32.768	ms
POR delay time accuracy (8)	$t_{POR\_DLY\_ACC}$	Relative to the POR_CTL_DLY (35h) command	-10		+10	%
POR rising threshold range (8) (9)	$V_{OUTx\_POR\_R}$		0.45		3.6375	V
POR rising threshold accuracy (10)	$V_{OUTx\_POR\_ACC}$	Relative to PORx_CTL_CTH commands (where x = 1 to 5) (30h to 34h), $V_{OUTx\_POR\_R}$ > 1V	-5		+5	%
		$V_{OUTx\_POR\_R}$ < 1V	-50		+50	mV
POR threshold hysteresis	$V_{OUTx\_POR\_HYS}$				40	mV
POR output low	V_{OL_POR}				0.1	V
POR pin leakage current	I_{POR_LKG}	V_{POR} = 5V			150	nA
Dual Error Output (ERRO1 and ERRO2)						
Error output low	V_{OL_ERRO}	With 10kΩ external pull-up resistor to 3.3V			0.1	V
Error output delay time range (8) (9)	t_{ERRO_DLY}	Transition from fault detection to pulling ERRO1/2 low	0		10	ms
Error output delay time accuracy (8)	$t_{ERRO\_DLY\_ACC}$	Relative to the ERRO_DLY bits (14h, bits[1:0])	-10		+10	%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
ERRO1 pin leakage current	I_{ERRO1_LKG}	V_{ERRO1} = 5V			150	nA
Error Input						
Error input high	V_{IH_ERRIN}		1.35			V
Error input low	V_{IL_ERRIN}				0.4	V
Error input delay time range (8) (9)	t_{ERRIN_DLY}	Transition from pulling the ERRIN pin low to the MPQ70700FS detecting an error input fault	0		10	ms
Error input delay time accuracy (8)	$t_{ERRIN\_DLY\_ACC}$	Relative to the ERRIN_DLY bits (14h, bits[3:2])	-10		+10	%
ERRIN pin leakage current	I_{ERRIN}	V_{ERRIN} = 5V			150	nA
System Clock						
System clock frequency	f_{CLK}		2.25	2.5	2.75	MHz
System clock monitor threshold		System primary clock is normal	118	124	130	% of f_{CLK}
			75	81	87	
Watchdog						
Watchdog open window range (8) (9)	t_{WD_OPEN}	The WDT_OPEN (4Dh) command value ranges between 0x00 and 0x1F, 1ms/step	1		32	ms
		The WDT_OPEN command value ranges between 0x20 and 0x3F, 2ms/step	34		96	ms
		The WDT_OPEN command value ranges between 0x40 and 0xFF, 4ms/step	98		864	ms
Watchdog open window accuracy (8)	$t_{WD\_OPEN\_ACC}$	Relative to the WDT_OPEN command	-10		+10	%
Watchdog closed window range (8) (9)	t_{WD_CLS}	The WDT_CLOSE (4Ch) command value ranges between 0x00 and 0x1F, 1ms/step	1		32	ms
		The WDT_CLOSE command value ranges between 0x20 and 0x3F, 2ms/step	34		96	ms
		The WDT_CLOSE command value ranges between 0x40 and 0xFF, 4ms/step	98		864	ms
Watchdog closed window accuracy (8)	$t_{WD\_CLS\_ACC}$	Relative to the WDT_CLOSE command	-10		+10	%
I²C Logic Interface (8)						
SCL/SDA input logic low	V_{IL}				0.4	V
SCL/SDA input logic high	V_{IH}		1.35			V
SCL/SDA output logic low	V_{OL}	With 10kΩ external pull-up resistor			0.4	V
SCL clock frequency	f_{SCL}				1000	kHz
SCL high time	t_{HIGH}		0.26			µs
SCL low time	t_{LOW}		0.5			µs
Data set-up time	t_{SU_DAT}		50			ns

ELECTRICAL CHARACTERISTICS *(continued)*

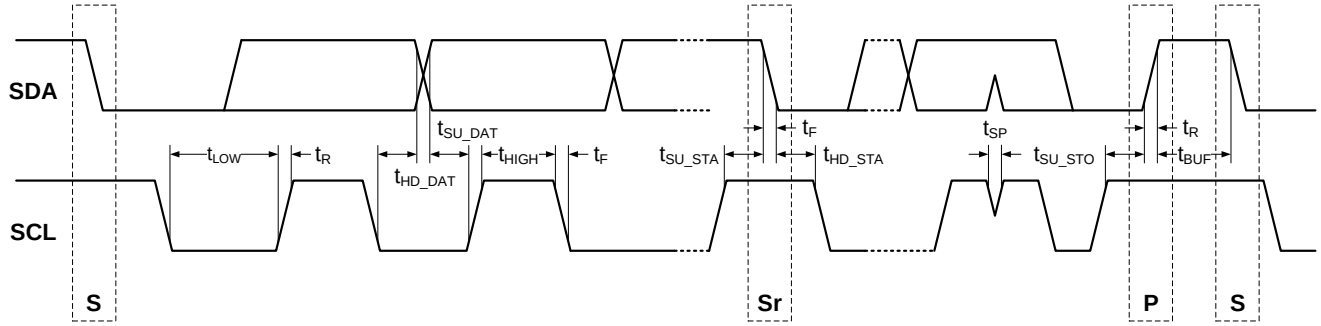
V_{IN} = 5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Data hold time	t_{HD_DAT}		0			µs
Set-up time for repeated start command	t_{SU_STA}		0.26			µs
Hold time for start command	t_{HD_STA}		0.26			µs
Bus free time between a start and stop command	t_{BUF}		0.5			µs
Set-up time for stop command	t_{SU_STO}		0.26			µs
Rising time of SCL/SDA	t_R				120	ns
Falling time of SCL/SDA	t_F	V_{DD} supplies the I^2C	20 x (V_{DD} / 5.5V)		120	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				550	pF

Notes:

8) Derived from bench characterization. Not tested in production.
9) Configurable via the I^2C interface.
10) Not tested across the entire optional range. MPS only guarantees accuracy at a factory-trimmed level according to custom unique code.
11) Line regulation = $\frac{\left|V_{OUTx}[V_{INx\_MAX}] - V_{OUTx}[V_{INx\_MIN}]\right|}{[V_{INx\_MAX} - V_{INx\_MIN}] \times V_{OUTx\_NOM}}$ x (%/V), where V_{OUTx} is the LDO output voltage that is tested at V_{IN} = 5V. If V_{OUTx} exceeds 2.8V, the minimum input voltage (V_{INx_MIN}) uses 5V instead of 2.8V to calculate line regulation.

TIMING DIAGRAM



S: Start Command

Sr: Repeated Start Command

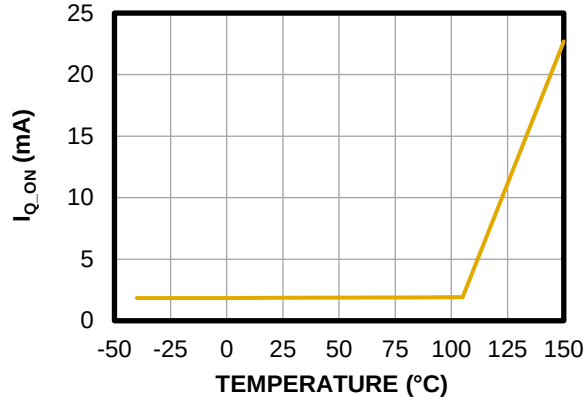
P: Stop Command

Figure 1: I²C-Compatible Interface Timing Diagram

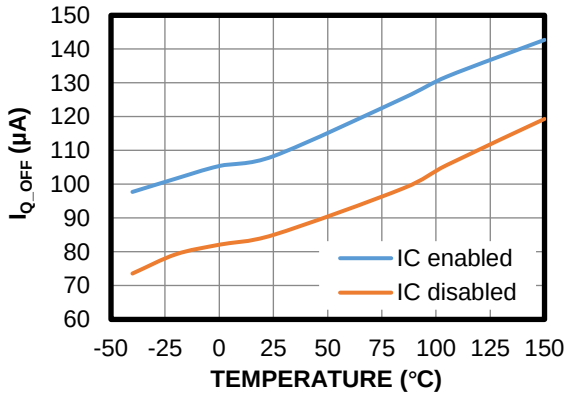
TYPICAL CHARACTERISTICS

V_{IN} = 5V, T_A = -40°C to +150°C, unless otherwise noted.

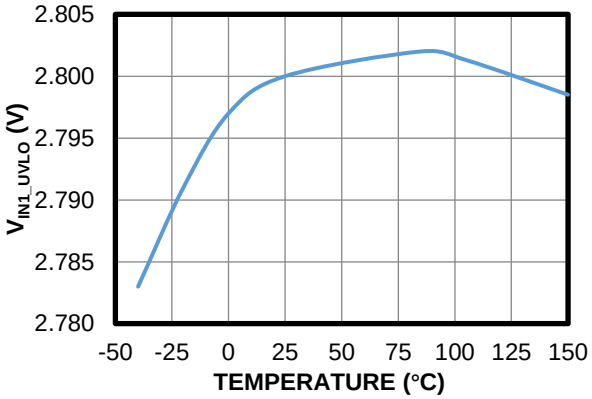
VINx Quiescent Current vs. Temperature



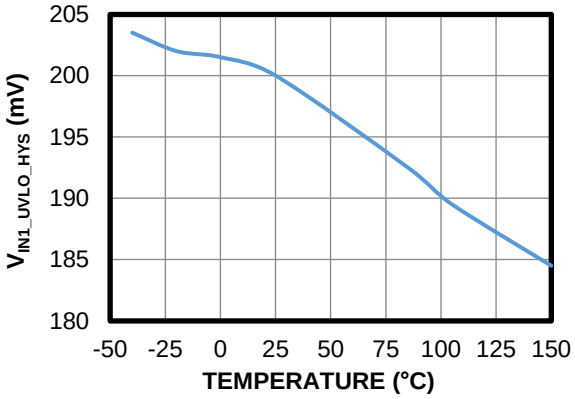
VINx Shutdown Current vs. Temperature



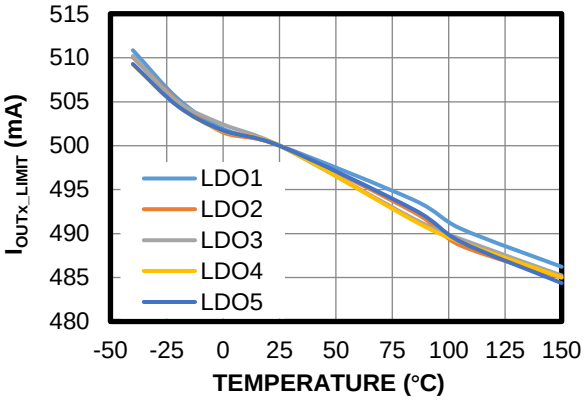
V_{IN1} UVLO Rising Threshold vs. Temperature



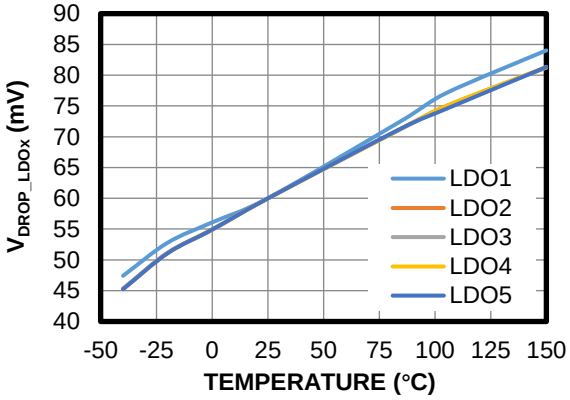
V_{IN1} UVLO Hysteresis vs. Temperature



LDOx Output Current Limit vs. Temperature



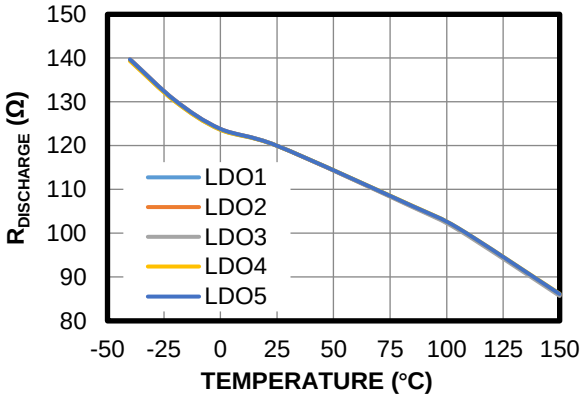
LDOx Dropout Voltage vs. Temperature



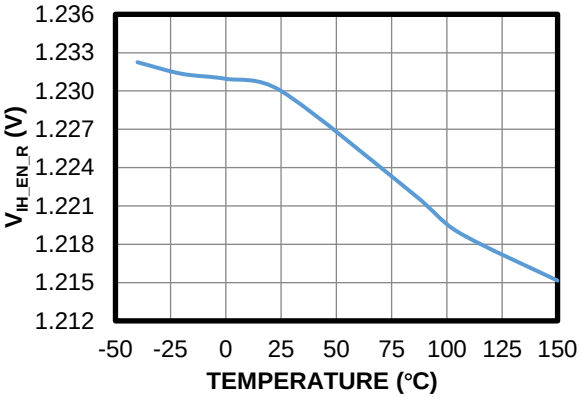
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = -40°C to +150°C, unless otherwise noted.

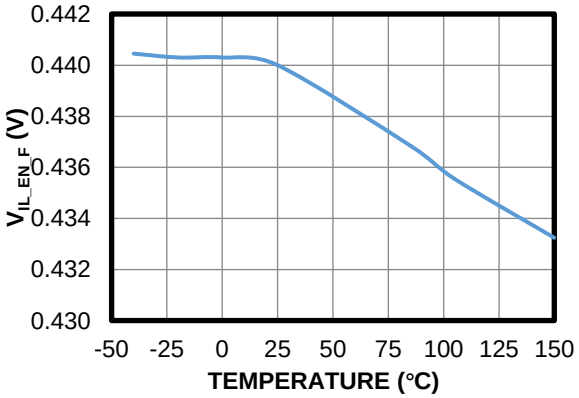
Output Discharge Resistance vs. Temperature



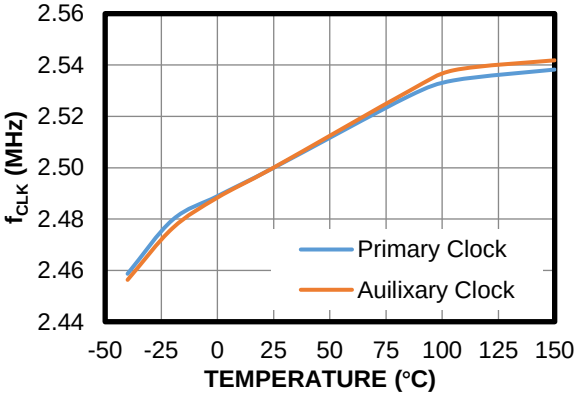
EN Rising Threshold vs. Temperature



EN Falling Threshold vs. Temperature



System Clock Frequency vs. Temperature

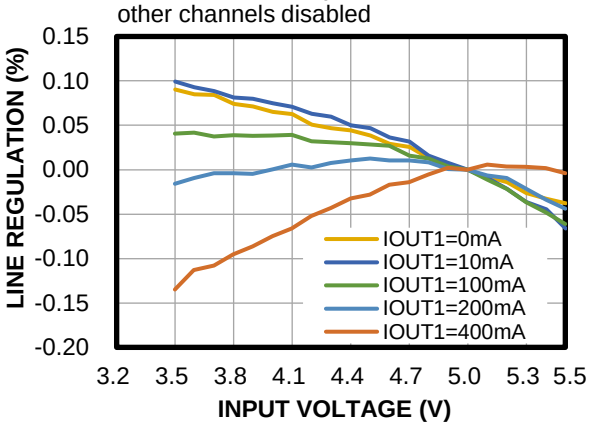


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

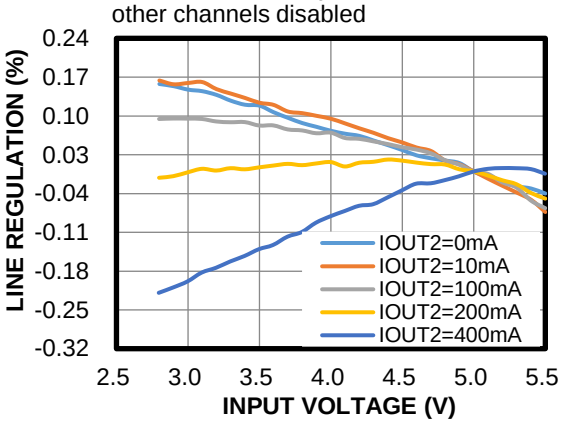
Line Regulation (LDO1)

V_{OUT1} = 3.3V, C_{OUT1} = 4.7µF,
C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF,
other channels disabled



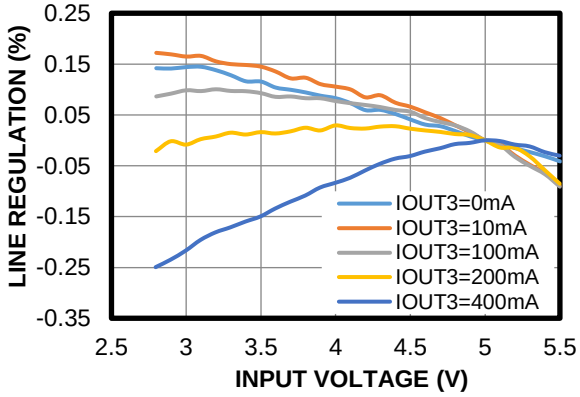
Line Regulation (LDO2)

V_{OUT2} = 0.75V, C_{OUT1} = 4.7µF,
C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF,
other channels disabled



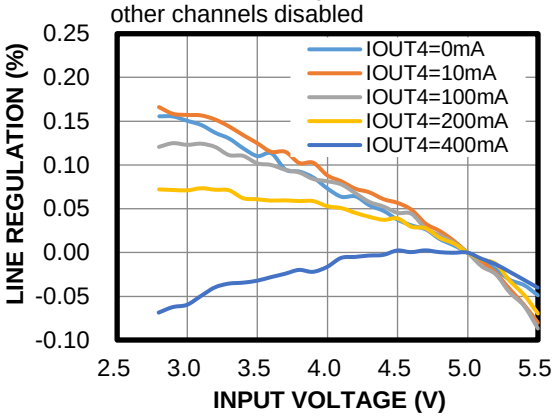
Line Regulation (LDO3)

V_{OUT3} = 1.8V, C_{OUT3} = 4.7µF,
C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF,
other channels disabled



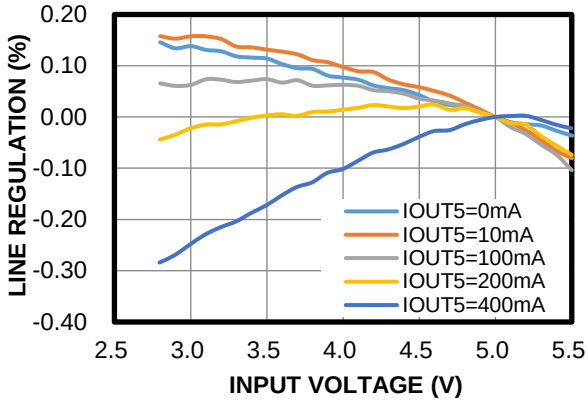
Line Regulation (LDO4)

V_{OUT4} = 0.75V, C_{OUT4} = 4.7µF,
C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF,
other channels disabled



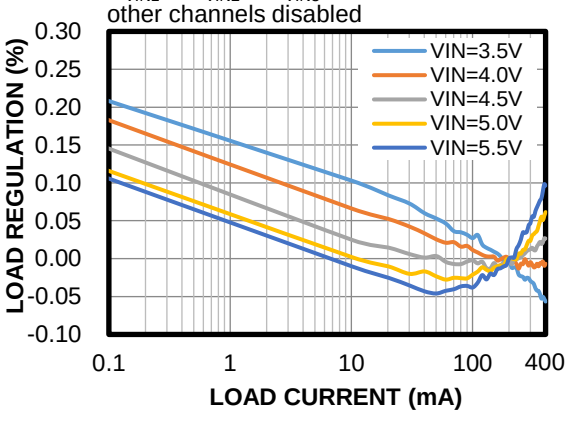
Line Regulation (LDO5)

V_{OUT5} = 0.75V, C_{OUT5} = 4.7µF,
C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF,
other channels disabled



Load Regulation (LDO1)

V_{OUT1} = 3.3V, C_{OUT1} = 4.7µF,
C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF,
other channels disabled

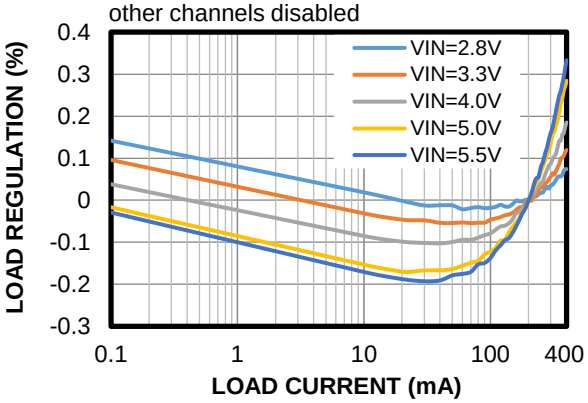


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

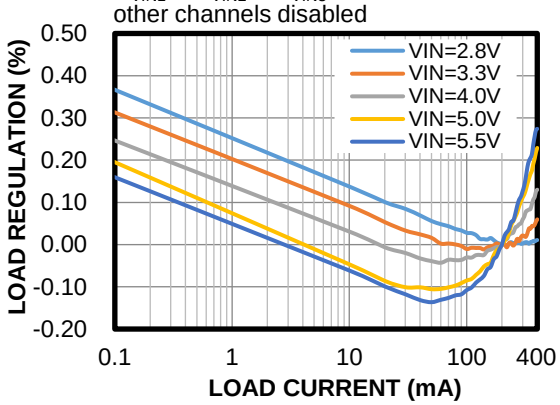
Load Regulation (LDO2)

V_{OUT2} = 0.75V, C_{OUT2} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



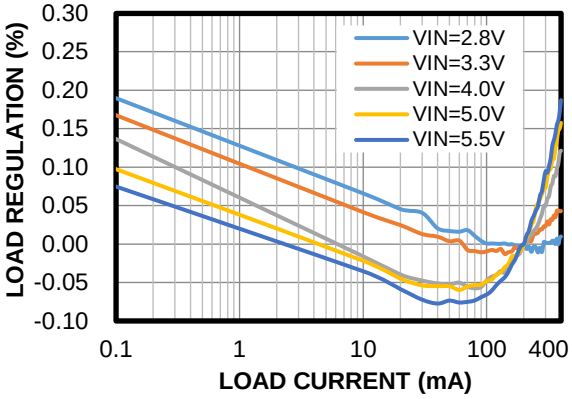
Load Regulation (LDO3)

V_{OUT3} = 1.8V, C_{OUT3} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



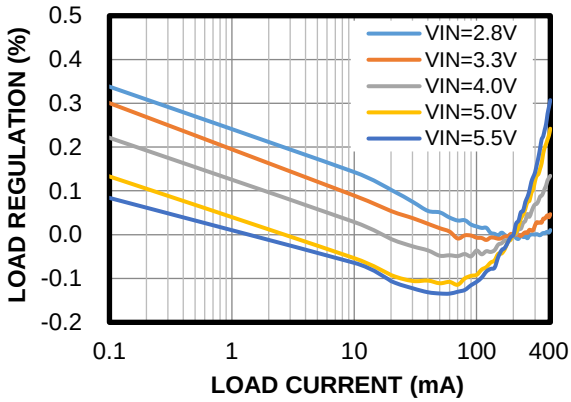
Load Regulation (LDO4)

V_{OUT4} = 0.75V, C_{OUT4} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



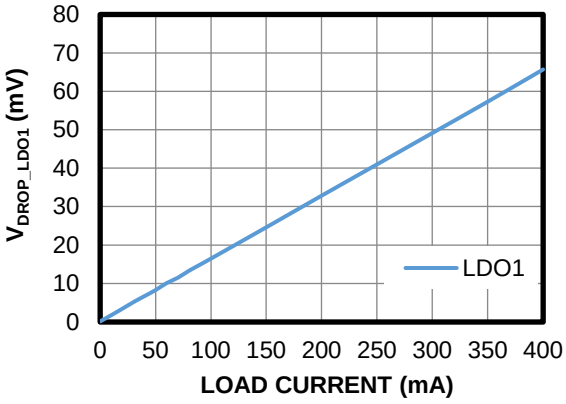
Load Regulation (LDO5)

V_{OUT5} = 1.8V, C_{OUT5} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



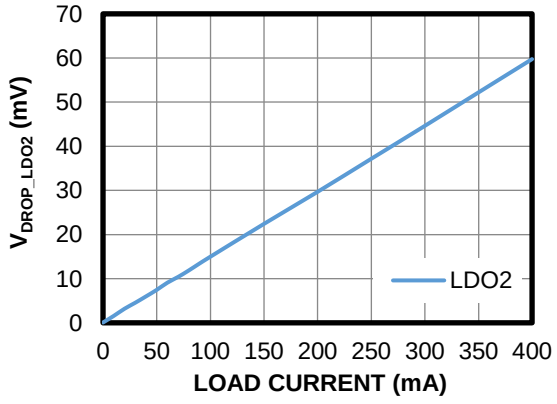
Load Dropout Voltage (LDO1)

V_{INx} = 3.2V, V_{OUT1} = 3.3V, C_{OUT1} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



Load Dropout Voltage (LDO2)

V_{INx} = 3.2V, V_{OUT2} = 3.3V, C_{OUT2} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled

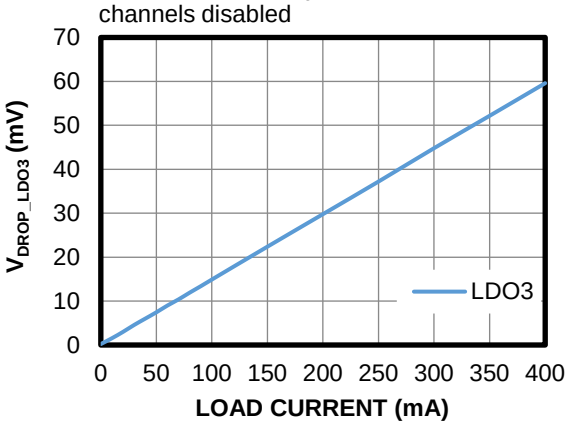


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

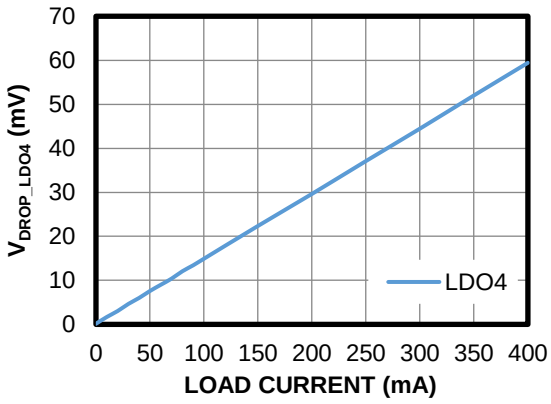
Load Dropout Voltage (LDO3)

V_{INx} = 3.2V, V_{OUT3} = 3.3V, C_{OUT3} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



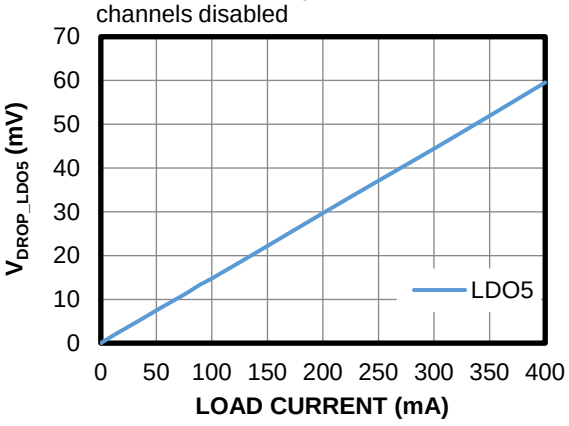
Load Dropout Voltage (LDO4)

V_{INx} = 3.2V, V_{OUT4} = 3.3V, C_{OUT4} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



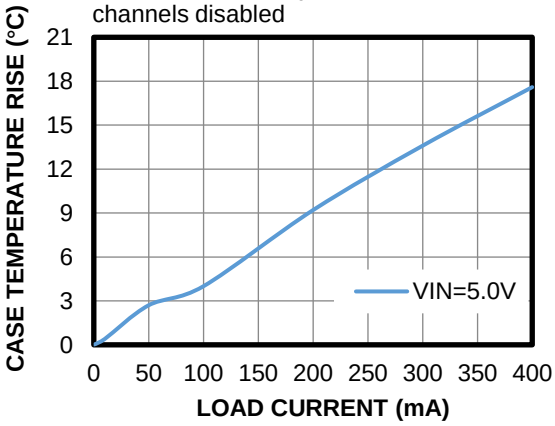
Load Dropout Voltage (LDO5)

V_{INx} = 3.2V, V_{OUT5} = 3.3V, C_{OUT5} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



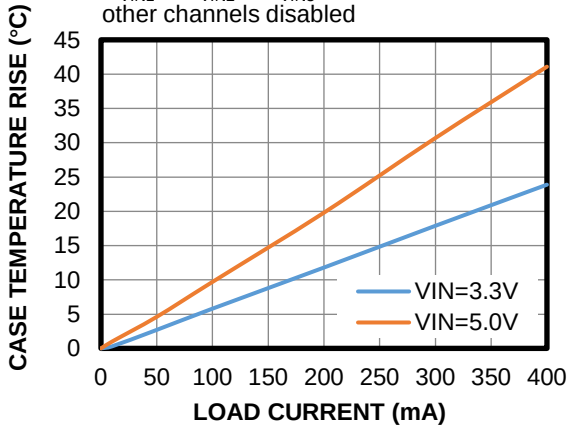
Case Temperature Rise (LDO1)

V_{INx} = 5V, V_{OUT1} = 3.3V, C_{OUT1} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



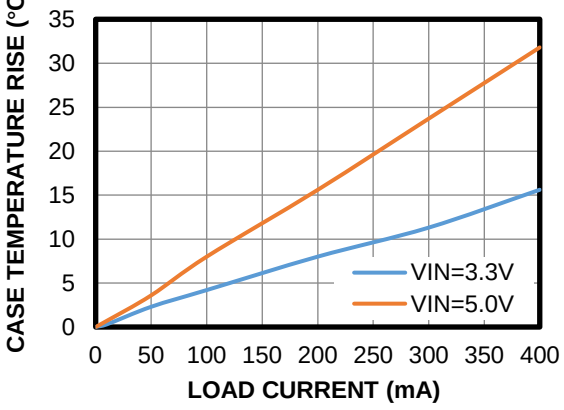
Case Temperature Rise (LDO2)

V_{OUT2} = 0.75V, C_{OUT2} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled



Case Temperature Rise (LDO3)

V_{OUT3} = 0.75V, C_{OUT3} = 4.7µF, C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF, other channels disabled

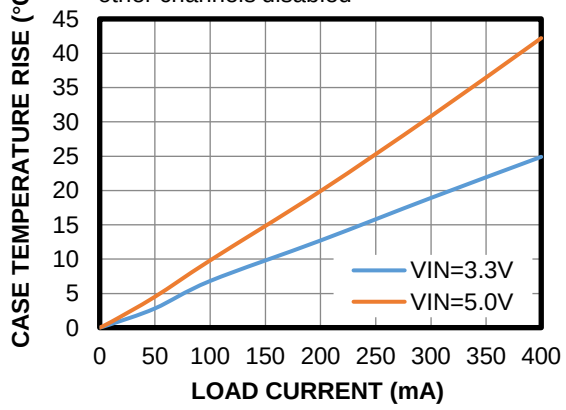


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

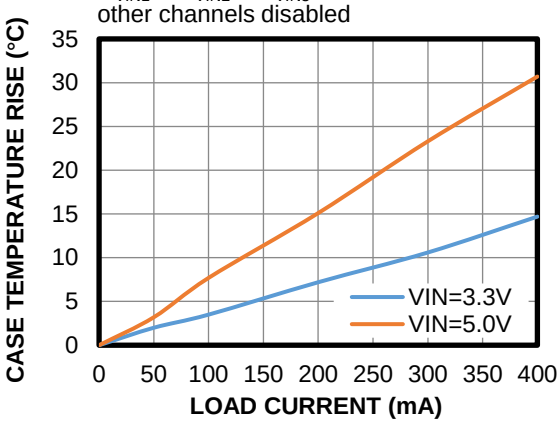
Case Temperature Rise (LDO4)

V_{OUT4} = 0.75V, C_{OUT4} = 4.7µF,
C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF,
other channels disabled



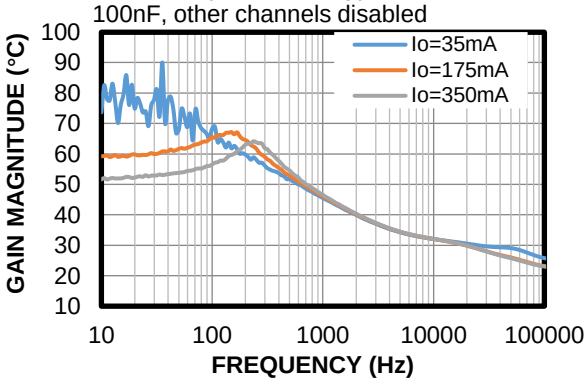
Case Temperature Rise (LDO5)

V_{OUT5} = 1.8V, C_{OUT5} = 4.7µF,
C_{VIN1} = C_{VIN2} = C_{VIN3} = 4.7µF,
other channels disabled



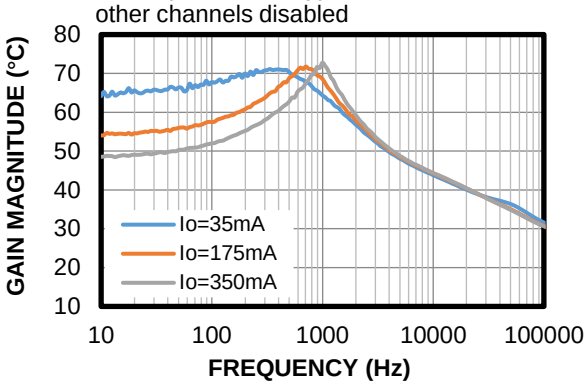
LDO1 PSRR

$V_{IN1/3}$ = 3.3V + Sine ripple, V_{IN2} = 3.3V,
V_{OUT1} = 1.8V, C_{IN1} = 100nF x2, C_{IN2} =
100nF, C_{IN3} = 100nF, C_{OUT1} = 4.7µF +
100nF, other channels disabled



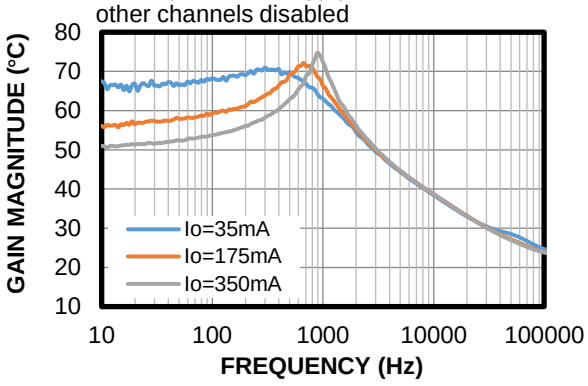
LDO2 PSRR

$V_{IN1/3}$ = 3.3V, V_{IN2} = 3.3V + Sine ripple,
V_{OUT2} = 1.8V, C_{IN1} = 100nF, C_{IN2} = 220nF
x3, C_{IN3} = 100nF, C_{OUT2} = 4.7µF + 100nF,
other channels disabled



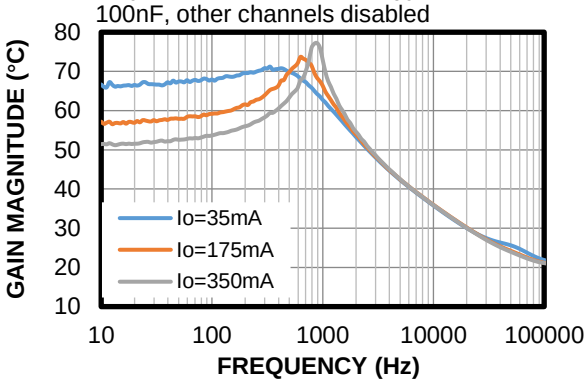
LDO3 PSRR

$V_{IN1/3}$ = 3.3V, V_{IN2} = 3.3V + Sine ripple,
V_{OUT3} = 1.8V, C_{IN1} = 100nF, C_{IN2} = 220nF
x3, C_{IN3} = 100nF, C_{OUT3} = 4.7µF + 100nF,
other channels disabled



LDO4 PSRR

$V_{IN1/2}$ = 3.3V, V_{IN3} = 3.3V + Sine ripple,
V_{OUT4} = 1.8V, C_{IN1} = 100nF, C_{IN2} = 100nF,
C_{IN3} = 100nF x2 + 220nF, C_{OUT4} = 4.7µF +
100nF, other channels disabled

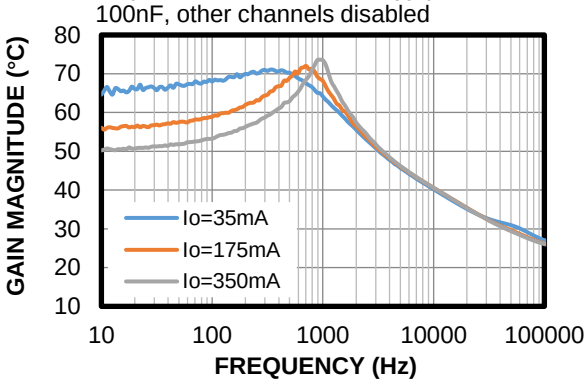


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

LDO5 PSRR

$V_{IN1/2}$ = 3.3V, V_{IN3} = 3.3V + Sine ripple, V_{OUT5} = 1.8V, C_{IN1} = 100nF, C_{IN2} = 100nF, C_{IN3} = 100nF x2 + 220nF, C_{OUT5} = 4.7µF + 100nF, other channels disabled

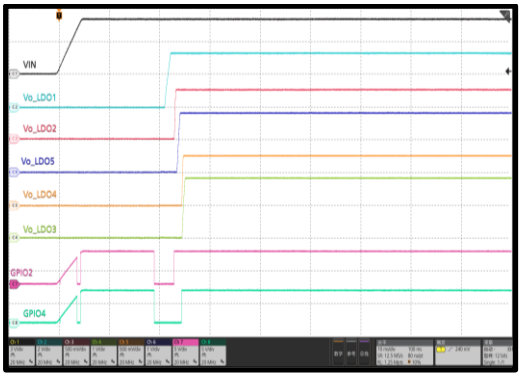


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

Start-Up through VIN

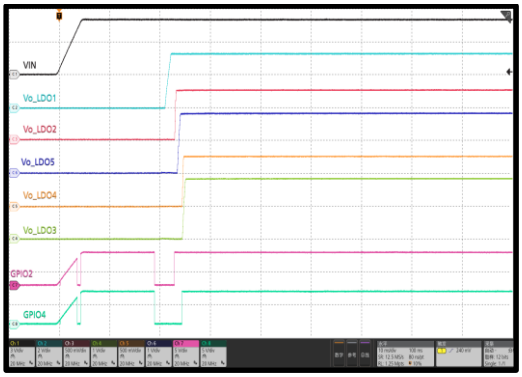
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A



10ms/div.

Start-Up through VIN

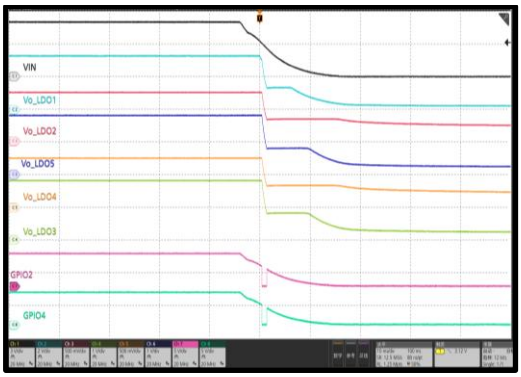
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A



10ms/div.

Shutdown through VIN

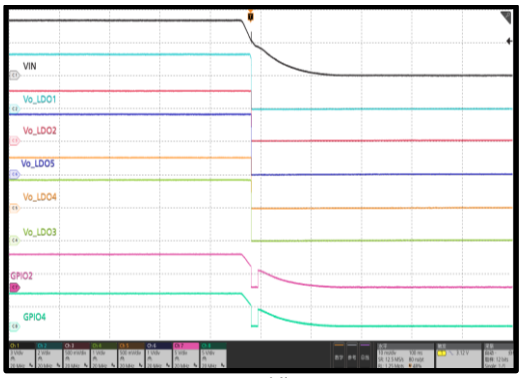
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A



10ms/div.

Shutdown through VIN

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

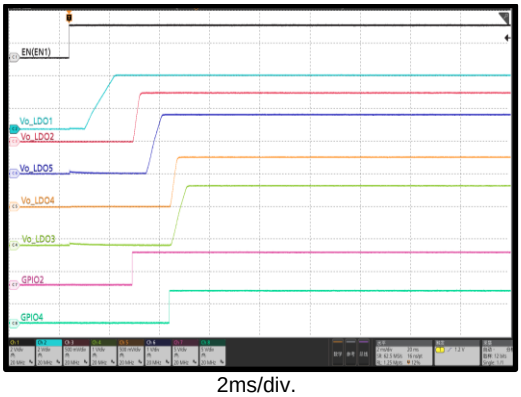


10ms/div.

Start-Up through EN (EN1)

V_{GPIO1_EN2} = 5V,

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

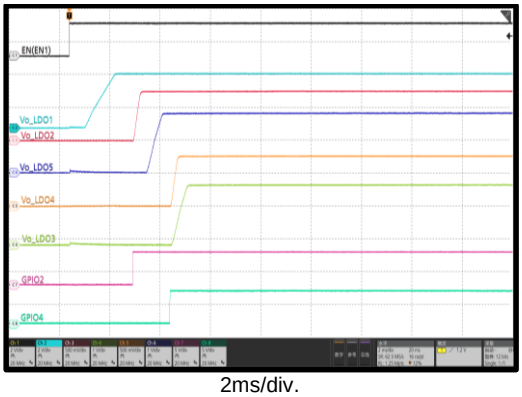


2ms/div.

Start-Up through EN (EN1)

V_{GPIO1_EN2} = 5V,

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A



2ms/div.

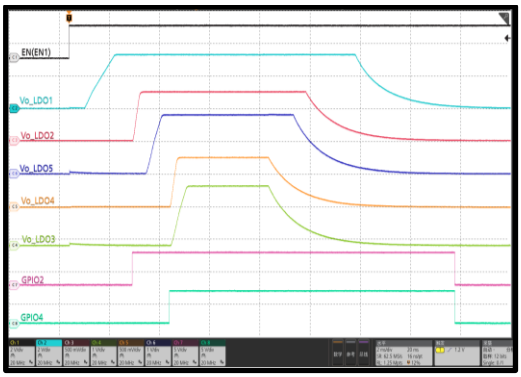
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

Start-Up through EN (EN1)

V_{GPIO1_EN2} = 0V,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

CH1: V_{EN_EN1} 2V/div.
CH2: V_{OUT_LDO1} 2V/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH6: V_{OUT_LDO5} 1V/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.

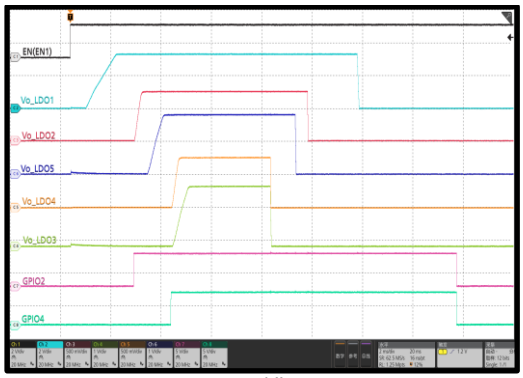


2ms/div.

Start-Up through EN (EN1)

V_{GPIO1_EN2} = 0V,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

CH1: V_{EN_EN1} 2V/div.
CH2: V_{OUT_LDO1} 2V/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH6: V_{OUT_LDO5} 1V/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.

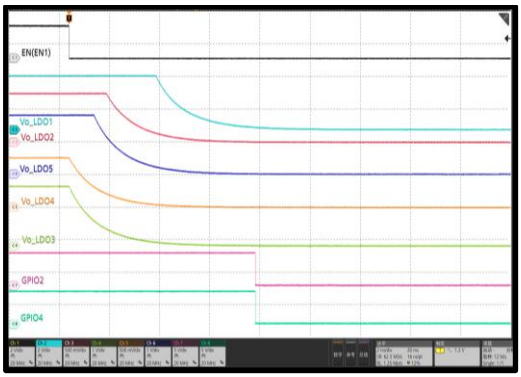


2ms/div.

Shutdown through EN (EN1)

V_{GPIO1_EN2} = 5V,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

CH1: V_{EN_EN1} 2V/div.
CH2: V_{OUT_LDO1} 2V/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH6: V_{OUT_LDO5} 1V/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.

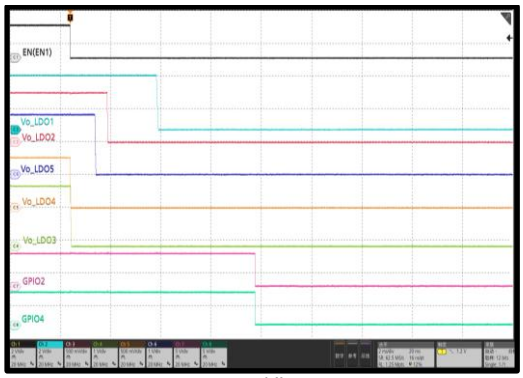


2ms/div.

Shutdown through EN (EN1)

V_{GPIO1_EN2} = 5V,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

CH1: V_{EN_EN1} 2V/div.
CH2: V_{OUT_LDO1} 2V/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH6: V_{OUT_LDO5} 1V/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.

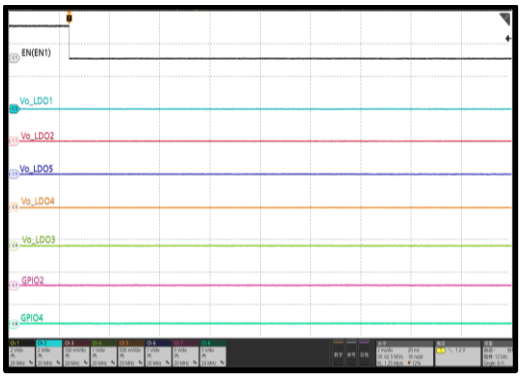


2ms/div.

Shutdown through EN (EN1)

V_{GPIO1_EN2} = 0V,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

CH1: V_{EN_EN1} 2V/div.
CH2: V_{OUT_LDO1} 2V/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH6: V_{OUT_LDO5} 1V/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.



2ms/div.

Shutdown through EN (EN1)

V_{GPIO1_EN2} = 0V,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

CH1: V_{EN_EN1} 2V/div.
CH2: V_{OUT_LDO1} 2V/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH6: V_{OUT_LDO5} 1V/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH4: V_{O_LDO3} 1V/div.
CH7: GPIO2 5V/div.
CH8: GPIO4 5V/div.

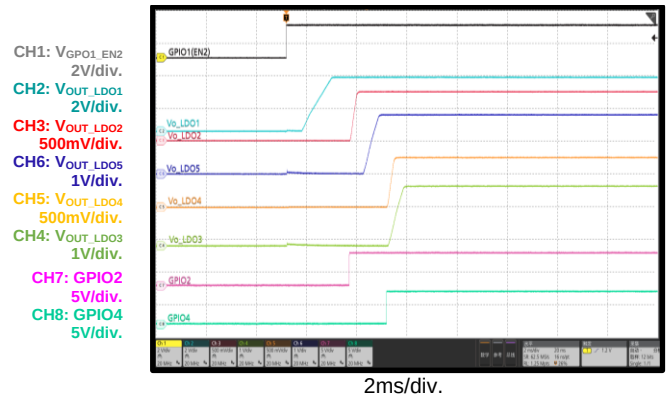
2ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

Start-Up through GPIO1 (EN2)

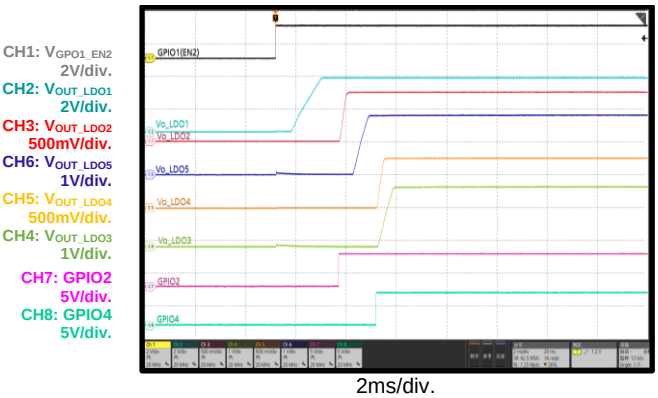
V_{EN_EN1} = 5V,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A



2ms/div.

Start-Up through GPIO1 (EN2)

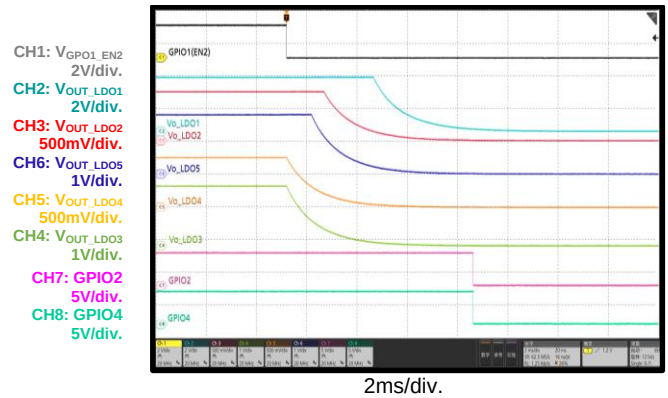
V_{EN_EN1} = 5V,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A



2ms/div.

Shutdown through GPIO1 (EN2)

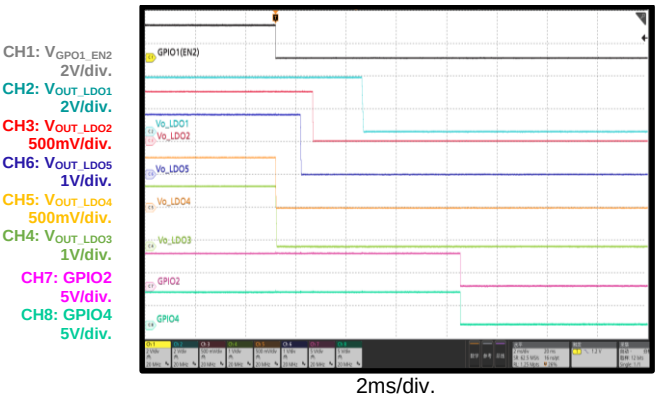
V_{EN_EN1} = 5V,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A



2ms/div.

Shutdown through GPIO1 (EN2)

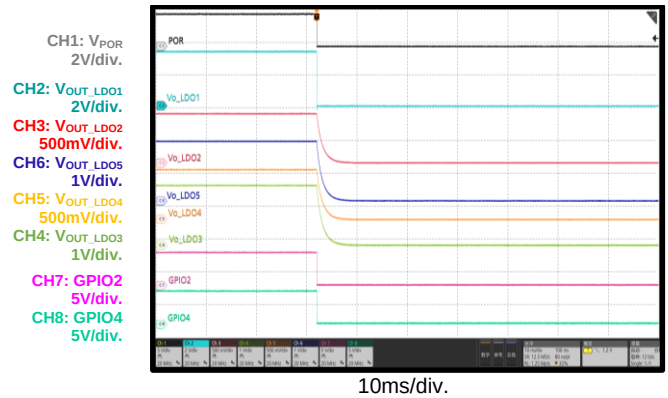
V_{EN_EN1} = 5V,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A



2ms/div.

SCP Entry (LDO1)

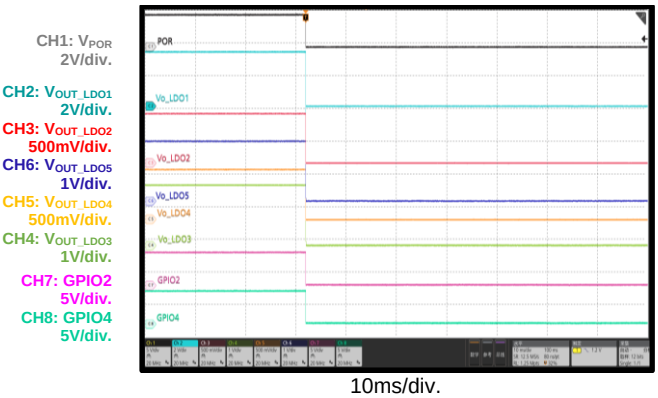
Configure the MPQ70700FS to enter failsafe mode after LDO1 SCP entry,
I_{OUT1} = 0A to short circuit, other I_{OUT} = 0A



10ms/div.

SCP Entry (LDO1)

Configure the MPQ70700FS to enter failsafe mode after LDO1 SCP entry,
I_{OUT1} = 0.4A to short circuit, other I_{OUT} = 0.4A



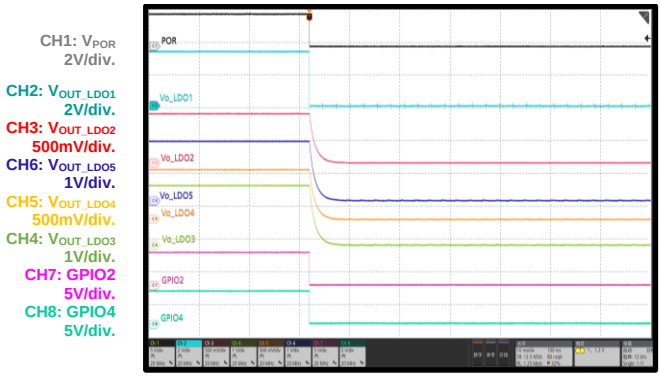
10ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

SCP Entry (LDO1)

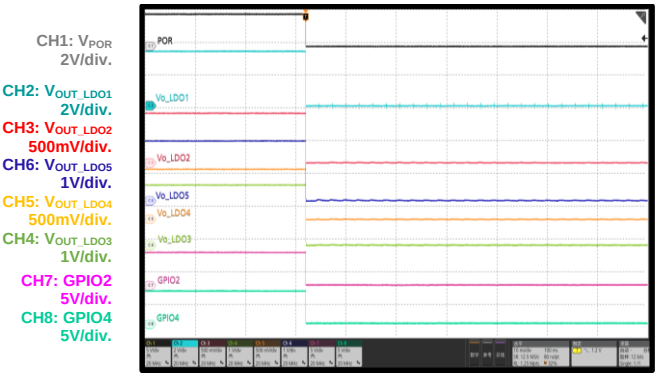
Configure the MPQ70700FS to enter fail-recovery mode after LDO1 SCP entry, I_{OUT1} = 0A to short circuit, other I_{OUT} = 0A



10ms/div.

SCP Entry (LDO1)

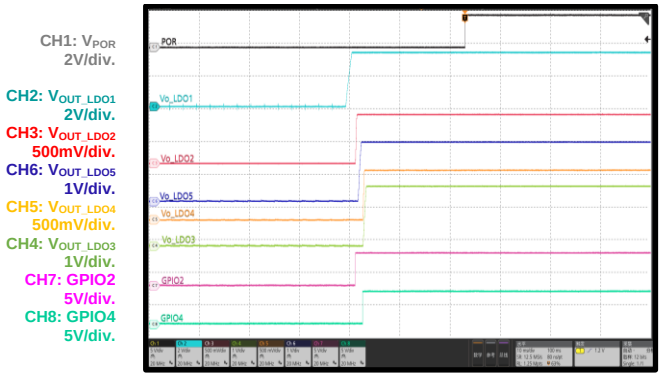
Configure the MPQ70700FS to enter fail-recovery mode after LDO1 SCP entry, I_{OUT1} = 0.4A to short circuit, other I_{OUT} = 0.4A



10ms/div.

SCP Recovery (LDO1)

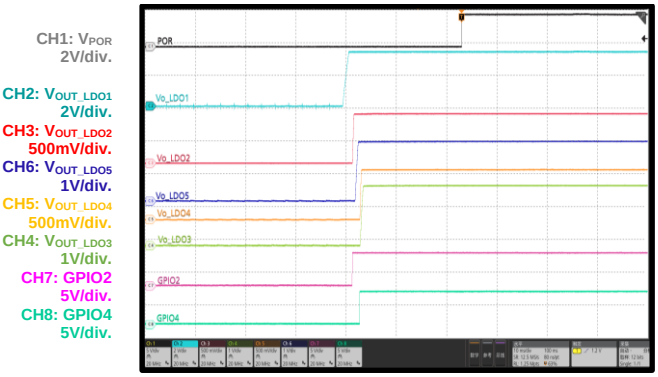
Configure the MPQ70700FS to enter fail-recovery mode after LDO1 SCP entry, I_{OUT1} = short circuit to 0A, other I_{OUT} = 0A



10ms/div.

SCP Recovery (LDO1)

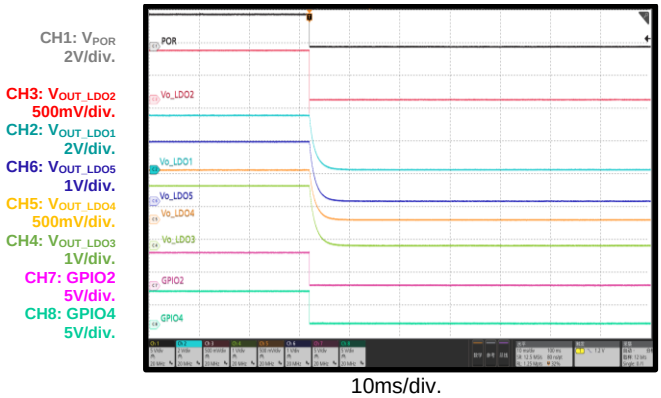
Configure the MPQ70700FS to enter fail-recovery mode after LDO1 SCP entry, I_{OUT1} = short circuit to 0.4A, other I_{OUT} = 0.4A



10ms/div.

SCP Entry (LDO2)

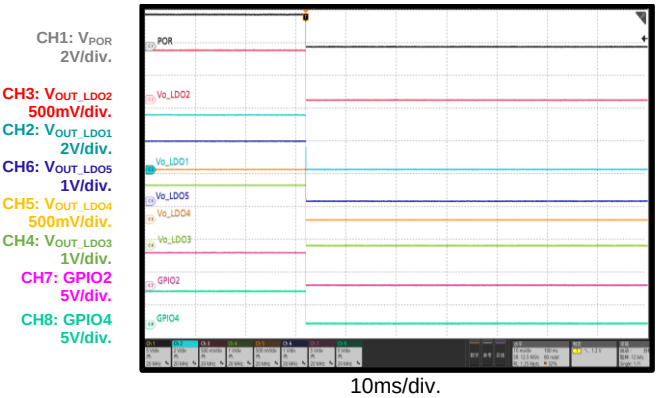
Configure the MPQ70700FS to enter failsafe mode after LDO2 SCP entry, I_{OUT2} = 0A to short circuit, other I_{OUT} = 0A



10ms/div.

SCP Entry (LDO2)

Configure the MPQ70700FS to enter failsafe mode after LDO2 SCP entry, I_{OUT2} = 0.4A to short circuit, other I_{OUT} = 0.4A



10ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

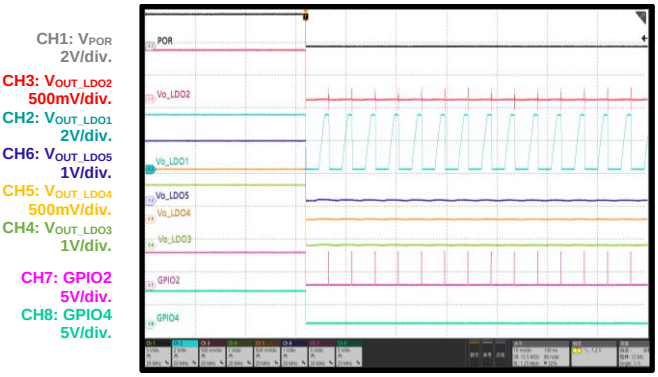
V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

SCP Entry (LDO2)

Configure the MPQ70700FS to enter fail-recovery mode after LDO2 SCP entry, I_{OUT2} = 0A to short circuit, other I_{OUT} = 0A

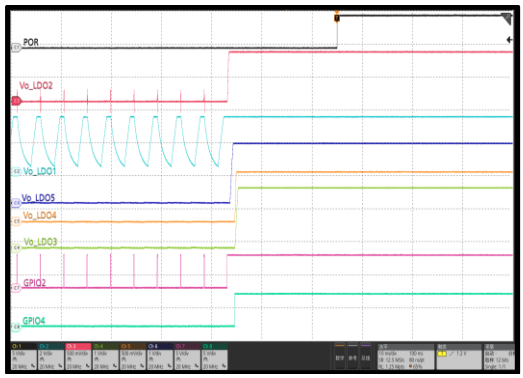
SCP Entry (LDO2)

Configure the MPQ70700FS to enter fail-recovery mode after LDO2 SCP entry, I_{OUT2} = 0.4A to short circuit, other I_{OUT} = 0.4A



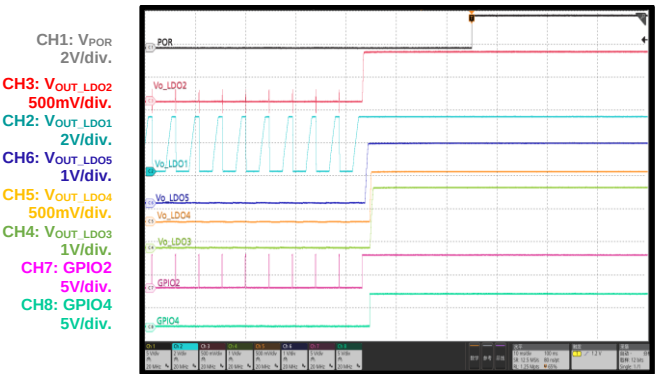
SCP Recovery (LDO2)

Configure the MPQ70700FS to enter fail-recovery mode after LDO2 SCP entry, I_{OUT2} = 0A to short circuit, other I_{OUT} = 0A



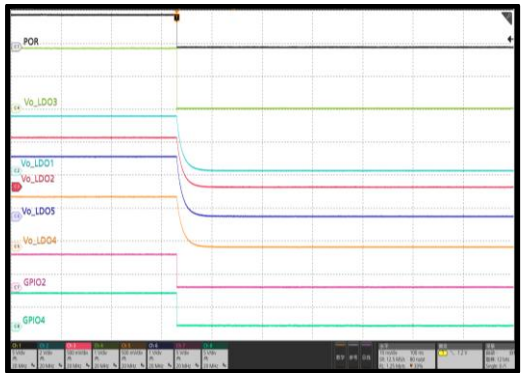
SCP Recovery (LDO2)

Configure the MPQ70700FS to enter fail-recovery mode after LDO2 SCP entry, I_{OUT2} = 0.4A to short circuit, other I_{OUT} = 0.4A



SCP Entry (LDO3)

Configure the MPQ70700FS to enter failsafe mode after LDO3 SCP entry, I_{OUT3} = 0A to short circuit, other I_{OUT} = 0A



SCP Entry (LDO3)

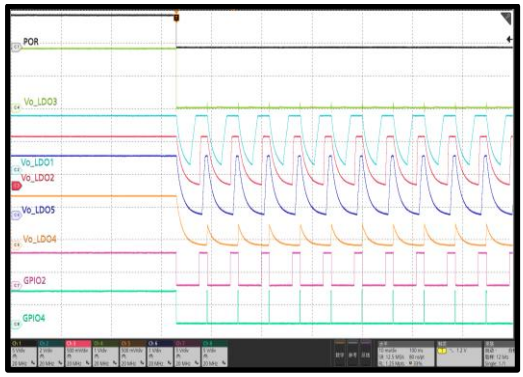
Configure the MPQ70700FS to enter failsafe mode after LDO3 SCP entry, I_{OUT3} = 0.4A to short circuit, other I_{OUT} = 0.4A

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

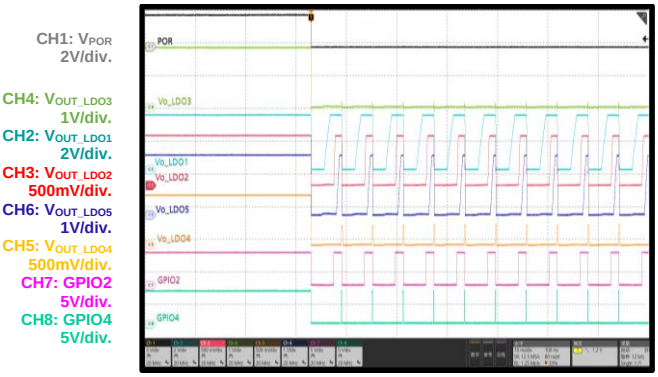
SCP Entry (LDO3)

Configure the MPQ70700FS to enter fail-recovery mode after LDO3 SCP entry, I_{OUT3} = 0A to short circuit, other I_{OUT} = 0A



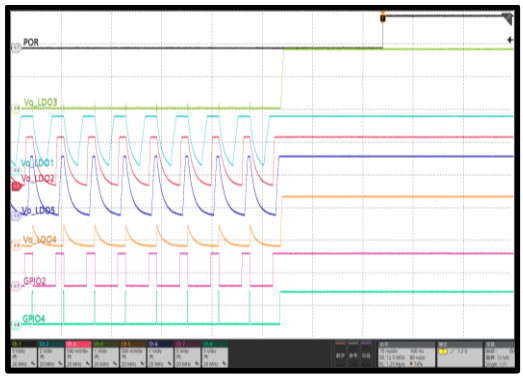
SCP Entry (LDO3)

Configure the MPQ70700FS to enter fail-recovery mode after LDO3 SCP entry, I_{OUT3} = 0.4A to short circuit, other I_{OUT} = 0.4A



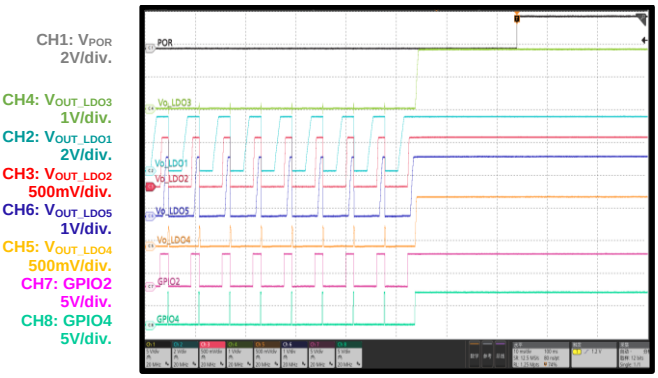
SCP Recovery (LDO3)

Configure the MPQ70700FS to enter fail-recovery mode after LDO3 SCP entry, I_{OUT3} = 0A to short circuit, other I_{OUT} = 0A



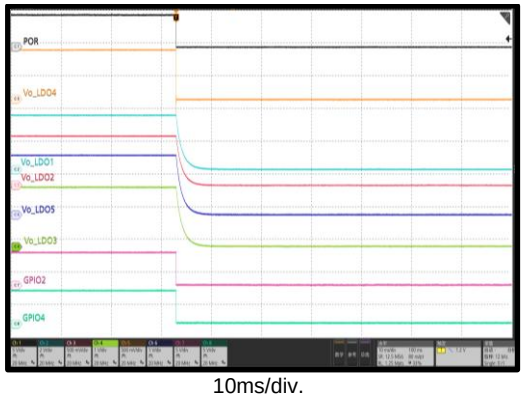
SCP Recovery (LDO3)

Configure the MPQ70700FS to enter fail-recovery mode after LDO3 SCP entry, I_{OUT3} = 0.4A to short circuit, other I_{OUT} = 0.4A



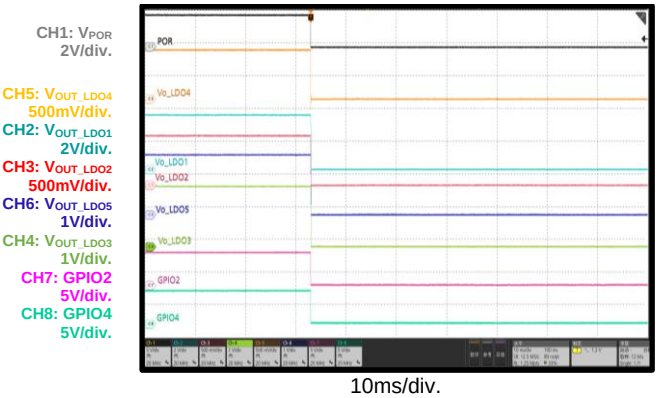
SCP Entry (LDO4)

Configure the MPQ70700FS to enter failsafe mode after LDO4 SCP entry, I_{OUT4} = 0A to short circuit, other I_{OUT} = 0A



SCP Entry (LDO4)

Configure the MPQ70700FS to enter failsafe mode after LDO4 SCP entry, I_{OUT4} = 0.4A to short circuit, other I_{OUT} = 0.4A

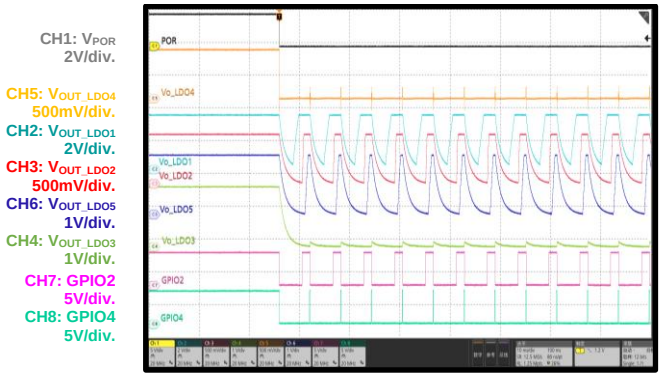


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

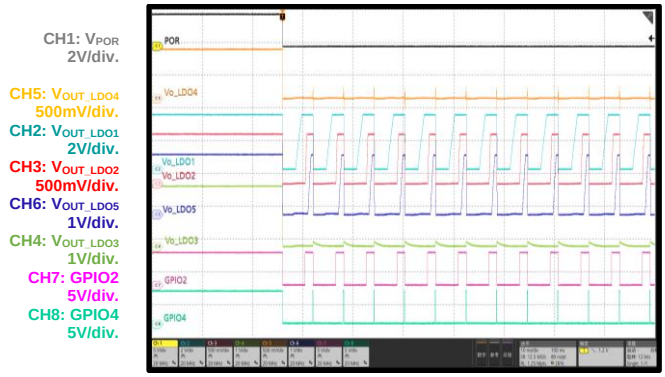
SCP Entry (LDO4)

Configure the MPQ70700FS to enter fail-recovery mode after LDO4 SCP entry, I_{OUT4} = 0A to short circuit, other I_{OUT} = 0A



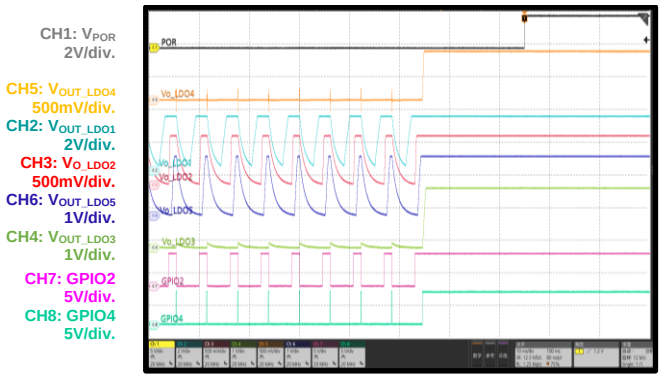
SCP Entry (LDO4)

Configure the MPQ70700FS to enter fail-recovery mode after LDO4 SCP entry, I_{OUT4} = 0.4A to short circuit, other I_{OUT} = 0.4A



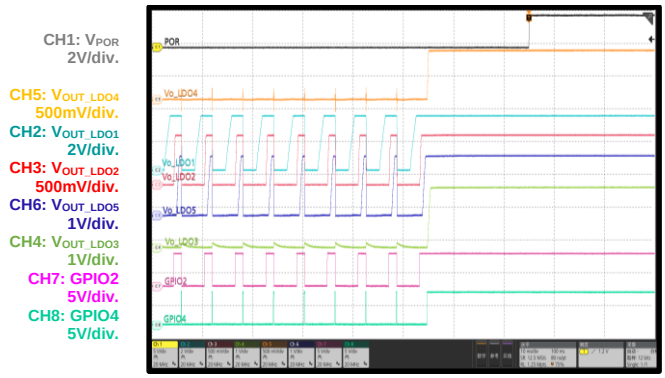
SCP Recovery (LDO4)

Configure the MPQ70700FS to enter fail-recovery mode after LDO4 SCP entry, I_{OUT4} = 0A to short circuit, other I_{OUT} = 0A



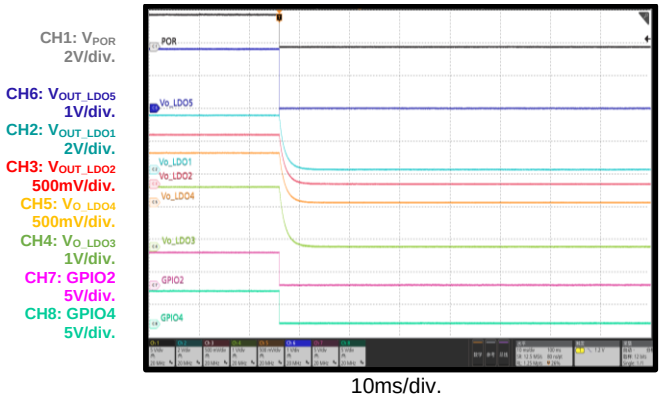
SCP Recovery (LDO4)

Configure the MPQ70700FS to enter fail-recovery mode after LDO4 SCP entry, I_{OUT4} = 0.4A to short circuit, other I_{OUT} = 0.4A



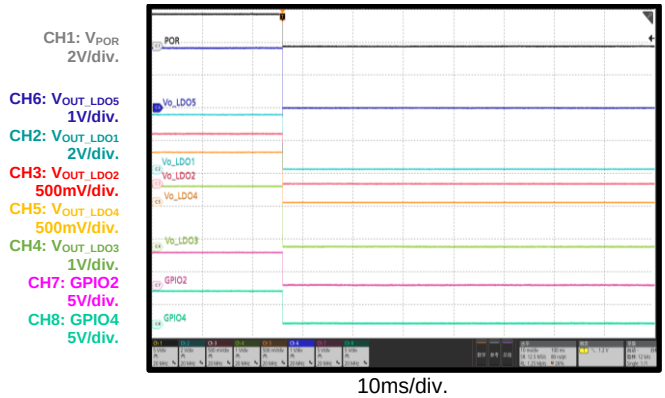
SCP Entry (LDO5)

Configure the MPQ70700FS to enter failsafe mode after LDO5 SCP entry, I_{OUT5} = 0A to short circuit, other I_{OUT} = 0A



SCP Entry (LDO5)

Configure the MPQ70700FS to enter failsafe mode after LDO5 SCP entry, I_{OUT5} = 0.4A to short circuit, other I_{OUT} = 0.4A

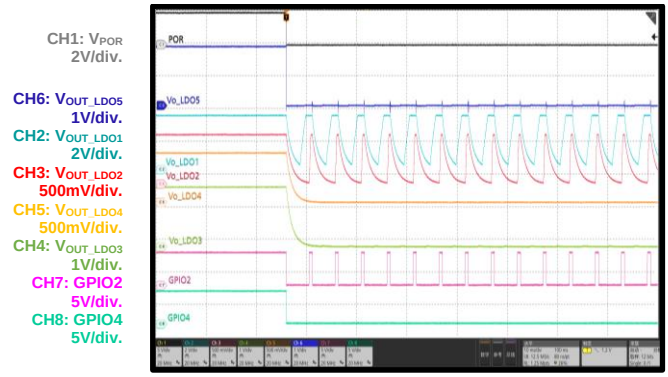


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

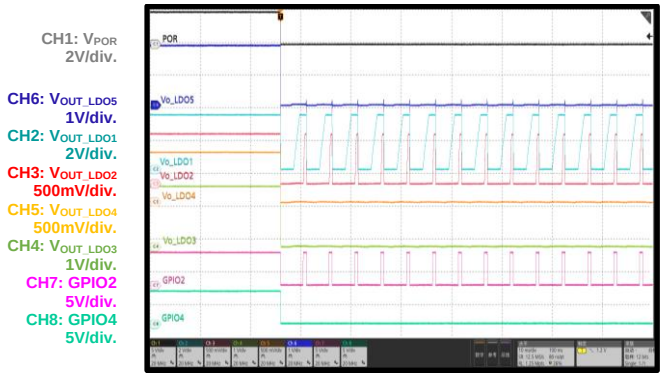
SCP Entry (LDO5)

Configure the MPQ70700FS to enter fail-recovery mode after LDO5 SCP entry, I_{OUT5} = 0A to short circuit, other I_{OUT} = 0A



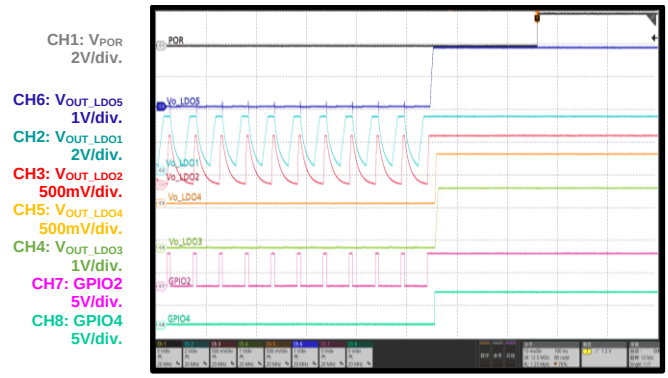
SCP Entry (LDO5)

Configure the MPQ70700FS to enter fail-recovery mode after LDO5 SCP entry, I_{OUT5} = 0.4A to short circuit, other I_{OUT} = 0.4A



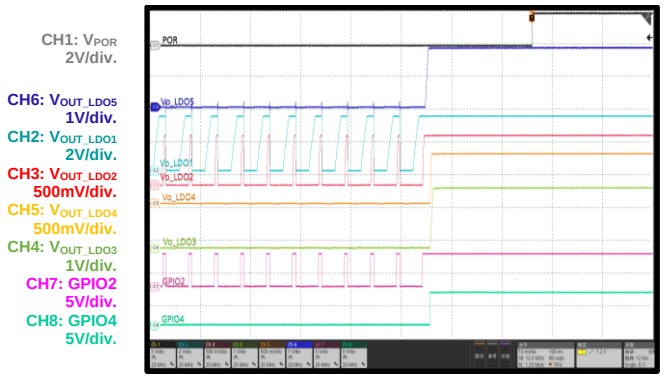
SCP Recovery (LDO5)

Configure the MPQ70700FS to enter fail-recovery mode after LDO5 SCP entry, I_{OUT5} = 0A to short circuit, other I_{OUT} = 0A



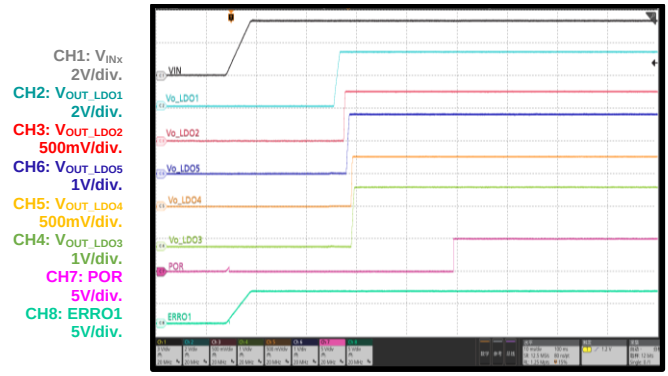
SCP Recovery (LDO5)

Configure the MPQ70700FS to enter fail-recovery mode after LDO5 SCP entry, I_{OUT5} = 0.4A to short circuit, other I_{OUT} = 0.4A



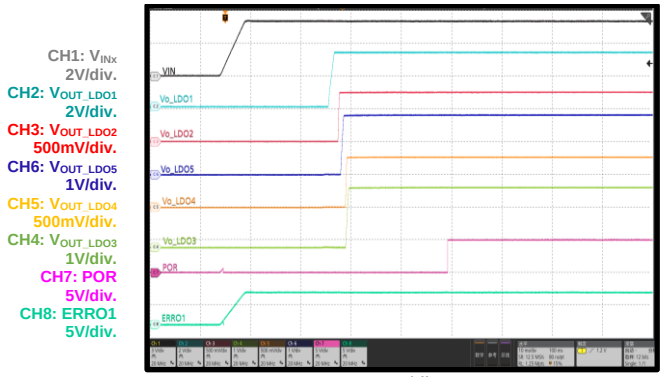
Start-Up through VIN (POR and ERRO1)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A



Start-Up through VIN (POR and ERRO1)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

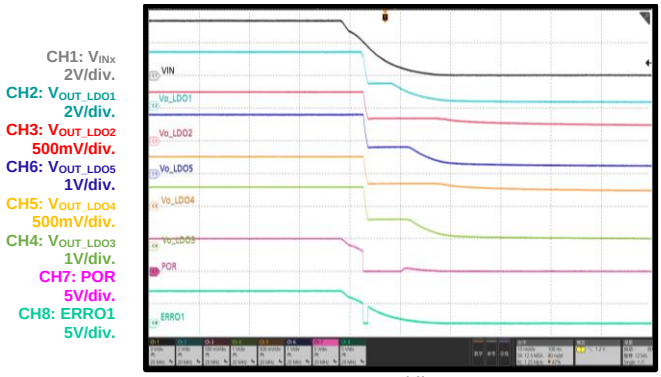


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

Shutdown through VIN (POR and ERRO1)

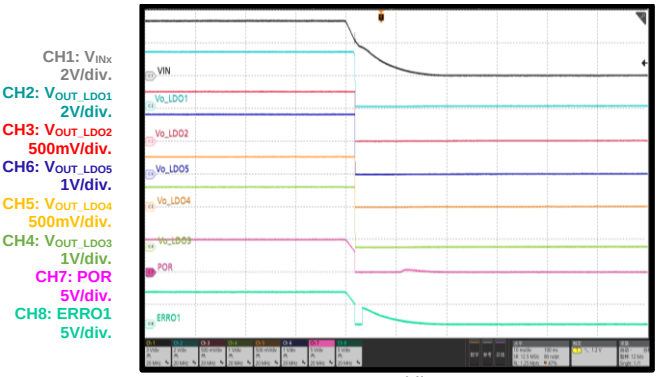
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A



10ms/div.

Shutdown through VIN (POR and ERRO1)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

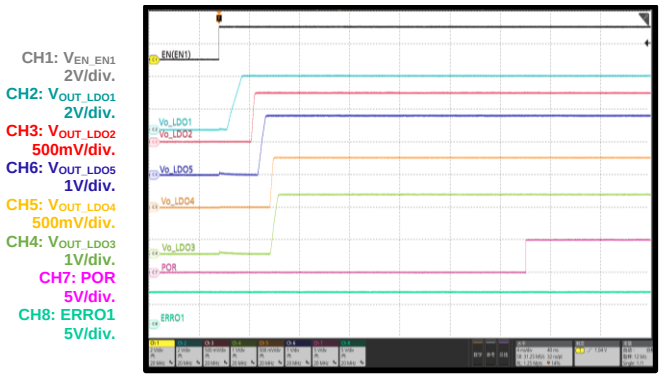


10ms/div.

Start-Up through EN (EN1) (POR and ERRO1)

V_{GPIO1_EN2} = 5V,

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

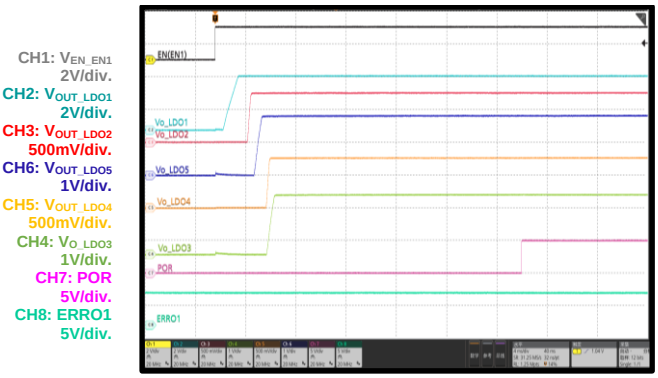


4ms/div.

Start-Up through EN (EN1) (POR and ERRO1)

V_{GPIO1_EN2} = 5V,

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

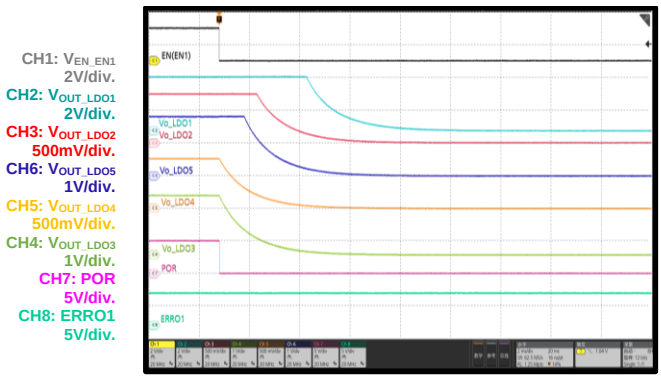


4ms/div.

Shutdown through EN (EN1) (POR and ERRO1)

V_{GPIO1_EN2} = 5V,

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

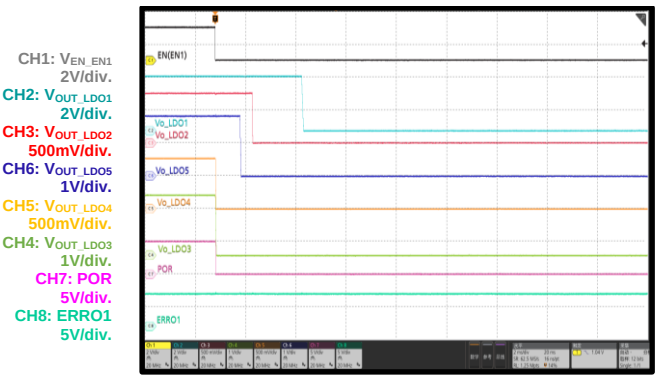


2ms/div.

Shutdown through EN (EN1) (POR and ERRO1)

V_{GPIO1_EN2} = 5V,

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A



2ms/div.

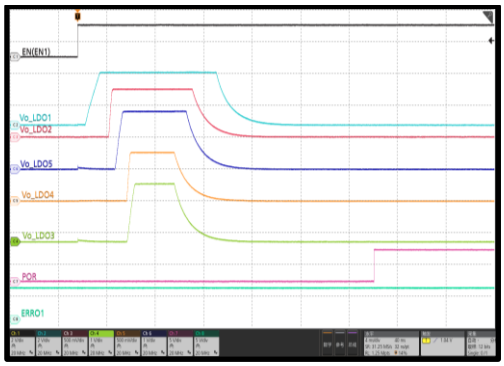
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

Start-Up through EN (EN1) (POR and ERRO1)

V_{GPIO1_EN2} = 0V,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

CH1: V_{EN_EN1} 2V/div.
CH2: V_{OUT_LDO1} 2V/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH6: V_{OUT_LDO5} 1V/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.



4ms/div.

Start-Up through EN (EN1) (POR and ERRO1)

V_{GPIO1_EN2} = 0V,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

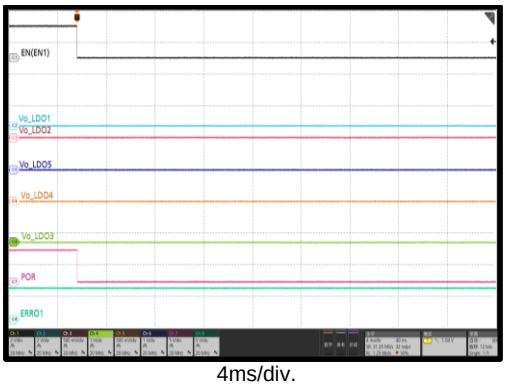
CH1: V_{EN_EN1} 2V/div.
CH2: V_{OUT_LDO1} 2V/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH6: V_{OUT_LDO5} 1V/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.

4ms/div.

Shutdown through EN (EN1) (POR and ERRO1)

V_{GPIO1_EN2} = 0V,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

CH1: V_{EN_EN1} 2V/div.
CH2: V_{OUT_LDO1} 2V/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH6: V_{OUT_LDO5} 1V/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.

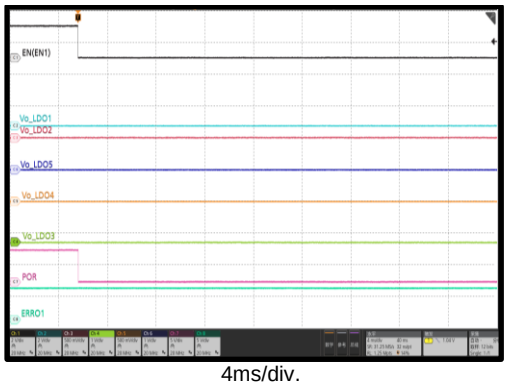


4ms/div.

Shutdown through EN (EN1) (POR and ERRO1)

V_{GPIO1_EN2} = 0V,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

CH1: V_{EN_EN1} 2V/div.
CH2: V_{OUT_LDO1} 2V/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH6: V_{OUT_LDO5} 1V/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.

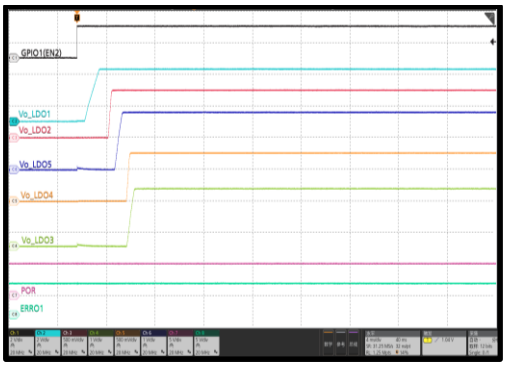


4ms/div.

Start-Up through GPIO1 (EN2) (POR and ERRO1)

V_{EN_EN1} = 5V,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

CH1: V_{GPIO1_EN2} 2V/div.
CH2: V_{OUT_LDO1} 2V/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH6: V_{OUT_LDO5} 1V/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.

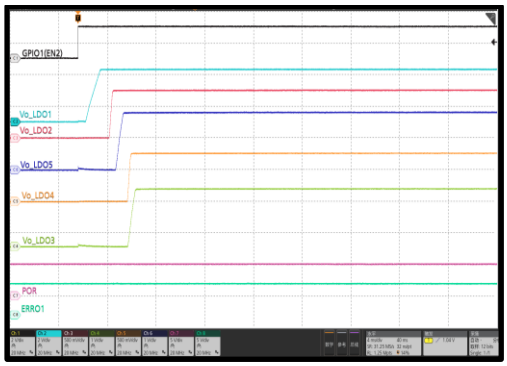


4ms/div.

Start-Up through GPIO1 (EN2) (POR and ERRO1)

V_{EN_EN1} = 5V,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

CH1: V_{GPIO1_EN2} 2V/div.
CH2: V_{OUT_LDO1} 2V/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH6: V_{OUT_LDO5} 1V/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.



4ms/div.

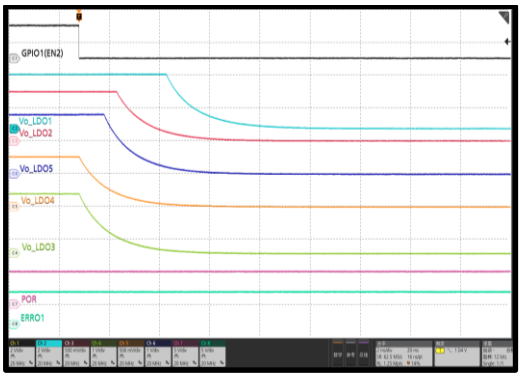
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

Shutdown through GPIO1 (EN2) (POR and ERRO1)

V_{EN_EN1} = 5V,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

CH1: V_{GPIO1_EN2} 2V/div.
CH2: V_{OUT_LDO1} 2V/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH6: V_{OUT_LDO5} 1V/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.

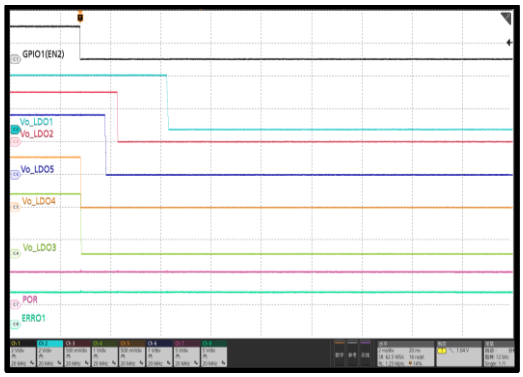


2ms/div.

V Shutdown through GPIO1 (EN2) (POR and ERRO1)

V_{EN_EN1} = 5V,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

CH1: V_{GPIO1_EN2} 2V/div.
CH2: V_{OUT_LDO1} 2V/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH6: V_{OUT_LDO5} 1V/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.

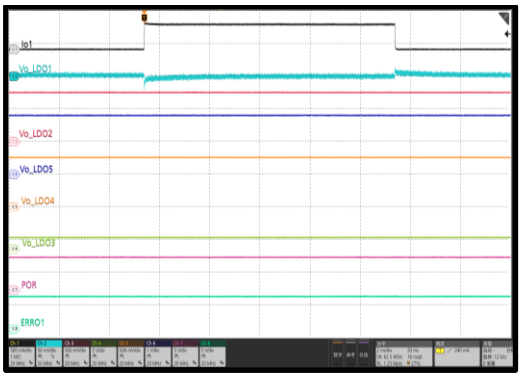


2ms/div.

Load Transient (LDO1)

I_{OUT1} = 0A to 0.4A, 2A/µs slew rate,
I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

CH1: I_{OUT1} 500mA/div.
CH2: V_{OUT_LDO1}/AC 50mV/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH6: V_{OUT_LDO5} 1V/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.



2ms/div.

Load Transient (LDO1)

I_{OUT1} = 0A to 0.4A, 2A/µs slew rate,
I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

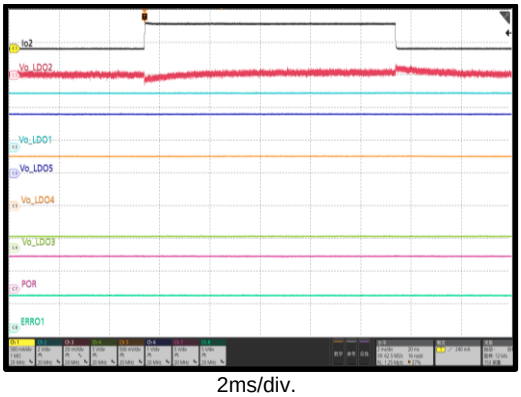
CH1: I_{OUT1} 500mA/div.
CH2: V_{OUT_LDO1}/AC 50mV/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH6: V_{OUT_LDO5} 1V/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.

2ms/div.

Load Transient (LDO2)

I_{OUT2} = 0A to 0.4A, 2A/µs slew rate,
I_{OUT1} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0A

CH1: I_{OUT2} 500mA/div.
CH3: V_{OUT_LDO2}/AC 20mV/div.
CH2: V_{OUT_LDO1} 2V/div.
CH6: V_{OUT_LDO5} 1V/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.

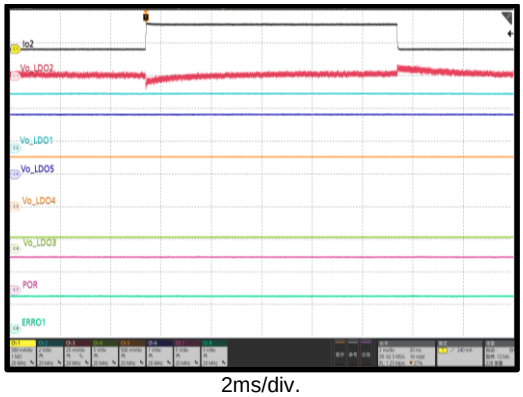


2ms/div.

Load Transient (LDO2)

I_{OUT2} = 0A to 0.4A, 2A/µs slew rate,
I_{OUT1} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0.4A

CH1: I_{OUT2} 500mA/div.
CH3: V_{OUT_LDO2}/AC 20mV/div.
CH2: V_{OUT_LDO1} 2V/div.
CH6: V_{OUT_LDO5} 1V/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.



2ms/div.

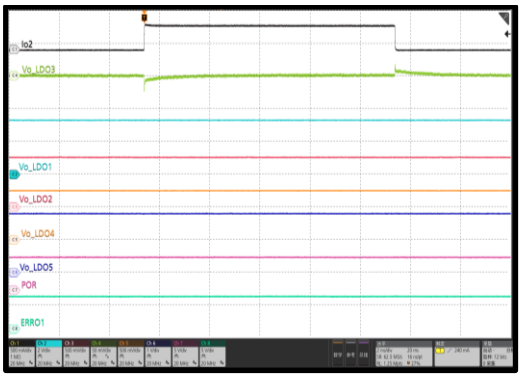
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.8V, V_{OUT4} = 0.75V, V_{OUT5} = 1.8V, C_{OUT1} = 4.7µF, C_{OUT2} = 4.7µF, C_{OUT3} = 4.7µF, C_{OUT4} = 4.7µF, C_{OUT5} = 4.7µF, T_A = 25°C, unless otherwise noted.

Load Transient (LDO3)

I_{OUT3} = 0A to 0.4A, 2A/µs slew rate,
I_{OUT1} = I_{OUT2} = I_{OUT4} = I_{OUT5} = 0A

CH1: I_{OUT3} 500mA/div.
CH4: V_{OUT_LDO3}/AC 50mV/div.
CH2: V_{OUT_LDO1} 2V/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH6: V_{OUT_LDO5} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.

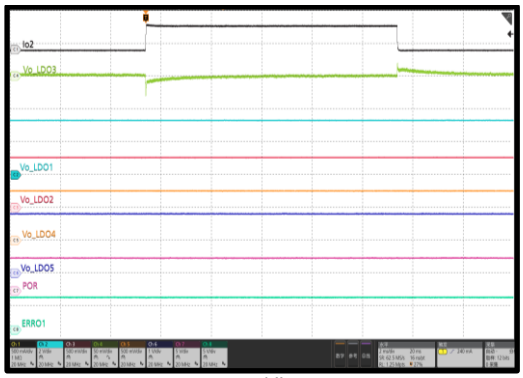


2ms/div.

Load Transient (LDO3)

I_{OUT3} = 0A to 0.4A, 2A/µs slew rate,
I_{OUT1} = I_{OUT2} = I_{OUT4} = I_{OUT5} = 0.4A

CH1: I_{OUT3} 500mA/div.
CH4: V_{OUT_LDO3}/AC 50mV/div.
CH2: V_{OUT_LDO1} 2V/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH6: V_{OUT_LDO5} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.

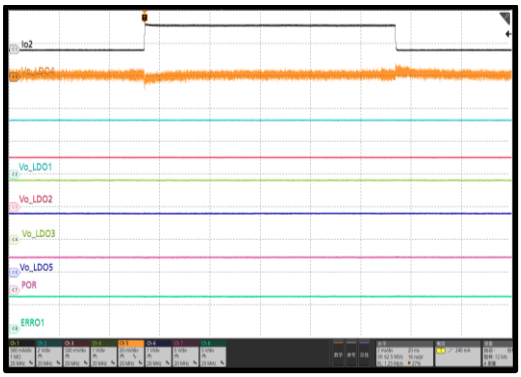


2ms/div.

Load Transient (LDO4)

I_{OUT4} = 0A to 0.4A, 2A/µs slew rate,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT5} = 0A

CH1: I_{OUT4} 500mA/div.
CH5: V_{OUT_LDO4}/AC 20mV/div.
CH2: V_{OUT_LDO1} 2V/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH6: V_{OUT_LDO5} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.

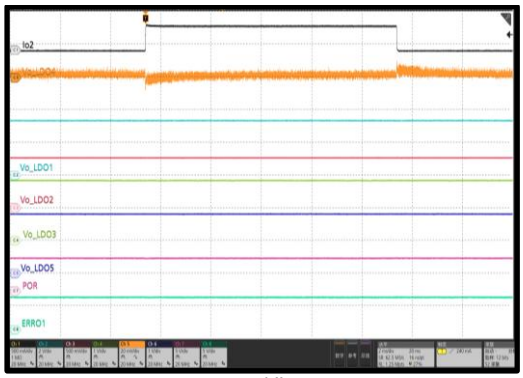


2ms/div.

Load Transient (LDO4)

I_{OUT4} = 0A to 0.4A, 2A/µs slew rate,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT5} = 0.4A

CH1: I_{OUT4} 500mA/div.
CH5: V_{OUT_LDO4}/AC 20mV/div.
CH2: V_{OUT_LDO1} 2V/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH6: V_{OUT_LDO5} 1V/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.

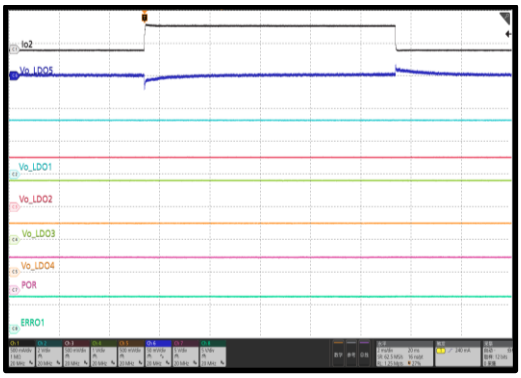


2ms/div.

Load Transient (LDO5)

I_{OUT5} = 0A to 0.4A, 2A/µs slew rate,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = 0A

CH1: I_{OUT5} 500mA/div.
CH6: V_{OUT_LDO5}/AC 50mV/div.
CH2: V_{OUT_LDO1} 2V/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.

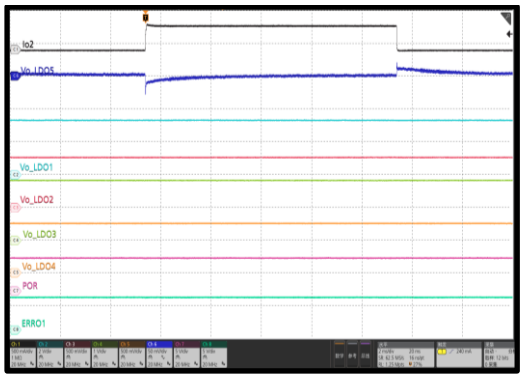


2ms/div.

Load Transient (LDO5)

I_{OUT5} = 0A to 0.4A, 2A/µs slew rate,
I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = 0.4A

CH1: I_{OUT5} 500mA/div.
CH6: V_{OUT_LDO5}/AC 50mV/div.
CH2: V_{OUT_LDO1} 2V/div.
CH3: V_{OUT_LDO2} 500mV/div.
CH4: V_{OUT_LDO3} 1V/div.
CH5: V_{OUT_LDO4} 500mV/div.
CH7: POR 5V/div.
CH8: ERRO1 5V/div.



2ms/div.

FUNCTIONAL BLOCK DIAGRAM

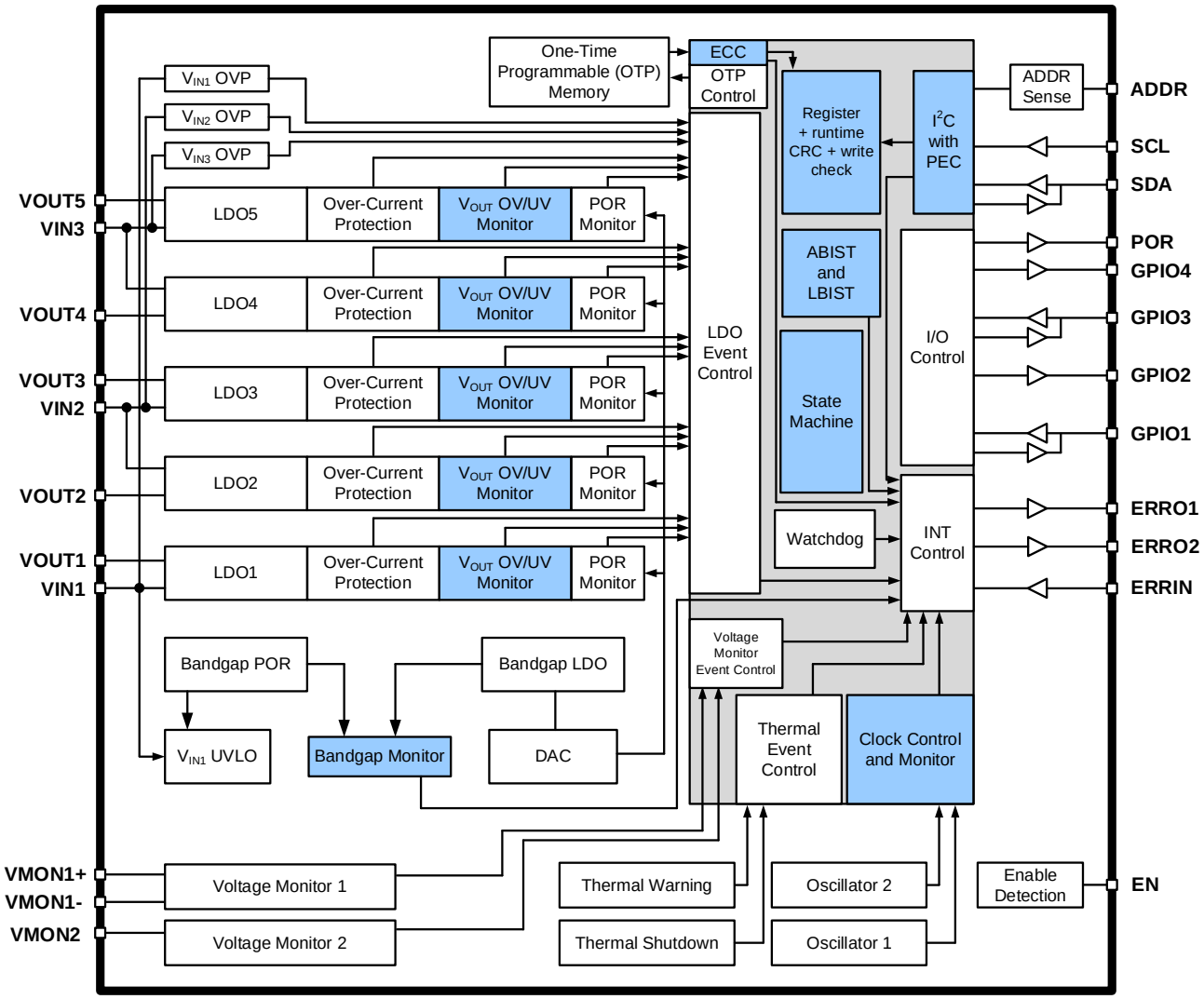


Figure 2: Functional Block Diagram

POWER-ON SEQUENCE

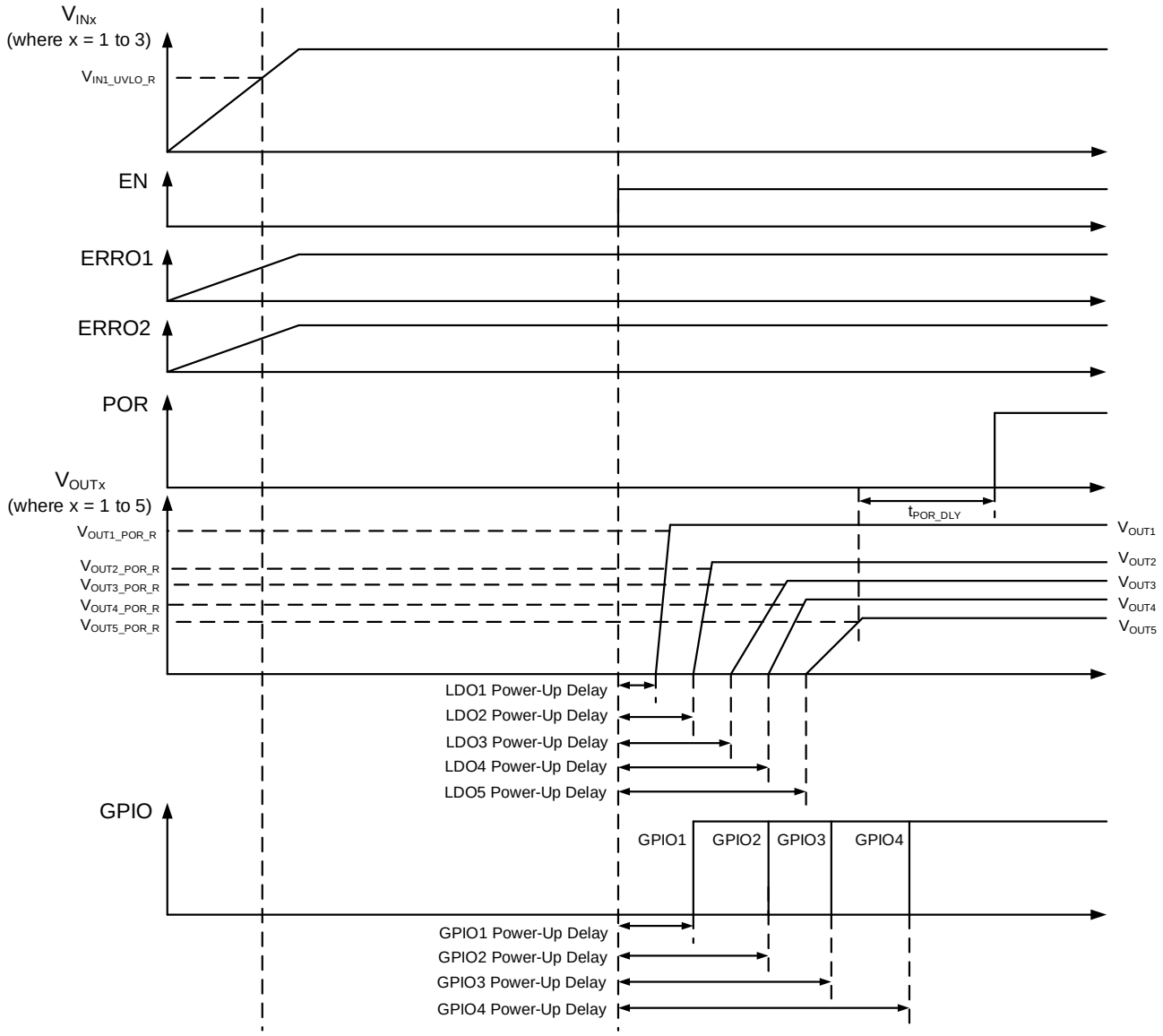


Figure 3: Power-Up Sequence Diagram (12)

Note:

12) ERRO1, ERRO2, and POR are connected to V_{INx} (where x = 1 to 3) via a 100kΩ resistor; VMON1 (the difference between VMON1+ and VMON1-) and VMON2 have input voltages that are between the VMONx (where x = 1 or 2) under-voltage (UV) threshold ($V_{MONx\_UV\_VTH}$) and VMONx over-voltage (OV) threshold ($V_{MONx\_OV\_VTH}$); and all GPIO pins are configured as output pins and connected to VOUT1 via a 100kΩ resistor.

OPERATION

The MPQ70700FS is a highly flexible power solution for advanced driver-assistance systems (ADAS) and system-on-chips (SoCs). It integrates 5 low-dropout (LDO) regulators. The integrated functional safety features improve system safety scores to meet ASIL-D requirements. The device also provides two voltage monitors and four GPIO pins that allow protection and sequence control to be extended to additional supplies. The I²C interface allows significant configurations to meet the requirements of the target SoC.

Low-Dropout (LDO) Regulators

The MPQ70700FS integrates 5 LDO regulators (LDO1, LDO2, LDO3, LDO4, and LDO5). The maximum output current (I_{OUT}) is 400mA. All the LDOs' output voltage (V_{OUTx}) (where x = 1 to 5) can be adjusted between 0.5V and 3.6V. V_{OUTx} can be set using the LDOx_VREF_MODE bit (where x = 1 to 5) (21h, 24h, 27h, 2Ah, 2Dh, bit[6]) and VREF_LDOx bits (where x = 1 to 5) (21h, 24h, 27h, 2Ah, 2Dh, bits[5:0]) via the I²C interface. If the LDOx_REF_MODE bit is set to 0, then the minimum V_{OUTx} step is 12.5mV, and the V_{OUTx} range is between 0.5V and 1.0375V. If the LDOx_REF_MODE bit is set to 1, then the minimum V_{OUTx} step is 50mV, and the V_{OUTx} range is between 1V and 3.6V. When setting V_{OUTx}, configure the LDOx_VREF_MODE bit, then configure the VREF_LDOx bits.

For example, the LDO2 output voltage (V_{OUT2}) can be set to 3.3V with the below steps:

1. Set LDO2_VREF_MODE (24h, bit[6]) to MODE1, with 50mV/step.
2. Based on the equations for calculating the LDO2 reference voltage (V_{REF2}) for MODE0 and MODE1 for the LDO2_VREF bits (24h, bits[5:0]), when V_{OUT2} is 3.3V, LDO2_VREF should be equal to 5'b101110.
3. Set V_{OUT2} to 3.3V via the LDO2_VREF bits.

The MPQ70700FS does not support dynamic voltage scaling (DVS). If V_{OUTx} is adjusted online, then the LDOs' over-voltage protection (OVP) and under-voltage protection (UVP) must be disabled via the I²C before adjusting V_{OUTx}. After V_{OUTx} is changed successfully, the LDOs' OVP and UVP must be enabled again via the I²C.

Internal Soft Start (SS)

Soft start (SS) is implemented to prevent the MPQ70700FS's V_{OUTx} from overshooting during start-up. When the MPQ70700FS starts up, the internal circuitry of each power rail generates a soft-start voltage (V_{SS}) that ramps up from 0V. V_{SS} is the positive input voltage of the error amplifier (EA). The soft-start period (t_{SS}) lasts until V_{SS} exceeds V_{REF}. At this point, V_{REF} becomes the EA's positive input voltage. The soft-start slew rate of each output is adjustable via the one-time programmable (OTP) memory.

The LDO output's soft-start rising slew rate voltage (V_{OUT_SS}) is configurable via the LDOx_SS_SLEW_RATE bits (where x = 1 to 5) (22h, 25h, 28h, 2Bh, 2Eh, bits[5:3]). If V_{OUTx} is between 10% x V_{REF} and 90% x V_{REF}, then V_{OUTx} increases according to V_{OUT_SS} during the SS period. V_{OUT_SS} can be adjusted between 0.625mV/µs and 66.6mV/µs.

Table 1 shows the V_{OUTx} slew rate configuration.

Table 1: V_{OUTx} Slew Rate Configuration

LDOx_SS_SLEW_RATE (where x = 1 to 5) (22h, 25h, 28h, 2Bh, 2Eh, bits[5:3])	LDO Soft-Start Rising Slew Rate Voltage (V_{OUT_SS})
000	0.625mV/µs
001	1.25mV/µs
010	2.5mV/µs
011	5mV/µs
100	10mV/µs
101	20mV/µs
110	33.3mV/µs
111	66.6mV/µs

A higher V_{OUT_SS} generates a larger LDO output current (I_{OUT_LIMIT}) during t_{SS}. This may trigger LDO over-current protection (OCP). As a result, a smaller output capacitance (C_{OUT}) can decrease I_{OUT_LIMIT} during t_{SS} when a higher V_{OUT_SS} is set. C_{OUT} must not be below 3.3µF.

Input Voltage

The LDO1 output voltage (V_{OUT1}) is powered by the LDO1 and internal circuit supply input voltage (V_{IN1}); the LDO2 and LDO3 output voltages (V_{OUT2} and V_{OUT3}, respectively) are powered by the LDO2 and LDO3 supply input voltage (V_{IN2}); and the LDO4 and LDO5 output voltages (V_{OUT4} and V_{OUT5}, respectively) are

powered by the LDO4 and LDO5 supply input voltage (V_{IN3}).

V_{IN1} is the main input of the power management IC (PMIC) for all internal circuits. No action is required if V_{IN1} is below its UVLO rising threshold ($V_{IN1\_UVLO\_R}$). Once V_{IN1} exceeds $V_{IN1\_UVLO\_R}$, the MPQ70700FS starts to pre-load the OTP. If V_{IN1} drops below its UVLO falling threshold ($V_{IN1\_UVLO\_F}$), then all the LDOs and the MPQ70700FS shut down.

The MPQ70700FS supports the separate use of the VIN1, VIN2, and VIN3 pins, where the input voltage (V_{INx}) (where x = 1 to 3) must exceed $V_{IN1\_UVLO\_R}$ and start up at the same time. In addition, V_{IN2} and V_{IN3} must not exceed V_{IN1}. If the system requires lower power dissipation on the LDOs, then the system can use a V_{INx} (where x = 2 to 3) to power a lower V_{OUTx} (where x = 2 to 5). V_{INx} must exceed $V_{IN1\_UVLO\_R}$ and start up at the same time. The MPQ70700FS provides V_{IN1}, V_{IN2}, and V_{IN3} OVP and different fault registers to record which V_{INx} OVP is triggered. The MPQ70700FS can enable V_{IN1}, V_{IN2}, and V_{IN3} OVP for each V_{INx} independently.

Enable (EN)

EN is a level-trigger input pin for the MPQ70700FS that generates a power-up or power-down event. If all V_{INx} are ready, pull the EN pin voltage (V_{EN}) below the falling threshold (0.4V) to shut down all V_{OUTx} and GPIO outputs. All GPIO outputs are configured via the GPIO_CFG (1Bh) command, and certain V_{OUTx} are enabled via the CHANNEL_EN (18h) command after pulling up the EN pin voltage (V_{EN}) above its rising threshold (1.3V). This means the physical EN pin has higher priority than the software enable function. If V_{EN} is pulled below 0.4V, then all V_{OUTx} are shut down even though all LDOs are enabled via the CHANNEL_EN command. After the EN pin's status is changed, if the EN level duration is shorter than 1µs, then the MPQ70700FS disregards the EN status change and does not take any action.

Figure 4 shows the EN power-on sequence.

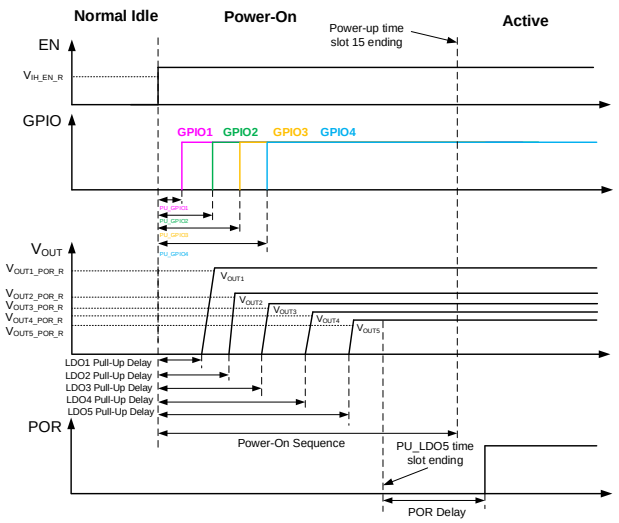


Figure 4: EN Power-On Sequence

Figure 5 shows the EN power-on and power-off sequences with an example where all GPIOs are configured to output and all LDOs are enabled.

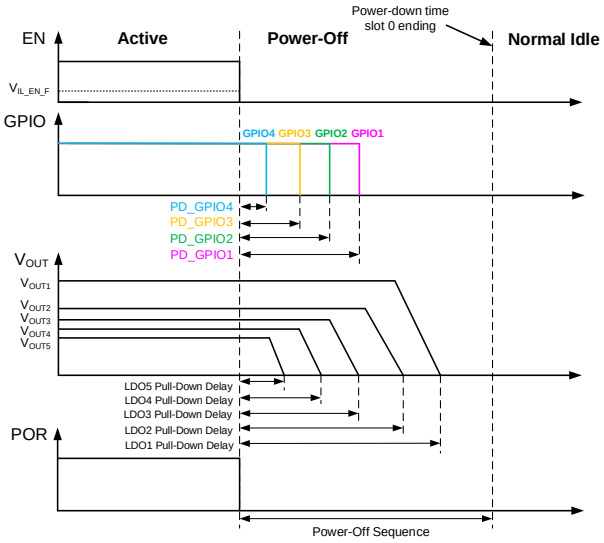


Figure 5: Example of EN Power-On and Power-Off Sequences with GPIO Outputs and Enabled LDOs

General-Purpose Input/Outputs (GPIOs)

The MPQ70700FS provides four GPIO pins (GPIO1, GPIO2, GPIO3, and GPIO4). GPIO1 and GPIO3 can be used as input or output pins, configured via the GPIO_CFG (1Bh) command. GPIO2 and GPIO4 are output pins, and cannot be configured as an input.

If configured as an output pin, the GPIOs can be used as a sequence output, and are controlled by the EN pin. The GPIO's output is pulled high

after the PU_GPIOx (where x = 1 to 4) (1Dh, 1Eh, 1Fh, and 20h, bits[7:4]) time, or pulled low after the PD_GPIOx time if V_{EN} exceeds its rising threshold ($V_{IH\_EN\_R}$) or drops below its falling threshold ($V_{IL\_EN\_F}$) (see Figure 4 and Figure 5 on page 37).

If the GPIOs are configured as input pins, then the MPQ70700FS can provide different functions for each GPIO pin.

If GPIO1 is configured as an input pin, then GPIO1 can control whether the MPQ70700FS enters or exits sleep mode in active state. In active state, if the GPIO1 input voltage (V_{GPIO1}) drops below its input low threshold (V_{IL_GPIO1}) (0.4V), then the MPQ70700FS shuts down each LDO and GPIO output, then enters sleep mode. In sleep mode, if V_{GPIO1} exceeds its input high threshold (V_{IH_GPIO1}) (1.3V), then the MPQ70700FS starts up each LDO and GPIO output, then exits sleep mode. The MPQ70700FS can configure whether each LDO and GPIO output is controlled by the GPIO1 pin via the EN2_GROUP (17h) command. The GPIO1 input pin can enable each LDO and GPIO output, meaning it can be regarded as EN2, and the EN pin can be regarded as EN1. The MPQ70700FS can turn off certain LDOs and GPIO outputs by pulling down EN2, which reduces power consumption in sleep mode.

Figure 6 shows the sleep mode entry sequence using an example where LDO1, LDO4, and LDO5 as well as the GPIO2 and GPIO3 outputs can be controlled by the GPIO1 pin (EN2) when it is configured as an input pin.

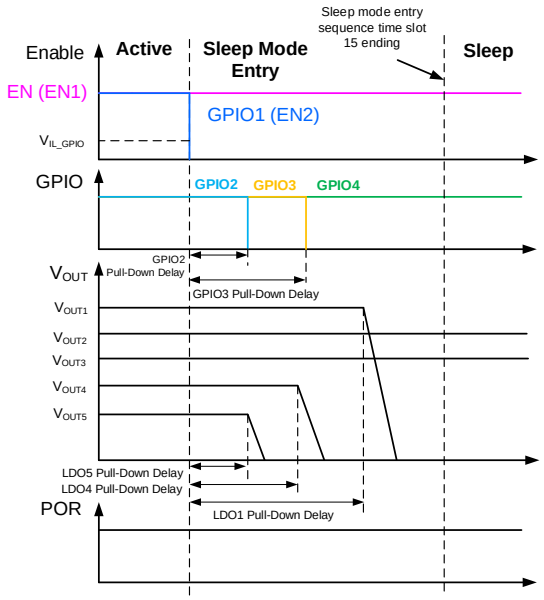


Figure 6: Sleep Mode Entry Sequence

Figure 7 shows the sleep mode exit sequence using an example where LDO1, LDO4, and LDO5 as well as the GPIO2 and GPIO3 outputs can be controlled by the GPIO1 pin (EN2) when GPIO1 is configured as an input pin.

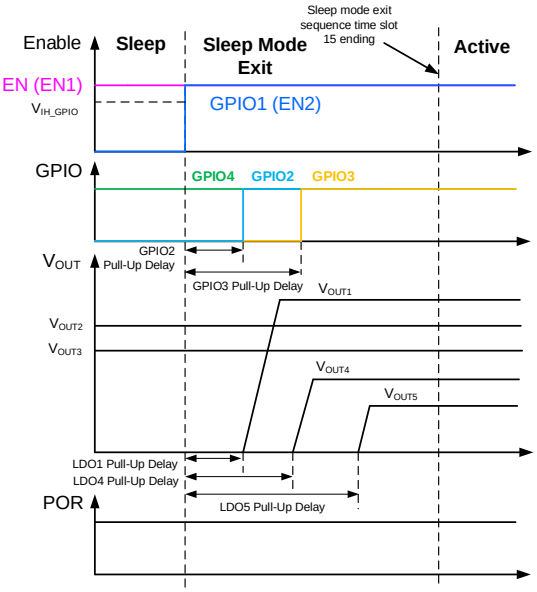


Figure 7: Sleep Mode Exit Sequence

Figure 8 on page 39 shows that when V_{EN} drops below $V_{IL\_EN\_F}$, all the LDOs and GPIO outputs shut down although EN2 is high.

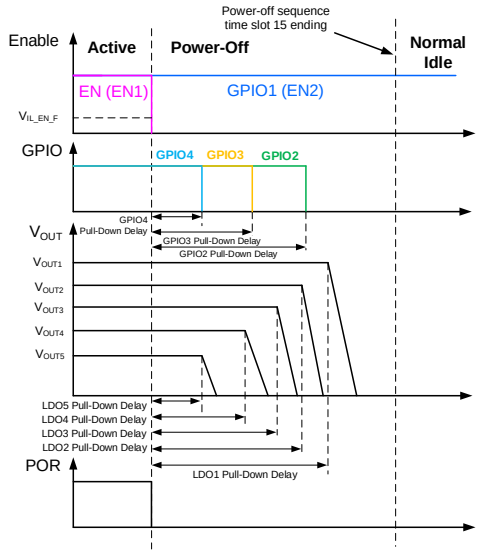


Figure 8: EN Power-Off Sequence with High GPIO1 (EN2)

If V_{EN} drops below $V_{IH\_EN\_F}$, then all the LDOs and GPIO outputs shut down although GPIO1 (EN2) is low. The state machine transitions from sleep mode to power-off and stops in normal idle state. Figure 9 shows an example where LDO2, LDO3, and the GPIO4 output are controlled by GPIO1 (EN2).

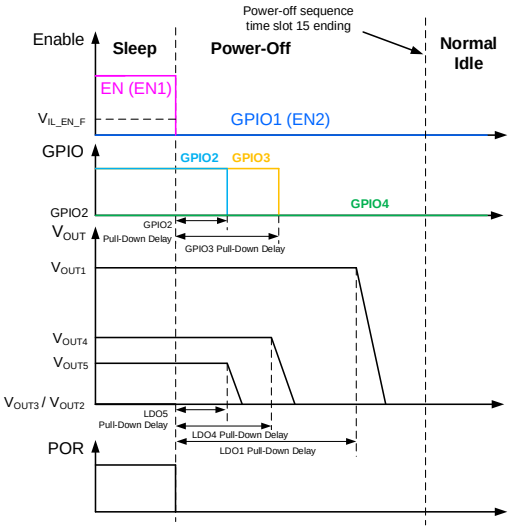


Figure 9: EN Power-Off Sequence with Low GPIO1 (EN2)

When the MPQ70700FS triggers start-up through EN (EN1), the LDOs' outputs and GPIO outputs have different actions with low GPIO1 (EN2). Figure 10 shows an example where GPIO1 (EN2) is low during start-up through EN (EN1).

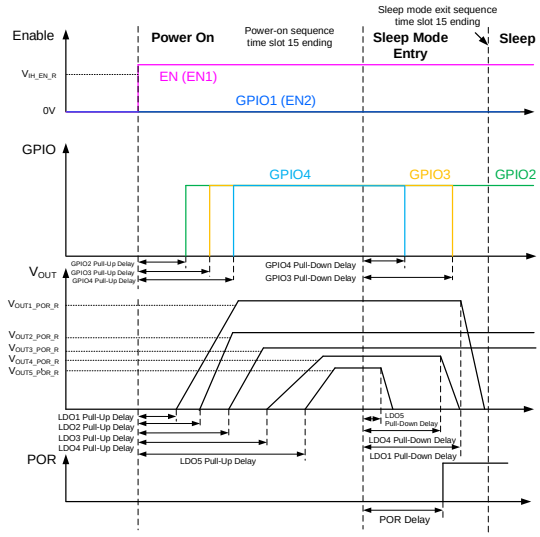


Figure 10: Low GPIO1 (EN2) during EN (EN1) Power-On Sequence

If GPIO3 is configured as an input pin, then GPIO3's input voltage controls V_{OUT1}. V_{OUT1} is 3.3V when this pin is low (V_{GPIO3} drops below V_{IL_GPIO3}), and V_{OUT1} is 1.8V when this pin is high (V_{GPIO3} exceeds V_{IH_GPIO3}). V_{OUT1} cannot be set by writing to the I^2C via the VREF_LDO1 (21h) command. Meanwhile, the V_{OUT1} over-voltage (OV), under-voltage (UV), and power-on reset (POR) thresholds can only be set via the LDO1_GPIO3_CTL_CFG bits (22h, bits[2:1]).

Similar to the adjustment via the VREF_LDO1 (21h) command, the GPIO3 input pin does not support setting V_{OUT1} online. If V_{OUT1} is adjusted online, then LDO1's OVP and UVP must be disabled via the I^2C before adjusting V_{OUT1}.

Time Slot

There are 16 time slots for the power-up and power-down sequences. A time slot can be set via the TIME_SLOT (1Ch) command, and ranges between 100µs and 6475µs, with 100µs/step. All the LDOs and GPIOs can be configurable between 0 and 15 time slots via the SEQ_LDOx commands (where x = 1 to 5) (23h, 26h, 29h, 2Ch, and 2Fh, respectively) and SEQ_GPIOx commands (where x = 1 to 4) (1Dh, 1Eh, 1Fh, and 20h, respectively). For the power-up sequence, time slot 0 is the first time slot; for the power-down sequence, time slot 15 is the first time slot. The turn-on and turn-off delay time of the LDO and GPIO outputs are determined by these commands.

An example of setting the turn-on and turn-off delay times of LDO1 and GPIO2 is provided below:

1. Confirm the turn-on and turn-off delay times of LDO1 and GPIO2, where the LDO1 turn-on delay time ($t_{ON\_DLY\_LDO1}$) is 5ms, the LDO1 turn-off delay time ($t_{OFF\_DLY\_LDO1}$) is 2ms, the GPIO2 turn-on delay time ($t_{ON\_DLY\_GPIO2}$) is 3ms, and the GPIO2 turn-off delay time ($t_{OFF\_DLY\_GPIO2}$) is 1ms.
2. Based on the maximum delay time to reach the minimum time slot, the minimum time slot is equal to the maximum delay time divided by 16. If the TIME_SLOT command is not between the minimum time slot and maximum time slot, then the next level greater than the calculated value should be selected. This means the minimum time slot is 400µs.
3. Based on the minimum delay time to reach the maximum time slot, the maximum time slot is equal to the minimum delay time. This means the maximum time slot is 1ms.
4. Select the time slot. The appropriate time slot must be selected to ensure that all delay times are divisible by time slots. The time slot can be 1ms.
5. Confirm the sequence number of LDO1 and GPIO2. The LDO1 power-up sequence number is time slot 5. The GPIO2 power-up sequence number is time slot 3. The LDO1 power-down sequence number is time slot 13. The GPIO2 power-down sequence number is time slot 14.

Figure 11 shows the power-on sequence. The first power-on sequence is time slot 0.

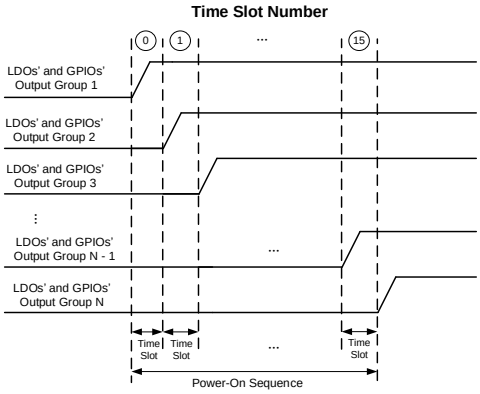


Figure 11: Power-On Sequence

Figure 12 shows the power-off sequence. The first power-off sequence is time slot 15.

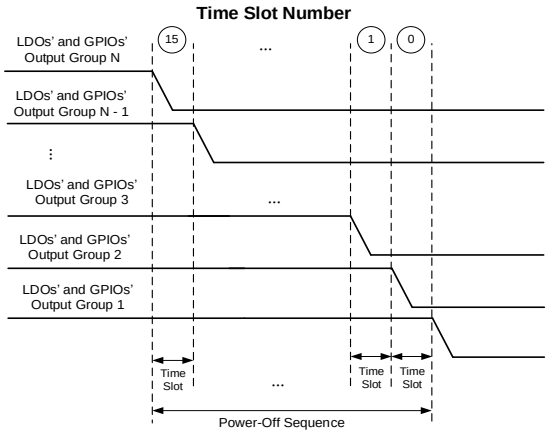


Figure 12: Power-Off Sequence

Power-On Reset (POR)

The POR pin is the open-drain output. During the power-on sequence, all V_{OUTx} exceed their respective POR rising thresholds ($V_{OUTx\_POR\_R}$), and no other faults force POR to go low. POR goes high after the power-up time slot of the last LDO ends. The MPQ70700FS asserts the POR pin until the POR delay time ends. The POR delay time can be set via the POR_CTL_DLY (35h) command.

Figure 13 shows POR with start-up through EN (EN1).

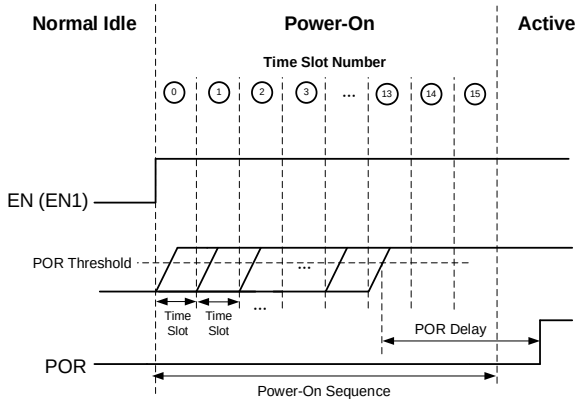


Figure 13: POR with Start-Up through EN (EN1)

If V_{OUTx} does not exceed $V_{OUTx\_POR\_R}$ during power-on, which is considered abnormal V_{OUTx}, then the POR pin is not pulled high. Figure 14 on page 41 shows the POR action with abnormal V_{OUTx}.

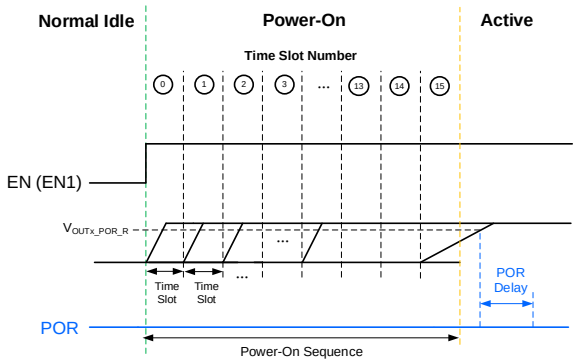


Figure 14: POR Action with Abnormal V_{OUTx}

After the shutdown through EN (EN1) signal, the POR pin is asserted. Figure 15 shows POR with shutdown through EN (EN1).

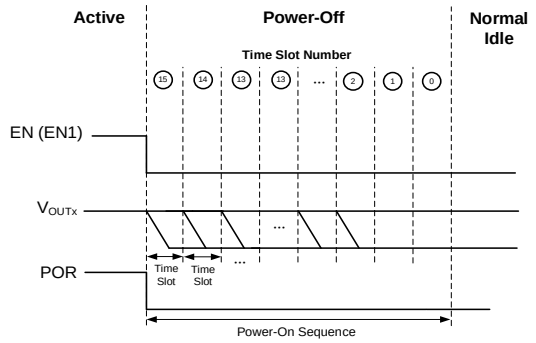


Figure 15: POR with Shutdown through EN (EN1)

If POR is pulled high, then GPIO1 (EN2) does not impact POR operation (see Figure 6 and Figure 7 on page 38).

The POR pin can be reset when the ERRIN signal is asserted (see Figure 16).

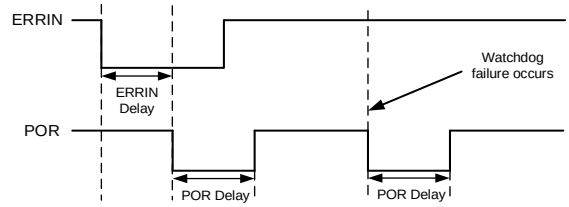


Figure 16: POR Pin Reset

1 indicates a low valid ERRIN signal, meaning the ERRIN signal is pulled low to assert the ERRIN signal. 2 indicates a high valid ERRIN signal, meaning the ERRIN signal is pulled high to assert the ERRIN signal. The ERRIN_MODE bit (14h, bit[6]) can configure whether the signal received by ERRIN is a high or low valid signal. Otherwise, a watchdog failure occurs. POR remains asserted (low) and is not pulled high until the POR delay time ends.

The SoC or microcontroller unit (MCU) must release the ERRIN signal during the POR delay. Otherwise, the POR pin continues to pull down after the delay. Figure 17 shows the POR action with a low valid ERRIN signal and the ERRIN pin always low.

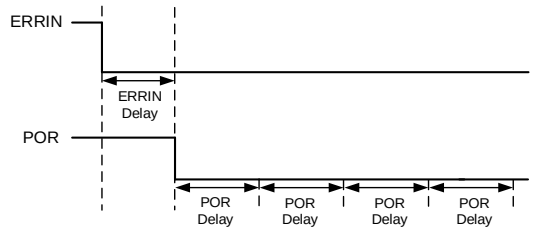


Figure 17: POR Action with the ERRIN Signal Continuously Asserted

ERRIN signal assertion and watchdog failure can cause the POR pin to reset. Other fault events can also cause the POR pin to reset. See Table 2 on page 44 for more details on the fault types.

Voltage Monitors (VMON1 and VMON2)

The MPQ70700FS provides two voltage monitors (VMON1 and VMON2). VMON1 is a differential input for monitoring important voltages such as the SoC CPU voltage, and VMON2 is a single input pin. These voltage monitors can extend ASIL protection to another power supply.

The MPQ70700FS provides configurable OVP and UVP for VMON1 and VMON2. The monitor's OV and UV limits are defined via the MONx_OV_THRESHOLD bits (where x = 1 or 2) (36h or 39h, bits[7:0]) and the MONx_UV_THRESHOLD bits (where x = 1 or 2) (37h or 3Ah, bits[7:0]), respectively, with 12.5mV/step. In addition, for each voltage monitor, the MPQ70700FS can independently set the state for monitoring voltage. The MON1_MODE (38h) and MON2_MODE (3Bh) commands can configure the option. If a fault occurs in the selected state, then the MPQ70700FS performs the corresponding action; in the other states, the MPQ70700FS has no reaction. Once a monitor OV/UV fault occurs, the MPQ70700FS can set the state machine to enter the fail-safe or fail-recovery protection mechanism via the FAULT_REACTION_GUPx command (where x = 1 to 4) (0Fh, 10h, 11h, and 12h).

If the set state machine enters fail-safe protection, then the MPQ70700FS is only reset by turning V_{INx} on and off after detecting a valid VMONx (where x = 1 or 2) OV or UV fault. If the set state machine enters fail-recovery protection, then the MPQ70700FS waits for the recovery delay time after detecting a valid VMONx OV or UV fault, then starts up again. All V_{OUTx} can recover to normal operation during the next start-up if the VMONx OV or UV fault is removed.

To prevent external interferences that cause the chip to mistakenly detect a VMONx OV or UV fault, the MPQ70700FS provides a debounce time to filter interference. If a VMONx OV or UV fault occurs and the duration exceeds the debounce time, then the MPQ70700FS shuts down all channels. If VMONx OV or UV fault occurs but the VMONx input voltage recovers normally before the debounce time ends, then the MPQ70700FS does not take any action. The debounce time is configurable between 10µs and 80µs (10µs, 20µs, 40µs, and 80µs) via the MON1_DEBOUNCE bits (38h, bits[1:0]) and MON2_DEBOUNCE bits (3Bh, bits[1:0]).

Figure 18 shows that if a VMONx OV fault occurs, then the MPQ70700FS enters fail-recovery protection.

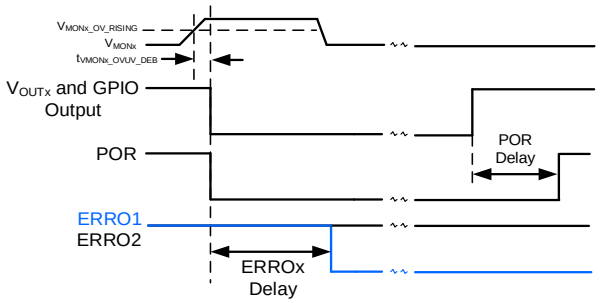


Figure 18: VMONx OV Fault Reaction

Low-Dropout (LDO) Output Voltage Protection

All the LDO channels have independent internal monitors for V_{OUTx}. If V_{OUTx} exceeds its OV rising threshold ($V_{OUTx\_OV\_RISING}$) or drops below its UV falling threshold ($V_{OUTx\_UV\_FALLING}$), then the MPQ70700FS shuts down all channels and records the fault in the F_LDOx_OV bits (where x = 1 to 5) (05h, bits[4:0]) or in the F_LDOx_UV bits (where x = 1 to 5) (06h, bit [4:0]). Then the PMIC enters failsafe or fail-recovery state. The state machine's reaction is configurable via the related FAULT_REACTION_GUP2 (10h) and FAULT_REACTION_GUP3 (11h) commands. $V_{OUTx\_OV\_RISING}$ and $V_{OUTx\_UV\_FALLING}$ can be set via the LDOx_OV_VTH (where x = 1 to 5) (3Ch, 3Fh, 42h, 45h, and 48h) and LDOx_UV_VTH (where x = 1 to 5) (3Dh, 40h, 43h, 46h, and 49h) commands.

To prevent external interferences that cause the chip to mistakenly trigger an OV or UV fault. The MPQ70700FS requires that the duration of V_{OUTx} OVP or UVP is longer than the debounce time. Otherwise, the MPQ70700FS can take any action. The debounce time is configurable between 10µs and 80µs (10µs, 20µs, 40µs, or 80µs) via the LDOx_MODE commands (where x = 1 to 5) (3Eh, 41h, 44h, 47h, and 4Ah).

If the set state machine enters failsafe protection, then the MPQ70700FS is only reset by turning V_{INx} on and off after detecting a valid V_{OUTx} OV or UV fault. If the set state machine enters fail-recovery protection, then the MPQ70700FS waits for the recovery delay time after detecting a valid V_{OUTx} OV or UV fault, then starts up again. All V_{OUTx} can recover to normal operation during the next start-up if the V_{OUTx} OV or UV fault is removed. Figure 19 shows that if V_{OUTx} drops below $V_{OUTx\_UV\_FALLING}$, then a V_{OUTx} UV fault is triggered.

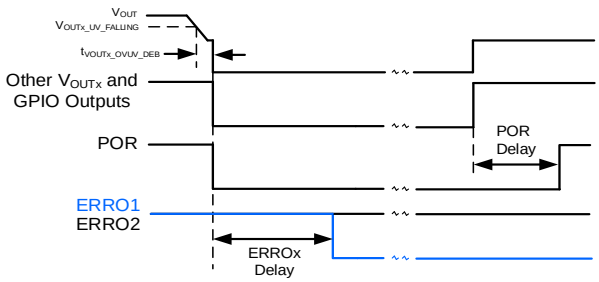


Figure 19: V_{OUTx} UV Fault Reaction

In addition, if V_{OUTx} is below the sum of $V_{OUTx\_UV\_FALLING}$ and $V_{OUTx\_UV\_HYS}$ during the power-on sequence, then the MPQ70700FS triggers a V_{OUTx} UV fault at the end of the power-on sequence (see Figure 20 on page 43).

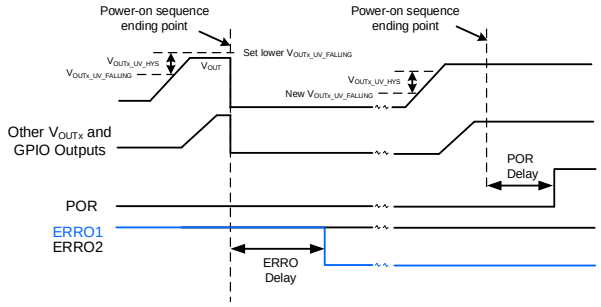


Figure 20: V_{OUTx} UV Fault Reaction during Power-On Sequence

Low-Dropout (LDO) Over-Current Protection (OCP)

The MPQ70700FS provides configurable output over-current protection (OCP) for each LDO, where OCP can be enabled via the F_EN_LDOx_OC bits (where x = 1 to 5) (0Dh, bits[4:0]). The OCP threshold is fixed at 500mA (typically). If any LDO I_{OUTx} (where x = 1 to 5) exceeds the OCP limit and the hold time exceeds the debounce time (configured to 10µs, 20µs, 40µs, or 80µs via the LDO1_MODE (3Eh) command), then the MPQ70700FS detects a valid OCP failure.

If the MPQ70700FS detects a valid OCP failure and discharge is enabled, then all channels shut down and discharge via a 100Ω resistor. ERRO1 is asserted after the ERRO delay time, which is the delay time for ERRO1 and ERRO2. POR is asserted immediately. The F_LDOx_OC bits (where x = 1 to 5) (07h, bits[4:0]) record the over-current (OC) fault in the corresponding LDO. In addition, the MPQ70700FS's state machine transitions from its current state to fail safe or fail recovery, which can be set via the F_GUP_LDOx_OC bits (where x = 1 to 5) (12h, bits[4:0]).

Once an OC fault occurs, if fail safe is selected, then V_{IN} on/off control is required to work properly again. If fail recovery is selected and I_{OUT} drops below the OCP limit, then the MPQ70700FS resumes normal operation during the next power-on sequence.

Figure 21 shows an example of an OC fault that causes a failsafe state, and the recovery from fail safe.

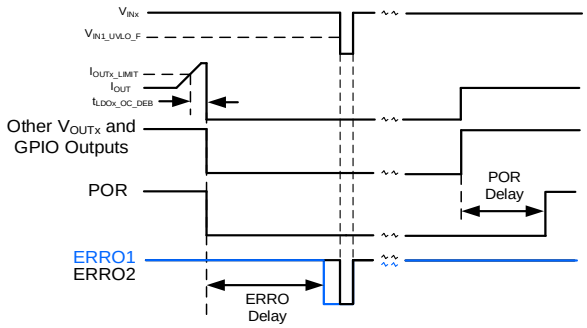


Figure 21: I_{OUTx} OC Fault Reaction

Adaptive Clock Enable Control

In normal idle state, the MPQ70700FS can disable the clock automatically. This disables the digital domain while the digital block does not take any action. The MPQ70700FS does not require a response from the digital block, which decreases the quiescent current (I_Q) and saves power.

Any fault events, sequence events, and I^2C communications trigger the MPQ70700FS to enable the clock and for the digital block to take action if a fault or sequence event occurs. Once all missions are done, the part disables the clock again to save power in normal IDLE state. If the ERRO1 and ERRO2 pins pull up V_{IN} via a 100kΩ resistor, then I_Q exceeds the previous value since ERRO1 and ERRO2 are pulled down. A clear fault flag can pull ERRO1 and ERRO2 high again, then I_Q is equal to the previous value.

Figure 22 shows ERRO2 connected to V_{IN} via a 100kΩ resistor and the VIN shutdown current (I_{Q_OFF}) under an ERRIN fault.

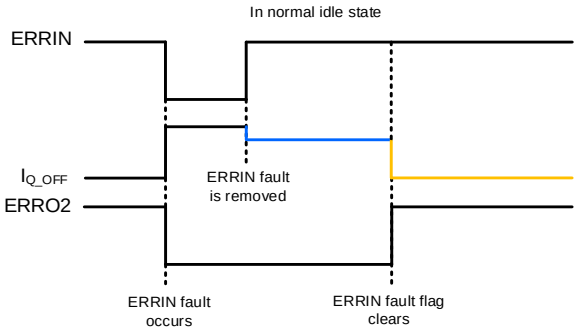


Figure 22: I_{Q_OFF} under an ERRIN Fault

Only normal idle state provides adaptive clock enable control. In other states, the MPQ70700FS cannot disable the clock.

Error Input (ERRIN)

ERRIN is an error input pin for the system error check. ERRIN's valid level is configurable, determined via the ERR_MODE (14h) command, to detect a valid error when ERRIN is pulled high or low. If a valid error signal is sent to ERRIN, then the MPQ70700FS must reset POR and pull down ERROR2. If the ERRIN signal recovers, then ERRO2 does not recover to the high level until the ERRIN fault flag is cleared via the F_ERRIN bit (02h, bit[4]), and POR can recover automatically after the POR delay. Figure 23 show a low valid ERRIN signal as an example.

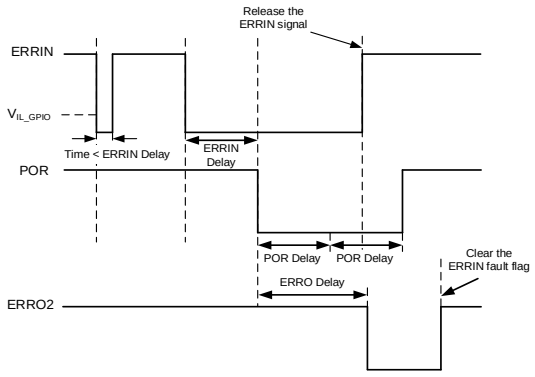


Figure 23: Low Valid ERRIN Signal

If the ERRIN signal low duration is shorter than the ERRIN delay, then the POR pin does not reset and the ERRO2 signal does not pull down. The ERRIN delay can be configurable via the ERR_MODE command.

Error Output (ERRO1 and ERRO2)

ERRO1 and ERRO2 are two error indicator pins. ERRO2 can only be used for reporting a watchdog failure and ERRIN fault. ERRO1 can be used for reporting the other errors. Table 2 shows the device reaction for ERRO1 and ERRO2.

The MPQ70700FS can enable the fault reaction of some check functions via the FAULT_ENABLE_INTERNAL (09h), FAULT_ENABLE_SYS (0Ah), FAULT_ENABLE_CHANNELS1 (0Bh), FAULT_ENABLE_CHANNELS2 (0Ch), FAULT_ENABLE_CHANNELS3 (0Dh), and FAULT_ENABLE_TEST (0Eh) commands. See Table 3 on page 45 for some check functions' fault reaction disabled.

Table 2: Device Reaction with ERRO1 and ERRO2

Error Type	POR	ERRO1	ERRO2	V_{OUTx} and GPIO Output	State Machine	Fault Register Included
$V_{INx} < V_{IN1\_UVLO\_F}$	Low	Hi-Z	Hi-Z	Output off	Off	No
V_{INx} OVP (13)	Low	Low	High	Output off	Fail safe or fail recovery (14)	Yes
OTP single-error correction (SEC) fault (13)	Low	Low	High	Output status does not change	No change	Yes
OTP double-error detection (DED) fault	Low	Low	High	Output status does not change	Fail safe	Yes
Logic built-in self-testing (LBIST) fault	Low	Low	High	Output status does not change	Fail safe	Yes
Analog built-in self-testing (ABIST) fault (13)	Low	Low	High	Output status does not change	Fail safe	Yes
Thermal shutdown (TSD) fault (13)	Low	Low	High	Output off	Fail safe or fail recovery (14)	Yes
Thermal warning (TWN) fault (13)	Low	Low	High	Output off	Fail safe or fail recovery (14)	Yes
Non-LBISTABLE register double-check fault (13)	Low or high (15)	Low	High	Output off or no change (16)	Fail safe or no reaction (14)	Yes
Register write check fault (13)	Low or high (15)	Low	High	Output off or no change (16)	Fail safe or no reaction (14)	Yes
Clock check fault	Low or high (15)	Low	High	Output off or no change (16)	Fail safe or no reaction (14)	Yes

Table 2: Device Reaction with Errors *(continued)*

Error Type	POR	ERRO1	ERRO2	V_{OUTx} and GPIO Outputs	State Machine	Fault Register Included
Bandgap (BG) monitor fault (13)	Low or high (15)	Low	High	Output off or no change (16)	Fail safe or no reaction (14)	Yes
Runtime register CRC fault (13)	Low or high (15)	Low	High	Output off or no change (16)	Fail safe or no reaction (14)	Yes
State machine check fault (13)	Low	Low	High	Output off	PRE_LOAD_ OTP state	Yes
I^2C PEC fault (13)	High	Low	High	No change	No reaction	Yes
Watchdog failure (13)	Low (17)	High	Low	No change	No reaction	Yes
ERRIN fault	Low	High	Low	No change	No reaction	Yes
V_{OUTx} OV fault (13)	Low	Low	High	Output off	Fail safe or fail recovery (14)	Yes
V_{OUTx} UV fault (13)	Low	Low	High	Output off	Fail safe or fail recovery (14)	Yes
V_{OUTx} OC fault (12)	Low	Low	High	Output off	Fail safe or fail recovery (14)	Yes
VMON1/2 OV fault (13)	Low	Low	High	Output off	Fail safe or fail recovery (14)	Yes
VMON1/2 UV fault (13)	Low	Low	High	Output off	Fail safe or fail recovery (14)	Yes

Notes:

13) Enables the fault reaction via the FAULT_ENABLE_INTERNAL (09h), FAULT_ENABLE_SYS (0Ah), FAULT_ENABLE_CHANNELS1 (0Bh), FAULT_ENABLE_CHANNELS2 (0Ch), FAULT_ENABLE_CHANNELS3 (0Dh), and FAULT_ENABLE_TEST (0Eh) commands. The fault reaction is enabled by default.
14) Configures the state machine change via the FAULT_REACTION_GUP1 (0Fh), FAULT_REACTION_GUP2 (10h), FAULT_REACTION_GUP3 (11h), FAULT_REACTION_GUP4 (12h), and FAULT_REACTION_INTERNAL (13h) commands.
15) This option is influenced by the state machine. If the state machine has no reaction, then POR does not change. If the state machine changes to fail safe, then POR goes low.
16) This option is influenced by the state machine. If the state machine has no reaction, then the output does not change. If the state machine changes to fail safe or fail recovery, then the output turns off.
17) Configure the POR pin by pulling it low via the WDT_FAIL_POR bit (4Bh, bit[7]).

Table 3: Device Reaction with Disabled Check Functions

Error Type	POR	ERRO1	ERRO2	V_{OUTx} and GPIO Outputs	State Machine	Fault Register Included
V_{IN} OVP	No change	No change	No change	Output status does not change	No reaction	No
OTP single-error correction (SEC) fault	No change	No change	No change	Output status does not change	No reaction	No
Analog built-in self-testing (ABIST) fault	No change	No change	No change	Output status does not change	No reaction	No
Thermal shutdown (TSD) fault	No change	No change	No change	Output status does not change	No reaction	Yes
Thermal warning (TWN) fault	No change	No change	No change	Output status does not change	No reaction	Yes
Non-LBISTABLE register double-check fault	No change	No change	No change	Output status does not change	No reaction	No
Register write check fault	No change	No change	No change	Output status does not change	No reaction	No
Bandgap (BG) monitor fault	No change	Low	No change	Output status does not change	No reaction	No
Runtime register CRC fault	No change	No change	No change	Output status does not change	No reaction	No

Table 3: Device Reaction with Disabled Check Functions *(continued)*

Error Type	POR	ERRO1	ERRO2	V_{OUTx} and GPIO Outputs	State Machine	Fault Register Included
State machine check fault	No change	No change	No change	Output status does not change	No reaction	No
I²C PEC fault	No change	No change	No change	Output status does not change	No reaction	No
Watchdog failure	No change	No change	No change	Output status does not change	No reaction	No
V_{OUTx} OV fault	No change	No change	No change	Output status does not change	No reaction	No
V_{OUTx} UV fault	No change	No change	No change	Output status does not change	No reaction	No
V_{OUTx} OC fault	No change	No change	No change	Output status does not change	No reaction	No
VMON1/2 OV fault	No change	No change	No change	Output status does not change	No reaction	No
VMON1/2 UV fault	No change	No change	No change	Output status does not change	No reaction	No

Output Discharge

An optional 100Ω discharge resistor is connected between the VOUTx pin (where x = 1 to 5) to GND. If the shutdown signal and discharge are enabled, then the discharge path turns on.

Each LDO can be independently set to enable output discharge and can be configured via the OTP.

Built-In Self-Testing (BIST) and Load Configuration

The MPQ70700FS provides built-in self-testing (BIST) for both critical analog and logic functions. BIST is optionally executed when the device starts up, and can be complied online via the AT_SHDN bit (19h, bit[4]) after power-off sequence monitoring or via the AT_RCOV bits (19h, bits[3:2]) after fail recovery (see Figure 16 on page 41). However, certain safety items are periodically checked while operating, instead of only being checked once during start-up.

The items that are always checked after BIST completes are listed below, unless otherwise noted:

1. I²C protocol packet error checking (PEC): Data transferred through the I²C have an attached packet error checking (PEC) code. The target device rejects data unless the PEC matches the initiator device. PEC is an optional function related to the I2C_PEC_EN bit (52h, bit[0]). For more details, see the Packet Error Checking (PEC) section on page 61.

   If the MPQ70700FS triggers an I²C PEC fault, then the state machine has no reaction, and all channels' outputs are normal. Only ERRO1 is pulled down, and the F_I2C_PEC bit (04h, bit[7]) can record the fault flag.

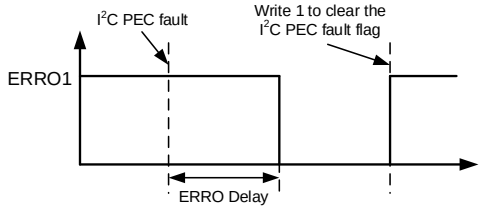


Figure 24: I²C PEC Fault Reaction

2. Thermal warning and shutdown: If the silicon die temperature exceeds the rising threshold (about 130°C), then a thermal warning (TWN) is indicated by asserting the F_TWNx bit (where x = 1 to 3) (04h, bit[4], bit[2], and bit[0]), and reported by ERRO1. Once the temperature drops below the falling threshold (about 115°C), the MPQ70700FS recovers from thermal warning.

   If the silicon die temperature exceeds the high rising threshold (about 172°C), then thermal shutdown (TSD) is also indicated by asserting the F_TSDx bits (where x = 1 to 3) (04h, bit[5], bit[3], and bit[1]), and reported by ERRO1. Once the temperature drops below

the falling threshold (about 157°C), the MPQ70700FS recovers from thermal shutdown.

If the MPQ70700FS detects a TWN or TSD fault, then ERRO1 is pulled down, and all the channels' outputs shut down (see Figure 25).

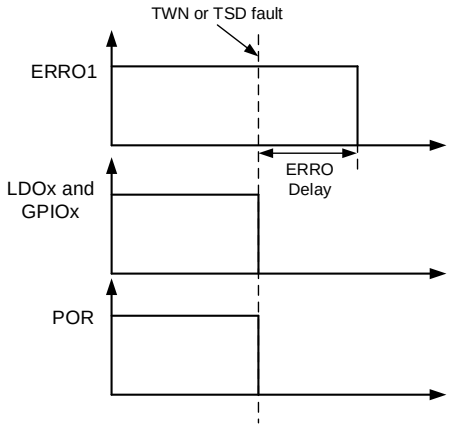


Figure 25: TWN or TSD Fault Reaction

The state machine transition can be configured to enter failsafe or fail-recovery state. If the state machine transitions to failsafe state, then the MPQ70700FS only starts up again by turning V_{INx} on or off. If the state machine transitions to fail-recovery state, then the system starts up again automatically after the fail-recovery delay time ($t_{FAIL\_REC\_DLY}$) ends. $t_{FAIL\_REC\_DLY}$ is configurable via the DLY_RCOV bits (1Ah, bits[5:0]). Once the retry times exceed the upper limit, which is configurable via the RETRY_CFG_RCOV bits (1Ah, bits[7:6]), the MPQ70700FS also enters failsafe state. A TWN or TSD fault can be masked via the FAULT_ENABLE_SYS (0Ah) command.

3. Register runtime cyclic redundancy check (CRC): When there is no data being transferred, CRC continues operating to detect accidental changes to the data.

   If the MPQ70700FS detects an RTCRC check fault, then ERRO1 is pulled down. The state machine can be configured to no action or transition to the failsafe state. If the state machine transitions to failsafe state, then all channels' output shut down, and POR is pulled down. The MPQ70700FS only starts up again by turning V_{INx} on and off. If the state machine does not change, then all the channels' outputs and POR remain unchanged. An RTCRC check fault can be masked via the F_EN_RTCRC_AUX bit (09h, bit[5]) and F_EN_RTCRC bit (09h, bit[0]).

   Figure 26 shows the RTCRC fault reaction.

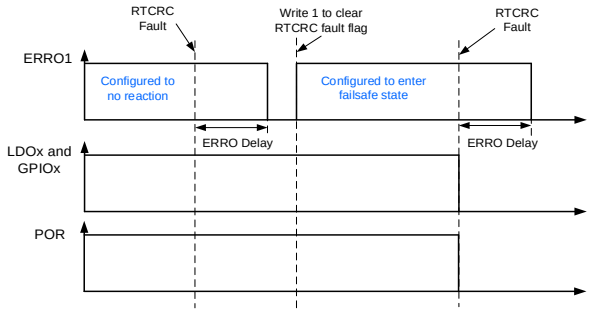


Figure 26: RTCRC Fault Reaction

4. State machine error monitoring: The state machine sequence is checked using one-hot coding, including the system state and several functional states.

   If the system detects a state machine fault, then the MPQ70700FS resets and starts up the pre-loaded OTP again. Meanwhile, all the channels' outputs shut down, and ERRO1 is pulled down. State machine faults can be masked via the F_EN_STATE bit (09h, bit[4]).

   Figure 27 shows the state machine reaction.

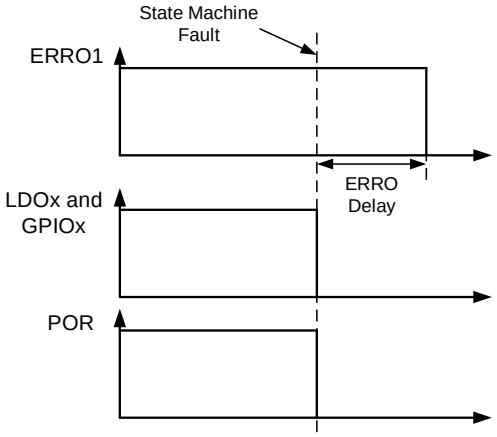


Figure 27: State Machine Reaction

5. Register write check: The I²C write register map provides an automatic readback check. If the MPQ70700FS detects a register write check fault, then ERRO1 is pulled down. The state machine can be configured to no action or transition to failsafe state.

If the state machine transitions to failsafe state, then all the channels' outputs shut down ,and POR is pulled down. The MPQ70700FS only starts up again by turning V_{INx} on or off. If the state machine does not change, then all the channels' outputs and POR remain unchanged. The register write check fault can be masked via the F_EN_REG_WR_CHK bit (09h, bit[2]).

Figure 28 shows the register write check fault reaction.

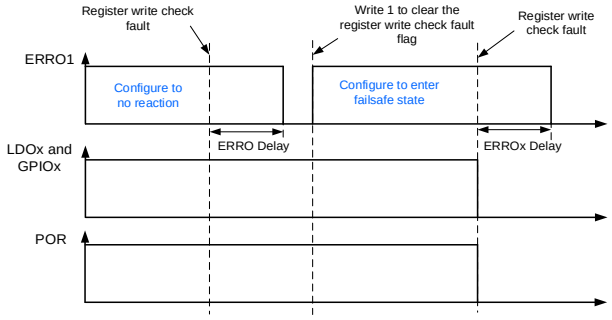


Figure 28: Register Write Check Fault Reaction

6. Clock monitor: In addition to system clock detection, the MPQ70700FS implements two digital clocks (CLK1 and CLK2). CLK1 is the system clock, and CLK2 is the reference clock.

   CLK1 or CLK2 can start counting at the same time. When the CLK1 or CLK2 counter reaches 100, the count number must be checked in another clock. This ensures cross-checking between the system clock and reference clock.

   If the MPQ70700FS detects a clock fault, then ERRO1 is pulled down. The state machine can be configured to no action or transition to failsafe state. If the state machine transitions to failsafe state, then all the channels' outputs shut down, and POR is pulled down. The MPQ70700FS only starts up again by turning V_{INx} on and off. If the state machine does not change, then all the channels' outputs and POR remain unchanged.

   Figure 29 shows the clock fault reaction.

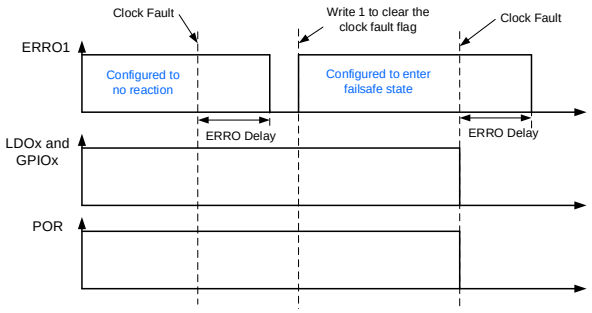


Figure 29: Clock Fault Reaction

7. Non-LBIST volatile memory (NBVM) check: The MPQ70700FS prepares two sets of registers that are not monitored by LBIST check. The two groups are cross-checked to ensure that the non-LBISTABLE register is normal.

   If the MPQ70700FS detects an NBVM check fault, then ERRO1 is pulled down. The state machine can be configured to no action or transition to failsafe state. If the state machine transitions to failsafe state, then all the channels' outputs shut down, and POR is pulled down. The MPQ70700FS only starts up again by turning V_{INx} on and off. If the state machine does not change, then all the channels' outputs and POR remain unchanged.

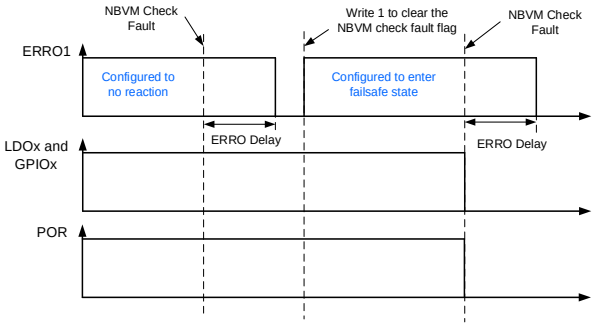


Figure 30: NBVM Check Fault Reaction

8. Bandgap (BG) monitor: There are two internal bandgap voltages: the LDO bandgap voltage (V_{BG_LDO}) and the POR bandgap voltage (V_{BG_PRO}), which are both equal to 1.2V. V_{BG_LDO} generates V_{REF} in the power stage and monitors the block. V_{BG_POR} generates V_{REF} in the internal LDO (3.1V). These two bandgap voltages cross-check each other in the MPQ70700FS.

If V_{INx} exceeds $V_{INx\_UVLO\_R}$, then the digital block resets, and the bandgap monitor starts operating. The BG fault can be only reported while waiting for BIST to complete.

If the difference between V_{BG_POR} and V_{BG_LDO} exceeds a certain threshold, then the BG fault is reported. If the MPQ70700FS detects a BG fault, then ERRO1 is pulled down. The state machine can be configured to no action or transition to failsafe state. If the state machine transitions to failsafe state, then all the channels' outputs shut down, and POR is pulled down. The MPQ70700FS only starts up again by turning V_{INx} on or off. If the state machine does not change, then all the channels' outputs and POR remain unchanged.

Figure 31 shows the BG fault reaction.

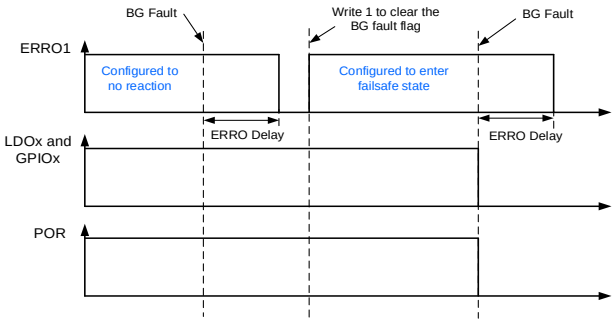


Figure 31: BG Fault Reaction

The items checked during start-up are listed below:

1. Non-volatile memory (NVM) error correction code (ECC): While loading the configuration from the NVM, every 32 bytes of data are attached with 7 ECC bits to protect against data integrity issues and maximize system availability. For 1-bit errors, single errors can be corrected using single-error correction (SEC), but double errors can only be detected using double-error detection (DED). The MPQ70700FS applies ECC again after BIST since all registers are reset during BIST.
2. Single-error correction (SEC): If SEC occurs, then the fault is reported in the F_OTP_SEC bit (08h, bit[3]), ERRO1 is pulled down, and the information is recorded to the FAULT_TEST (08h) command. Faults in the FAULT_TEST command can be written to 1 to be cleared. Before clearing the fault, the host can read the error status from the FAULT_TEST command and respond.
3. Double-error detection (DED): If DED occurs, then the fault is reported in the F_OTP_DED bit (08h, bit[2]), the information is recorded in the FAULT_TEST command, and ERRO1 is pulled down. The MPQ70700FS enters failsafe state. The F_OTP_DED bit cannot be written to 1 to clear the fault flag.
4. Analog built-in self-testing (ABIST): ABIST typically involves exercising diagnostic circuits into and out of fault scenarios by injecting currents or voltages into the diagnostic circuit. This ensures that the diagnostic circuit can switch to both fault and non-fault states. The analog circuit is controlled by a digital circuit that verifies the correct functionality of the analog safety mechanisms.

   During this process, the LDO output OV/UV/OC comparators, external monitor OV/UV comparators, bandgap monitor comparators, and thermal monitor comparators are checked. If an error is detected in ABIST, then ERRO1 is pulled down, and the error is reported in the F_BIST_A bit (08h, bit[1]). The information is recorded in the FAULT_TEST command. The F_BIST_A bit can be written to 1 to be cleared.
5. Logic built-in self-testing (LBIST): The MPQ70700FS's logic circuits are checked during LBIST. If an error is detected in LBIST, then ERRO1 is pulled down, and the error is reported in the F_BIST_L bit (08h, bit[0]). The information is recorded in the FAULT_TEST command. The F_BIST_L bit cannot be written to 1 to be cleared, meaning ERRO1 remains latched.

WATCHDOG OPERATION

The watchdog (WD) monitors the software execution of an external microcontroller. It can reset the MPQ70700FS's POR pin via the WDT_FAIL_POR bit (4Bh, bit[7]) if the microcontroller stops serving the watchdog due to a lock-up in the software from the watchdog fault count reaching its limit.

There are two different watchdog configurations in the MPQ70700FS: window watchdog and Q&A watchdog. These configurations can be selected via the WDT_MODE bit (4Bh, bit[6]).

Watchdog operation occurs in two steps, described below:

1. Detect whether the POR pin is pulled high. If the MPQ70700FS detects the POR pin is pulled high, then the watchdog begins counting the delay time. The watchdog delay time is t_{WDT_DLY}, and is determined using the WDTDLY bit (4Bh, bits[2:0]), as well as the closed and open window times. t_{WDT_DLY} is typically used for the microcontroller loads' code.
2. After t_{WDT_DLY} ends, the watchdog starts the first watchdog sequence and the counter's closed window time. At this point, the watchdog starts to work properly, and the microcontroller must provide the correct feeding signal to the MPQ70700FS.

Window Watchdog Operation

The window watchdog is the default operating configuration of the MPQ70700FS's watchdog.

Figure 32 and Figure 33 on page 51 show the window watchdog timing diagrams that define watchdog refreshment.

The microcontroller that is being monitored must write a different value to the WDTKEY (50h) command within the open window via the I^2C, which is called a good WD refreshment. Figure 32 on page 51 shows an example of good WD refreshments. The microcontroller reads the WDT_KEY bits (50h, bits[7:0]) before writing these bits. This ensures that the written value is different from the previously read value; this is also called a write update.

If a write update is sent during the closed window, which is called a bad WD refreshment, then the watchdog fault counter increases by 1. This signals that a potential microcontroller fault has occurred.

If a write update is not sent, which is called a WD timeout, then the WDT_EXPIRE bit (56h, bit[0]) is set to 1, and the watchdog fault counter increases by 1. During a watchdog sequence, the value written to the WDT_KEY bits is always the same as the previous value; otherwise, no write command is sent to the WDT_KEY bits, which is considered a WD timeout. Figure 33 on page 51 shows an example of bad WD refreshments and WD timeout, where the watchdog fault count limit is set to 4.

A good WD refreshment, bad WD refreshment, or WD timeout immediately result in starting a new window watchdog sequence using a new closed window, followed by an open window.

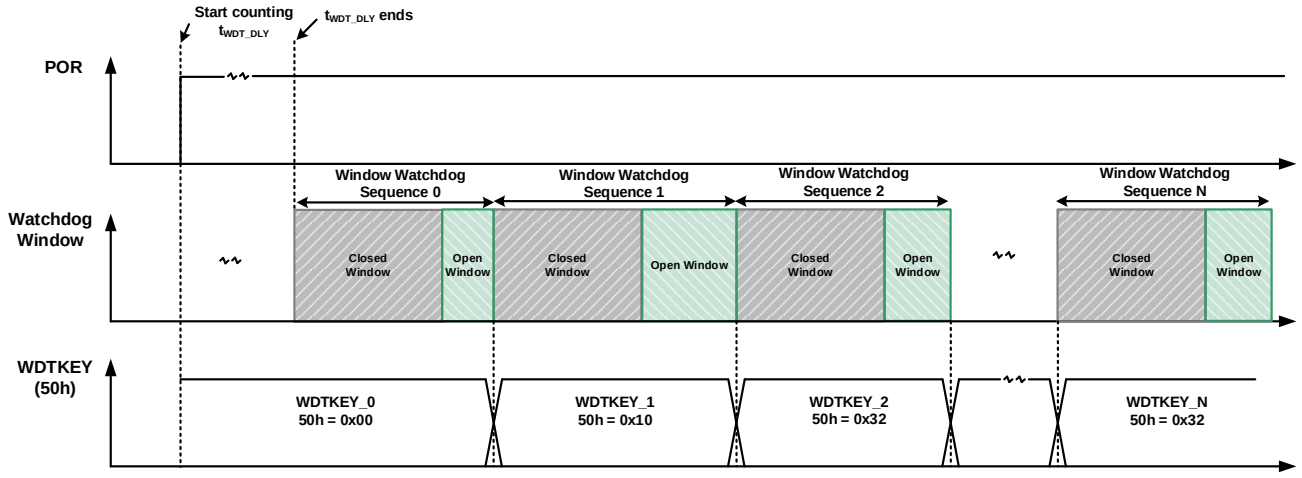


Figure 32: Timing Diagram of the Window Watchdog (Good WD Refreshments) (18)

Note:

18) WDTKEY_N is separate from WDTKEY_N - 1 (where N > 0).

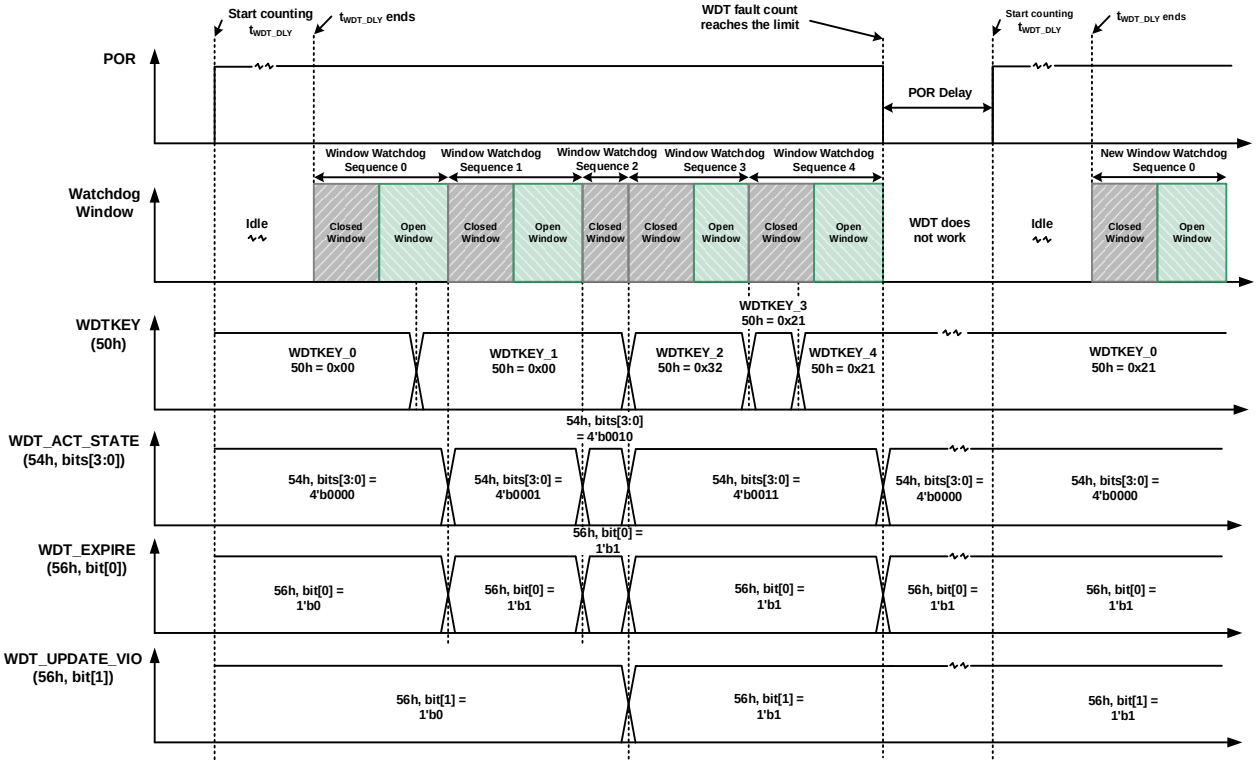


Figure 33: Timing Diagram of Window Watchdog (Bad WD Refreshments and WD Timeout)

Q&A Watchdog Operation

The Q&A watchdog is another operation that monitors the microcontroller. Setting the WDT_MODE bit (4Bh, bit[6]) to 1 configures the watchdog for the Q&A watchdog.

In the Q&A watchdog, the device provides a question (TOKEN) for the microcontroller via the WDT_TOKEN bits (55h, bits[7:3]). The microcontroller performs a fixed series of arithmetic operations on the question to calculate the required 32-bit answer. This answer is split into 4 answer bytes. The microcontroller writes these answer bytes via the I²C, 1 byte at a time, into the WDTKEY command

The device verifies that the microcontroller returns the answer bytes within the specified timing windows, and that the answer bytes are correct. A new question is generated only if a good WD refreshment occurred in the previous Q&A watchdog sequence, causing the token counter (internal counter) to increment and generate a new question.

The microcontroller sends the correct answer bytes calculated for the current question within the correct Q&A watchdog window and in the correct order, which is called a good WD refreshment. Then the watchdog error counter set via the WDT_ACT_STATE bits (54h, bits[3:0]) has no change, and the internal token counter increases by 1, causing a new question to be generated.

An event is considered a bad WD refreshment if the microcontroller sends the following situations:

- The answer bytes are correct and in order, but the last answer is not in the open watchdog window
- Incorrectly calculated answer bytes
- The correct answer bytes in the wrong order

If the MPQ70700FS detects a bad WD refreshment, then the watchdog error counter set via the WDT_ACT_STATE bits increases by 1 or 2, signaling a potential microcontroller fault has occurred. The internal token counter does not change. As a result, the question does not change. The WDT_STATUS2 (55h) and WDT_STATUS3 (56h) commands record which type of watchdog fault occurs.

If the microcontroller stops sending answer bytes because the MPQ70700FS does not receive four answers, which is called a WD timeout, then the WDT_EXPIRE bit is set, and the watchdog error counter set via the WDT_ACT_STATE bits increases by 1.

In addition, there is a specific watchdog refreshment, where the last answer is correct and sent in the open window, but the first three answers are not correct. The fault counter does not change, and the new watchdog question is not generated in the next watchdog sequence. The WDT_TOKEN_ERR_SRC bit (55h, bit[1]) is set to 1.

Table 4 shows that different Q&A watchdog refreshments cause varying results.

Table 4: Q&A Watchdog Refreshment

Watchdog Answer		Action	WDT_STATUS2 (55h) and WDT_STATUS3 (56h)				Comments
Closed Window	Open Window		WDT_ANS0_ERR_SR (55h, bit[2])	WDT_TOKEN_ERR_SRC (55h, bit[1])	WDT_UPDATE_VIO (56h, bit[1])	WDT_EXPIRE (56h, bit[0])	
4 correct answers	N/A	1. A new WD sequence starts after the 4th WD answer 2. WDT fault counter + 1 3. A new WD sequence starts with the same WD question	0	0	1	0	4 WD answers in the closed window
3 correct or incorrect answers + 1 incorrect answer	N/A	1. A new WD sequence after the 4th WD answer 2. WDT fault counter + 2 3. A new WD sequence starts with the same WD question	1	1	1		
3 correct or incorrect answers	1 incorrect answer	1. A new WD sequence starts after the 4th WD answer 2. WDT fault counter + 1 3. A new WD sequence starts with the same WD question	1	1	0	0	Incorrect 4th WD answer in the open window
N/A	3 correct or incorrect answers + 1 incorrect answer		1	1	0	0	

Table 4: Q&A Watchdog Refreshment *(continued)*

Watchdog Answer		Action	WDT_STATUS2 (55h) and WDT_STATUS3 (56h)				Comments
Closed Window	Open Window		WDT_ANS0_ ERR_SR (55h, bit[2])	WDT_ TOKEN_ ERR_SRC (55h, bit[1])	WDT_ UPDATE_ VIO (56h, bit[1])	WDT_ EXPIRE (56h, bit[0])	
3 correct answers	1 correct answer	1. A new WD sequence starts after the 4th WD answer 2. The WDT fault counter remains at the same value 3. A new WD sequence starts with a new WD question	0	0	0	0	4 correct WD answers, and correct 4th WD answer in the open window. The first three answers must be sent in the correct order in this WD sequence (either in the closed window or open window)
N/A	4 correct answers		0	0	0	0	
3 incorrect answers	1 correct answer	1. A new WD sequence starts after the 4th WD answer 2. The WDT fault counter remains at the same value 3. A new WD sequence starts with the same WD question	0	1	0	0	Correct 4th WD answer in the open window. One or more of the first 3 answers is wrong in this WD sequence (either in the closed window or open window)
N/A	3 incorrect answers + 1 correct answer		0	1	0	0	
N/A	N/A	1. A new WD sequence starts after the open window ends 2. WDT fault counter + 1 3. A new WD sequence starts with the same WD question	0	0/1	0	1	Less than 4 WD answers in a WD sequence. If the watchdog answers sent are all correct, then the WDT_TOKEN_ERR_SRC bit is set to 0. Otherwise, the WDT_TOKEN_ERR_SRC bit is set to 1
3 correct or incorrect answers	N/A		0	0/1	0	1	
N/A	3 correct or incorrect answers		0	0/1	0	1	

A good WD refreshment, bad WD refreshment, or WD timeout immediately results in starting a new Q&A watchdog sequence.

The Q&A watchdog is performed step-by-step as described below:

1. Set the adjustable closed and open window time. The microcontroller can change the closed and open window time via the WDT_CLOSE (4Ch) or WDT_OPEN (4Dh) commands. If the microcontroller sends a write command to the WDT_CLOSE or WDT_OPEN command, then the MPQ70700FS records the action using the WDT_CFG_CHG_SRC bit (55h, bit[0]). After the MPQ70700FS receives the write command, the watchdog window is refreshed to the close window and starts a watchdog sequence. If the one-time programmable (OTP) value is the expected closed or open window time, then this step can be ignored.
2. Set the WDT_MODE bit to the Q&A watchdog. Watchdog mode must be configured before enabling the watchdog function. If watchdog mode is changed during watchdog operation, then the microcontroller must reconfigure the closed and open window time after changing watchdog mode. If the OTP value is the expected watchdog mode, then this step can be ignored.
3. Set the WDT_EN bits (4Bh, bits[5:4]) to enable the watchdog as well as to set the watchdog fault limit. If the watchdog status is enabled via the I²C, then the MPQ70700FS starts counting t_{WDT_DLY} after POR is pulled high. Once t_{WDT_DLY} ends, the first watchdog sequence starts. In every watchdog sequence, the closed window is timed first. The microcontroller must read the WDT_STATUS1 (54h), WDT_STATUS2 (55h), and WDT_STATUS3 (56) command to obtain the watchdog fault status and count. If the watchdog fault counter is equal to the watchdog fault limit, then the MPQ70700FS reports the watchdog failure. The POR and ERRO2 pins are pulled down, and can be configured via the WDT_FAIL_POR bit (4Bh, bit[7]) and

F_EN_REG_WD bit (0Ah, bit[2]), respectively. If the OTP value is the expected watchdog status and fault limit, then this step can be ignored.

4. The microcontroller reads the question (via the WDT_TOKEN bits) from the WDT_STATUS2 (55h) command. A 5-bit seed in WDT_SEED (4Eh, bits[4:0]) (either stored in the MPQ70700FS or from the microcontroller) is applied to a linear feedback shift register (LFSR) inside the MPQ70700FS to generate a 5-bit question (via the WDT_TOKEN bits). In every watchdog sequence, the closed window is timed first. At the beginning of each watchdog sequence, the question is read first. Within a watchdog sequence, the watchdog question can only be read once. If the microcontroller reads the question again in the process of replying to the answers, then the answer count is refreshed to the default value.
5. The microcontroller reads the answer count via the WDT_ANSW_CNT bits (54h, bits[7:6]). According to the answer count order of 2'b11, 2'b10, 2b'01, and 2'b00, these answers are called Answer-3, Answer-2, Answer-1, and Answer-0. The default value is 2'b11 to indicate that the MPQ70700FS expects the microcontroller to send Answer-3 via the WDT_KEY bits. When the MPQ70700FS receives an answer in a watchdog sequence, the WDT_ANSW_CNT bits are decreased by 1. The WDT_ANSW_CNT bits always change in the order of 2'b11, 2'b10, 2'b01, and 2'b00. If the microcontroller reads the question again in the process of replying to the answers, then the answer count is refreshed to the default value.
6. In a watchdog sequence, the microcontroller must perform a pre-defined calculation formula (see Figure 34 on page 55) to calculate the corresponding 8-bit answer based on the watchdog question and answer count. These answers are only applicable to this particular watchdog sequence. According to the answer count order of 2'b11, 2'b10, 2b'01, and 2'b00, these answers are called Answer-3, Answer-2, Answer-1, and Answer-0.
7. The microcontroller must send these answers to the WDT_KEY bits one by one. If the MPQ70700FS does not receive four answers in a watchdog sequence, then the MPQ70700FS reports a timeout error at the end of the open window.
8. The answer sent by the microcontroller is verified by the MPQ70700FS. For each question, the MPQ70700FS requires 4 correct answer bytes from the microcontroller in the correct order, and Answer-0 in the open window. Answer-3, Answer-2, and Answer-1 may be in the closed window or open window in the correct order, and Answer-0 must be in the open window to be detected as a good WD refreshment.
9. The new Q&A watchdog sequence results from a good WD refreshment, bad WD refreshment, or a timeout error. Only a good WD refreshment can make the MPQ70165FS generate a new question for the microcontroller. If a bad WD refreshment or WD timeout occurs, then a new question is not generated. Once the new Q&A watchdog sequence is generated, the microcontroller reads the WDT_STATUS1, WDT_STATUS2, and WDT_STATUS3 commands to obtain the watchdog fault status and count.

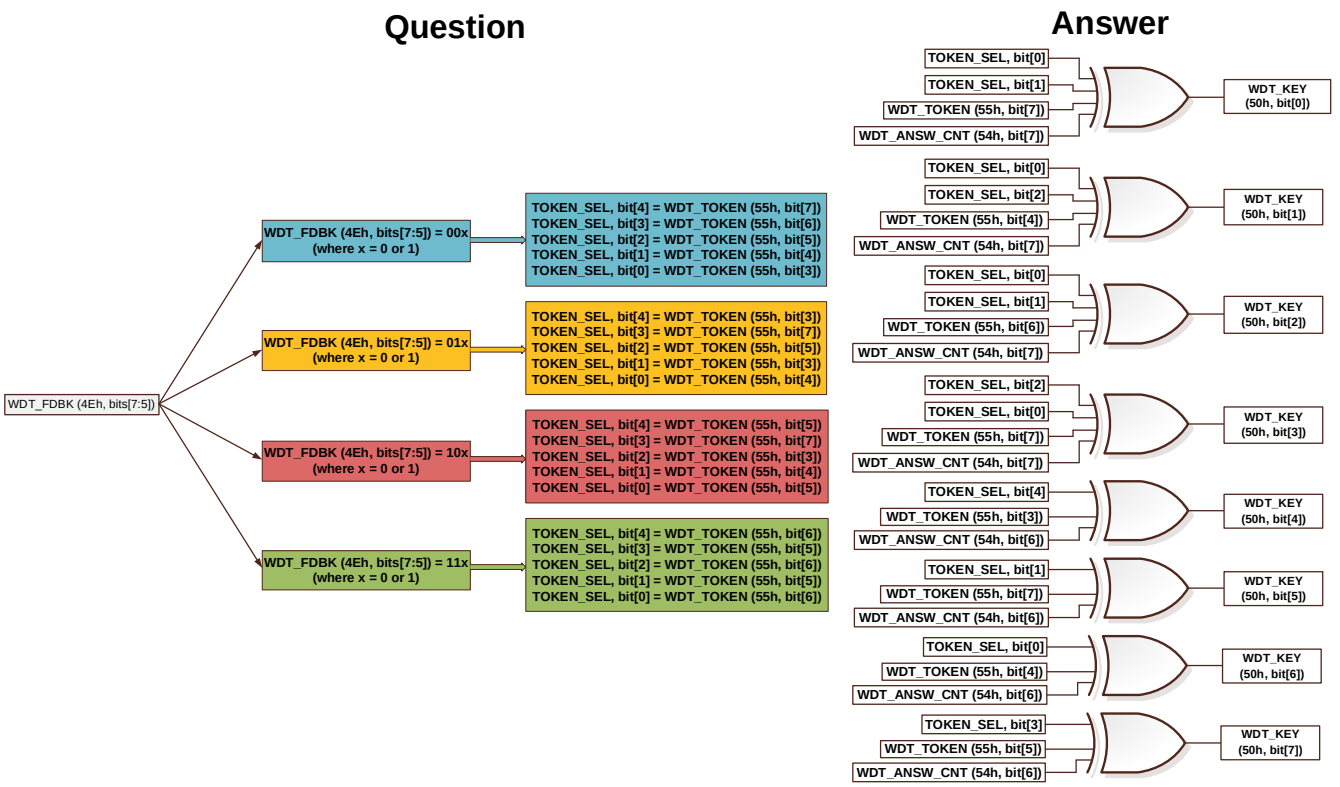


Figure 34: Question and Answer Generation for Q&A Mode

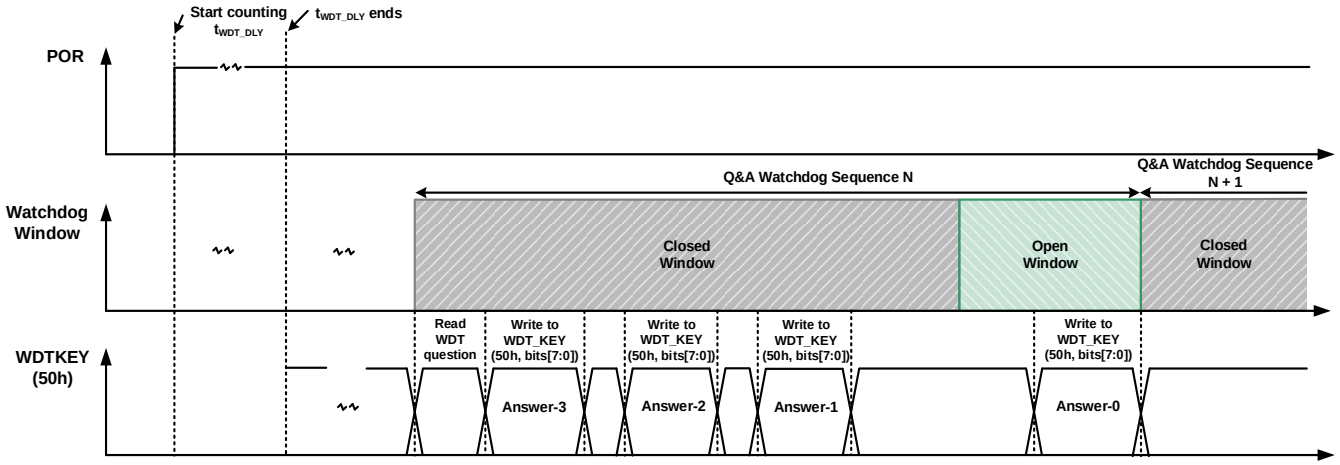


Figure 35: Timing Diagram of Q&A Watchdog WD Refreshments

Watchdog Error Counter and Watchdog Fail Flag

The MPQ70700FS provides a watchdog error counter via the WDT_ACT_STATE bits, which increases or maintains the value after every watchdog refreshment.

The watchdog error counter ranges between 0 and 8, and it is initialized to 0 after the power-on reset (POR). A good WD refreshment maintains the value in the WDT_ACT_STATE bits. A bad WD refreshment and WD timeout increase the WDT_ACT_STATE bits by 1, up to the maximum of 8. Once the watchdog error counter reaches the watchdog failure limit in the WDT_CFG (4Bh) command, the WDT_ACT_STATE bits are reset to 0 immediately. The microcontroller does not read that the WDT_ACT_STATE are equal to 8.

If a watchdog fail event occurs, the watchdog fail flag set via the F_WD bit (04h, bit[6]) is set to 1, and the POR and ERRO2 pins are pulled down

via the WDT_FAIL_POR bit and F_EN_REG_WD, respectively.

Watchdog Sequence

One window watchdog sequence in the MPQ70700FS consists of a closed window, followed by an open window. Both the window and Q&A watchdog configurations share the same watchdog sequence settings.

The watchdog window sequence is derived from the values in the WDT_OPEN_WIN bits (4Dh, bits[7:0]) and WDT_CLOSE_WIN bits (4Ch, bits[7:0]). The microcontroller unit (MCU) can configure the time period of the closed window (t_{WD_CLOSE}) and open window (t_{WD_OPEN}) by writing to the WDT_OPEN_WIN and WDT_CLOSE_WIN bits. The watchdog uses the MPQ70700FS's internal system clock as a time reference and tolerates ±10% deviances of the internal oscillator. The microcontroller must allow a reasonable timing margin during configuration.

Watchdog Synchronization

When the POR pin is released, the external microcontroller should have been powered up properly and started its own initialization. The watchdog starts to operate after t_{WDT_DLY} ends, where t_{WDT_DLY} can be configured via the WDTDLY bits (4Bh, bits[2:0]).

To synchronize the microcontroller timer with the watchdog timer, the microcontroller can write to the WDT_OPEN (4Dh) and WDT_CLOSE (4Ch) commands to start a new watchdog sequence. After a write access is sent to the WDT_OPEN (4Dh) command or WDT_CLOSE (4Ch) command by the microcontroller, the WDT_CFG_CHG_SRC bit is set to 1. The device immediately starts a new watchdog sequence. Therefore, the write access only takes effect in this new watchdog sequence.

When the microcontroller timer is synchronized with the watchdog timer, the MPQ70700FS requires a clear fault action to de-assert ERRO2 using the microcontroller. To clear the fault, write 1 to the WDT_FAULT_CLR bit (4Fh, bit[1]). Then the WDT_FAULT_CLR bit must be written to 0; otherwise, the watchdog fault count remains at 0. A good WD refreshment from the microcontroller immediately starts a new watchdog sequence. In this way, the microcontroller remains synchronized with the watchdog sequence.

Contact an MPS FAE for the full safety-related instructions.

STATE MACHINE

The state machine describes the different states of operation (see Figure 36). There are 5 stable states and 11 transient states in the device. The stable states include off, normal idle, active, sleep, and failsafe. The transient states include pre-loaded one-time programmable (OTP) memory, BIST after preloaded OTP passes set via the AT_POR bits (19h, bits[1:0]), built-in self-testing (BIST), reloaded OTP, normal, power on, sleep mode entry, sleep mode exit, power off, fail recovery, and BIST after the fail-recovery delay time ends set via the AT_RCOV (19h, bits[3:2]).

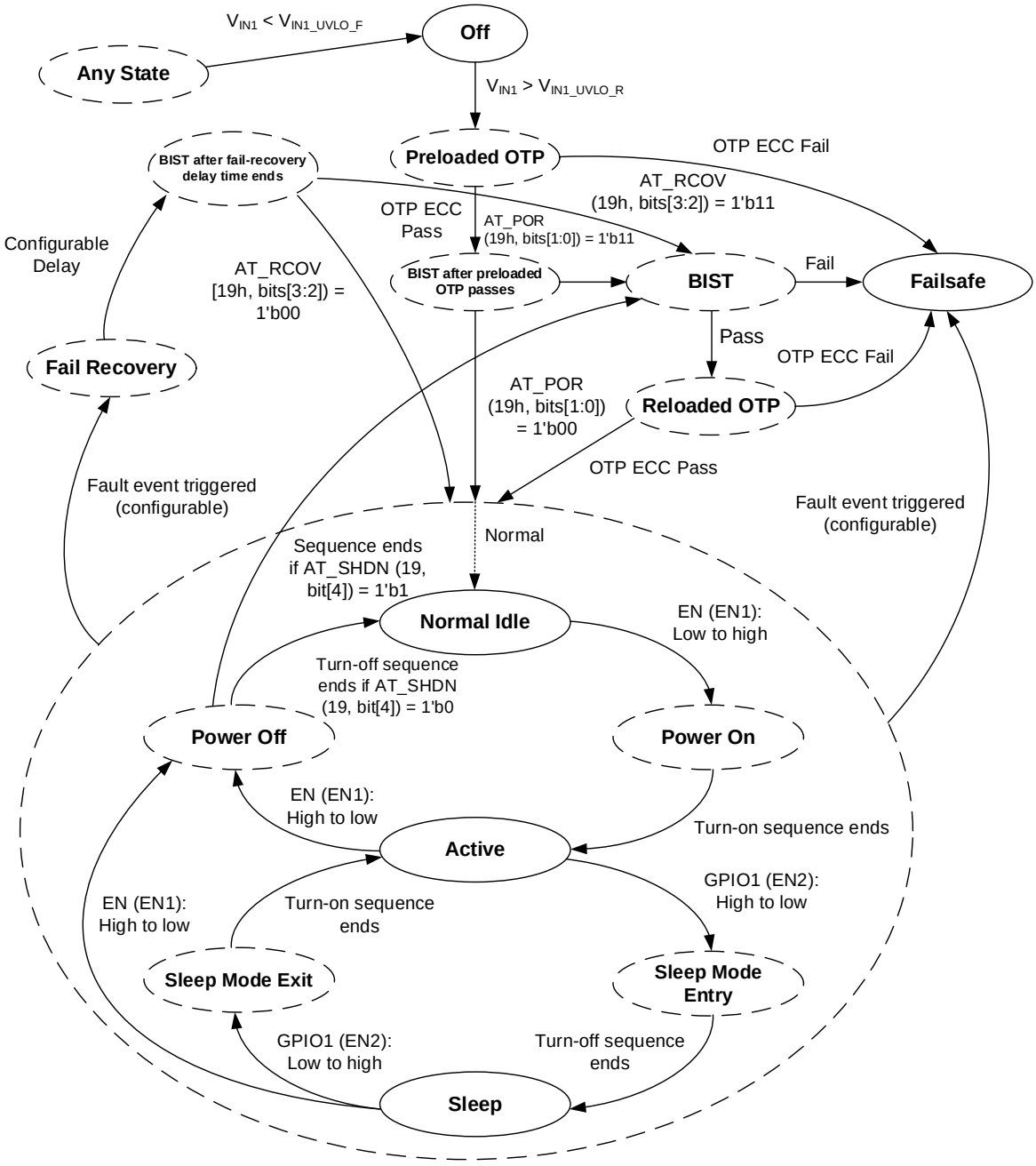


Figure 36: Operation State Diagram

Off

If the LDO1 and internal circuit supply input voltage (V_{IN1}) drops below its under-voltage lockout (UVLO) falling threshold ($V_{IN1\_UVLO\_F}$), then MPQ70700FS turns off. While the MPQ70700FS is in the off state, the I²C interface is disabled.

If V_{IN1} exceeds its UVLO rising threshold ($V_{IN1\_UVLO\_R}$), then the digital block is reset, and the MPQ70700FS enters the preloaded OTP state.

Preloaded One-Time Programmable (OTP) Memory

While the MPQ70700FS is in the preloaded OTP state, the device preloads the OTP configurations and sends the OTP error correction code (ECC).

In preloaded OTP, the I²C interface is disabled. If OTP ECC fails (a double error detected), then the MPQ70700FS enters failsafe state. If single-error correction (SEC) occurs, then the fault can only be reported via the ERRO1 pin, and OTP ECC passes.

If OTP ECC passes, then the MPQ70700FS enters normal state when the AT_POR bits (19h, bits[1:0]) are set to 0. This means that the device does not need to run BIST when it resets. When the AT_POR bits are set to 1, the device enters BIST state, which means that analog built-in self-testing (ABIST) and logic built-in self-testing (LBIST) run.

Built-In Self-Testing (BIST)

While the MPQ70700FS is in BIST state, the I²C interface is disabled, and runs ABIST and LBIST, which are described below:

1. Analog built-in self-testing (ABIST): The aim of ABIST is to verify the correct function of the diagnostic circuits (e.g. voltage supervisor) and to increase the detection of latent faults.

   ABIST typically involves exercising diagnostic circuits into and out of fault scenarios by injecting currents or voltages into the diagnostic circuit to ensure that the diagnostic circuit (e.g. under-voltage and over-voltage monitoring, and the thermal protection circuits) can switch to both faulted and non-faulted states.

2. Logic built-in self-testing (LBIST): The aim of LBIST is a no-bit error for the register and combinational/sequential logic blocks.

   Test vectors are applied to the digital core to verify the correct functionality.

The MPQ70700FS enters reloaded OTP state after BIST pass, then enters failsafe state after BIST fails. Afterwards, the related faults are reported.

Reloaded One-Time Programmable (OTP) Memory

While the MPQ70700FS is in reloaded OTP, it reloads the OTP configurations and sends the OTP ECC.

The MPQ70700FS enters normal state when the OTP ECC passes; the device enters failsafe state if the OTP ECC fails. Afterwards, the related faults are reported.

Normal

While the MPQ70700FS is in normal state, the I²C interface is available. If a thermal shutdown (TSD) or thermal warning (TWN) fault event is triggered in normal state, then the MPQ70700FS can be configured to enter failsafe state or fail-recovery state via the FAULT_REACTION_GUP1 (0Fh) command.

The device returns to the off state if the input voltage (V_{INx}) is below its UVLO falling threshold ($V_{INx\_UVLO\_F}$). If no fault occurs in normal state, then the device enters normal idle state.

Normal Idle

While the MPQ70700FS is in normal idle state, the I²C interface is available. The device waits for the EN (EN1) voltage (V_{EN}) to exceed its rising threshold ($V_{IH\_EN\_R}$). The MPQ70700FS enters the power-on state after V_{EN} exceeds $V_{IH\_EN\_R}$.

Power On

While the MPQ70700FS is in power-on state, the I²C interface is available. All the LDO and GPIO outputs enter the power-on sequence.

If no other faults occur, then the MPQ70700FS enters active state once the turn-on sequence ends.

Active

While the MPQ70700FS is in active state, the I²C interface is available. If V_{EN} drops below its falling threshold ($V_{IL\_EN\_F}$) in active state, then the MPQ70700FS enters power-off state.

If GPIO1 is configured as an input pin in active state, then the GPIO1 input voltage (V_{GPIO1}) drops below its input high threshold (V_{IH_GPIO1}), and the MPQ70700FS enters sleep mode entry state.

Power Off

While the MPQ70700FS is in power-off state, the I²C interface is available. All LDO and GPIO outputs shut down according to the turn-off sequence. The MPQ70700FS returns to normal idle state once the power-down sequence ends.

Sleep Mode Entry

During sleep mode entry, the I²C interface is available. These outputs are controlled by GPIO1 (EN2), which shuts down according to the turn-off sequence. The MPQ70700FS enters sleep state once the turn-off sequence ends.

Sleep Mode

While the MPQ70700FS is in sleep mode, the I²C interface is available and shuts down the outputs that are controlled by GPIO1 (EN2). The EN2_GROUP (17h) command configures which channels can be controlled by GPIO1 (EN2).

If GPIO1 (EN2) goes high in sleep mode, then the MPQ70700FS enters sleep mode exit state.

If EN (EN1) goes low in sleep mode, then the MPQ70700FS enters power-off state.

Sleep Mode Exit

During sleep mode exit, the I²C interface is available. These outputs are controlled by GPIO1 (EN2), which starts up according to the turn-on sequence. The MPQ70700FS enters active state once the turn-on sequence ends.

Failsafe

While the MPQ70700FS is in failsafe state, the I²C interface is available. The I²C disables the output and waits for a new power cycle.

If any of the faults listed below occurs, then the MPQ70700FS enters failsafe state. There are no LDO outputs, and the part does not restart until VINx (where x = 1 to 3) cycle resets. Once VINx resets, the MPQ70700FS is configurable to run BIST again via the AT_POR bits. If the AT_POR bits are set to 1, then the device runs BIST again.

If any of the below configurable faults occur, then the MPQ70700FS reports the fault and enters failsafe state:

- Input over-voltage (OV) fault
- Thermal shutdown or thermal warning
- Output OV or under-voltage (UV) fault
- Output over-current (OC) fault
- Voltage monitor OV or UV fault
- Bandgap fault
- Clock monitor fault
- Register cyclic redundancy check (CRC) fault
- Register write check fault
- Non-LBISTABLE register double-check fault

If any of the below non-configurable faults occur, then the MPQ70700FS reports the fault and enters failsafe state:

- OTP ECC
- ABIST or LBIST

Fail Recovery

While the MPQ70700FS is in fail-recovery state, the I²C interface is available and enters recovery operation with a configuration delay time. After the delay time completes, if the AT_RCOV bit is set to 0, then the MPQ70700FS enters normal state; if AT_RCOV is set to 1, then the MPQ70700FS enters BIST state.

If any of the below faults occurs, then the MPQ70700FS reports the fault and can be configured to enter fail-recovery state:

- Input OV fault
- Thermal shutdown or thermal warning
- Output OV or UV fault
- Output OC fault
- Voltage monitor OV or UV fault

I²C INTERFACE

I²C Serial Interface Description

The I²C bus is a two-wire, bidirectional serial interface, consisting of a serial data line (SDA) and a serial clock line (SCL). The lines are externally pulled to a bus voltage (V_{BUS}) when they are idle. When connected to the line, an initiator device generates the SCL signal and device address, then arranges the communication sequence. The MPQ70700FS works as a target-only device, which supports up to 1Mbs of bidirectional data transfer in fast-mode plus, adding flexibility to the sequencer. Device parameters can be instantaneously controlled via the I²C interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on SDA must be stable during the clock's high period. The SDA line's high or low state only changes when the clock signal on the SCL line is low (see Figure 37).

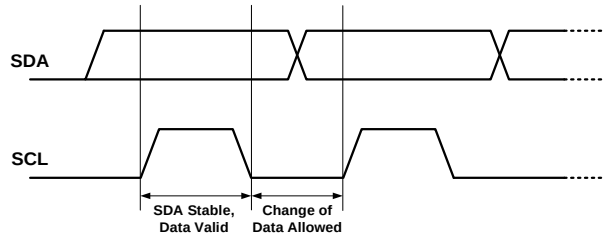


Figure 37: Bit Transfer on the I²C Bus

Start and Stop Commands

Start (S) and stop (P) commands are signaled by the initiator device, which signifies the beginning and the end of the I²C transfer. A start command is defined as the SDA signal transitioning from high to low while SCL is high. A stop command is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 38).

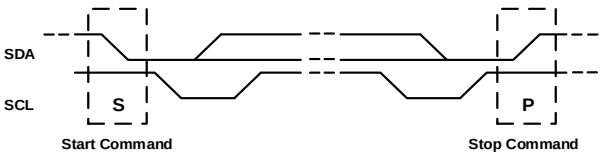


Figure 38: Start and Stop Commands

Start and stop commands are always generated by the initiator. The bus is considered busy after a start command. The bus is considered free again after a delay following a stop command.

The bus remains busy if a repeated start (Sr) command is generated instead of a stop command. Start and repeated start commands are functionally identical.

Data Transfer

Every byte placed on SDA must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the initiator. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, allowing it to remain stable (low) during the clock pulse's high period.

Figure 39 shows the data transfer format.

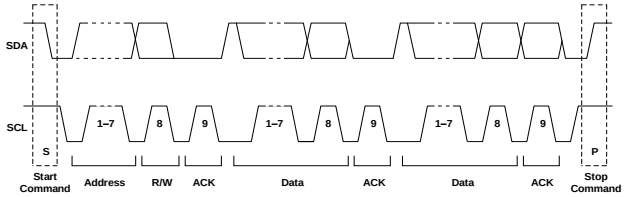


Figure 39: Complete Data Transfer

After the start command, a slave address is sent. This address is 7 bits long, followed by an 8th data direction bit. The data direction bit determines whether the transmission is a read (R) or write (W). A 0 indicates a write transmission, and a 1 indicates a read (a request for data). A data transfer is always terminated by a stop command generated by the initiator. However, if the initiator still wants to communicate on the bus, then it can generate a repeated start command and address another target without first generating a stop command.

Write Data Format

A write to the MPQ70700FS includes a start command, the target device address with the read/write (RW) bit set to 0, 1 data byte to the register address, 1 data byte to the register content, and a stop command.

Sequential writing is also supported in the MPQ70700FS, where multiple bytes can be written into the registers. The 1st data byte can be written to register address N, and the 2nd data byte can be written to register address N++, and so on, until a stop command is received. When packet error checking (PEC) is enabled, the MPQ70700FS does not support sequential writing.

Figure 40 shows an I²C write single register example, and Figure 41 on page 62 shows an I²C sequential write register example.

I²C Address Pin

The MPQ70700FS supports 127 different addresses (00h to 7Fh), which can be preset to the I2C_ADDRESS (51h) command via the I²C bus. The I²C address's high 5 least significant bit (5LSB) address is controlled via the I2C_ADDRESS_NVM bits (51h, bits[6:2]). The I²C address's low 2LSB can be configured via the ADDR pin (see Table 5).

Table 5: I²C Address Low 2LSB Configuration

I2C_ADDRESS_PIN (51h, bits[1:0])	Configuration
00	ADDR connected to GND
01	ADDR connected to GND via a 100kΩ resistor
10	ADDR connected to VIN1 via a 100kΩ resistor
11	ADDR connected to VIN1

The I²C function can be disabled to further decrease the quiescent current (I_Q) via the I2C_IO_CTL (53h) command. The I²C is only disabled in normal idle state, and it is automatically enabled once the EN pin voltage (V_{EN}) exceeds its rising threshold ($V_{IH\_EN\_R}$).

Read Data Format

A read to the MPQ70700FS includes a start command; the target device address with the R/W bit set to 1; 1 data byte to the register address, followed by a repeat start command; the same target device address; 1 data byte from the target, and a stop command.

Sequential reading is also supported in the MPQ70700FS, where multiple bytes can be sequentially read from the power management (PMIC) registers with register address++.

Figure 42 on page 62 shows an I²C read single register example, and Figure 43 on page 62 shows an I²C read multi-byte register example.

Packet Error Checking (PEC)

PEC improves communication reliability and robustness. Whenever applicable, PEC is implemented by appending a packet error code after the data of each message transfer.

PEC is a CRC-8 error-checking byte, calculated on all the message bytes (including addresses and R/W bits). PEC is appended to the message by the device that supplied the last data byte. In addition, PEC is register-configurable to be disabled if not necessary.

If an incorrect PEC is received or no PEC value is sent during the write command, then the MPQ70700FS does not receive the data. The PEC fault is reported, and the ERRO1 pin asserts.

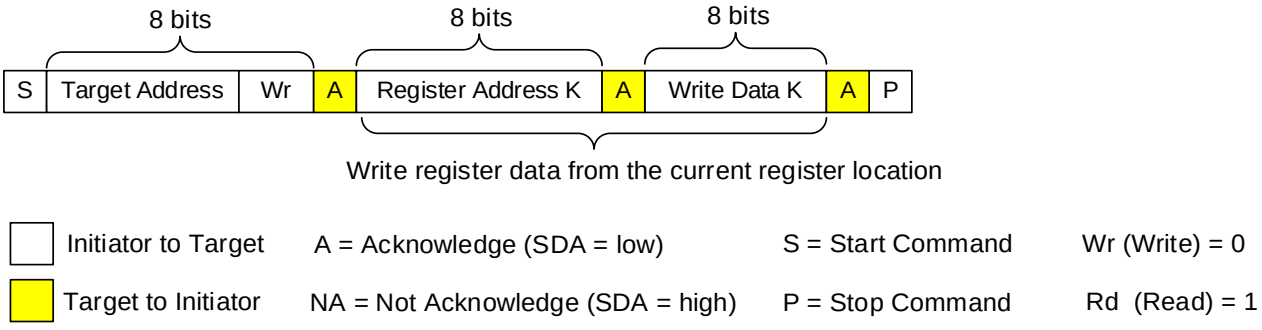


Figure 40: I²C Write Single Register Example

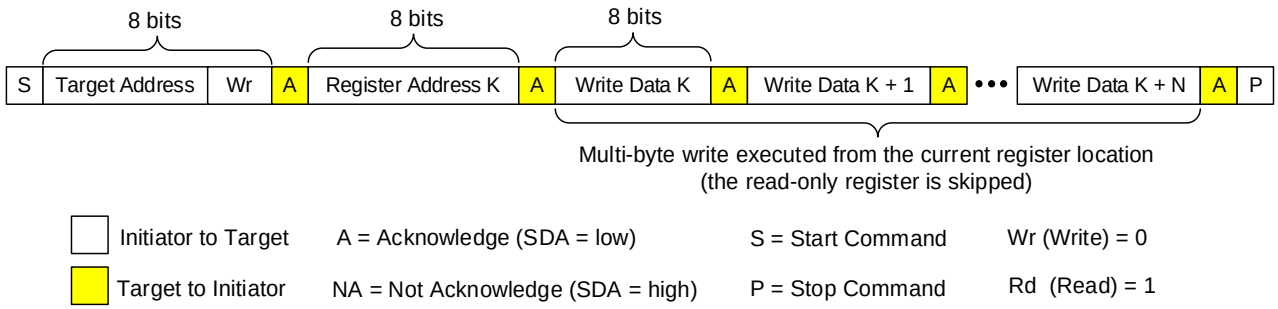


Figure 41: I²C Sequential Write Register Example

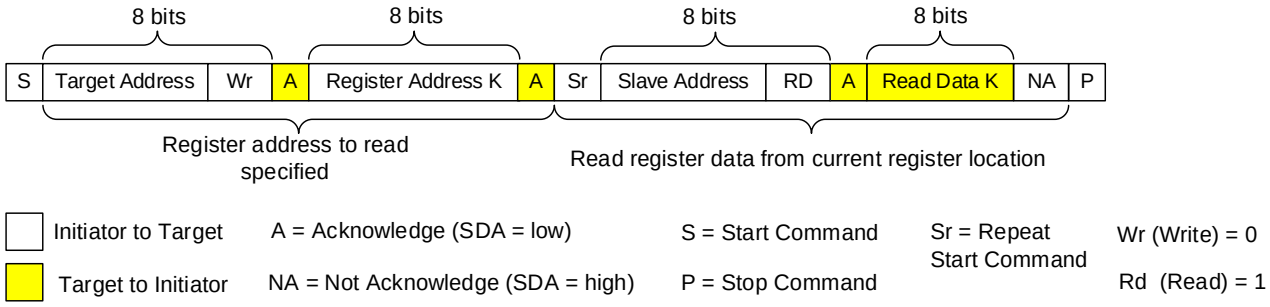


Figure 42: I²C Read Single Register Example

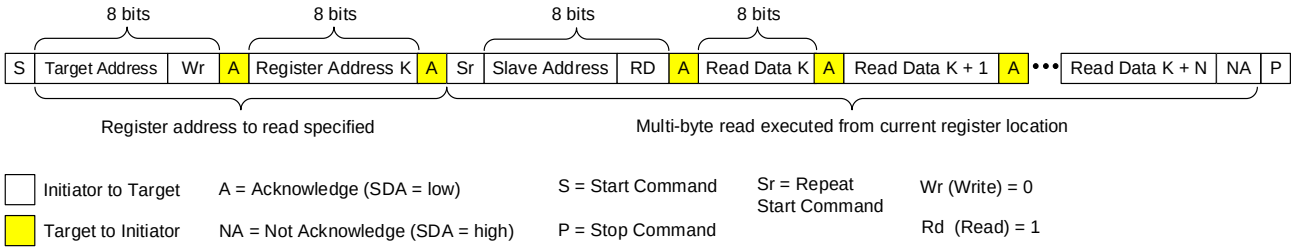


Figure 43: I²C Read Multi-Byte Register Example

SUPPORTED I²C COMMANDS

Command Code	Command Name	Type	Bytes	OTP	RTCRC	Default (19)	Lockout
00h	DEVICE_REV	R	1	Yes	No	00h	No
01h	WRITE_PROTECT	R/W	1	No	No	B6h	No
02h	FAULT_GROU	R/W	1	No	No	00h	No
03h	FAULT_INTERNAL	R/W	1	No	No	00h	No
04h	FAULT_SYS	R/W	1	No	No	00h	No
05h	FAULT_CHANNELS1	R/W	1	No	No	00h	No
06h	FAULT_CHANNELS2	R/W	1	No	No	00h	No
07h	FAULT_CHANNELS3	R/W	1	No	No	00h	No
08h	FAULT_TEST	R/W	1	No	No	00h	No
09h	FAULT_ENABLE_INTERNAL	R/W	1	Yes	Yes	00h	Yes
0Ah	FAULT_ENABLE_SYS	R/W	1	Yes	Yes	00h	Yes
0Bh	FAULT_ENABLE_CHANNELS1	R/W	1	Yes	Yes	00h	Yes
0Ch	FAULT_ENABLE_CHANNELS2	R/W	1	Yes	Yes	00h	Yes
0Dh	FAULT_ENABLE_CHANNELS3	R/W	1	Yes	Yes	00h	Yes
0Eh	FAULT_ENABLE_TEST	R/W	1	Yes	Yes	00h	Yes
0Fh	FAULT_REACTION_GUP1	R/W	1	Yes	Yes	00h	Yes
10h	FAULT_REACTION_GUP2	R/W	1	Yes	Yes	00h	Yes
11h	FAULT_REACTION_GUP3	R/W	1	Yes	Yes	00h	Yes
12h	FAULT_REACTION_GUP4	R/W	1	Yes	Yes	00h	Yes
13h	FAULT_REACTION_GUP_ INTERNAL	R/W	1	Yes	Yes	00h	Yes
14h	ERR_MODE	R/W	1	Yes	Yes	00h	Yes
15h	IO_STAT	R	1	Yes	No	-	No
16h	FORCE_CTL	R/W	1	Yes	Yes	00h	Yes
17h	EN2_GROUP	R/W	1	Yes	Yes	00h	Yes
18h	CHANNEL_EN	R/W	1	Yes	Yes	00h	Yes
19h	TEST_CFG	R/W	1	Yes	Yes	00h	Yes
1Ah	DLY_RCOV_CFG	R/W	1	Yes	Yes	00h	Yes
1Bh	GPIO_CFG	R/W	1	Yes	Yes	00h	Yes
1Ch	TIME_SLOT	R/W	1	Yes	Yes	00h	Yes
1Dh	SEQ_GPIO1	R/W	1	Yes	Yes	00h	Yes
1Eh	SEQ_GPIO2	R/W	1	Yes	Yes	00h	Yes
1Fh	SEQ_GPIO3	R/W	1	Yes	Yes	00h	Yes
20h	SEQ_GPIO4	R/W	1	Yes	Yes	00h	Yes
21h	VREF_LDO1	R/W	1	Yes	Yes	00h	Yes
22h	SETUP_LDO1	R/W	1	Yes	Yes	00h	Yes
23h	SEQ_LDO1	R/W	1	Yes	Yes	00h	Yes
24h	VREF_LDO2	R/W	1	Yes	Yes	00h	Yes
25h	SETUP_LDO2	R/W	1	Yes	Yes	00h	Yes
26h	SEQ_LDO2	R/W	1	Yes	Yes	00h	Yes

SUPPORTED I²C COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes	OTP	RTCRC	Default (19)	Lockout
27h	VREF_LDO3	R/W	1	Yes	Yes	00h	Yes
28h	SETUP_LDO3	R/W	1	Yes	Yes	00h	Yes
29h	SEQ_LDO3	R/W	1	Yes	Yes	00h	Yes
2Ah	VREF_LDO4	R/W	1	Yes	Yes	00h	Yes
2Bh	SETUP_LDO4	R/W	1	Yes	Yes	00h	Yes
2Ch	SEQ_LDO4	R/W	1	Yes	Yes	00h	Yes
2Dh	VREF_LDO5	R/W	1	Yes	Yes	00h	Yes
2Eh	SETUP_LDO5	R/W	1	Yes	Yes	00h	Yes
2Fh	SEQ_LDO5	R/W	1	Yes	Yes	00h	Yes
30h	POR1_CTL_CTH	R/W	1	Yes	Yes	FFh	Yes
31h	POR2_CTL_CTH	R/W	1	Yes	Yes	FFh	Yes
32h	POR3_CTL_CTH	R/W	1	Yes	Yes	FFh	Yes
33h	POR4_CTL_CTH	R/W	1	Yes	Yes	FFh	Yes
34h	POR5_CTL_CTH	R/W	1	Yes	Yes	FFh	Yes
35h	POR_CTL_DLY	R/W	1	Yes	Yes	00h	Yes
36h	MON1_OV_VTH	R/W	1	Yes	Yes	FFh	Yes
37h	MON1_UV_VTH	R/W	1	Yes	Yes	00h	Yes
38h	MON1_MODE	R/W	1	Yes	Yes	00h	Yes
39h	MON2_OV_VTH	R/W	1	Yes	Yes	FFh	Yes
3Ah	MON2_UV_VTH	R/W	1	Yes	Yes	00h	Yes
3Bh	MON2_MODE	R/W	1	Yes	Yes	00h	Yes
3Ch	LDO1_OV_VTH	R/W	1	Yes	Yes	FFh	Yes
3Dh	LDO1_UV_VTH	R/W	1	Yes	Yes	00h	Yes
3Eh	LDO1_MODE	R/W	1	Yes	Yes	00h	Yes
3Fh	LDO2_OV_VTH	R/W	1	Yes	Yes	FFh	Yes
40h	LDO2_UV_VTH	R/W	1	Yes	Yes	00h	Yes
41h	LDO2_MODE	R/W	1	Yes	Yes	00h	Yes
42h	LDO3_OV_VTH	R/W	1	Yes	Yes	FFh	Yes
43h	LDO3_UV_VTH	R/W	1	Yes	Yes	00h	Yes
44h	LDO3_MODE	R/W	1	Yes	Yes	00h	Yes
45h	LDO4_OV_VTH	R/W	1	Yes	Yes	FFh	Yes
46h	LDO4_UV_VTH	R/W	1	Yes	Yes	00h	Yes
47h	LDO4_MODE	R/W	1	Yes	Yes	00h	Yes
48h	LDO5_OV_VTH	R/W	1	Yes	Yes	FFh	Yes
49h	LDO5_UV_VTH	R/W	1	Yes	Yes	00h	Yes
4Ah	LDO5_MODE	R/W	1	Yes	Yes	00h	Yes
4Bh	WDT_CFG	R/W	1	Yes	Yes	00h	Yes
4Ch	WDT_CLOSE	R/W	1	Yes	Yes	00h	Yes
4Dh	WDT_OPEN	R/W	1	Yes	Yes	00h	Yes
4Eh	WDT_QA_CFG	R/W	1	No	Yes	00h	Yes

SUPPORTED I²C COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes	OTP	RTCRC	Default (19)	Lockout
4Fh	WDT_TEST	R/W	1	No	Yes	00h	Yes
50h	WDTKEY	R/W	1	No	Yes	00h	Yes
51h	I2C_ADDRESS	R/W	1	No	Yes	08h	Yes
52h	I2C_CONFIG	R/W	1	Yes	Yes	00h	Yes
53h	I2C_IO_CTL	R/W	1	No	Yes	01h	No
54h	WDT_STATUS1	R	1	No	No	00h	No
55h	WDT_STATUS2	R	1	No	No	00h	No
56h	WDT_STATUS3	R	1	No	No	00h	No
57h	BIST_STATUS	R	1	No	No	00h	No
58h	FORCE_EXIT_FS	R/W	1	No	No	00h	No

Note:

19) The default value is the initial configuration for the MPQ70700FS-0000 registers. These values can be redefined if the OTP function is available.

REGISTER MAP

DEVICE_REV (00h)

Format: Unsigned binary

POR Value: 0x00

The DEVICE_REV command returns the device information through the register type.

Bits	Access	Bit Name	Description
7:0	R/W	DEVICE_REV	Returns the device's revision information.

WRITE_PROTECT (01h)

Format: Unsigned binary

POR Value: 0xB6

The WRITE_PROTECT command can protect specific read/write (R/W) commands that include lockout (indicated as "Yes" for the Lockout column in the Supported I²C Commands section starting on page 63) by making them read-only. These R/W commands' default status is unlocked after power on. The status is changed to lockout when the other values (except for the default value) is written to the register. Once the default value is written to the register again, the specific R/W commands are unlocked.

Bits	Access	Bit Name	Description
7:0	R/W	WRITE_PROTECT	Makes specific R/W commands that include lockout read-only. 8'b10110110: Unlocks the specific R/W commands that include lockout Other values: Locks out the specific R/W commands that include lockout

FAULT_GROUP (02h)

Format: Unsigned binary

POR Value: 0x00

The FAULT_GROUP command indicates whether any of the following errors occurred: ERRIN fault, internal fault, system fault, channel fault, and test fault. This command supports writing 1 to clear the fault flag.

Bits	Access	Bit Name	Description
7:5	R/W	RESERVED	Reserved.
4	R/W	F_ERRIN	If the ERRIN status changed from high to low, or from low to high, then the MPQ70700FS detects an ERRIN fault. This bit is set to 1. 1'b0: No ERRIN fault has occurred 1'b1: An ERRIN fault has occurred
3	R/W	F_INTERNAL	If an internal fault occurs in the MPQ70700FS, then this bit is set to 1. See the FAULT_INTERNAL (03h) command on page 67 for more details regarding the internal fault types. 1'b0: No internal fault has occurred 1'b1: An internal fault has occurred
2	R/W	F_SYS	If a system fault occurs in the MPQ70700FS, then this bit is set to 1. See the FAULT_SYS (04h) command on page 68 for more details regarding system fault types. 1'b0: No system fault has occurred 1'b1: A system fault has occurred

1	R/W	F_CHANNELS	If a fault occurs in any of the MPQ70700FS's channels, then this bit is set to 1. See the FAULT_CHANNELS1 (05h) command on page 69, FAULT_CHANNELS2 (06h) on page 70, and FAULT_CHANNELS3 (07h) on page 71 for details regarding the channel fault types. 1'b0: No fault occurs in any of the MPQ70700FS's channels 1'b1: A fault occurs in one of the MPQ70700FS's channels
0	R/W	F_TEST	If a test fault occurs in the MPQ70700FS, then this bit is set to 1. See the FAULT_TEST (08h) command on page 71 for more details regarding the test fault types. 1'b0: No test fault has occurred 1'b1: A test fault has occurred

FAULT_INTERNAL (03h)

Format: Unsigned binary

POR Value: 0x00

The FAULT_INTERNAL command indicates internal faults, including the state machine fault, non-LBIST volatile memory (NBVM) fault, register write check fault, clock check fault, bandgap (BG) voltage check fault, and RTCRC fault. This command supports writing 1 to clear the fault flag.

Bits	Access	Bit Name	Description
7:6	R/W	RESERVED	Reserved.
5	R/W	F_STATE	Indicates whether a state machine fault occurs. The state machine fault is a one-hot coding state error of the system controller or power sequence controller. 1'b0: No state machine fault has occurred 1'b1: A state machine fault has occurred
4	R/W	F_NBVM_CHK	Indicates whether a non-LBISTABLE register double-check (NBVM check) fault occurs. NBVM check focuses on registers that are not checked by the LBIST check function. This ensures that all registers can be checked. 1'b0: No NBVM check fault has occurred 1'b1: A NBVM check fault has occurred
3	R/W	F_REG_WR_CHK	Indicates whether a register write check fault occurs. A register write check detects whether the register value is the same as the written data. 1'b0: No register write check fault has occurred 1'b1: A register write check fault has occurred
2	R/W	F_CLK	Indicates whether a clock check fault occurs. 1'b0: No clock fault has occurred 1'b1: A clock fault has occurred
1	R/W	F_BG	Indicates whether a bandgap (BG) voltage check fault occurs. 1'b0: No BG fault has occurred 1'b1: A BG fault has occurred
0	R/W	F_RTCRC	Indicates whether a register runtime CRC (RTCRC) check fault occurs. 1'b0: No RTCRC fault has occurred 1'b1: A RTCRC fault has occurred

FAULT_SYS (04h)

Format: Unsigned binary

POR Value: 0x00

The FAULT_SYS command indicates system faults, including the I²C packet error checking (PEC) fault, watchdog (WD) fault, thermal shutdown 1 (TSD1) fault, thermal warning 1 (TWN1) fault, thermal shutdown 2 (TSD2) fault, thermal warning 2 (TWN2) fault, thermal shutdown 3 (TSD3) fault, and thermal warning 3 (TWN3) fault. This command supports writing 1 to clear the fault flag.

Bits	Access	Bit Name	Description
7	R/W	F_I2C_PEC	Indicates whether an I²C PEC fault occurs. During an I²C write command, if the PEC value is incorrect, then this bit is set to 1. 1'b0: No I²C PEC fault has occurred 1'b1: An I²C PEC fault has occurred
6	R/W	F_WD	Indicates whether a WD failure occurs. If the WD fault count reaches the WD fault limit, then this bit is set to 1. 1'b0: No WD failure has occurred 1'b1: A WD failure has occurred
5	R/W	F_TSD1	Indicates whether a thermal shutdown 1 (TSD1) occurs. If the MPQ70700FS detects that the junction temperature (T_J) near LDO1 exceeds the thermal shutdown threshold (T_{TSD}), then a TSD1 fault is reported, and this bit is set to 1. 1'b0: No TSD1 fault has occurred 1'b1: A TSD1 fault has occurred
4	R/W	F_TWN1	Indicates whether a thermal warning 1 (TWN1) fault occurs. If the MPQ70700FS detects that T_J near LDO1 exceeds the thermal warning threshold (T_{TW}), then a TWN1 fault is reported, and this bit is set to 1. 1'b0: No TWN1 fault has occurred 1'b1: A TWN1 fault has occurred
3	R/W	F_TSD2	Indicates whether a thermal shutdown 2 (TSD2) fault occurs. If the MPQ70700FS detects that T_J near LDO2 or LDO3 exceeds T_{TSD}, then a TSD2 fault is reported, and this is set to 1. 1'b0: No TSD2 fault occurs 1'b1: A TSD2 fault occurred.
2	R/W	F_TWN2	Indicates whether a thermal warning 2 (TWN2) fault occurs. If the MPQ70700FS detects that T_J near LDO2 or LDO3 exceeds T_{TW}, then a TWN2 fault is reported, and this bit is set to 1. 1'b0: No TWN2 fault has occurred 1'b1: A TWN2 fault has occurred
1	R/W	F_TSD3	Indicates whether a thermal shutdown 3 (TSD3) fault occurs. If the MPQ70700FS detects that T_J near LDO4 or LDO5 exceeds T_{TSD}, then a TSD3 fault is reported, and this bit is set to 1. 1'b0: No TSD3 fault has occurred 1'b1: A TSD3 fault has occurred
0	R/W	F_TWN3	Indicates whether a thermal warning 3 (TWN3) fault occurs. If the MPQ70700FS detects that T_J near LDO4 or LDO5 exceeds T_{TW}, then a TWN3 fault is reported, and this bit is set to 1. 1'b0: No TWN3 fault has occurred 1'b1: A TWN3 fault has occurred

FAULT_CHANNELS1 (05h)

Format: Unsigned binary

POR Value: 0x00

The FAULT_CHANNELS1 command indicates fault in channel 1, including the voltage monitor 1 (VMON1) over-voltage (OV) fault, voltage monitor 2 (VMON2) OV fault, LDO1 and internal circuit supply input voltage (V_{IN1}) OV fault, LDO5 OV fault, LDO4 OV fault, LDO3 OV fault, LDO2 OV fault, and LDO1 OV fault. This command supports writing 1 to clear the fault flag.

Bits	Access	Bit Name	Description
7	R/W	F_MON1_OV	Indicates whether a VMON1 OV fault occurs. A VMON1 OV fault indicates that the VMON1 voltage (V_{MON1}) exceeds its OV threshold (V_{MON1_OV}) for a duration longer than the debounce time. 1’b0: No VMON1 OV fault has occurred 1’b1: A VMON1 OV fault has occurred
6	R/W	F_MON2_OV	Indicates whether a VMON2 OV fault occurs. A VMON2 OV fault indicates that the VMON2 voltage (V_{MON2}) exceeds its OV threshold (V_{MON2_OV}) for a duration longer than the debounce time. 1’b0: No VMON2 OV fault has occurred 1’b1: A VMON2 OV fault has occurred
5	R/W	F_VIN1_OV	Indicates whether a V_{IN1} OV fault occurs. A V_{IN1} OV fault indicates that V_{IN1} exceeds its OV rising threshold ($V_{IN1\_OV\_R}$). 1’b0: No V_{IN} OV fault has occurred 1’b1: A V_{IN} OV fault has occurred
4	R/W	F_LDO5_OV	Indicates whether an LDO5 OV fault occurs. An LDO5 OV fault indicates that the LDO5 output voltage (V_{OUT5}) exceeds its OV rising threshold ($V_{OUT5\_OV\_RISING}$) for a duration longer than the debounce time. 1’b0: No LDO5 OV fault has occurred 1’b1: An LDO5 OV fault has occurred
3	R/W	F_LDO4_OV	Indicates whether an LDO4 OV fault occurs. An LDO4 OV fault indicates that the LDO4 output voltage (V_{OUT4}) exceeds its OV rising threshold ($V_{OUT4\_OV\_RISING}$) for a duration longer than the debounce time. 1’b0: No LDO4 OV fault has occurred 1’b1: An LDO4 OV fault has occurred
2	R/W	F_LDO3_OV	Indicates whether an LDO3 OV fault occurs. An LDO3 OV fault indicates that the LDO3 output voltage (V_{OUT3}) exceeds its OV rising threshold ($V_{OUT3\_OV\_RISING}$) for a duration longer than the debounce time. 1’b0: No LDO3 OV fault has occurred 1’b1: An LDO3 OV fault has occurred
1	R/W	F_LDO2_OV	Indicates whether an LDO2 OV fault occurs. An LDO2 OV fault indicates that the LDO2 output voltage (V_{OUT2}) exceeds its OV rising threshold ($V_{OUT2\_OV\_RISING}$) for a duration longer than the debounce time. 1’b0: No LDO2 OV fault has occurred 1’b1: An LDO2 OV fault has occurred
0	R/W	F_LDO1_OV	Indicates whether an LDO1 OV fault occurs. An LDO1 OV fault indicates that the LDO1 output voltage (V_{OUT1}) exceeds its OV rising threshold ($V_{OUT1\_OV\_RISING}$) for a duration longer than the debounce time. 1’b0: No LDO1 OV fault has occurred 1’b1: An LDO1 OV fault has occurred

FAULT_CHANNELS2 (06h)

Format: Unsigned binary

POR Value: 0x00

The FAULT_CHANNELS2 command indicates faults in channel 2, including the VMON1 under-voltage (UV) fault, VMON2 UV fault, LDO2 and LDO3 supply voltage input voltage (V_{IN2}) over-voltage (OV) fault, LDO5 UV fault, LDO4 UV fault, LDO3 UV fault, LDO2 UV fault, and LDO1 UV fault. This command supports writing 1 to clear the fault flag.

Bits	Access	Bit Name	Description
7	R/W	F_MON1_UV	Indicates whether a VMON1 UV fault occurs. A VMON1 UV fault indicates that V_{MON1} exceeds its UV threshold (V_{MON1_UV}) for a duration longer than the debounce time. 1'b0: No VMON1 UV fault has occurred 1'b1: A VMON1 UV fault has occurred
6	R/W	F_MON2_UV	Indicates whether a VMON2 UV fault occurs. A VMON2 UV fault indicates that V_{MON2} exceeds its UV threshold (V_{MON2_UV}) for a duration longer than the debounce time. 1'b0: No VMON2 UV fault has occurred 1'b1: A VMON2 UV fault has occurred
5	R/W	F_VIN2_OV	Indicates whether a V_{IN2} OV fault occurs. A V_{IN2} OV fault indicates that V_{IN2} exceeds its OV rising threshold ($V_{IN2\_OV\_R}$). 1'b0: No V_{IN2} OV fault has occurred 1'b1: A V_{IN2} OV fault has occurred
4	R/W	F_LDO5_UV	Indicates whether an LDO5 UV fault occurs. An LDO5 UV fault indicates that V_{OUT5} exceeds its UV falling threshold ($V_{OUT5\_UV\_FALLING}$) for a duration longer than the debounce time. 1'b0: No LDO5 UV fault has occurred 1'b1: An LDO5 UV fault has occurred
3	R/W	F_LDO4_UV	Indicates whether an LDO4 UV fault occurs. An LDO4 UV fault indicates that V_{OUT4} exceeds its UV falling threshold ($V_{OUT4\_UV\_FALLING}$) for a duration longer than the debounce time. 1'b0: No LDO4 UV fault has occurred 1'b1: An LDO4 UV fault has occurred
2	R/W	F_LDO3_UV	Indicates whether an LDO3 UV fault occurs. An LDO3 UV fault indicates that V_{OUT3} exceeds its UV falling threshold ($V_{OUT3\_UV\_FALLING}$) for a duration longer than the debounce time. 1'b0: No LDO3 UV fault has occurred 1'b1: An LDO3 UV fault has occurred
1	R/W	F_LDO2_UV	Indicates whether an LDO2 UV fault occurs. An LDO2 UV fault indicates that V_{OUT2} exceeds its UV falling threshold ($V_{OUT2\_UV\_FALLING}$) for a duration longer than the debounce time. 1'b0: No LDO2 UV fault has occurred 1'b1: An LDO2 UV fault has occurred
0	R/W	F_LDO1_UV	Indicates whether an LDO1 UV fault occurs. An LDO1 UV fault indicates that V_{OUT1} exceeds its UV falling threshold ($V_{OUT1\_UV\_FALLING}$) for a duration longer than the debounce time. 1'b0: No LDO1 UV fault has occurred 1'b1: An LDO1 UV fault has occurred

FAULT_CHANNELS3 (07h)

Format: Unsigned binary

POR Value: 0x00

The FAULT_CHANNELS3 command indicates faults in channel 3, including the LDO4 and LDO5 supply input voltage (V_{IN3}) over-voltage (OV) fault, LDO5 over-current (OC) fault, LDO4 OC fault, LDO3 OC fault, LDO2 OC fault, and LDO1 OC fault. This command supports writing 1 to clear the fault flag.

Bits	Access	Bit Name	Description
7:6	R/W	RESERVED	Reserved.
5	R/W	F_VIN3_OV	Indicates whether a V_{IN3} OV fault occurs. A V_{IN3} OV fault indicates that V_{IN3} exceeds its OV rising threshold ($V_{IN3\_OV\_R}$). 1'b0: No V_{IN3} OV fault has occurred 1'b1: A V V_{IN3} OV fault has occurred
4	R/W	F_LDO5_OC	Indicates whether an LDO5 OC fault occurs. An LDO5 OC fault indicates that the LDO5 output current (I_{OUT5}) exceeds its limit (I_{OUT5_LIMIT}) for a duration longer than the debounce time. 1'b0: No LDO5 OC fault has occurred 1'b1: An LDO5 OC fault has occurred
3	R/W	F_LDO4_OC	Indicates whether an LDO4 OC fault occurs. An LDO4 OC fault indicates that the LDO4 output current (I_{OUT4}) exceeds its limit (I_{OUT4_LIMIT}) for a duration longer than the debounce time. 1'b0: No LDO4 OC fault has occurred 1'b1: An LDO4 OC fault has occurred
2	R/W	F_LDO3_OC	Indicates whether an LDO3 OC fault occurs. An LDO3 OC fault indicates that the LDO3 output current (I_{OUT3}) exceeds its limit (I_{OUT3_LIMIT}) for a duration longer than the debounce time. 1'b0: No LDO3 OC fault has occurred 1'b1: An LDO3 OC fault has occurred
1	R/W	F_LDO2_OC	Indicates whether an LDO2 OC fault occurs. An LDO2 OC fault indicates that LDO2 output current (I_{OUT2}) exceeding its limit (I_{OUT2_LIMIT}) for a duration longer than the debounce time. 1'b0: No LDO2 OC fault has occurred 1'b1: An LDO2 OC fault has occurred
0	R/W	F_LDO1_OC	Indicates whether an LDO1 OC fault occurs. An LDO1 OC fault indicates that the LDO1 output current (I_{OUT1}) exceeds its limit (I_{OUT1_LIMIT}) for a duration longer than the debounce time. 1'b0: No LDO1 OC fault has occurred 1'b1: An LDO1 OC fault has occurred

FAULT_TEST (08h)

Format: Unsigned binary

POR Value: 0x00

The FAULT_TEST command indicates test faults, including the one-time programmable (OTP) single-error correction (SEC) fault, OTP double-error detection (DED) fault, analog built-in testing (ABIST) fault, and logic built-in testing (LBIST) fault. This command supports writing 1 to clear the fault flag, except for the OTP DED fault and LBIST fault.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.

3	R/W	F_OTP_SEC	Indicates whether an OTP SEC fault occurs. An OTP SEC fault indicates that during OTP ECC process, the MPQ70700FS detects and corrects for a single bit error. 1’b0: No OTP SEC fault has occurred 1’b1: An OTP SEC fault has occurred
2	R/W	F_OTP_DED	Indicates whether an OTP DED fault occurs. An OTP DED fault indicates that during the OTP ECC process, the MPQ70700FS detects a double bit error. 1’b0: No OTP DED fault has occurred 1’b1: An OTP DED fault has occurred
1	R/W	F_BIST_A	Indicates whether an ABIST fault occurs. An ABIST fault indicates that the MPQ70700FS detects an ABIST error during the BIST process. 1’b0: No ABIST fault has occurred 1’b1: An ABIST fault has occurred
0	R/W	F_BIST_L	Indicates whether an LBIST fault occurs. An LBIST fault indicates that the MPQ70700FS detects an LBIST error during the BIST process. 1’b0: No LBIST fault has occurred 1’b1: An LBIST fault has occurred

FAULT_ENABLE_INTERNAL (09h)

Format: Unsigned binary

POR Value: 0x00

The FAULT_ENABLE_INTERNAL command enables the reaction of internal faults, including the fault enable of the auxiliary register runtime CRC (RTCRC) check, state machine, non-LBIST volatile memory (NBVM) check, register write check, bandgap check, and RTCRC check.

Bits	Access	Bit Name	Description
7:6	R/W	RESERVED	Reserved.
5	R/W	F_EN_RTCRC_AUX	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the RTCRC check fault. If this bit is set to 1 when an RTCRC check fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. This bit is the same as bit[0] of this command. If either this bit or bit[0] of this command is set to 1, then the RTCRC check fault reaction is enabled; otherwise, the RTCRC check fault reaction is disabled. 1’b0: Disabled 1’b1: Enabled
4	R/W	F_EN_STATE	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the one-hot coding state check fault (state machine error). If this bit is set to 1 when a one-hot coding state check fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. 1’b0: Disabled 1’b1: Enabled
3	R/W	F_EN_NBVM_CHK	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the non-LBISTABLE register double-check fault. If this bit is set to 1 when a non-LBISTABLE register double-check fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. 1’b0: Disabled 1’b1: Enabled

2	R/W	F_EN_REG_WR_CHK	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the register write check fault. If this bit is set to 1 when a register write check fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. 1'b0: Disabled 1'b1: Enabled
1	R/W	F_EN_BG	If this bit is set to 0, then ERRO1 is asserted, and the fault register does not have a reaction due to the bandgap check fault. If this bit is set to 1 when a bandgap check fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. 1'b0: Disabled 1'b1: Enabled
0	R/W	F_EN_RTCRC	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the RTCRC check fault. If this bit is set to 1 when an RTCRC check fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. This bit is the same as bit[5] of this command. If either this bit or bit[5] of this command is set to 1, then the RTCRC check fault reaction is enabled; otherwise, the RTCRC check fault reaction is disabled. 1'b0: Disabled 1'b1: Enabled

FAULT_ENABLE_SYS (0Ah)

Format: Unsigned binary

POR Value: 0x00

The FAULT_ENABLE_SYS command enables the reaction of system faults, including the fault enable of I^2C packet error checking (PEC), watchdog (WD) failure, thermal shutdown, and thermal warning.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3	R/W	F_EN_I2C_PEC	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the I^2C PEC fault. If this bit is set to 1 when an I^2C PEC fault occurs. then ERRO1 is asserted, and the fault register has the corrected reaction. 1'b0: Disabled 1'b1: Enabled
2	R/W	F_EN_REG_WD	If this bit is set to 0, then ERRO2 and the fault register do not have a reaction due to the WD failure. If this bit is set to 1 when a WD failure occurs, then ERRO2 is asserted, and fault register has the corrected reaction. 1'b0: Disabled 1'b1: Enabled
1	R/W	F_EN_TSD	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the thermal shutdown fault. If this bit is set to 1 when a thermal shutdown fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. 1'b0: Disabled 1'b1: Enabled
0	R/W	F_EN_TWN	If this bit is set to 0, then ERRO1 and the fault register do not have reaction due to the thermal warning fault. If this bit is set to 1 when a thermal warning fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. 1'b0: Disabled 1'b1: Enabled

FAULT_ENABLE_CHANNELS1 (0Bh)

Format: Unsigned binary

POR Value: 0x00

The FAULT_ENABLE_CHANNELS1 command enables the reaction of faults in channel 1, including the fault enable of voltage monitor 1 (VMON1) over-voltage (OV), voltage monitor 2 (VMON2) OV, LDO1 and internal circuit supply input voltage (V_{IN1}) OV, LDO5 OV, LDO4 OV, LDO3 OV, LDO2 OV, and LDO1 OV.

Bits	Access	Bit Name	Description
7	R/W	F_EN_MON1_OV	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the VMON1 OV fault. If this bit is set to 1 when a VMON1 OV fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. 1’b0: Disabled 1’b1: Enabled
6	R/W	F_EN_MON2_OV	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the VMON2 OV fault. If this bit is set to 1 when a VMON1 OV fault occurs, then ERRO1 is asserted, and fault register has the corrected reaction. 1’b0: Disabled 1’b1: Enabled
5	R/W	F_EN_VIN1_OV	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the V_{IN1} OV fault. If this bit is set to 1 when a V_{IN1} OV fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. 1’b0: Disabled 1’b1: Enabled
4	R/W	F_EN_LDO5_OV	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the LDO5 OV fault. If this bit is set to 1 when an LDO5 OV fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. 1’b0: Disabled 1’b1: Enabled
3	R/W	F_EN_LDO4_OV	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the LDO4 OV fault. If this bit is set to 1 when an LDO4 OV fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. 1’b0: Disabled 1’b1: Enabled
2	R/W	F_EN_LDO3_OV	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the LDO3 OV fault. If this bit is set to 1 when an LDO3 OV fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. 1’b0: Disabled 1’b1: Enabled
1	R/W	F_EN_LDO2_OV	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the LDO2 OV fault. If this bit is set to 1 when an LDO2 OV fault occurs, then ERRO1 is asserted, and fault register has the corrected reaction. 1’b0: Disabled 1’b1: Enabled
0	R/W	F_EN_LDO1_OV	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the LDO1 OV fault. If this bit is set to 1 when an LDO1 OV fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. 1’b0: Disabled 1’b1: Enabled

FAULT_ENABLE_CHANNELS2 (0Ch)

Format: Unsigned binary

POR Value: 0x00

The FAULT_ENABLE_CHANNELS2 command enables the reaction of faults in channel 2, including the fault enable of voltage monitor 1 (VMON1) under-voltage (UV), voltage monitor 2 (VMON2) UV, LDO2 and LDO3 supply voltage input voltage (V_{IN2}) over-voltage (OV), LDO5 UV, LDO4 UV, LDO3 UV, LDO2 UV, and LDO1 UV.

Bits	Access	Bit Name	Description
7	R/W	F_EN_MON1_UV	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the VMON1 UV fault. If this bit is set to 1 when a VMON1 UV fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. 1’b0: Disabled 1’b1: Enabled
6	R/W	F_EN_MON2_UV	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the VMON2 UV fault. If this bit is set to 1 when a VMON2 UV fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. 1’b0: Disable 1’b1: Enabled
5	R/W	F_EN_VIN2_OV	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the V_{IN2} OV fault. If this bit is set to 1 when a V_{IN2} OV fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. 1’b0: Disabled 1’b1: Enabled
4	R/W	F_EN_LDO5_UV	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the LDO5 UV fault. If this bit is set to 1 when an LDO5 UV fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. 1’b0: Disabled 1’b1: Enabled
3	R/W	F_EN_LDO4_UV	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the LDO4 UV fault. If this bit is set to 1 when an LDO4 UV fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. 1’b0: Disabled 1’b1: Enabled
2	R/W	F_EN_LDO3_UV	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the LDO3 UV fault. If this bit is set to 1 when an LDO3 UV fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. 1’b0: Disabled 1’b1: Enabled
1	R/W	F_EN_LDO2_UV	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the LDO2 UV fault. If this bit is set to 1 when an LDO2 UV fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. 1’b0: Disabled 1’b1: Enabled
0	R/W	F_EN_LDO1_UV	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the LDO1 UV fault. If this bit is set to 1 when an LDO1 UV fault occurs, then ERRO1 is asserted, and the fault register has the corrected reaction. 1’b0: Disabled 1’b1: Enabled

FAULT_ENABLE_CHANNELS3 (0Dh)

Format: Unsigned binary

POR Value: 0x00

The FAULT_ENABLE_CHANNELS3 command enables the reaction of the faults in channel 3, including the fault enable of the supply input voltage (V_{IN3}) over-voltage (OV), LDO5 over-current (OC), LDO4 OC, LDO3 OC, LDO2 OC, and LDO1 OC.

Bits	Access	Bit Name	Description
7:6	R/W	RESERVED	Reserved.
5	R/W	F_EN_VIN3_OV	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the V_{IN3} OV fault. If this bit is set to 1 when a V_{IN3} OV fault occurs, then ERRO1 is asserted, and the fault register has a corrected reaction. 1’b0: Disabled 1’b1: Enabled
4	R/W	F_EN_LDO5_OC	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the LDO5 OC fault. If this bit is set to 1 when an LDO5 OC fault occurs, then ERRO1 is asserted, and the fault register has a corrected reaction. 1’b0: Disabled 1’b1: Enabled
3	R/W	F_EN_LDO4_OC	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the LDO4 OC fault. If this bit is set to 1 when an LDO4 OC fault occurs, then ERRO1 is asserted, and the fault register has a corrected reaction. 1’b0: Disabled 1’b1: Enabled
2	R/W	F_EN_LDO3_OC	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the LDO3 OC fault. If this bit is set to 1, when an LDO3 OC fault occurs, then ERRO1 is asserted, and fault register has a corrected reaction. 1’b0: Disabled 1’b1: Enabled
1	R/W	F_EN_LDO2_OC	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the LDO2 OC fault. If this bit is set to 1 when an LDO2 OC fault occurs, then ERRO1 is asserted, and the fault register has a corrected reaction. 1’b0: Disabled 1’b1: Enabled
0	R/W	F_EN_LDO1_OC	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the LDO1 OC fault. If this bit is set to 1 when an LDO1 OC fault occurs, then ERRO1 is asserted, and the fault register has a corrected reaction. 1’b0: Disabled 1’b1: Enabled

FAULT_ENABLE_TEST (0Eh)

Format: Unsigned binary

POR Value: 0x00

The FAULT_ENABLE_TEST command enables the reaction of test faults, including the fault enable of one-time programmable (OTP) single-error correction (SEC) and the BIST_A fault.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.

1	R/W	F_EN_OTP_SEC	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the OTP single-bit error correction fault. If this bit is set to 1 when an OTP SEC fault occurs, then ERRO1 is asserted, and the fault register has a corrected reaction. 1'b0: Disabled 1'b1: Enabled
0	R/W	F_EN_BIST_A	If this bit is set to 0, then ERRO1 and the fault register do not have a reaction due to the BIST_A fault. If this bit is set to 1 when a BIST_A fault occurs, then ERRO1 is asserted, and the fault register has a corrected reaction. 1'b0: Disabled 1'b1: Enabled

FAULT_REACTION_GUP1 (0Fh)

Format: Unsigned binary

POR Value: 0x00

The FAULT_REACTION_GUP1 command configures the state machine reaction after triggering thermal shutdown and thermal warning.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1	R/W	F_GUP_TSD	If the MPQ70700FS detects a thermal shutdown fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state
0	R/W	F_GUP_TWN	If the MPQ70700FS detects a thermal warning (TWN) fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state

FAULT_REACTION_GUP2 (10h)

Format: Unsigned binary

POR Value: 0x00

The FAULT_REACTION_GUP2 command configures the state machine reaction after triggering the faults in channel 1.

Bits	Access	Bit Name	Description
7	R/W	F_GUP_MON1_OV	If the MPQ70700FS detects a VMON1 OV fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state. 1'b1: Enters failsafe state.
6	R/W	F_GUP_MON2_OV	If the MPQ70700FS detects a VMON2 OV fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state
5	R/W	F_GUP_VIN1_OV	If the MPQ70700FS detects a V_{IN1} OV fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state

4	R/W	F_GUP_LDO5_OV	If the MPQ70700FS detects an LDO5 OV fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state
3	R/W	F_GUP_LDO4_OV	If the MPQ70700FS detects an LDO4 OV fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state
2	R/W	F_GUP_LDO3_OV	If the MPQ70700FS detects an LDO3 OV fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state
1	R/W	F_GUP_LDO2_OV	If the MPQ70700FS detects an LDO2 OV fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state
0	R/W	F_GUP_LDO1_OV	If the MPQ70700FS detects an LDO1 OV fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state

FAULT_REACTION_GUP3 (11h)

Format: Unsigned binary

POR Value: 0x00

The FAULT_REACTION_GUP3 command configures the state machine reaction after triggering the faults in channel 2.

Bits	Access	Bit Name	Description
7	R/W	F_GUP_MON1_UV	If the MPQ70700FS detects a VMON1 UV fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state
6	R/W	F_GUP_MON2_UV	If the MPQ70700FS detects a VMON2 UV fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state
5	R/W	F_GUP_VIN2_OV	If the MPQ70700FS detects a V_{IN2} OV fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state
4	R/W	F_GUP_LDO5_UV	If the MPQ70700FS detects an LDO5 UV fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state
3	R/W	F_GUP_LDO4_UV	If the MPQ70700FS detects an LDO4 UV fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state

2	R/W	F_GUP_LDO3_UV	If the MPQ70700FS detects an LDO3 UV fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state
1	R/W	F_GUP_LDO2_UV	If the MPQ70700FS detects an LDO2 UV fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state
0	R/W	F_GUP_LDO1_UV	If the MPQ70700FS detects an LDO1 UV fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state

FAULT_REACTION_GUP4 (12h)

Format: Unsigned binary

POR Value: 0x00

The FAULT_REACTION_GUP4 command configures the state machine reaction after triggering the faults in channel 3.

Bits	Access	Bit Name	Description
7:6	R/W	RESERVED	Reserved.
5	R/W	F_GUP_VIN3_OV	If the MPQ70700FS detects a V_{IN3} OV fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state
4	R/W	F_GUP_LDO5_OC	If the MPQ70700FS detects an LDO5 OC fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state
3	R/W	F_GUP_LDO4_OC	If the MPQ70700FS detects an LDO4 OC fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state
2	R/W	F_GUP_LDO3_OC	If the MPQ70700FS detects an LDO3 OC fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state
1	R/W	F_GUP_LDO2_OC	If the MPQ70700FS detects an LDO2 OC fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state
0	R/W	F_GUP_LDO1_OC	If the MPQ70700FS detects an LDO1 OC fault, then the state machine can be set to enter failsafe state or fail-recovery state. 1'b0: Enters fail-recovery state 1'b1: Enters failsafe state

FAULT_REACTION_INTERNAL (13h)

Format: Unsigned binary

POR Value: 0x00

The FAULT_REACTION_INTERNAL command configures the state machine reaction after triggering the internal faults.

Bits	Access	Bit Name	Description
7:5	R/W	RESERVED	Reserved.
4	R/W	F_GUP_NBVM_CHK	If the MPQ70700FS detects a non-LBISTABLE register double-check fault, then the state machine can be set to enter failsafe state or no reaction. 1’b0: No reaction 1’b1: Enters failsafe state
3	R/W	F_GUP_REG_WR_CHK	If the MPQ70700FS detects a register write check fault, then the state machine can be set to enter failsafe state or no reaction. 1’b0: No reaction 1’b1: Enters failsafe state
2	R/W	F_GUP_CLK	If the MPQ70700FS detects a clock check fault, then the state machine can be set to enter failsafe state or no reaction. 1’b0: No reaction 1’b1: Enters failsafe state
1	R/W	F_GUP_BG	If the MPQ70700FS detects a bandgap check fault, then the state machine can be set to enter failsafe state or no reaction. 1’b0: No reaction 1’b1: Enters failsafe state
0	R/W	F_GUP_RTCRC	If the MPQ70700FS detects an RTCRC check fault, then the state machine can be set to enter failsafe state or no reaction. 1’b0: No reaction 1’b1: Enters failsafe state

ERR_MODE (14h)

Format: Unsigned binary

POR Value: 0x00

The ERR_MODE command configures the ERRIN mode and delay time.

Bits	Access	Bit Name	Description
7	R/W	RESERVED	Reserved.
6	R/W	ERRIN_MODE	If the system has an error, then the system-on-chip (SoC) sends a signal to the MPQ70700FS’s ERRIN pin. The MPQ70700FS can use ERRIN mode to set whether ERRIN receives a high or low valid signal. 1’b0: The ERRIN pin voltage (V_{ERRIN}) exceeds the error input high threshold (V_{IH_ERRIN}) as a valid ERRIN fault. 1’b1: V_{ERRIN} drops below the error input low threshold (V_{IL_ERRIN}) as a valid ERRIN fault
5:4	R/W	RESERVED	Reserved.

3:2	R/W	ERRIN_DLY	If the MPQ70700FS's ERRIN pin receives a valid signal and the duration is longer than the error input delay time (t_{ERRIN_DLY}), then an ERRIN fault has occurred. If the ERRIN signal recovers to normal before t_{ERRIN_DLY} ends, then the part does not detect an ERRIN fault. 2'b00: 0ms 2'b01: 2ms 2'b10: 5ms 2'b11: 10ms
1:0	R/W	ERRO_DLY	If the MPQ70700FS detects a valid error, then the ERROx pins (where x = 1 or 2) are changed from high to low after the error output delay time (t_{ERRO_DLY}). 2'b00: 0ms 2'b01: 2ms 2'b10: 5ms 2'b11: 10ms

IO_STAT (15h)

Format: Unsigned binary

POR Value: 0x00

The IO_STAT command indicates the status of the input/output (I/O) pins.

Bits	Access	Bit Name	Description
7:6	R	RESERVED	Reserved
5	R	ST_ERRIN	Indicates the ERRIN pin status. 1'b0: Low 1'b1: High
4	R	ST_EN	Indicates the EN pin status. 1'b0: Low 1'b1: High
3	R	ST_GPIO4	Indicates the GPIO4 pin status. 1'b0: Low 1'b1: High
2	R	ST_GPIO3	Indicates the GPIO3 pin status. 1'b0: Low 1'b1: High
1	R	ST_GPIO2	Indicates the GPIO2 pin status. 1'b0: Low 1'b1: High
0	R	ST_GPIO1	Indicates the GPIO1 pin status. 1'b0: Low 1'b1: High

FORCE_CTL (16h)

Format: Unsigned binary

POR Value: 0x00

The FORCE_CTL command configures BIST after power-off and whether the I/O pins (GPIO1, GPIO2, GPIO3, and GPIO4) can be pulled down normally.

Bits	Access	Bit Name	Description
7	R/W	BIST_GATING_ BYPASS	During power off, if the system's internal fault still exists and has not been cleared, then the system bypasses BIST. If this bit is set to 1, then the system can continue performing BIST. 1'b0: Bypasses BIST 1'b1: Performs BIST
6	R/W	FORCE_GPIO4	If this bit is set to 1, then the GPIO4 pin status is forced low. If this bit is set to 0, then the GPIO4 pin status is controlled by normal logic. 1'b0: Not forced low 1'b1: Forced low
5	R/W	FORCE_GPIO3	If this bit is set to 1, the GPIO3 pin status is forced low. If this bit is set to 0, then the GPIO3 pin status is controlled by normal logic. 1'b0: Not forced low 1'b1: Forced low
4	R/W	FORCE_GPIO2	If this bit is set to 1, then the GPIO2 pin status is forced low. If this bit is set to 0, then the GPIO2 pin status is controlled by normal logic. 1'b0: Not forced low 1'b1: Forced low
3	R/W	FORCE_GPIO1	If this bit is set to 1, then the GPIO1 pin status is forced low. If this bit is set to 0, then the GPIO1 pin status is controlled by normal logic. 1'b0: Not forced low 1'b1: Forced low
2	R/W	FORCE_ERRO2	If this bit is set to 1, then the ERRO2 pin status is forced low. If this bit is set to 0, then the ERRO2 pin status is controlled by normal logic. 1'b0: Not forced low 1'b1: Forced low
1	R/W	FORCE_ERRO1	If this bit is set to 1, then the ERRO1 pin status is forced low. If this bit is set to 0, then the ERRO1 pin status is controlled by normal logic. 1'b0: Not forced low 1'b1: Forced low
0	R/W	FORCE_POR	If this bit is set to 1, then the POR pin status is forced low. If this bit is set to 0, then the POR pin status is controlled by normal logic. 1'b0: Not forced low 1'b1: Forced low

EN2_GROUP (17h)

Format: Unsigned binary

POR Value: 0x00

The EN2_GROUP command configures whether the GPIO2, GPIO3, and GPIO4 outputs, as well as the LDO1, LDO2, LDO3, LDO4, and LDO5 outputs are controlled by the GPIO1 input (EN2).

Bits	Access	Bit Name	Description
7	R/W	GPIO4_EN2_GUP	If this bit is set to 1, then the GPIO4 output shuts down or starts up while the MPQ70700FS enters or exits sleep state. Otherwise, the GPIO4 output maintains the previous status. 1’b0: Cannot be controlled by EN2 1’b1: Controlled by EN2
6	R/W	GPIO3_EN2_GUP	If this bit is set to 1, then the GPIO3 output shuts down or starts up while the MPQ70700FS enters or exits sleep state. Otherwise, the GPIO3 output maintains the previous status. 1’b0: Cannot be controlled by EN2 1’b1: Controlled by EN2
5	R/W	GPIO2_EN2_GUP	If this bit is set to 1, then the GPIO2 output shuts down or starts up while the MPQ70700FS enters or exits sleep state. Otherwise, the GPIO2 output maintains the previous status. 1’b0: Cannot be controlled by EN2 1’b1: Controlled by EN2
4	R/W	LDO5_EN2_GUP	If this bit is set to 1, then the LDO5 output shuts down or starts up while the MPQ70700FS enters or exits sleep state. Otherwise, LDO5 maintains the previous status. 1’b0: Cannot be controlled by EN2 1’b1: Controlled by EN2
3	R/W	LDO4_EN2_GUP	If this bit is set to 1, LDO4 output will shut down or start up while MPQ70700FS enters SLEEP state or exits SLEEP state. Otherwise, LDO4 maintains previous status. 1’b0: Cannot controlled by EN2 1’b1: Controlled by EN2
2	R/W	LDO3_EN2_GUP	If this bit is set to 1, then the LDO3 output shuts down or starts up while the MPQ70700FS enters or exits sleep state. Otherwise, LDO3 maintains the previous status. 1’b0: Cannot be controlled by EN2 1’b1: Controlled by EN2
1	R/W	LDO2_EN2_GUP	If this bit is set to 1, then the LDO2 output shuts down or starts up while the MPQ70700FS enters or exits sleep state. Otherwise, LDO2 maintains the previous status. 1’b0: Cannot be controlled by EN2 1’b1: Controlled by EN2
0	R/W	LDO1_EN2_GUP	If this bit is set to 1, then the LDO1 output shuts down or starts up while the MPQ70700FS enters or exits sleep state. Otherwise, LDO1 maintains the previous status. 1’b0: Cannot be controlled by EN2 1’b1: Controlled by EN2

CHANNEL_EN (18h)

Format: Unsigned binary

POR Value: 0x00

The CHANNEL_EN command enables the LDO1, LDO2, LDO3, LDO4, and LDO5 outputs.

Bits	Access	Bit Name	Description
7:5	R/W	RESERVED	Reserved.
4	R/W	LDO5_EN	Enables the LDO5 output. If this bit is set to 1, then the LDO5 output starts up once the EN pin goes high. If this bit is set to 0, then the LDO5 output does not start up when the EN pin goes high. This bit is not allowed to be changed from disabled to enabled when EN is high. 1’b0: Disabled 1’b1: Enabled
3	R/W	LDO4_EN	Enables the LDO4 output. If this bit is set to 1, then the LDO4 output starts up once the EN pin goes high. If this bit is set to 0, then the LDO4 output does not start up when the EN pin goes high. This bit is not allowed to be changed from disabled to enabled when EN is high. 1’b0: Disabled 1’b1: Enabled
2	R/W	LDO3_EN	Enables the LDO3 output. If this bit is set to 1, then the LDO3 output starts up once the EN pin goes high. If this bit is set to 0, then the LDO3 output does not start up when the EN pin goes high. This bit is not allowed to be changed from disabled to enabled when EN is high. 1’b0: Disabled 1’b1: Enabled
1	R/W	LDO2_EN	Enables the LDO2 output. If this bit is set to 1, then the LDO2 output starts up once the EN pin goes high. If this bit is set to 0, then the LDO2 output does not start up when the EN pin goes high. This bit is not allowed to be changed from disabled to enabled when EN is high. 1’b0: Disabled 1’b1: Enabled
0	R/W	LDO1_EN	Enables the LDO1 output. If this bit is set to 1, then the LDO1 output starts up once the EN pin goes high. If this bit is set to 0, then the LDO1 output does not start up when the EN pin goes high. This bit is not allowed to be changed from disabled to enabled when EN is high. 1’b0: Disabled 1’b1: Enabled

TEST_CFG (19h)

Format: Unsigned binary

POR Value: 0x00

The TEST_CFG command enables built-in self-testing (BIST) after power off, fail recovery, and power-on reset (POR).

Bits	Access	Bit Name	Description
7:5	R/W	RESERVED	Reserved.
4	R/W	AT_SHDN	Enables BIST after the power-off sequence ends. If this bit is set to 1, then the MPQ70700FS performs BIST after the power-off sequence ends. Otherwise, the MPQ70700FS bypasses BIST and returns to normal idle state directly. This bit does not support one-time programmable (OTP) memory. 1’b0: Disabled 1’b1: Enabled

3:2	R/W	AT_RCOV	Enables BIST after the fail-recovery delay time ends. If this bit is set to 1, then the MPQ70700FS performs BIST after the fail-recovery delay time ends. Otherwise, the MPQ70700FS bypasses BIST and returns to normal idle state directly. 2'b00: Disabled 2'b11: Enabled Others: Invalid
1:0	R/W	AT_POR	Enables BIST after preloaded OTP passes. If this bit is set to 1, then the MPQ70700FS performs BIST after preloaded OTP passes. Otherwise, the MPQ70700FS bypasses BIST and returns to normal idle state directly. 2'b00: Disabled 2'b11: Enabled Others: Invalid

DLY_REOV_CFG (1Ah)

Format: Unsigned binary

POR Value: 0x00

The DLY_REOV_CFG command configures the retry times as well as the fail-recovery delay.

Bits	Access	Bit Name	Description
7:6	R/W	RETRY_CFG_RCOV	Sets the retry times of fail recovery. The MPQ70700FS has a counter that increases by 1 each time the state machine enters fail-recovery state. Once the counter hits the limit, the MPQ70700FS enters failsafe state. If the MPQ70700FS enter power-on state, then this counter resets to 0. 2'b00: No limit 2'b01: 3 times 2'b10: 5 times 2'b11: 10 times
5:0	R/W	DLY_RCOV	Sets the fail-recovery delay time (also called the fail-recovery duration) between 128µs and 8.192ms. This time can be calculated with the following equation: Fail-Recovery Delay Time = 128µs x (DLY_RCOV + 1)

GPIO_CFG (1Bh)

Format: Unsigned binary

POR Value: 0x00

The GPIO_CFG command configures GPIO1 and GPIO3 as output or input pins.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3	R/W	AF_GPIO4	GPIO4 is an output pin and can be a sequence output. 1'b1: Output Others: Invalid
2	R/W	AF_GPIO3	Configures GPIO3 as an output or input pin. If this bit is set to 1, then GPIO3 is configured as an output pin. If this bit is set to 0, then GPIO3 is configured as an input pin that can control the LDO1 output voltage (V_{OUT1}). 1'b0: Input 1'b1: Output
1	R/W	AF_GPIO2	GPIO2 is an output pin and can be a sequence output. 1'b1: Output Others: Invalid

0	R/W	AF_GPIO1	Configures GPIO1 as an output or input pin. If this bit is set to 1, then GPIO1 is configured as an output pin. If this bit is set to 0, then GPIO1 is configured as an input pin that controls the MPQ70700FS's sleep mode entry and exit. 1'b0: Input 1'b1: Output

TIME_SLOT (1Ch)

Format: Unsigned binary

POR Value: 0x00

The TIME_SLOT command configures the sequence time slot.

Bits	Access	Bit Name	Description
7:0	R/W	TIME_SLOT	Sets the sequence time slot between 100µs and 6475µs, and it can be calculated with the following equation: Sequence Time Slot = 100µs + 25µs x TIME_SLOT

SEQ_GPIO1 (1Dh)

Format: Unsigned binary

POR Value: 0x00

The SEQ_GPIO1 command configures the power-on and power-off sequence time slots of the GPIO1 output.

Bits	Access	Bit Name	Description
7:4	R/W	PU_GPIO1	Sets GPIO1's power-on sequence time slot between 0 and 15. The turn-on delay time is between 0 x 100µs and 15 x 6475µs. Turn-On Delay Time = PU_GPIO1 x TIME_SLOT (1Ch, bits[7:0])
3:0	R/W	PD_GPIO1	Sets GPIO1's power-down sequence time slot between 15 and 0. The turn-off delay time is between (15 - 15) x 100µs and (15 - 0) x 6475µs. Turn-Off Delay Time = (15 - PD_GPIO1) x TIME_SLOT (1Ch, bits[7:0])

SEQ_GPIO2 (1Eh)

Format: Unsigned binary

POR Value: 0x00

The SEQ_GPIO2 command configures the power-on and power-off sequence time slots of the GPIO2 output.

Bits	Access	Bit Name	Description
7:4	R/W	PU_GPIO2	Sets GPIO2's power-on sequence time slot between 0 and 15. The turn-on delay time is between 0 x 100µs and 15 x 6475µs. Turn-On Delay Time = PU_GPIO2 x TIME_SLOT (1Ch, bits[7:0])
3:0	R/W	PD_GPIO2	Sets GPIO2's power-down sequence time slot between 15 and 0. The turn-off delay time is between (15 - 15) x 100µs and (15 - 0) x 6475µs. Turn-Off Delay Time = (15 - PD_GPIO2) x TIME_SLOT (1Ch, bits[7:0])

SEQ_GPIO3 (1Fh)

Format: Unsigned binary

POR Value: 0x00

The SEQ_GPIO3 command configures the power-on and power-off sequence time slots of the GPIO3 output.

Bits	Access	Bit Name	Description
7:4	R/W	PU_GPIO3	Sets GPIO3's power-on sequence time slot between 0 and 15. The turn-on delay time is between 0 x 100µs and 15 x 6475µs. Turn-On Delay Time = PU_GPIO3 x TIME_SLOT (1Ch, bits[7:0])
3:0	R/W	PD_GPIO3	Sets GPIO3's power-down sequence time slot between 15 and 0. The turn-off delay time is between (15 - 15) x 100µs and (15 - 0) x 6475µs. Turn-Off Delay Time = (15 - PD_GPIO3) x TIME_SLOT (1Ch, bits[7:0])

SEQ_GPIO4 (20h)

Format: Unsigned binary

POR Value: 0x00

The SEQ_GPIO4 command configures the power-on and power-off sequence time slots of the GPIO4 output.

Bits	Access	Bit Name	Description
7:4	R/W	PU_GPIO4	Sets GPIO4's power-on sequence time slot between 0 and 15. The turn-on delay time is between 0 x 100µs and 15 x 6475µs. Turn-On Delay Time = PU_GPIO4 x TIME_SLOT (1Ch, bits[7:0])
3:0	R/W	PD_GPIO4	Sets GPIO4's power-down sequence time slot between 15 and 0. The turn-off delay time is between (15 - 15) x 100µs and (15 - 0) x 6475µs. Turn-Off Delay Time = (15 - PD_GPIO4) x TIME_SLOT (1Ch, bits[7:0])

VREF_LDO1 (21h)

Format: Unsigned binary

POR Value: 0x00

The VREF_LDO1 command sets LDO1's reference voltage (V_{REF1}).

Bits	Access	Bit Name	Description
7	R/W	RESERVED	Reserved.
6	R/W	LDO1_VREF_MODE	Sets the V_{REF1} step mode. The adjustable step mode can be selected according to the target LDO1 output voltage (V_{OUT1}). 1'b0: MODE0, 12.5mV/step, V_{REF1} range is between 0.5V and 1.0375V 1'b1: MODE1, 50mV/step, V_{REF1} range is between 1V and 3.6V
5:0	R/W	LDO1_VREF	If GPIO3 is configured as an output pin, then V_{REF1} is set by these bits. Otherwise, V_{REF1} is set via the LDO1_GPIO3_CTL_CFG bits (22h, bits[2:1]). For MODE0, V_{REF1} can be calculated with the following equation: V_{REF1} = MIN(0.5V + LDO1_VREF_MODE x LDO1_VREF, 1.0375) For MODE1, V_{REF1} can be calculated with the following equation: V_{REF1} = MIN(1V + LDO1_VREF_MODE x LDO1_VREF, 3.6)

SETUP_LDO1 (22h)

Format: Unsigned binary

POR Value: 0x00

The SETUP_LDO1 command sets LDO1's soft-start (SS) slew rate and enables the LDO1 output discharge. If the GPIO3 pin is configured to control the LDO1 output, then this command sets the LDO1 OV and UV thresholds and POR threshold via the LDO1_GPIO3_CTL_CFG bits (22h, bits[2:1]).

Bits	Access	Bit Name	Description
7:6	R/W	RESERVED	Reserved.
5:3	R/W	LDO1_SS_SLEW_RATE	Sets LDO1's SS rising slew rate. The slew rate is available between 10% x V_{OUT1} and 90% x V_{OUT1}. When setting an SS slew rate, the LDO1 output capacitance (C_{OUT1}) must be considered to ensure that the sum of the C_{OUT1} charge current and LDO1 load current does not exceed the LDO1 output current limit (I_{OUT1_LIMIT}) during the soft-start period. 3'b000: 0.625mV/µs 3'b001: 1.25mV/µs 3'b010: 2.5mV/µs 3'b011: 5mV/µs 3'b100: 10mV/µs 3'b101: 20mV/µs 3'b110: 33.3mV/µs 3'b111: 66.6mV/µs
2:1	R/W	LDO1_GPIO3_CTL_CFG	If GPIO3 is configured as an input pin, then the LDO1 output is 3.3V when this pin is low, and 1.8V when this pin is high. The LDO1 output OV and UV thresholds and POR threshold can be configured via these bits. The LDO1 OV threshold when V_{REF1} = 1.8V is set as the following: 2'b00: 1.975V 2'b01: 1.925V 2'b10: 1.8875V 2'b11: 1.8625V The LDO1 UV threshold when V_{REF1} = 1.8V is set as the following: 2'b00: 1.625V 2'b01: 1.675V 2'b10: 1.7125V 2'b11: 1.7375V The LDO1 POR threshold when V_{REF1} = 1.8V is set as the following: 2'b00: 1.625V 2'b01: 1.625V 2'b10: 1.625V 2'b11: 1.625V The LDO1 OV threshold when V_{REF1} = 3.3V is set as the following: 2'b00: 3.625V 2'b01: 3.5375V 2'b10: 3.4625V 2'b11: 3.4125V The LDO1 UV threshold when V_{REF1} = 3.3V is set as the following: 2'b00: 2.975V 2'b01: 3.0625V 2'b10: 3.1375V 2'b11: 3.1875V The LDO1 POR threshold when V_{REF1} = 3.3V is set as the following: 2'b00: 2.975V 2'b01: 2.975V 2'b10: 2.975V 2'b11: 2.975V

0	R/W	DISCHARGE_LDO1	Enables the LDO1 output discharge function. The output discharge function is only active during LDO1 output shutdown. 1'b0: Disabled 1'b1: Enabled

SEQ_LDO1 (23h)

Format: Unsigned binary

POR Value: 0x00

The SEQ_LDO1 command configures the power-on and power-off sequence time slots of LDO1.

Bits	Access	Bit Name	Description
7:4	R/W	PU_LDO1	Sets LDO1's power-on sequence time slot between 0 and 15. The turn-on delay time is between 0 x 100us and 15 x 6475us. Turn-On Delay Time = PU_LDO1 x TIME_SLOT (1Ch, bits[7:0])
3:0	R/W	PD_LDO1	Sets LDO1's power-down sequence time slot between 15 and 0. The turn-off delay time is between (15 - 15) x 100us and (15 - 0) x 6475us. Turn-Off Delay Time = (15 - PD_LDO1) x TIME_SLOT (1Ch, bits[7:0])

VREF_LDO2 (24h)

Format: Unsigned binary

POR Value: 0x00

The VREF_LDO2 command sets the LDO2 reference voltage (V_{REF2}).

Bits	Access	Bit Name	Description
7	R/W	RESERVED	Reserved.
6	R/W	LDO2_VREF_MODE	Sets the V_{REF2} step mode. The adjustable step mode can be selected according to the target V_{OUT2}. 1'b0: MODE0, 12.5mV/step, V_{REF2} range is between 0.5V and 1.0375V 1'b1: MODE1, 50mV/step, V_{REF2} range is between 1V and 3.6V
5:0	R/W	LDO2_VREF	Sets V_{REF2}. For MODE0, V_{REF2} can be calculated with the following equation: V_{REF2} = MIN(0.5V + LDO2_VREF_MODE x LDO2_VREF, 1.0375) For MODE1, V_{REF2} can be calculated with the following equation: V_{REF2} = MIN(1V + LDO2_VREF_MODE x LDO2_VREF, 3.6)

SETUP_LDO2 (25h)

Format: Unsigned binary

POR Value: 0x00

The SETUP_LDO2 command sets LDO2's soft-start (SS) slew rate and enables the LDO2 output discharge.

Bits	Access	Bit Name	Description
7:6	R/W	RESERVED	Reserved.

5:3	R/W	LDO2_SS_SLEW_RATE	Sets LDO2's SS rising slew rate. The slew rate is available between 10% x V_{OUT2} and 90% x V_{OUT2}. When setting an SS slew rate, the LDO2 output capacitance (C_{OUT2}) must be considered to ensure that the sum of the C_{OUT2} charge current and LDO2 load current does not exceed the LDO2 output current limit (I_{OUT2_LIMIT}) during the soft-start period. 3'b000: 0.625mV/µs 3'b001: 1.25mV/µs 3'b010: 2.5mV/µs 3'b011: 5mV/µs 3'b100: 10mV/µs 3'b101: 20mV/µs 3'b110: 33.3mV/µs 3'b111: 66.6mV/µs
2:1	R/W	RESERVED	Reserved.
0	R/W	DISCHARGE_LDO2	Enables the LDO2 output discharge function. The output discharge function is only active during LDO2 output shutdown. 1'b0: Disabled 1'b1: Enabled

SEQ_LDO2 (26h)

Format: Unsigned binary

POR Value: 0x00

The SEQ_LDO2 command configures the power-on and power-off sequence time slots of LDO2.

Bits	Access	Bit Name	Description
7:4	R/W	PU_LDO2	Sets LDO2's power-on sequence time slot between 0 and 15. The turn-on delay time is between 0 x 100µs and 15 x 6475µs. Turn-On Delay Time = PU_LDO2 x TIME_SLOT (1Ch, bits[7:0])
3:0	R/W	PD_LDO2	Sets LDO2's power-down sequence time slot between 15 and 0. The turn-off delay time is between (15 - 15) x 100µs and (15 - 0) x 6475µs. Turn-Off Delay Time = (15 - PD_LDO2) x TIME_SLOT (1Ch, bits[7:0])

VREF_LDO3 (27h)

Format: Unsigned binary

POR Value: 0x00

The VREF_LDO3 command sets the LDO3 reference voltage (V_{REF3}).

Bits	Access	Bit Name	Description
7	R/W	RESERVED	Reserved.
6	R/W	LDO3_VREF_MODE	Sets the V_{REF3} step mode. Select adjustable step mode according to the target V_{OUT3}. 1'b0: MODE0, 12.5mV/step, V_{REF3} range is between 0.5V and 1.0375V 1'b1: MODE1, 50mV/step, V_{REF3} range is between 1V and 3.6V
5:0	R/W	LDO3_VREF	Sets V_{REF3}. For MODE0, V_{REF3} can be calculated with the following equation: V_{REF3} = MIN(0.5V + LDO3_VREF_MODE x LDO3_VREF, 1.0375) For MODE1, V_{REF3} can be calculated with the following equation: V_{REF3} = MIN(1V + LDO3_VREF_MODE x LDO3_VREF, 3.6)

SETUP_LDO3 (28h)

Format: Unsigned binary

POR Value: 0x00

The SETUP_LDO3 command sets LDO3's soft-start (SS) slew rate and enables the LDO3 output discharge.

Bits	Access	Bit Name	Description
7:6	R/W	RESERVED	Reserved.
5:3	R/W	LDO3_SS_SLEW_RATE	Sets LDO3's SS rising slew rate. The slew rate is available between 10% x V_{OUT3} and 90% x V_{OUT3}. When setting an SS slew rate, the LDO3 output capacitance (C_{OUT3}) must be considered to ensure that the sum of the C_{OUT3} charge current and LDO3 load current does not exceed the LDO3 output current limit (I_{OUT3_LIMIT}) during the soft-start period. 3'b000: 0.625mV/µs 3'b001: 1.25mV/µs 3'b010: 2.5mV/µs 3'b011: 5mV/µs 3'b100: 10mV/µs 3'b101: 20mV/µs 3'b110: 33.3mV/µs 3'b111: 66.6mV/µs
2:1	R/W	RESERVED	Reserved.
0	R/W	DISCHARGE_LDO3	Enables the LDO3 output discharge function. The output discharge function is only active during LDO3 output shutdown. 1'b0: Disabled 1'b1: Enabled

SEQ_LDO3 (29h)

Format: Unsigned binary

POR Value: 0x00

The SEQ_LDO3 command configures the power-on and power-off sequence time slots of LDO3.

Bits	Access	Bit Name	Description
7:4	R/W	PU_LDO3	Sets LDO3's power-on sequence time slot between 0 and 15. The turn-on delay time is between 0 x 100µs and 15 x 6475µs. Turn-On Delay Time = PU_LDO3 x TIME_SLOT (1Ch, bits[7:0])
3:0	R/W	PD_LDO3	Sets LDO3's power down sequence time slot between 15 and 0. The turn-off delay time is between (15 - 15) x 100µs and (15 - 0) x 6475µs. Turn-Off Delay Time = (15 - PD_LDO3) x TIME_SLOT (1Ch, bits[7:0])

VREF_LDO4 (2Ah)

Format: Unsigned binary

POR Value: 0x00

The VREF_LDO4 command sets the LDO4 reference voltage (V_{REF4}).

Bits	Access	Bit Name	Description
7	R/W	RESERVED	Reserved.
6	R/W	LDO4_VREF_MODE	Sets the V_{REF4} step mode. The adjustable step mode can be selected according to the target V_{OUT4}. 1'b0: MODE0, 12.5mV/step, V_{REF4} range is between 0.5V and 1.0375V 1'b1: MODE1, 50mV/step, V_{REF4} range is between 1V and 3.6V

5:0	R/W	LDO4_VREF	Sets V_{REF4}. For MODE0, V_{REF4} can be calculated with the following equation: V_{REF4} = MIN(0.5V + LDO4_VREF_MODE x LDO4_VREF, 1.0375) For MODE1, V_{REF4} can be calculated with the following equation: V_{REF4} = MIN(1V + LDO4_VREF_MODE x LDO4_VREF, 3.6)

SETUP_LDO4 (2Bh)

Format: Unsigned binary

POR Value: 0x00

The SETUP_LDO4 command sets LDO4's soft-start (SS) slew rate and enables the LDO4 output discharge.

Bits	Access	Bit Name	Description
7:6	R/W	RESERVED	Reserved.
5:3	R/W	LDO4_SS_SLEW_RATE	Sets LDO4's SS rising slew rate. The slew rate is available between 10% x V_{OUT4} and 90% x V_{OUT4}. When setting an SS slew rate, the LDO4 output capacitance (C_{OUT4}) must be considered to ensure that the sum of the C_{OUT4} charge current and LDO4 load current does not exceed the LDO4 output current limit (I_{OUT4_LIMIT}) during the soft-start period. 3'b000: 0.625mV/µs 3'b001: 1.25mV/µs 3'b010: 2.5mV/µs 3'b011: 5mV/µs 3'b100: 10mV/µs 3'b101: 20mV/µs 3'b110: 33.3mV/µs 3'b111: 66.6mV/µs
2:1	R/W	RESERVED	Reserved.
0	R/W	DISCHARGE_LDO4	Enables the LDO4 output discharge function. The output discharge function is only active during LDO4 output shutdown. 1'b0: Disabled 1'b1: Enabled

SEQ_LDO4 (2Ch)

Format: Unsigned binary

POR Value: 0x00

The SEQ_LDO4 command configures the power-on and power-off sequence time slots of LDO4.

Bits	Access	Bit Name	Description
7:4	R/W	PU_LDO4	Sets LDO4's power-on sequence time slot between 0 and 15. The turn-on delay time is between 0 x 100µs and 15 x 6475µs. Turn-On Delay Time = PU_LDO4 x TIME_SLOT (1Ch, bits[7:0])
3:0	R/W	PD_LDO4	Sets LDO4's power-down sequence time slot between 15 and 0. The turn-off delay time is between (15 - 15) x 100µs and (15 - 0) x 6475µs. Turn-Off Delay Time = (15 - PD_LDO4) x TIME_SLOT (1Ch, bits[7:0])

VREF_LDO5 (2Dh)

Format: Unsigned binary

POR value: 0x00

The VREF_LDO5 command sets the LDO5 reference voltage (V_{REF5}).

Bits	Access	Bit Name	Description
7	R/W	RESERVED	Reserved.
6	R/W	LDO5_VREF_MODE	Sets the V_{REF5} step mode. The adjustable step mode can be selected according to the target V_{OUT5}. 1'b0: MODE0, 12.5mV/step, V_{REF5} range is between 0.5V and 1.0375V 1'b1: MODE1, 50mV/step, V_{REF5} range is between 1V and 3.6V
5:0	R/W	LDO5_VREF	Sets V_{REF5}. For MODE0, V_{REF5} can be calculated with the following equation: V_{REF5} = MIN(0.5V + LDO5_VREF_MODE x LDO5_VREF, 1.0375) For MODE1, V_{REF5} can be calculated with the following equation: V_{REF5} = MIN(1.0V + LDO5_VREF_MODE x LDO5_VREF, 3.6)

SETUP_LDO5 (2Eh)

Format: Unsigned binary

POR Value: 0x00

The SETUP_LDO5 command sets LDO5's soft-start (SS) slew rate and enables the LDO5 output discharge.

Bits	Access	Bit Name	Description
7:6	R/W	RESERVED	Reserved.
5:3	R/W	LDO5_SS_SLEW_RATE	Sets LDO5's SS rising slew rate. The slew rate is available between 10% x V_{OUT5} and 90% x V_{OUT5}. When setting an SS slew rate, the LDO5 output capacitance (C_{OUT5}) must be considered to ensure that the sum of the C_{OUT5} charge current and LDO5 load current does not exceed the LDO5 output current limit (I_{OUT5_LIMIT}) during the soft-start period. 3'b000: 0.625mV/µs 3'b001: 1.25mV/µs 3'b010: 2.5mV/µs 3'b011: 5mV/µs 3'b100: 10mV/µs 3'b101: 20mV/µs 3'b110: 33.3mV/µs 3'b111: 66.6mV/µs
2:1	R/W	RESERVED	Reserved.
0	R/W	DISCHARGE_LDO5	Enables the LDO5 output discharge function. The output discharge function is only active during LDO5 output shutdown. 1'b0: Disabled 1'b1: Enabled

SEQ_LDO5 (2Fh)

Format: Unsigned binary

POR Value: 0x00

The SEQ_LDO5 command configures the power-on and power-off sequence time slots of LDO5.

Bits	Access	Bit Name	Description
7:4	R/W	PU_LDO5	Sets LDO5's power-on sequence time slot between 0 and 15. The turn-on delay time is between 0 x 100µs and 15 x 6475µs. Turn-On Delay Time = PU_LDO5 x TIME_SLOT (1Ch, bits[7:0])
3:0	R/W	PD_LDO5	Sets LDO5's power-down sequence time slot between 15 and 0. The turn-off delay time is between (15 - 15) x 100µs and (15 - 0) x 6475µs. Turn-Off Delay Time = (15 - PD_LDO5) x TIME_SLOT (1Ch, bits[7:0])

POR1_CTL_CTH (30h)

Format: Unsigned binary

POR Value: 0xFF

The POR1_CTL_CTH command configures the LDO1 output's POR threshold.

Bits	Access	Bit Name	Description
7:0	R/W	LDO1_POR_ THRESHOLD	Sets the LDO1 output's POR threshold, which is between 0.45V and 3.6375V, 12.5mV/step. The LDO1 output's POR threshold can be calculated with the following equation: LDO1 Output POR Threshold = 0.45V + 0.0125V x LDO1_POR_THRESHOLD

POR2_CTL_CTH (31h)

Format: Unsigned binary

POR Value: 0xFF

The POR2_CTL_CTH command configures the LDO2 output's POR threshold.

Bits	Access	Bit Name	Description
7:0	R/W	LDO2_POR_ THRESHOLD	Sets the LDO2 output's POR threshold, which is between 0.45V and 3.6375V, 12.5mV/step. The LDO2 output's POR threshold can be calculated with the following equation: LDO2 Output POR Threshold = 0.45V + 0.0125V x LDO2_POR_THRESHOLD

POR3_CTL_CTH (32h)

Format: Unsigned binary

POR Value: 0xFF

The POR3_CTL_CTH command configures the LDO3 output's POR threshold.

Bits	Access	Bit Name	Description
7:0	R/W	LDO3_POR_ THRESHOLD	Sets the LDO3 output's POR threshold, which is between 0.45V and 3.6375V, 12.5mV/step. LDO3 Output POR Threshold = 0.45V + 0.0125V x LDO3_POR_THRESHOLD

POR4_CTL_CTH (33h)

Format: Unsigned binary

POR Value: 0xFF

The POR4_CTL_CTH command configures the LDO4 output's POR threshold.

Bits	Access	Bit Name	Description
7:0	R/W	LDO4_POR_ THRESHOLD	Sets the LDO4 output's POR threshold, which is between 0.45V and 3.6375V, 12.5mV/step. LDO4 Output POR Threshold = 0.45V + 0.0125V x LDO4_POR_THRESHOLD

POR5_CTL_CTH (34h)

Format: Unsigned binary

POR Value: 0xFF

The POR5_CTL_CTH command configures the LDO5 output's POR threshold.

Bits	Access	Bit Name	Description
7:0	R/W	LDO5_POR_ THRESHOLD	Sets the LDO5 output's POR threshold, which is between 0.45V and 3.6375V, 12.5mV/step. LDO5 Output POR Threshold = 0.45V + 0.0125V x LDO5_POR_THRESHOLD

POR_CTL_DLY (35h)

Format: Unsigned binary

POR Value: 0x00

The POR_CTL_DYL command configures the POR delay time.

Bits	Access	Bit Name	Description
7:0	R/W	POR_DELAY	Sets the POR de-asserted delay time and reset pulse width, which is between 128µs and 32.768ms, 128µs/step. POR Delay Time = 128µs x (POR_DELAY + 1)

MON1_OV_VTH (36h)

Format: Unsigned binary

POR Value: 0xFF

The MON1_OV_VTH command sets the VMON1 input voltage over-voltage (OV) threshold (V_{MON1_OV}).

Bits	Access	Bit Name	Description
7:0	R/W	MON1_OV_ THRESHOLD	Sets V_{MON1_OV}, which is between 0.45V and 3.6375V, 12.5mV/step. This can be calculated with the following equation: V_{MON1_OV} = 0.45V + 0.0125V x MON1_OV_THRESHOLD

MON1_UV_VTH (37h)

Format: Unsigned binary

POR Value: 0x00

The MON1_UV_VTH command sets the VMON1 input voltage under-voltage (UV) threshold (V_{MON1_UV}).

Bits	Access	Bit Name	Description
7:0	R/W	MON1_UV_ THRESHOLD	Sets V_{MON1_UV}, which is between 0.45V and 3.6375V, 12.5mV/step. This can be calculated with the following equation: V_{MON1_UV} = 0.45V + 0.0125V x MON1_UV_THRESHOLD

MON1_MODE (38h)

Format: Unsigned binary

POR Value: 0x00

The MON1_MODE command sets the VMON1 status and debounce time.

Bits	Access	Bit Name	Description
7	R/W	RESERVED	Reserved.
6	R/W	MON1_EN	Enables VMON1. 1'b0: Disabled 1'b1: Enabled
5	R/W	MON1_EN_IDLE	Configures whether the VMON1 OV or UV fault is detected as a valid fault when the system is in normal idle state. 1'b0: Invalid 1'b1: Valid
4	R/W	MON1_EN_ACTIVE	Configures whether the VMON1 OV or UV fault is detected as a valid fault when the system is in active, power-on, or power-off state. 1'b0: Invalid 1'b1: Valid
3	R/W	MON1_EN_SLEEP	Configures whether the VMON1 fault is detected as a valid fault when the system is in sleep mode, sleep mode entry, or sleep mode exit. 1'b0: Invalid 1'b1: Valid
2	R/W	RESERVED	Reserved.
1:0	R/W	MON1_DEBOUNCE	Sets the VMON1 OV or UV fault's debounce time. 2'b00: 10µs 2'b01: 20µs 2'b10: 40µs 2'b11: 80µs

MON2_OV_VTH (39h)

Format: Unsigned binary

POR Value: 0xFF

The MON2_OV_VTH command sets the VMON2 input voltage over-voltage (OV) threshold (V_{MON2_OV}).

Bits	Access	Bit Name	Description
7:0	R/W	MON2_OV_ THRESHOLD	Sets V_{MON2_OV}, which is between 0.45V and 3.6375V, 12.5mV/step. This can be calculated with the following equation: V_{MON2_OV} = 0.45V + 0.0125V x MON2_OV_THRESHOLD

MON2_UV_VTH (3Ah)

Format: Unsigned binary

POR Value: 0x00

The MON2_UV_VTH command sets the VMON2 input voltage under-voltage (UV) threshold (V_{MON2_UV}).

Bits	Access	Bit Name	Description
7:0	R/W	MON2_UV_ THRESHOLD	Sets V_{MON2_UV}, which is between 0.45V and 3.6375V, 12.5mV/step. This can be calculated with the following equation: V_{MON2_UV} = 0.45V + 0.0125V x MON2_UV_THRESHOLD

MON2_MODE (3Bh)

Format: Unsigned binary

POR Value: 0x00

The MON2_MODE command sets the VMON2 status and debounce time.

Bits	Access	Bit Name	Description
7	R/W	RESERVED	Reserved.
6	R/W	MON2_EN	Enables VMON2. 1’b0: Disabled 1’b1: Enabled
5	R/W	MON2_EN_IDLE	Configures whether the VMON2 OV or UV fault is detected as a valid fault when the system is in normal idle state. 1’b0: Invalid 1’b1: Valid
4	R/W	MON2_EN_ACTIVE	Configures whether the VMON2 OV or UV fault is detected as a valid fault when the system is in active, power-on, or power-off state. 1’b0: Invalid 1’b1: Valid
3	R/W	MON2_EN_SLEEP	Configure whether the VMON2 OV/UV fault is detected as a valid fault when the system is in sleep mode, sleep mode entry, or sleep mode exit. 1’b0: Invalid 1’b1: Valid
2	R/W	RESERVED	Reserved.
1:0	R/W	MON2_DEBOUNCE	Sets the VMON2 OV or UV fault’s debounce time. 2’b00: 10µs 2’b01: 20µs 2’b10: 40µs 2’b11: 80µs

LDO1_OV_VTH (3Ch)

Format: Unsigned binary

POR Value: 0xFF

The LDO1_OV_VTH command sets the LDO1 output voltage over-voltage (OV) rising threshold ($V_{OUT1\_OV\_RISING}$).

Bits	Access	Bit Name	Description
7:0	R/W	LDO1_OV_ THRESHOLD	Sets $V_{OUT1\_OV\_RISING}$, which is between 0.45V and 3.6375V, 12.5mV/step. $V_{OUT1\_OV\_RISING}$ is limited for V_{OUT1} and the LDO1 output OV hysteresis ($V_{OUT1\_OV\_HYS}$). To improve the accuracy of the parameters, the minimum $V_{OUT1\_OV\_RISING}$ must exceed the sum of the maximum V_{OUT1} and maximum $V_{OUT1\_OV\_HYS}$. $V_{OUT1\_OV\_RISING}$ can be calculated with the following equation: $V_{OUT1\_OV\_RISING}$ = 0.45V + 0.0125V x LDO1_OV_THRESHOLD

LDO1_UV_VTH (3Dh)

Format: Unsigned binary

POR Value: 0x00

The LDO1_UV_VTH command sets the LDO1 output voltage under-voltage (UV) falling threshold ($V_{OUT1\_UV\_FALLING}$).

Bits	Access	Bit Name	Description
7:0	R/W	LDO1_UV_ THRESHOLD	Sets $V_{OUT1\_UV\_FALLING}$, which is between 0.45V and 3.6375V, 12.5mV/step. $V_{OUT1\_UV\_FALLING}$ is limited for V_{OUT1} and the LDO1 output UV hysteresis ($V_{OUT1\_UV\_HYS}$). To improve the accuracy of the parameters, the maximum $V_{OUT1\_UV\_FALLING}$ must be below the difference between the minimum V_{OUT1} and maximum $V_{OUT1\_UV\_HYS}$. $V_{OUT1\_UV\_FALLING}$ can be calculated with the following equation: $V_{OUT1\_UV\_FALLING}$ = 0.45V + 0.0125V x LDO1_UV_THRESHOLD

LDO1_MODE (3Eh)

Format: Unsigned binary

POR Value: 0x00

The LDO1_MODE command sets the status and debounce time of LDO1 under-voltage (UV) and over-voltage (OV) faults, and all LDO over-current (OC) faults.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved
3:2	R/W	LDO_OC_ DEBOUNCE	Set the LDO OC fault's debounce time. 2'b00: 10µs 2'b01: 20µs 2'b10: 40µs 2'b11: 80µs
1:0	R/W	LDO1_DEBOUNCE	Sets the LDO1 UV and OV faults' debounce time. 2'b00: 10µs 2'b01: 20µs 2'b10: 40µs 2'b11: 80µs

LDO2_OV_VTH (3Fh)

Format: Unsigned binary

POR Value: 0xFF

The LDO2_OV_VTH command sets the LDO2 output voltage over-voltage (OV) rising threshold ($V_{OUT2\_OV\_RISING}$).

Bits	Access	Bit Name	Description
7:0	R/W	LDO2_OV_ THRESHOLD	Sets $V_{OUT2\_OV\_RISING}$, which is between 0.45V and 3.6375V, 12.5mV/step. $V_{OUT2\_OV\_RISING}$ is limited for V_{OUT2} and the LDO2 output OV hysteresis ($V_{OUT2\_OV\_HYS}$). To improve the accuracy of the parameters, the minimum $V_{OUT2\_OV\_RISING}$ must exceed the sum of the maximum V_{OUT2} and maximum $V_{OUT2\_OV\_HYS}$. $V_{OUT2\_OV\_RISING}$ can be calculated with the following equation: $V_{OUT2\_OV\_RISING}$ = 0.45V + 0.0125V x LDO2_OV_THRESHOLD

LDO2_UV_VTH (40h)

Format: Unsigned binary

POR Value: 0x00

The LDO2_UV_VTH command sets the LDO2 output voltage under-voltage (UV) falling threshold ($V_{OUT2\_UV\_FALLING}$).

Bits	Access	Bit Name	Description
7:0	R/W	LDO2_UV_ THRESHOLD	Sets $V_{OUT2\_UV\_FALLING}$, which is between 0.45V and 3.6375V, 12.5mV/step. $V_{OUT2\_UV\_FALLING}$ is limited for V_{OUT2} and the LDO2 output UV hysteresis ($V_{OUT2\_UV\_HYS}$). To improve the accuracy of the parameters, the maximum $V_{OUT2\_UV\_FALLING}$ must be below the difference between the minimum V_{OUT2} and maximum $V_{OUT2\_UV\_HYS}$. $V_{OUT2\_UV\_FALLING}$ can be calculated with the following equation: $V_{OUT2\_UV\_FALLING}$ = 0.45V + 0.0125V x LDO2_UV_THRESHOLD

LDO2_MODE (41h)

Format: Unsigned binary

POR Value: 0x00

The LDO2_MODE command is used to set the status and debounce time of LDO2 UV/OV fault.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1:0	R/W	LDO2_DEBOUNCE	Sets the LDO2 UV and OV faults' debounce time. 2'b00: 10µs 2'b01: 20µs 2'b10: 40µs 2'b11: 80µs

LDO3_OV_VTH (42h)

Format: Unsigned binary

POR Value: 0xFF

The LDO3_OV_VTH command sets the LDO3 output voltage over-voltage (OV) rising threshold ($V_{OUT3\_OV\_RISING}$).

Bits	Access	Bit Name	Description
7:0	R/W	LDO3_OV_ THRESHOLD	Sets $V_{OUT3\_OV\_RISING}$, which is between 0.45V and 3.6375V, 12.5mV/step. $V_{OUT3\_OV\_RISING}$ is limited for V_{OUT3} and the LDO2 output OV hysteresis ($V_{OUT2\_OV\_HYS}$). To improve the accuracy of the parameters, the minimum $V_{OUT3\_OV\_RISING}$ must exceed the sum of the maximum V_{OUT3} and maximum $V_{OUT3\_OV\_HYS}$. $V_{OUT3\_OV\_RISING}$ can be calculated with the following equation: $V_{OUT3\_OV\_RISING}$ = 0.45V + 0.0125V x LDO3_OV_THRESHOLD

LDO3_UV_VTH (43h)

Format: Unsigned binary

POR Value: 0x00

The LDO3_UV_VTH command sets the LDO3 output voltage under-voltage (UV) falling threshold ($V_{OUT3\_UV\_FALLING}$).

Bits	Access	Bit Name	Description
7:0	R/W	LDO3_UV_ THRESHOLD	Sets $V_{OUT3\_UV\_FALLING}$, which is between 0.45V and 3.6375V, 12.5mV/step. $V_{OUT3\_UV\_FALLING}$ is limited for V_{OUT3} and the LDO3 output UV hysteresis ($V_{OUT3\_UV\_HYS}$). To improve the accuracy of the parameters, the maximum $V_{OUT3\_UV\_FALLING}$ must be below the difference between the minimum V_{OUT3} and the maximum $V_{OUT3\_UV\_HYS}$. $V_{OUT3\_UV\_FALLING}$ can be calculated with the following equation: $V_{OUT3\_UV\_FALLING}$ = 0.45V + 0.0125V x LDO3_UV_THRESHOLD

LDO3_MODE (44h)

Format: Unsigned binary

POR Value: 0x00

The LDO3_MODE command sets the debounce time of the LDO3 UV and OV faults.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1:0	R/W	LDO3_DEBOUNCE	Sets the LDO3 UV and OV faults' debounce time. 2'b00: 10µs 2'b01: 20µs 2'b10: 40µs 2'b11: 80µs

LDO4_OV_VTH (45h)

Format: Unsigned binary

POR Value: 0xFF

The LDO4_OV_VTH command sets the LDO4 output voltage over-voltage (OV) rising threshold ($V_{OUT4\_OV\_RISING}$).

Bits	Access	Bit Name	Description
7:0	R/W	LDO4_OV_ THRESHOLD	Sets $V_{OUT4\_OV\_RISING}$, which is between 0.45V and 3.6375V, 12.5mV/step. $V_{OUT4\_OV\_RISING}$ is limited for V_{OUT4} and the LDO4 output OV hysteresis ($V_{OUT4\_OV\_HYS}$). To improve the accuracy of the parameters, the minimum $V_{OUT4\_OV\_RISING}$ must exceed the sum of the maximum V_{OUT4} and maximum $V_{OUT4\_OV\_HYS}$. $V_{OUT4\_OV\_RISING}$ can be calculated with the following equation: $V_{OUT4\_OV\_RISING}$ = 0.45V + 0.0125V x LDO4_OV_THRESHOLD

LDO4_UV_VTH (46h)

Format: Unsigned binary

POR Value: 0x00

The LDO4_UV_VTH command sets the LDO4 output voltage under-voltage (UV) falling threshold ($V_{OUT4\_UV\_FALLING}$).

Bits	Access	Bit Name	Description
7:0	R/W	LDO4_UV_ THRESHOLD	Sets $V_{OUT4\_UV\_FALLING}$, which is between 0.45V and 3.6375V, 12.5mV/step. $V_{OUT4\_UV\_FALLING}$ is limited for V_{OUT4} and the LDO4 output UV hysteresis ($V_{OUT4\_UV\_HYS}$). To improve the accuracy of the parameters, the maximum $V_{OUT4\_UV\_FALLING}$ must be below the difference between the minimum V_{OUT4} and maximum $V_{OUT4\_UV\_HYS}$. $V_{OUT4\_UV\_FALLING}$ can be calculated with the following equation: $V_{OUT4\_UV\_FALLING}$ = 0.45V + 0.0125V x LDO4_UV_THRESHOLD

LDO4_MODE (47h)

Format: Unsigned binary

POR Value: 0x00

The LDO4_MODE command sets the debounce time of the LDO4 UV and OV faults.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1:0	R/W	LDO4_DEBOUNCE	Sets the LDO4 UV and OV faults' debounce time. 2'b00: 10µs 2'b01: 20µs 2'b10: 40µs 2'b11: 80µs

LDO5_OV_VTH (48h)

Format: Unsigned binary

POR Value: 0xFF

The LDO5_OV_VTH command sets the LDO5 output voltage over-voltage (OV) rising threshold ($V_{OUT5\_OV\_RISING}$).

Bits	Access	Bit Name	Description
7:0	R/W	LDO5_OV_ THRESHOLD	Sets $V_{OUT5\_OV\_RISING}$, which is between 0.45V and 3.6375V, 12.5mV/step. $V_{OUT5\_OV\_RISING}$ is limited for V_{OUT5} and the LDO5 output OV hysteresis ($V_{OUT5\_OV\_HYS}$). To improve the accuracy of the parameters, the minimum $V_{OUT5\_OV\_RISING}$ must exceed the sum of the maximum V_{OUT5} and maximum $V_{OUT5\_OV\_HYS}$. $V_{OUT5\_OV\_RISING}$ can be calculated with the following equation: $V_{OUT5\_OV\_RISING}$ = 0.45V + 0.0125V x LDO5_OV_THRESHOLD

LDO5_UV_VTH (49h)

Format: Unsigned binary

POR Value: 0x00

The LDO5_UV_VTH command sets the LDO5 output voltage under-voltage (UV) falling threshold ($V_{OUT5\_UV\_FALLING}$).

Bits	Access	Bit Name	Description
7:0	R/W	LDO5_UV_ THRESHOLD	Sets $V_{OUT5\_UV\_FALLING}$, which is between 0.45V and 3.6375V, 12.5mV/step. $V_{OUT5\_UV\_FALLING}$ is limited for V_{OUT5} and the LDO5 output UV hysteresis ($V_{OUT5\_UV\_HYS}$). To improve the accuracy of the parameters, the maximum $V_{OUT5\_UV\_FALLING}$ must be below the difference between the minimum V_{OUT5} and maximum $V_{OUT5\_UV\_HYS}$. $V_{OUT5\_UV\_FALLING}$ can be calculated with the following equation: $V_{OUT5\_UV\_FALLING}$ = 0.45V + 0.0125V x LDO5_UV_THRESHOLD

LDO5_MODE (4Ah)

Format: Unsigned binary

POR Value: 0x00

The LDO5_MODE command sets the and debounce time of the LDO5 UV and OV faults.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1:0	R/W	LDO5_DEBOUNCE	Sets the LDO5 UV and OV faults' debounce time. 2'b00: 10µs 2'b01: 20µs 2'b10: 40µs 2'b11: 80µs

WDT_CFG (4Bh)

Format: Unsigned binary

POR Value: 0x00

The WDT_CFG command sets the watchdog configuration.

Bits	Access	Bit Name	Description
7	R/W	WDT_FAIL_POR	Enables whether the watchdog failure pulls the POR pin low. 1'b0: Disabled 1'b1: Enabled

6	R/W	WDT_MODE	Sets watchdog mode to window mode or Q&A mode. 1'b0: Window mode 1'b1: Q&A mode
5:4	R/W	WDT_EN	Enables the watchdog function and sets the watchdog fault limit. Once the watchdog fault count reaches the limit, the watchdog failure is reported. 2'b00: Disabled 2'b01: Enabled. The watchdog fault limit value is 2 2'b10: Enabled. The watchdog fault limit value is 4 2'b11: Enabled. The watchdog fault limit value is 8
3	R/W	WDT_SLP_EN	Enables the watchdog function when the MPQ70700FS is in sleep mode, sleep mode entry, or sleep mode exit. 1'b0: Disabled 1'b1: Enabled
2:0	R/W	WDTDLY	Sets the watchdog delay immediately after the watchdog function is enabled. If the watchdog is enabled by default, the watchdog delay time starts when the POR pin is pulled high. If the watchdog is disabled by default and POR is pulled high, then the watchdog delay time starts when the watchdog is enabled via the I^2C interface. The watchdog delay can be calculated with the following equation: Watchdog Delay = (RG_WDTDLY + 1) x (Open Window Time + Closed Window Time)

WDT_CLOSE (4Ch)

Format: Unsigned binary

POR Value: 0x00

The WDT_CLOSE command sets the watchdog's closed window time.

Bits	Access	Bit Name	Description
7:0	R/W	WDT_CLOSE_WIN	Sets the watchdog's closed window time, which is between 1ms and 864ms. Different settings of these bits have different formulas for calculating the closed window time, which can be divided into three cases: If the setting of these bits is between 8'b00000000 ~ 8'b00011111, then the closed window time can be calculated with the following equation: Closed Window Time = (WDT_CLOSE_WIN + 1) x 1ms If the setting of these bits is between 8'b00100000 ~ 8'b00111111, then the closed window time can be calculated with the following equation: Closed Window Time = 32ms + (WDT_CLOSE_WIN - 31) x 2ms If the setting of these bits is between 8'b01000000 ~ 8'b11111111, then the closed window time can be calculated with the following equation: Closed Window Time = 96ms + (WDT_CLOSE_WIN - 63) x 4ms

WDT_OPEN (4Dh)

Format: Unsigned binary

POR Value: 0x00

The WDT_OPEN command sets the watchdog's open window time.

Bits	Access	Bit Name	Description
7:0	R/W	WDT_OPEN_WIN	Sets the watchdog's open window time, which is between 1ms and 864ms. Different settings of these bits have different formulas for calculating the open window time, which can be divided into three cases: If the setting of these bits is between 8'b00000000 ~ 8'b00011111, then the open window time can be calculated with the following equation: Open Window Time = (WDT_OPEN_WIN + 1) x 1ms If the setting of these bits is between 8'b00100000 ~ 8'b00111111, then the open window time can be calculated with the following equation: Open Window Time = 32ms + (WDT_OPEN_WIN - 31) x 2ms If the setting of these bits is between 8'b01000000 ~ 8'b11111111, then the open window time can be calculated with the following equation: Open Window Time = 96ms + (WDT_OPEN_WIN - 63) x 4ms

WDT_QA_CFG (4Eh)

Format: Unsigned binary

POR Value: 0x00

The WDT_QA_CFG command configures the Q&A mode watchdog.

Bits	Access	Bit Name	Description
7:5	R/W	WDT_FDBK	Controls the sequence of the generated questions and the corresponding answers.
4:0	R/W	WDT_SEED	Watchdog token seed value. These bits generate a set of new questions.

WDT_TEST (4Fh)

Format: Unsigned binary

POR Value: 0x00

The WDT_TEST command clears the watchdog fault count.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1	R/W	WDT_FAULT_CLR	If 1'b1 is written to this bit, then the watchdog fault count is reset to 0. This bit is not reset to 0 automatically. If this bit remains set to 1, then the watchdog fault count remains at 0. 1'b0: Does not clear the watchdog fault count to 0 1'b1: Clears the watchdog fault count to 0
0	R/W	RESERVED	Reserved.

WDTKEY (50h)

Format: Unsigned binary

POR Value: 0x00

The WDTKEY command receives and stores the watchdog key.

Bits	Access	Bit Name	Description
7:0	R/W	WDT_KEY	Receives and stores the watchdog key.

I2C_ADDRESS (51h)

Format: Unsigned binary

POR Value: 0x08

The I2C_ADDRESS command sets the I²C address.

Bits	Access	Bit Name	Description
7	R/W	I2C_ADDRESS_LSB_CFG	The low 2 least significant bits (LSB) I²C target address is determined by the ADDR pin. 1'b0: I²C address = I2C_ADDRESS_NVM x 4 + I2C_ADDRESS_PIN Others: Invalid.
6:2	R/W	I2C_ADDRESS_NVM	The high 5LSB I²C target address.
1:0	R	I2C_ADDRESS_PIN	Obtains the low 2LSB I²C target address by pulling up or pulling down the ADDR pin. 2'b00: The ADDR pin is connected to GND 2'b01: The ADDR pin is connected to GND via a 100kΩ resistor 2'b10: The ADDR pin is connected to VIN1 via a 100kΩ resistor 2'b11: The ADDR pin is connected to VIN1

I2C_CONFIG (52h)

Format: Unsigned binary

POR Value: 0x00

The I2C_CONFIG command enables the I²C packet error checking (PEC) function.

Bits	Access	Bit Name	Description
7:1	R/W	RESERVED	Reserved.
0	R	I2C_PEC_EN	Enables the I²C PEC function. 1'b0: Disabled 1'b1: Enabled

I2C_IO_CTL (53h)

Format: Unsigned binary

POR Value: 0x01

The I2C_IO_CTL command disables the I²C function in normal idle state to decrease the quiescent current (I_Q).

Bits	Access	Bit Name	Description
7:1	R/W	RESERVED	Reserved.
0	R	I2C_IO_EN	In normal idle state, 1'b0 can be written to this bit to disable the I²C PEC function, which decreases I_Q. The I²C PEC function is only enabled again once the MPQ70700FS enters power-on state. 1'b0: Disabled. This bit can only be written in normal idle state 1'b1: Enabled. Cannot support writing to this bit

WDT_STATUS1 (54h)

Format: Unsigned binary

POR Value: 0x00

The WDT_STATUS1 command indicates the watchdog status, including the watchdog answer to be written, watchdog state, and the watchdog fault count.

Bits	Access	Bit Name	Description
7:6	R	WDT_ANSW_CNT	In a watchdog sequence, these bits determine which watchdog answer must be written. 2'b00: Watchdog answer 0 must be written 2'b01: Watchdog answer 1 must be written 2'b10: Watchdog answer 2 must be written 2'b11: Watchdog answer 3 must be written
5:4	R	WDT_STATE	Indicates the watchdog state. 2'b00: Idle 2'b01: Closed window 2'b10: Open window Other: Invalid command
3:0	R	WDT_ACT_STATE	Indicates the watchdog fault count. The maximum watchdog fault count is 8. If the watchdog fault count reaches the limit (8), then the MPQ70700FS reports a watchdog failure. The watchdog enters idle state, and the watchdog fault count resets to 0. This means the watchdog fault count may not be 8, and the maximum watchdog fault that can be read via the I^2C interface is 7. Watchdog Fault Count = MIN(WDT_ACT_STATE, 8)

WDT_STATUS2 (55h)

Format: Unsigned binary

POR Value: 0x00

The WDT_STATUS2 command indicates the watchdog status, including the watchdog Q&A question token, watchdog Q&A answer 0 token error, watchdog Q&A answer token error, and watchdog closed/open window time configuration.

Bits	Access	Bit Name	Description
7:3	R	WDT_TOKEN	Watchdog Q&A question token.
2	R	WDT_ANS0_ERR_SRC	Watchdog Q&A answer 0 token error. After the initiator device reads the WDT_STATUS2 (55h) command, this bit is cleared. 1'b0: Answer 0 byte is correct 1'b1: Answer 0 byte is wrong
1	R	WDT_TOKEN_ERR_SRC	Any WDT Q&A answer token error. After the initiator device reads the WDT_STATUS2 (55h) command, this bit is cleared. 1'b0: The answer byte is correct 1'b1: The answer byte is wrong
0	R	WDT_CFG_CHG_SRC	Changes in the watchdog closed/open window time configuration. After the initiator device reads the WDT_STATUS2 (55h) command, this bit is cleared. 1'b0: The watchdog closed/open window time does not change 1'b1: The watchdog closed/open window time changes

WDT_STATUS3 (56h)

Format: Unsigned binary

POR Value: 0x00

The WDT_STATUS3 command indicates the watchdog status, including the watchdog Q&A question token, watchdog update window, watchdog violation detection, and watchdog timer expiry.

Bits	Access	Bit Name	Description
7:3	R	WDT_TOKEN	Watchdog Q&A question token.
2	R	WDT_WIN_OPEN	Indicates whether the watchdog update window is open or closed. 1'b0: The watchdog update window is closed 1'b1: The watchdog update window is open
1	R	WDT_UPDATE_VIO	Indicates whether an watchdog update violation occurs. After the initiator device reads the WDT_STATUS3 (56h) command, this bit is cleared. 1'b0: No violation detected 1'b1: The watchdog updates too early
0	R	WDT_EXPIRE	The watchdog timer expires without update to the WDTKEY register. After the initiator device reads the WDT_STATUS3 (56h) command, this bit is cleared. 1'b0: Not expired 1'b1: Expired

BIST_STATUS (57h)

Format: Unsigned binary

POR Value: 0x00

The BIST_STATUS command indicates the watchdog status state.

Bits	Access	Bit Name	Description
7	R	RESERVED	Reserved.
6:5	R	ABIST_LDOOC_ FAIL_CNT	Indicates the ABIST LDO over-current (OC) failure count status.
4:3	R	ABIST_COMP_FAIL_ CNT	Indicates the ABIST comparator's flip-fail count status.
2:1	R	LBIST_FAIL_CNT	Indicates the LBIST fail count status.
0	R	LBIST_DONE	Indicates LBIST complete.

FORCE_EXIT_FS (58h)

Format: Unsigned binary

POR Value: 0x00

The BIST_STATUS command indicates the watchdog status, including exiting failsafe state.

Bits	Access	Bit Name	Description
7:1	R	RESERVED	Reserved.
0	R1C/W	FORCE_EXIT_FS	Write 1 to this bit to force the device to exit failsafe state and enter normal state. This bit resets to 0 automatically after writing 1.

APPLICATION INFORMATION

Figure 44 shows the typical application circuit for the MPQ70700FS.

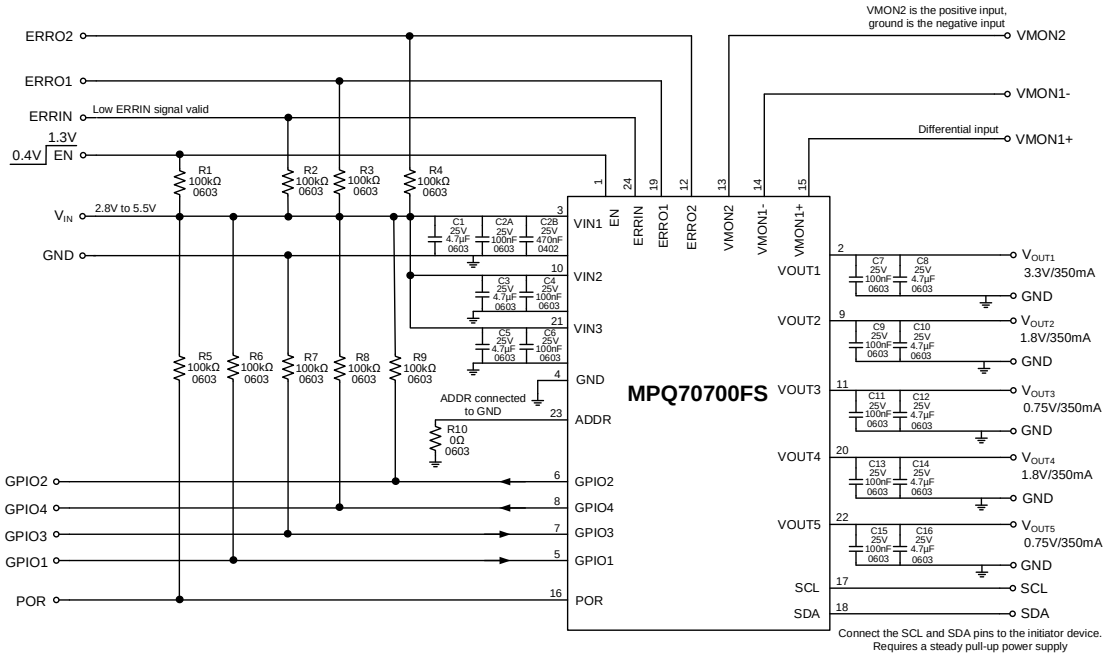


Figure 44: Typical Application Circuit (ADDR Connected to GND, Low Valid ERRIN Signal, GPIO1 and GPIO3 as Inputs Connected to GND, V_{OUT1} = 3.3V, V_{OUT2} = 0.75V, V_{OUT3} = 1.2V, V_{OUT4} = 0.75V, and V_{OUT5} = 1.2V,)

Table 6 shows the design guide index.

Table 6: Design Guide Index

Pin #	Name	Components	Design Guide Index
1	EN	R1	Enable (EN, Pin 1)
2	VOUT1	C7, C8	Selecting the Output Capacitors for LDO (VOUT1, Pin 2; VOUT2, Pin 9; VOUT3, Pin 11; VOUT4, Pin 20; VOUT5, Pin 22)
3	VIN1	C1, C2A, C2B	Selecting the Input Capacitors (VIN1, Pin 3; VIN2, Pin 10; VIN3, Pin 21)
4	GND	-	Ground Connection (GND, Pin 4)
5	GPIO1	R6	Setting GPIO1 and GPIO3 as the Input/Output (GPIO1, Pin 5; GPIO3, Pin 7)
6	GPIO2	R8	Setting GPIO2 and GPIO4 as the Output (GPIO2, Pin 6; GPIO4, Pin 8)
7	GPIO3	R7	Setting GPIO1 and GPIO3 as the Input/Output (GPIO1, Pin 5; GPIO3, Pin 7)
8	GPIO4	R9	Setting GPIO2 and GPIO4 as the Output (GPIO2, Pin 6; GPIO4, Pin 8)
9	VOUT2	C9, C10	Selecting the Output Capacitors for LDO (VOUT1, Pin 2; VOUT2, Pin 9; VOUT3, Pin 11; VOUT4, Pin 20; VOUT5, Pin 22)
10	VIN2	C3, C4	Selecting the Input Capacitors (VIN1, Pin 3; VIN2, Pin 10; VIN3, Pin 21)
11	VOUT3	C11, C12	Selecting the Output Capacitors for LDO (VOUT1, Pin 2; VOUT2, Pin 9; VOUT3, Pin 11; VOUT4, Pin 20; VOUT5, Pin 22;)
12	ERRO2	R4	Error Output Indicator (ERRO2, Pin 12; ERRO1, Pin 19)
13	VMON2	-	Voltage Monitor (VMON2, Pin 13; VMON1-, Pin 14; VMON1+, Pin 15)
14	VMON1-	-	Voltage Monitor (VMON2, Pin 13; VMON1-, Pin 14; VMON1+, Pin 15)
15	VMON1+	-	Voltage Monitor (VMON2, Pin 13; VMON1-, Pin 14; VMON1+, Pin 15)
16	POR	R5	Power-On Reset (POR, Pin 16)
17	SCL	-	I^2C Interface (SCL, Pin 17; SDA, Pin 18)
18	SDA	-	I^2C Interface (SCL, Pin 17; SDA, Pin 18)

Table 6: Design Guide Index *(continued)*

Pin #	Name	Components	Design Guide Index
19	ERRO1	R3	Error Output Indicator (ERRO2, Pin 12; ERRO1, Pin 19)
20	VOUT4	C13, C14	Selecting the Output Capacitors for LDO (VOUT1, Pin 2; VOUT2, Pin 9; VOUT3, Pin 11; VOUT4, Pin 20; VOUT5, Pin 22)
21	VIN3	C5, C6	Selecting the Input Capacitors (VIN1, Pin 3; VIN2, Pin 10; VIN3, Pin 21)
22	VOUT5	C15, C16	Selecting the Output Capacitors for LDO (VOUT1, Pin 2; VOUT2, Pin 9; VOUT3, Pin 11; VOUT4, Pin 20; VOUT5, Pin 22)
23	ADDR	R10	Selecting the Resistor for the I²C Address (ADDR, Pin 23)
24	ERRIN	R2	Error Input Signal (ERRIN, Pin 24)

Enable (EN, Pin 1)

The EN pin can enable and disable all GPIO and LDO outputs. Pull the EN below its falling threshold ($V_{IL\_EN\_F}$) (0.4V) to shut down all outputs. Pull EN above its rising threshold ($V_{IH\_EN\_R}$) (1.3V) to enable all GPIO and LDO outputs.

There are separate dedicated register bits via bits[4:0] of the CHANNEL_EN (18h) command to enable the software for all the LDOs (LDO1, LDO2, LDO3, LDO4, and LDO5). The physical EN pin has a higher priority than the software enable function.

The MPQ70700FS provides an internal, fixed under-voltage lockout (UVLO) threshold. In the normal input voltage (V_{INx}) (where x = 1 to 3) range, the rising threshold is 2.8V, and the falling threshold is 2.6V.

The MPQ70700FS does not have a reaction for start-up or shutdown through EN during power-on/power-off and sleep mode exit/entry. This means the shutdown through EN time should be longer than 16 x time slot when starting up and shutting down EN quickly.

Selecting the Output Capacitors for LDO (VOUT1, Pin 2; VOUT2, Pin 9; VOUT3, Pin 11; VOUT4, Pin 20; VOUT5, Pin 22)

For stable operation, place a 3.3µF to 22µF, ceramic capacitor with X5R or X7R dielectrics between the VOUT pin and ground. Output capacitors (C_{OUTx}) (where x = 1 to 5) of other dielectric types may be used, but they are not recommended as their capacitance can deviate greatly from their rated value across different temperatures.

Larger-value capacitors improve line transient response and reduce noise. For LDO, a larger C_{OUTx} means that the MPQ70700FS must provide a larger charge current during the soft-start period. As such, C_{OUTx} selection should consider the output voltage (V_{OUTx}) (where x = 1 to 5) soft-start (SS) slew rate (V_{OUTx_SS}), minimum output current limit ($I_{OUTx\_LIMIT\_MIN}$) (where x = 1 to 5) and load current (I_{LOAD}). The maximum allowable effective LDO1 output capacitance (C_{OUT1}) can be calculated with Equation (1):

$$C_{OUT1} = \frac{I_{OUT1\_LIMIT\_MIN} - I_{LOAD1}}{V_{OUT1\_SS}} \quad (1)$$

For example, if V_{OUT1_SS} = 20mV/µs, $I_{OUT1\_LIMIT\_MIN}$ = 420mA, and I_{LOAD1} = 320mA, then the maximum allowable effective C_{OUT1} should be 5µF.

If the calculated maximum C_{OUTx} is less than 3.3µF, then V_{OUTx_SS} should be reduced to increase the maximum C_{OUTx}. If the calculated maximum C_{OUTx} exceeds 22µF, then the actual C_{OUTx} should not exceed 80% of the calculated maximum C_{OUTx}.

Selecting the Output Voltage for LDO

The V_{OUTx} range is between 0.5V and 3.6V. The MPQ70700FS provides a different voltage step depending on V_{OUTx}. If MODE = 0, then the voltage step is 12.5mV, and the V_{OUTx} range is between 0.5V and 1.0375V. If MODE = 1, then the voltage step is 50mV, and the V_{OUTx} range is between 1V and 3.6V. As such, when setting V_{OUTx}, select MODE via the LDOx_VREF_MODE bit (where x = 1 to 5) (21h, 24h, 27h, 2Ah, 2Dh, bit[6]), then set V_{OUTx} via the LDOx_VREF bits (where x = 1 to 5) (21h, 24h, 27h, 2Ah, 2Dh, bits[5:0]).

For example, to set V_{OUT2} to 3.3V, follow the below steps:

1. Set the LDO2_VREF_MODE bit (24h, bit[6]) to MODE1, 50mV/step.

2. According to the formula of the LDO2_VREF bits (24h, bits[5:0]), the LDO2 reference voltage (V_{REF2}) should be equal to 5'b101110 when V_{OUT2} is 3.3V.
3. Set V_{OUT2} to 3.3V via the LDO2_VREF bits.

Selecting the Input Capacitors (VIN1, Pin 3; VIN2, Pin 10; VIN3, Pin 21)

For efficient operation, place a ceramic capacitor with dielectrics (X5R or X7R) between the VINx pin (where x = 1 to 3) and ground. The capacitor is recommended to be between 1µF and 10µF. Larger-value capacitors improve the line transient response.

For VIN1, a 470nF, 0402 capacitor should be placed between the VIN1 and GND pins, as close to the IC as possible in the layout. Meanwhile, for lower ambient temperatures (T_A), a lower V_{INx} is recommended to be applied to start-up.

Setting GPIO1 and GPIO3 as the Input/Output (GPIO1, Pin 5; GPIO3, Pin 7)

GPIO1 and GPIO3 can be configured as an output pin or input pin via the GPIO_CFG (1Bh) command. When GPIO and GPIO3 are configured as output pins, connect them to a stable power supply (e.g. V_{OUT1}) via a pull-up resistor (e.g. 100kΩ).

If GPIO1 is configured as the input pin, then pull GPIO1 above its input high threshold (V_{IH_GPIO1}) (1.3V) to make the MPQ70700FS enter sleep mode. Pull GPIO1 below its input low threshold (V_{IL_GPIO1}) (0.4V) to make MPQ70700FS exit sleep mode.

If GPIO3 is configured as an input pin, then GPIO3 is used to control V_{OUT1} instead of using the VREF_LDO1 (21h) command. Pull GPIO3 above its input high threshold (V_{IH_GPIO3}) (1.3V) to set V_{OUT1} to 1.8V. Pull GPIO3 below its input low threshold (V_{IL_GPIO3}) (0.4V) to set V_{OUT1} to 3.3V.

If GPIO1 and GPIO3 are not used, then configure these pins as outputs, and connect them to GND.

Setting GPIO2 and GPIO4 as the Output (GPIO2, Pin 6; GPIO4, Pin 8)

GPIO2 and GPIO4 are the output pins. Connecting GPIO2 and GPIO4 to a stable power supply (e.g. V_{OUT1}) via a pull-up resistor (e.g. 100kΩ). If GPIO2 and GPIO4 are not used, then connect them to GND.

In the PCB layout, a ground wire should be placed between the two adjacent GPIO signals. This avoids crosstalk when the GPIO signal level changes.

Error Output Indicator (ERRO2, Pin 12; ERRO1, Pin 19)

ERRO1 and ERRO2 are open-drain output pins. Connect ERRO1 and ERRO2 to a stable power supply (e.g. V_{IN1}) via a pull-up resistor (e.g. 100kΩ).

ERRO2 can indicate an ERRIN fault and watchdog failure. ERRO1 can indicate other faults.

Voltage Monitor (VMON2, Pin 13; VMON1-, Pin 14; VMON1+, Pin 15)

The MPQ70700FS provides two voltage monitors (VMON1 and VMON2). VMON1 is a differential input, and VMON2 is a single input. For VMON1, the negative V_{INx} must be below 0.3V. If the VMON1- pin exceeds 0.3V, then the internal diode may turn on, which results in an incorrect internal VMON1 sense voltage. As such, it is recommended to connect VMON1- to GND.

VMON1 and VMON2 can be enabled via the MON1_EN bit (38h, bit[6]) and MON2_EN bit (3Bh, bit[6]. The VMON1/2 over-voltage (OV) and under-voltage (UV) thresholds are also set via the MON1_OV_VTH (36h), MON2_OV_VTH (39h), MON1_UV_VTH (37h), and MON2_UV_VTH (3Ah) commands. If VMON1 or VMON2 is not used, then disable the corresponding pins (VMON1-, VMON1+, and VMON2, respectively), and connect the pins to GND.

Power-On Reset (POR, Pin 16)

The POR pin is an open-drain output, and can indicate whether all V_{OUTx} are good after the power-on sequence. In addition, the POR pin can indicate a watchdog failure and ERRIN fault. This means the system can use the POR pin to reset.

Connecting the POR pin to a stable power supply (e.g. V_{IN1}) via a pull-up resistor (e.g. 100kΩ).

Error Input Signal (ERRIN, Pin 24)

ERRIN is an error input pin. If the ERRIN pin voltage (V_{ERRIN}) is not the expected value, then the MPQ70700FS can pull up ERRO2 and reset the POR pin. This helps the system to reset if a fault occurs, and the fault is sent to the ERRIN pin.

The ERRIN_MODE pin (14h, bit[6]) can set whether the signal received by ERRIN is a high or low valid signal. Pulling ERRIN above the error input high threshold (V_{IH_ERRIN}) (1.3V) means the ERRIN signal is high. Pulling GPIO3 below V_{IL_GPIO3} (0.4V) means the ERRIN signal is low. If the ERRIN pin is not used, pull the pin to a high valid signal, then connect it to GND.

I²C Interface (SCL, Pin17; SDA, Pin 18)

The MPQ70700FS's interface is an I²C target that supports up to 1Mbs of bidirectional data transfer in fast-mode plus, which adds flexibility to the sequencer.

If the I²C interface is not used, it is recommended to connect the SDA and SCL pins to VIN1 via a resistor (e.g. 100kΩ).

Selecting the Resistor for the I²C Address (ADDR, Pin 23)

The MPQ70700FS supports 127 addresses. The low 2 least significant bit (LSB) I²C address can be determined by detecting the voltage on the ADDR pin (V_{ADDR}). Table 5 on page 61 shows the resistance and the pin connections for different I²C addresses. The resistor tolerance should not exceed 1% of the recommended resistance.

Ground Connection (GND, Pin4)

See the PCB Layout Guidelines section on page 112 for more details.

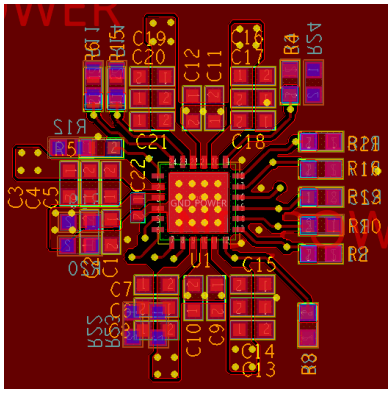
PCB Layout Guidelines [20]

Efficient PCB layout (especially the input capacitor, boost output capacitor, inductor, and Schottky diode placement) is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 45 and follow the guidelines below:

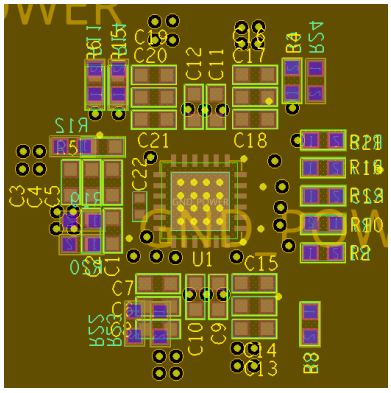
1. Place the 470nF, 0402 input capacitor (C_{IN}) as close to the VIN1 and GND pins as possible.
2. Place another C_{IN} as close to the VIN1, VIN2, and VIN3 pins as possible.
3. Use a large ground plane to connect to GND.
4. Add vias near PGND if the bottom layer is a ground plane.
5. Ensure that the high-current paths (e.g. GND and VIN) have short, direct, and wide traces.
6. Place the input/output bypass capacitor, especially the small package size (0603), as close as possible to the VIN, VOUT, and GND pins to minimize high frequency.
7. Keep the connection between C_{IN} and the VIN1, VIN2, and VIN3 pins as short and wide as possible.
8. Place a ground wire between two adjacent GPIO signals.
9. Use multiple vias to connect the power planes to the internal layers.

Note:

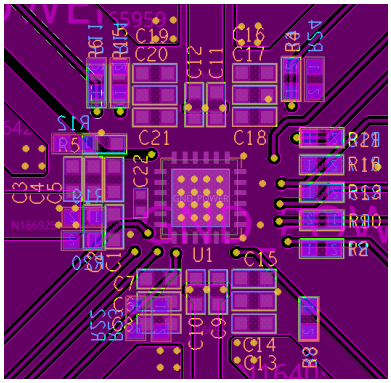
20) The recommended PCB layout is based on the typical application circuit (see Figure 46 on page 113).



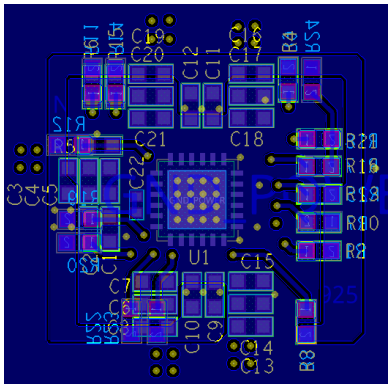
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 45: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

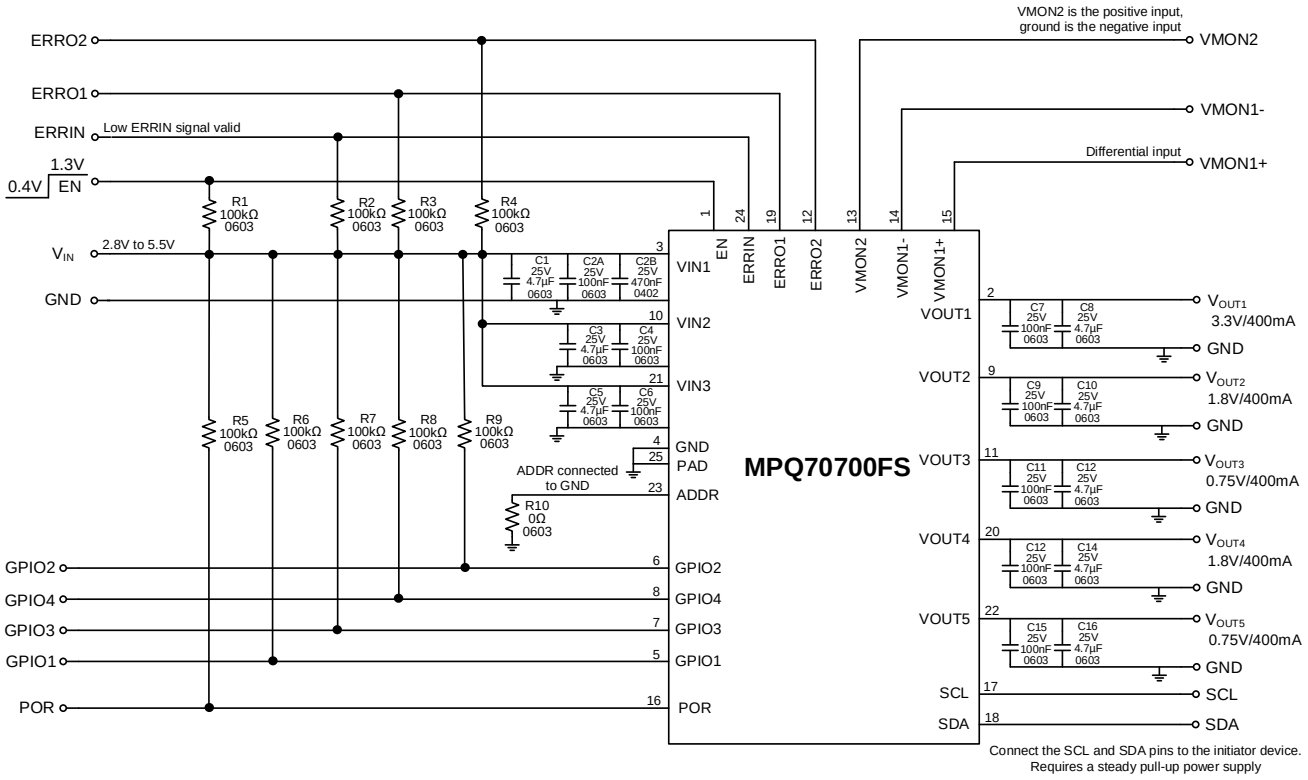


Figure 46: Typical Application Circuit (ADDR Connected to GND, Low Valid ERRIN Signal, and All GPIOs as Output Pins)

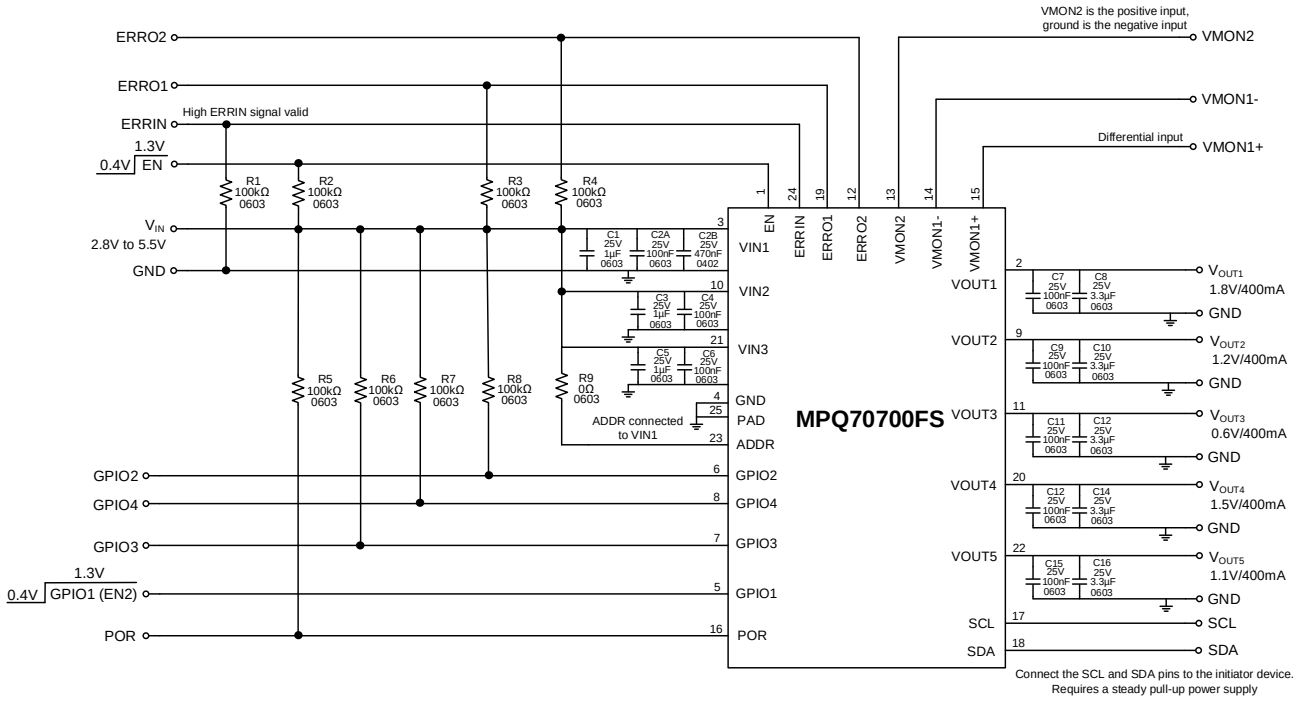
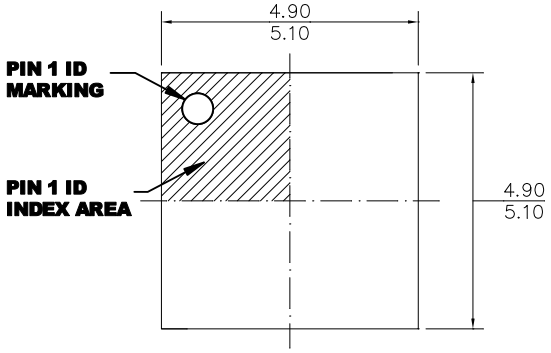


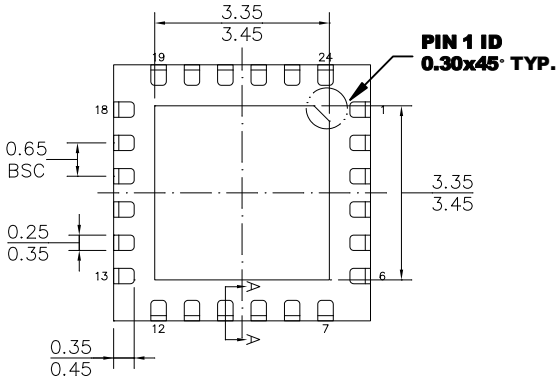
Figure 47: Typical Application Circuit (ADDR Connected to VIN1, High Valid ERRIN Signal, GPIO2 and GPIO4 as Output Pins, and GPIO1 and GPIO3 as Input Pins)

PACKAGE INFORMATION

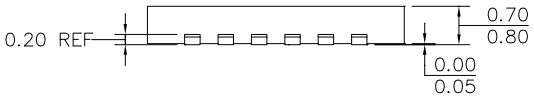
TQFN-24 (5mmx5mm)
Wettable Flanks



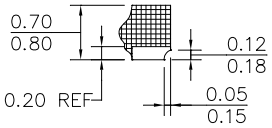
TOP VIEW



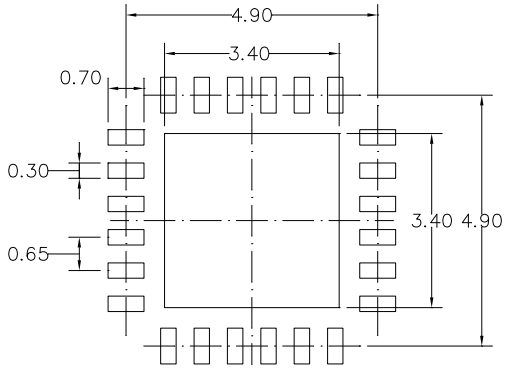
BOTTOM VIEW



SIDE VIEW



SECTION A-A

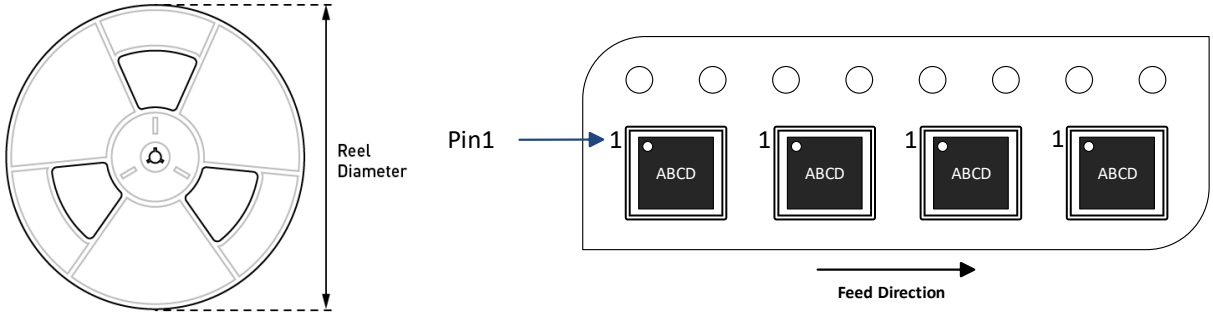


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION (21)



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ70700FSGUTE-xxxxAEC1-Z	TQFN-24 (5mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

Note:

21) N/A indicates “not available” in tubes. For 500-piece tape & reel prototype quantities, see factory. (The order code for a 500-piece of a partial reel is “-P,” and the tape & reel dimensions are the same as the full reel.)

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/30/2025	Initial Release	-