



MP6638

16V, 1.7A Peak, Three-Phase, Sensorless BLDC Motor Driver with Integrated MOSFETs

DESCRIPTION

The MP6638 is a three-phase sensorless, brushless DC (BLDC) motor driver with integrated power MOSFETs. It features sinusoidal sensorless control for improved efficiency and low vibration, with up to 1.7A of peak phase current. The input voltage (V_{IN}) ranges from 2.5V to 16V.

The MP6638 controls the motor speed via the pulse-width modulation (PWM) signal with a 50Hz to 100kHz PWM input frequency.

The MP6638 also features rotational speed detection. The rotational speed detector is an open-drain output via the FG/RD pin.

Rich protections include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown protection.

The MP6638 is available in a UTQFN-8 (2mmx2.5mm) package.

FEATURES

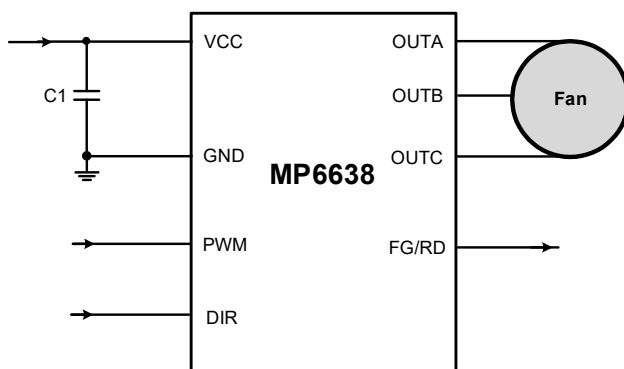
- 2.5V to 16V Input Voltage (V_{IN}) Operating Range
- Up to 1.7A Peak Phase Current
- Up to 1.2A Root Mean Square (RMS) Phase Current
- Sinusoidal Sensorless Control
- Integrated 330m Ω High-Side MOSFETs (HS-FETs) and Low-Side MOSFETs (LS-FETs)
- Supports 50Hz to 100kHz Pulse-Width Modulation (PWM) Input
- Power-Save Mode
- 30kHz PWM Output Frequency
- Direction Control
- Selectable 1x, 1/2x, 1/3x FG or RD Output
- Over-Current Protection (OCP)
- Maximum Peak Current Protection
- Over-Voltage Protection (OVP)
- Locked-Rotor Protection
- Thermal Shutdown Protection
- Available in a UTQFN-8 (2mmx2.5mm) Package

APPLICATIONS

- Gaming Fans
- Notebook Fans
- Pumps
- Three-Phase BLDC Motors

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TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6638GRPU-xxxx**	UTQFN-8 (2mmx2.5mm)	See Below	1

* For Tape & Reel, add suffix -Z (e.g. MP6638GRPU-xxxx-Z).

** “xxxx” is the configuration code identifier. The first four digits of the suffix (xxxx) can be a hexadecimal value between 0 and F. The default code is “-0000.” Work with an MPS FAE to create a unique number for non-default function options.

TOP MARKING

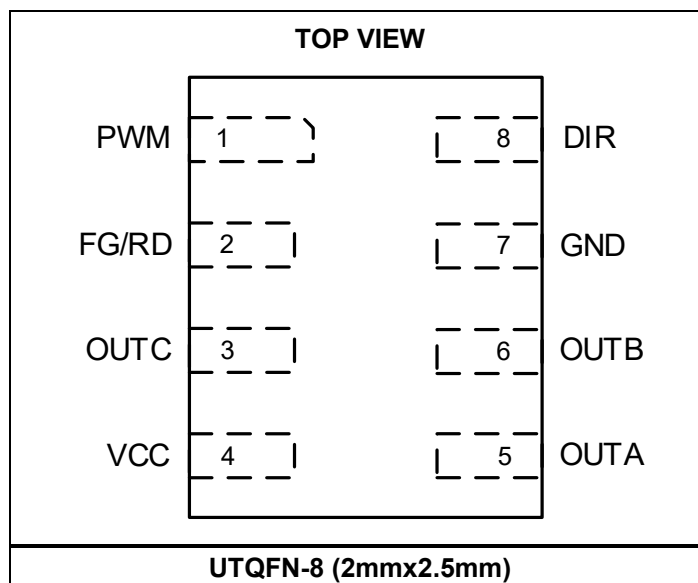
NUY
LLL

NU: Product code

Y: Year

LLL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	PWM	Speed control input. A pulse-width modulation (PWM) signal is applied on the PWM pin, where the PWM signal's duty cycle controls the motor speed. The PWM pin supports a 50Hz to 100kHz PWM input frequency, and it is internally pulled high.
2	FG/RD	Speed indicator (FG) or locked-rotor indicator (RD) output. The FG/RD pin is an open-drain output, and must be externally pulled up.
3	OUTC	Phase C terminal.
4	VCC	Input voltage supply. A bypass capacitor is essential in application. Place the capacitor as close to the VCC and GND pins as possible.
5	OUTA	Phase A terminal.
6	OUTB	Phase B terminal.
7	GND	Ground.
8	DIR	Rotation direction control. Pull the DIR pin high for reverse rotation, where $A \rightarrow C \rightarrow B$; pull DIR low for forward rotation, where $A \rightarrow B \rightarrow C$. To avoid noise injection, it is not recommended to float this pin in application.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

VCC, PWM, FG/RD, DIR -0.3V to +18V
OUTA, OUTB, OUTC -0.3V to $V_{CC} + 0.3V$
Junction temperature (T_J) 150°C
Lead temperature 260°C
Continuous power dissipation ($T_A = 25^\circ C$) ⁽²⁾
..... 1.7W
Storage temperature -60°C to +150°C

ESD Ratings

Human body model (HBM) 2kV
Charged-device model (CDM) 750V

Recommended Operating Conditions ⁽³⁾

Supply voltage (V_{IN}) 2.5V to 16V
Operating junction temp (T_J) -40°C to +125°C

Thermal Resistance ⁽⁴⁾ θ_{JA} θ_{JC}
UTQFN-8 (2mmx2.5mm) 70 15... °C/W

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA} , and the ambient temperature, T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = $(T_J$ (MAX) - T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation can generate an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, a 4-layer PCB.

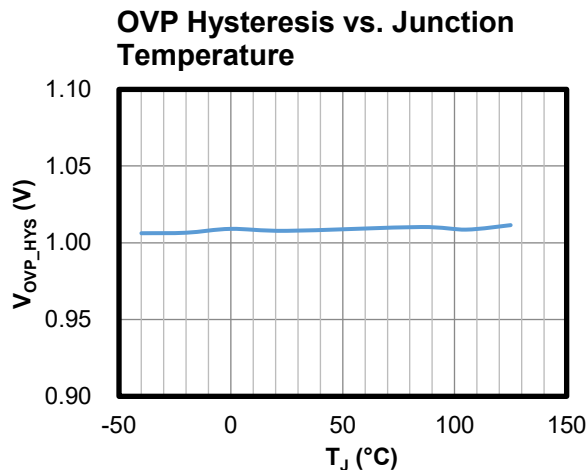
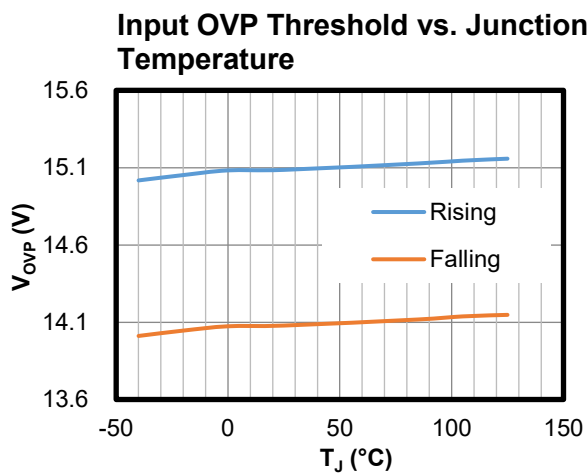
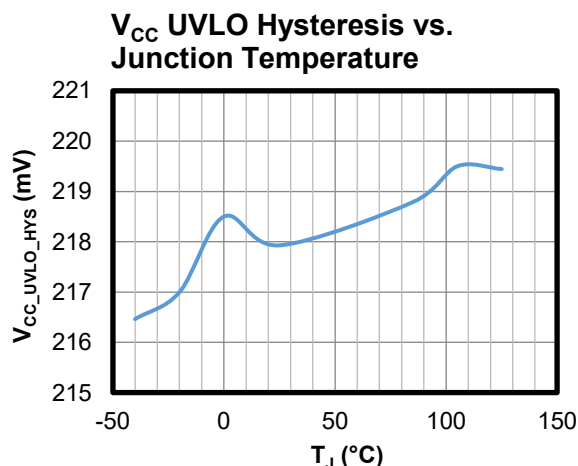
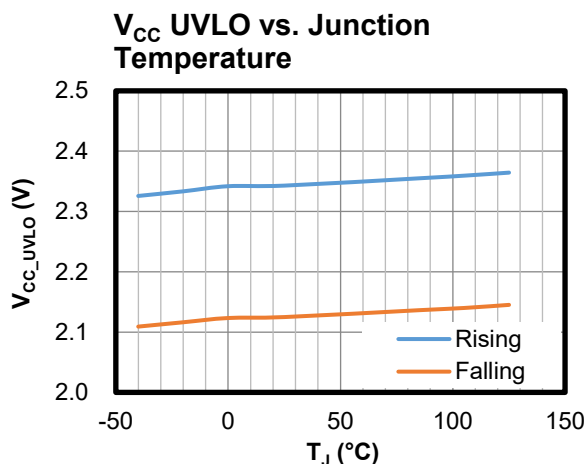
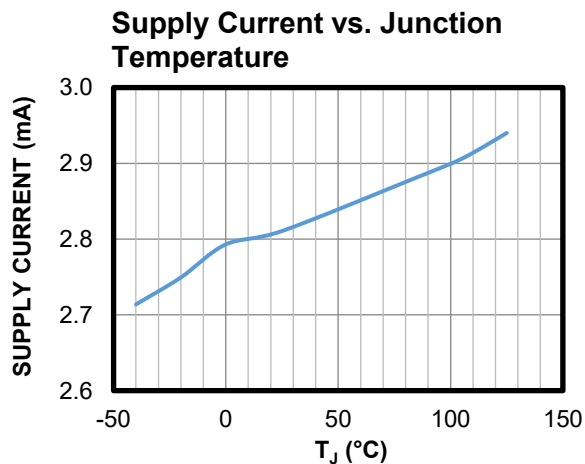
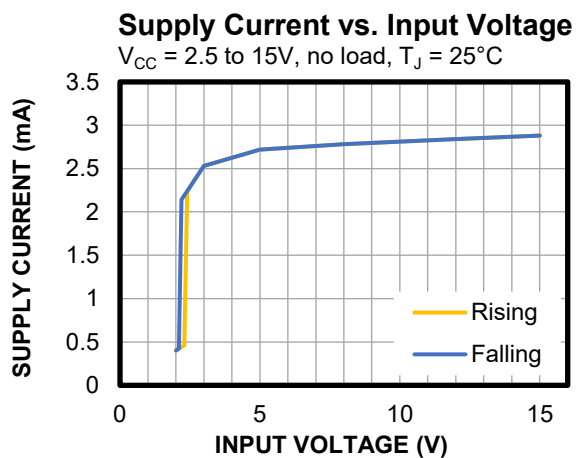
ELECTRICAL CHARACTERISTICS

$V_{CC} = 12V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input under-voltage lockout (UVLO) rising threshold	V_{UVLO}			2.3	2.45	V
Input UVLO hysteresis	V_{UVLO_HYS}			0.2		V
Operating supply current	I_{CC}	Float PWM, no load		2.8		mA
Standby current	I_{ST}	PWM low		92	150	μA
PWM input high voltage	V_{PWMH}		2			V
PWM input low voltage	V_{PWML}				0.8	V
PWM input internal pull-up resistance	R_{PWM}			50	100	k Ω
DIR input high voltage	V_{DIRH}		2			V
DIR input low voltage	V_{DIRL}				0.8	V
DIR internal pull-down resistance	R_{DIR}			50	100	k Ω
Switching frequency	f_{SW}			30		kHz
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$			170		m Ω
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$			160		m Ω
Over-current protection (OCP) threshold	I_{OCP}			1.7		A
Maximum peak current threshold	I_{SCP}			2.2		A
FG/RD output low-level voltage	V_{FG_L}	$I_{FG/RD} = 3mA$			0.35	V
Locked-rotor retry time	t_{RE}			4.4		s
Input over-voltage protection (OVP) threshold	V_{OVP}			15		V
OVP hysteresis	V_{OVP_HYS}			1		V
Thermal shutdown threshold	T_{SD}			160		$^{\circ}C$
Thermal shutdown hysteresis	T_{SD_HYS}			25		$^{\circ}C$

TYPICAL CHARACTERISTICS

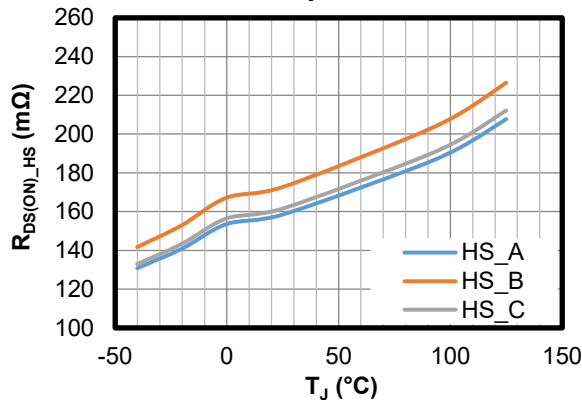
$V_{CC} = 12V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted.



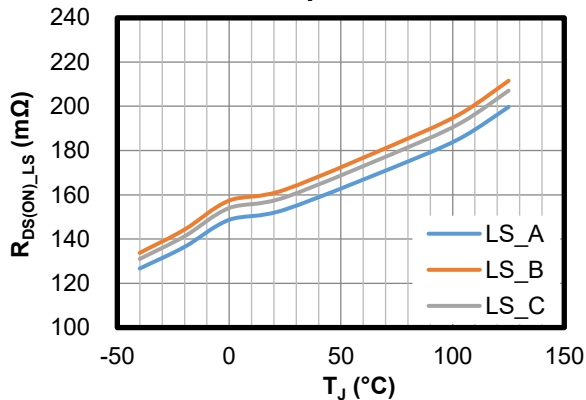
TYPICAL CHARACTERISTICS *(continued)*

$V_{CC} = 12V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted.

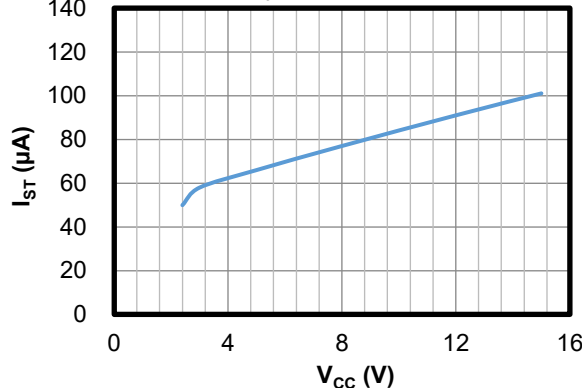
HS-FET On Resistance vs. Junction Temperature



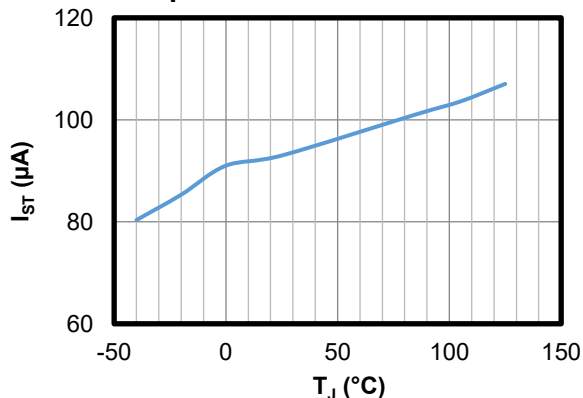
LS-FET On Resistance vs. Junction Temperature



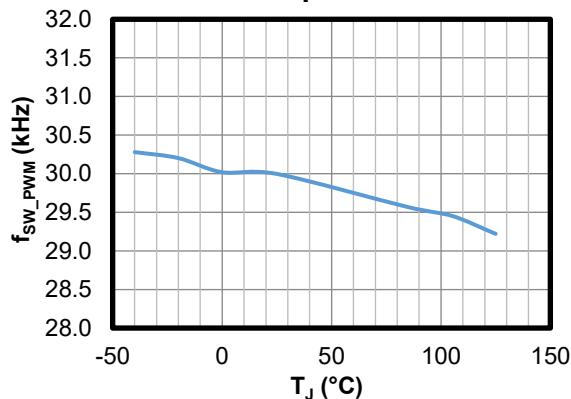
Standby Current vs. Input Voltage
PWM = low, $T_J = 25^{\circ}C$



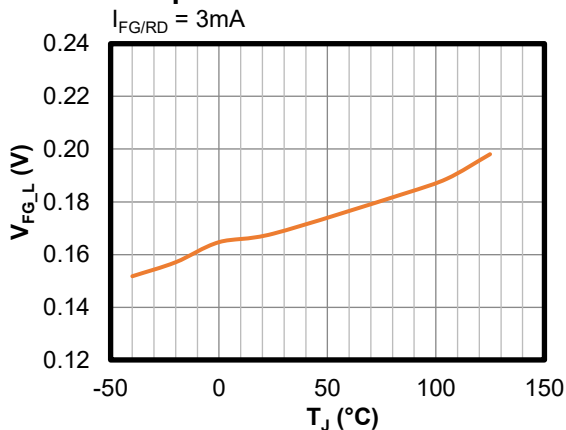
Standby Current vs. Junction Temperature



PWM Output Frequency vs. Junction Temperature



FG/RD Output Low-Level Voltage vs. Junction Temperature
 $I_{FG/RD} = 3mA$

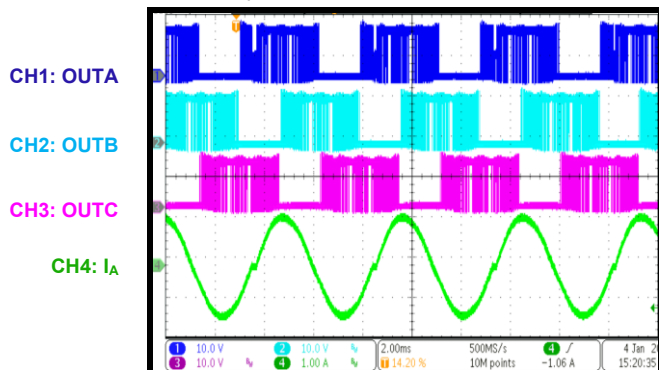


TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. $V_{IN} = 12V$, PWM frequency = 20kHz, $T_A = 25^{\circ}C$, unless otherwise noted.

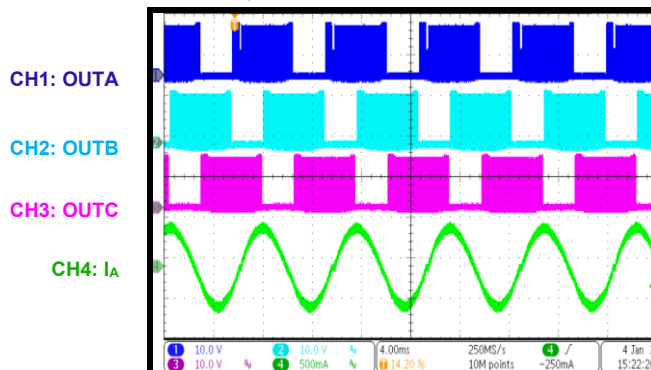
Steady State

PWM duty = 100%, DIR = low



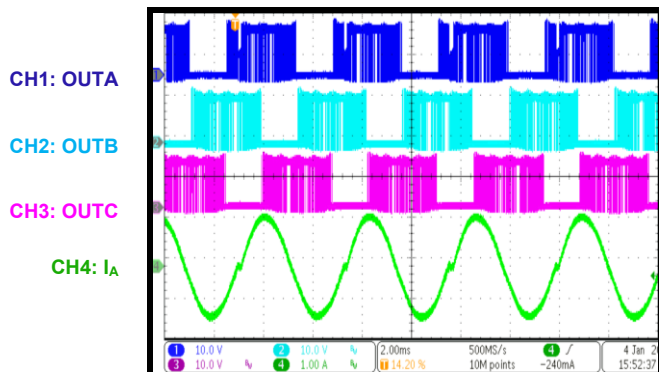
Steady State

PWM duty = 50%, DIR = low



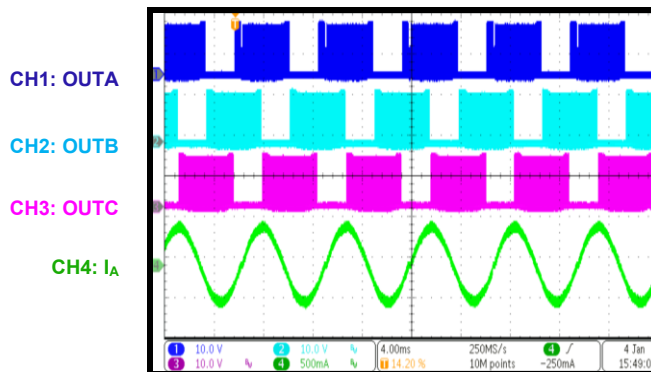
Steady State

PWM duty = 100%, DIR = high



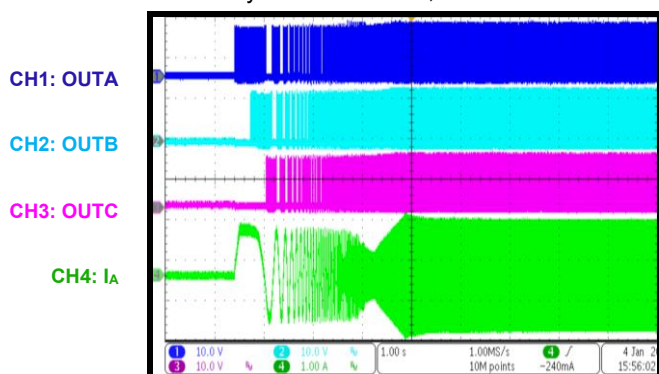
Steady State

PWM duty = 50%, DIR = high



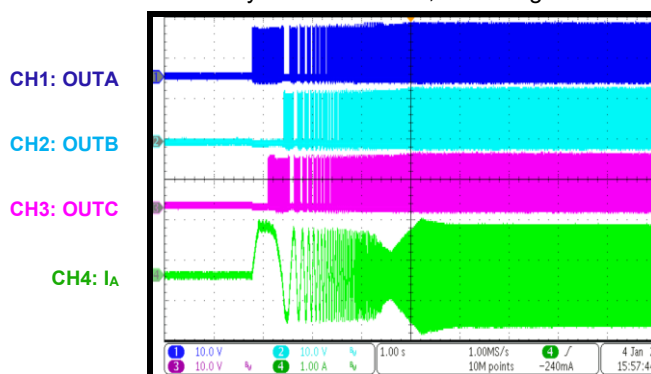
Start-Up through PWM

PWM duty = 10% to 100%, DIR = low



Start-Up through PWM

PWM duty = 10% to 100%, DIR = high

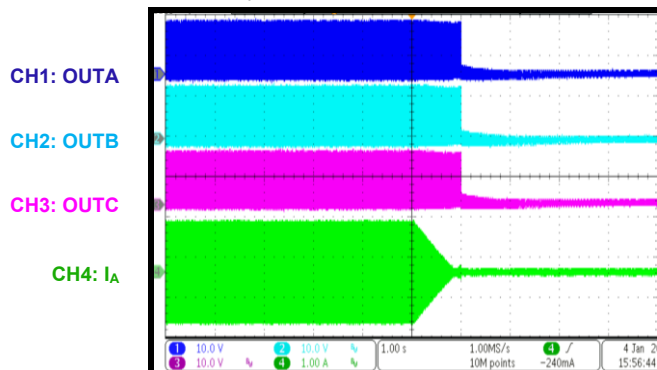


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. $V_{IN} = 12V$, PWM frequency = 20kHz, $T_A = 25^{\circ}C$, unless otherwise noted.

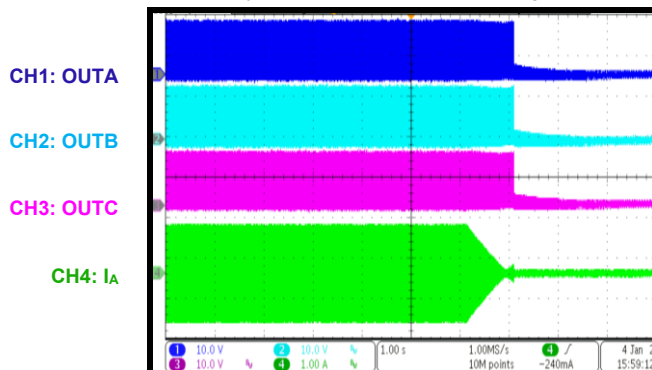
Shutdown through PWM

PWM duty = 100% to 10%, DIR = low



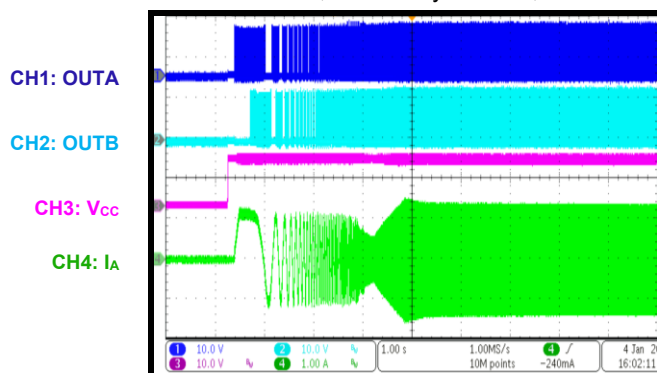
Shutdown through PWM

PWM duty = 100% to 10%, DIR = high



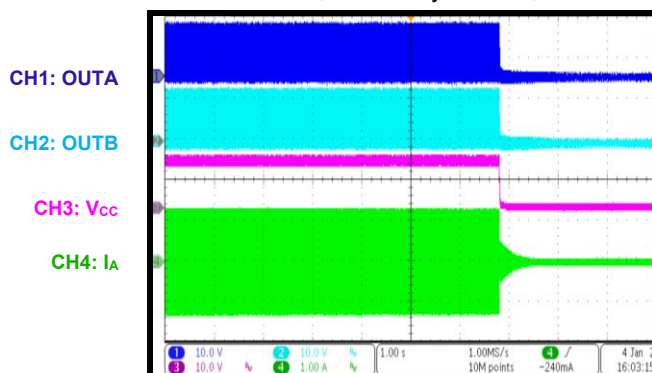
Start-Up through VCC

$V_{CC} = 0V$ to 12V, PWM duty = 100%, DIR = low



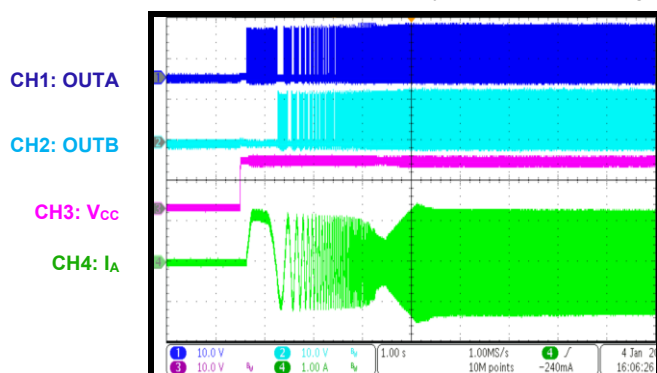
Shutdown through VCC

$V_{CC} = 12V$ to 0V, PWM duty = 100%, DIR = low



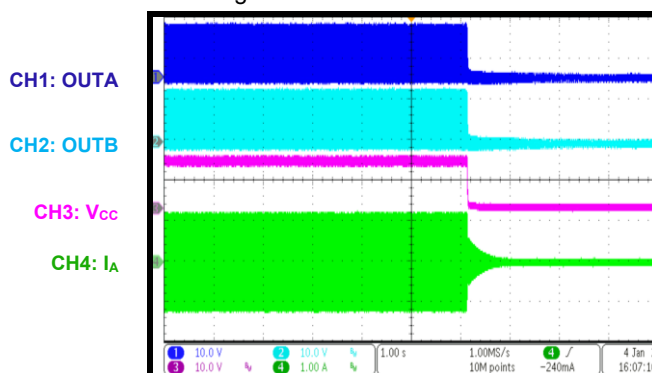
Start-Up through VCC

$V_{CC} = 0V$ to 12V, PWM duty = 100%, DIR = high



Shutdown through VCC

$V_{CC} = 12V$ to 0V, PWM duty = 100%, DIR = high

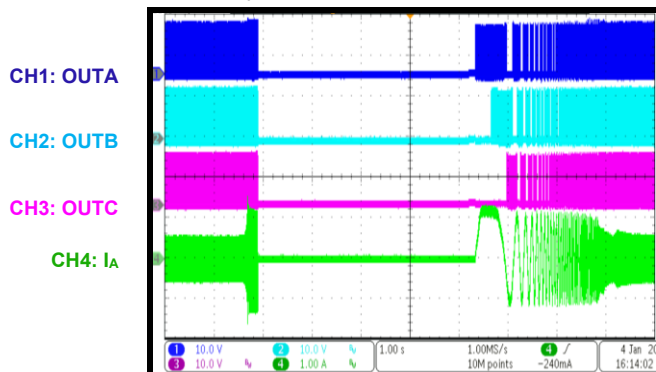


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. $V_{IN} = 12V$, PWM frequency = 20kHz, $T_A = 25^\circ C$, unless otherwise noted.

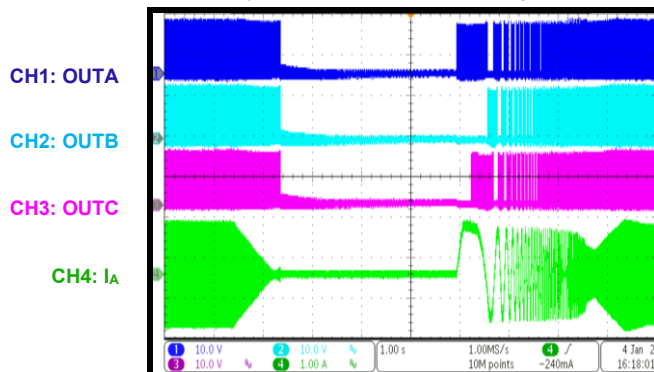
Rotor Lock and Retry

PWM duty = 50%, lock rotor then release



Direction Change

PWM duty = 100%, DIR = low to high



FUNCTIONAL BLOCK DIAGRAM

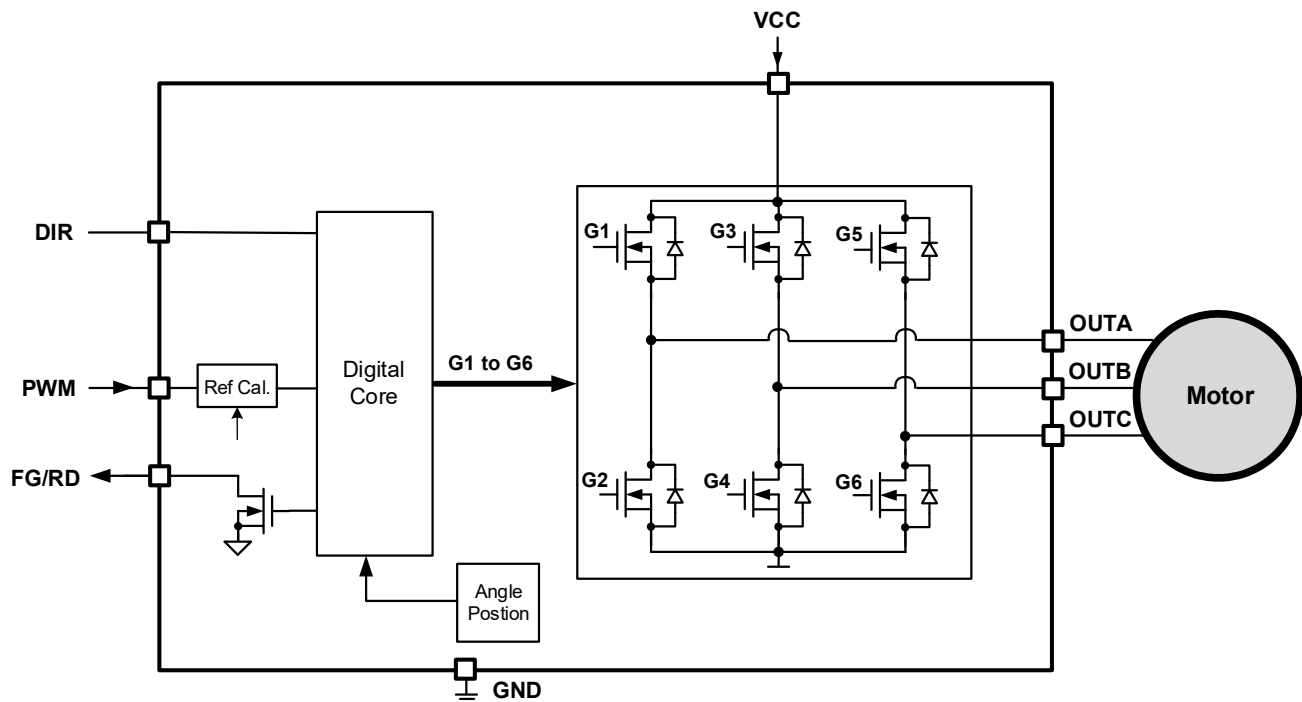


Figure 1: Functional Block Diagram

OPERATION

The MP6638 is a three-phase, sensorless, brushless DC (BLDC) motor driver with integrated power MOSFETs. It features sinusoidal sensorless control for improved efficiency and low vibration, with up to 1.7A peak phase current. The input voltage (V_{IN}) ranges from 2.5V to 16V.

Speed Control

The speed is controlled via an input pulse-width-modulation (PWM) signal applied on the PWM pin. The input PWM signal frequency ranges from 50Hz to 100kHz, and the output duty cycle is determined by the input PWM duty cycle.

Direction Control

The rotation direction is controlled by the DIR input signal's polarity. Pull the DIR pin low for forward rotation (OUTA → OUTB → OUTC); pull DIR high for reverse rotation (OUTA → OUTC → OUTB). DIR is pulled low via an internal resistor.

Starting Duty

The starting duty cycle is configured via the DIN_MIN bits (01h, bits[3:0]). If the SPD_ZERO bit (03h, bit[2]) is set to 1 and the input PWM duty cycle is below the duty cycle selected via DIN_MIN, then the MP6638 stops switching. If the input PWM duty cycle is higher than DIN_MIN + 1.2% hysteresis, then the MP6638 starts to output the duty cycle, and the motor spins (see Figure 2). By default, DIN_MIN is selected as 12.5%.

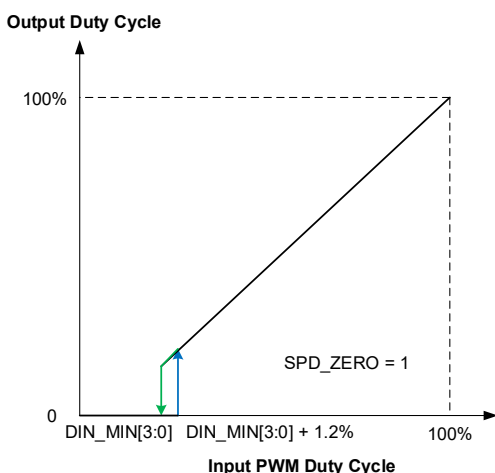


Figure 2: Starting Duty with SPD_ZERO = 1

If the SPD_ZERO bit is set to 0 and the input PWM duty cycle is below the duty cycle selected via DIN_MIN, then the MP6638 can also be configured to maintain the minimum speed (see Figure 3).

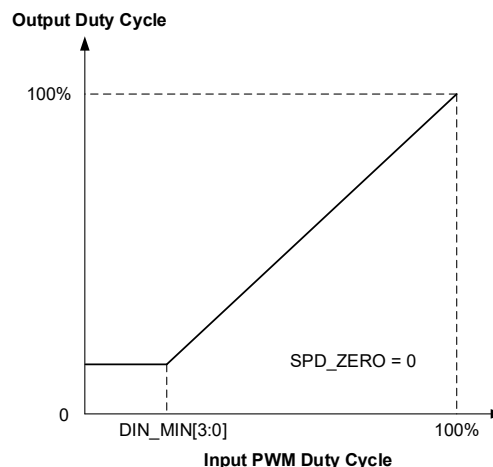


Figure 3: Maintain the Minimum Speed with SPD_ZERO = 0

Rotor Alignment

If motor is stationary, a set voltage vector is applied for a configurable time to align the rotor to the phase A position. The maximum voltage vector amplitude is limited via the VOL_LIM bit (01h, bit[7]). The ALIGN_TIME bits (00h, bits[7:6]) set the alignment times for different motors.

Open-Loop Acceleration Start-Up

After rotor alignment, the MP6638 openly accelerates the motor by increasing the driven vector's frequency. The frequency slew rate is selected via the F_SLEW bits (00h, bits[5:3]). After the motor speed reaches the set handoff threshold, the MP6638 enters sinusoidal sensorless control.

Soft Dynamic

After the open-loop acceleration start-up stage, the MP6638 enters sinusoidal sensorless control. During this stage, the output duty cycle reaches the target cycle smoothly, depending on the soft-start time (t_{SS}). t_{SS} is configured via the T_SS bits (02h, bits[3:2]).

Steady State

During steady state operation, the sensorless

sinusoidal control is selected. The motor's back electromotive force (BEMF) zero crossing is detected to obtain the rotor position and drive the motor with sinusoidal drive based on the rotor position.

Standby Mode

If the VCC pin voltage (V_{CC}) exceeds its under-voltage lockout (UVLO) rising threshold and the PWM pin remains low, then the MP6638 enters standby mode. Once the PWM input signal is detected, or power is cycled on the VCC pin, the MP6638 exits standby mode.

Rotor Speed Indication (FG) and Locked-Rotor Indicator (RD)

The FG/RD pin can be configured as the speed indicator via the FGRD bits (02h, bits[1:0]):

- If FGRD = 00, then the FG/RD pin outputs one cycle in one electrical cycle.
- If FGRD = 01, then the FG/RD pin outputs one cycle in two electrical cycles.
- If FGRD = 10, then the FG/RD pin outputs one cycle in three electrical cycles.

FG/RD is an open-drain output, and must be externally pulled up via an external resistor. This pin can also be configured as a locked-rotor protection indicator (RD) via the FGRD bits. If locked-rotor protection is triggered, then the FG/RD pin outputs low.

Protection Circuits

The MP6638 is fully protected against over-voltage (OV), under-voltage (UV), over-current (OC), and over-temperature (OT) events.

Over-Current Protection (OCP)

During normal switching, if the current flowing through the MOSFET exceeds the threshold (1.7A typically) after a blanking time, then the output duty decreases to limit the load current.

The over-current protection (OCP) function can be disabled via the FGRD bits.

Maximum Peak Current Protection (SCP)

If the current is not limited by OCP, then maximum peak current protection is triggered by detecting the current flowing through each MOSFET.

If the current flowing through any MOSFET exceeds the protection threshold (2.2A

typically), then all the MOSFETs turn off immediately after a blanking time. The MP6638 attempts to resume normal operation after a lock-retry time.

Thermal Shutdown (TSD)

The MP6638 provides thermal monitoring. If the die temperature exceeds 160°C, then all the MOSFETs turn off. Once the die temperature drops to 135°C, the MP6638 resumes normal operation.

Under-Voltage Lockout (UVLO)

If V_{CC} drops below its UVLO threshold, then all circuitries in the device are disabled and the internal logic resets. Once V_{CC} exceeds its UVLO threshold, the MP6638 resumes normal operation.

Dead Locked-Rotor Protection

If locked-rotor protection is triggered, then all the low-side MOSFETs (LS-FETs) turn on. After a lock-retry time (4.4s typically), the MP6638 attempts to resume normal operation.

Over-Voltage Protection (OVP)

The MP6638 employs input over-voltage protection (OVP). If V_{CC} exceeds 15V (typically), then all the MOSFETs turn off. Once V_{CC} drops below 14V, the MP6638 attempts to resume normal operation. As such, if V_{IN} exceeds 15V, then the OVP function must be disabled.

The OVP function can also be disabled via the FGRD bits.

Fault Diagnosis

Over-current protection (OCP), short-circuit protection (SCP), thermal shutdown (TSD), over-voltage protection (OVP), and locked-rotor indication have fault bits to indicate if any protection is triggered.

Test Mode and Factory Mode

The MP6638 supports a test mode to configure the internal registers. In test mode, all internal registers can be read or written. After the design is finalized, the register value can be configured to the non-volatile memory (NVM).

REGISTER DESCRIPTION

Register Map

Add	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00h (OTP/REG)	ALIGN_TIME		F_SLEW			F_TAR		
01h (OTP/REG)	VOL_LIM	RESERVED	WD_BLK	WD_ANG	DIN_MIN			
02h (OTP/REG)	RPM_SEL		OC_VF		T_SS		FGRD	
03h (OTP/REG)	ST_SEL	WD_BLK_MD	BEMF_SAMP	RESERVED	PWM_MD	SPD_ZERO	OCP	OVP
07h (REG)	OTP_PAGE		RESERVED	RD_FLG	SCP_FLG	TSD_FLG	OVP_FLG	OCP_FLG

VF (00h)

The VF command configures the frequency slew rate and handoff frequency.

Bits	Access	Bit Name	Default	Description
7:6	R/W	ALIGN_TIME	01	Sets the rotor alignment time at start-up. 00: 547ms 01: 274ms 10: 137ms 11: 68ms
5:3	R/W	F_SLEW	100	The frequency slew rate during open-loop acceleration. If the frequency slew rate is higher, then start-up is quicker. 000: 14Hz 001: 19Hz 010: 26Hz 011: 39Hz 100: 62Hz 101: 117Hz 110: 234Hz 111: 469Hz
2:0	R/W	F_TAR	001	The handoff speed during open-loop acceleration (electrical speed). 000: 20Hz 001: 39Hz 010: 59Hz 011: 78Hz 100: 98Hz 101: 117Hz 110: 137Hz 111: 156Hz

CURVE_WINDOW_PWM_DUTY (01h)

The CURVE_WINDOW_PWM_DUTY command configures the starting duty, detection window, and duty limit.

Bits	Access	Bit Name	Default	Description
7	R/W	VOL_LIM	0	The duty limit during open-loop acceleration. 0: 87.5% 1: 50%
6	NA	RESERVED	0	Reserved.

5	R/W	WD_BLK	0	Back electromotive force (BEMF) detection window's blanking time. 0: 33μs 1: 100μs
4	R/W	WD_ANG	1	Selects the BEMF detection window. 0: 30° 1: 15°
3:0	R/W	DIN_MIN	0100	Selects the starting duty cycle. 0000: 6.22% 0001: 7.78% 0010: 9.35% 0011: 10.91% 0100: 12.47% 0101: 14.03% 0110: 15.6% 0111: 17.16% 1000: 18.72% 1001: 20.28% 1010: 21.85% 1011: 22.41% 1100: 24.97% 1101: 26.53% 1110: 28.1% 1111: 29.66%

SOFT_START (02h)

The SOFT_START command configures the wait speed, frequency slew rate and handoff frequency stage's current limit, soft-start time (t_{ss}), and FG/RD output.

Bits	Access	Bit Name	Default	Description
7:6	R/W	RPM_SEL	00	Selects the threshold speed when the wait function is enabled. The IC waits for the fan speed to drop to the threshold speed before it starts driving the motor. These bits refer to the electrical frequency, rather than the mechanical frequency. 00: 7.5Hz 01: 14.5Hz 10: 22.5Hz 11: 29.5Hz
5:4	R/W	OC_VF	10	Current limit threshold during open-loop acceleration. 00: ¼ x over-current protection (OCP) 01: ½ x OCP 10: ¾ x OCP 11: 1 x OCP
3:2	R/W	T_SS	11	t_{ss} is the time duration when the output duty cycle increases from 0% to 100%. 00: 8.7s 01: 4.4s 10: 2.2s 11: 1.1s

1:0	R/W	FGRD	00	Speed indicator or locked-rotor indicator output selection via the FG/RD pin. 00: 1x, the FG/RD pin outputs the speed indicator, with one pulse in each electrical cycle 01: 1/2x, the FG/RD pin outputs the speed indicator, with one pulse in two electrical cycles 10: 1/3x, the FG/RD pin outputs the speed indicator, with one pulse in three electrical cycles 11: The FG/RD pin outputs the locked-rotor indicator
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CONTROL (03h)

The CONTROL configures the wait function, window blank mode, back electromotive force (BEMF) sample mode, pulse-width frequency (PWM) frequency selection, SPD_ZERO function, over-current protection (OCP), and over-voltage protection (OVP).

Bits	Access	Bit Name	Default	Description
7	R/W	ST_SEL	0	Enables the wait function with high-speed start-up. 0: Disables the wait function 1: The motor continues coasting until the motor speed drops to the set threshold
6	R/W	WD_BLK_MD	0	Selects the BEMF blank time mode. 0: Automatic time 1: Fixed time
5	R/W	BEMF_SAMP	0	Selects the active BEMF detection. 0: During BEMF detection window 1: At the end of the BEMF detection window
4	NA	RESERVED	0	Reserved.
3	R/W	PWM_MD	0	Selects the PWM input frequency. 0: 1kHz to 100kHz 1: 50Hz to 1kHz
2	R/W	SPD_ZERO	1	Selects zero speed. 0: Maintains the minimum speed when the input duty cycle is below the duty cycle set via the DIN_MIN bits (01h, bits[3:0]) 1: Stops when the input duty cycle is below the duty cycle set via DIN_MIN[3:0]
1	R/W	OCP	0	Enables OCP. 0: Enables OCP 1: Disables OCP
0	R/W	OVP	0	Enables input OVP. 0: Disables OVP 1: Enables OVP

OTP_FAULT_INDICATOR (07h)

The OTP_FAULT_INDICATOR command provides the one-time programmable (OTP) memory times and protection indicator.

Bits	Access	Bit Name	Default	Description
7:6	R	OTP_PAGE	00	OTP page indicator. 00: No OTP page is configured 01: The first OTP page is configured 11: The second OTP page is configured
5	R	RESERVED	1	Reserved.
4	R	RD_FLG	0	Dead locked-rotor protection indicator. 0: No dead locked-rotor protection 1: Triggers dead locked-rotor protection
3	R	SCP_FLG	0	Maximum peak current protection indicator. 0: No short-circuit protection (SCP) 1: Triggers SCP
2	R	TSD_FLG	0	Thermal shutdown (TSD) protection indicator. 0: No TSD protection 1: Triggers TSD protection
1	R	OVP_FLG	0	OVP indicator. 0: No OVP 1: Triggers OVP
0	R	OCP_FLG	0	OCP indicator. 0: No OCP 1: Triggers OCP

APPLICATION INFORMATION

Selecting the Input Capacitor

Place an input capacitor (C_{IN}) as close to the VCC and GND pins as possible to maintain a stable input voltage (V_{IN}) and reduce noise at the input. C_{IN} must have a low impedance at the switching frequency (f_{SW}).

Ceramic capacitors with X7R dielectrics are recommended for their low-ESR characteristics. The effective capacitance decreases when the voltage across the ceramic capacitor increases. If the ceramic capacitor is biased with its voltage rating, then the effective capacitance drops below 50%; ensure that sufficient capacitance is applied.

In addition, ensure that the ceramic capacitor's voltage rating is high enough to avoid over-voltage (OV) rating events.

Input Clamping TVS

High-voltage spikes are caused by the energy stored in the motor charging back to the C_{IN} side. To avoid these spikes, add a voltage-clamping transient voltage suppressor (TVS) diode or Zener diode. For a 12V application, a 15V TVS with a SOD-123 package or Zener diode is sufficient.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation and to minimize noise. For the best performance, refer to Figure 4 and follow the guidelines below:

1. Place C_{IN} as close to the VCC and GND pins as possible to minimize the switching loop area.
2. Typically, a small-package ceramic capacitor (C1) is recommended to improve high-frequency noise performance.

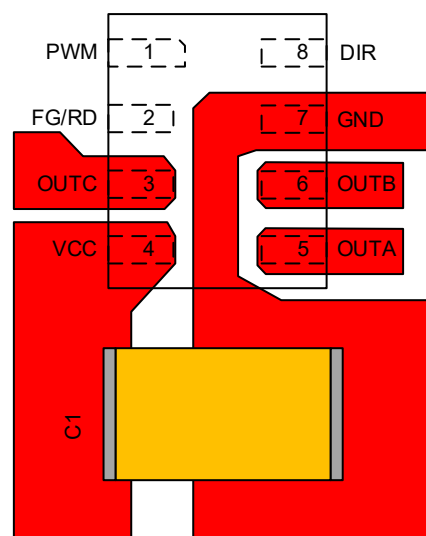


Figure 4: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

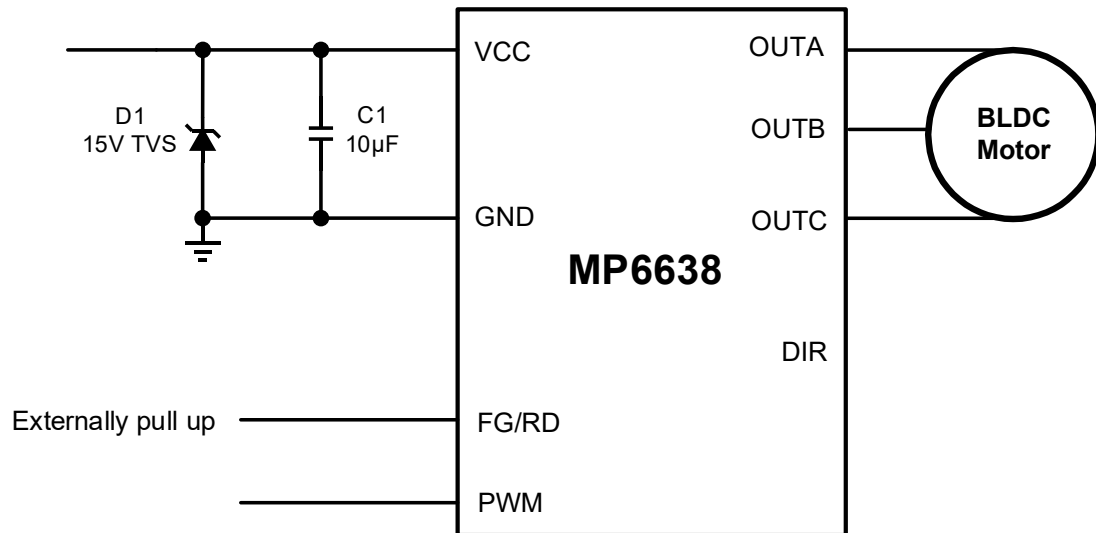
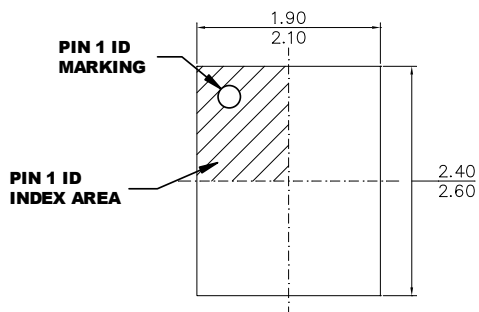


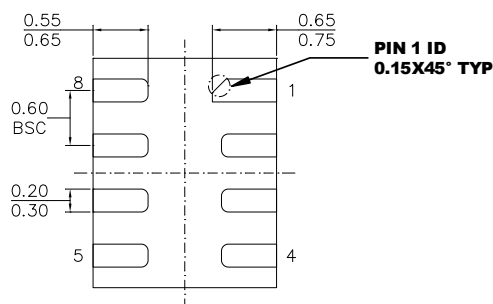
Figure 5: Typical Application Circuit

PACKAGE INFORMATION

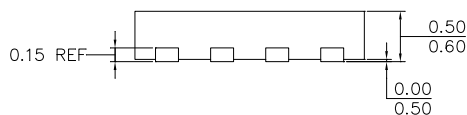
UTQFN-8 (2mmx2.5mm)



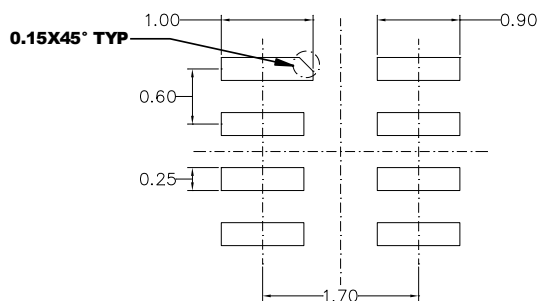
TOP VIEW



BOTTOM VIEW



SIDE VIEW

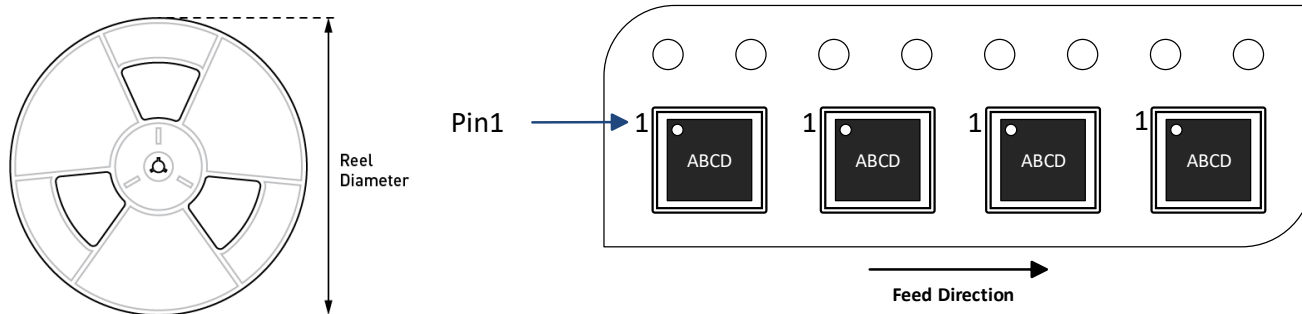


RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 3) JEDEC REFERENCE IS MO-220.
- 4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6638GRPU-xxxx-Z	UTQFN-8 (2mmx2.5mm)	5000	N/A	N/A	13in	12mm	8mm



REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/17/2025	Initial Release	-

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