# L4983

Datasheet

# High Efficiency Continuous Conduction Mode (CCM) Power Factor Correction (PFC) Boost Controller


## Features

- Peak current mode CCM-operated
- Proprietary multiplier “emulator” with minimum THD of line current in all operating conditions (CCM and DCM)
- Extremely few external components
- Protections: feedback loop failure, OVP, OCP, inductor saturation
- Inductor current sense
- Disable and low consumption function
- In-rush current monitoring
- Soft-start for smooth startup
- 1.2% (@ Tj = 25 °C) internal reference voltage
- 65 kHz (A version) and 130 kHz (B version) switching frequency
- SO8 package

| Product status link |
| --- |
| L4983 |

SUSTAINABLE TECHNOLOGY

## Applications

- PFC pre-regulators for:
  - IEC61000-3-2 and JEIDA-MITI compliant SMPS in excess of 1 kW
  - Desktop PC, server, web server, game console
  - High power LED luminaries
  - Industrial and medical SMPS according to IEC 60601-1-2

## Description

The L4983 is a peak current-mode PFC controller for boost converter with a proprietary multiplier “emulator” which in addition to the innovative THD optimizers guarantee very low Total Harmonic Distortion (THD) performance in all operating conditions. The device comes in a pin SO package and offers a high performance/ low-component count solution for CCM-operated boost PFC pre-regulators in EN61000-3-2 and JEIDA-MITI compliant applications, in a power range that spans from few hundred W to some kW.

The device, thanks to a proprietary off-time modulator, operates in quasi-fixed frequency in all operating conditions. Two options are available, 65 kHz for A and 130 kHz for B.

The device features low consumption and disable functions allowing usage in applications supposed to comply even with the latest energy saving requirements issued by Energy Star, the Department of Energy (DoE) in the United States, the European Code of Conduct, the European Union’s Ecodesign Directive, and other guidelines.

In addition to an overvoltage protection able to keep the output voltage under control during transient conditions, the IC is provided also with a protection against feedback loop failures or erroneous settings and boost inductor saturation. Soft-start limits the peak current.

The totem-pole output stage, capable of 0.7 A source and 1.5 A sink current, is suitable for big MOSFET or IGBT drives.

# 1 Block diagram and typical application

Figure 1. **Block diagram**

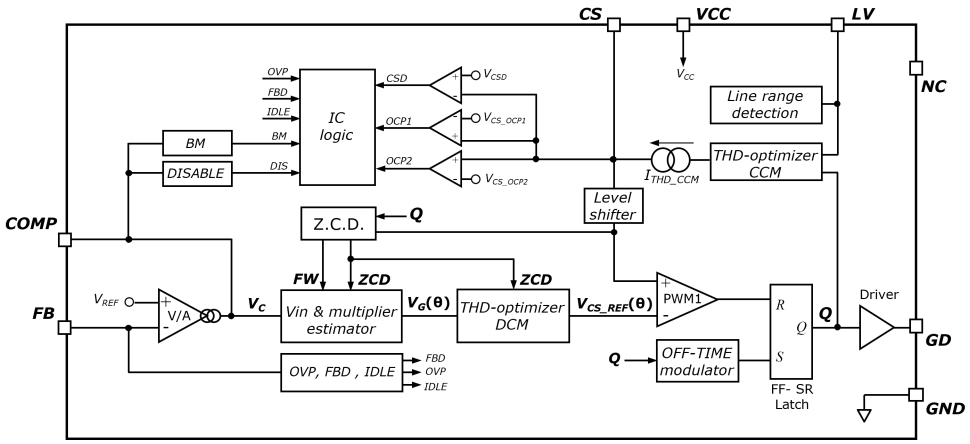
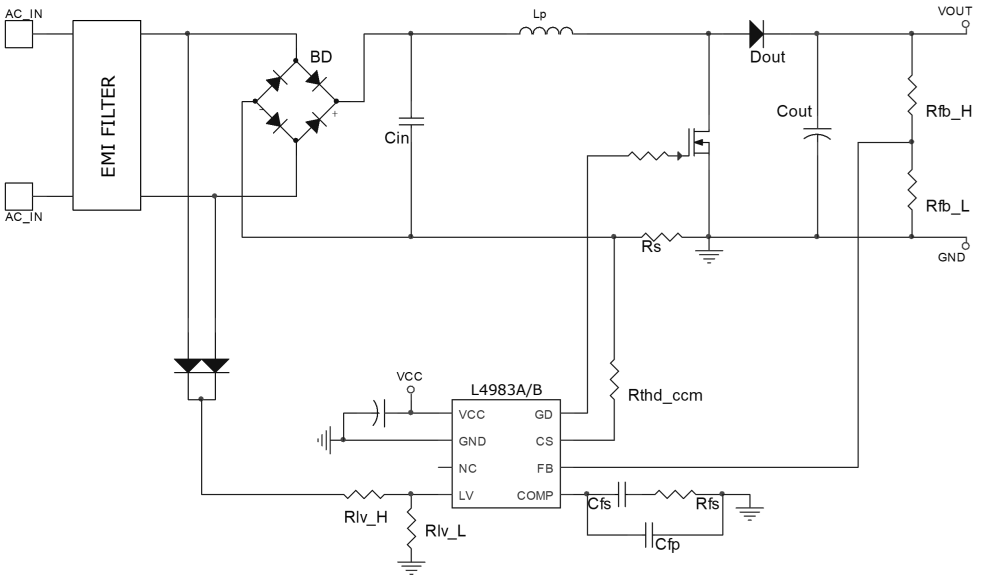



Figure 2. **Typical application**



# 2 Pin connection and functions

Figure 3. **Pin connection (top view)**

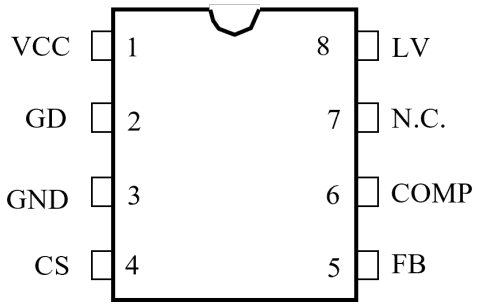



Table 1. **Pin description**

| No. | Name | Function |
|---|---|---|
| 1 | VCC | Supply voltage. A bypass capacitor to GND has to be placed close to the pins to get a clean bias voltage. |
| 2 | GD | Gate driver output. The output stage is able to drive power MOSFETs and IGBTs; it is capable of 0.7 A source current and 1.5 A sink current (typical values). |
| 3 | GND | IC ground. Current return for both the signal/bias part of the IC and the gate driver current. All of the ground connections of the bias components should be tied to a track going to this pin and kept separate from any pulsed current return. |
| 4 | CS | Current sense input. The inductor current is sensed through a resistor $R_S$ on the current return side. The resulting negative voltage is applied to this pin and compared to an internal sinusoidal-shaped reference to determine the turn-off instant of the external power switch. The pin is equipped with an internal current generator (sourced current during power switch on-time); it can be used, by simply adding a series resistor ($R_{THD\_CCM}$) for improved THD in CCM operation.<br>If the voltage on the pin goes below $V_{CS\_OCP1}$ (-0.49 V typ.) the internal overcurrent comparator is triggered and terminates the conduction cycle of the external power switch before the normal PWM circuit does. In this way, the peak inductor current is limited at a maximum of 0.49/$R_S$.<br>A second overcurrent level set at $V_{CS\_OCP2}$ (-0.75 V typ.) detects abnormal current values (e.g. due to boost inductor saturation) and, on this occurrence, activates a safety procedure that immediately stops the converter activity until the current level reaches the zero-current threshold $V_{CS\_ZCD}$ (-10 mV typical value). It allows safe operations also during current surges occurring at power-up or after a mains dip or missing cycle; in fact it allows switching start/restart only when the overcurrent event is definitively over. |
| 5 | FB | Inverting input of the trans-conductance Error Amplifier (OTA).<br>The information on the output voltage of the PFC regulator is fed into the pin through a resistor divider so that its voltage is proportional to the instantaneous value of the high voltage bus ($V_{BULK}$). Under steady-state conditions the voltage on pin sits at the internal reference of the error amplifier (VREF = 2.5 V). If the voltage exceeds the steady-state value by 7% ($V_{FB} > V_{FB\_S}$), e.g. due to an output voltage overshoot, the switching activity is stopped until $V_{FB} < V_{FB\_R}$ (2.55V typ.).<br>If the voltage at the FB pin is below $V_{FB\_FF/EBM}$ (0.5 V typ.) either a failure of the output divider is assumed or the device is externally forced in burst-mode operation. In both cases the PFC controller is stopped with low consumption. See Idle operation (external burst-mode function) and Feedback failure detection for further details. |
| 6 | COMP | Output pin of the trans-conductance Error Amplifier (OTA). A compensation network is placed between this pin and GND to allow stability of the control loop and ensure high PF and THD. To avoid uncontrolled rise of the output voltage at light or zero load, when $V_{COMP} < V_{COMP\_S}$ (1 V typ. Burst Mode condition) the gate driver pin (GD) is forced low and the switching activity is stopped. If the Burst Mode condition is triggered when GD is high, the system is allowed to complete the current on-time and the system stoppage takes place after GD falling edge.<br>The pin can be also used to disable the device by forcing $V_{COMP} < V_{COMP\_DIS}$ (0.7 V typ.) by means of an external pull-down active network. |

| No. | Name | Function |
|---|---|---|
| 7 | N.C. | Not internally connected . |
| 8 | LV | Line Voltage sense. This pin is connected to the AC side of the input bridge via a pair of diodes (1N400x type) and a resistor divider providing the input voltage information to both THD-CCM optimizer and Line Range detection (2-level feedforward) circuits. |

# 3 Electrical data

## 3.1 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

| Symbol | Pin | Parameter | Value | Unit |
|---|---|---|---|---|
| VCC | 1 | Supply voltage | -0.3 to 30 | V |
| ICC | 1 | Maximum supply current | 0 to 25 | mA |
| GD | 2 | Gate driver | -0.3 to VCC | V |
| CS | 4 | Current sense | -10 to 3.6 | V |
| FB | 5 | Input feedback ($I_{FB}$ < 1 mA) | -0.3 to self-limited | V |
| COMP | 6 | OTA output | -0.3 to 6 | V |
| LV | 8 | Line voltage sense ($I_{LV}$ < 0.5mA) | -0.3 to self-limited | V |

**Table 3. Recommended operating conditions.**

| Symbol | Pin | Parameter | Min. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| VCC | 1 | IC supply voltage | -0.3 | 24.5 | V | Internal clamp at 24.5 V min. |
| CS | 4 | Current sense input | -10 | 3.3 | V | |
| FB | 5 | Feedback input | -0.3 | 3.0 | V | Internal clamp at 3 V min. |
| COMP | 6 | OTA output | -0.3 | 5.3 | V | Values referred to an externally forced condition |
| LV | 8 | Line voltage input | -0.3 | 2.5 | V | Internal clamp at 4.5 V min |

## 3.2 Thermal data

**Table 4. Thermal data**

| Symbol | Parameter | Max. value | Unit |
|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance, junction-to-ambient | 150 | °C/W |
| $P_{tot}$ | Power dissipation @Tamb = 50 °C | 0.65 | W |
| $T_j$ | Junction temperature operating range | -40 to 150 | °C |
| $T_{stg}$ | Storage temperature | -55 to 150 | °C |

# 4 Electrical characteristics

$T_j$ = -25 to 125 °C, $V_{CC}$ = 15 V, $C_{GD}$ = 1 nF unless otherwise specified.

**Table 5. Electrical characteristics**

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Supply voltage** | | | | | | |
| $V_{CC}$ | Operating range | After turn-on | 10 | | 24.5 | V |
| $V_{CC\_ON}$ | Turn-on threshold | Voltage rising(1) | 9.5 | 10.5 | 11.5 | V |
| $V_{CC\_OFF}$ | Turn-off threshold | Voltage falling (1) | 8.5 | 9.0 | 9.5 | V |
| $V_Z$ | $V_{CC}$ clamp voltage | $I_{VCC}$ = 20 mA(2) | 24.5 | 26 | 27 | V |
| **Supply current** | | | | | | |
| $I_{START\_UP}$ | Start-up current | Before turn-on, $V_{CC}$ = 14 V | | 400 | 550 | µA |
| $I_Q$ | Quiescent current | $V_{FB} < V_{FB\_FF/EBM}$ | | 0.6 | 0.8 | mA |
| | | $V_{FB}$ = 2.5 V, $V_{COMP} < V_{COMP\_S}$ | | 0.65 | 0.85 | mA |
| | | $V_{FB} > V_{FB\_S}$ | | 0.65 | 0.85 | mA |
| $I_{CC}$ | Operating supply current | L4983A, $T_{ON}=T_{ON\_MIN}$(3) | | 2.2 | 2.8 | mA |
| | | L4983A, $LV*T_{ON}$ = 6.6 µs(4) | | 3.8 | 4.7 | mA |
| | | L4983B, $T_{ON}=T_{ON\_MIN}$(3) | | 3.4 | 4.0 | mA |
| | | L4983B, $LV*T_{ON}$ = 3.3 µs(4) | | 4.6 | 5.5 | mA |
| $I_{DIS}$ | Quiescent in disable | $V_{COMP} < V_{COMP\_DIS}$ | | 450 | 600 | µA |
| **Line voltage sense** | | | | | | |
| $I_{LV}$ | Input bias current | $V_{LV}$ = 0 to 3V | -0.1 | 0 | 0.1 | µA |
| $V_{LVCLAMP}$ | Internal clamp level | $I_{LV}$= 0.5mA | 4.5 | 5 | | V |
| $V_{LVPK\_LOW}$ | Low Line (LL) range detection | Voltage falling(1) | 1.026 | | | V |
| $V_{LVPK\_HIGH}$ | High Line (HL) range detection | Voltage rising(1) | | | 1.193 | V |
| **Error amplfier** | | | | | | |
| $V_{REF}$ | Voltage feedback input threshold | $T_j$ = 25 °C | 2.47 | 2.5 | 2.53 | V |
| | | 10 V < $V_{CC}$ < 24.5 V(1) | 2.45 | | 2.57 | V |
| $I_{FB}$ | Input bias current | $V_{FB}$ = 0 to 3 V | -0.1 | 0 | 0.1 | µA |
| $V_{FBCLAMP}$ | Internal clamp level | $I_{FB}$ = 1 mA | 3.0 | 3.3 | | V |
| gm | Transconductance gain | $V_{REF}$ -150 mV < $V_{FB}$ < $V_{REF}$ +150 mV | 160 | 200 | 240 | µS |
| $R_O$ | Output impedance | | 5 | | | MΩ |
| $I_{COMP}$ | Source current | $V_{COMP}$ = 3 V, $V_{FB}$=1.9 V | 0.7 | 1 | 1.45 | mA |
| | Sink current | $V_{COMP}$ = 3 V, $V_{FB}$=3.0 V | 0.7 | 1 | 1.45 | mA |
| $V_{COMP}$ | Upper saturation voltage | $I_{SOURCE}$ = 0.2 mA | 5.0 | | | V |
| | Lower clamp voltage | $V_{FB}$ = 3.0 V | 0.8 | | 0.9 | |
| **Dynamic (D_OVP) and static (S_OVP) overvoltage protections** | | | | | | |
| $V_{COMP\_S}$ | Burst mode threshold S_OVP (Static OVP) | Voltage falling(1) | 0.95 | 1.00 | 1.05 | V |

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{COMP\_R}$ | Restart threshold after S_OVP | Voltage rising(1) | 1 | 1.05 | 1.1 | V |
| $V_{FB\_S}$ | D_OVP disable threshold | 10 V < $V_{CC}$ < 24.5 V | 2.595 | 2.675 | 2.755 | V |
| $V_{FB\_R}$ | Restart threshold after D_OVP | 10 V < $V_{CC}$ < 24.5 V | 2.44 | 2.55 | 2.65 | V |
| **Disable** | | | | | | |
| $V_{COMP\_DIS}$ | Disable threshold | Voltage falling(1) | 0.65 | 0.7 | 0.75 | V |
| $V_{COMP\_EN}$ | Enable threshold | Voltage rising(1) | 0.85 | 0.9 | 0.95 | V |
| $I_{COMP\_DIS}$ | Pull-up current at disable | | 8 | 12 | 16 | µA |
| **Current sensing** | | | | | | |
| $I_{CS}$ | Leakage bias current | $V_{CS}$ = -0.5 V | | 15 | 21 | µA |
| | | $V_{CS}$ = 0.235 V | 7.5 | 10 | 14 | µA |
| $V_{CS\_OFS}$ | CS level shifter offset | CS = 0 V | 3 | 10 | 17 | mV |
| $V_{CS\_GAIN}$ | CS level shifter gain | C = -0.5 V | 0.94 | 0.98 | 1.02 | V/V |
| $V_{CS\_OCP1}$ | 1st level overcurrent threshold | | -510 | -490 | -470 | mV |
| $T_{SS\_OCP1}$ | 1st level OCP threshold ramp up time | | 104 | 130 | 156 | ms |
| $T_{BLK}$ | Leading edge blanking | LV > 360mV rising | 120 | 150 | 180 | ns |
| | | LV < 360mV rising | 235 | 310 | 385 | ns |
| $td_{(H-L)}$ | Delay to output | | | | 110 | ns |
| $V_{CS\_OCP2}$ | 2nd level overcurrent threshold | | -0.80 | -0.75 | -0.70 | V |
| $V_{CS\_ZCD}$ | Zero current threshold | | -15 | -10 | -5 | mV |
| **Current sense disconnection** | | | | | | |
| $V_{CSD}$ | Current sense disconnection threshold | Voltage rising | 165 | 200 | 235 | mV |
| $T_{CSD\_DB}$ | Disconnection debounce time | | 8 | 10 | 12 | µs |
| **Equivalent multiplier** | | | | | | |
| $K_M$ | Equivalent multiplier gain | LL range | 0.405 | 0.44 | 0.475 | V/V |
| | | HL range | 0.092 | 0.10 | 0.108 | V/V |
| **THD CCM-optimizer** | | | | | | |
| $K_{CCM}$ | | | 0.51 | 0.55 | 0.59 | H |
| **Feedback failure protection/External Burst Mode (EBM)** | | | | | | |
| $V_{FB\_FF/EBM}$ | Feedback failure protection (on FB) / external burst mode threshold | Voltage falling(1) | 460 | 500 | 540 | mV |
| | | Hysteresis | | 50 | | mV |
| $T_{FF/EBM\_DB}$ | FFP/EBM debounce time | | 1.25 | 1.8 | 2.35 | µs |
| $I_{FB\_EBM}$ | FB current during EBM | $V_{FB}$ < $V_{FB\_FF/EBM}$ | 70 | 100 | 135 | µA |
| | FB current at exit EBM | $V_{FB\_FF/EBM}$ < $V_{FB}$ < $V_{REF}$ | 0.75 | 1 | 1.25 | mA |
| **Switching frequency** | | | | | | |
| $F_{SW}$ | Switching frequency (L4983A) | $T_{ON}$ = 9µs, LL range | 60 | 65 | 71 | kHz |
| | | $T_{ON}$ = 3µs, HL range | | | | |
| | Switching frequency (L4983B) | $T_{ON}$ = 4.5µs, LL range | 120 | 130 | 142 | kHz |
| | | $T_{ON}$ = 1.5µs, HL range | | | | |

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Maximum on-time** | | | | | | |
| $T_{ON\_MAX}$ | Maximum on-time | L4983A | 32 | 40 | 50 | µs |
| | | L4983B | 16 | 20 | 26 | µs |
| **Minimum off-time** | | | | | | |
| $T_{OFF\_MIN}$ | Minimum off-time | L4983A | 0.75 | 1.0 | 1.35 | µs |
| | | L4983B | 0.35 | 0.5 | 0.75 | µs |
| **Gate driver** | | | | | | |
| $V_{OL}$ | Output low voltage | $I_{sink}$ = 200 mA | | | 0.7 | V |
| | | $I_{sink}$ = 5 mA | | | 0.02 | V |
| $V_{OH}$ | Output high voltage | 15V<VCC<24.5 V, $I_{source}$ = 5 mA | 11 | 12 | 13 | V |
| | | $V_{CC}$ = 9 V, $I_{source}$ = 5 mA | 7.85 | | | V |
| $I_{srcpk}$ | Peak source current | | | -0.7 | | A |
| $I_{snkpk}$ | Peak sink current | | | 1.5 | | A |
| $t_f$ | Voltage fall time | $V_{GD}$ from 8 V to 1 V | 3 | 7 | 15 | ns |
| $t_r$ | Voltage rise time | $V_{GD}$ from 1 V to 8 V | 5 | 10 | 15 | ns |
| | UVLO saturation | $V_{CC}$ = 0 V to $V_{CC\_ON}$, $I_{sink}$ = 1 mA | | | 1.1 | V |

1. *Parameters tracking each other.*
2. *The VCC pin is self-limited by an internal clamp when the device is in switching modality.*
3. *Equivalent to just before burst-mode condition.*
4. *Equivalent to full-load condition.*

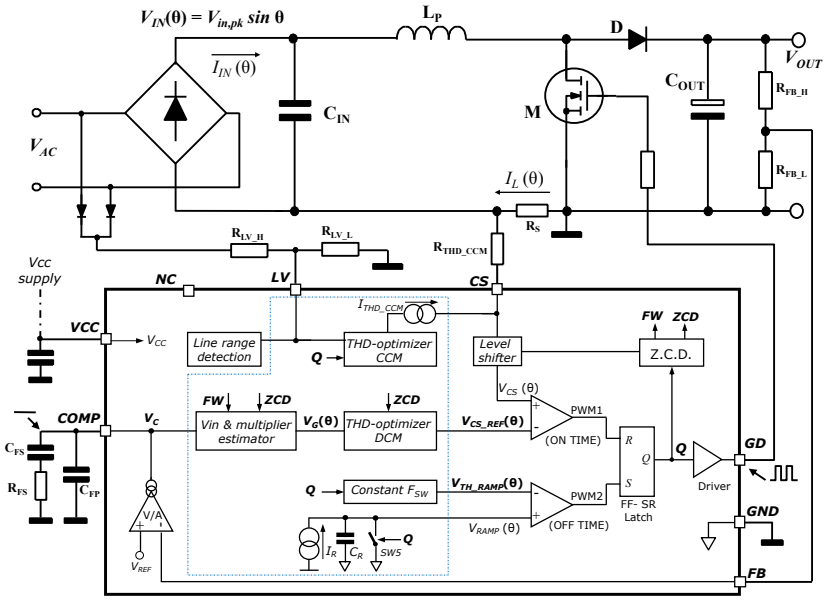
# 5 Application information

## 5.1 Theory of operation

The L4983A/B implements a conventional peak current mode control, based on fixed-off-time (FOT) control technique, with some proprietary circuitries that permit to ideally achieve the same performance of the more complex/expensive average current mode control.

Referring to Figure 4, the power switch on-time ($T_{ON}$) is programmed by the output voltage control loop comparing the current sense signal $V_{CS}$ with the internal current reference $V_{CS\_REF}$ in order to keep the VOUT regulation; whereas the power switch off-time ($T_{OFF}$) is programmed by the "OFF-TIME modulator" circuitry in order to keep quasi-fixed the switching frequency FSW in all operating conditions (see "Section 5.2" section for more details).

**Figure 4. Control loop connections**




The trans-conductance Error Amplifier V/A compares a portion of the output voltage $V_{OUT}$, brought at its inverting input externally available on pin FB via the resistor divider $R_3$-$R_4$, with an accurate internal reference $V_{REF}$ (2.5 V typ.) connected to the non-inverting input, and generates an error signal $V_C$ proportional to their difference. If the bandwidth of the error amplifier, essentially determined by the frequency compensation network connected between pin COMP and ground, is narrow enough – typically below 20 Hz – and a steady-state operation is assumed, the $V_C$ error signal available at pin COMP can be regarded as a DC level, at least as a first approximation. The $V_C$ voltage is then used by the "Vin & multiplier estimator" circuitry that, based also on the FW and ZCD signals (see Figure 5 and Figure 6 for more details), generates a voltage expressed by:

**Equation 1**

(1)

$$V_G\left(\theta\right) = V_C\ K_1\ \frac{V_{IN}(\theta)}{V_{OUT}}$$

where $K_1$ is the circuitry gain (constant term) and $V_{IN}(\theta) = V_{in,pk} sin\,\theta$ (with $0 \le \theta \le \pi$, as a result of the rectification operated by the input bridge) is the instantaneous line input voltage.

Equation 1 shows as the $V_G(\theta)$ voltage is proportional to the $V_{IN}(\theta)$ input voltage and to the $V_C$ control voltage like in a standard current-mode PFC, but without using the standard multiplier block and without the AC line sensing.

The $V_G(\theta)$ voltage is then managed by the “THD-DCM optimizer” circuitry that acts as a simple gain ($K_2$) in CCM operation whereas in DCM operation opportunely shapes the $V_G(\theta)$ voltage in order to achieve ideally sinusoidal input current.

Considering the CCM operation, the $V_{CS\_REF}(\theta)$ voltage is then expressed by:

**Equation 2**

(2)

$$V_{CS\_REF}(\theta)^{CCM} = V_G\left(\theta\right)\ K_2 = \frac{K_M}{V_{OUT}}\ V_{\ C}\ V_{IN}\left(\theta\right)$$

where $K_M = K_1\ K_2$ is the equivalent multiplier gain (see Electrical characteristics table for details).

The internal current reference voltage $V_{CS\_REF}(\theta)$ is then compared with the current sense $V_{CS}(\theta)$ pin voltage (which is internally translated due to negative inductor current sensing) that is opportunely shaped by the “THD-CCM optimizer” in order to achieve sinusoidal input current in CCM operation.

In particular, referring to Figure 4 and Figure 5, during the power switch-on time the “THD-CCM optimizer“ circuitry sources a current $I_{THD\_CCM}(\theta)$ to the CS pin, generating a voltage across the external $R_{THD\_CCM}$ resistor that is subtracted to the inductor current sense voltage $R_S\ I_L(\theta)$.

The resulting $V_{CS}(\theta)$ voltage, at external power switch turn-off condition, is then:

**Equation 3**

(3)

$$V_{CS}(\theta) = \ R_S\ I_{L,PK}(\theta) - \ R_{THD\_CCM}\ I_{THD_{CCM}}(\theta) = V_{CS\_REF}(\theta)$$

where the sourced $I_{THD\_CCM}(\theta)$ current is:

**Equation 4**

(4)

$$I_{THD\_CCM}(\theta) = \frac{L_P}{2\ K_{CCM}}\ \Delta I_L\left(\theta\right)$$

$L_P$ is the inductor value, $\Delta I_L(\theta)$ is the inductor current ripple, $K_{CCM}$ (0.55 typ.) is the circuitry gain.

**Figure 5. Left key waveforms of the circuit in figure 4**

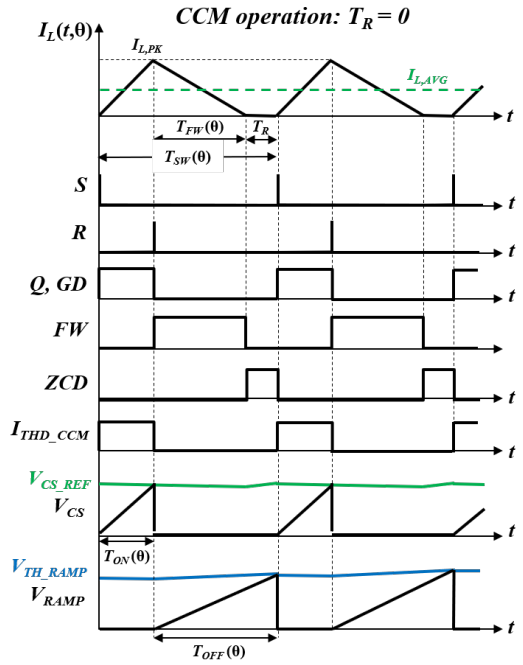
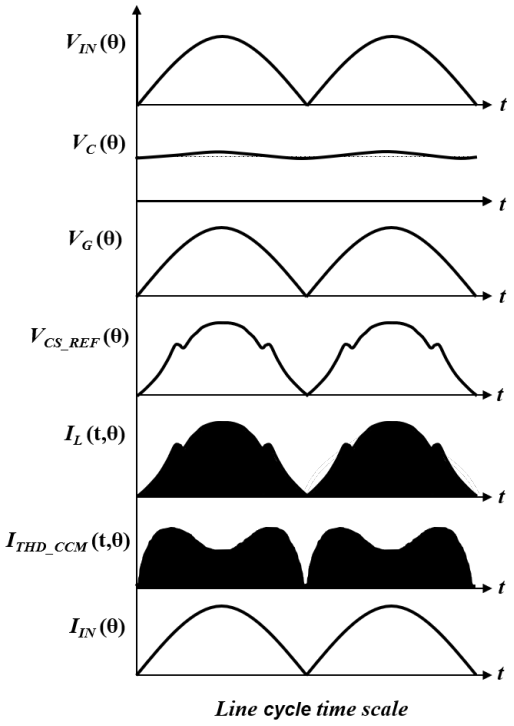



**Figure 6. Right key waveforms of the circuit in figure 4**




Now considering that the input current $I_{IN}(\theta)$ of the converter is the average value of the inductor current in a switching cycle results:

**Equation 5**

(5)

$$I_{IN}(\theta)^{CCM} = I_{L,PK}(\theta) - \frac{\Delta I_L(\theta)}{2}$$

Selecting the THD-CCM optimizer resistor equal to:

**Equation 6**

(6)

$$R_{THD\_CCM} = K_{CCM}\frac{R_S}{L_P}$$

and replacing equations #2 and #4 in equation #3, after some calculations the inductor peak current results:

**Equation 7**

(7)

$$I_{L,PK}(\theta) = \frac{1}{R_S}\frac{K_M}{V_{OUT}}V_C\ V_{IN}(\theta) + \frac{\Delta I_L(\theta)}{2}$$

Finally replacing equation #7 in equation #5, the input current of the converter results:

**Equation 8**

(8)

$$I_{IN}(\theta)^{CCM} = \frac{1}{R_S}\frac{K_M}{V_{OUT}}V_C\ V_{IN}(\theta)$$

which is sinusoidal and in phase with the $V_{IN}(\theta)$ input voltage (ideally zero-THD and unity-PF)

Considering the DCM operation ($T_R>0$), through geometrical consideration, the input current $I_{IN}(\theta)$ of the converter can be expressed by:

**Equation 9**

(9)

$$I_{IN}(\theta)^{DCM} = \frac{1}{2} I_{L,PK}(\theta) \frac{T_{ON}(\theta) + T_{FW}(\theta)}{T_{ON}(\theta) + T_{FW}(\theta) + T_R(\theta)}$$

Equation 9 shows that the term TR>0 introduces distortion if $I_{L,PK}(\theta)$ has a sinusoidal shape like in a standard PFC. Referring to Figure 4, the sinusoidal voltage $V_G\left(\theta\right) = V_C \ K_1 \ \frac{V_{IN}(\theta)}{V_{OUT}}$ is then opportunely shaped by the "THD-DCM" optimizer block, which generates the current reference voltage expressed by:

**Equation 10**

(10)

$$V_{CS\_REF}(\theta)^{DCM} = \ V_G(\theta) \ \frac{T_{ON}(\theta) + T_{FW}(\theta) + T_R(\theta)}{T_{ON}(\theta) + T_{FW}(\theta)}$$

Replacing equation #1 in equation #10, and considering that in DCM operation the peak of the inductor current is $I_{L,PK}(\theta) = \Delta I_L\left(\theta\right)$ , after some calculations results:

**Equation 11**

(11)

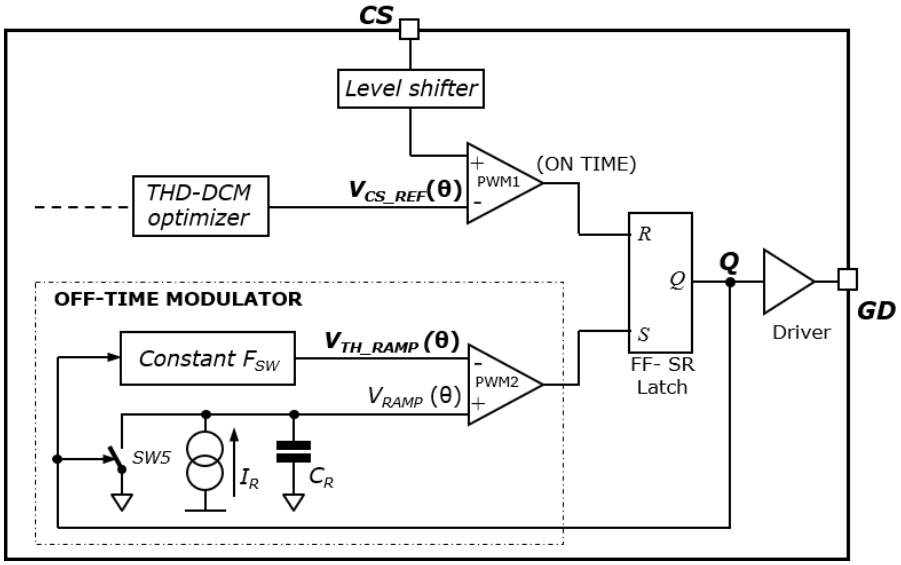
$$I_{IN}(\theta)^{DCM} = \frac{1}{R_S} \frac{K_M}{V_{OUT}} V_{\ C} \ V_{IN}(\theta)$$

which is sinusoidal and in phase with the $VI_N(\theta)$ input voltage (ideally zero-THD and unity-PF), and it has the same gain like in CCM operation.

## 5.2 OFF-time modulator

The device embeds a novel OFF-time modulator which is able to achieve quasi-fixed switching frequency in all operating conditions (CCM and DCM operation) and independent from the input/output voltage, the load conditions and the converter's parasitic as the existing modulators.

**Figure 7. OFF-time modulator - details**




Referring to Figure 7, once the power switch ON-time is ended (Q signal goes low) the internal switch $S_{W5}$ is open and the constant current generator $I_R$ starts to charge linearly the capacitor $C_R$. The resulting voltage $V_{RAMP}$ is compared with the voltage $V_{TH\_RAMP}$, which is generated by the "Constant $F_{SW}$" circuitry based on the Q signal duration ($T_{ON}$). As soon as the ramp voltage $V_{RAMP}$ reaches the $V_{TH\_RAMP}$ voltage, the flip-flop is set and the external power switch is turned on (Q signal goes high).

In other words, the power switch off-time ($T_{OFF}$) is modulated based on the on-time information ($T_{ON}$) to keep cycle-by-cycle constant the resulting switching frequency ($F_{SW}=1/T_{SW\_TARGET}$):

$T_{OFF} = T_{SW\_TARGET} - T_{ON}$.

**Figure 8. Left OFF-time modulator timing – Line cycle time scale**

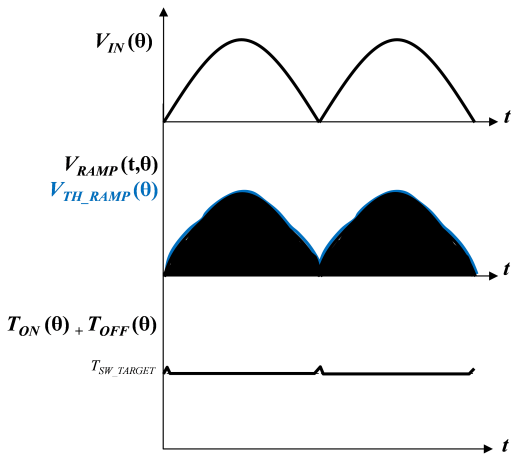
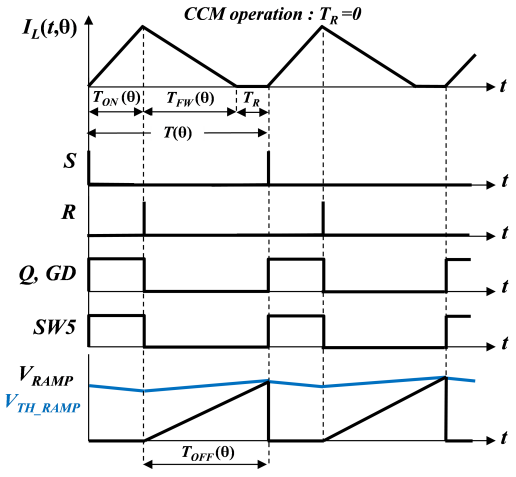



**Figure 9. Right OFF-time modulator timing – Switching cycle time scale**

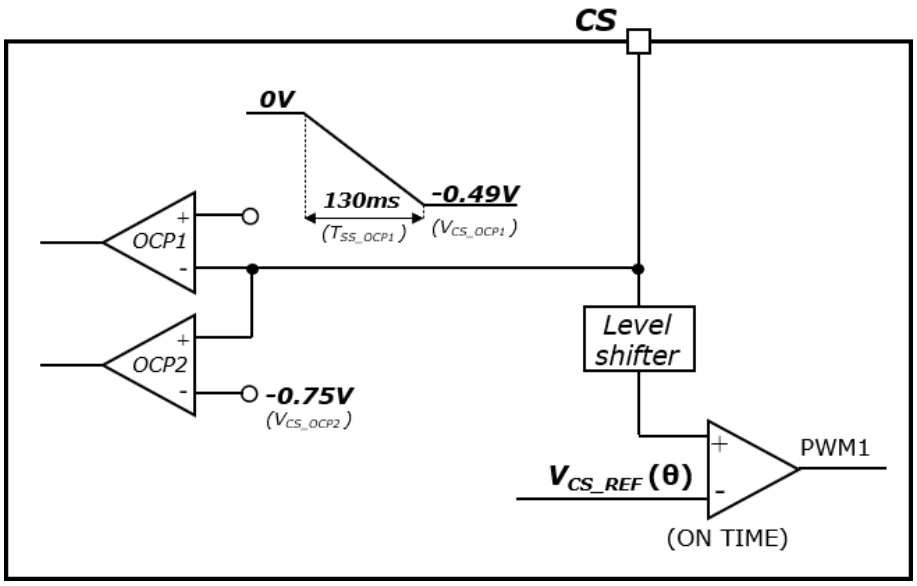


## 5.3 Soft-start

To limit the in-rush current of the converter at the startup, the device implements a soft startup increasing the peak of the inductor current from zero up to the required value programmed by the control loop to regulate the output voltage.

In particular, the device changes the reference threshold of the first overcurrent comparator (OCP1) from zero up to $V_{CS\_OCP1}$ (-0.49 V typ.) in $T_{SS\_OCP1}$ time (130 ms typ.), as shown in Figure 10 .

**Figure 10. Soft-start circuitry details**




## 5.4 No load operation (burst-mode function)

To avoid uncontrolled rise of the output voltage at light or zero load, when $V_{COMP} < V_{COMP\_S}$ (1 V typ.) the device stops the switching activity and reduces its power consumption. As soon as the $V_{COMP} > V_{COMP\_R}$ (1.05 V typical and in tracking with the threshold $V_{COMP\_S}$) the device restarts the switching activity.

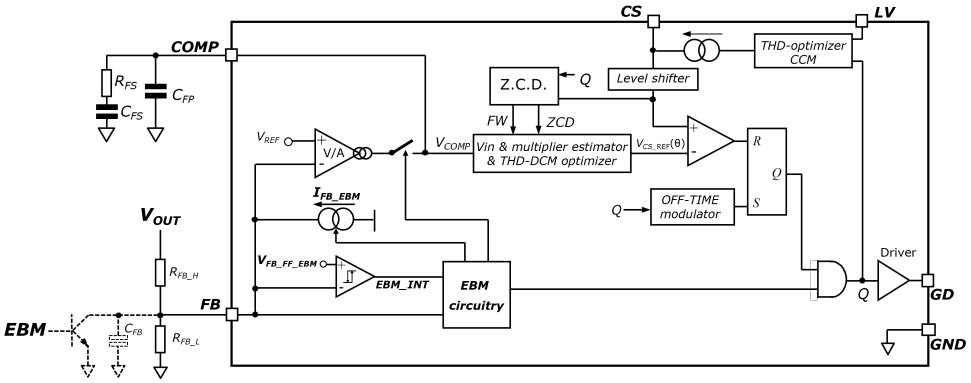
If the burst-mode condition is triggered when the gate driver GD is “high”, the device completes the current ON-time and the system stoppage takes place after GD falling edge.

During the burst-mode operation, the system application should guarantee $V_{CC} > V_{CC\_OFF}$. In fact, if the VCC pin voltage drops down to $V_{CC\_OFF}$, the device shutdown and a $V_{CC\_OFF}/V_{CC\_ON}$ cycle is needed to restart the operation (performing the soft-start).

## 5.5 Idle operation (external burst-mode function)

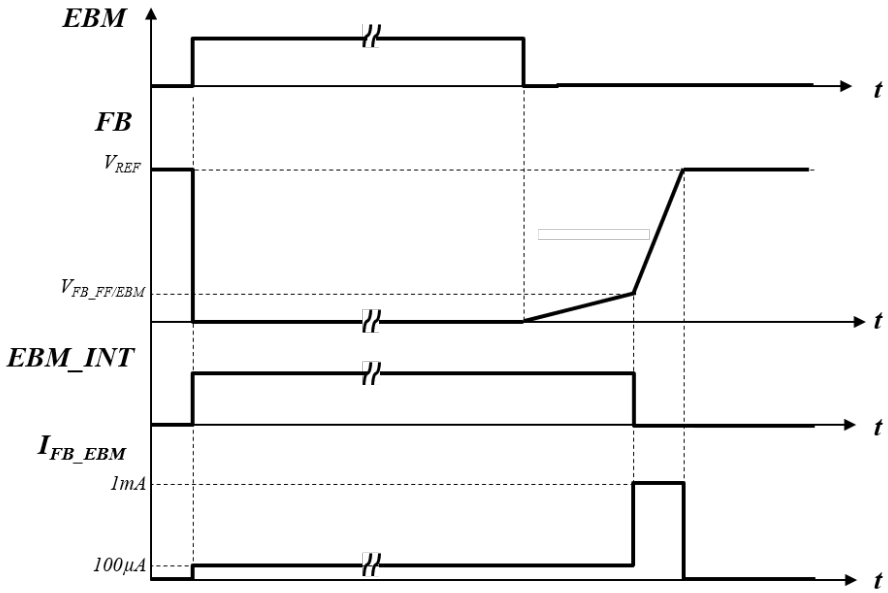
The FB pin can be used to implement an external burst-mode (EBM), forcing the pin lower than the internal threshold $V_{FB\_FF/EBM}$ (500 mV typ.): the switching activity is stopped and the IC power consumption is reduced (Error Amplifier is also turned off and the COMP pin is forced to “high impedance”). The device restarts switching, without implementing the soft-start, as soon as the FB voltage exceeds the $V_{FB\_FF/EBM}$ threshold by 50 mV typ. De-bounce time $T_{FF/EBM\_DB}$ (1.8 µs typ.) is provided to avoid false triggering. Referring to Figure 11, it is worth noting that as soon as the device enters the EBM state (the internal signal EBM_INT is high) a weak pull-up current $I_{FB\_EBM}$ (100 µA typ.) is sourced from the FB pin in order to speed up the FB voltage rising edge when the external pull-down is released. In addition, once the FB voltage exceeds $V_{FB\_FF/EBM}$ + 50 mV the $I_{FB\_EBM}$ current of 100 µA is increased to 1 mA till the FB pin voltage reaches the final target of 2.5 V (internal $V_{REF}$). When using the EBM function, the suggested value of the FB filter capacitor $C_{FB}$ is 3.3 nF.

Figure 11. **External Burst-Mode (EBM) function – circuit details**




During the external burst-mode condition (FB < $V_{FB\_FF/EBM}$), the system application should guarantee $V_{CC}$ > $V_{CC\_OFF}$. In fact, if the VCC pin voltage drops down to $V_{CC\_OFF}$, the device shutdown and a $V_{CC\_OFF}$/$V_{CC\_ON}$ cycle is needed to restart the operation (performing the soft-start).

Figure 12. **External Burst-Mode (EBM) function – timing**

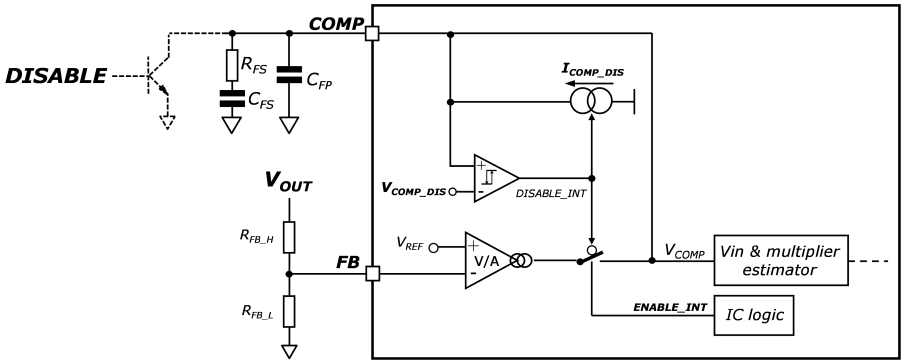



## 5.6 Disable operation (DISABLE function)

Forcing the COMP pin lower than the internal threshold $V_{COMP\_DIS}$ (0.7 V typ.), the device stops the operation and enters into low power consumption. The Error Amplifier is turned off and a weak internal pull-up current $I_{COMP\_DIS}$ (10 µA typ.) is activated. De-bounce time $T_{COMP\_DIS\_DB}$ (50 µs typ.) is provided to avoid false triggering.

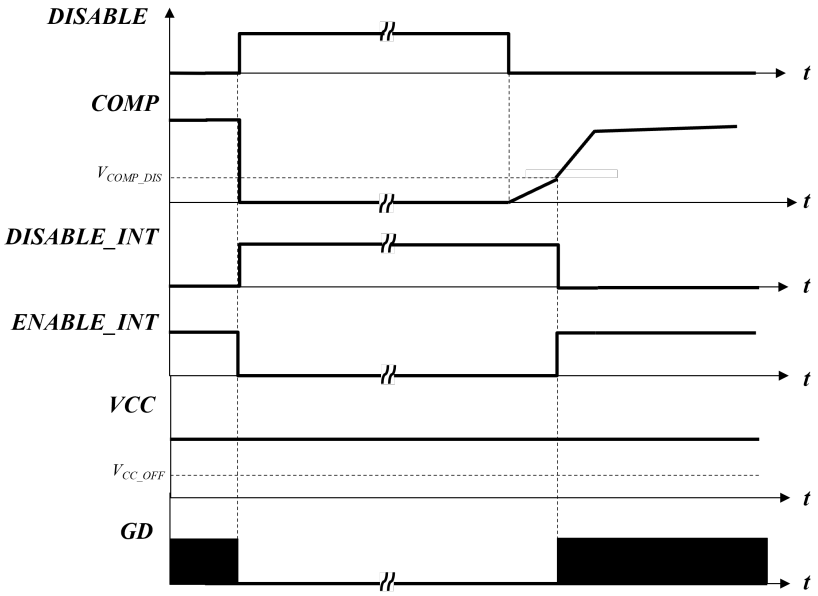
Referring to Figure 13, releasing the external pull-down the internal pull-up current $I_{COMP\_DIS}$ charges the compensation network connected between COMP pin and ground and the COMP voltage starts to increase. As soon as the COMP pin reaches the enable threshold $V_{COMP\_EN}$ (0.9V typ.), the device restarts the operation implementing the soft-start.

Figure 13. **DISABLE function – circuit details**




During the disable operation, the system application should be guarantee VCC > $V_{CC\_OFF}$. In fact, if the VCC drops down to $V_{CC\_OFF}$, the device shutdown and a $V_{CC\_OFF}/V_{CC\_ON}$ cycle is needed to restart the operation. .

Figure 14. **DISABLE function – timing**




## 5.7 Protections

A comprehensive set of protections is embedded to ensure a high level of reliability of the final application without adding extra components and/or circuitry.

### 5.7.1 Output overvoltage (OVP function)

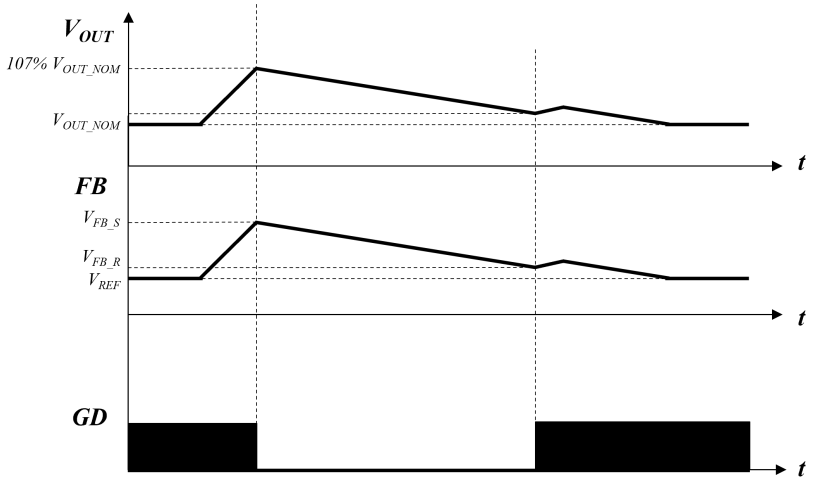
To limit an output voltage overshoot, e.g. due to a heavy load release or at startup with light-load, the device stops the switching activity as soon as the instantaneous output voltage $V_{OUT}$ is higher than 7% typ. in respect to the programmed value.

In fact, the device detects an overvoltage condition monitoring the FB pin which is proportional to the instantaneous value of the output voltage $V_{OUT}$ and in steady-state conditions sits at the internal reference of the error amplifier ($V_{REF}$ = 2.5 V).

As soon as the FB voltage exceeds the steady-state value by 7% ($V_{FB} > V_{FB\_S}$), the switching activity is stopped until it gets back close to it ($V_{FB} < V_{FB\_R}$).

De-bounce time $T_{DOVP\_DB}$ (50 µs typ.) is provided to avoid false activation of the protection.

Figure 15. **OVP timing**




### 5.7.2 Overcurrent (OCP1 function)

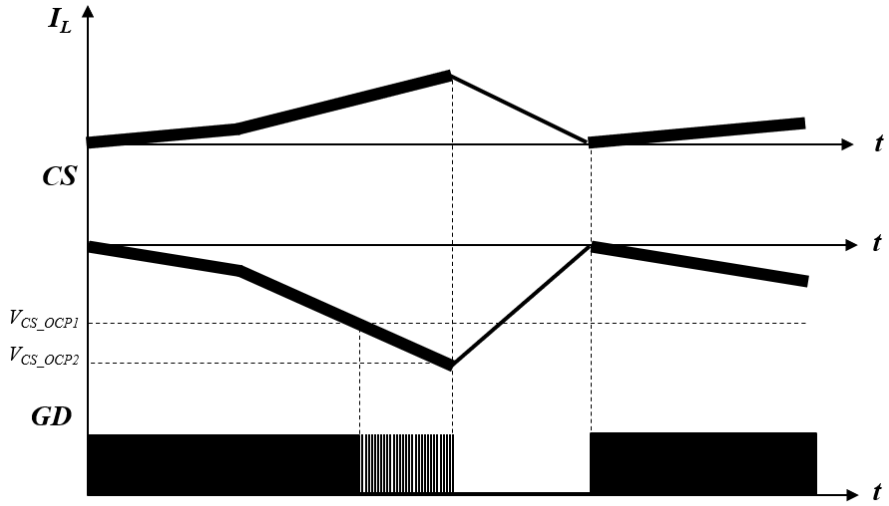
To limit the peak inductor current in case of extra request (e.g. heavy load changes), the device implements a cycle-by-cycle overcurrent protection. The device monitors the CS pin during the power switch on-time and as soon as the voltage on the CS pin goes below $V_{CS\_OCP1}$ (-0.49 V typ.), the internal overcurrent comparator is triggered and terminates the conduction cycle of the power switch before the normal PWM circuit does. In this way, the peak inductor current is limited to a maximum of $0.49/R_S$.

### 5.7.3 Inductor saturation detection (OCP2 function)

A second overcurrent level set at $V_{CS\_OCP2}$ (-0.75 V typ.) detects abnormal current values (e.g. due to boost inductor saturation) and, on this occurrence for two consecutive switching cycles, activates a safety procedure that immediately stops the converter activity until the current level reaches the zero-current threshold ($V_{CS\_ZCD}$).

The zero-current threshold monitor allows safe operations also during current surges occurring at power-up or after a mains dip or missing cycle; in fact it allows switching start/restart only when the overcurrent event is definitively over.

Figure 16. **OCP2 timing**



### 5.7.4 Feedback failure detection

The device handles the possible disconnection of both output voltage feedback and input current monitoring. At startup, as soon as the VCC pin voltage reaches the $V_{CC\_ON}$ turn-on threshold, the device checks the FB and CS pins:

- if the FB pin voltage is lower than the internal $V_{FB\_FF/EBM}$ threshold (0.5 V typ.) a failure of the output divider resistor is assumed (e.g. $R_{FB\_H}$ resistor not mounted), then the device stops the switching activity and reduces its consumption.
  - De-bounce time $T_{FF/EBM\_DB}$ (1.8 µs typ.) is provided to avoid false triggering.
- if the CS pin voltage is higher than the internal $V_{CSD}$ threshold (200 mV typ.) a failure of the current sensing resistors is assumed (e.g. $R_{THD\_CCM}$ resistor not mounted and/or $R_S$ resistor burned), then the device stops the switching activity and reduces its consumption. A recycle of VCC between the turn-off threshold ($V_{CC\_OFF}$) and the turn-on threshold (V.) is needed to restart the converter.
  - De-bounce time $T_{CSD\_DB}$ (10 µs typ.) is provided to avoid false triggering.

## 5.8 Line feedforward

To keep the maximum output power deliverable by the converter almost constant with respect to the AC input voltage, a two-level discrete voltage feedforward is integrated in the controller. Basically, the AC input voltage is monitored through the LV pin and internally compared with a fixed threshold to properly set the value of equivalent multiplier gain $K_M$ (see Table 1 for details). Using an input voltage resistor divider, composed by the $R_{LV\_H}$ and $R_{LV\_L}$ resistors in Figure 2 with the following gain:

**Equation 12**

$$K_p = \frac{R_{LV\_L}}{R_{LV_H} + R_{LV\_L}} \cong \frac{R_{LV_L}}{R_{LV_H}} = 4.83 \cdot 10^{-3} \quad (12)$$

the proper operation of the converter (with the right $K_M$ multiplier gain) is guaranteed for an ac input voltage below 140 Vrms and above 176 Vrms.

# 6 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 6.1 SO-8 package information

**Figure 17. SO-8 package dimensions**

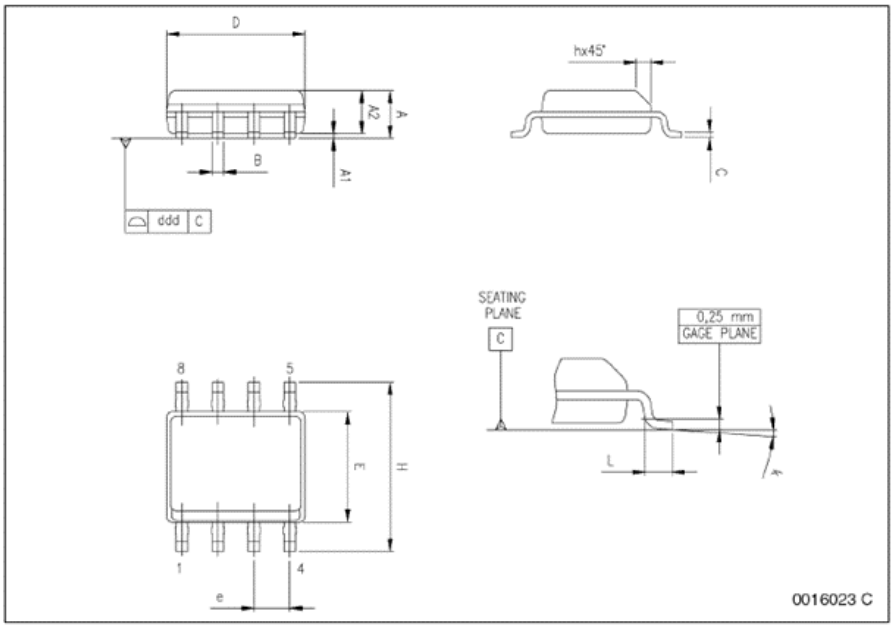



**Table 6. SO-8 mechanical data**

| Dim. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 1.35 | | 1.75 | 0.053 | | 0.069 |
| A1 | 0.10 | | 0.25 | 0.004 | | 0.010 |
| A2 | 1.10 | | 1.65 | 0.043 | | 0.065 |
| B | 0.33 | | 0.51 | 0.013 | | 0.020 |
| C | 0.19 | | 0.25 | 0.007 | | 0.010 |
| D(1) | 4.80 | | 5.00 | 0.189 | | 0.197 |
| E | 3.80 | | 4.00 | 0.15 | | 0.157 |
| e | | 1.27 | | | 0.050 | |
| H | 5.80 | | 6.20 | 0.228 | | 0.244 |
| h | 0.25 | | 0.50 | 0.010 | | 0.020 |
| L | 0.40 | | 1.27 | 0.016 | | 0.050 |
| k | 0° (min.), 8° (max.) | | | | | |
| ddd | | | 0.10 | | | 0.004 |

1. *Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (.006 inch) in total (both side).*

# 7 Ordering information

Table 7. **Order codes**

| Order code | Package | Package marking | Packaging |
|---|---|---|---|
| L4983A | SO-8 | L4983A | Tube |
| L4983B | SO-8 | L4983B | Tube |
| L4983ATR | SO-8 | L4983A | Tape and reel |
| L4983BTR | SO-8 | L4983B | Tape and reel |

## Revision history

Table 8. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 31-Mar-2026 | 1 | Initial release. |
| 20-May-2026 | 2 | Modified the title. |

# Contents

# List of tables

# List of figures

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