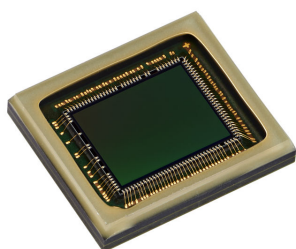


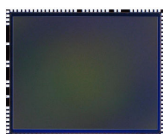
## RGB-NIR 5.1 megapixel image sensor with combined global shutter and rolling shutter modes for consumer and industrial applications



VB1943



VD1943



| Product | Description |
|---------|-------------|
| VB1943  | OBGA        |
| VD1943  | Bare die    |

### Features

- **Resolution:** 5.1 megapixel sensor (2560 x 1984)
- **Chroma:** RGB-NIR, NIR or Bayer
- **Optical format:** 1/2.5 inch
- **Image array size:** 5.8 mm x 4.5 mm
- **Pixel technology:**
  - 3D stacked sensor with 2.25  $\mu\text{m}$  x 2.25  $\mu\text{m}$  BSI pixel size
  - Global and rolling shutter technology
- **Functions:**
  - Dual and single exposure modes with separated controls of RGB pixels and NIR pixels
  - Automatic/external synchronization mode
  - Independent horizontal and vertical image flip
  - Automatic dark calibration
  - Dynamic defective pixel correction
  - Integrated noise reduction feature
- **Advanced image processing:**
  - Embedded 18-bit high dynamic range pixel reconstruction
  - Embedded Bayer reconstruction with NIR depollution
  - Embedded NIR smart upscale to full resolution monochrome output
  - Four programmable contexts with versatile sequencing management
- **Frame rates:**
  - Up to 100 frames per second at full resolution in global shutter mode
  - Up to 50 frames per second at full resolution in rolling shutter mode
- **Interfaces:**
  - MIPI CSI-2 interface (dual/quad lanes, max. 1.5 Gbps/lane)
  - MIPI CCI control interface up to 1 MHz
  - 4 programmable GPIOs (general-purpose input/output) to control external illuminators:
    - Output is synchronized with sensor integration periods
    - PWM (pulse-width modulation) control
- Additional features: Integrated temperature sensor
- **Package options:**
  - Available as bare die
  - Available in OBGA package
- **OBGA package:**
  - Package size: 10.3 x 8.9 mm
  - Ball matrix: 10 x 9 balls, pitch 0.8 mm

## Description

The VB1943 and VD1943 are 5.1 megapixel, 2.25  $\mu\text{m}$  global, and rolling shutter image sensors. They are designed for a wide spectrum of applications that require capturing color and NIR images. Operation of these sensors combines global and rolling shutter technology with an extended dynamic range.

Leveraging from preeminent 3D stacking and ST patented processes, these sensors perform outstandingly in the NIR (940 nm) and visible region. In global shutter mode, they can capture up to 100 frames per second in a 2560 x 1984 resolution format.

The VB1943 and VD1943 sensors can be used in rolling shutter mode, taking advantage of low dark noise capability. They can operate in an 18-bit HDR mode compressed down to 12 or 10 bits through a customizable PWL.

The RGB-NIR input image is processed by the integrated advanced ISP. It can reconstruct a full resolution NIR smart upscaled monochrome image or a 2x2 color Bayer image NIR depolluted.

For computer vision applications, acquisition can be switched to global shutter mode with an NIR light source. Switching to global shutter mode with an external NIR light source greatly reduces the system power consumption that is required to drive the illumination.

# 1 Product overview

## 1.1 Product characteristics

**Table 1. Key characteristics**

| Category                | Parameter                                      | Characteristics                                 |
|-------------------------|------------------------------------------------|-------------------------------------------------|
| Shutter                 | Type                                           | Global Shutter (GS)<br>and Rolling Shutter (RS) |
| Resolution              | Pixel resolution                               | 2560 x 1984 (5.1MP)                             |
| Pixel                   | Sensor technology                              | 3D stacked BSI pixel                            |
|                         | Pixel size                                     | 2.25 μm x 2.25 μm                               |
| Optical characteristics | Image array size [H x V]                       | 5.8 mm x 4.5 mm                                 |
|                         | Optical format                                 | 1/2.5 inch                                      |
|                         | Chief ray angle                                | Linear shift 20° max at 3.6 mm diagonal         |
|                         | Color filter array                             | RGB-NIR in a 4x4 kernel                         |
| Package OBGA            | Package type                                   | OBGA                                            |
|                         | Package dimensions                             | 10.3 mm x 8.9 mm                                |
|                         | Ball pitch                                     | 0.8 mm                                          |
|                         | Ball array                                     | 10 x 9 balls                                    |
| Wafer reconstruction    | Silicon die size                               | 6546 x 5349 μm                                  |
| Communication interface | Sensor data interface                          | MIPI CSI-2, dual or quad lanes                  |
|                         |                                                | 300 Mbps - 1.5 Gbps                             |
|                         | Sensor control interface                       | I²C up to 1 MHz                                 |
| Output format           | Pixel output format SDR                        | GS operation: RAW10 / RAW8                      |
|                         |                                                | RS operation: RAW12 / RAW10 / RAW8              |
|                         | Pixel output format HDR<br>(after compression) | RS operation only: RAW12 / RAW10                |
| Operating conditions    | Supply voltages                                | 2.8 V analog (VANA)                             |
|                         |                                                | 1.15 V digital core (VCORE)                     |
|                         |                                                | 1.8 V digital I/O (VDDIO)                       |
|                         | External clock frequency range                 | 12 MHz to 50 MHz                                |
|                         | Junction temperature range (Tj)                | -30°C to +85°C functional                       |

**Table 2. Key features**

| Category          | Embedded features                                                                                                                                     |
|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| Common control    | Analog gains: x1 to x4                                                                                                                                |
|                   | Digital gains: x1 to x32                                                                                                                              |
|                   | 4 programmable GPIOs                                                                                                                                  |
|                   | Thermal sensors                                                                                                                                       |
| Readout control   | Cropping   NIR subsampling                                                                                                                            |
|                   | Mirror/Flip                                                                                                                                           |
|                   | Test pattern generation                                                                                                                               |
| Synchronization   | Leader mode                                                                                                                                           |
|                   | Follower mode with configurable GPIO input                                                                                                            |
|                   | Exposure strobe output signal in GS mode                                                                                                              |
|                   | MIPI readout VSYNC output signal                                                                                                                      |
|                   | Programmable delays                                                                                                                                   |
|                   | Start of exposure output signal                                                                                                                       |
| Image processing  | Automatic dark calibration                                                                                                                            |
|                   | Noise reduction                                                                                                                                       |
|                   | Dynamic defective pixel correction                                                                                                                    |
|                   | Pedestal adjustment                                                                                                                                   |
| Advanced features | Embedded Bayer reconstruction with NIR depollution (5.1 MP Bayer RGB)                                                                                 |
|                   | NIR smart upscale (5.1 MP NIR)                                                                                                                        |
|                   | Output pattern: <ul style="list-style-type: none"> <li>• Monochrome NIR (optional smart upscaling)</li> <li>• RGB-NIR</li> <li>• RGB Bayer</li> </ul> |
|                   | Context management: <ul style="list-style-type: none"> <li>• up to 4 contexts</li> <li>• configurable switching sequence</li> </ul>                   |
|                   | NIR pixel split exposure                                                                                                                              |
|                   | Histograms and statistics on programmable region                                                                                                      |
|                   |                                                                                                                                                       |

**Table 3. Typical product performances**

The product performances are provided at Tj = 60°C.

| Parameter                              |                 | Performances       |                          |
|----------------------------------------|-----------------|--------------------|--------------------------|
|                                        |                 | Global shutter     | Rolling shutter          |
| Dynamic range (SDR)                    |                 | Up to 62 dB        | Up to 69 dB              |
| Dynamic range (HDR)                    |                 | NA                 | Up to 100 dB             |
| Modulation transfer function at 940 nm |                 | Nyquist: 0.50      |                          |
|                                        |                 | Nyquist/2: 0.70    |                          |
| VB1943 Peak QE                         | NIR (940 nm)    | 23%                |                          |
|                                        | Red             | 67%                |                          |
|                                        | Green           | 74%                |                          |
|                                        | Blue            | 62%                |                          |
| VD1943 Peak QE                         | NIR (940 nm)    | 23%                |                          |
|                                        | Red             | 69%                |                          |
|                                        | Green           | 75%                |                          |
|                                        | Blue            | 63%                |                          |
| Fixed pattern noise                    |                 | 3.5 e-             | 1.1 e-                   |
| Temporal noise                         |                 | 5 e-               | 2 e-                     |
| Max frame rate                         | Full resolution | 100 fps            | 50 fps                   |
| Power consumption                      |                 | 60 fps NIR: 354 mW | 50 fps Bayer RGB: 376 mW |

## 1.2 Functional description summary

The VB1943 and VD1943 are compact global and rolling shutter image sensors featuring an RGB-NIR matrix of 2560 x 1984 pixels.

With global shutter operation, all pixels are synchronized to capture light at the same time. Once the integration time is completed for the whole matrix, each pixel information is transferred to a storage node, before being read and digitized row by row with a 10-bit ADC. This feature gets rid of the motion blur and is optimal for applications with NIR active illumination system, minimizing NIR power budget.

With rolling shutter operation, the exposure of pixels is done sequentially, row by row. It is digitized via a 12-bit ADC. The lower dark noise in rolling shutter mode provides an improved image quality. There is no GPIO support for driving illumination systems in rolling shutter mode.

In rolling shutter mode, the sensor also offers HDR feature by combining two consecutive exposures with different durations in the same frame. A FIFO buffers the pixel conversion result of the first exposure. The HDR merge bloc combines data coming from the FIFO (first exposure) and the pixel digitization of the second exposure, then generates the HDR image. The ratio of exposure can be up to 64, providing 18-bit resolution images.

The RGB-NIR image input stream goes through the internal ISP where dark level subtraction, digital gain, pedestal, pixel correction, noise reduction, image histograms, and statistics are applied.

The output stream can be the RGB-NIR input image, but to fit ISPs of conventional application hosts, the sensor can reconstruct and transmit a color Bayer image depolluted from NIR content. It can also extract and transmit the NIR pixels only as gray scale, smart upsampled to the input image size.

The images are output as frames of RAW8, RAW10, or RAW12 data through a MIPI CSI-2 scalable to two or four data lanes. When the output resolution is not the native ADC resolution (10 bit for global shutter or 12 bit for rolling shutter), the image is compressed following a 32 points PWL curve.

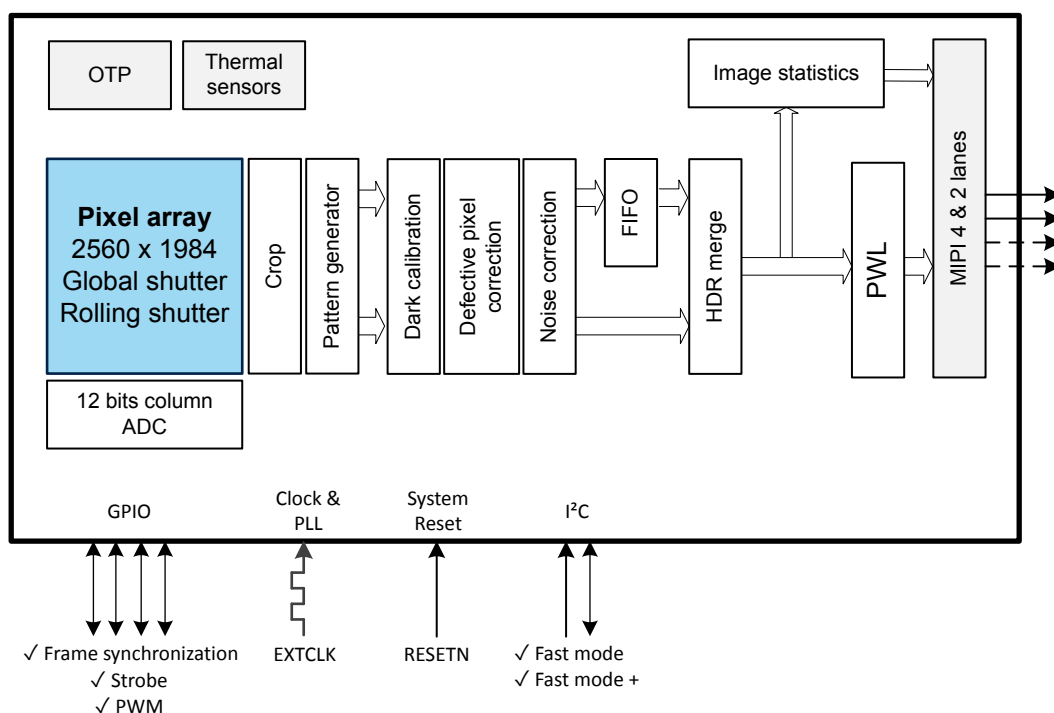
A MIPI line containing image status can be added to prior image content (TOP status line), statistics, and histograms can be appended at the end of each image (bottom status line).

The sensor can operate in leader mode (free running) or follower mode based on triggering event on one selected GPIO.

The device is fully configurable through the I<sup>2</sup>C interface and provides flexible frame-to-frame parameter configuration changes via the use of programmable contexts.

It also embeds a one-time programmable (OTP) nonvolatile memory, structured in 32-bit words that can be used for traceability and customer data.

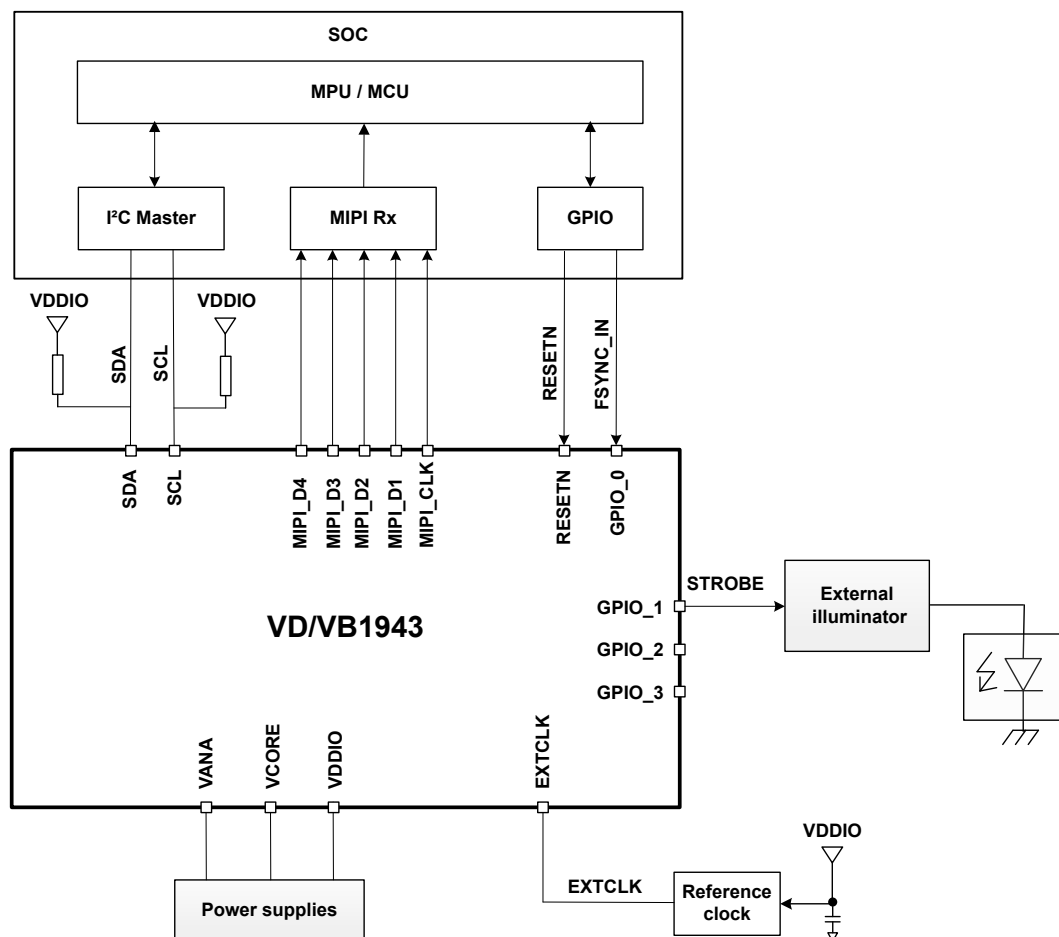
**Figure 1. Functional block diagram**



### 1.3 Typical configuration into application

The typical device integration is shown in the figure below:

**Figure 2. Typical application implementation**



On top of interfacing with SoC/MCU, the sensor can support the following features:

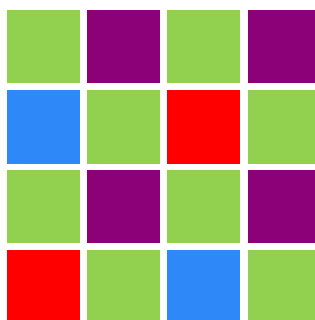
- Synchronization with a second camera module as leader or follower mode.
- Control external illumination system synchronized to exposure period with configurable PWM generation.
- Additional input/output digital control capabilities.

## 2 Optical characteristics

### 2.1 Device specific color filter array

When the sensor array is read, the output order of red, green, blue, and NIR depends on the settings of the vertical flip and horizontal mirror. [Figure 3. Color filter array](#) shows the readout order of the default settings when the vertical flip and horizontal mirror are both turned off. Refer to the product user manual for a complete description of the different output patterns according to the orientation.

**Figure 3. Color filter array**



RGB-NIR 4x4

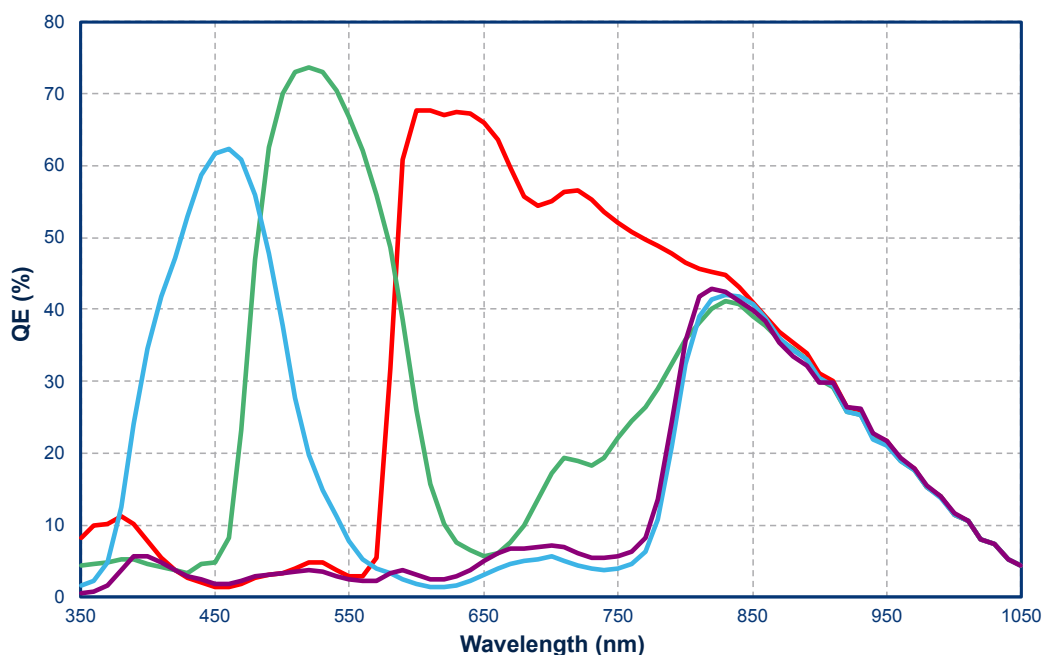
### 2.2 Optical performance

Typical pixel performance is described in the curves below.

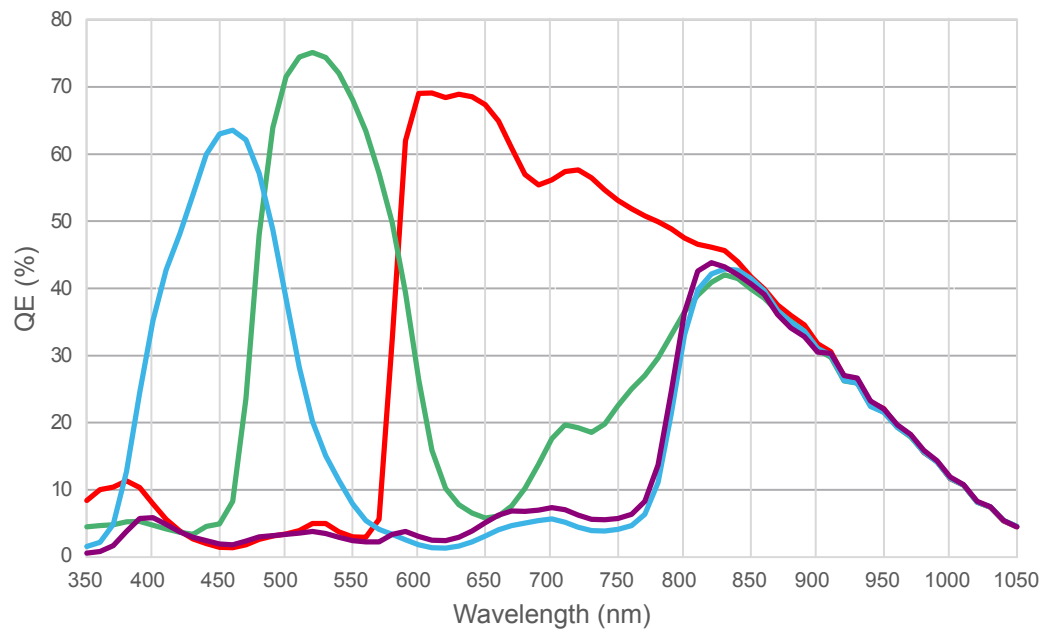
#### 2.2.1 Quantum efficiency

Quantum efficiency (QE) is the percentage of incident photons converted into electrons.

**Figure 4. VB1943 peak QE (60°C)**



**Figure 5. VD1943 peak QE (60°C)**



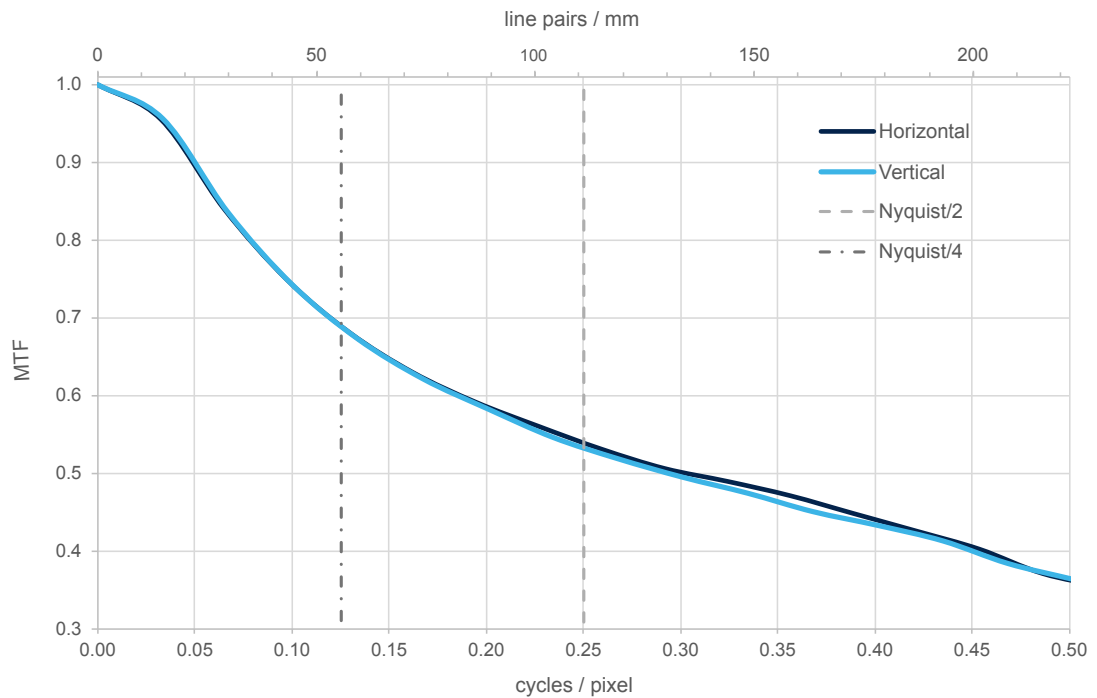
### 2.2.2 Modulation transfer function

The modulation transfer function (MTF) measures the ability of the devices to differentiate spatial frequencies.

The MTF value represents the contrast restitution for the corresponding spatial frequency. In other words, it describes the contrast attenuation. It is a sharpness indicator that quantifies the extent to which image sensors can capture and discriminate fine detailed contrast of objects within the field of view.

The figure below presents the on-axis MTF, measured in a 100x100 pixel ROI using the slanted-edge method, following ISO12233 sfrmat5.

**Figure 6. Modulation transfer function (MTF) on axis at 940 nm**



### 2.2.3 Microlens shift and CRA matching

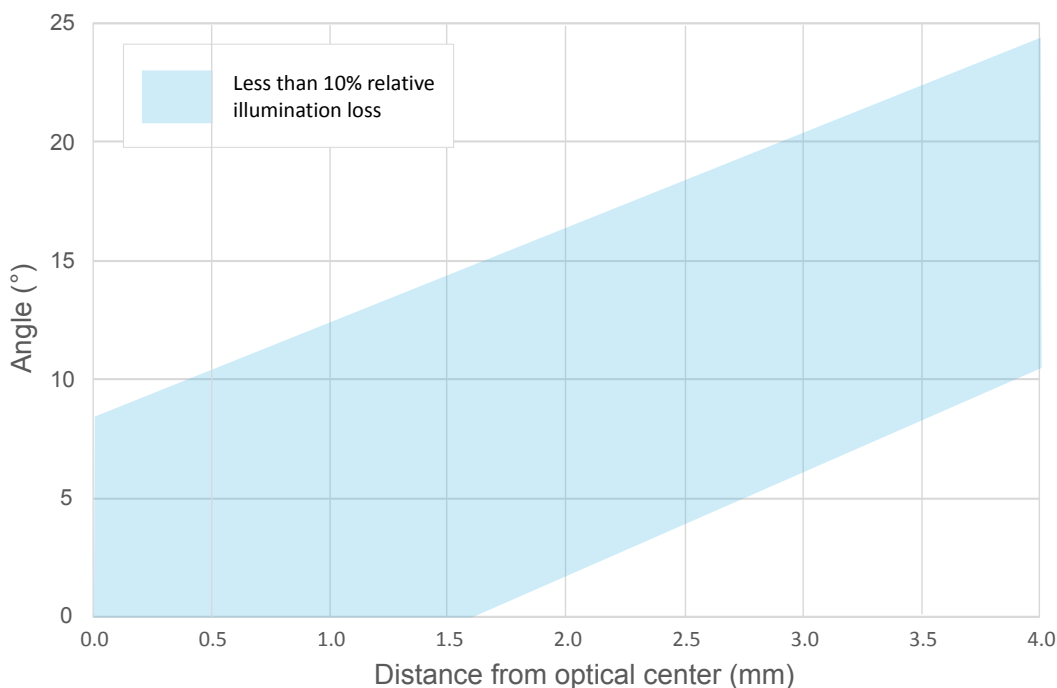
The VB1943 and VD1943 include an array of microlenses. One microlens being placed on top of each pixel to better focus light on the photosensitive area as a magnifying glass so that incoming light is optimized in the image sensor.

The microlens shift is linear with a maximum of 20° in corners. The table provides the optimal lens chief ray angle (CRA) with regard to distance from the optical center.

With NIR source (940 nm), there is a significant tolerance to lens CRA because the relative illumination remains higher than 90% over the full matrix. This is true even with significant mismatch of lens CRA to microlens shift.

With visible source, there is a general tolerance to the lens CRA, see the figure below. Up to 10° mismatch, the relative illumination loss is much lower than the one from the lens itself (vignetting).

**Figure 7. Lens CRA tolerance in visible (green)**



**Table 4. Optimal CRA**

| Distance (mm) | CRA (deg) |
|---------------|-----------|
| 0.0           | 0         |
| 0.5           | 3         |
| 1.0           | 6         |
| 1.5           | 8         |
| 2.0           | 11        |
| 2.5           | 14        |
| 3.0           | 17        |
| 3.5           | 19        |
| 3.6           | 20        |

## 3 Product integration

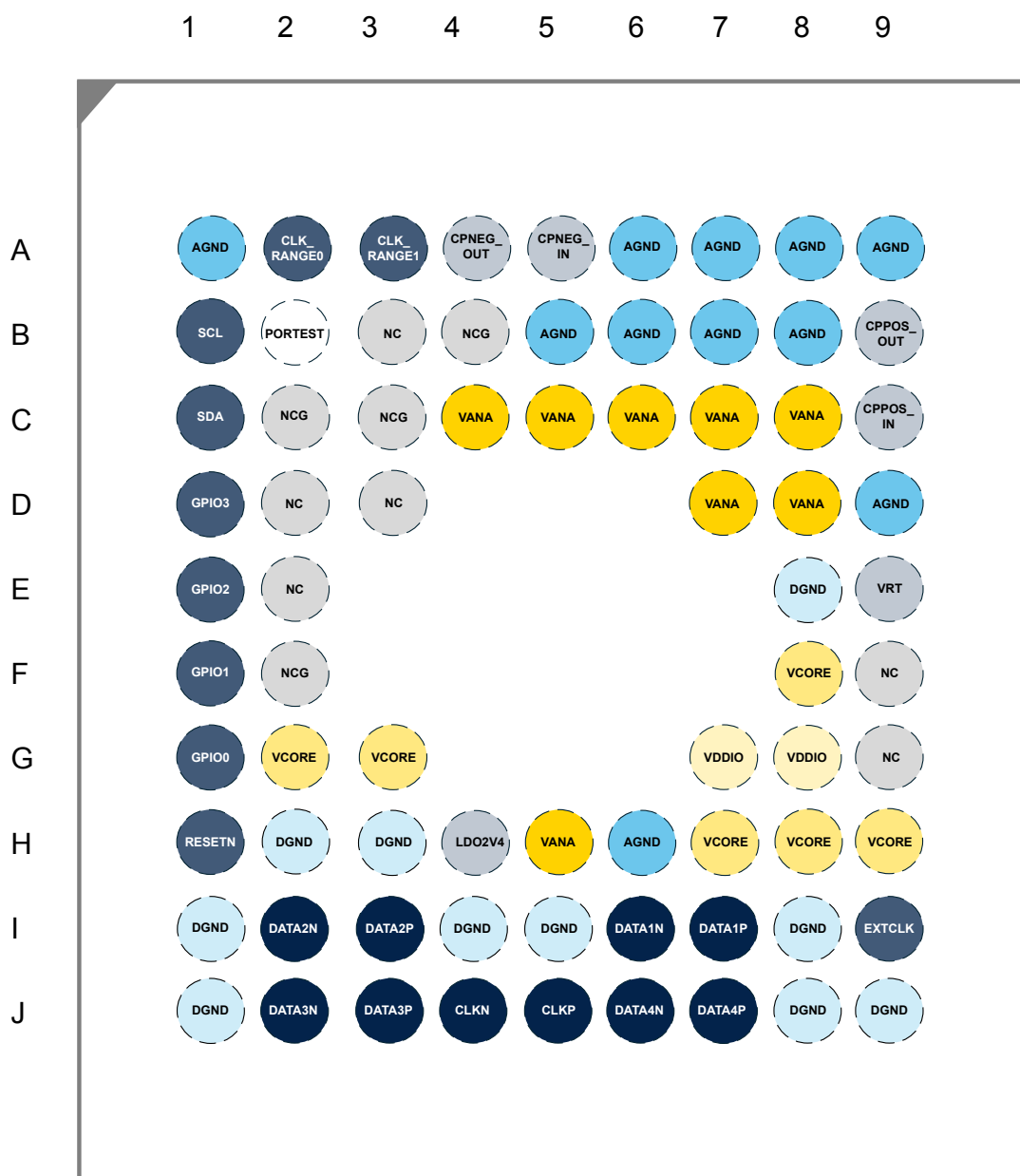
### 3.1 Device signal descriptions

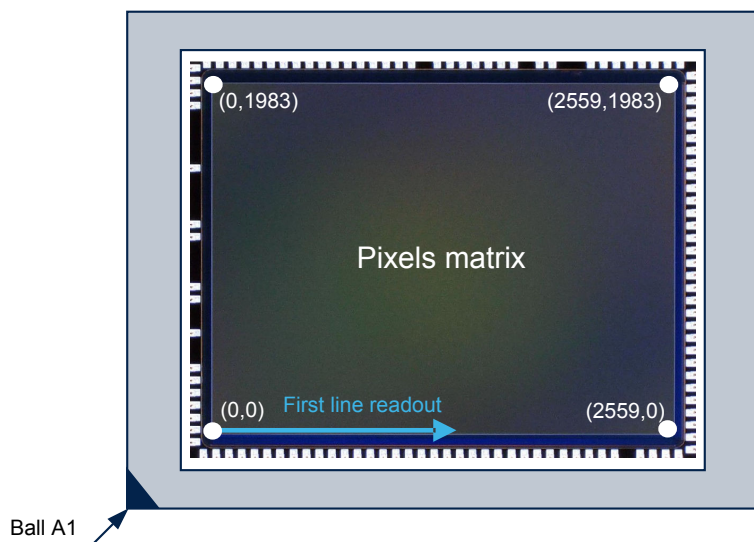
**Table 5. Signal descriptions**

| Ball name       | Type      | Description                                                     | Reset state | Reference supply |
|-----------------|-----------|-----------------------------------------------------------------|-------------|------------------|
| Power supply    |           |                                                                 |             |                  |
| VANA            | PWR       | 2.8 V power supply for the analog blocks                        | —           | 2.8 V            |
| VCORE           |           | 1.15 V power supply for the digital core                        | —           | 1.15 V           |
| VDDIO           |           | 1.8 V power supply for the input/output                         | —           | 1.8 V            |
| DGND            |           | Digital ground                                                  | —           | VDDIO            |
| AGND            |           | Analog ground                                                   | —           | VANA             |
| Reference       |           |                                                                 |             |                  |
| LDO2V4          | REF       | Internal reference (must be connected)                          | —           | VANA             |
| CPNEG_IN        |           | Must be connected to CPNEG_OUT                                  | —           | VANA             |
| CPNEG_OUT       |           | Must be connected to CPNEG_IN                                   | —           |                  |
| CPPOS_IN        |           | Must be connected to CPPOS_OUT                                  | —           |                  |
| CPPOS_OUT       |           | Must be connected to CPPOS_IN                                   | —           |                  |
| VRT             |           | Internal reference (must be connected)                          | —           | VANA             |
| CSI-2 interface |           |                                                                 |             |                  |
| DATA1P, DATA1N  | MIPI DPHY | CSI-2 data lane 1, positive and negative                        | Low         | VCORE            |
| DATA2P, DATA2N  |           | CSI-2 data lane 2, positive and negative                        |             |                  |
| DATA3P, DATA3N  |           | CSI-2 data lane 3, positive and negative                        |             |                  |
| DATA4P, DATA4N  |           | CSI-2 data lane 4, positive and negative                        |             |                  |
| CLKP, CLKN      |           | CSI-2 clock, positive and negative                              |             |                  |
| Host interface  |           |                                                                 |             |                  |
| RESETN          | I         | Reset active low                                                | —           | VDDIO            |
| SDA             | I/O       | I <sup>2</sup> C data                                           | —           |                  |
| SCL             | I         | I <sup>2</sup> C clock                                          | —           |                  |
| GPIO0           | I/O       | General purpose I/O and strobe light control<br>(FAIL SAFE pad) | Input       |                  |
| GPIO1           |           |                                                                 |             |                  |
| GPIO2           |           |                                                                 |             |                  |
| GPIO3           |           |                                                                 |             |                  |
| CLK_RANGE0      | I         | To select the range of the input clock<br>(FAIL SAFE pad)       | —           |                  |
| CLK_RANGE1      | I         |                                                                 |             |                  |
| EXTCLK          | I         | Input clock                                                     | —           |                  |
| Other balls     |           |                                                                 |             |                  |
| PORTEST         | I         | Must be connected to the digital ground                         | —           | VDDIO            |
| NC              | —         | Must not be connected and must be left floating                 | —           | —                |
| NCG             | I         | Can be left floating or connected to analog ground              | —           | VANA             |

### 3.1.1 OBGA package ball assignment

**Figure 8. Ball assignment (see-through view)**



**Figure 9. Die orientation in OBGA package (top view)**

**Table 6. Ball assignment table**

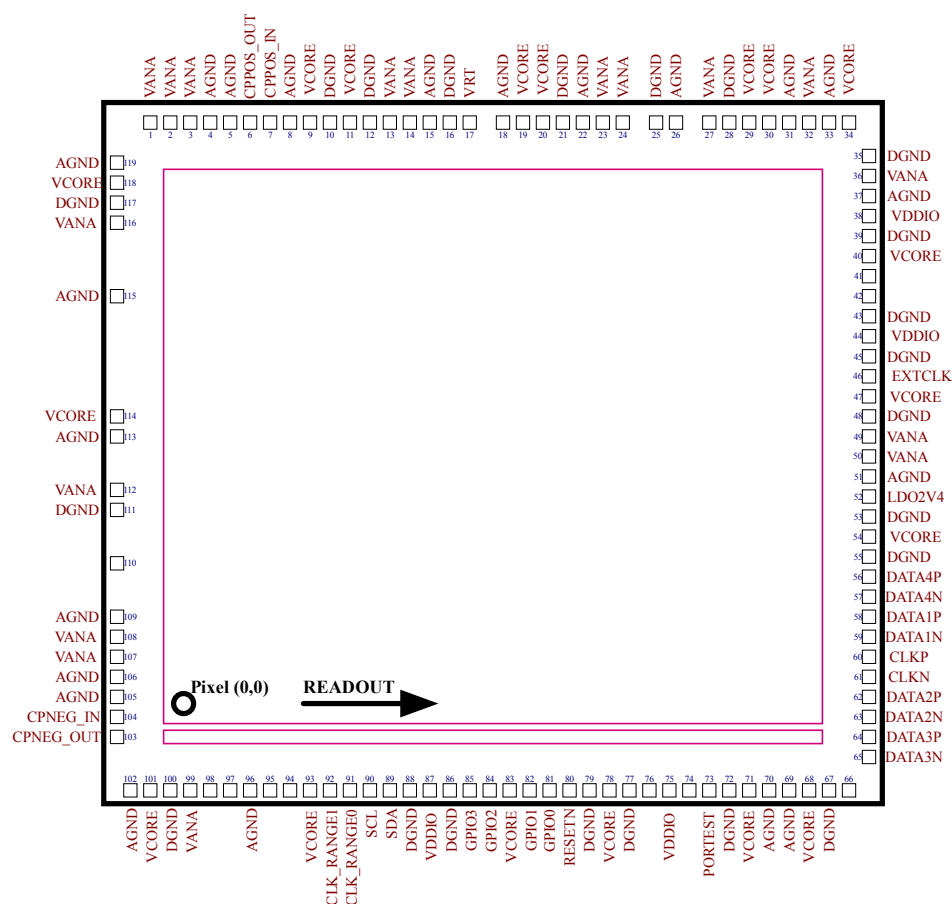
| Ball ID | Signal     |
|---------|------------|
| A1      | AGND       |
| A2      | CLK_RANGE0 |
| A3      | CLK_RANGE1 |
| A4      | CP_NEG_OUT |
| A5      | CP_NEG_IN  |
| A6      | AGND       |
| A7      | AGND       |
| A8      | AGND       |
| A9      | AGND       |
| B1      | SCL        |
| B2      | PORTEST    |
| B3      | NC         |
| B4      | NCG        |
| B5      | AGND       |
| B6      | AGND       |
| B7      | AGND       |
| B8      | AGND       |
| B9      | CP_POS_OUT |
| C1      | SDA        |
| C2      | NCG        |
| C3      | NCG        |
| C4      | VANA       |
| C5      | VANA       |
| C6      | VANA       |
| C7      | VANA       |

| Ball ID | Signal    |
|---------|-----------|
| C8      | VANA      |
| C9      | CP_POS_IN |
| D1      | GPIO3     |
| D2      | NC        |
| D3      | NC        |
| D7      | VANA      |
| D8      | VANA      |
| D9      | AGND      |
| E1      | GPIO2     |
| E2      | NC        |
| E8      | DGND      |
| E9      | VRT       |
| F1      | GPIO1     |
| F2      | NCG       |
| F8      | VCORE     |
| F9      | NC        |
| G1      | GPIO0     |
| G2      | VCORE     |
| G3      | VCORE     |
| G7      | VDDIO     |
| G8      | VDDIO     |
| G9      | NC        |
| H1      | RESETN    |
| H2      | DGND      |
| H3      | DGND      |
| H4      | LDO2V4    |
| H5      | VANA      |
| H6      | AGND      |
| H7      | VCORE     |
| H8      | VCORE     |
| H9      | VCORE     |
| J1      | DGND      |
| J2      | DATA2N    |
| J3      | DATA2P    |
| J4      | DGND      |
| J5      | DGND      |
| J6      | DATA1N    |
| J7      | DATA1P    |
| J8      | DGND      |
| J9      | EXTCLK    |
| K1      | DGND      |

| Ball ID | Signal |
|---------|--------|
| K2      | DATA3N |
| K3      | DATA3P |
| K4      | CLKN   |
| K5      | CLKP   |
| K6      | DATA4N |
| K7      | DATA4P |
| K8      | DGND   |
| K9      | DGND   |

### 3.1.2 Bare die pad assignment

**Figure 10. Pad assignment**

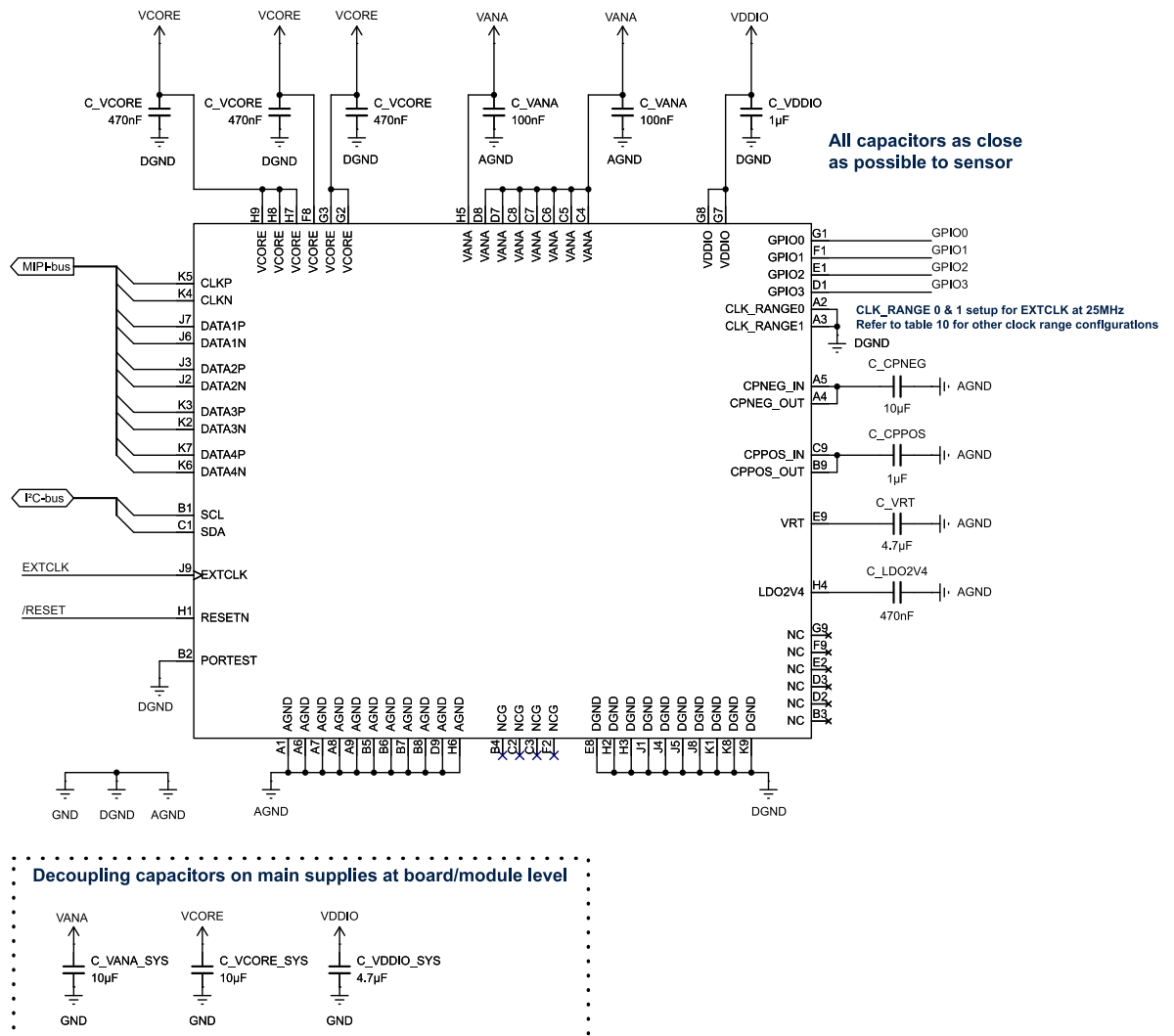


Note that pad mechanical positions are described in [Section 8.2: Die mechanical description](#).

## 3.2 Application schematic

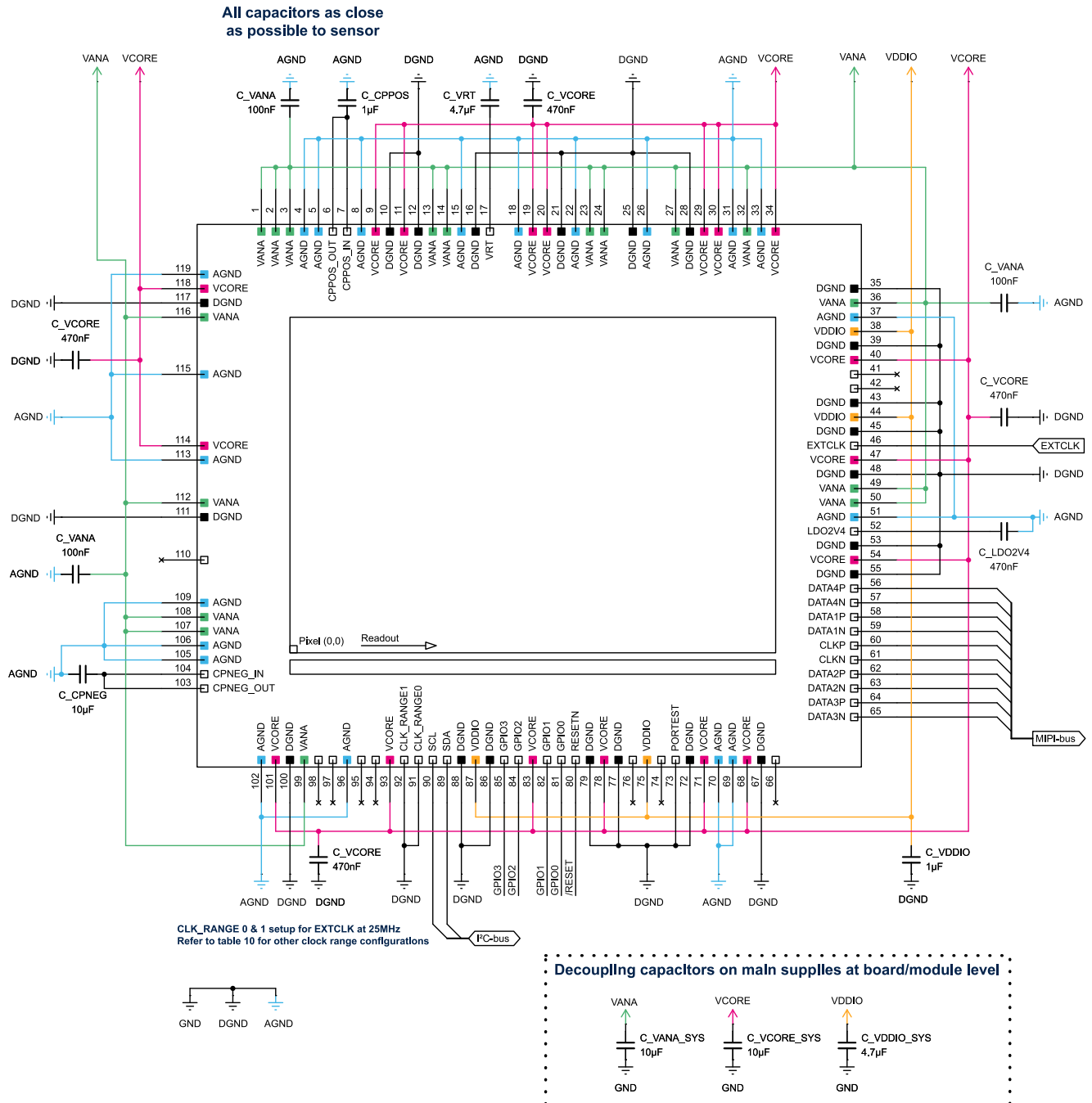
### 3.2.1 OBGA typical application schematic

Figure 11. OBGA typical application schematic



### 3.2.2 Bare die typical application schematic

Figure 12. Bare die typical application schematic



### 3.2.3 Additional external components

Dedicated capacitors are required to complete the circuit, especially to filter out supply noise properly. The table below presents the range of the different capacitances. Values are provided after voltage derating only; capacitors should be selected to maintain their capacitance within the range while considering operating conditions (tolerance, aging, temperature).

Large bulk capacitors are recommended to filter low frequency at the entry point of the main power supply on the PCB.

- C\_VANA\_SYS
- C\_VCORE\_SYS

Other capacitors shall be placed as close to the pins as possible.

**Table 7. Capacitor needs**

| Name        | Associated pin         | Voltage | Minimum capacitance | Maximum capacitance | Operating frequencies | Ground | Purpose           |
|-------------|------------------------|---------|---------------------|---------------------|-----------------------|--------|-------------------|
| C_VANA      | VANA                   | 2.8 V   | 100 nF              | —                   | 160 MHz               | AGND   | Supply decoupling |
| C_VANA_SYS  | VANA                   | 2.8 V   | 10 $\mu$ F          | —                   | 160 MHz               | AGND   | Supply decoupling |
| C_VCORE     | VCORE                  | 1.15 V  | 470 nF              | —                   | 1.0 to 1.5 GHz        | DGND   | Supply decoupling |
| C_VCORE_SYS | VCORE                  | 1.15 V  | 10 $\mu$ F          | —                   | 160 to 200 MHz        | DGND   | Supply decoupling |
| C_VDDIO     | VDDIO                  | 1.8 V   | 1 $\mu$ F           | —                   | 1 MHz                 | DGND   | Supply decoupling |
| C_CPPOS     | CPPOS_IN,<br>CPPOS_OUT | 3.55 V  | 470 nF              | 1 $\mu$ F           | 500 MHz               | AGND   | Bulk capacitor    |
| C_CPNEG     | CPNEG_IN,<br>CPNEG_OUT | -2.0 V  | 4 $\mu$ F           | 12 $\mu$ F          | 500 MHz               | AGND   | Bulk capacitor    |
| C_LDO2V4    | LDO2V4                 | 2.4 V   | 100 nF              | 1 $\mu$ F           | DC                    | AGND   | Bulk capacitor    |
| C_VRT       | VRT                    | 2.5 V   | 2.4 $\mu$ F         | 5 $\mu$ F           | DC                    | AGND   | Bulk capacitor    |

### 3.3 Layout guidelines

In addition to the component selections, their placement and layout play a critical role.

#### 3.3.1 General rules

- Use power and ground planes to supply power to the sensor.
- Join AGND and DGND into one single, solid ground plane underneath the sensor.
- Connect this GND plane to the sensor pins with one via per GND pin when possible.
- Maximize copper fill on the power planes near the sensor and use vias to improve heat transfer from the sensor. Do not place any power dissipative component under or close to the sensor.

#### 3.3.2 Charge pumps (positive and negative)

- Connect CPNEG\_IN and CPNEG\_OUT with a short track. Place the bulk capacitor C\_CPNEG on this path, and not on an isolated track.
- Connect CPPOS\_IN and CPPOS\_OUT with a short track. Place the bulk capacitor C\_CPPOS on this path, and not on an isolated track.

#### 3.3.3 CSI-2 signal traces

- Route the high-speed signal pairs of the MIPI CSI-2 interface with balanced and controlled impedance traces (50 ohms common-mode and 100  $\Omega$  differential). This is a requirement for high-speed signaling.
- Route each pair together and match them in length to minimize skew below 10 ps.
- Keep traces on layers adjacent to the ground plane.

### 3.3.4 Electromagnetic compatibility (EMC)

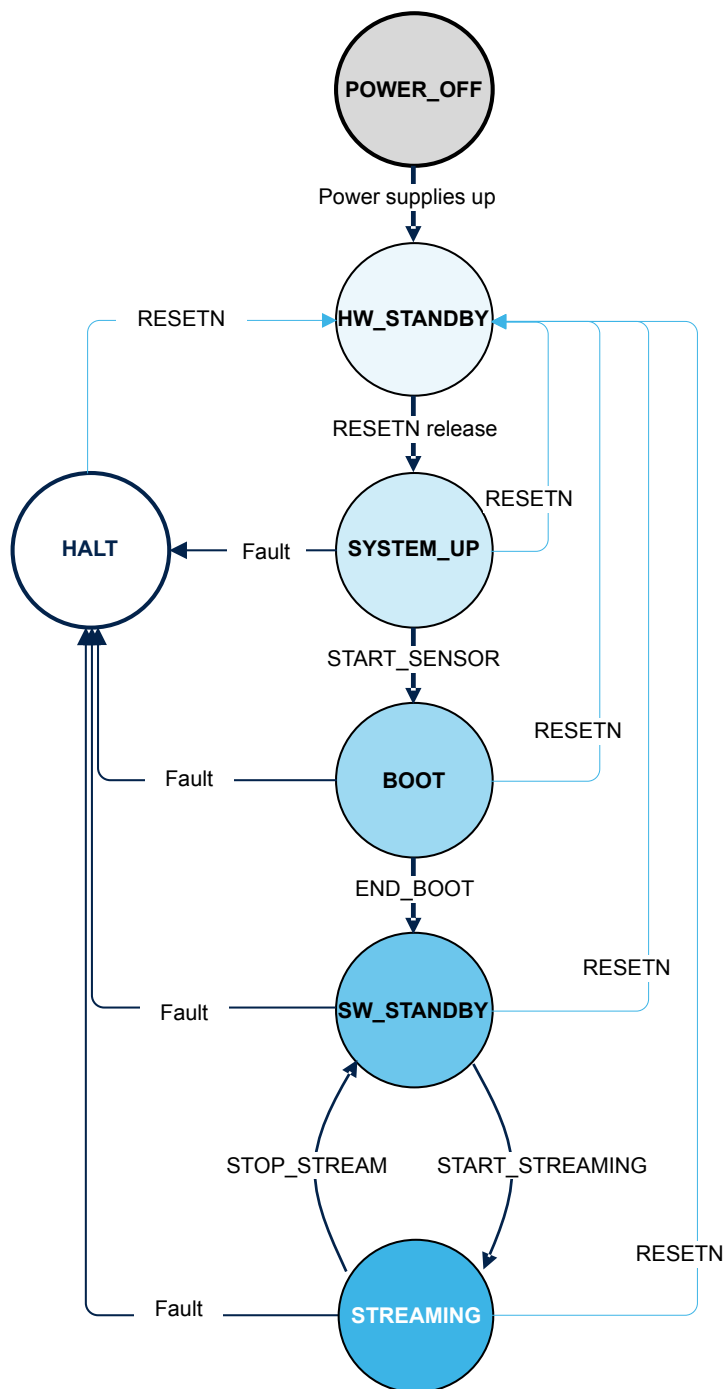
Electromagnetic compatibility (EMC) recommendations are linked to PCB design and routing. Below are some guidelines:

- MIPI related recommendations:
  - Use common-mode filters (ECMF) for MIPI data lanes
  - Bury the MIPI tracks (stripline transmission line type)
  - Minimize the skew by equalizing length of MIPI lanes track to ensure the same signal propagation time
  - Preserve signal integrity using matched lines having a 50 ohms common-mode impedance and 100 ohms differential impedance.
- Power supplies related recommendations:
  - Use ferrites for parasitic signal filtering
  - Add decoupling capacitors (refer to [Section 3.2.3: Additional external components](#))
    - As close as possible from the power supplies
    - For each power domain, use multiple capacitance values in different ranges to spread the self-ringing frequency
    - Smaller values are fitted closer to the sensor
  - Use a dedicated power supply for the sensor, not shared with other components
- Ground management:
  - Add a ground ring all around the PCB and on all layers. Interconnect the ground planes on the different layers using a multitude of vias
- Limit overshoots on external clock
- Ensure that there is no track close to the PCB border

## 4 Product features

### 4.1 Device state machine and state definition

Figure 13. Firmware state machine



**POWER\_OFF state**

In this state, the power supplies are switched off.

**HW\_STANDBY state**

In this state the device is supplied, EXTCLK must run, and the RESETN pin is asserted LOW. The sensor is ready to start.

**SYSTEM\_UP state**

In system-up state, I<sup>2</sup>C operations are allowed. Firmware execution is started. The external clock frequency and eventually new I<sup>2</sup>C address can be configured.

**BOOT state**

After execution of the START\_SENSOR command, the sensor transitions to boot state. The internal clocks are initialized, and NVM content is retrieved by the firmware.

**SW\_STANDBY state**

After execution of command END\_BOOT, the sensor transitions to software standby state. At that point, I<sup>2</sup>C instructions are sent by the host to configure MIPI settings, static and dynamic streaming settings.

**STREAMING state**

After execution of the command STREAMING, the sensor transitions to streaming state and starts transmitting frames over the MIPI interface. In streaming state, only dynamic settings can be changed.

The system status can be read via I<sup>2</sup>C in UI status registers, or from the MIPI TOP ISL.

**HALT state**

In HALT state, streaming is interrupted and the sensor goes in a dead-end state, only the cycling RESETN pin can exit the sensor from HALT state.

The I<sup>2</sup>C is still functional to allow the host to read the UI status registers to assess the error detected.

## 4.2 Device power up/power down sequence and general control interfacing

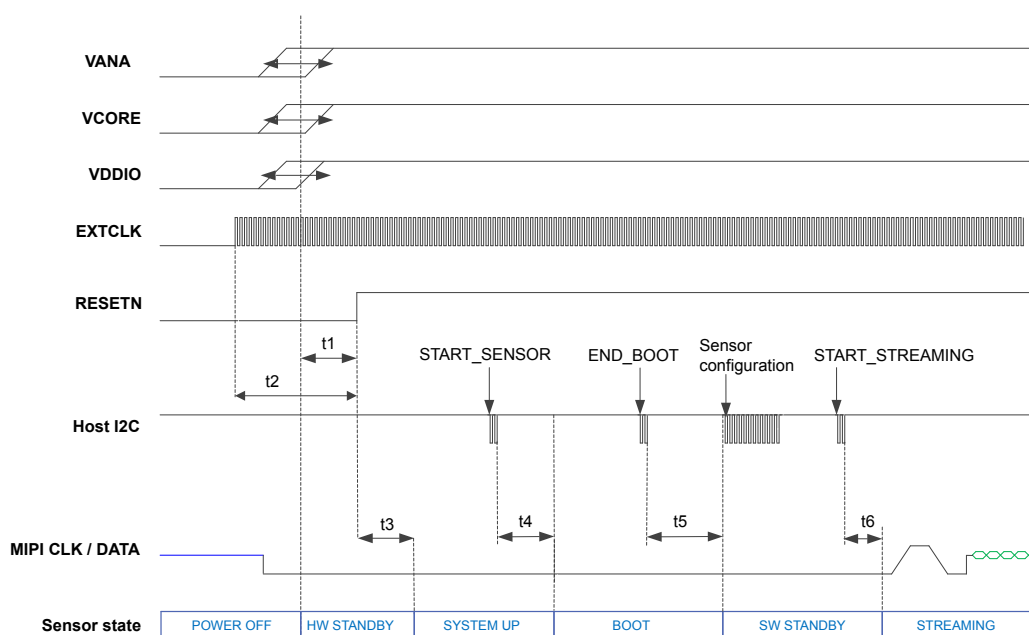
### 4.2.1 Device power up sequence

To power on the device, all external supplies (VANA, VCORE, VDDIO) must be properly provided according to the device characteristics described in [Section 7: Electrical characteristics](#). As long as RESETN is low, the device is in HW\_STANDBY state.

The power on sequence must be done as follows:

1. Provide all the external supplies (VANA, VCORE, VDDIO) according to the device characteristics described in [Section 7: Electrical characteristics](#). As long as RESETN is low, the device is in HW\_STANDBY state.
2. External supplies can be switched on in any order, as well as EXTCLK.
3. Set RESETN to high.

**Figure 14. Device power up to streaming mode sequence**



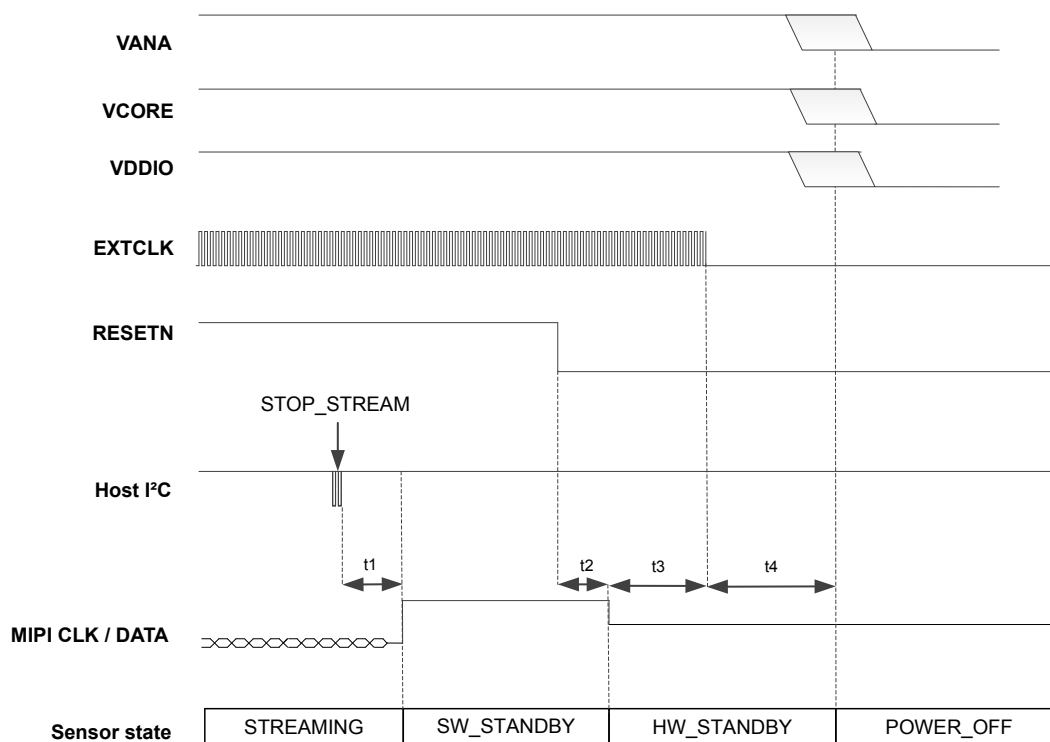
**Table 8. Power up sequence timings**

| Timing | Description                                     | Typical delay<br>(EXTCLK= 25 MHz, I <sup>2</sup> C 1 MHz) |
|--------|-------------------------------------------------|-----------------------------------------------------------|
| t1     | POWER SUPPLIES stable to RESETN signal released | 100 $\mu$ s                                               |
| t2     | CLOCK stable to RESETN signal released          | 1 $\mu$ s                                                 |
| t3     | RESETN signal released to SYSTEM_UP state       | 5.5 ms                                                    |
| t4     | START_SENSOR command to BOOT state              | 1.8 ms                                                    |
| t5     | END_BOOT command to SW_STANDBY state            | 4 ms                                                      |
| t6     | START_STREAMING command to STREAMING state      | 4 ms                                                      |

### 4.2.2 Device power down sequence

The power down sequence must be done as follows:

1. Send the command to stop the streaming and wait until sensor reaches SW\_STANDBY state.
2. Release RESETN pin (low level).
3. Shutdown EXTCLK.
4. External supplies can be switched off in any order.

**Figure 15. Power down sequence**

**Table 9. Power down sequence timings**

| Timing | Description                              | Typical delay<br>(EXTCLK = 25 MHz) |
|--------|------------------------------------------|------------------------------------|
| t1     | STOP_STREAM command to SW_STANDBY state  | Less than two frames periods       |
| t2     | RESETN signal assertion HW_STANDBY state | Simultaneous                       |
| t3     | HW_STANDBY state to EXTCLK stopped       | Any                                |
| t4     | EXTCLK stopped to POWER SUPPLIES down    | Any                                |

### 4.2.3 Power supplies

Three power supplies required by the sensor are:

- 2.8 V for the analog blocks
- 1.15 V for the core digital logic and MIPI CSI-2 output driver
- 1.8 V for the digital I/Os

The pixel array requires different positive and negative voltages, all internally generated by charge pumps and regulators. Four voltage references, internally generated, need external decoupling capacitors. The internal CPU handles the entire power management of the sensor to ensure the lowest power consumption at any given time.

The sensor's internal CPU handles the entire power management to ensure the lowest power consumption. Internal voltage reference supplies are powered up as soon as a streaming command is issued.

### 4.2.4 Clock and phase-locked loop (PLL)

An input clock is required from an external digital clock source in the range of 12 MHz to 50 MHz. Firmware is preconfigured for a 25 MHz external source clock. Two built-in, phase-locked loop (PLL) blocks generate all necessary internal clocks for the pixel array, processing pipe, embedded CPU, and output interface.

The internal CPU handles the PLL startup/down sequence when the device is entering/stopping the streaming mode to ensure the lowest power consumption.

#### 4.2.4.1 Input clock configuration

Because the input clock (EXTCLK) supports a wide range of frequencies (12 MHz to 50 MHz), it is mandatory to select a sub-range by configuring two inputs of the device: CLK\_RANGE0 and CLK\_RANGE1.

Moreover, there is a value for each configuration to specifically optimize the boot time of the sensor. Refer to the table below:

**Table 10. Input clock configuration**

| CLK_RANGE0 | CLK_RANGE1 | Range of the input clock | Optimal input clock |
|------------|------------|--------------------------|---------------------|
| Low        | Low        | 25 MHz (default value)   | 25 MHz              |
| High       | Low        | 12 – 24 MHz              | 24 MHz              |
| Low        | High       | 24.01 – 36 MHz           | 36 MHz              |
| High       | High       | 36.01 – 50 MHz           | 50 MHz              |

The reference supply of these inputs is VDDIO.

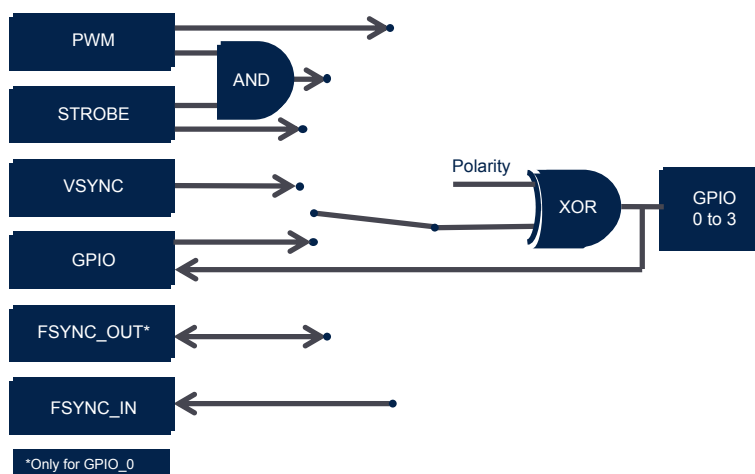
#### 4.2.5 General-purpose control pin behavior

The sensor provides four GPIOs with different modes:

- Frame start synchronization
- Strobe output
- PWM output
- Strobe PWM output
- Generic GPIO

All GPIOs have configurable polarity (see figure below).

**Figure 16. GPIO section modes**



GPIOs can also be configured to input state.

The typical pull-down value is 50 kΩ.

The below table provides the behavior of the different GPIOs according to the sensor state.

**Table 11. GPIO behavior for the different FSM states**

| GPIO       | HW_STANDBY    |           | SYSTEM_UP/BOOT |           | SW_STANDBY    |           | STREAMING GP_in or DISABLED mode |           |
|------------|---------------|-----------|----------------|-----------|---------------|-----------|----------------------------------|-----------|
|            | I/O direction | Mode      | I/O direction  | Mode      | I/O direction | Mode      | I/O direction                    | Mode      |
| GPIO_0     | INPUT         | Pull down | OUT            | Drive low | INPUT         | Pull down | INPUT                            | Pull down |
| GPIO_1     | INPUT         | HiZ       | OUT            | Drive low | INPUT         | Pull down | INPUT                            | Pull down |
| GPIO_2     | INPUT         | HiZ       | OUT            | Drive low | INPUT         | Pull down | INPUT                            | Pull down |
| GPIO_3     | INPUT         | HiZ       | INPUT          | Pull down | INPUT         | Pull down | INPUT                            | Pull down |
| CLK_RANGE0 | INPUT         | Pull down | INPUT          | Pull down | INPUT         | Pull down | INPUT                            | Pull down |
| CLK_RANGE1 | INPUT         | Pull down | INPUT          | Pull down | INPUT         | Pull down | INPUT                            | Pull down |

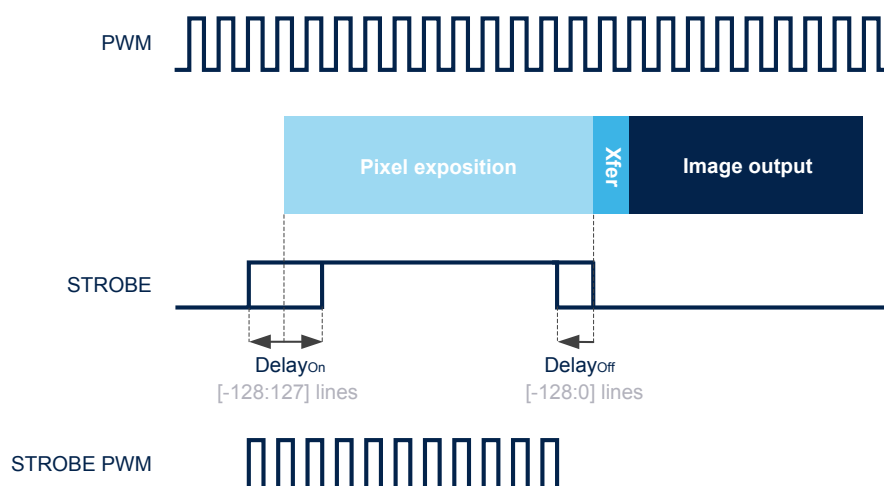
#### 4.2.5.1 Device synchronization modes

The sensor has two synchronization modes:

1. Leader: In this mode, the device controls the internal frame sequencing and can synchronize other follower sensors with the FSYNC\_OUT signal (only available on GPIO0).
2. Follower: In this mode, the internal sequencer starts the pixel exposure when receiving the synchronization signal rising edge FRAME\_START. A programmable delay can be added between the synchronization signal and the start of integration.

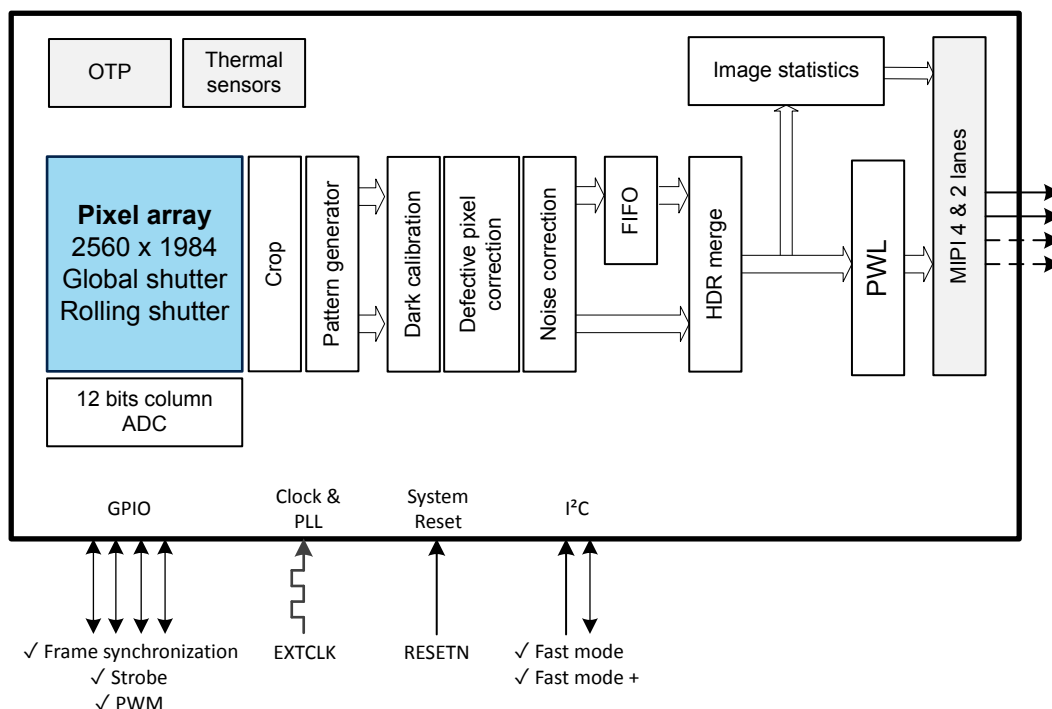
#### 4.2.5.2 Device peripheral synchronization and PWM capability

In both synchronization modes, the device can generate on GPIOs PWM or STROBE PWM signals. It can be used for driving an illumination system or other. The STROBE signal available on any GPIO is synchronized with the sensor integration period as shown in the figure below.

**Figure 17. Pulse-width modulation (PWM) and STROBE overview**


## 4.3 Image processing features

**Figure 18. Functional block diagram**

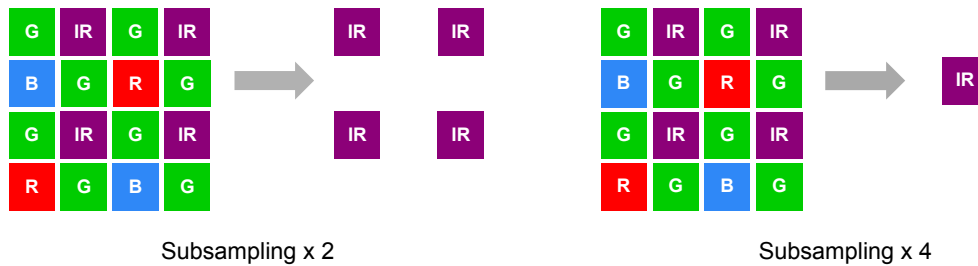


The video pipe performs several features designed to ensure high image quality. These features include:

- Analog subsampling (NIR pixel only)
- Analog gain
- Digital gain
- Pedestal insertion
- Exposure and split exposure control
- Global shutter / rolling shutter
- Test pattern generation
- Automatic dark calibration (linked to temperature)
- Dynamic defective pixel correction
- Dynamic gaussian noise reduction
- Image crop
- Image flip and mirror
- RGB NIR to Bayer RGB conversion
- RGB NIR to mono NIR conversion
- HDR merge (rolling shutter only)
- PWL compression
- Output interface
- Embedded status lines
- Exposure statistics
- Exposure histograms
- Context management

### 4.3.1 Analog subsampling

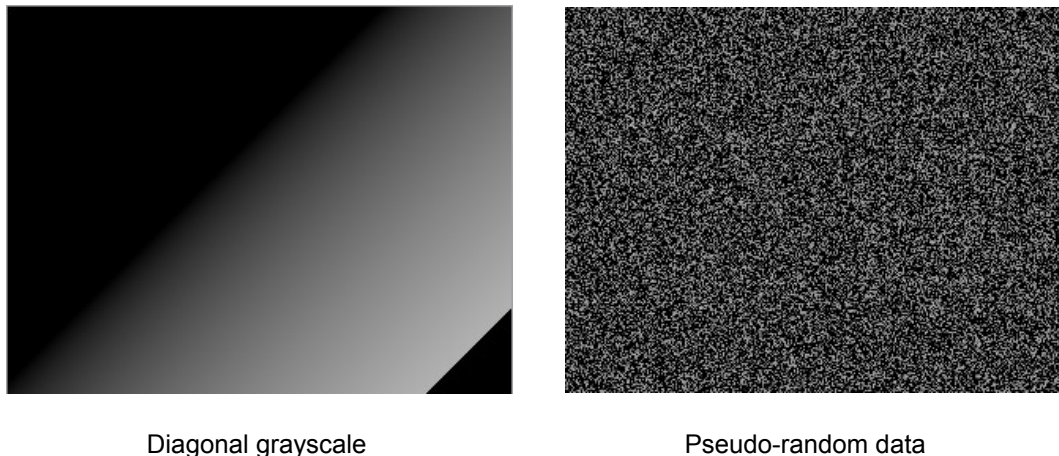
The device supports x2, x4, and x32 subsampling for NIR pixels, which reduces overall image size and keeps the same FoV. Subsampling is applied vertically and horizontally.

**Figure 19. Subsampling example**


### 4.3.2 Test pattern generation

The pattern generator allows the generation of digital patterns in the output frame. Available patterns are:

- Diagonal grayscale
- Pseudo-random data PN28

**Figure 20. Available patterns**


### 4.3.3 Dynamic defective pixel correction

Active pixels are automatically corrected by a dynamic algorithm embedded in the sensor ISP. This mechanism can be deactivated for debugging purposes and for specific use cases such as structured light.

Small particles on the image matrix array, pixels with upper or lower sensitivity than neighbors, and leaky pixels among the millions of pixels of the matrix appear as unusual spots, being either too dark or too bright.

The embedded automatic defective pixel correction removes defects by performing on-the-fly correction of single or paired defective pixels.

Hence, defect-free images are provided directly from the sensor without requiring further postprocessing at the application level.

The feature performs as follows:

1. For a defined pixel P, the algorithm identifies if there are spatial gradients in the area by considering the values of the surrounding pixels in the same color plane.
2. The algorithm computes the theoretical value  $V_{theory}$  that pixel P would have if it was following the spatial gradients identified in the area.
3. The actual value  $V_{actual}$  of pixel P is compared to the theoretical value  $V_{theory}$ .
4. If  $V_{actual}$  is too far from  $V_{theory}$ , considering a certain range of tolerance, the pixel P is considered defective because of its unusual value, and the value of pixel P is replaced by  $V_{theory}$ .

Tunable tolerance thresholds allow a perfect balance between systematic defect correction and preserving textures/patterns in the image for various use cases.

Defective pixel correction operates on all the color planes of the RGB-NIR image.

#### 4.3.4 Automatic dark calibration

A dark calibration is performed by extracting the dark rows from the stream, then averaging and removing the dark noise from pixels in the active image.

The pixel matrix has dedicated lines with shielded pixels that are used as references to estimate and subtract dynamically the dark level from the active image. This keeps the dark level constant regardless of the temperature, exposure time, or analog gain changes.

Temporal smoothing and fractional bit dithering are applied to avoid a sudden one-code step.

This block also embeds a programmable digital gain control feature, independent for each channel (R,G,B,NIR) ,with a granularity of 1/256 code.

And last, a configurable pedestal can offset the dark level along the ISP pipe.

#### 4.3.5 Cropping

The image dimension can be horizontally and vertically reduced to a smaller region of interest (ROI) with adjustable position in the active matrix.

Cropping is allowed in X and Y direction independently, ROI width and height must be a multiple of 4 pixels.

The benefits of cropping the image are:

- Lightening image-processing requirements with less data to process reducing sensor power consumption.
- Increasing frame rate by saving both on readout time and preprocessing time.

This increases the frame rate as shown in the table below:

**Table 12. Maximum frame rate with reduced image size**

| Resolution  | MIPI 4 lanes |     | MIPI 2 lanes |     |
|-------------|--------------|-----|--------------|-----|
|             | GS           | RS  | GS           | RS  |
| 320 x 240   | 610          | 370 | 590          | 360 |
| 640 x 480   | 360          | 200 | 360          | 200 |
| 1280 x 720  | 260          | 140 | 260          | 140 |
| 1920 x 1080 | 180          | 97  | 129          | 98  |

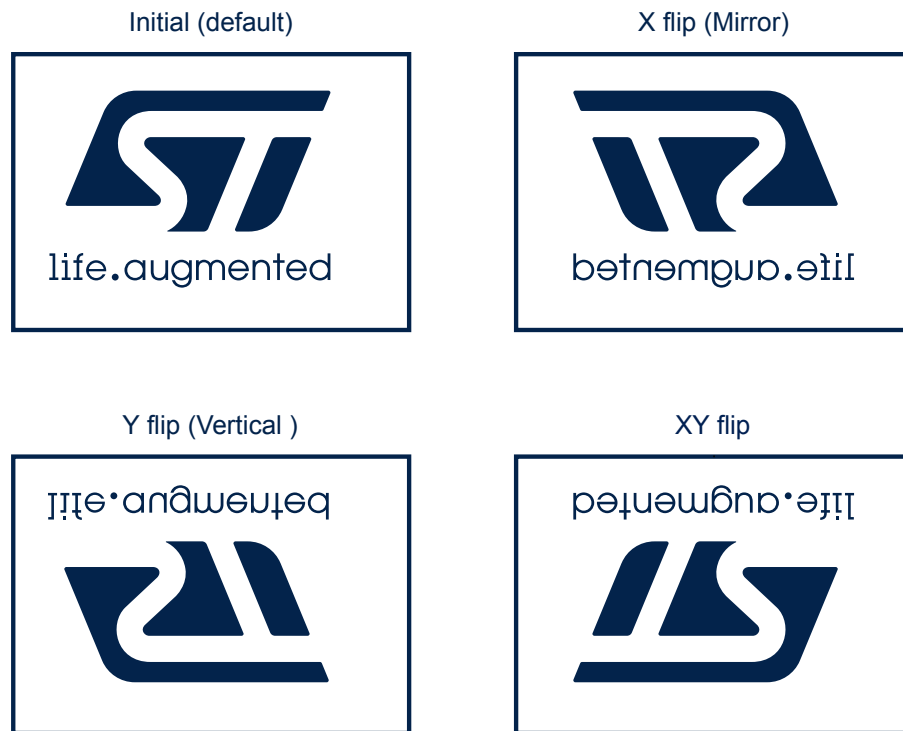
#### 4.3.6 Vertical and horizontal flip

Mirror (or X FLIP) reverses the output image horizontally.

Flip (or Y FLIP) reverses the output image vertically.

Combining both flip and mirror (XY FLIP) rotates the output image by 180°.

Figure 21. Illustration of mirror and flip modes



#### 4.3.7

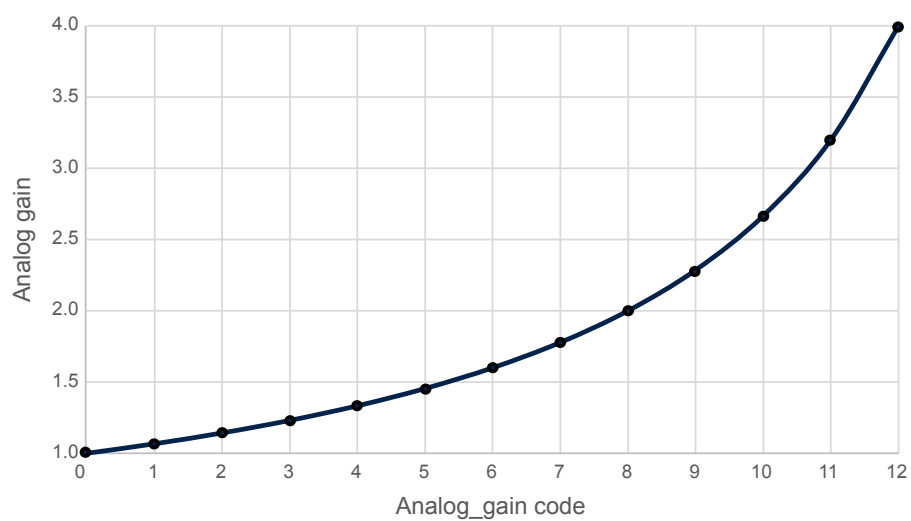
#### Analog and digital gains

The sensor enables setting analog and digital gains for the capture of clear high-contrast images even in low-light conditions.

Analog gain is common to all pixel types (R,G,B,NIR), while digital gain has a per color plane control.

Analog gain is applied prior to ADC conversion and avoids adding extra noise amplification. Its range is from 1.0 to 4.0 in 12 steps. If required, analog gain must be increased before digital gain.

Figure 22. Analog gain factors available



**Table 13. Available analog gain factors**

| Analog gain code | Analog gain value |
|------------------|-------------------|
| 0                | 1.00              |
| 1                | 1.07              |
| 2                | 1.14              |
| 3                | 1.23              |
| 4                | 1.33              |
| 5                | 1.45              |
| 6                | 1.60              |
| 7                | 1.78              |
| 8                | 2.00              |
| 9                | 2.29              |
| 10               | 2.67              |
| 11               | 3.20              |
| 12               | 4.00              |

Digital gain is applied inside ISP digital pipe after dark calibration stage. Its range is from 0 to 32 with a 1/256th step.

#### 4.3.8

#### PWL compression

Piecewise linear (PWL) compression involves applying a compression or decompression function to the incoming pixel stream. It maps the input dynamic range to the output range according to a programmable piecewise linear transformation function. The curve of the function must be monotonic and is described using 32 points as free (X, Y) doublets that give a high level of flexibility in curve shapes and accuracy.

PWL compression may be used to decrease the required bit width RAW resolution. This is achieved by applying a compression curve which reduces the overall dynamic in a nonlinear way.

Pixel resolution at the output of the video pipe is 10 bits (global shutter), 12 bits (rolling shutter SDR), and 18 bits (rolling shutter HDR), while formatting at the output interface is in the range RAW8 to RAW12.

The sensor has four default PWL curves:

- 10 bits to 8 bits (dedicated to global shutter)
- 12 bits to 8 bits (dedicated to rolling shutter SDR)
- 12 bits to 10 bits (dedicated to rolling shutter SDR)
- 18 bits to 12 bits (dedicated to rolling shutter HDR)
- 18 bits to 10 bits (dedicated to rolling shutter HDR)

PWL compression can be reprogrammed by the host to apply custom compression curve when sensor operation is rolling shutter HDR.

### 4.3.9 Output interface

The OIF embeds quad data lanes to communicate with the MIPI D-PHY interface. It supports up to 1.5 Gb/s of data per lane and can be scaled down to a dual-lane system. The OIF outputs active pixel data in RAW12, RAW10, or RAW8. The output interface supports virtual channels and data types.

MIPI lanes polarity and lanes ordering can be reconfigured before starting the image stream.

**Table 14. Video mode support**

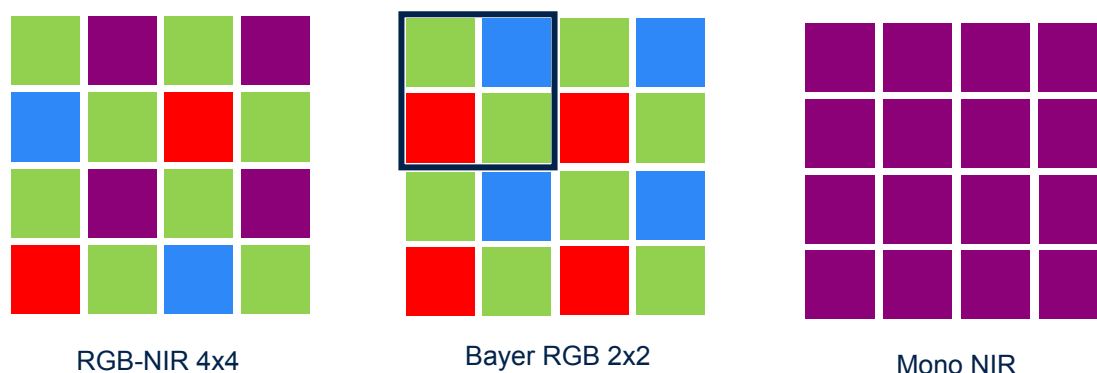
| Exposure        |                   |                    | MIPI supported format |              |             |
|-----------------|-------------------|--------------------|-----------------------|--------------|-------------|
| Mode            | Image output type | Remark             | RAW12                 | RAW10        | RAW8        |
| Global shutter  | RGB-NIR           | Kernel 4x4         | —                     | Direct       | PWL 10 => 8 |
|                 | RGB               | Depolluted NIR     | —                     | Direct       | PWL 10 => 8 |
|                 | NIR               | With smart upscale | —                     | Direct       | PWL 10 => 8 |
|                 | NIR subsampled    | x2, x4, or x32     | —                     | Direct       | PWL 10 => 8 |
| Rolling shutter | RGB-NIR           | SDR                | Direct                | PWL 12 => 10 | PWL 12 => 8 |
|                 | RGB               | SDR depolluted NIR | Direct                | PWL 12 => 10 | PWL 12 => 8 |
|                 | RGB-NIR           | HDR                | PWL 18 => 12          | PWL 18 => 10 | —           |
|                 | RGB               | HDR depolluted NIR | PWL 18 => 12          | PWL 18 => 10 | —           |

### 4.3.10 Device output pattern configuration capabilities

Thanks to its dedicated color filter and internal processing, the sensor can output three different patterns, depending on the selected configuration, as shown in [Figure 23. Output patterns](#).

In addition to standard single-pattern streaming, it is also possible to dynamically combine multiple patterns by chaining several configurations (see [Section 4.3.12: Contexts management](#)).

**Figure 23. Output patterns**



This Figure illustrates the readout order for the default configuration when both vertical flip and horizontal mirror are disabled.

For a complete description of the available output patterns and their behavior with different image orientations, refer to the product user manual.

### 4.3.11 Embedded status lines

The output interface (OIF) embeds the intelligent status line (ISL) generator to allow metadata to be sent inside every frame through the MIPI CSI ahead of the image content.

The CPU has access to a bank of status registers, refreshed at each frame, and providing detailed information on the current state of the sensor. Most of the content of this bank is also available in ISLs. The ISLs contain all information related to the current transmitted frame such as:

- Clock settings
- Image cropping and orientation parameters
- Analog and digital gains
- Integration time
- Frame counter index
- Thermal sensor values
- Dark calibration parameters

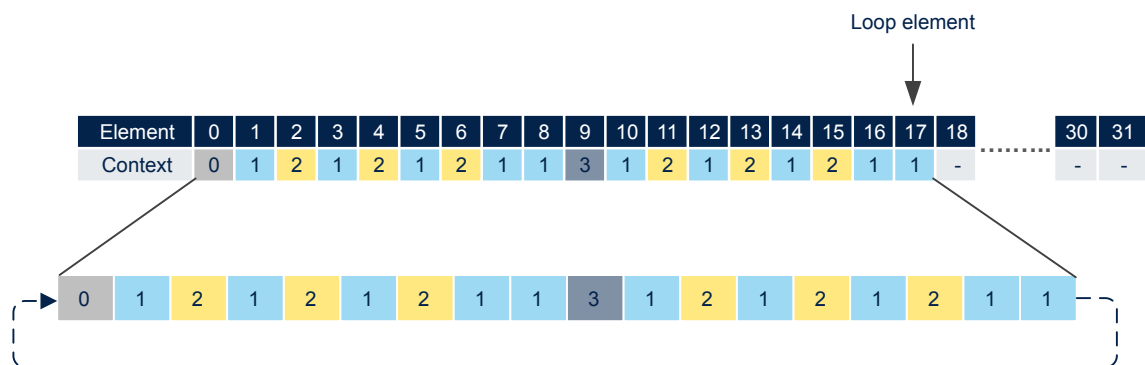
Transmission of ISL data packets can be disabled by configuring a static register during SW STANDBY state before streaming.

#### 4.3.12 Contexts management

The sensor allows the configuration of up to four different contexts (or frame setups).

The context sequence is configured with the context sequencing vector and the loop element register. The context sequencing vector contains 32 2-bit elements. Each element selects contexts: 0, 1, 2 or 3. The loop element register is a value from 0 to 31. Each element from 0 to *Loop element* is executed once and after execution, the next context to be executed is the one defined in *Element 0* (refer to [Figure 24. Context sequencing configuration](#)).

**Figure 24. Context sequencing configuration**



Some context parameters must be defined and stay frozen during streaming (static parameters), while other context parameters such as gain or integration time can be changed while streaming (dynamic parameters).

The sensor can be configured to generate a predefined number of frames before switching automatically back to SW\_STANDBY without any host supervision. This feature is possible in both leader and follower mode.

Context parameters that can be configured through the context management feature are listed in the following table:

**Table 15. Context parameters configurable for sequencing**

| Parameter                  | Description                                                                       |
|----------------------------|-----------------------------------------------------------------------------------|
| Sensor configuration       | Operating mode global or rolling (SDR or HDR) shutter, output pattern and bitwise |
| Virtual channel            | Selection of MIPI virtual channel ID                                              |
| Frame length               | To define the frame rate of the sensor                                            |
| Image ROI selection        | select ROI among four programmable ROIs                                           |
| Statistics ROI             | Define ROI geometry for statistics and histograms computation                     |
| GPIOs control              | Selectively enable or disable GPIOs features in the context                       |
| Defective pixel correction | Enable/disable pixel defect correction and control correction strength            |
| Noise reduction            | Enable/disable noise reduction and control reduction strength                     |
| DARK pedestal              | Enable/disable DARK calibration and set pedestal value                            |
| Analog gain                | Gain applied before ADC readout to adjust brightness                              |
| Digital gain               | Gain applied after ADC readout to adjust brightness                               |
| Integration time           | Adjust the exposure times applied to each frame                                   |

#### 4.3.13 Output format and structure of frames

The MIPI frame is made of a succession of long packets.

Each packet is sized to contain the payload of one line regardless of the image pixel format.

When enabled, top status line (TOP ISL) is transmitted after the *Start of Frame* short packet. This packet contains the first 512 bytes of the User Interface (UI) status registers, it describes the characteristics of the current image and is refreshed every frame.

TOP ISL packet is padded to have a total length fitting the size of a line packet. If a line packet is below 512 bytes, a second TOP ISL packet is generated.

When enabled, bottom status lines (BOT ISL) are transmitted before the *End of Frame* short packet, and contain statistics and histograms of the current frame.

The first packet has an initial padding of 256 bytes. The total number of BOT ISL lines differs according to the number of histograms to output.

BOT ISL packets are padded to have a total length fitting the size of a line packet.

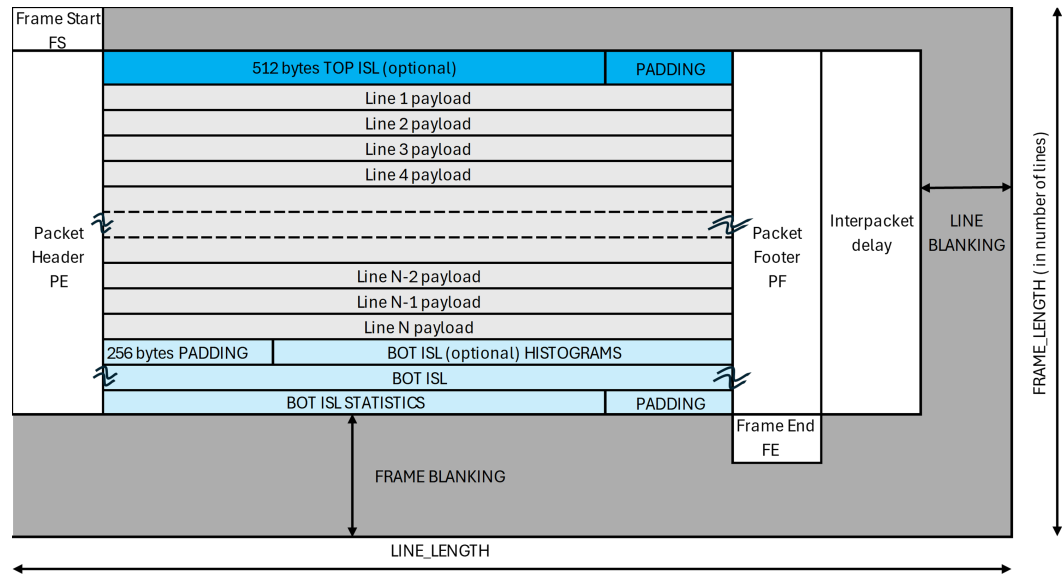
A partial frame buffer allows a MIPI line packet transmission time to be longer than the line period, ie no more line blanking.

Conversely, MIPI line packets may not be transmitted continuously lines after lines, the sensor can insert line pauses in the MIPI transmission.

The sensor is applying a programmable minimum interpacket delay between line packets.

Images for each of the four contexts have their own configurable virtual channels and datatypes. Top and bottom status lines also have a common configurable datatype.

**Figure 25. MIPI frame format**



## 5 Product interfaces

### 5.1 Inter-integrated circuit

The image sensor is configured and controlled via an I<sup>2</sup>C interface operating either in fast mode (400 kHz) or in fast mode plus (1 MHz) at 1.8 V. After the sensor boot sequence, the default I<sup>2</sup>C configuration is fast mode plus with a sink capability set to 20 mA. Drive capability can be decreased to 4 mA (fast mode) by setting a dedicated register once the system has booted.

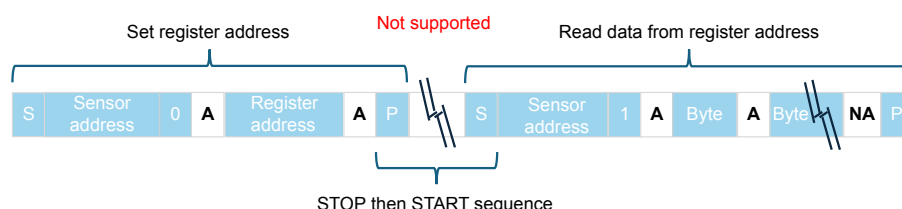
Device addressing uses a camera control interface (CCI) protocol with 2-byte subaddresses.

The default sensor address is 0x20 (including R/W bits) and can be overridden permanently (by storing a nonnull value in a dedicated OTP register), or temporarily (by storing a nonnull value in a dedicated user interface register).

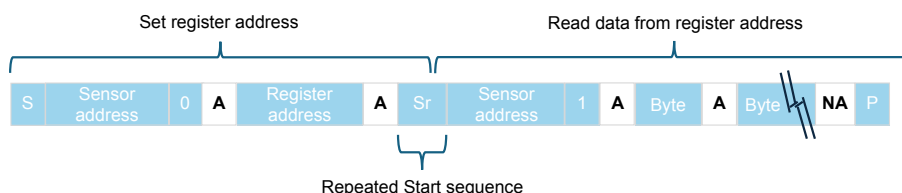
#### 5.1.1 Known limitation and workaround

The sensor's I<sup>2</sup>C interface does not support single or sequential reads that start from the current location. Consequently, use a repeated start condition to read the registers.

**Figure 26. Incompatible I<sup>2</sup>C read sequence**



**Figure 27. Reliable I<sup>2</sup>C read sequence**



### 5.2 MIPI CSI-2 interface

The sensor is ready to connect via a quad-lane MIPI CSI-2 serial interface. It is also able to operate on a reduced dual-lane interface. The MIPI CSI-2 serial interface supports up to 1.5 Gbps per lane. It is the industry standard for low electromagnetic interference (EMI) and excellent electromagnetic compatibility (EMC) high-speed interfacing. Resolution is scalable between RAW8, RAW10, and RAW12.

The quad per lane interface does not support an ultralow power state. The clock and data lanes remain in LP-11 (TX-stop state) when the video stream stops.

The interface supports data rates from 300 Mbps up to 1.5 Gbps per lane. However, the minimum data rate for the rolling shutter HDR configurations is 750 Mbps per lane.

## 6 Thermal characteristics

### 6.1 Thermal absolute maximum ratings

**Caution:** Stresses above those listed in the [Table 16. Absolute maximum rating conditions](#), may cause permanent damage to the device. These are absolute maximum ratings only. Functional operation of the device is not implied at these or any other conditions beyond those specified in the operating sections of this document. Prolonged exposure to absolute maximum rating conditions may affect device reliability.

**Table 16. Absolute maximum rating conditions**

| Parameter                   | Min. | Max. | Unit |
|-----------------------------|------|------|------|
| Storage temperature (T_STG) | -40  | +125 | °C   |

### 6.2 Junction operating temperature conditions

The junction operating temperature is the temperature range within which the device can be powered and operated without damage. This specification applies to both the OBGA package version and the wafer reconstruction version.

The device includes internal thermal sensors that can be read during operation to continuously monitor the silicon temperature.

**Table 17. Junction operating temperature**

| Symbol | Parameter                                   | Min. | Typ. | Max. | Unit |
|--------|---------------------------------------------|------|------|------|------|
| T_JF   | Junction temperature (functional operation) | -30  | —    | 85   | °C   |

### 6.3 Package thermal resistance

**Table 18. OBGA package thermal resistance**

| Parameter                              | Minimum | Typical | Maximum | Unit |
|----------------------------------------|---------|---------|---------|------|
| R <sub>th JA</sub><br>(JEDEC 2s2p PCB) | —       | 30      | —       | °C/W |

## 7 Electrical characteristics

Unless otherwise specified:

- Typical values are quoted for nominal voltage, process, and temperature
- Maximum values are quoted for worst case conditions (process, voltage, and functional temperature)

### 7.1 Absolute maximum ratings

**Caution:** Stresses above those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 19. Absolute maximum ratings**

| Symbol                              | Parameter                 | Maximum | Unit |
|-------------------------------------|---------------------------|---------|------|
| VANA                                | Analog power supply       | 3.99    | V    |
| VCORE                               | Digital core power supply | 1.89    | V    |
| VDDIO                               | Digital I/O power supply  | 2.85    | V    |
| VESD, electrostatic discharge model | Human body model (HBM)    | ±2      | kV   |
|                                     | Charge device model (CDM) | ±500    | V    |

### 7.2 Operating conditions

**Table 20. Operating conditions**

| Symbol | Parameter                 | Min. | Typ. | Max. | Unit |
|--------|---------------------------|------|------|------|------|
| VANA   | Analog power supply       | 2.70 | 2.80 | 2.90 | V    |
| VCORE  | Digital core power supply | 1.05 | 1.15 | 1.26 |      |
| VDDIO  | Digital I/O power supply  | 1.70 | 1.80 | 1.90 |      |

### 7.3 Electrical parameters

#### 7.3.1 Power supplies POR threshold

The device has power-on-reset (POR) detection cells with hysteresis on all power supplies. The POR is released after a typical delay of 20 µs on the rising edge. Bursts with a duration of less than 2 µs (typical) are ignored.

**Table 21. POR threshold**

| Supply | Maximum threshold on rising edge | Minimum threshold on falling edge | Unit |
|--------|----------------------------------|-----------------------------------|------|
| VANA   | 1.33                             | 0.84                              | V    |
| VCORE  | 0.74                             | 0.49                              |      |
| VDDIO  | 1.32                             | 0.83                              |      |

## 7.3.2 Power consumption

### 7.3.2.1 Typical streaming power consumption versus image size

Sensor common settings:

- AGAIN = 2
- Exposure time = 10 ms
- Tj = 60°C
- MIPI 1.5 Gbps
- RAW10
- EXTCLK = 25 MHz

Use case Rolling Shutter, Bayer RGB output, 50 fps, MIPI 4 lanes:

**Table 22. Typical power consumption in rolling shutter mode**

| Resolution | VANA (mA) | VCORE (mA) | VDDIO (mA) | Total power (mW) |
|------------|-----------|------------|------------|------------------|
| 2560x1984  | 51.6      | 208        | 0.52       | 376              |
| 1920x1080  | 38        | 139        | 0.52       | 263              |
| 1280x720   | 32.6      | 113        | 0.52       | 220              |
| 640x480    | 28.7      | 97         | 0.52       | 191              |

Use case Global Shutter, NIR output, 30 fps, MIPI 2 lanes:

**Table 23. Typical power consumption in global shutter mode**

| Resolution | VANA (mA) | VCORE (mA) | VDDIO (mA) | Total power (mW) |
|------------|-----------|------------|------------|------------------|
| 2560x1984  | 33        | 158        | 0.52       | 271              |
| 1920x1080  | 26        | 124        | 0.52       | 214              |
| 1280x720   | 21.3      | 111        | 0.52       | 186              |
| 640x480    | 19.5      | 103        | 0.52       | 173              |

### 7.3.2.2 Typical streaming power consumption versus frame rate

Sensor common settings:

- AGAIN = 2
- exposure time = 10ms
- Tj = 60°C
- MIPI 1.5Gbps , 4 lanes
- RAW10
- Image 2560x1984
- EXTCLK = 25 MHz

Use case Rolling Shutter, Bayer RGB output:

**Table 24. Typical power consumption in rolling shutter mode**

| Frame rate (fps) | VANA (mA) | VCORE (mA) | VDDIO (mA) | Total power (mW) |
|------------------|-----------|------------|------------|------------------|
| 20               | 32.2      | 126        | 0.52       | 233              |
| 30               | 39        | 153        | 0.52       | 281              |
| 40               | 45.5      | 180        | 0.52       | 330              |
| 50               | 51.6      | 208        | 0.52       | 376              |

Use case Global Shutter, NIR output:

**Table 25. Typical power consumption in global shutter mode**

| Frame rate (fps)      | VANA (mA) | VCORE (mA) | VDDIO (mA) | Total power (mW) |
|-----------------------|-----------|------------|------------|------------------|
| 20                    | 26        | 135        | 0.52       | 225              |
| 30                    | 29        | 153        | 0.52       | 254              |
| 40                    | 32.8      | 175        | 0.52       | 290              |
| 50                    | 36        | 191        | 0.52       | 315              |
| 60                    | 39.5      | 219        | 0.52       | 354              |
| 100 (exposure 9.5 ms) | 53        | 297        | 0.52       | 475              |

### 7.3.2.3 Typical and maximum power consumption

Maximum values are quoted for worst case conditions (process, voltage, and functional temperature) and evaluated on a limited number of devices.

Typical values are quoted at nominal voltage and  $T_j = 60^\circ\text{C}$ .

Sensor streaming settings:

- AGAIN = 1
- Exposure time = 3 ms
- MIPI 1.3 Gbps, 4 lanes
- Global shutter NIR Smart Upscale RAW10
- Image 2560x1984
- Frame rate 60 fps
- Test pattern generator pseudo random PN28
- EXTCLK = 25 MHz
- Defect pixel correction ON
- Gaussian filter ON

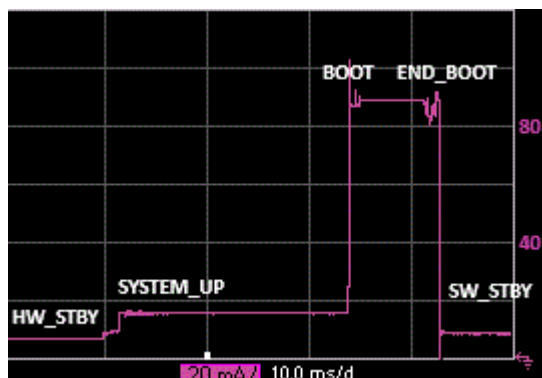
**Table 26. Typical and maximum power consumption**

|                            | VANA |      | VCORE |       | VDDIO |      | Unit |
|----------------------------|------|------|-------|-------|-------|------|------|
|                            | Typ. | Max. | Typ.  | Max.  | Typ.  | Max. |      |
| HW_STANDBY                 | 0.08 | 0.1  | 9.0   | 45.0  | 0.013 | 0.02 | mA   |
| SW_STANDBY after BOOT      | 0.7  | 1.0  | 11.0  | 55.0  | 0.013 | 0.02 |      |
| SW_STANDBY after STREAMING | 4.5  | 5.0  | 13.5  | 60.0  | 0.013 | 0.02 |      |
| STREAMING                  | 38.5 | 40.0 | 222.0 | 290.0 | 0.52  | 0.6  |      |

### 7.3.3 Current profile

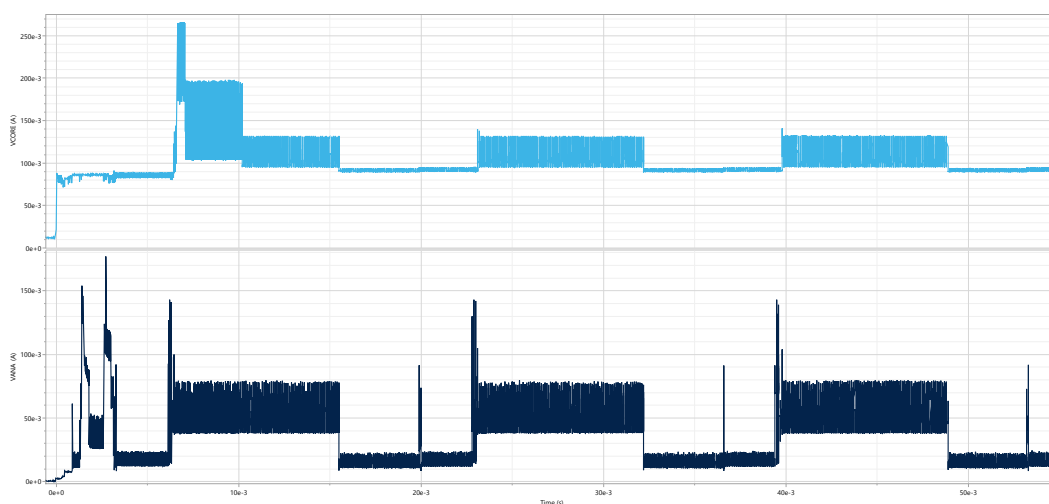
#### BOOT sequence

The data of the figure below has been captured on one device at nominal temperature and voltage.

**Figure 28. V<sub>CORE</sub> transient current during BOOT**


### START\_STREAM sequence

Refer to [Section 7.3.2: Power consumption](#) for the streaming conditions.

**Figure 29. First frames typical current profile (A) over time (s)**


## 7.3.4 EXTCLK input

**Table 27. EXTCLK input**

$V_{EXTCLKL}$ ,  $V_{EXTCLKH}$ ,  $f_{EXTCLK}$ ,  $C_{toCjitter}$ , and duty cycle are evaluated on a limited number of devices.

| Symbol          | Parameter                               | Min.                  | Max.                  | Unit    |
|-----------------|-----------------------------------------|-----------------------|-----------------------|---------|
| $V_{EXTCLKL}$   | DC-coupled square wave low-level input  | -0.5                  | $0.3 \times V_{DDIO}$ | V       |
| $V_{EXTCLKH}$   | DC-coupled square wave high-level input | $0.7 \times V_{DDIO}$ | $V_{DDIO} + 0.5$      |         |
| $f_{EXTCLK}$    | Clock input frequency                   | 12                    | 50                    | MHz     |
| $C_{toCjitter}$ | Clock maximum cycle to cycle jitter     | —                     | 200                   | ps      |
| Duty cycle      | Clock duty cycle                        | 40                    | 60                    | %       |
| $I_{EXTCLK}$    | Input leakage current                   | —                     | 10                    | $\mu A$ |

### 7.3.5 Digital inputs

**Table 28. Digital inputs**

$V_{IL}$  and  $V_{IH}$  are evaluated on a limited number of devices.

| Symbol     | Parameter                            | Min.                  | Max.                  | Unit |
|------------|--------------------------------------|-----------------------|-----------------------|------|
| $V_{IL}$   | Low-level input voltage              | -0.5                  | $0.3 \times V_{DDIO}$ | V    |
| $V_{IH}$   | High-level input voltage             | $0.7 \times V_{DDIO}$ | $V_{DDIO} + 0.5$      |      |
| $I_{Leak}$ | Input leakage current <sup>(1)</sup> | —                     | 10                    | μA   |

1. For  $0 \leq V_I \leq V_{DDIO}$

**Table 29. GPIO pull down resistance value**

| Symbol | Parameter            | Min. | Typical | Unit |
|--------|----------------------|------|---------|------|
| Rpd    | Pull down resistance | 28   | 50      | KΩ   |

### 7.3.6 Digital outputs

**Table 30. Digital outputs**

| Symbol    | Parameter                 | Conditions               | Min.             | Max. | Unit |
|-----------|---------------------------|--------------------------|------------------|------|------|
| $V_{OL}$  | Low-level output voltage  | $I_{OL} = -4 \text{ mA}$ | —                | 0.4  | V    |
| $V_{OH}$  | High-level output voltage | $I_{OH} = 4 \text{ mA}$  | $V_{DDIO} - 0.4$ | —    |      |
| $I_{max}$ | Maximum current           |                          | —                | 4    | mA   |

### 7.3.7 I<sup>2</sup>C interface - SDA, SCL

I<sup>2</sup>C timing and voltage conform to the standard described in UM10204: I<sup>2</sup>C-bus specification and user manual, Rev. 6. Refer to [Appendix A: I<sup>2</sup>C interface - SDA, SCL - Norm extract](#) for further information.

Conformance to specification is evaluated on a limited number of devices.

Refer to [Section 5.1: Inter-integrated circuit](#) for limitation description.

## 7.3.8

**CSI-2 interface**

The CSI-2 interface conforms to the MIPI Alliance specification for D-PHY version 1.1. Refer to the standard for complete details of the specification. Refer to [Appendix B: CSI-2 interface - Specification extract](#) for further information.

The interface has been evaluated by characterization for a typical process, at ambient temperature, and with full VCORE voltage coverage (minimum/typical/maximum). The sensor has been programmed as follows:

- Resolution = Full
- Shutter mode = Rolling
- Frame rate = 30 fps
- External clock = 25 MHz
- CSI-2 data rate = 1.3 Gbps/lane
- Pattern generator = Enabled

High-speed mode - AC is evaluated on a limited number of devices.

## 8 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 8.1 OBGA package information

#### 8.1.1 OBGA package dimensions

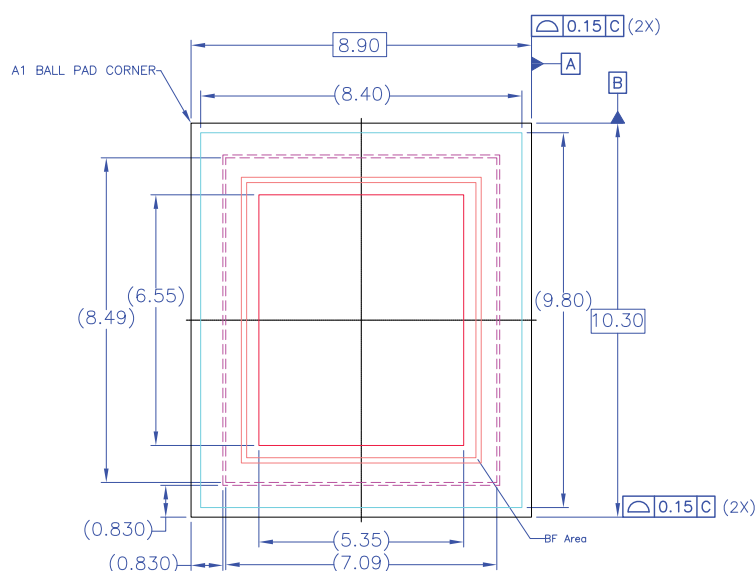
**Table 31. OBGA package mechanical data**

| Parameter | Minimum | Typical | Maximum | Unit |
|-----------|---------|---------|---------|------|
| Width     | 8.75    | 8.90    | 9.05    | mm   |
| Height    | 10.15   | 10.30   | 10.45   | mm   |
| Thickness | 1.90    | 2.05    | 2.20    | mm   |

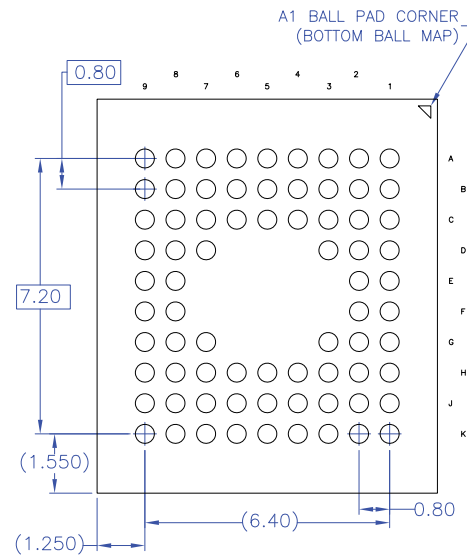
- The bond line thickness (substrate to silicon interface) is 20  $\mu\text{m}$ .
- The silicon die thickness is 200  $\mu\text{m}$ .
- The optical center is aligned with the package center.
- The focusing plane is designed to be on the top surface of the silicon, with a height tolerance of  $\pm 30$   $\mu\text{m}$ .
- Focusing plane tilt is maximum 25  $\mu\text{m}$ .
- The ball pitch is 800  $\mu\text{m}$  in both directions
- The ball diameter is 520  $\mu\text{m}$

#### 8.1.2 Mechanical drawings

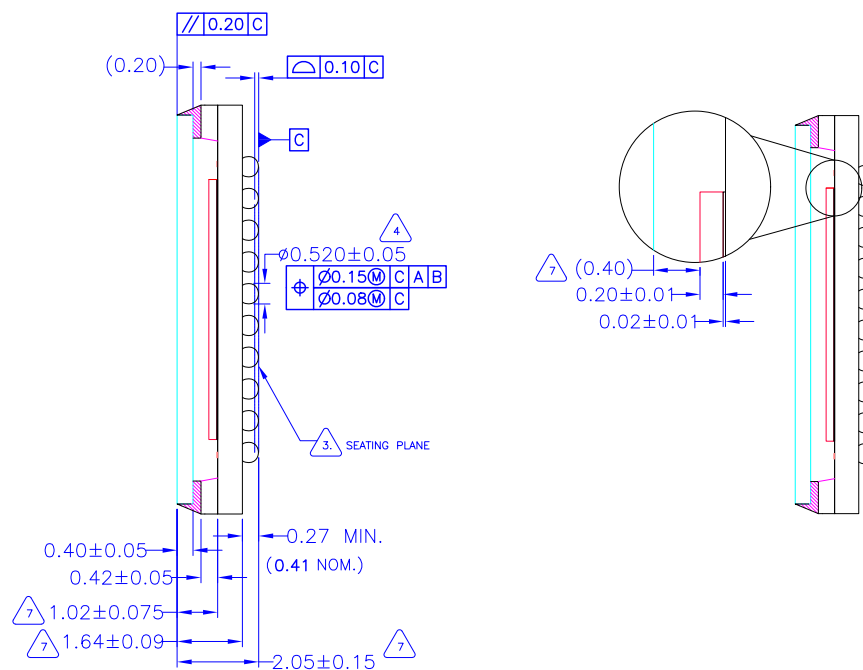
**Figure 30. Top view**



**Figure 31. Bottom view**



**Figure 32. Side view**



**Note:** These drawings are subject to change without notice.

**Note:** All linear dimensions are in millimeters.

### 8.1.3 Glass properties

**Note:** OBGA-packaged devices delivered in tape and reel are supplied without a protective liner on the glass window. Therefore, ESD-safe handling, cleanroom-compatible tools, and any appropriate cleanliness controls are required and under the customer's responsibility to prevent contamination, scratching, or other damage to the optical surface.

**Table 32. Glass reflectance and transmittance**

| Items                       |                   | Requirements |                   |                    |                                  |
|-----------------------------|-------------------|--------------|-------------------|--------------------|----------------------------------|
| Glass optical specification |                   | Band nm      | 0° <sup>(1)</sup> | 30° <sup>(1)</sup> | 5° <sup>(1)</sup>                |
|                             | Transmittance (T) | 900-1000     | Tminimum > 97.5%  | Tminimum > 97%     |                                  |
|                             | Reflectivity (R)  | 900-1000     | —                 |                    | Raverage < 1.5%<br>Rmaximum < 2% |

1. Incidence angle

## 8.2 Die mechanical description

### 8.2.1 Die dimensions

In the table below, the die dimensions are after sawing.

**Table 33. Die dimensions**

| Parameter            | Minimum | Typical | Maximum | Unit |
|----------------------|---------|---------|---------|------|
| X die (after sawing) | 6536    | 6546    | 6556    | μm   |
| Y die (after sawing) | 5339    | 5349    | 5359    | μm   |
| Die thickness        | 190     | 200     | 210     | μm   |

### 8.2.2 Optical center

The reference of the optical center is the die center.

**Table 34. Optical center**

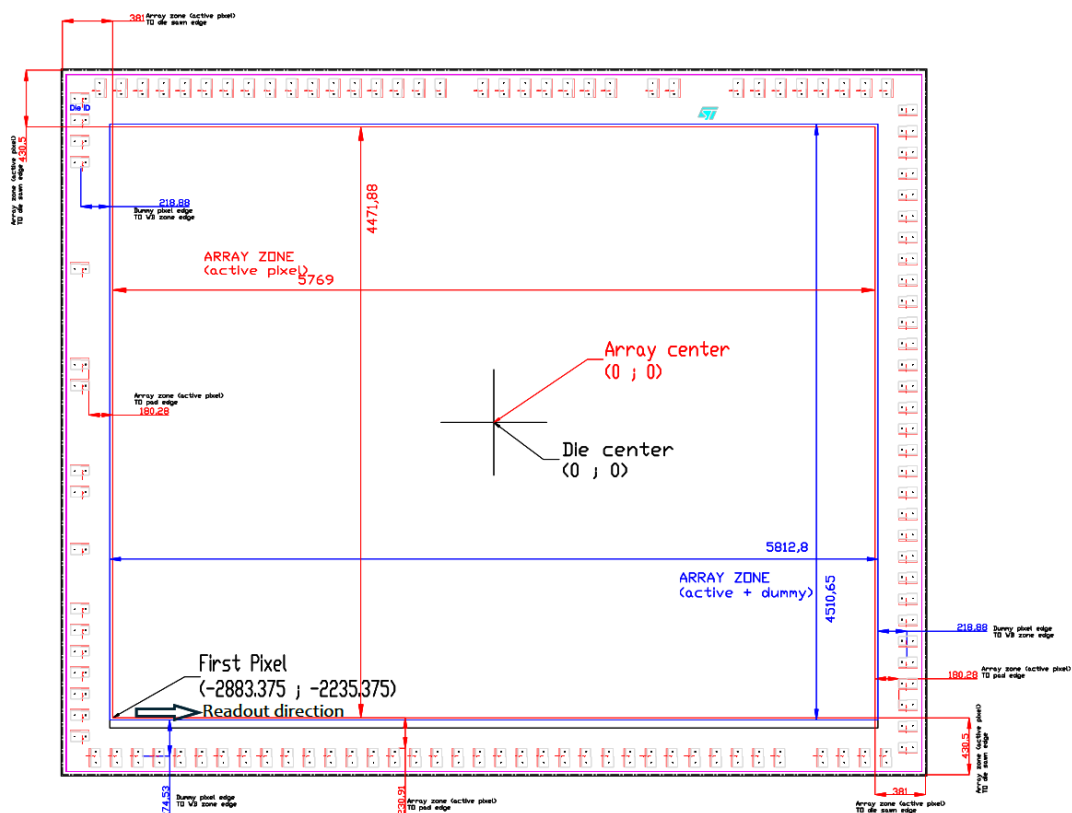
| Parameter      | X position (μm) | Y positon (μm) |
|----------------|-----------------|----------------|
| Optical center | 0               | 0              |

### 8.2.3 Die layout

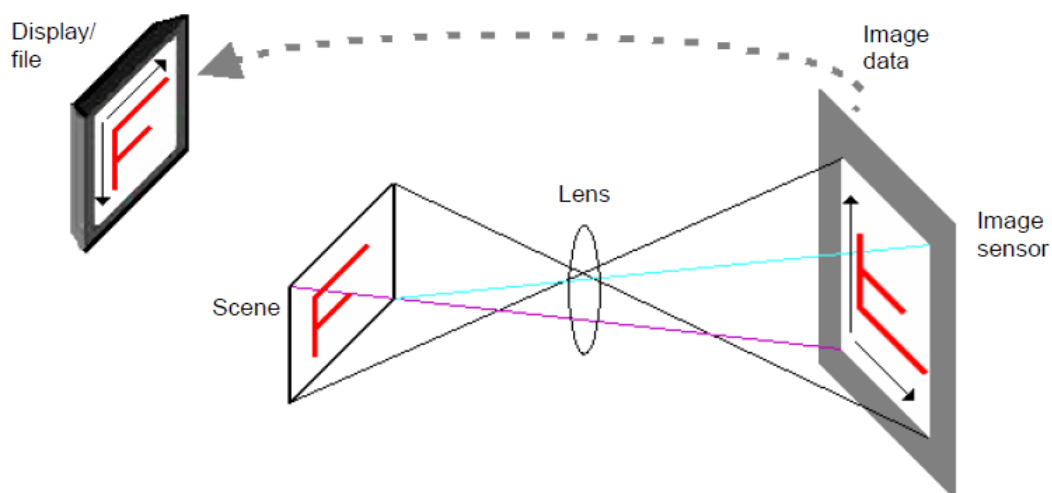
See [Table 35. Pad assignment](#) for signal descriptions.

The optical area in [Figure 33](#) corresponds to the pixel matrix. This pixel matrix is surrounded by a crown of two pixels (two rows on the top, two rows on the bottom, two columns on the left, and two columns on the right). The pixels on the edge are used by the digital processing blocks for optimizing image quality. They are not transmitted by the sensor, although they are considered for designing the optical stack of the camera module.

The extended zone in [Figure 33](#) corresponds to all pixels of the matrix, plus dummy and dark pixels. Dummy and dark pixels are exclusively processed internally. Do not consider them for designing the optical stack.

**Figure 33. Die pad positions (see-through view)**


The actual image of the scene projected through the lens onto the pixel array means that it is necessary to read the array starting at the bottom-left corner. This is so that the final displayed image is correct (refer to the arrow "Read OUT" in Figure 33).

**Figure 34. Image orientation**


As this document is related to the die, the image orientation (depicted by an "F" symbol) shows the image as it is really being captured by the sensor. The pixel readout is fully programmable (mirror and flip) but the default readout fashion is from left to right and bottom to top as shown in Figure 34. Image orientation.

## 8.2.4 Pad assignment

The following assignment is listed from top left of the die in a clockwise direction.

**Table 35. Pad assignment**

| Pad number | Side  | Pin name  | Bonding point, X co-ordinate | Bonding point, Y co-ordinate |
|------------|-------|-----------|------------------------------|------------------------------|
| 1          | Top   | VANA      | -2983.99                     | 2569.61                      |
| 2          | Top   | VANA      | -2822.97                     | 2569.61                      |
| 3          | Top   | VANA      | -2661.94                     | 2569.61                      |
| 4          | Top   | AGND      | -2500.91                     | 2569.61                      |
| 5          | Top   | AGND      | -2339.88                     | 2569.61                      |
| 6          | Top   | CPPOS_OUT | -2178.86                     | 2569.61                      |
| 7          | Top   | CPPOS_IN  | -2017.83                     | 2569.61                      |
| 8          | Top   | AGND      | -1856.8                      | 2569.61                      |
| 9          | Top   | VCORE     | -1695.77                     | 2569.61                      |
| 10         | Top   | DGND      | -1534.74                     | 2569.61                      |
| 11         | Top   | VCORE     | -1373.72                     | 2569.61                      |
| 12         | Top   | DGND      | -1212.69                     | 2569.61                      |
| 13         | Top   | VANA      | -1051.66                     | 2569.61                      |
| 14         | Top   | VANA      | -890.63                      | 2569.61                      |
| 15         | Top   | AGND      | -729.6                       | 2569.61                      |
| 16         | Top   | DGND      | -568.58                      | 2569.61                      |
| 17         | Top   | VRT       | -407.55                      | 2569.61                      |
| 18         | Top   | AGND      | -85.49                       | 2569.61                      |
| 19         | Top   | VCORE     | 75.54                        | 2569.61                      |
| 20         | Top   | VCORE     | 236.57                       | 2569.61                      |
| 21         | Top   | DGND      | 397.59                       | 2569.61                      |
| 22         | Top   | AGND      | 558.62                       | 2569.61                      |
| 23         | Top   | VANA      | 719.65                       | 2569.61                      |
| 24         | Top   | VANA      | 880.68                       | 2569.61                      |
| 25         | Top   | DGND      | 1202.730                     | 2569.61                      |
| 26         | Top   | AGND      | 1363.76                      | 2569.61                      |
| 27         | Top   | VANA      | 1846.85                      | 2569.61                      |
| 28         | Top   | DGND      | 2007.87                      | 2569.61                      |
| 29         | Top   | VCORE     | 2168.9                       | 2569.61                      |
| 30         | Top   | VCORE     | 2329.93                      | 2569.61                      |
| 31         | Top   | AGND      | 2490.96                      | 2569.61                      |
| 32         | Top   | VANA      | 2651.99                      | 2569.61                      |
| 33         | Top   | AGND      | 2813.01                      | 2569.61                      |
| 34         | Top   | VCORE     | 2974.04                      | 2569.61                      |
| 35         | Right | DGND      | 3168.11                      | 2374.78                      |
| 36         | Right | VANA      | 3168.11                      | 2213.76                      |
| 37         | Right | AGND      | 3168.11                      | 2052.73                      |

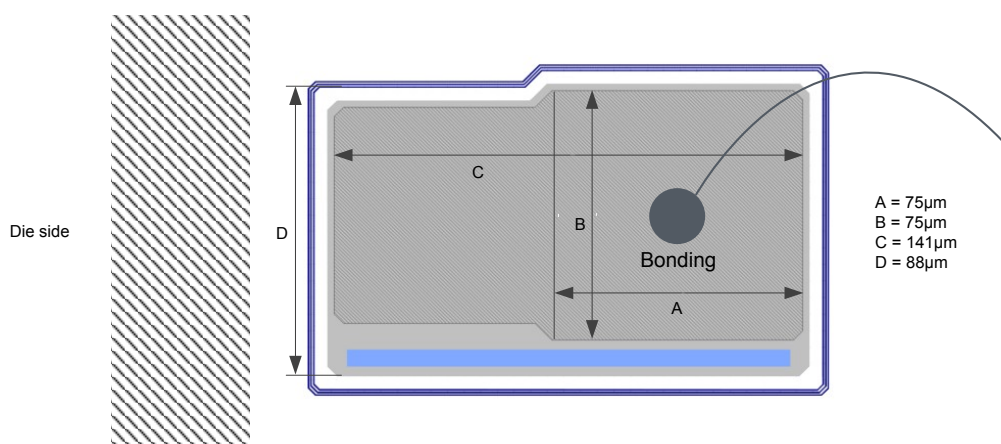
| Pad number | Side   | Pin name                   | Bonding point,<br>X co-ordinate | Bonding point,<br>Y co-ordinate |
|------------|--------|----------------------------|---------------------------------|---------------------------------|
| 38         | Right  | VDDIO                      | 3168.11                         | 1891.7                          |
| 39         | Right  | DGND                       | 3168.11                         | 1730.67                         |
| 40         | Right  | VCORE                      | 3168.11                         | 1569.64                         |
| 41         | Right  | NC                         | 3168.11                         | 1408.62                         |
| 42         | Right  | NC                         | 3168.11                         | 1247.59                         |
| 43         | Right  | DGND                       | 3168.11                         | 1086.56                         |
| 44         | Right  | VDDIO                      | 3168.11                         | 925.53                          |
| 45         | Right  | DGND                       | 3168.11                         | 764.51                          |
| 46         | Right  | EXTCLK                     | 3168.11                         | 603.48                          |
| 47         | Right  | VCORE                      | 3168.11                         | 442.45                          |
| 48         | Right  | DGND                       | 3168.11                         | 281.42                          |
| 49         | Right  | VANA                       | 3168.11                         | 120.39                          |
| 50         | Right  | VANA                       | 3168.11                         | -40.63                          |
| 51         | Right  | AGND                       | 3168.11                         | -201.66                         |
| 52         | Right  | LDO2V4                     | 3168.11                         | -362.69                         |
| 53         | Right  | DGND                       | 3168.11                         | -523.72                         |
| 54         | Right  | VCORE                      | 3168.11                         | -684.75                         |
| 55         | Right  | DGND                       | 3168.11                         | -845.77                         |
| 56         | Right  | DATA4P                     | 3168.11                         | -1006.8                         |
| 57         | Right  | DATA4N                     | 3168.11                         | -1167.83                        |
| 58         | Right  | DATA1P                     | 3168.11                         | -1328.86                        |
| 59         | Right  | DATA1N                     | 3168.11                         | -1489.89                        |
| 60         | Right  | CLKP                       | 3168.11                         | -1650.91                        |
| 61         | Right  | CLKN                       | 3168.11                         | -1811.94                        |
| 62         | Right  | DATA2P                     | 3168.11                         | -1972.97                        |
| 63         | Right  | DATA2N                     | 3168.11                         | -2134                           |
| 64         | Right  | DATA3P                     | 3168.11                         | -2295.03                        |
| 65         | Right  | DATA3N                     | 3168.11                         | -2456.06                        |
| 66         | Bottom | NC                         | 2974.04                         | -2569.61                        |
| 67         | Bottom | DGND                       | 2813.01                         | -2569.61                        |
| 68         | Bottom | VCORE                      | 2651.99                         | -2569.61                        |
| 69         | Bottom | AGND                       | 2490.96                         | -2569.61                        |
| 70         | Bottom | AGND                       | 2168.9                          | -2569.61                        |
| 71         | Bottom | VCORE                      | 2007.87                         | -2569.61                        |
| 72         | Bottom | DGND                       | 1846.85                         | -2569.61                        |
| 73         | Bottom | PORTEST (must be grounded) | 1685.82                         | -2569.61                        |
| 74         | Bottom | NC                         | 1524.79                         | -2569.61                        |
| 75         | Bottom | VDDIO                      | 1353.56                         | -2569.61                        |
| 76         | Bottom | NC                         | 1192.53                         | -2569.61                        |
| 77         | Bottom | DGND                       | 1031.5                          | -2569.61                        |

| Pad number | Side   | Pin name   | Bonding point,<br>X co-ordinate | Bonding point,<br>Y co-ordinate |
|------------|--------|------------|---------------------------------|---------------------------------|
| 78         | Bottom | VCORE      | 870.47                          | -2569.61                        |
| 79         | Bottom | DGND       | 699.24                          | -2569.61                        |
| 80         | Bottom | RESETN     | 538.21                          | -2569.61                        |
| 81         | Bottom | GPIO0      | 377.18                          | -2569.61                        |
| 82         | Bottom | GPIO1      | 216.15                          | -2569.61                        |
| 83         | Bottom | VCORE      | 55.13                           | -2569.61                        |
| 84         | Bottom | GPIO2      | -105.9                          | -2569.61                        |
| 85         | Bottom | GPIO3      | -266.93                         | -2569.61                        |
| 86         | Bottom | DGND       | -427.96                         | -2569.61                        |
| 87         | Bottom | VDDIO      | -588.99                         | -2569.61                        |
| 88         | Bottom | DGND       | -750.02                         | -2569.61                        |
| 89         | Bottom | SDA        | -911.04                         | -2569.61                        |
| 90         | Bottom | SCL        | -1072.07                        | -2569.61                        |
| 91         | Bottom | CLK_RANGE0 | -1233.1                         | -2569.61                        |
| 92         | Bottom | CLK_RANGE1 | -1394.13                        | -2569.61                        |
| 93         | Bottom | VCORE      | -1555.15                        | -2569.61                        |
| 94         | Bottom | NC         | -1716.18                        | -2569.61                        |
| 95         | Bottom | NC         | -1877.21                        | -2569.61                        |
| 96         | Bottom | AGND       | -2048.45                        | -2569.61                        |
| 97         | Bottom | NC         | -2209.47                        | -2569.61                        |
| 98         | Bottom | NC         | -2370.5                         | -2569.61                        |
| 99         | Bottom | VANA       | -2531.53                        | -2569.61                        |
| 100        | Bottom | DGND       | -2692.56                        | -2569.61                        |
| 101        | Bottom | VCORE      | -2853.59                        | -2569.61                        |
| 102        | Bottom | AGND       | -3014.61                        | -2569.61                        |
| 103        | Left   | CPNEG_OUT  | -3168.11                        | -2375.54                        |
| 104        | Left   | CPNEG_IN   | -3168.11                        | -2214.51                        |
| 105        | Left   | AGND       | -3168.11                        | -2053.49                        |
| 106        | Left   | AGND       | -3168.11                        | -1892.46                        |
| 107        | Left   | VANA       | -3168.11                        | -1731.43                        |
| 108        | Left   | VANA       | -3168.11                        | -1570.4                         |
| 109        | Left   | AGND       | -3168.11                        | -1409.370                       |
| 110        | Left   | NC         | -3168.11                        | -959.430                        |
| 111        | Left   | DGND       | -3168.11                        | -523.72                         |
| 112        | Left   | VANA       | -3168.11                        | -362.69                         |
| 113        | Left   | AGND       | -3168.11                        | 281.42                          |
| 114        | Left   | VCORE      | -3168.11                        | 442.45                          |
| 115        | Left   | AGND       | -3168.11                        | 1167.08                         |
| 116        | Left   | VANA       | -3168.11                        | 1972.97                         |
| 117        | Left   | DGND       | -3168.11                        | 2134                            |

| Pad number | Side | Pin name | Bonding point, X co-ordinate | Bonding point, Y co-ordinate |
|------------|------|----------|------------------------------|------------------------------|
| 118        | Left | VCORE    | -3168.11                     | 2295.03                      |
| 119        | Left | AGND     | -3168.11                     | 2456.06                      |

### 8.2.5 Bonding pad information

**Figure 35. Bonding pad opening**



**Table 36. Pad opening size**

| Parameter        | X (µm) | Y (µm) |
|------------------|--------|--------|
| Pad opening size | 75     | 75     |

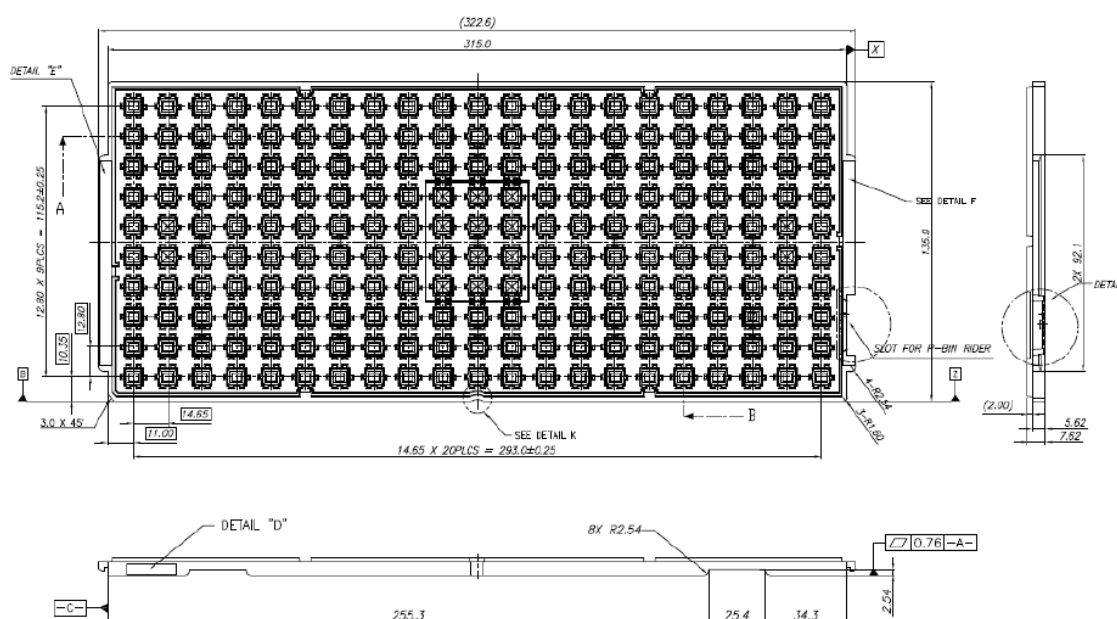
## 9 Packing and labeling information

## 9.1 Packing delivery modes

Devices are delivered either in tray or tape and reel format.

### 9.1.1 Tray information

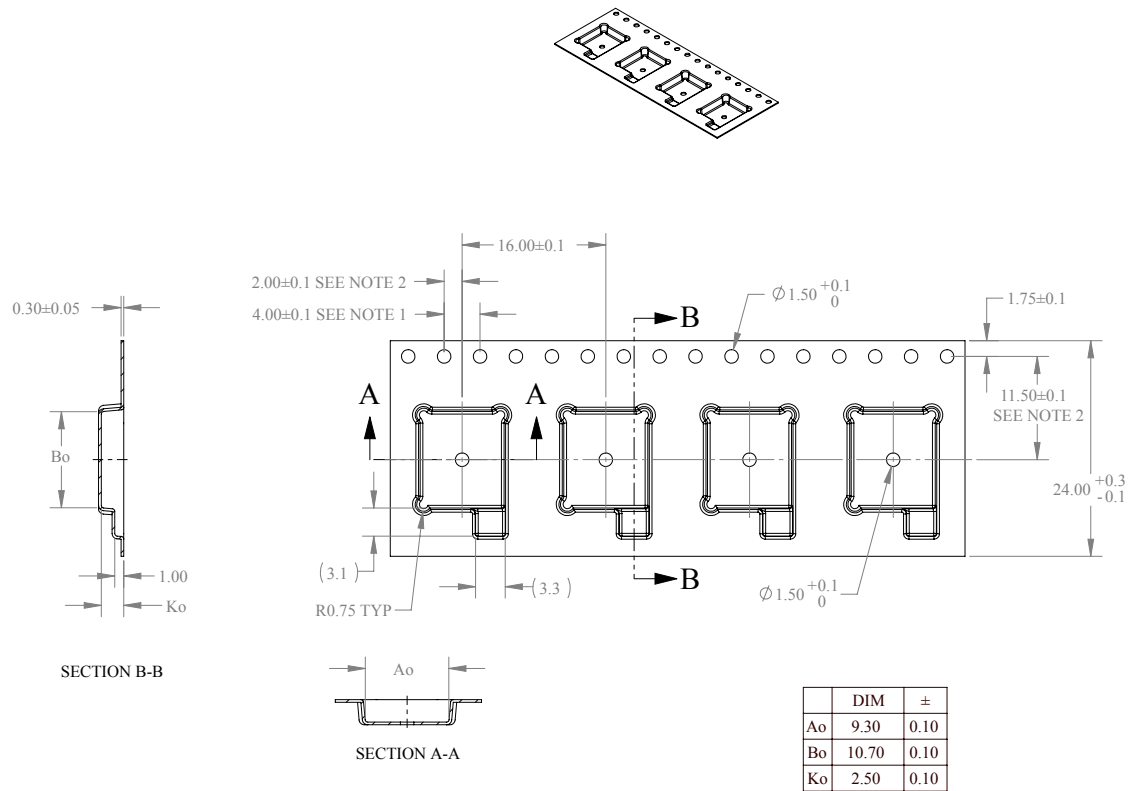
### Figure 36. Tray dimensions



### 9.1.2 Tape and reel information

The carrier tape is wound onto a reel.

**Figure 37. Carrier tape**



Tested dice are delivered as sawn dice which are reconstructed into a wafer format on UV-tape, and delivered on a metallic ring (see figure below). The frames are packed in plastic containers, each including a maximum of 13 double-spaced reconstructed wafer rings. A mapping information file is also provided for localizing dice that may have been damaged during wafer reconstruction on sticking foil.

|   | 1                                                 | 2                                    | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---------------------------------------------------|--------------------------------------|---|---|---|---|---|---|
|   | FEATURE                                           | DESCRIPTION                          |   |   |   |   |   |   |
|   | WAFER DIAMETER                                    | 300mm(12")                           |   |   |   |   |   |   |
| A | GRINDING THICKNESS                                | 200um±10um                           |   |   |   |   |   |   |
|   | SINGULATED DIE SIZE                               | X=6546um±10um<br>Y=5349um±10um       |   |   |   |   |   |   |
|   | SCRIBE WIDTH                                      | X=100um Y=100um                      |   |   |   |   |   |   |
| B | BOND PAD SIZE                                     | X=75.5um Y=141um                     |   |   |   |   |   |   |
|   | BOND PAD OPENING                                  | X=75.5um Y=75.5um                    |   |   |   |   |   |   |
|   | MINIMUM BOND PAD PITCH                            | 161um                                |   |   |   |   |   |   |
| C | OPTICAL ARRAY<br>(OPTICAL CENTER FROM DIE CENTER) | X = 0um Y = 0um                      |   |   |   |   |   |   |
|   | RECONSTRUCTED WAFER STREET WIDTH                  | 500±100um                            |   |   |   |   |   |   |
| D | RW SIZE                                           | ≤200mm                               |   |   |   |   |   |   |
|   | RW OFFSET                                         | (X1-X2)/2=0 ±5mm<br>(Y1-Y2)/2=0 ±5mm |   |   |   |   |   |   |
| E | PLACEMENT<br>ACCURACY X,Y,THETA                   | X,Y(±100um) Theta<1°                 |   |   |   |   |   |   |
|   | SHIPPING TAPE                                     | UV TAPE<br>(ADWILL D-175)            |   |   |   |   |   |   |
|   | FILM FRAME                                        | COMPACT DISCO<br>STAINLESS SUS420    |   |   |   |   |   |   |
| F | MAXIMUM TOTAL DIE COUNT                           | 700 EA                               |   |   |   |   |   |   |
|   | RW LAYOUT                                         | X=28 Y=34                            |   |   |   |   |   |   |

The parts must be stored in a sealed bag for a maximum of 24 months at <40°C and <90% relative humidity (RH).

## 10 Handling, moisture, and reflow profile

### 10.1 Storage conditions

Store all packing material in an appropriate indoor area. This is to prevent any dust and/or damage from the sun, external light, and physical shocks.

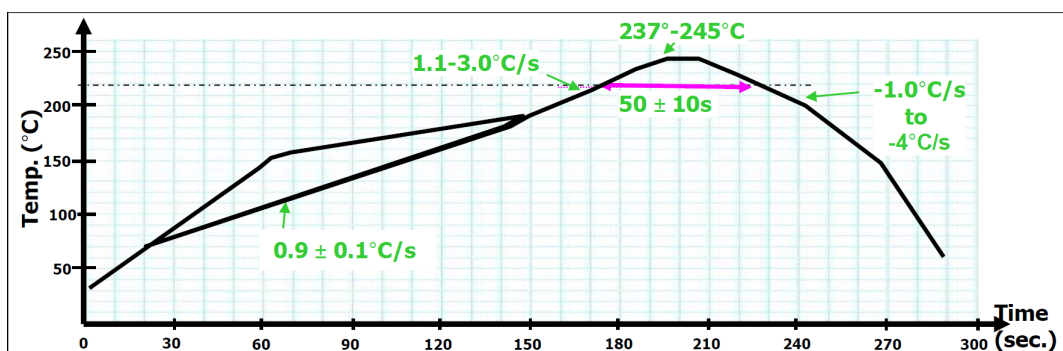
Keep the temperature between 15°C and 35°C, with a relative humidity range between 10% and 70% maximum.

Refer to the Technical Note TN1497, Reconstructed wafer specifications for visual inspection and packing for additional information.

### 10.2 Soldering information

The OBGA package is compliant with the RoHS and “green” standards and is qualified for soldering heat resistance according to JEDEC J-STD-020.

**Figure 39. Soldering temperature vs time**



**Table 37. Soldering details**

| Profile                                        | Ramp to strike             |
|------------------------------------------------|----------------------------|
| Temperature gradient in preheat (T = 70-180°C) | 0.9 ± 0.1°C/s              |
| Temperature gradient (T = 200-225°C)           | 1.1 - 3.0°C/s              |
| Peak temperature in reflow                     | 237°C - 245°C              |
| Time above 220°C                               | 50 ± 10 s                  |
| Temperature gradient in cooling                | -1 to -4°C/s (-6°C/s max.) |
| Temperature from 50°C to 220°C                 | 160 to 220 s               |

## 11 Ordering information

**Table 38. Order code**

| Order code   | Pixel type | Resolution (MPixel) | Package  | Packing             |
|--------------|------------|---------------------|----------|---------------------|
| VB1943CAJX   | RGB NIR    | 5.1                 | OBGA     | Tray                |
| VB1943CAJX/1 |            |                     |          | Tape and reel       |
| VD1943CE/RW  |            |                     | Bare die | Reconstructed wafer |

## 12 Acronyms and abbreviations

**Table 39. Acronyms and abbreviations**

| Acronym/abbreviation | Definition                          |
|----------------------|-------------------------------------|
| ADC                  | Analog-to-digital converter         |
| BIST                 | built-in self-test                  |
| BSI                  | backside illumination               |
| CAB                  | custom analog block                 |
| CCI                  | camera control interface            |
| CPU                  | central processing unit             |
| CRA                  | chief ray angle                     |
| CRC                  | cyclic redundancy check             |
| CSI                  | camera serial interface             |
| DAC                  | Digital-to-analog converter         |
| ECC                  | error correction code               |
| EMC                  | electromagnetic compatibility       |
| EMI                  | electromagnetic interference        |
| FoV                  | field of view                       |
| fps                  | frames per second                   |
| GPIO                 | General-purpose input/output        |
| HDR                  | high dynamic range                  |
| ISL                  | intelligent status line             |
| ISP                  | image signal processor              |
| I <sup>2</sup> C     | Inter-integrated circuit (bus)      |
| NIR                  | near infrared                       |
| OIF                  | output interface                    |
| OTP                  | one-time programmable               |
| PLL                  | phase-locked loop                   |
| PWL                  | piecewise linear                    |
| PWM                  | pulse-width modulation              |
| RGB                  | red green blue                      |
| ROM                  | read-only memory                    |
| SCL                  | serial clock (for I <sup>2</sup> C) |
| SDA                  | serial data (for I <sup>2</sup> C)  |
| SDR                  | standard dynamic range              |
| UI                   | user interface                      |
| SOC                  | system on chip                      |
| MCU                  | microcontroller unit                |
| MPU                  | microprocessor unit                 |

## Appendix A I<sup>2</sup>C interface - SDA, SCL - Norm extract

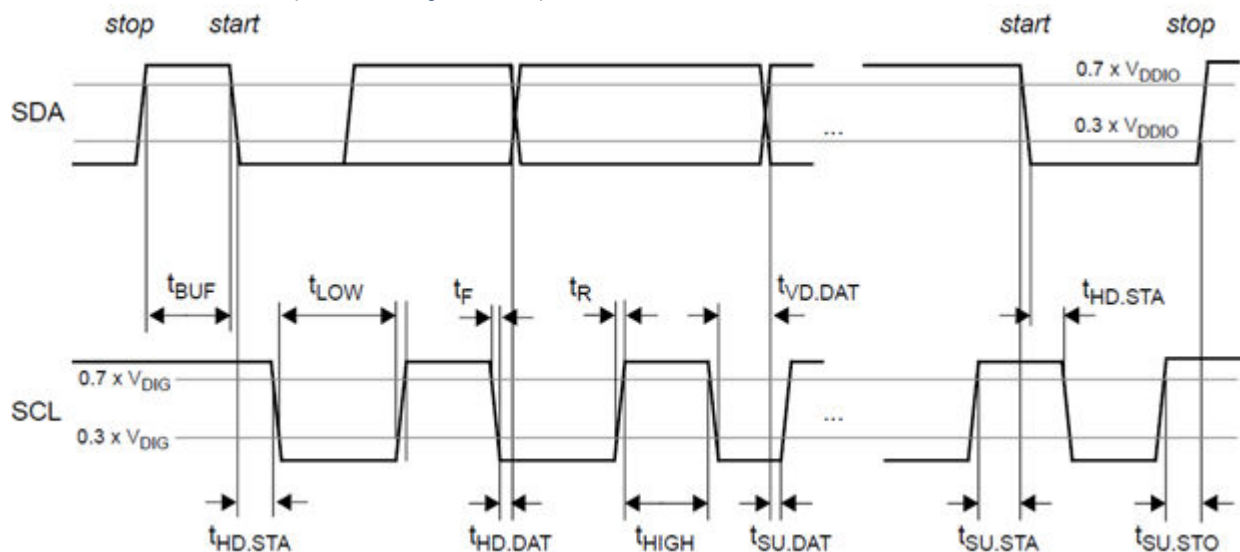
**Table 40. I<sup>2</sup>C timing**

The values below are for all process, voltage, and temperature conditions.

| Parameter                                                                                   | Symbol       | Fast mode                          |      | Fast mode plus                     |      | Unit    |
|---------------------------------------------------------------------------------------------|--------------|------------------------------------|------|------------------------------------|------|---------|
|                                                                                             |              | Min.                               | Max. | Min.                               | Max. |         |
| SCL clock frequency                                                                         | $t_{SCL}$    | 0                                  | 400  | 0                                  | 1000 | kHz     |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated | $t_{HD.STA}$ | 0.6                                | —    | 0.26                               | —    | $\mu s$ |
| LOW period of the SCL clock                                                                 | $t_{LOW}$    | 1.3                                | —    | 0.5                                | —    |         |
| HIGH period of the SCL clock                                                                | $t_{HIGH}$   | 0.6                                | —    | 0.26                               | —    |         |
| Setup time for a repeated START condition                                                   | $t_{SU.STA}$ | 0.6                                | —    | 0.26                               | —    |         |
| Data hold time                                                                              | $t_{HD.DAT}$ | 0                                  | —    | 0                                  | —    | ns      |
| Data set-up time                                                                            | $t_{SU.DAT}$ | 100                                | —    | 50                                 | —    |         |
| Rise time of both SDA and SCL                                                               | $t_R$        | 20                                 | 300  | —                                  | 120  |         |
| Fall time of both SDA and SCL                                                               | $t_F$        | $20 \times (V_{DD}/5.5 \text{ V})$ | 300  | $15 \times (V_{DD}/5.5 \text{ V})$ | 120  | $\mu s$ |
| Set-up time for STOP condition                                                              | $t_{SU.STO}$ | 0.6                                | —    | 0.26                               | —    |         |
| Bus free time between a STOP and START condition                                            | $t_{BUF}$    | 1.3                                | —    | 0.5                                | —    | $\mu s$ |
| Capacity load for each bus line                                                             | $C_O$        | —                                  | 400  | —                                  | 550  | pF      |
| Data valid time                                                                             | $t_{VD.DAT}$ | —                                  | 0.9  | —                                  | 0.45 | $\mu s$ |
| Data valid acknowledge time                                                                 | $t_{VD.ACK}$ | —                                  | 0.9  | —                                  | 0.45 |         |
| Noise margin at LOW level for each connected device (including hysteresis)                  | $V_{nL}$     | $0.054 \times V_{DD}$              |      | $0.054 \times V_{DD}$              |      | V       |
| Noise margin at HIGH level for each connected device (including hysteresis)                 | $V_{nH}$     |                                    |      |                                    |      |         |

**Figure 40. I<sup>2</sup>C timing**

The values below are for all process, voltage, and temperature conditions.



## Appendix B CSI-2 interface - Specification extract

### DC specification

The DC specifications are evaluated by characterization for all process, voltage, and temperature conditions. They are not tested in production.

**Table 41. CSI-2 interface - high-speed mode - DC specifications**

| Symbol            | Parameter                                        | Min | Typical | Max  | Unit     |
|-------------------|--------------------------------------------------|-----|---------|------|----------|
| $V_{\text{CMTX}}$ | HS transmits static common-mode voltage          | 150 | 200     | 250  | mV       |
| $V_{\text{OD}}$   | HS transmits differential voltage <sup>(1)</sup> | 140 | 200     | 270  |          |
| $V_{\text{OHHS}}$ | HS outputs high voltage <sup>(2)</sup>           | —   | —       | 360  |          |
| $Z_{\text{OS}}$   | Single-ended output impedance                    | 40  | 50      | 62.5 | $\Omega$ |

1. Value when driving into load impedance anywhere in the ZID range (80-125  $\Omega$ )

2. Characterization data only

**Table 42. CSI-2 interface - low-power mode - DC specifications**

| Symbol           | Parameter                          | Min | Typical | Max | Unit     |
|------------------|------------------------------------|-----|---------|-----|----------|
| $V_{\text{OH}}$  | Output high-level                  | 1.1 | 1.2     | 1.3 | V        |
| $V_{\text{OL}}$  | Output low-level                   | -50 | —       | 50  | mV       |
| $Z_{\text{OLP}}$ | Output impedance of LP transmitter | 110 | —       | —   | $\Omega$ |

### AC specification

**Table 43. CSI-2 interface - high-speed mode - AC specifications**

| Symbol            | Parameter                               | Min.    | Typ. | Max.   | Unit   |
|-------------------|-----------------------------------------|---------|------|--------|--------|
| —                 | Data rate                               | 250     | 804  | 1500   | Mbit/s |
| $t_{\text{clkp}}$ | Average data period                     | —       | 1.25 | —      | ns     |
| $t_r$ and $t_f$   | $t_r$ 20% - 80% rise time and fall time | 100     | —    | 0.3UI  | ps     |
| $t_{\text{skew}}$ | Data-to-clock skew                      | -0.15UI | —    | 0.15UI |        |

## Revision history

**Table 44. Document revision history**

| Date        | Version | Changes                                                                                                                                                               |
|-------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 09-Apr-2026 | 1       | Initial release                                                                                                                                                       |
| 28-May-2026 | 2       | Section 8.1.3: Glass properties: Reworded for more clarity.<br>Appendix A: I <sup>2</sup> C interface - SDA, SCL - Norm extract: Added I <sup>2</sup> C timing table. |

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