



Product Change Notification: SYST-300CGQ577

Date:

06-Jul-2026

Product Category:

Ethernet Phys

Notification Subject:

LAN8670/1/2 Errata

Affected CPNs:

[SYST-300CGQ577_Affected_CPN_07062026.pdf](#)

[SYST-300CGQ577_Affected_CPN_07062026.csv](#)

Notification Text:

SYST-300CGQ577
Microchip has released a new Document for the LAN8670/1/2 Errata of devices. If you are using one of these devices please read the document located at LAN8670/1/2 Errata. Notification Status: Final Description of Change: Section/Figure/Entry: d8 Correction: Added adjusted RMII output invalid timing to d8 Impacts to Data Sheet: None Reason for Change: To Improve Productivity Change Implementation Status: Complete Date Document Changes Effective: 06 Jul 2026

Description of Change:

Section/Figure/Entry: d8

Correction: Added adjusted RMII output invalid timing to d8

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 06 Jul 2026

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

LAN8670/1/2 Errata

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

Terms and Conditions:

If you wish to receive Microchip PCNs via email please register for our PCN email service at our [PCN home page](#) select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the [PCN FAQ](#) section.

If you wish to change your PCN profile, including opt out, please go to the [PCN home page](#) select login and sign into your myMicrochip account. Select a profile option from

Affected Catalog Part Numbers (CPN)

LAN8670C2-E/LMX

LAN8670C2-E/LMXVAO

LAN8670C2T-E/LMX

LAN8670C2T-E/LMXV03

LAN8670C2T-E/LMXV04

LAN8670C2T-E/LMXV05

LAN8670C2T-E/LMXVAO

LAN8670D0-E/LMX

LAN8670D0-E/LMXV05

LAN8670D0-E/LMXV07

LAN8670D0-E/LMXV08

LAN8670D0-E/LMXV09

LAN8670D0-E/LMXV10

LAN8670D0-E/LMXVAO

LAN8670D0T-E/LMX

LAN8670D0T-E/LMXV03

LAN8670D0T-E/LMXV06

LAN8670D0T-E/LMXV10

LAN8670D0T-E/LMXVAO

LAN8671C2-E/U3B

LAN8671C2-E/U3BVAO

LAN8671C2T-E/U3B

LAN8671C2T-E/U3BV02

LAN8671C2T-E/U3BV06

LAN8671C2T-E/U3BVAO

LAN8671D0-E/U3B

LAN8671D0-E/U3BV01

LAN8671D0-E/U3BV02

LAN8671D0-E/U3BVAO

Date: Monday, July 6, 2026

LAN8671D0T-E/U3B

LAN8671D0T-E/U3BV04

LAN8671D0T-E/U3BVAO

LAN8672C2-E/LNX

LAN8672C2-E/LNXVAO

LAN8672C2T-E/LNX

LAN8672C2T-E/LNXV01

LAN8672C2T-E/LNXVAO

10BASE-T1S Ethernet PHY Transceiver Silicon Errata and Data Sheet Clarifications

LAN8670/1/2



The LAN8670/1/2 devices that you have received conform functionally to the Device Data Sheet (DS60001573K), except for the anomalies described in this document.

The issues discussed in the following pages are for hardware revisions listed in [Table 1](#). The silicon issues are summarized in [Table 1-1](#). Items relating to data sheet changes are summarized in [Table 2-1](#) of the Data Sheet Clarifications section.

Table 1. Silicon Part ID and Hardware Revision Values

Part Number	Part ID ¹	Hardware Revision ¹	Package Marking
LAN8670 LAN8671	010110	0110	D0
LAN8670	010110	0101	C2
LAN8671	010110	0100	C1
LAN8672	010110	0010	B1

Note:

1. The Part ID and Hardware Revision are located in the PHY_ID2 register Model Number and Revision Number fields, respectively. See Data Sheet (DS60001573K) for details.

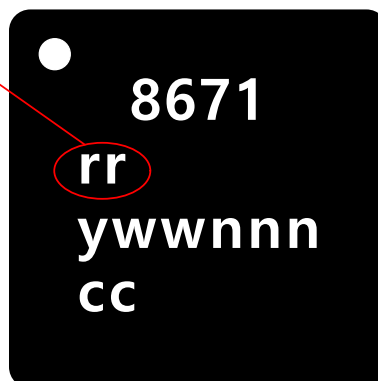
Figure 1. Top Marking for LAN8670 Device

Marking in this position
indicates product revision



Figure 2. Top Marking for LAN8671 Device

Marking in this position
indicates product revision

**Figure 3.** Top Marking for LAN8672 Device

Marking in this position
indicates product revision



1. Device Errata

Table 1-1. Silicon Issue Summary

Item Number	Issue Summary	Affected Devices			
		B1	C1	C2	D0
s1	Media interface mode (RMII) identification	LAN8671	—	—	—
s2	Package Type identification	LAN8671	—	—	—
s3	RMII CSMA/CD operation in mixed PLCA segments	LAN8670 LAN8671	LAN8670 LAN8671	LAN8670 LAN8671	—
s4	Incorrect reset indication on IRQ_N	ALL	—	—	—
s5	Multi-coordinator PLCA action	ALL	ALL	ALL	ALL
s6	Transmission of collision fragments with PLCA and RMII	LAN8670 LAN8671	LAN8670 LAN8671	LAN8670 LAN8671	LAN8670 LAN8671
s7	In RMII mode: incorrect assertion of Carrier Sense may occur following a logical collision	LAN8670 LAN8671	LAN8670 LAN8671	—	—
s8	Revert to CSMA/CD when PLCA Beacons are missing	ALL	—	—	—
s9	Packet pattern matcher incorrectly matches for all message types	ALL	—	—	—
s10	SLPCAL field of SLPCTL0 register may deliver invalid result on read	—	ALL	ALL	—
s11	When configured as a PLCA coordinator, the device does not stop transmitting beacons immediately upon entering sleep mode	—	ALL	ALL	—
s12	A trade-off exists between noise immunity and carrier sense latency	—	ALL	ALL	—
s13	Increased packet latency and coordinator anomalies in large PLCA segments	—	—	ALL	ALL
Legend: — Erratum is not applicable.					

1.1. s1: Media interface mode (RMII) identification

Description

Resolved with the release of Silicon Rev C1. Additional Information available in Data Sheet Clarifications d6 and d7.

1.2. s2: Package Type identification

Resolved with the release of Silicon Rev C1.

1.3. s3: RMII CSMA/CD operation in mixed PLCA segments

Description

The LAN8670/1 RMII cannot be operated with PLCA disabled on a network with other PLCA-enabled nodes. When the device is configured for CSMA/CD operation (i.e., PLCA is disabled), then the reception of PLCA BEACON and COMMIT symbols from the network will be improperly transferred via the RMII to the MAC resulting in undefined behavior including dropped packets.

The LAN8672 does not support RMII operation.

End User Implications

The RMII may only be used with PLCA disabled when all other nodes on the mixing segment are also configured for pure CSMA/CD operation.

Work Around

None.

Resolved with the release of Silicon Rev D0.

1.4. s4: Incorrect reset indication on IRQ_N

Resolved with the release of Silicon Rev C1.

1.5. s5: Multi-coordinator PLCA action**Description**

When operating as a PLCA Coordinator, if the PHY receives an unexpected BEACON from an additional coordinator on the segment, it will set the Unexpected BEACON Received (UNEXPB) bit in the Status 1 (STS1) register. The PHY will then enter a recovery state in which it can receive packets but will transmit neither packets nor BEACONS for the next two PLCA bus cycles. Should the duplicate Coordinator continue sending periodic BEACONS, then the PHY will remain in the recovery state unable to transmit to avoid collisions with the duplicate Coordinator in Transmit Opportunity 0.

Clause 148 of IEEE Std 802.3™ describes that when this condition occurs, the PHY should avoid transmitting in its transmit opportunity until the end of the current bus cycle when the PHY will again transmit its BEACON to the segment.

End User Implications

The PHY will halt transmitting packets and BEACONS to the network when configured as a PLCA Coordinator and an unexpected BEACON is detected. This results in the node becoming an inactive Coordinator.

Work Around - Revision C2 and earlier

The station management entity should monitor the Unexpected BEACON Received bit and configure the PHY as a PLCA Follower.

Work Around - Revision D0

As of revision D0, this silicon errata may be resolved with the register configuration provided in the table below.

Note: The configuration provided by the *LAN8670/1/2 Configuration Application Note*, DS60001699, includes the following register access to work around this silicon issue. If the configuration recommended by this Application Note is followed, then the register write in the following table is not necessary.

Access	MMD	Address	Data
Write	0x1F	0x0037	0x0800

1.6. s6: Transmission of collision fragments with PLCA and RMII**Description**

Clause 4 of IEEE Std 802.3 specifies the MAC shall implement an Inter-Packet Gap (IPG) delay of 96 bit times (BT) between packets. This IPG is split into two parts. The first part, IPG part 1, requires that no carrier be sensed. If carrier is sensed during IPG part 1, then the timer is restarted. Once IPG part 1 is complete, the MAC may transmit following IPG part 2. The IPG part 1 is nominally 64 BT, but may be less, including zero. The IPG part 2 timing is nominally 32 BT, but is always equal to the full IPG duration minus the IPG part 1.

Some MACs implement an IPG part 1 of very small duration. If the IPG part 1 time is too small, then the MAC may attempt to transmit after the PHY has asserted carrier indication with CRSDV. The result is that the MAC will quickly detect a collision and send a collision fragment to the PHY. When PLCA is enabled, the PHY, not expecting the MAC to transmit after carrier was indicated, will not detect the collision and end up transmitting the collision fragment to the network.

End User Implications

Use of a MAC with an IPG part 1 time of less than 18 bits will result in the transmission of short 10.4 μs packets onto the network.

Work Around

While the transmission of the collision fragments to the network are benign, they may be eliminated by reducing the size of the PLCA delay line buffer with the register configuration provided below. This will cause the MAC to detect a normal logical collision preventing the transmission of the collision fragment. Additionally, the PHY will capture the next transmit opportunity guaranteeing the MAC the ability to transmit according to the PLCA algorithm.

Access	MMD	Address	Data	Mask
RMW	0x1F	0x008F	0x00E0	0x07F0

Legend:

R - Read

W - Write

RMW - Read-Modify-Write

1.7. **s7: In RMI mode: incorrect assertion of Carrier Sense may occur following a logical collision**

Resolved with the release of Silicon Rev C2.

1.8. **s8: Revert to CSMA/CD when PLCA Beacons are missing**

Resolved with the release of Silicon Rev C1.

1.9. **s9: Packet pattern matcher incorrectly matches for all message types**

Resolved with the release of Silicon Rev C1.

1.10. **s10: SLPCAL field of SLPCTL0 register may deliver invalid result on read**

Description

When reading the SLPCTL0 register, the SLPCAL field returns 0x0001. This bitfield must always be written as 0x0000.

End User Implications

Sleep mode may not function properly if this bitfield is set to anything other than 0.

Work Around

When writing to the SLPCTL0, including when performing read-modify-write sequences, ensure that the SLPCAL bitfield is always written as 0x0000.

Resolved with the release of Silicon Rev D0.

1.11. **s11: When configured as a PLCA coordinator, the device does not stop transmitting beacons immediately upon entering sleep mode**

Description

The device does not stop transmitting beacons immediately upon entering sleep mode when configured as a PLCA coordinator. The coordinator node, NODE_ID = 0, transmits a beacon at the start of each PLCA bus cycle. When sleep mode begins, the transmitter is not disabled until VDDA drops below its valid level. When configured to sleep on the inactivity timeout, the coordinator node will recognize the beacon as bus activity and wake itself back up.

End User Implications

The coordinator mode will not reliably remain in sleep mode when configured to sleep on an inactivity timeout, as it will interpret its own beacon as network activity. Continued presence of beacons will cause other devices on the mixing segment to detect signal activity, so any other devices that are configured to sleep on inactivity will not sleep.

Work Around

The coordinator node (NODE_ID = 0) must never be configured to sleep on inactivity timers. It must be put into sleep mode by its station controller. In addition, immediately before entering sleep, the coordinator must have PLCA disabled to stop the beacon.

1. Clear the EN bit of the PLCA_CTRL0 to disable the beacon.
2. Enter sleep mode and configure a non-zero delay by writing to the following bitfields of SLPCTL0:
 - Set SLPEN to 1.
 - Set WKINEN and MDIWKEN to configure desired wake source(s).
 - SLPCAL must be written as 0x0.
 - Set SLPINHDLY to 1 or greater.

Resolved with the release of Silicon Rev D0.

1.12. s12: A trade-off exists between noise immunity and carrier sense latency**Description**

When configured to work in noisy environments, such as those required to pass standard EMI/EMC tests, it is necessary to use additional filtering, which increases carrier sense latency. The recommended default configuration, which is required to pass these tests, results in a longer carrier assertion time, which imposes a limitation on the usable range of the PLCA Transmit Opportunity Timer. As a reminder, this value must be configured equally among all nodes in the mixing segment. Values below the default can, theoretically, provide insignificant increases in throughput at the cost of system robustness.

End User Implications

- The default value, in the specification and for this device, is 3.2 us (TO_TMR = 32). Using this value is strongly recommended except when collisions are detected on a PLCA enabled multidrop mixing segment containing third party devices.
- This device should never be configured with TO_TMR < 29, and values less than 32 require the user thoroughly test the final system for robustness.

Work Around

The Transmit Opportunity timer (TO_TMR) should be configured with the default value of 32. In the event that a smaller value is used, it must always be 29 or greater.

If collisions are detected during operation with devices from third-party vendors on the mixing segment, the Transmit Opportunity Timer may need to be increased to greater than 32. As the necessary value will be dependent upon various latency characteristics of other devices on the mixing segment, as well as the propagation delay on the physical medium, contact Microchip support.

Resolved with the release of Silicon Rev D0.

1.13. s13: Increased packet latency and coordinator anomalies in large PLCA segments**Description**

The PLCA sublayer includes a FIFO which acts as an elastic buffer to align transmit packets coming from the MAC with the device's transmit opportunity. If a MAC begins data transmission outside of a valid transmit opportunity, the elastic buffer will store MAC transmit data until it is full. If the transmit opportunity starts before this buffer is full, data will be transmitted onto the mixing segment delayed by the FIFO. If the elastic buffer fills before the transmit opportunity starts, a logical collision is signaled to the MAC and carrier sense is held asserted. The MAC will stop transmitting the packet, back off, and retransmit the packet at the device's next appropriate transmit opportunity. The device indicates this transmit opportunity by de-asserting carrier sense.

In the event that the PLCA elastic buffer becomes full at the same time as the assigned transmit opportunity begins, the device will exhibit the following deviations from expected behavior:

1. The device will assert carrier sense for only a short time.
2. The device will transmit a single 'J' symbol on TRXN/P during the node's transmit opportunity instead of a valid Ethernet packet.

Additionally, in a coordinator, when the PLCA elastic buffer becomes full at the same time as a beacon is being transmitted, the beacon is properly transmitted. However, the device will exhibit the following deviations from expected behavior:

3. In RMII mode, the coordinator will ignore received packets after the transmitted beacon until the device's next valid transmit opportunity.
4. In MII mode, the COL pin of the coordinator may exhibit a short de-assertion pulse during a logical collision coincident with the transmission of a beacon.

Due to the size of the internal elastic buffer, these deviations can only happen on mixing segments with more than 11 idle transmit opportunities in a row.

End User Implications

In a system where more than 11 idle transmit opportunities occur in a row, there is a small possibility that a transmitted packet will fill the elastic buffer FIFO at exactly the time that the transmit opportunity starts in the node. Should this happen, the fault behaviors above will have the following consequences:

1. The MAC will react to the early de-assertion of carrier sense and attempt to re-transmit the packet earlier than it should following a logical collision. If the MAC retry timing is such that the FIFO becomes full at the start of the transmit opportunity, the packet latency will increase as the MAC will use the exponential back off algorithm to determine when to retry transmission. Should retries continue to occur for a single packet, the exponential back off will continue to increase. It is unlikely but possible that the packet may be dropped by the MAC due to excessive retries. In this case, the transmitter will fail to transmit the packet.
2. It is theoretically possible that other devices on the mixing segment may detect a short carrier sense due to the transmitted 'J' symbol which could cause one packet to be delayed in transmission, however, there are no known devices which detect carrier based on a single 'J' symbol.
3. An RMII coordinator may miss receiving packets.
4. The brief de-assertion of the COL pin has not been shown to have any negative effects on MACs.

Work Around

This issue can only occur with more than 11 idle transmit opportunities in a row. This maximum number of transmit opportunities for a mixing segment is set by the NCNT bit field of the PLCA_CTRL1 register of the coordinator. If this bit field is set to 11 or less, this behavior will never occur.

A system in which the end application can tolerate an occasional delayed packet is called latency insensitive. Even when a system has 12 or more transmit opportunities, if it is latency insensitive there may be no need for a workaround.

When a system has 12 or more transmit opportunities, is latency sensitive, and the end application uses a packet numbering and a retry mechanism, such as used in TCP, there may be no need for a workaround.

If a latency sensitive system requires 12 or more transmit opportunities, traffic flows should be designed to avoid more than 11 sequential idle transmit opportunities. If a small number of devices are using most of the transmit bandwidth, burst mode should be avoided but the multiple node ID feature can be used to distribute the load so that there are no more than 11 idle transmit

opportunities. A heart-beat safety mechanism, as recommended in the safety manual, can also be used to keep nodes active.

Plan

This erratum will be corrected in an upcoming revision.

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the data sheet (DS60001573K):

Table 2-1. Data Sheet Clarification Summary

Item Number	Port Function	Issue Summary	Resolved with Data Sheet Revision
d1	Table 3-7. Miscellaneous Pins	The table incorrectly states that clock oscillators may be used in MII mode.	DS60001573F
d2	Section 4.1 Media Independent Interface (MII)	Text does not clearly state that a crystal must be used in MII mode.	DS60001573F
d3	Section 4.8.1 Crystal Pins (XTI/XTO)	Text incorrectly states that clock oscillators may be used in MII mode.	DS60001573F
d4	Figure 4-4. Crystal Oscillator Input	Figure incorrectly states that clock oscillators may be used in MII mode.	DS60001573F
d5	Table 7-7. DC Electrical Characteristics (other than 10BASE-T1S PMA)	Note 3 incorrectly states that the MII crystal input XTI may be driven by a clock oscillator.	DS60001573F
d6	Port/Function: 3.5.1 Device Mode (MODE[1:0])	It is unclear that the behavior of the mode configuration strap bits varies with part number.	DS60001573J
d7	Port/Function: 5.1.7 Strap Control 0 Register	The MITYP bit field should be documented as undetermined for the LAN8671 and LAN8672.	DS60001573J
d8	Table 7-15. RMII Timing	The RMII setup and output invalid times have been updated.	—

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1. d1: Table 3-7. Miscellaneous Pins

Resolved with the release of Data Sheet DS60001573F.

2.2. d2: Section 4.1 Media Independent Interface (MII)

Resolved with the release of Data Sheet DS60001573F.

2.3. d3: Section 4.8.1 Crystal Pins (XTI/XTO)

Resolved with the release of Data Sheet DS60001573F.

2.4. d4: Figure 4-4. Crystal Oscillator Input

Resolved with the release of Data Sheet DS60001573F.

2.5. d5: Table 7-7. DC Electrical Characteristics (other than 10BASE-T1S PMA)

Resolved with the release of Data Sheet DS60001573F.

2.6. d6: Port/Function: 3.5.1 Device Mode (MODE[1:0])

Resolved with the release of Data Sheet DS60001573J.

2.7. d7: Port/Function: 5.1.7 Strap Control 0 Register

Resolved with the release of Data Sheet DS60001573J.

2.8. d8: Table 7-15. RMII Timing

The guaranteed RMII timings has been updated. The minimum setup timing is reduced to 2 ns and the minimum output invalid time is being increased to 4 ns. Replace Table 7-15 in section 7.6.7 with the following updated table.

Table 7-15. RMII Timing

Description	Symbol	Min	Typ	Max	Units	Additional Information
REFCLKIN period	t_{clkp}		20		ns	Note 1
REFCLKIN high time	t_{clkh}	$t_{clkp} * 0.45$		$t_{clkp} * 0.55$	ns	Note 1, 2
REFCLKIN low time	t_{clkl}	$t_{clkp} * 0.45$		$t_{clkp} * 0.55$	ns	Notes 1, 2
RXD[1:0], RXER, CRSDV output valid from rising edge of REFCLKIN	t_{oval}			12	ns	
RXD[1:0], RXER, CRSDV output invalid from rising edge of REFCLKIN	t_{oinvld}	4.0			ns	
TXD[1:0], TXEN setup time to rising edge of REFCLKIN	t_{su}	2.0			ns	
TXD[1:0], TXEN hold time after rising edge of REFCLKIN	t_{ihold}	1.5			ns	
Notes: 1. Design parameter, not tested. 2. 1.8V 50 MHz clock input on REFCLKIN						

3. Revision History

Table 3-1. Errata Sheet Revision History

Revision Level & Date	Section/Figure/Entry	Correction
DS80000962J, 06/2026	d8	Added adjusted RMII output invalid timing to d8
DS80000962I, 05/2026	s13	Added Errata
	s5	Added resolution for Rev D0 silicon
	d8	Added Data Sheet clarification d8 for relaxed RMII setup timing
DS80000962H		Not issued
DS80000962G, 10/2025	s3	Updated for Rev D0 silicon
	s10	
	s11	
	s12	
DS80000962F, 3/2025	s1	Added reference to Data Sheet clarifications
	d6	Added Data Sheet clarification for Device Mode
	d7	Added Data Sheet clarification for Strap Control
DS80000962E, 12/2023	s7	Updated for Rev C2 silicon
DS80000962D, 7/2023	s7	Updated details
	s11	Clarified issue summary
DS80000962C, 6/2023		Updated for Rev C1 silicon Data Sheet Clarifications resolved
DS80000962B, 1/2023		Added Data Sheet Clarification section
DS80000962A, 7/2021	ALL	Initial Release of Errata

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at <https://www.microchip.com/en-us/about/legal-information/microchip-trademarks>.

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP “AS IS”. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP’S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip products are strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.