

Enhancement Mode Gallium Nitride (GaN) HEMT

100 V, 3.8 mΩ, 146 A, PTFP-N9

NTLCC5D0N10GN1

Features

- Low $R_{DS(ON)}$ to Minimize Conduction Losses
- Ultra Low Gate Charge for High Speed Switching
- $FOM-Q_G = 21.7 \text{ nC} \cdot \text{m}\Omega$
- Small Footprint for High Density PCB Design
- Pb-Free, Halogen Free and RoHS Compliant

Typical Applications

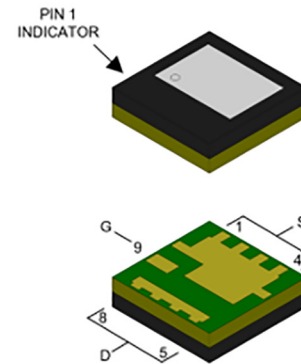
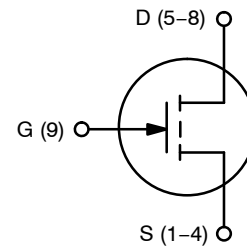
- High Density Power Modules
- High Frequency DC-DC Converters
- High Power Synchronous Rectifiers
- Motor Drivers

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	100	V
Drain-to-Source Transient Voltage, total time = 1 h, non-repetitive	$V_{DS(TRAN)}$	120	V
Gate-to-Source Voltage	V_{GS}	-4 to 6	V
Gate-to-Source Transient Voltage, $t_p = 100 \text{ ns}$, $f_p = 100 \text{ kHz}$, open drain	$V_{GS(PULSE)}$	6.5	V
Continuous Drain Current, $T_{CASE} = 25^\circ\text{C}$ $T_{CASE} = 100^\circ\text{C}$	I_{DS}	146 93	A
Pulsed Drain Current, $t_p < 100 \mu\text{s}$, $T_J = 25^\circ\text{C}$ $T_J = 150^\circ\text{C}$	$I_{DS(PULSE)}$	300 230	A
Power Dissipation, $V_{GS} = 5 \text{ V}$, $T_{CASE} = 25^\circ\text{C}$	P_{TOT}	208	W
Operating Junction Temperature	T_J	-40 to 150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 to 150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ TYP}$	$I_{DS} \text{ MAX}$
100 V	3.8 mΩ	146 A



PTFP-N9 3.30 x 3.30 x 0.87, 0.65P
CASE 522AF

MARKING DIAGRAM



5D0N10 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Junction-to-Cases	$R_{\theta JC}$	0.6	$^{\circ}\text{C/W}$
Junction-to-Board	$R_{\theta JB}$	7.0	$^{\circ}\text{C/W}$
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	50	$^{\circ}\text{C/W}$
Maximum Soldering Temperature (MSL3)	T_{SLD}	260	$^{\circ}\text{C}$

1. Device on 1 in², 2 oz copper pad on single layer FR-4 PCB

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$	100			V
Drain-to-Source Leakage Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}$		0.3	70	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, T_J = 125^{\circ}\text{C}$ (Note 3)		70		
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = 6\text{ V}, V_{DS} = 0\text{ V}$		0.2	70	μA
		$V_{GS} = 6\text{ V}, V_{DS} = 0\text{ V}, T_J = 125^{\circ}\text{C}$ (Note 3)		10		μA

ON CHARACTERISTICS (Note 2)

Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = 5\text{ V}, I_{DS} = 20\text{ A}$		3.8	5.0	$\text{m}\Omega$
		$V_{GS} = 5\text{ V}, I_{DS} = 20\text{ A}, T_J = 125^{\circ}\text{C}$ (Note 3)		6.6		
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_{DS} = 5.5\text{ mA}, T_J = 25^{\circ}\text{C}$	0.8	1.1	2.1	V
		$V_{DS} = V_{GS}, I_{DS} = 5.5\text{ mA}, T_J = 125^{\circ}\text{C}$ (Note 3)		1.0		

DYNAMIC CHARACTERISTICS (Note 3)

Input Capacitance	C_{ISS}	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		681		pF
Output Capacitance	C_{OSS}			292		
Reverse Transfer Capacitance	C_{RSS}			4.7		
Output Capacitance, Energy Related	$C_{OSS(ER)}$	$V_{DS} = 0\text{ V to } 50\text{ V}, V_{GS} = 0\text{ V}$		456		pF
Output Capacitance, Time Related	$C_{OSS(TR)}$			648		
Output Charge	Q_{OSS}			32.4		nC
Output Capacitance Stored Energy	E_{OSS}			0.57		μJ
Gate Resistance	R_G	$f = 5\text{ MHz}$		0.7		Ω
Gate Charge	Q_G	$V_{DS} = 50\text{ V}, I_{DS} = 20\text{ A}, V_{GS} = 0/5\text{ V}$		5.2		nC
Gate-to-Source Charge	Q_{GS}			1.4		
Gate-to-Drain Charge	Q_{GD}			0.83		
Gate Plateau Voltage	V_{PLAT}			2.1		V

REVERSE CONDUCTION CHARACTERISTICS

Source-to-Drain Reverse Voltage	V_{SD}	$V_{GS} = -3\text{ V}, I_{SD} = 20\text{ A}$ (Note 3)		4.7		V
		$V_{GS} = 0\text{ V}, I_{SD} = 20\text{ A}$		2.0		
		$V_{GS} = 5\text{ V}, I_{SD} = 20\text{ A}$ (Note 3)		0.08		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. No prior drain bias or switching stress is applied during the measurement of $V_{GS(TH)}$ and $R_{DS(ON)}$.
3. Defined by design, not subject to production test.

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TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

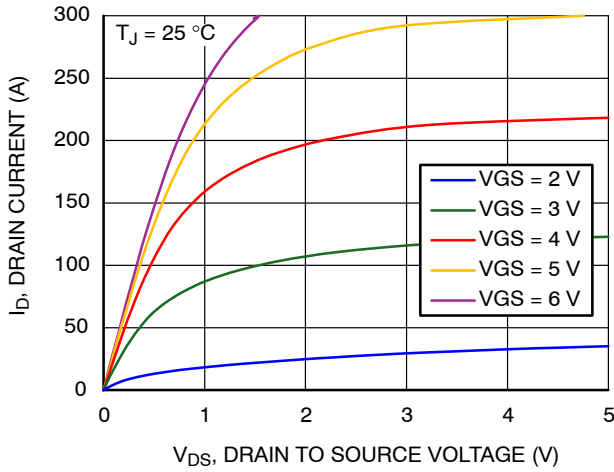


Figure 1. Output Characteristics at $T_J = 25^\circ\text{C}$

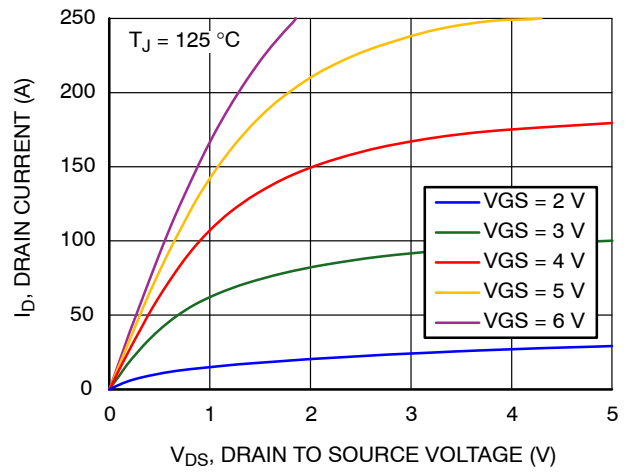


Figure 2. Output Characteristics at $T_J = 125^\circ\text{C}$

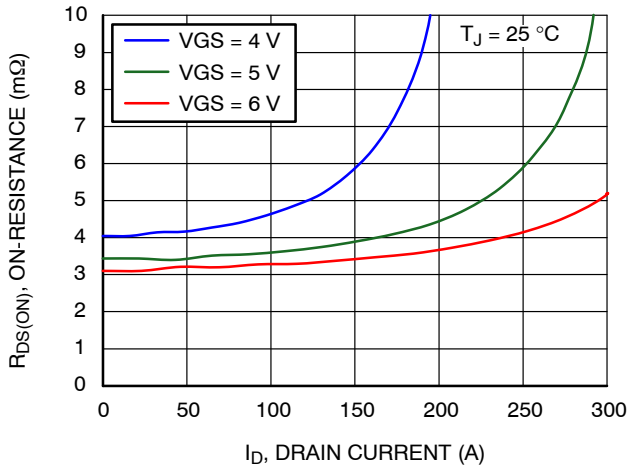


Figure 3. On-Resistance vs. Drain Current at $T_J = 25^\circ\text{C}$

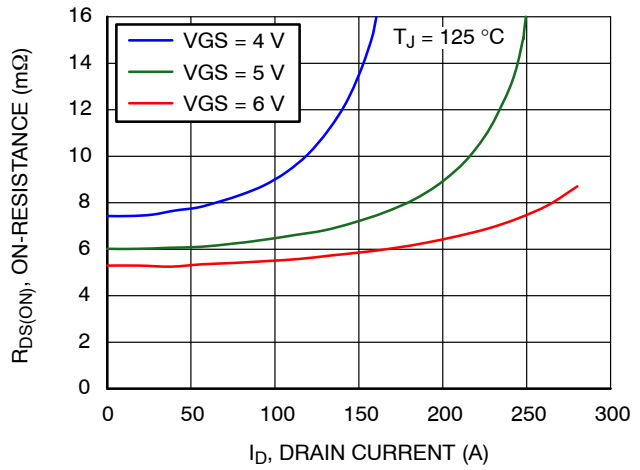


Figure 4. On-Resistance vs. Drain Current at $T_J = 125^\circ\text{C}$

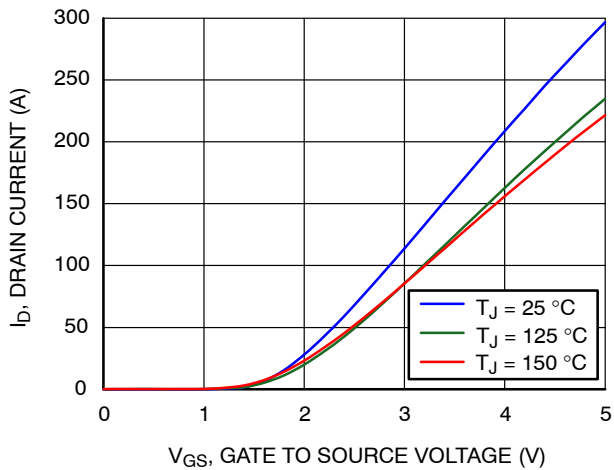


Figure 5. Transfer Characteristics at $V_{DS} = 3\text{ V}$

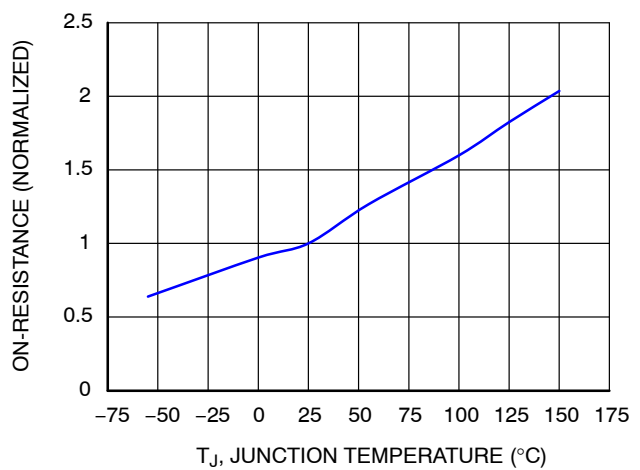


Figure 6. Normalized On-Resistance vs. Temperature at $V_{GS} = 5\text{ V}$

TYPICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified) (continued)

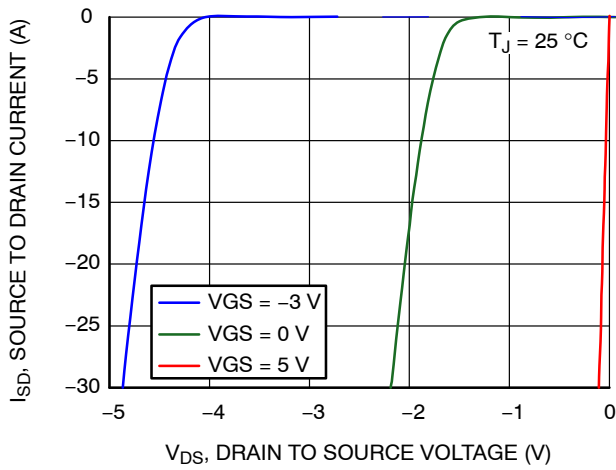


Figure 7. Reverse Conduction Characteristics at $T_J = 25\text{ }^{\circ}\text{C}$

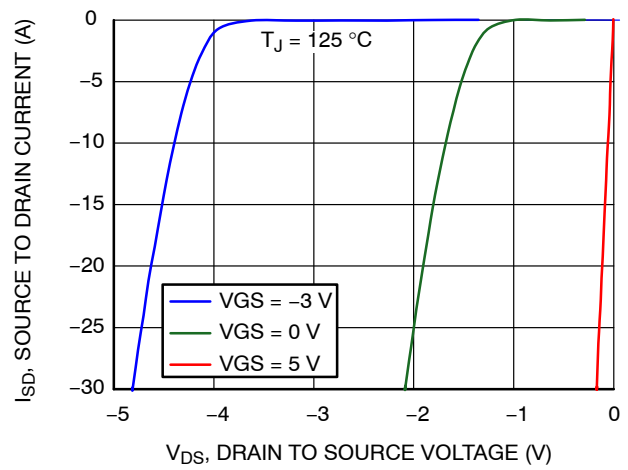


Figure 8. Reverse Conduction Characteristics at $T_J = 125\text{ }^{\circ}\text{C}$

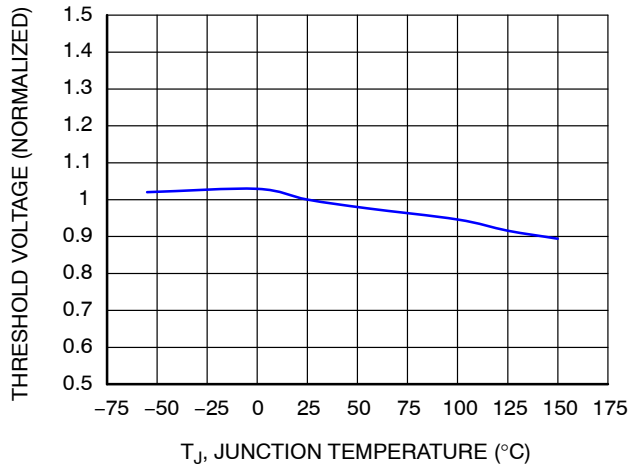


Figure 9. Normalized Threshold Voltage vs. Temperature

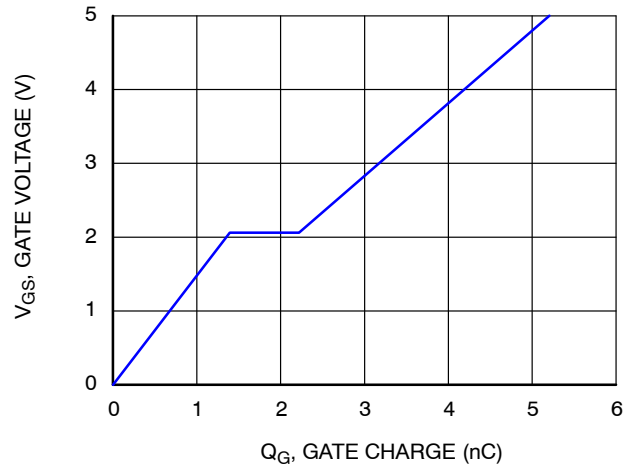


Figure 10. Gate Charge Characteristics at $I_{DS} = 20\text{ A}$

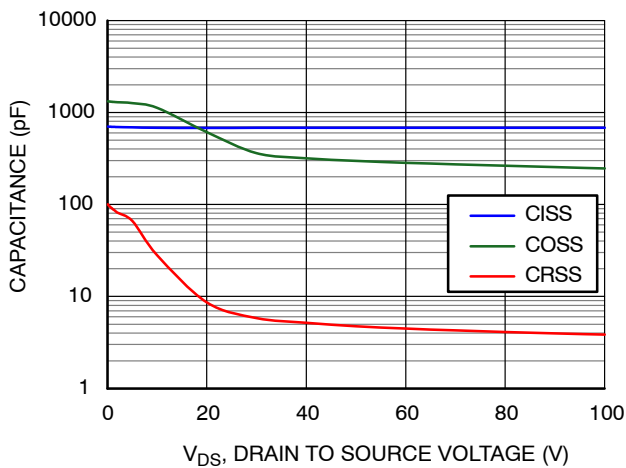


Figure 11. Capacitance Characteristics

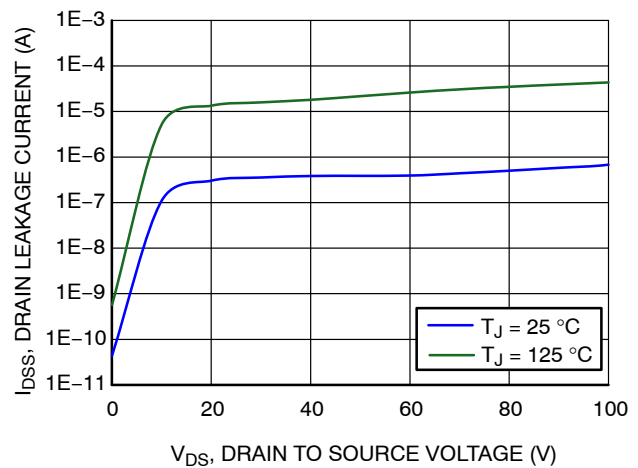


Figure 12. Drain Leakage Characteristics

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TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified) (continued)

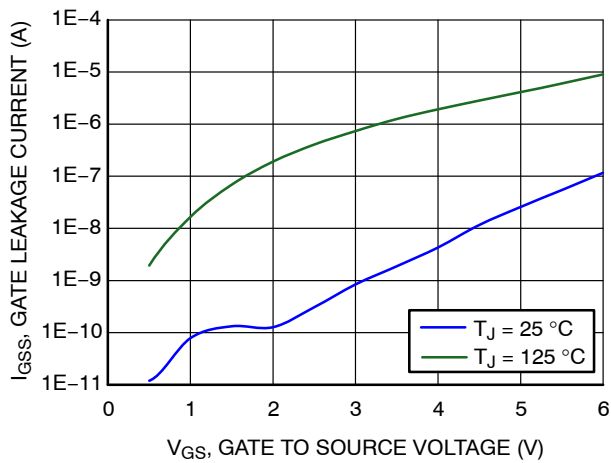


Figure 13. Gate Leakage Characteristics

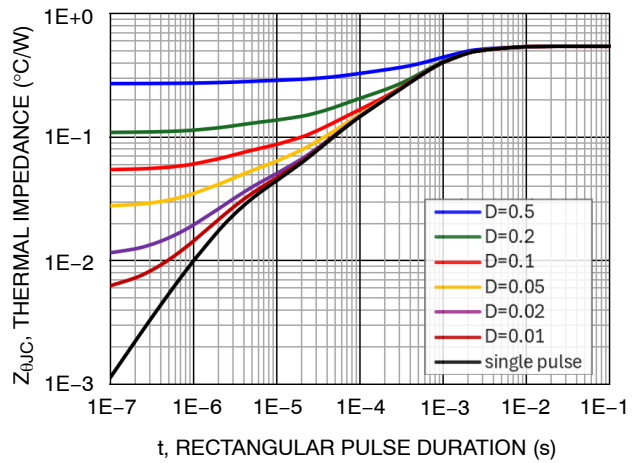


Figure 14. Transient Thermal Impedance

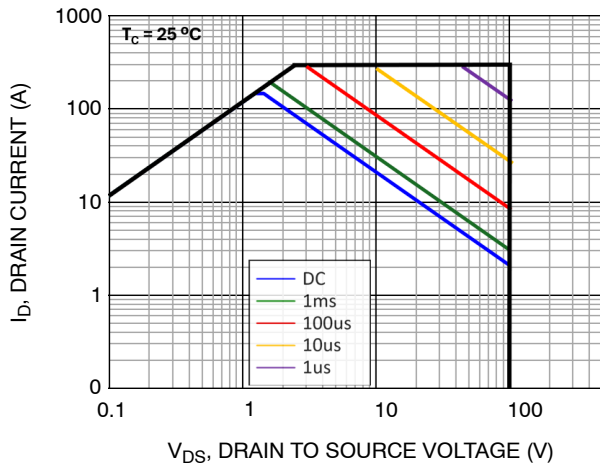


Figure 15. Safe Operating Area at $T_C = 25^\circ\text{C}$

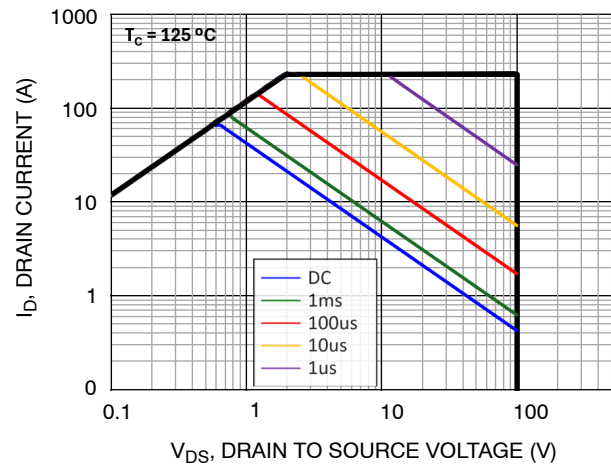


Figure 16. Safe Operating Area at $T_C = 125^\circ\text{C}$

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Gate Drive Guidelines

This GaN device utilizes a Schottky gate structure, which behaves similarly to a MOSFET with a purely capacitive input and does not require continuous gate current during the on-state. For optimal performance, apply a low-impedance gate driver with appropriate gate resistance to control switching speed and limit ringing. A typical gate voltage of

5 – 6 V is recommended, with optional negative gate bias for hard-switching applications to improve dv/dt immunity and prevent false turn-on. Minimize gate loop inductance (<1 nH) through careful PCB layout and short connections. For additional robustness, Zener clamps may be used to limit gate voltage in both polarities.

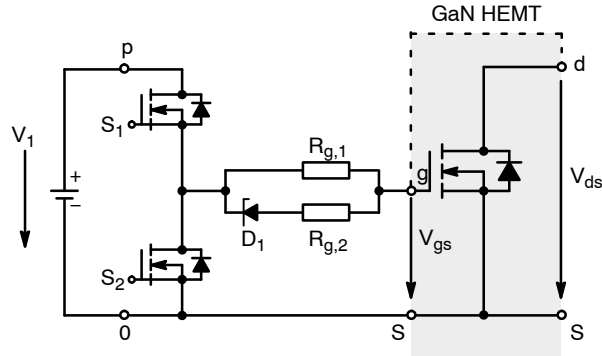


Figure 17. Schottky Gate Conventional Driver Schematic

ORDERING INFORMATION

Device Order Number	Package Type	Shipping [†]
NTLCC5D0N10GN1TWG	PTFP-N9 3.30 x 3.30 x 0.87, 0.65P (Pb-Free)	2500 / Tape & Reel

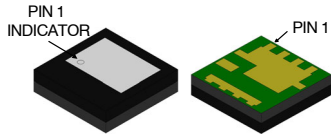
[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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REVISION HISTORY

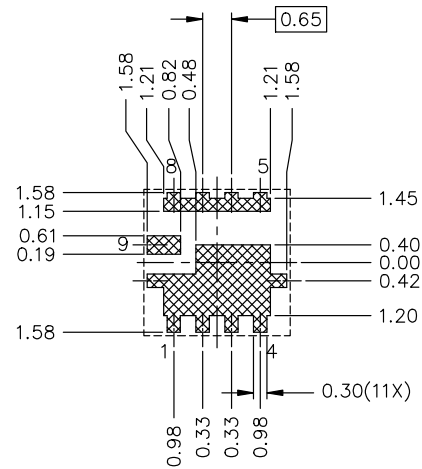
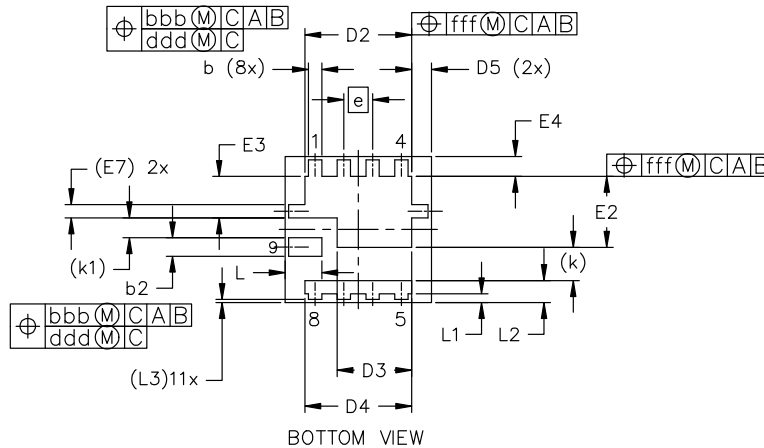
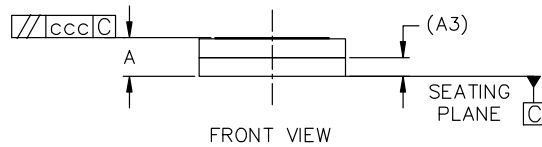
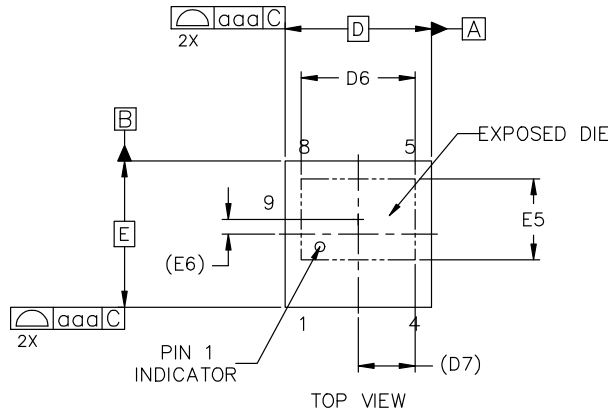
Revision	Description of Changes	Date
0	Initial document release.	6/15/2026





PTFP-N9 3.30x3.30x0.87, 0.65P
CASE 522AF
ISSUE A

DATE 04 MAY 2026

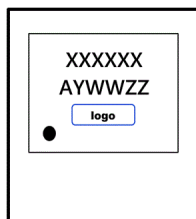


LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE
STRATEGY AND SOLDERING DETAILS, PLEASE
DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING
TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

UNIT IN MILLIMETER			
DIM	MIN	NOM	MAX
A	0.77	0.87	0.97
A3	0.42 REF		
b	0.25	0.30	0.35
b2	0.37	0.42	0.47
D	3.30 BSC		
D2	2.31	2.41	2.51
D3	1.58	1.68	1.78
D4	2.31	2.41	2.51
D5	0.35	0.45	0.55
D6	2.20	—	2.70
D7	1.29 REF		
E	3.30 BSC		
E2	1.50	1.60	1.70
E3	0.84	0.94	1.04
E4	0.35	0.45	0.55
E5	1.60	—	2.10
E6	0.33 REF		
E7	0.30 REF		
e	0.65 BSC		
k	0.75 REF		
k1	0.45 REF		
L	0.73	0.83	0.93
L1	0.10	0.20	0.30
L2	0.40	0.50	0.60
L3	0.075 REF		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
fff	0.10		

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to
device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "•", may
or may not be present. Some products may
not follow the Generic Marking.

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