Automotive LPDDR5X SDRAM

MT62F1G32D2, MT62F2G32D4, MT62F4G32D8

Features

- **Architecture**
  - 19.2 GB/s maximum bandwidth per channel
  - Frequency range: 1200–5 MHz (data rate range per pin: 9600–40 Mb/s with WCK:CK = 4:1)
  - Selectable CKR (WCK:CK = 2:1 or 4:1)
- **LPDDR5X/LPDDR5 data interface**
  - Single x16 channel/die
  - Double-data-rate command/address entry
  - Differential command clocks (CK_t/CK_c) for high-speed operation
  - Differential data clocks (WCK_t/WCK_c)
  - Optional differential read strobe (RDQS_t/RDQS_c)
  - 16*n*-bit or 32*n*-bit prefetch architecture
  - Bank Architecture: Bank Group (BG) mode, and 16-bank (16B) mode supported
  - Command-selectable burst lengths (BL = 16 or 32) in bank group or 16-bank modes
  - Background ZQ cal/Cmd-based ZQ calibration
  - Optional link protection (link ECC)
  - Partial-array self refresh (PASR) and partial-array auto refresh (PARC) with segment mask
- **Ultra-low-voltage core and I/O power supplies**
  - V_{DD1} = 1.70–1.95V; 1.80V TYP
  - V_{DD2H} = 1.01–1.12V; 1.05V TYP
  - V_{DD2L} = V_{DD2H} or 0.87–0.97V; 0.90V TYP
  - V_{DDQ} = 0.50V or 0.45V[1] TYP; 0.30V TYP (ODT off only)
- **I/O characteristics**
  - Interface-LVSTL 0.5/0.3
  - I/O type: Low-swing single-ended, V_{SS} terminated
  - V_{OH}-compensated output drive
  - Programmable V_{SS} on-die termination (ODT)
  - Non target ODT support
  - DVFSQ support
  - Per byte and per pin DFE support
- **Low power features**
  - Enhanced DVFSC: Enhanced dynamic voltage frequency scaling core
  - Single-ended (CK, WCK, RDQS)
  - Data copy
  - Write X

Options	Marking
• **Operating Voltage**	F
– $V_{DD1}/V_{DD2H}/V_{DD2L}/V_{DDQ}/V_{DDQ}$ (ODT off only): 1.80V/1.05V/V_{DD2H} or 0.90V/0.50V or 0.45V[1]/0.30V	
• **Array Configuration**	
– 1Gb x 32 (1Gbx16 x 1die x 2Ch x 1R)	1G32
– 2Gb x 32 (1Gbx16 x 1die x 2Ch x 2R)	2G32
– 4Gb x 32 (2Gbx8 x 2 die x 2Ch x 2R)	4G32
• **Device configuration**	
– 2 die in package (1Gb16 x 2 die)	D2
– 4 die in package (1Gb16 x 4 die)	D4
– 8 die in package (2Gb8 x 8 die)	D8
• **FBGA RoHS-compliant "green" package**	
– 315-ball TFBGA 12.4mm x 15.0mm (TYP), seated height 1.1mm (MAX)	DS
– 315-ball LFBGA 12.4mm x 15.0mm (TYP), seated height 1.3mm (MAX)	DV
• Speed grade, cycle time (^{t}WCK)	
– 9600 Mb/s	-020
• **Functional safety, DLEP & RAS**	F[2]
– ISO 26262 ASIL D and IEC 61508 SIL 3 compliant	
– ASIL D/SIL 3 systematic fault coverage	
– Suitable for meeting random HW metrics up to ASIL D/SIL 3	
– Micron safety documentation	
– Micron safety features enabled	
– Direct Link ECC Protocol (DLEP)	
– Improved RAS	
• **Automotive**	A
– AEC-Q100	
– PPAP	
• **Operating temperature:**	
– –40°C ≤ T_C ≤ +95°C	IT
– –40°C ≤ T_C ≤ +105°C	AT
– –40°C ≤ T_C ≤ +125°C	UT[3]
• Revision	:D

Notes: 1. V_{DDQ} = 0.45V (TYP) support on all packages up to 7500 Mb/s.
2. For functional safety documentation to aid in ISO 26262 functional safety system design, contact Micron sales representative.

3. Based on automotive usage model. Contact Micron sales representative with questions.

Part Number Ordering Information (Die Rev D)

Figure 1: Part Number Chart

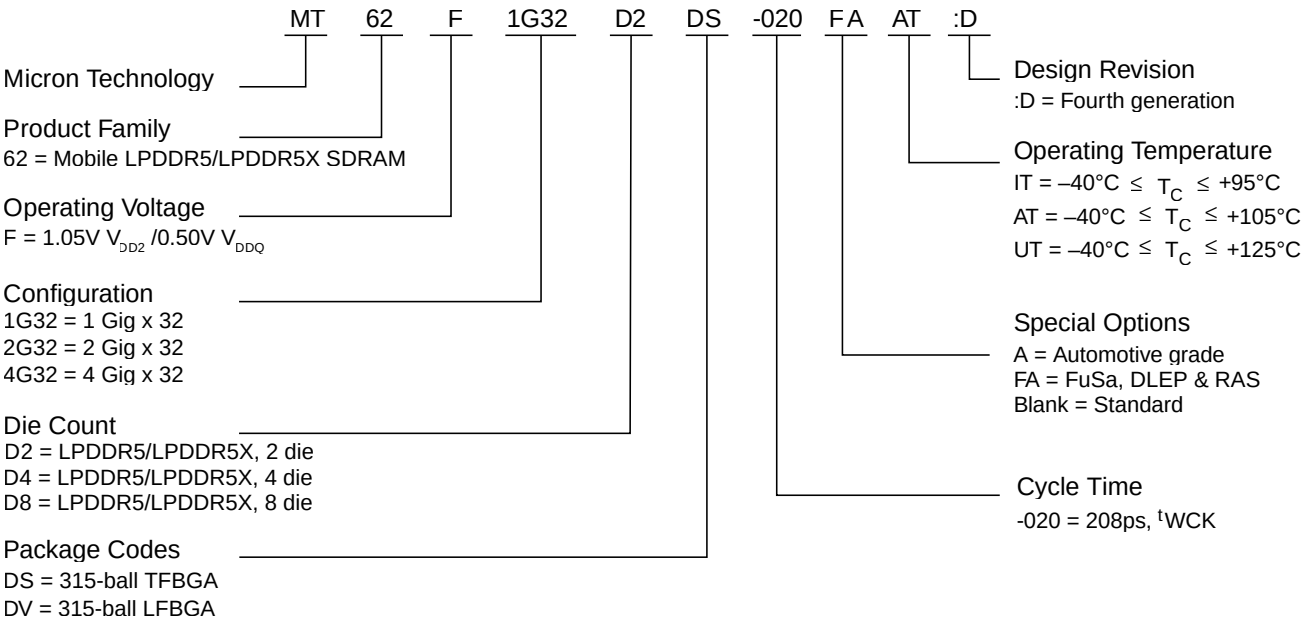

Table 1: Part Number List

Part Number	Total Density	Data Rate per Pin
MT62F1G32D2DS-020AIT:D	4GB (32Gb)	9600 Mb/s
MT62F1G32D2DS-020AAT:D		
MT62F1G32D2DS-020AUT:D		
MT62F1G32D2DS-020FAIT:D		
MT62F1G32D2DS-020FAAT:D		
MT62F1G32D2DS-020FAUT:D		
MT62F2G32D4DS-020AIT:D	8GB (64Gb)	
MT62F2G32D4DS-020AAT:D		
MT62F2G32D4DS-020AUT:D		
MT62F2G32D4DS-020FAIT:D		
MT62F2G32D4DS-020FAAT:D		
MT62F2G32D4DS-020FAUT:D		
MT62F4G32D8DV-020AIT:D	16GB (128Gb)	
MT62F4G32D8DV-020AAT:D		
MT62F4G32D8DV-020AUT:D		
MT62F4G32D8DV-020FAIT:D		
MT62F4G32D8DV-020FAAT:D		
MT62F4G32D8DV-020FAUT:D		

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

LPDDR5/LPDDR5X Data Sheet List

For general LPDDR5/LPDDR5X specifications, please refer to the data sheets below.

- General LPDDR5/LPDDR5X Specifications 1: Mode Registers
- General LPDDR5/LPDDR5X Specifications 2: AC/DC and Interface Specifications
- General LPDDR5/LPDDR5X Specifications 3: Features and Functionalities

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System Design and Implementation. This product has been developed for multiple applications based on assumed use cases and requirements (including assumed functional safety requirements and constraints). It is the customer’s sole responsibility to evaluate and confirm the validity and suitability of Micron’s product datasheet, assumed use cases and requirements, and evaluation results by verifying Micron’s assumptions against actual use cases and requirements in the intended end system and application. The customer must ensure compliance with all applicable requirements and standards (including industry, product, security, privacy, safety, etc.) to its system and applications. The customer must protect against death, personal injury, and severe property and environmental damage by ensuring that adequate design and redundancy (as needed), manufacturing and operating safeguards are included into customer's applications to ensure that failure of the Micron component will not result in such harms.

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General Notes

Throughout the data sheet, figures and text refer to DQs as DQ. DQ should be interpreted as any or all DQs collectively, unless specifically stated otherwise.

RDQS, CK, and WCK should be interpreted as RDQS_t, RDQS_c, CK_t, CK_c, and WCK_t, WCK_c respectively unless specifically stated otherwise. CA includes all CA pins used for a given density.

In timing diagrams, CMD is used as an indicator only. Actual signals occur on CA[6:0].

V_{REF} indicates $V_{REF(CA)}$, $V_{REF(CS)}$, and $V_{REF(DQ)}$.

Complete functionality is described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any content defined in this device ID specific data sheet document takes precedence over similar content defined in the general core LPDDR5/LPDDR5X SDRAM data sheet document(s).

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

Automotive Product Notes

The automotive LPDDR5/LPDDR5X DRAM Product family ("A" parts - see Part Number Ordering Information) are not allowed to be used in functional safety (ASIL/SIL rated) applications. Should customer or distributor purchase, use, or sell any Micron "A" component for any functional safety (ASIL/SIL rated) application, customer and distributor shall indemnify and hold harmless Micron and its subsidiaries, subcontractors, and affiliates and the directors, officers, and employees of each against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, or death arising in any way out of such functional safety (ASIL/SIL rated) application, whether or not Micron or its subsidiaries, subcontractors, or affiliates were negligent in the design, manufacture, or warning of the Micron product.

Functional Safety, DLEP & RAS Product Notes

This functional safety, DLEP and improved RAS LPDDR5/LPDDR5X DRAM product family ("F" parts - see Part Numbering Ordering Information). This product has been developed according to ISO 26262:2018 end IEC 61508:2010 requirements for use in functional safety systems targeting up to ASIL D / SIL 3 compliance.

The functional safety, DLEP and improved RAS LPDDR5/LPDDR5X DRAM product family contains several new features that operate within the JEDEC LPDDR5/LPDDR5X protocols (commands, timings, and so forth) and are made available to the integrator on “F” parts. The specification addendum governing these functional safety, DLEP and improved RAS features is available under NDA. This LPDDR5/LPDDR5X DRAM may operate as a standard JEDEC LPDDR5/LPDDR5X DRAM only, or as a standard JEDEC LPDDR5/LPDDR5X DRAM specifically designed with functional safety, DLEP and improved RAS features (only available on “F” parts).

Additional support is available to customers who need to integrate Micron’s products in their functional safety-related applications. This support may include Safety Analysis Report, reporting FMEDA results and metrics, Safety Manual and Pin FMEA Report, providing guidelines and instructions for using Micron products in safety-related applications.

Contact a Micron sales representative to initiate the process required to obtain the functional safety documentation.

Device Configuration (x32)

Table 2: Die Organization in the Package (x32)

Die Organization	1G32 (32 Gb/package)	2G32 (64 Gb/package)	4G32 (128 Gb/package)
Channel A	x16 mode × 1 die	–	–
Channel B	x16 mode × 1 die	–	–
Channel A, rank 0	–	x16 mode × 1 die	–
Channel B, rank 0	–	x16 mode × 1 die	–
Channel A, rank 1	–	x16 mode × 1 die	–
Channel B, rank 1	–	x16 mode × 1 die	–
Channel A, rank 0 DQ[7:0]	–	–	x8 mode × 1 die
Channel A, rank 1 DQ[7:0]	–	–	x8 mode × 1 die
Channel B, rank 0 DQ[7:0]	–	–	x8 mode × 1 die
Channel B, rank 1 DQ[7:0]	–	–	x8 mode × 1 die
Channel A, rank 0 DQ[15:8]	–	–	x8 mode × 1 die
Channel A, rank 1 DQ[15:8]	–	–	x8 mode × 1 die
Channel B, rank 0 DQ[15:8]	–	–	x8 mode × 1 die
Channel B, rank 1 DQ[15:8]	–	–	x8 mode × 1 die

Note: 1. Refer to the Package Block Diagram section in this data sheet.

Table 3: Die Addressing

Description	1G32 (32 Gb/package), 2G32 (64 Gb/package)		4G32 (128 Gb/package)	
Density per die	16Gb		16Gb	
Bits	17,179,869,184		17,179,869,184	
Bank mode	BG mode	16B mode	BG mode	16B mode
Configuration	64Mb × 16 DQ × 4 Banks × 4BG	64Mb × 16 DQ × 16 Banks	128Mb × 8 DQ × 4 Banks × 4BG	128Mb × 8 DQ × 16 Banks
Number of banks	4	16	4	16
Number of bank groups	4	1	4	1
Array prefetch bits	256	256	128	128
Rows per bank	65,536		131,072	
Columns	64		64	
Page size (bytes)	2048	2048	1024	1024
Native burst length	16	16	16	16
Number of I/Os	16		8	
Bank address	BA[1:0]	BA[3:0]	BA[1:0]	BA[3:0]
Bank group address	BG[1:0]	–	BG[1:0]	–
Row address	R[15:0]		R[16:0]	
Column address	C[5:0]		C[5:0]	
Burst address	B[3:0]	B[3:0]	B[3:0]	B[3:0]
Burst starting address boundary	128-bit		128-bit	

Note: 1. Refer to the SDRAM Addressing section in General LPDDR5/LPDDR5X Specifications 3.

Refresh Requirement Parameters

Table 4: Refresh Requirement Parameters

Parameter	Symbol	16Gb Die		Unit
		BG and 16B Mode		
		Enhanced DVFSC Disabled	Enhanced DVFSC Enabled	
REFRESH cycle time (all banks)	^{t}RFCab	280	300	ns
REFRESH cycle time (per bank)	^{t}RFCpb	140	150	ns
Per bank refresh to per bank refresh time (different bank)	^{t}PBR2PBR	90	100	ns
Per bank refresh to ACTIVATE command time (different bank)	^{t}PBR2ACT	7.5	7.5	ns

Note: 1. This table only describes refresh parameters that are density dependent. Refer to Refresh Requirement section in General LPDDR5/LPDDR5X Specifications 3 for all refresh parameters.

CS Rx Relaxed Specification

Table 5: CS Rx Specifications

Item	Symbol	Min/ Max	CK Frequency (MHz)															Unit	Note
			67[6]	133	200	266	344	400	467	533	600	688	750	800	937.5	1066.5	1200		
Rx mask																			
CS Rx mask height	vCSIVW	Max	155															mV	2, 7
CS Rx mask width at V_{REF} CS	^{t}CSIVW1	Max	0.3															^{t}CK(avg)	1
CS Rx mask width at vCSIVW	^{t}CSIVW2	Max	0.22															^{t}CK(avg)	1
Rx single pulse																			
CS Rx pulse amplitude	vCSIHL_AC	Min	240															mV	3
CS reference voltage	vREFCS		V_{DD2H}/3															mV	
CS Rx pulse width	^{t}CSIPW	Min	0.6															^{t}CK(avg)	
Power down																			
CS V_{IL} during power down/ deep sleep	V_{ILPD}	Max	130															mV	4
CS V_{IH} during power down/ deep sleep	V_{IHPD}	Min	550															mV	5
		Max	V_{DD2H} + 200																

Notes: 1. CS Rx mask voltage and timing parameters at the pin include temperature drift and voltage AC noise impact based on Z(f) specification at a fixed temperature on the package. The voltage supply noise must comply to the component min/max DC operating conditions.
2. CS single-pulse signal amplitude into the receiver must meet or exceed vCSIHL_AC at any point over the total UI; No timing requirement above a certain level. vCSIIHL_AC is the peak-to-peak voltage centered around V_{REF} CS such that vCSIHL_AC/2 min has to be met both above and below V_{REF} CS.
3. vCSIHL_AC does not have to be met when no transitions are occurring.
4. The input voltage presented to the CS Rx pin during power down should be 0V nominally to minimize leakage current.
5. V_{IHPD} is only applied for POWER DOWN and DEEP SLEEP EXIT operations.

6. The Rx voltage and absolute timing requirements apply for all CS operating frequencies at or below 67 for all speed bins. For example, ^{t}CSIVW1 (ns) = 4.477ns at or below 67 MHz CK frequency.
7. Measured at die pad.

DQ Rx Mask and Single Input Pulse Relaxed Specifications

Table 6: DQ Rx Mask and Single Input Pulse Specifications

Item	Symbol	Min/ Max	WCK Frequency (MHz)		Unit	Notes
			4266	4800		
DQ Rx mask height	vDIVW	Max	70		mV	1, 2, 3
DQ Rx mask width at $V_{REF(DQ)}$	^{t}DIVW1	Max	0.35		UI	1, 3
DQ Rx mask width at vDIVW	^{t}DIVW2	Max	0.18		UI	1, 3
DQ Rx pulse width at $V_{REF(DQ)}$	^{t}DIPW1	Min	0.51		UI	4
DQ Rx pulse reference	^{t}DIPW2	Min	0.26		UI	4
DQ Rx pulse width at $V_{REF(DQ)}$ ±vDIVW/2	^{t}DIHL	Min	0.24		UI	4
DQ Rx pulse amplitude from programmed $V_{REF(DQ)}$	vDIHP1	Min	70		mV	
	vDILP1	Max	–70		mV	
DQ Rx early pulse amplitude from programmed $V_{REF(DQ)}$	vDIHP2	Min	55		mV	
	vDILP2	Max	–55		mV	

Notes: 1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies greater than TBD MHz and maximum voltage of TBD mV peak-to-peak from DC-TBD MHz at a fixed temperature on the package. The voltage supply noise must comply with the component min/max DC operating conditions.
2. Rx mask voltage vDIVW must be centered around $V_{REF(DQ)}$.
3. Mask specifications (^{t}DIVW1, ^{t}DIVW2, and vDIVW) are the same regardless DFE enabled or disabled. DFE coefficient can be included as part of input waveform amplitude when DFE is enabled.
4. UI = ^{t}WCK/2, programed V_{REF}, is defined as a percentage of MR14/15 code x V_{DDQ}.

Figure 2: DQ Rx Mask Definition

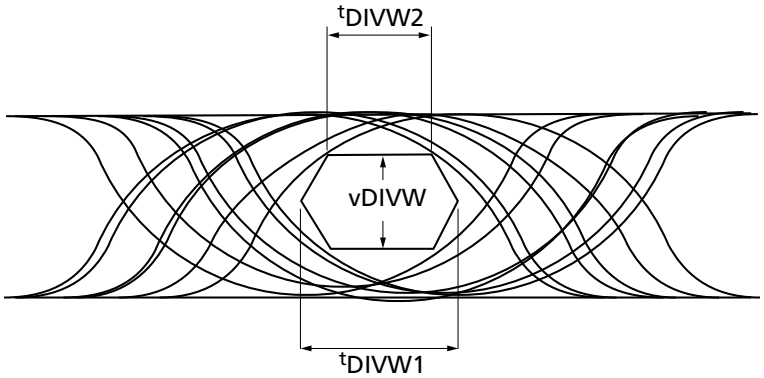
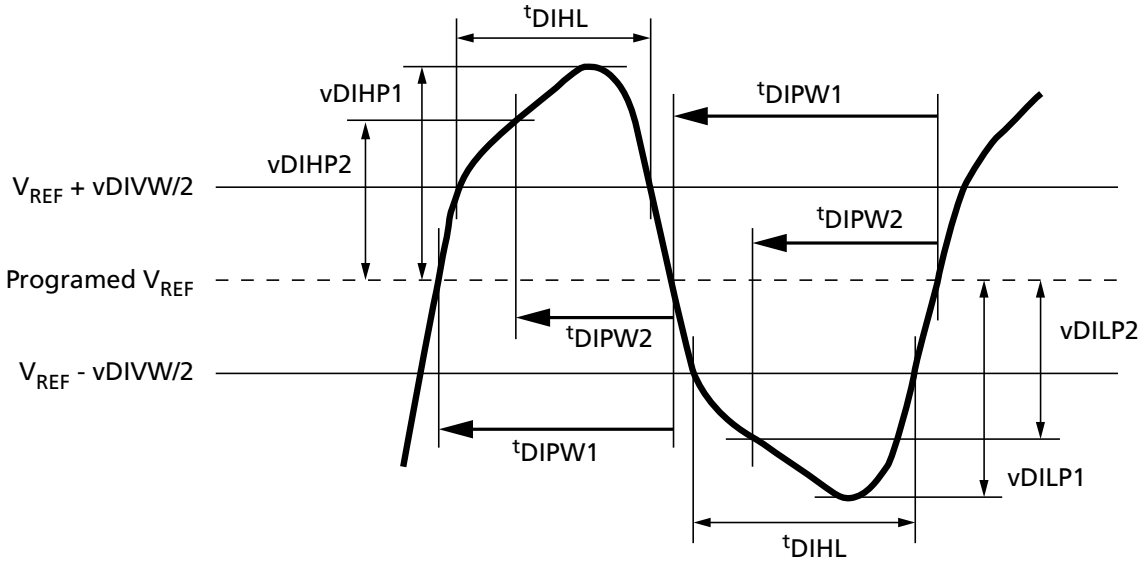


Figure 3: LPDDR5X DQ Single Pulse Definition



Note: 1. vDIHL_AC/2 = vDIHP1 = vDILP1. Programmed $V_{REF(DQ)}$ is defined as percentage of MR14/15 code * V_{DDQ}.

DQ Rx Mask and Single Input Pulse Relaxed Specifications 3200 MHz

Table 7: DQ, DMI, Parity and DBI Rx Mask and Single Input Pulse Specifications

Item	Symbol	Min/Max	WCK Frequency (MHz)	Unit	Notes
			3200		
DQ Rx mask height	vDIVW	Max	70	mV	1, 2, 3, 6
DQ Rx mask width at $V_{REF(DQ)}$	^{t}DIVW1	Max	0.35	UI	1, 3
DQ Rx mask width at vDIVW	^{t}DIVW2	Max	0.18	UI	1, 3
DQ Rx pulse width at $V_{REF(DQ)}$	^{t}DIPW1	Min	0.51	UI	4, 6
DQ Rx pulse reference	^{t}DIPW2	Min	0.26	UI	4
DQ Rx pulse width at $V_{REF(DQ)}$ ± vDIVW/2	^{t}DIHL	Min	0.24	UI	4, 6
DQ Rx pulse amplitude from programmed $V_{REF(DQ)}$	vDIHP1	Min	70	mV	
	vDILP1	Max	–70	mV	
DQ Rx early pulse amplitude from programmed $V_{REF(DQ)}$	vDIHP2	Min	55	mV	
	vDILP2	Max	–55	mV	
DQ V_{REF}	$V_{REF(DQ)}$	Min	75	mV	6
		Max	180	mV	6
DQ to DQ offset	^{t}DQ2DQ	Max	30	ps	5

Notes: 1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies greater than TBD MHz and maximum voltage of TBD mV peak-to-peak from DC-TBD MHz at a fixed temperature on the package. The voltage supply noise must comply with the component min/max DC operating conditions.
2. Rx mask voltage vDIVW must be centered around $V_{REF(DQ)}$.
3. Mask specifications (^{t}DIVW1, ^{t}DIVW2, and vDIVW) are the same regardless DFE enabled or disabled. DFE co-efficient can be included as part of input waveform amplitude when DFE is enabled.
4. UI = ^{t}WCK/2, programed V_{REF}, is defined as a percentage of MR14/15 code x V_{DDQ}.
5. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
6. When vDIVW is 70mV or more and less than 80mV.

16-Bank Extended Frequency

16-Bank Extended Frequency Description

Micron's LPDDR5 SDRAM device which are marked with 8533 Mb/s per-pin (-023) capability can support frequency set points using 2:1 WCK to CK ratio and above the 1600 MHz limit. Shown in the table below is specification requirements when considering 1867 MHz and 2133 MHz frequencies. This support is not available on 1-alpha process node and earlier Device ID's, this feature can expand capabilities of your system.

Table 8: 16-Bank Operation[1] @ 4.3 Gb/s

Parameter	3733 Mb/s per-pin	Comments	4267 Mb/s per-pin	Comments
RL Set 1/2/3	20/22/24	MR2[3:0] = 1100	23/25/26	MR2[3:0] = 1101
*n*RBTP	6		6	
WL Set A/B	11/19	MR1[7:4] = 1100	12/22	MR1[7:4] = 1101
*n*WR x16/x8	32/34	MR2[7:4] = 1100	37/39	MR2[7:4] = 1101
^{t}WCKPRE_static[2]	5	Follows 7500 data rate	6	Follows 8533 data rate
^{t}WCKPRE_WR_toggle	4	Follows 3200 datarate	4	Follows 3200 data rate
^{t}WCKPRE_RD_toggle	10	Follows 3200 datarate	10	Follows 3200 data rate
^{t}WCKENL_FS	2	Follows 3200 data rate	2	Follows 3200 data rate
^{t}WCKPRE_toggle_FS[3]	14	Minimum	16	Minimum
ODTLon	WL - 4	Follows 3200 data rate	WL - 4	Follows 3200 data rate
ODTLoff[4]	WL + 5 (BL16), WL + 9 (BL32)	Follows 3200	WL + 5 (BL16), WL + 9 (BL32)	Follows 3200 data rate
ODTLoff_RD_DQ	RL - 4	Follows 3200 data rate	RL - 4	Follows 3200 data rate
ODTLoff_RD_RDQS	RL - 6	MR10 OP[1, 5:4] = 000, 001, 010	RL - 6	MR10 OP[1, 5:4] = 000, 001, 010
	RL - 8	MR10 OP[1, 5:4] = 011, 1XX	RL - 8	MR10 OP[1, 5:4] = 011, 1XX
ODTLon_RD_DQ[5]	RL + 6 (BL16), RL + 10 (BL32)		RL + 6 (BL16), RL + 10 (BL32)	
ODTLon_RD_RDQS[6]	RL + 8 (BL16), RL + 12 (BL32)		RL + 8 (BL16), RL + 12 (BL32)	

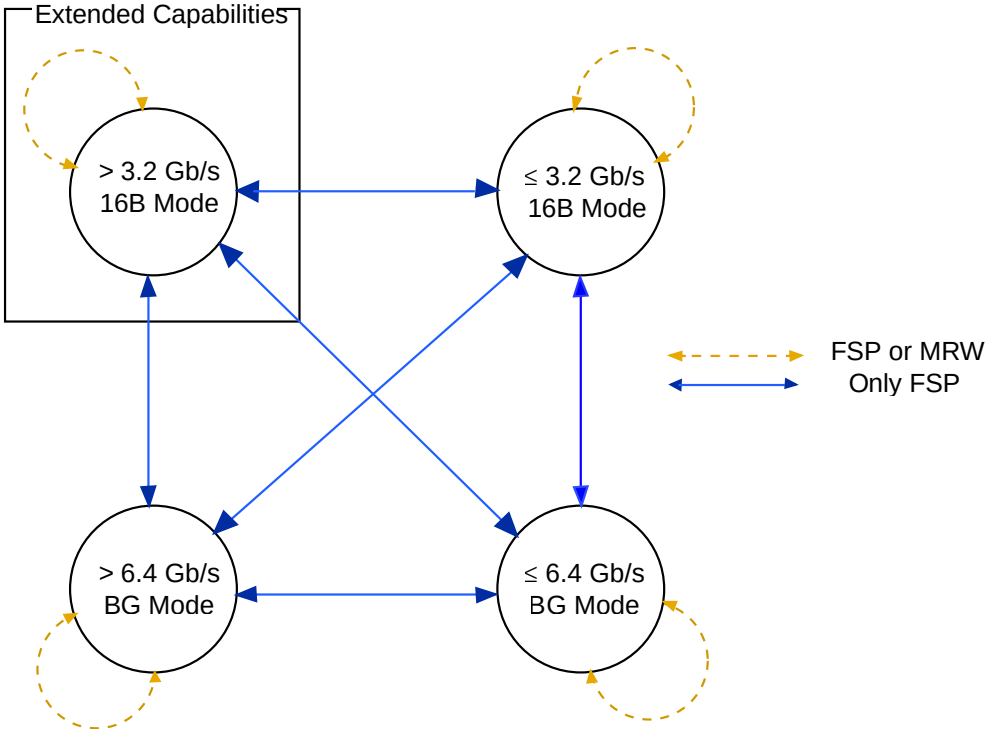
Notes: 1. Restricted to WCK:CK 2:1 ratio, WCK:CK 4:1 ratio not supported; Link ECC is disabled, and DVFSC/E-DVFSC is disabled.
2. Common for WR/RD/FS.
3. Minimum 1 + RL - (^{t}WCKENL_FS + ^{t}WCKPRE_Static) when CAS to RD is 1CK.
4. (WL + BL/n_min + RU(^{t}WCK2DQI(max)/^{t}CK)).
5. (RL + BL/n_min + RU(^{t}WCK2DQO(max)/^{t}CK)).
6. (RL + BL/n_min + RU(^{t}WCK2DQO(max)/^{t}CK)) + 2.
7. 8533 MT/s or higher data rated parts support 16-bank mode up to 4267 MT/s with restrictions, all other speed rated parts greater than 3200 MT/s per-pin and less than 8533 MT/s per-pin are restricted from the extended 16B mode capabilities. Refer to the above table for constraints for operating in 16-bank mode when data rate is greater than 3200 MT/s per-pin and equal to or less than 4267 MT/s per-pin.
8. When operating in the 16-bank mode, the FSP procedure must be used when setting the data rate above 3.2 Gb/s per-pin even when setting for the first time. For example, if the device is powered-up and initialized for 4266 Gb/s per-pin timing at the initial operation start, the FSP procedure must still be used. See Figure 4: 16B and BG Data Rate Change Flow Chart Showing Extended Capabilities on page 17 for details of FSP usage.

16B/BG Data Rate Change Diagram With FSP Requirements

The following flow chart diagram shows the needed 16-bank (16B) and bank group (BG) data rate change details and how the frequency set protocol (FSP) supports the extended frequency range.

The diagram below represents the device extended capabilities which are extended to 4267 Mb/s per-pin data rate in 16B mode.

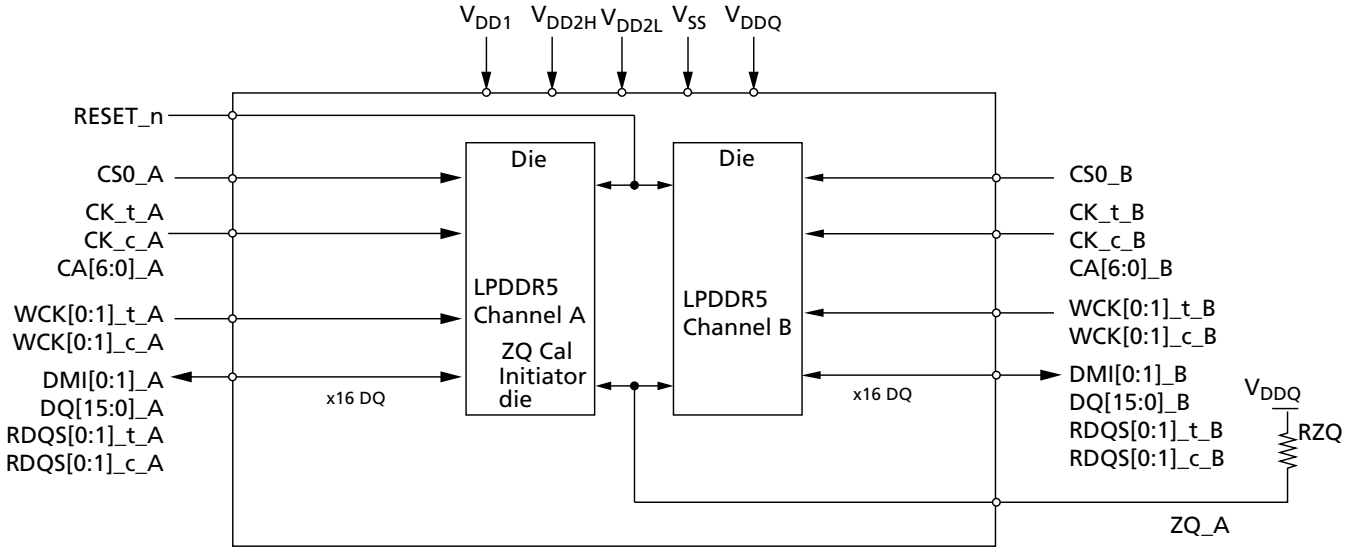
Figure 4: 16B and BG Data Rate Change Flow Chart Showing Extended Capabilities



Package Block Diagrams

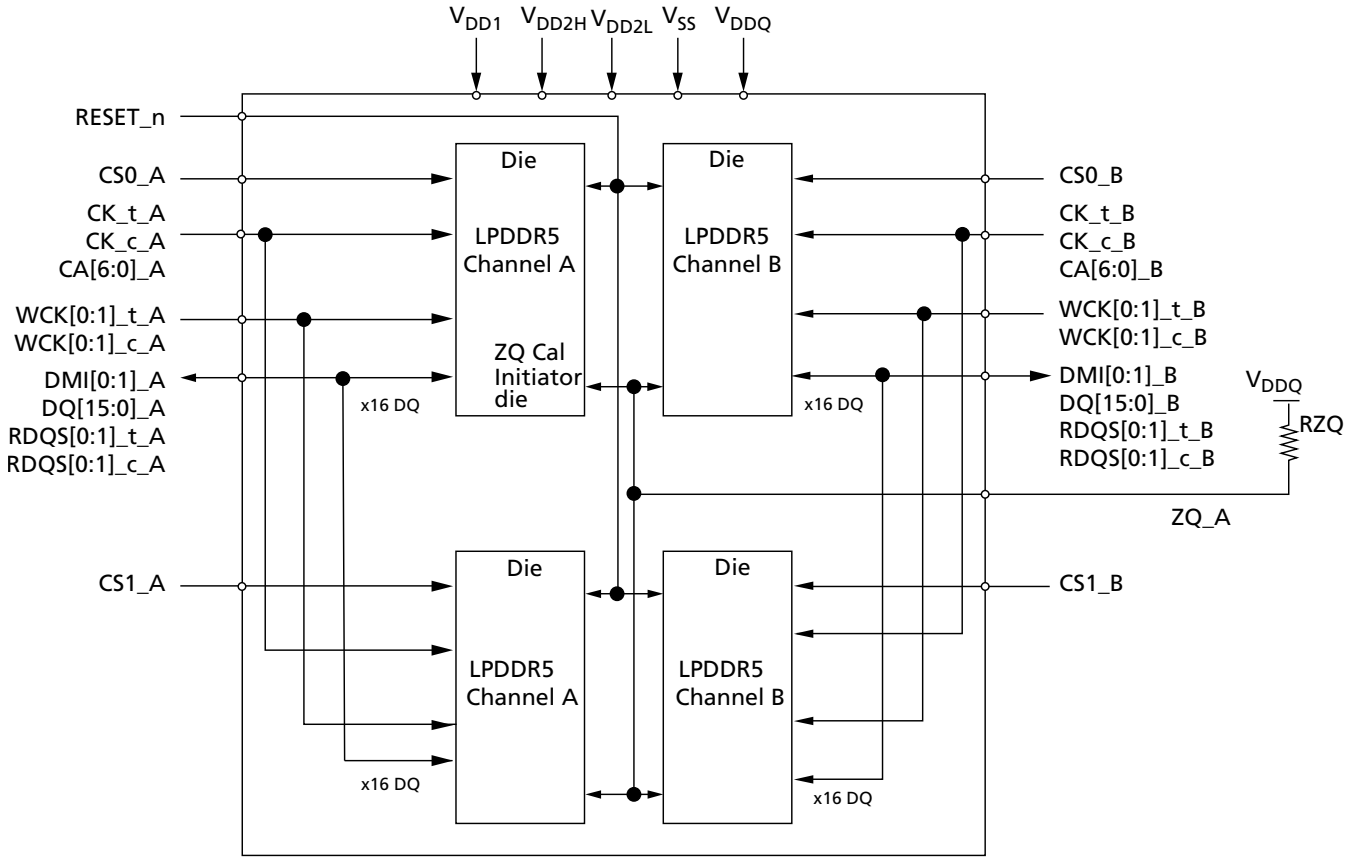
Dual Die, Dual Channel, Single Rank

Figure 5: Dual-Die, Dual-Channel, Single-Rank Package Block Diagram



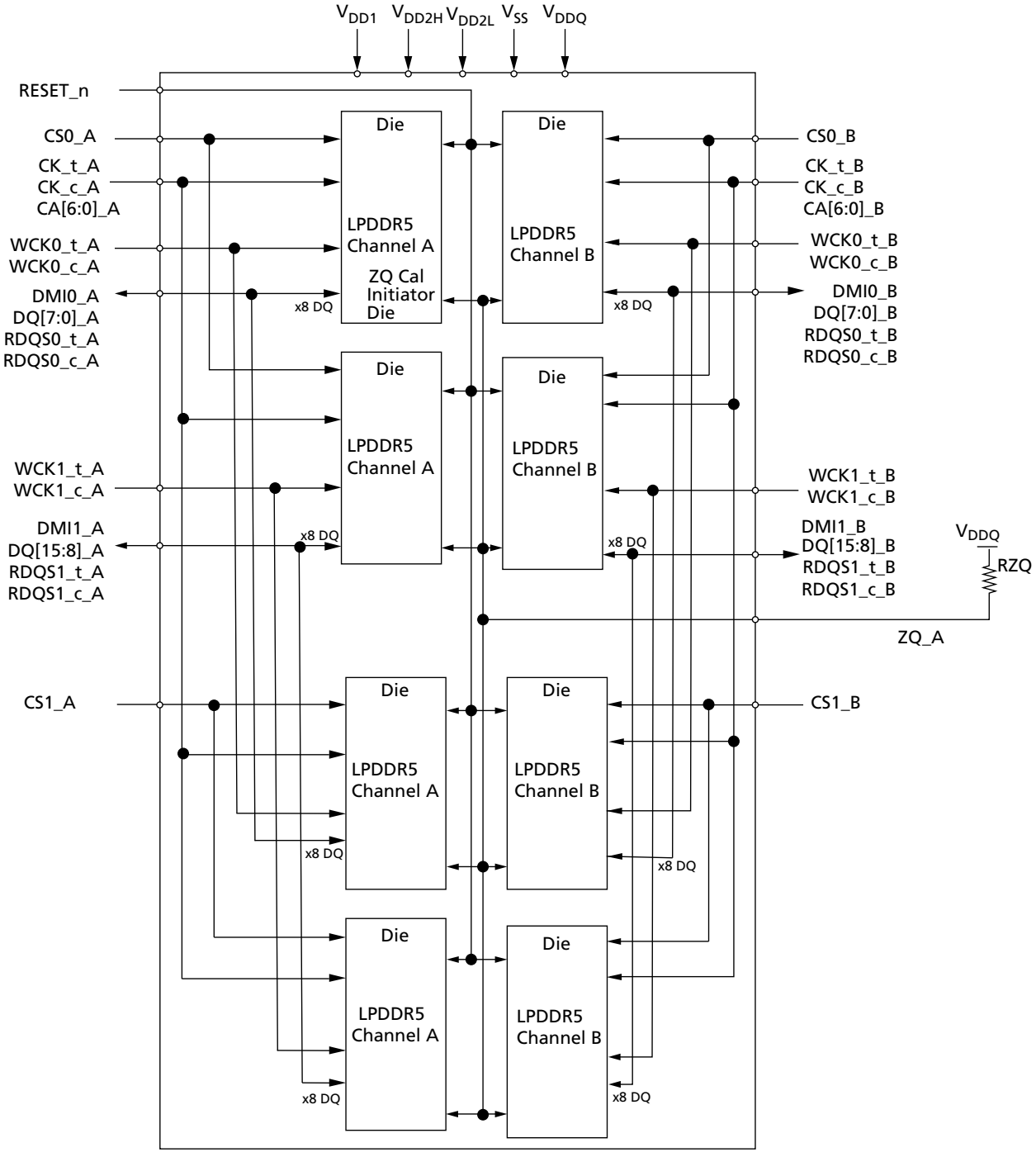
Quad Die, Dual Channel, Dual Rank

Figure 6: Quad-Die, Dual-Channel, Dual-Rank Package Block Diagram



Eight Die, Dual Channel, Dual Rank

Figure 7: Eight-Die, Dual-Channel, Dual-Rank Package Block Diagram



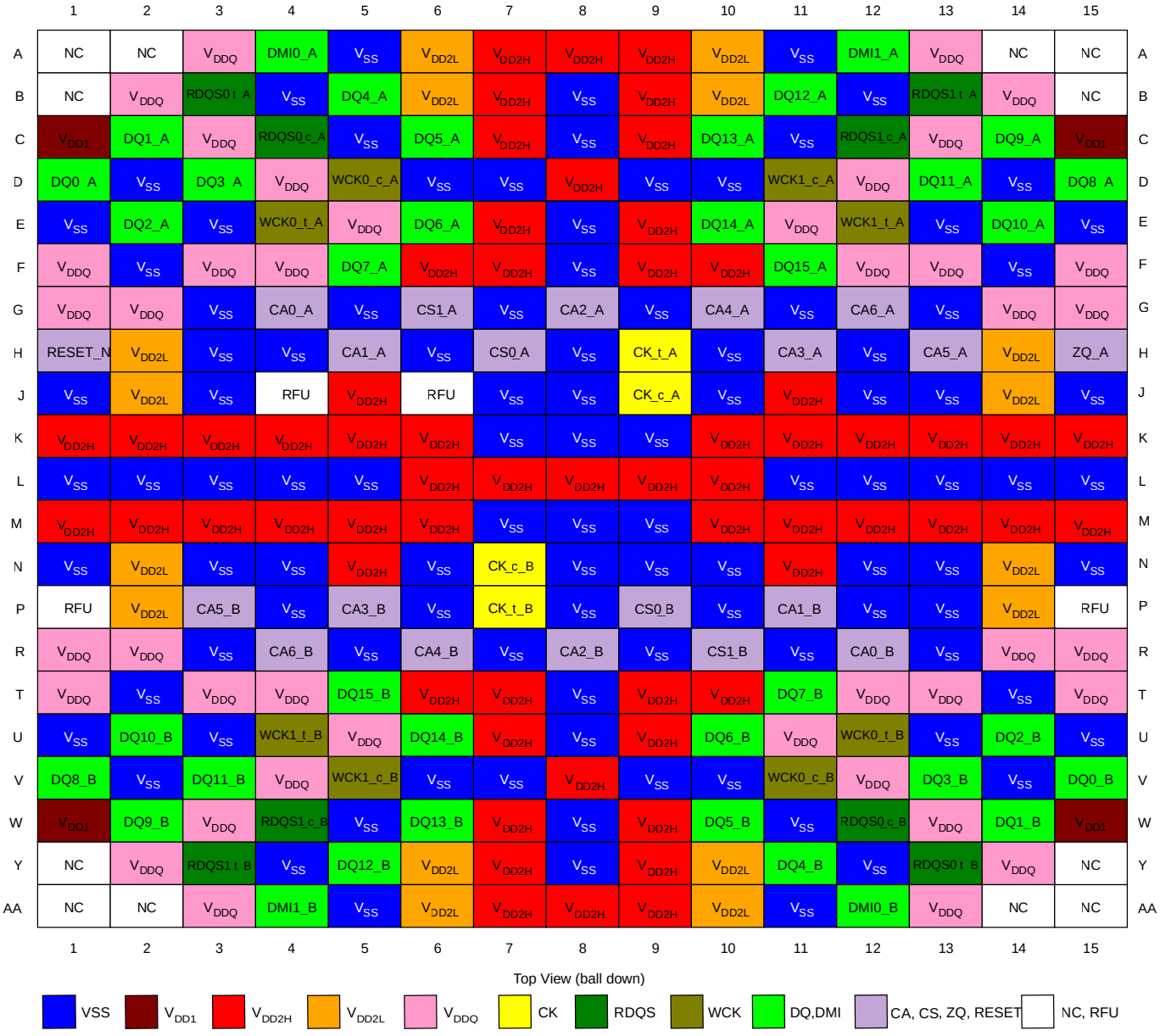
Ball Assignments and Descriptions

315b Dual Channel, 1 Rank, 2 Rank

Table 9: 315-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:B], CK_c_[A:B]	Input	**Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:B], CS1_[A:B]	Input	**Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:B] become NC pins in a single-rank package.
CA[6:0]_[A:B]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:B], WCK[1:0]_c_[A:B]	Input	**Data clock:** WCK_t and WCK_c are differential clock inputs used for write data capture and read data output.
DQ[15:0]_[A:B]	I/O	**Data input/output:** Bidirectional data bus.
RDQS[1:0]_t_[A:B], RDQS[1:0]_c_[A:B]	I/O Output	**Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:B]	I/O	**Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V_{DDQ} through a 240 ohm ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2H}, V_{DD2L}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	**No connect:** Not internally connected.
RFU	–	**Reserved Future Use:** Not internally connected.

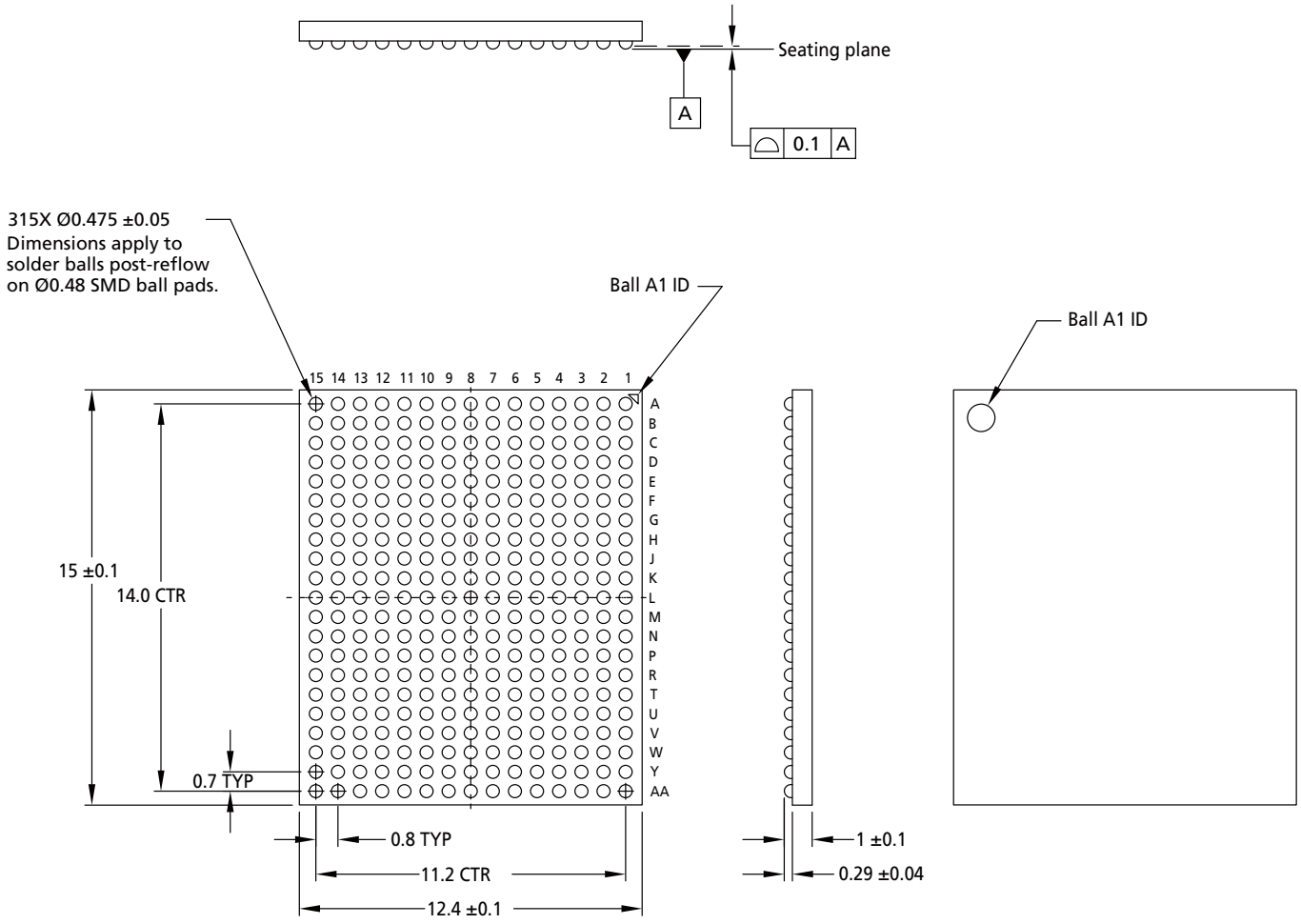
Figure 8: 315-Ball Dual-Channel Discrete FBGA



Package Dimensions

315-Ball Package (Package Code: DS)

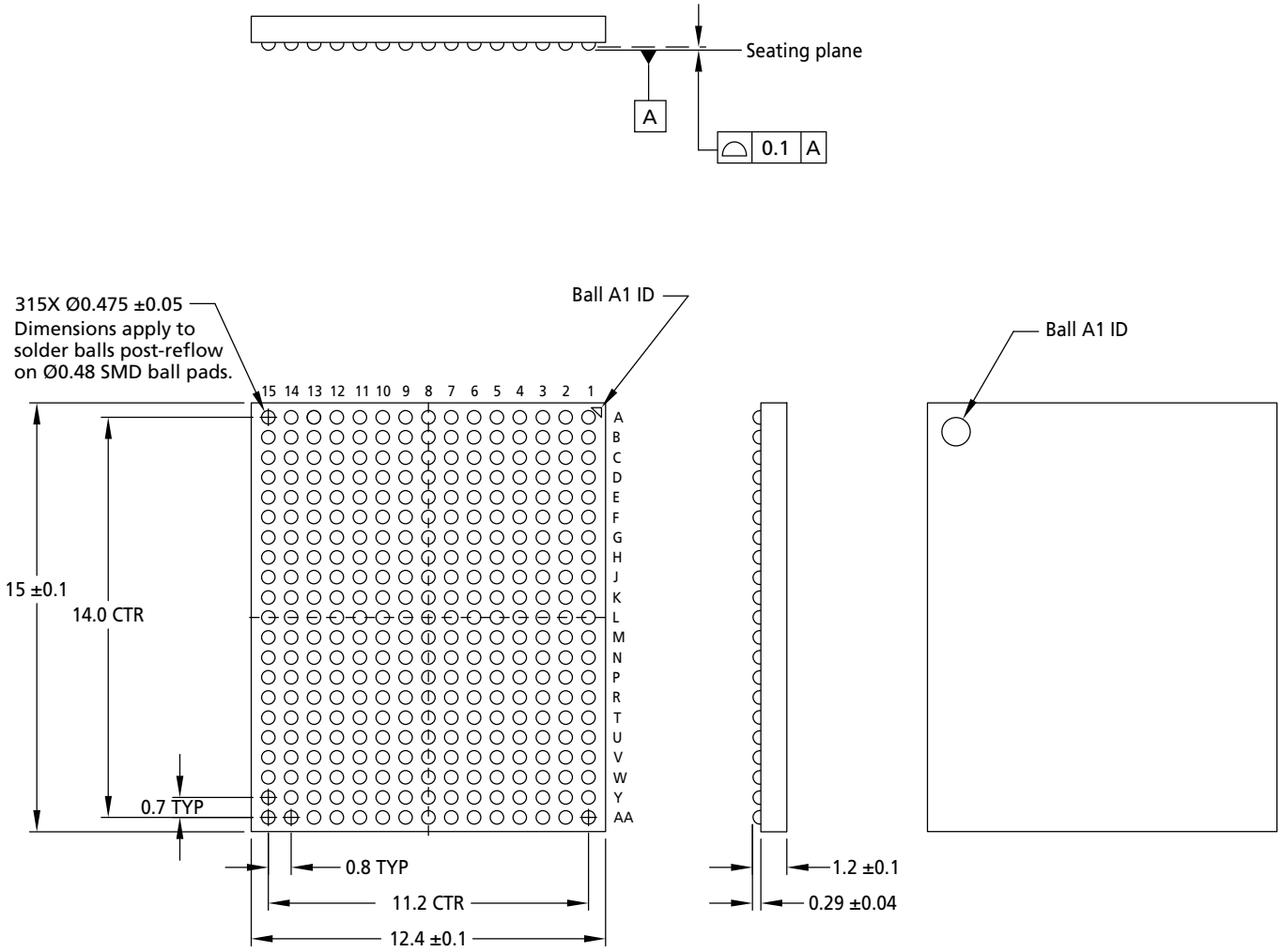
Figure 9: 315-Ball TFBGA – 12.4mm (TYP) × 15.0mm (TYP) × 1.1mm (MAX) (Package Code: DS)



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni).

315-Ball Package (Package Code: DV)

Figure 10: 315-Ball LFBGA – 12.4mm (TYP) × 15.0mm (TYP) × 1.3mm (MAX) (Package Code: DV)



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni).

Package Thermal Impedance

Table 10: Package Thermal Impedance Characteristics

Die Revision	Package	Parameter	Symbol	Value	Unit
Rev D	315-ball, DDP, package code DS	Junction-to-case (TOP)	Θ_{JC}	3.3	°C/W
		Junction-to-board	Θ_{JB}	10.1	°C/W
	315-ball, QDP, package code DS	Junction-to-case (TOP)	Θ_{JC}	2.5	°C/W
		Junction-to-board	Θ_{JB}	8.3	°C/W
	315-ball, 8DP, package code DV	Junction-to-case (TOP)	Θ_{JC}	2.4	°C/W
		Junction-to-board	Θ_{JB}	10.0	°C/W

Product-Specific Mode Register Definition

Table 11: Mode Register Contents

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0	**Per-pin DFE**	**Pre Emphasis**	**Unified NT ODT behavior mode**	**DMI output behavior mode**	**Optimized refresh mode**	**Enhanced WCK always-on mode**	**Latency mode**	**NT ODT timing mode**
	OP[0] = 1b: Device supports different NT ODT latency for DQ and RDQS							
	OP[1] = 0b: Device supports x16 mode latency for 1G32, 2G32 OP[1] = 1b: Device supports x8 mode latency for 4G32							
	OP[2] = 1b: Device supports enhanced WCK always-on mode							
	OP[3] = 1b: Device supports optimized refresh mode							
	OP[4] = 1b: Device supports both DMI behavior mode 1 and 2 and mode selection							
	OP[5] = 1b: The NT ODT behavior follows the unified NT ODT behavior							
	OP[6] = 1b: Device supports Pre Emphasis mode							
	OP[7] = 1b: Device supports Per Pin DFE							
MR1						**DRFM support[3]**	**ARFM support[3]**	**CS ODT OP support**
	OP[0] = 1b: Device supports CS ODT behavior OP							
	OP[1] = 1b: Device supports ARFM							
	OP[2] = 1b: Device supports DRFM							
MR3				**BK/BG ORG**				
	OP[4:3] = 00b: BG, 10b: 16B Mode support							
MR4				**Refresh Multiplier** (Note 6, 7)				
	OP[4:0]: Refer to General LPDDR5/LPDDR5X Specification 1 for mode register definitions.							
MR5	**Manufacturer ID**							
	1111 1111b: Micron							
MR6	**Revision ID1**							
	0000 1001b							
MR8	**I/O width**		**Density**				**Device Type[5]**	
	OP[7:6] = 00b: x16 for 1G32, 2G32 OP[7:6] = 01b: x8 for 4G32		OP[5:2] = 0110b: 16Gb				OP[1:0] = 10b: LPDDR5X SDRAM (up to 9600 Mb/s)	
MR19			**WCK2DQ OSC FM**					
	OP[5] = 1b: WCK2DQ OSC FM supported							
MR21	**WXS**				**ODTD-CSFS**	**WXFS**	**RDCFS**	**WDCFS**
	OP[0] = 1b: WRITE DATA COPY function supported							
	OP[1] = 1b: READ DATA COPY function supported							
	OP[2] = 1b: WRITE X function supported							
	OP[3] = 1b: Device ODTD-CS is supported							
	OP[7] = 1b: Data to be written can be selected with 0 and 1							

Table 11: Mode Register Contents (Continued)

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR24	**DFES**				**Read DCA**			
	OP[3] = 1b: Device supports Read DCA							
	OP[7] = 1b: Device supports DFE (See Note 4)							
MR26		**RDQSTFS**						
	OP[6] = 1b: Read/write-based RDQS_t TRAINING function supported							
MR27	**RAAMULT**		**RAAIMT**					**RFM**
	OP[0] = 1b: RFM is required							
	OP[5:1] = 01000b: 64							
	OP[7:6] = 01b: 4X							
MR41					**E-DVFSC ODT**	**DVFSC/ E-DVFSC Support**		
	OP[2:1] = 01b: Only Enhanced DVFSC Mode supported							
	OP[3] = 0b: Enhanced DVFSC ODT option not supported							
MR43		**SBEC rule**						
	OP[6] = 1b: Simultaneous SBE on each DQ byte and DMI are independently counted							
MR57					**RFMSB**		**RAADEC**	
	OP[1:0] = 10b: 2 × RAAIMT							
	OP[3:2] = 01b: Single Bank Mode supported							
MR75								**BRCS**
	OP[0] = 1b: BRC is supported							
MR63 - MR74, MR76 - MR164	Reserved MR bits MR63 through MR74 and MR76 through MR164 are RFU by JEDEC standard and should not be accessed by user.							

Notes: 1. The contents of mode registers described here reflect information specific to each die in these packages.
2. Refer to General LPDDR5/LPDDR5X Specification 1 for mode registers not described here.
3. Refer to General LPDDR5/LPDDR5X Specification 3 for feature description not described here.
4. Device supports 7-step DFE.
5. Device type only supports bank group and 16B modes.
6. MR4 OP[4:0] output from each die in a defined package shall be used to determine the required package level refresh rate. Any other method used to determine a valid refresh rate, places ownership and responsibility of the correct refresh rate on the system developer or end user. T_{OPER} (case surface temperature) shall be used to determine whether operating temperature requirements are being met. Any other method used to determine operating temperature, places ownership and responsibility of the correct operating temperature on the system developer or end user.
7. The intent of a MR4 OP[4:0] output of <01111> is to not to support a refresh rate of 0.125xd; rather a method to inform the host the die temperature is most likely being operated beyond its supported upper maximum limit and the host should immediately place the DRAM in to a refresh only state at 0.125xd refresh rate until the MR4 readout of <01111> no longer exists. No other operation other than refresh should be conducted.

I_{DD} Parameters

Refer to I_{DD} Specification Parameters and Test Conditions section in General LPDDR5/LPDDR5X Specifications 2 for detailed conditions.

Table 12: I_{DD} Parameters at 9600 Mb/s – Single Die

Symbol	Supply	x8 Mode			x16 Mode			Unit	Note
		UT	AT	IT	UT	AT	IT		
I_{DD01}	V_{DD1}	4.40	4.10	4.10	4.40	4.10	4.10	mA	
I_{DD02H}	V_{DD2H}	75.00	59.00	59.00	75.00	59.00	59.00		
I_{DD02L}	V_{DD2L}	0.20	0.20	0.20	0.20	0.20	0.20		
I_{DD0Q}	V_{DDQ}	0.60	0.60	0.60	0.60	0.60	0.60		
I_{DD2P1}	V_{DD1}	2.30	1.60	1.60	2.30	1.60	1.60	mA	
I_{DD2P2H}	V_{DD2H}	7.00	4.80	4.80	7.00	4.80	4.80		
I_{DD2P2L}	V_{DD2L}	0.20	0.20	0.20	0.20	0.20	0.20		
I_{DD2PQ}	V_{DDQ}	0.60	0.60	0.60	0.60	0.60	0.60		
I_{DD2PS1}	V_{DD1}	2.30	1.60	1.60	2.30	1.60	1.60	mA	
$I_{DD2PS2H}$	V_{DD2H}	7.00	4.80	4.80	7.00	4.80	4.80		
$I_{DD2PS2L}$	V_{DD2L}	0.20	0.20	0.20	0.20	0.20	0.20		
I_{DD2PSQ}	V_{DDQ}	0.60	0.60	0.60	0.60	0.60	0.60		
I_{DD2N1}	V_{DD1}	2.30	1.60	1.60	2.30	1.60	1.60	mA	
I_{DD2N2H}	V_{DD2H}	51.50	42.50	42.50	52.00	43.00	43.00		
I_{DD2N2L}	V_{DD2L}	0.20	0.20	0.20	0.20	0.20	0.20		
I_{DD2NQ}	V_{DDQ}	0.60	0.60	0.60	0.60	0.60	0.60		
I_{DD2NS1}	V_{DD1}	2.30	1.60	1.60	2.30	1.60	1.60	mA	
$I_{DD2NS2H}$	V_{DD2H}	51.50	42.50	42.50	52.00	43.00	43.00		
$I_{DD2NS2L}$	V_{DD2L}	0.20	0.20	0.20	0.20	0.20	0.20		
I_{DD2NSQ}	V_{DDQ}	0.60	0.60	0.60	0.60	0.60	0.60		
I_{DD3P1}	V_{DD1}	2.90	2.20	2.20	2.90	2.20	2.20	mA	
I_{DD3P2H}	V_{DD2H}	33.00	18.00	18.00	33.00	18.00	18.00		
I_{DD3P2L}	V_{DD2L}	0.20	0.20	0.20	0.20	0.20	0.20		
I_{DD3PQ}	V_{DDQ}	0.60	0.60	0.60	0.60	0.60	0.60		
I_{DD3PS1}	V_{DD1}	2.90	2.20	2.20	2.90	2.20	2.20	mA	
$I_{DD3PS2H}$	V_{DD2H}	33.00	18.00	18.00	33.00	18.00	18.00		
$I_{DD3PS2L}$	V_{DD2L}	0.20	0.20	0.20	0.20	0.20	0.20		
I_{DD3PSQ}	V_{DDQ}	0.60	0.60	0.60	0.60	0.60	0.60		
I_{DD3N1}	V_{DD1}	4.00	3.10	3.10	4.00	3.10	3.10	mA	
I_{DD3N2H}	V_{DD2H}	74.00	50.50	50.50	75.00	51.00	51.00		
I_{DD3N2L}	V_{DD2L}	0.20	0.20	0.20	0.20	0.20	0.20		
I_{DD3NQ}	V_{DDQ}	0.60	0.60	0.60	0.60	0.60	0.60		

Table 12: I_{DD} Parameters at 9600 Mb/s – Single Die (Continued)

Symbol	Supply	x8 Mode			x16 Mode			Unit	Note
		UT	AT	IT	UT	AT	IT		
I_{DD4R1}	V_{DD1}	22.00	21.00	21.00	24.00	23.00	23.00	mA	3, 4, 6
I_{DD4R2H}	V_{DD2H}	300.00	260.00	260.00	420.00	380.00	380.00		
I_{DD4R2L}	V_{DD2L}	0.20	0.20	0.20	0.20	0.20	0.20		
I_{DD4RQ}	V_{DDQ}	69.00	69.00	69.00	138.00	138.00	138.00		
I_{DD4W1}	V_{DD1}	20.00	19.00	19.00	22.00	21.00	21.00	mA	3, 6
I_{DD4W2H}	V_{DD2H}	235.00	205.00	205.00	325.00	295.00	295.00		
I_{DD4W2L}	V_{DD2L}	0.20	0.20	0.20	0.20	0.20	0.20		
I_{DD4WQ}	V_{DDQ}	0.60	0.60	0.60	0.60	0.60	0.60		
I_{DD51}	V_{DD1}	22.00	20.00	20.00	22.00	20.00	20.00	mA	
I_{DD52H}	V_{DD2H}	250.00	200.00	200.00	250.00	200.00	200.00		
I_{DD52L}	V_{DD2L}	0.20	0.20	0.20	0.20	0.20	0.20		
I_{DD5Q}	V_{DDQ}	0.60	0.60	0.60	0.60	0.60	0.60		
I_{DD5AB1}	V_{DD1}	3.60	3.30	3.30	3.60	3.30	3.30	mA	
$I_{DD5AB2H}$	V_{DD2H}	75.00	49.00	49.00	75.00	50.00	50.00		
$I_{DD5AB2L}$	V_{DD2L}	0.20	0.20	0.20	0.20	0.20	0.20		
I_{DD5ABQ}	V_{DDQ}	0.60	0.60	0.60	0.60	0.60	0.60		
I_{DD5PB1}	V_{DD1}	3.60	3.30	3.30	3.60	3.30	3.30	mA	
$I_{DD5PB2H}$	V_{DD2H}	75.00	49.00	49.00	75.00	50.00	50.00		
$I_{DD5PB2L}$	V_{DD2L}	0.20	0.20	0.20	0.20	0.20	0.20		
I_{DD5PBQ}	V_{DDQ}	0.60	0.60	0.60	0.60	0.60	0.60		

Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BG mode enabled. Enhanced DVFSC and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V (DVFSQ disabled)/0.27-0.37V (DVFSQ enabled)
6. I_{DD4R2} and I_{DD4W2} have implemented a more stringent pattern than required by JEDEC and therefore these I_{DD} values are slightly higher than if the JEDEC pattern was used.
7. Notes 1, 2, and 5 apply to entire table.

Table 13: I_{DD} Parameters at 3200 Mb/s – With Enhanced DVFSC Enabled – Single Die

Symbol	Supply	x8 Mode			x16 Mode			Unit	Note
		UT	AT	IT	UT	AT	IT		
$I_{DD4R-DVFSC1}$	V_{DD1}	14.00	13.00	13.00	15.00	14.00	14.00	mA	3, 4, 6
$I_{DD4R-DVFSC2H}$	V_{DD2H}	41.00	31.00	31.00	42.00	32.00	32.00		
$I_{DD4R-DVFSC2L}$	V_{DD2L}	95.00	90.00	90.00	125.00	120.00	120.00		
$I_{DD4R-DVFSCQ}$	V_{DDQ}	44.00	44.00	44.00	88.00	88.00	88.00		
$I_{DD4W-DVFSC1}$	V_{DD1}	13.00	12.00	12.00	14.00	13.00	13.00	mA	3, 6
$I_{DD4W-DVFSC2H}$	V_{DD2H}	39.00	31.00	31.00	40.00	32.00	32.00		
$I_{DD4W-DVFSC2L}$	V_{DD2L}	85.00	80.00	80.00	115.00	110.00	110.00		
$I_{DD4W-DVFSCQ}$	V_{DDQ}	0.60	0.60	0.60	0.60	0.60	0.60		
I_{DD5ED1}	V_{DD1}	22.00	20.00	20.00	22.00	20.00	20.00	mA	
$I_{DD5ED2H}$	V_{DD2H}	195.00	180.00	180.00	195.00	180.00	180.00		
$I_{DD5ED2L}$	V_{DD2L}	25.00	23.00	23.00	25.00	23.00	23.00		
I_{DD5EDQ}	V_{DDQ}	0.60	0.60	0.60	0.60	0.60	0.60		
$I_{DD5ABED1}$	V_{DD1}	3.60	3.30	3.30	3.60	3.30	3.30	mA	
$I_{DD5ABED2H}$	V_{DD2H}	39.00	27.00	27.00	37.00	27.00	27.00		
$I_{DD5ABED2L}$	V_{DD2L}	23.50	21.50	21.50	24.00	22.00	22.00		
$I_{DD5ABEDQ}$	V_{DDQ}	0.60	0.60	0.60	0.60	0.60	0.60		
$I_{DD5PBED1}$	V_{DD1}	3.60	3.30	3.30	3.60	3.30	3.30	mA	
$I_{DD5PBED2H}$	V_{DD2H}	39.00	27.00	27.00	37.00	27.00	27.00		
$I_{DD5PBED2L}$	V_{DD2L}	23.50	21.50	21.50	24.00	22.00	22.00		
$I_{DD5PBEDQ}$	V_{DDQ}	0.60	0.60	0.60	0.60	0.60	0.60		

Notes:
1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. Enhanced DVFSC enabled, DVFSQ enabled, 3200 Mb/s, 16B mode
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V (DVFSQ disabled)/0.27-0.37V (DVFSQ enabled)
6. I_{DD4R2} and I_{DD4W2} have implemented a more stringent pattern than required by JEDEC and therefore these I_{DD} values are slightly higher than if the JEDEC pattern was used.
7. Notes 1, 2, and 5 apply to entire table.

Table 14: Full-Array Power-Down Self Refresh Current – Single Die

Temperature	Symbol	Supply	Value	Unit	Notes
25°C	I_{DD61}	V_{DD1}	0.20	mA	4
	I_{DD62H}	V_{DD2H}	0.5		
	I_{DD62L}	V_{DD2L}	0		
	I_{DD6Q}	V_{DDQ}	0.03		
	I_{DD6DS1}	V_{DD1}	0.19	mA	4
	$I_{DD6DS2H}$	V_{DD2H}	0.49		
	$I_{DD6DS2L}$	V_{DD2L}	0		
	I_{DD6DSQ}	V_{DDQ}	0.01		
45°C	I_{DD61}	V_{DD1}	0.27	mA	4
	I_{DD62H}	V_{DD2H}	0.92		
	I_{DD62L}	V_{DD2L}	0		
	I_{DD6Q}	V_{DDQ}	0.03		
	I_{DD6DS1}	V_{DD1}	0.25	mA	4
	$I_{DD6DS2H}$	V_{DD2H}	0.92		
	$I_{DD6DS2L}$	V_{DD2L}	0		
	I_{DD6DSQ}	V_{DDQ}	0.01		
65°C	I_{DD61}	V_{DD1}	0.48	mA	4
	I_{DD62H}	V_{DD2H}	2.30		
	I_{DD62L}	V_{DD2L}	0		
	I_{DD6Q}	V_{DDQ}	0.03		
	I_{DD6DS1}	V_{DD1}	0.46	mA	4
	$I_{DD6DS2H}$	V_{DD2H}	2.30		
	$I_{DD6DS2L}$	V_{DD2L}	0		
	I_{DD6DSQ}	V_{DDQ}	0.01		
85°C	I_{DD61}	V_{DD1}	4.00	mA	4
	I_{DD62H}	V_{DD2H}	23.00		
	I_{DD62L}	V_{DD2L}	0.20		
	I_{DD6Q}	V_{DDQ}	0.60		
	I_{DD6DS1}	V_{DD1}	4.00	mA	4
	$I_{DD6DS2H}$	V_{DD2H}	23.00		
	$I_{DD6DS2L}$	V_{DD2L}	0.20		
	I_{DD6DSQ}	V_{DDQ}	0.60		

Notes: 1. I_{DD6} 25/45/65°C is the typical value in the distribution with nominal V_{DD} and a reference-only value. I_{DD6} 85°C is the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. DVFSC and DVFSQ disabled.
3. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V
4. While entering and exiting Self-Refresh modes, all defined/used supply rails (V_{DD1}, V_{DD2H}, V_{DD2L}, V_{DDQ}) are required to be at valid levels. After the Self-Refresh with Power down mode entrance commands are completed and ^{t}ESPD timing requirement has been satisfied, the V_{DDQ} power rail may be turned off by the controller.

Revision History

Rev. G – 06/2026

- Updated Part Number Ordering Information

Rev. F – 03/2026

- Updated legal status to Production

Rev. E – 03/2026

- Updated Features Page
- Updated Functional Safety Page
- Updated Automotive Product Notes Page

Rev. D – 01/2026

- Updated CS Rx and DQ Rx Mask for 9600 Mbps
- Updated Package Thermal Impedance Characteristics table for 8DP
- Specified I_{DD} values for UT
- Added I_{DD} 6 values for 45/65C

Rev. C – 12/2025

- Removed 8533 and 7500 Mb/s part numbers and their related information
- Updated Package Thermal Impedance Characteristics table
- Specified I_{DD} values for IT and AT

Rev. B – 09/2025

- Updated legal status to Preliminary
- Added Functional Safety, DLEP & RAS Notes
- Updated Package Thermal Impedance Characteristics table

Rev. A – 06/2024

- Initial Advanced data sheet release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.