EVAL-LT3099

Evaluates: LT3099

General Description

The LT3099 evaluation board (EVAL-LT3099-AZ) features the LT®3099, a -20V, 1A, ultralow noise, ultrahigh power-supply rejection ratio (PSRR) negative linear regulator that incorporates voltage input-to-output control (VIOC) tracking. VIOC allows control of the upstream switching converter to maintain a constant voltage across the LT3099 and, therefore, minimizes power dissipation and maintains PSRR.

The EVAL-LT3099-AZ operates over an input voltage range of -3.8V to -20V. The LT3099 delivers a maximum output current of 1A. In addition to featuring ultralow noise and ultrahigh PSRR, the regulator offers programmable power-good functionality and a programmable current limit. The Enable function (EN/UV pin) is bidirectional and can be controlled with either a positive or a negative voltage.

Built-in protection includes an internal current limit with foldback and a thermal limit with hysteresis.

For full details on the LT3099, refer to the LT3099 datasheet. It is recommended to read the LT3099 data sheet and this user guide prior to using or making any hardware changes to the EVAL-LT3099-AZ evaluation board.

The LT3099 of the EVAL-LT3099-AZ features a 14-lead, 3mm x 4mm, plastic dual-flat no-leads (DFN) package with an exposed pad on the bottom side of the IC. A proper board layout is essential for maximum thermal performance.

Design files for this circuit board are available at www.analog.com.

Features and Benefits

- Input Voltage Range: -3.8V to -20V
- Resistor Programmed -3.32V Output Voltage
- Maximum Output Current: 1A
- BNC Connectors for Noise and PSRR Measurement
- Resistor-Programmed Power-Good and Fast Start-Up
- Resistor Programmable Current Limit and UVLO
- VIOC to manage Power Dissipation and PSRR
- Thermally Enhanced, 14-Lead, 3mm x 4mm, DFN Package

***Ordering Information* appears at end of this datasheet**

Quick Start

Required Equipment

- A DC power supply
- Multimeters for voltage and current measurements
- Electronic or resistive loads

Procedure

The EVAL-LT3099-AZ is easy to set up to evaluate the performance of the LT3099. See *Figure 1* for the proper measurement equipment setup, and use the following steps:

1. Connect the load between the V_{OUT} and GND terminals. Observe the correct polarity for the load.
2. With the power off, connect the input power supply to the V_{IN} and GND terminals. Confirm that GND is positive, and V_{IN} is negative.
3. When the load is turned down, turn the input power supply on, and ensure that the voltage from the V_{IN} terminal with respect to the GND terminal is between -3.8V and -20V.
4. Vary V_{IN} from -3.8V to -20V and vary the load current from 0A to 1A. Note the following when setting the V_{IN} and the load current:
   - An input voltage too close to the programmed output voltage (too low) can cause dropout operation and a loss of output voltage regulation.
   - The amount of output current combined with an input voltage that is too high above the output can increase power dissipation to an unacceptable level.
   - The LT3099 limits output current at higher input-to-output voltage differentials. Refer to the LT3099 datasheet for more information.
5. Refer to *Application Note 83* and *Application Note 159* for guidance on measuring output noise and PSRR. Note that J1 and J2 are Bayonet Neill-Concelman (BNC) connectors that are used for noise and PSRR measurements.
6. R6 can be used to set an accurate undervoltage lockout (UVLO) threshold.
7. Change to a suitable ILIM resistor (R2) to program a current limit. ILIM architecture does not allow output current monitoring for the LT3099.

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8. Additionally, adjust the PGFB divider resistors (R3 and R4) if the SET resistor (R1) is modified. Apply a power source at V_{EXT} and monitor the power-good at the PG terminal.
9. Refer to the *High-efficiency linear regulator—input-to-output voltage control* section in the LT3099 data sheet for more details on the usage of the VIOC terminal.

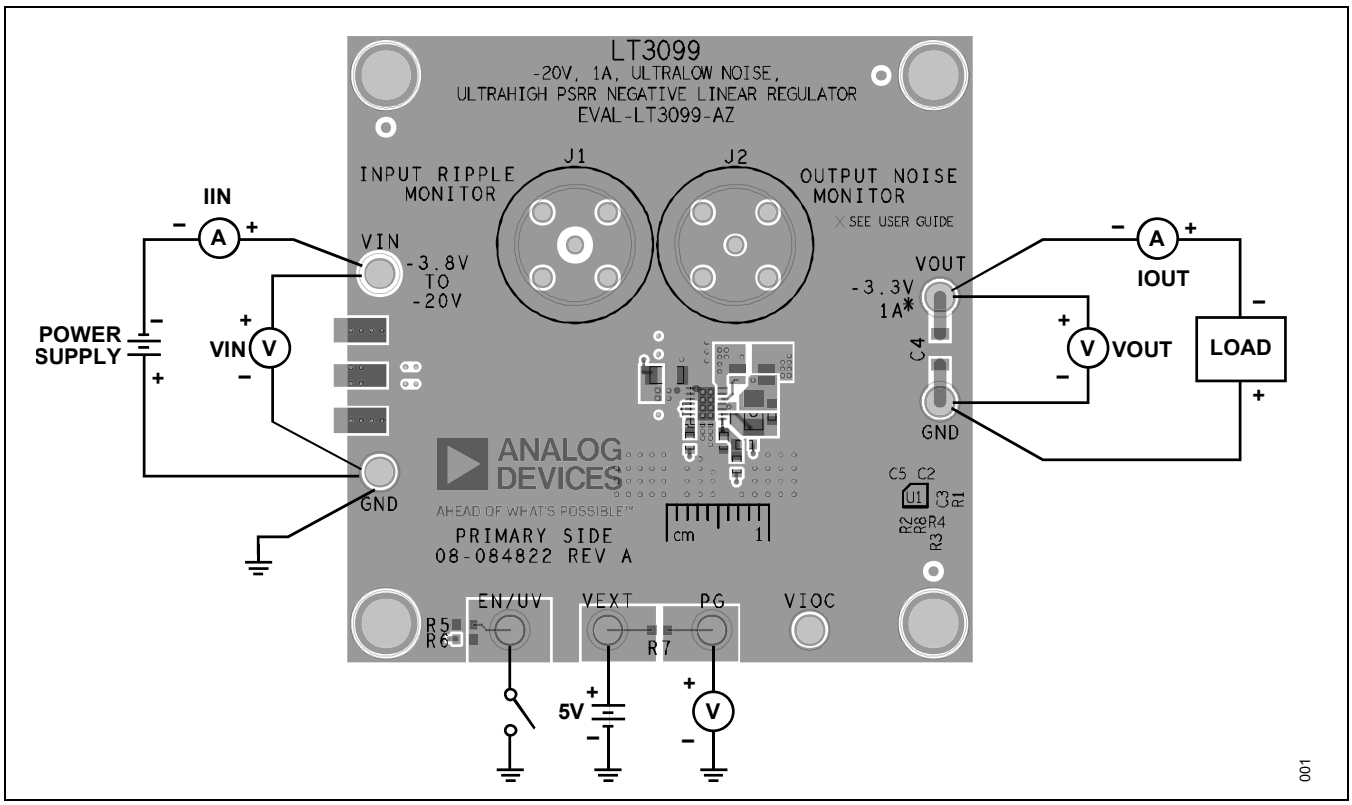

Figure 1. Proper Measurement Equipment Setup

Performance Summary

Specifications are at T_A = 25°C, unless otherwise noted.

Table 1. Performance Summary for EVAL-LT3099-AZ

PARAMETER	SYMBOL	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{IN}	I_{OUT} = 150mA, V_{OUT} = -3.3V	-3.8		-20	V
		I_{OUT} = 1A, V_{OUT} = -3.3V	-3.8		-5.8*	V
Output Voltage	V_{OUT}	V_{IN} = -5V, I_{OUT} = 1A, R1 = 33.2kΩ	-3.25	-3.32	-3.39	V
Shutdown Input Current	I_{IN}	$V_{EN/UV}$ = 0V, V_{IN} = -5V, R5 = OPEN		5		µA

*The maximum power dissipation and, consequently, the maximum input voltage for a 1 A load current is set by the 60°C temperature rise of the LT3099 on the evaluation board. Higher input voltages can be reached if a larger copper area or forced-air cooling is applied. In addition, the effect of ambient temperature and the maximum junction temperature that may occur should be considered. The LT3099 limits output current at higher input-to-output voltage differentials. Refer to the LT3099 data sheet for more information.

Printed Circuit Board (PCB) Layout

Best PSRR Performance: PCB Layout for Input Traces

For applications using the LT3099 for post-regulating switching converters, placing a capacitor directly at the LT3099 input results in AC (at the switching frequency) flowing near the LT3099. Without careful attention to the PCB layout, the relatively high-frequency switching current generates an electromagnetic field (EMF) that couples to the LT3099 output, degrading its effective PSRR. Because PSRR is highly dependent on the PCB, the switching preregulator, and the input capacitor size, among other factors, the PSRR degradation can easily be 30 dB at 1 MHz. This degradation persists even when the LT3099 is desoldered from the board, as the coupling effectively degrades the PSRR of the PCB itself. While negligible for conventional low PSRR low dropout (LDO) regulators, the ultra-high PSRR of the LT3099 requires careful attention to higher-order parasitics to realize the full performance offered by the regulator.

The EVAL-LT3099-AZ alleviates this degradation in PSRR by using a specialized layout technique. The VIN input trace and its corresponding return path (GND) are highlighted in red in *Figure 2* and *Figure 3*. *Figure 3* also shows the location of the C1 input capacitor and the connection between the V_{IN} input trace corresponding to the GND return path and the V_{IN} for the rest of the PCB. When AC voltage is applied to the inputs of the EVAL-LT3099-AZ, an AC flows through the path formed by the input and ground traces via C1. Without the proper PCB layout, the AC that flows through this path can generate EMFs that do not completely cancel and couple to the output capacitor C2 and its related traces, making the PSRR appear worse than it is. With the input trace directly above the return path, the EMFs are in opposite directions and, consequently, cancel each other out. Ensure these traces exactly overlap each other to maximize the cancellation effect and thus provide the maximum PSRR offered by the regulator.

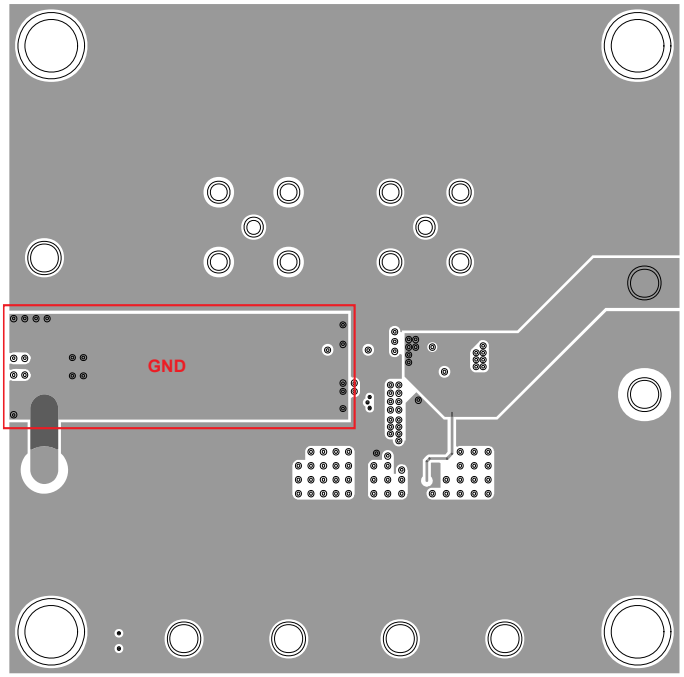

Figure 2. Layer 3 of EVAL-LT3099-AZ

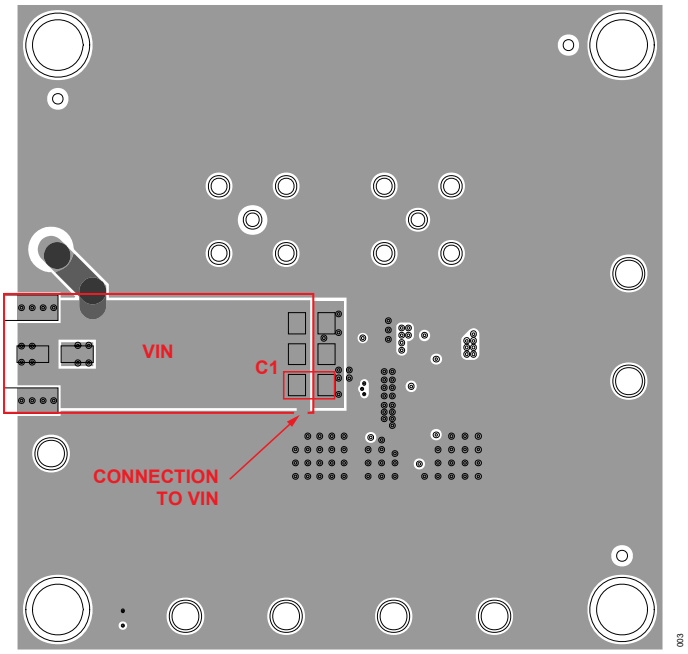

Figure 3. Layer 4 of EVAL-LT3099-AZ

Best AC Performance: PCB layout for Output Capacitors C3 and C4

For ultrahigh PSRR performance, the LT3099's bandwidth is quite high (~1 MHz), which is very close to the output capacitor's self-resonance frequency (~1.6 MHz). Therefore, avoiding the addition of extra impedance (effective series inductance (ESL) and effective series resistance (ESR)) outside the feedback loop is crucial. To achieve this avoidance, minimize the effects of PCB trace and solder inductance by Kelvin connecting output sense (OUTS) and SET pin capacitor (CSET) GND directly to the terminals of output capacitor (C2) using a split capacitor technique as shown in *Figure 4* and *Figure 5*. With only a small AC flowing through these connections, the impact of solder joint/PCB trace inductance on stability is eliminated. While the LT3099 is robust enough not to oscillate, the phase margin, gain margin, and stability degrade if the recommended layout is not followed.

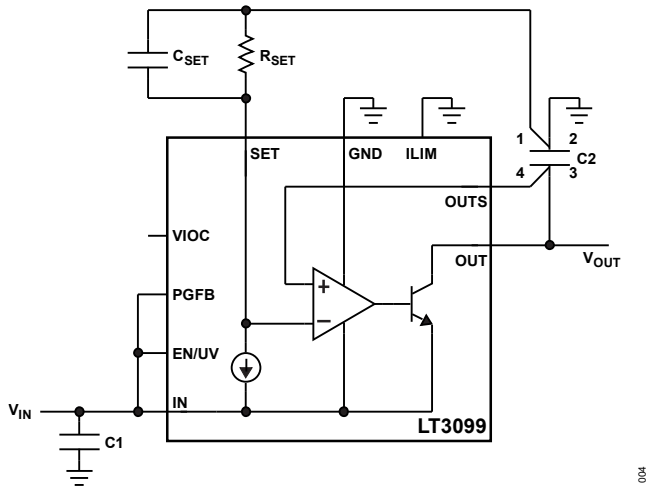

Figure 4. C2 and CSET Connections for Best Performance

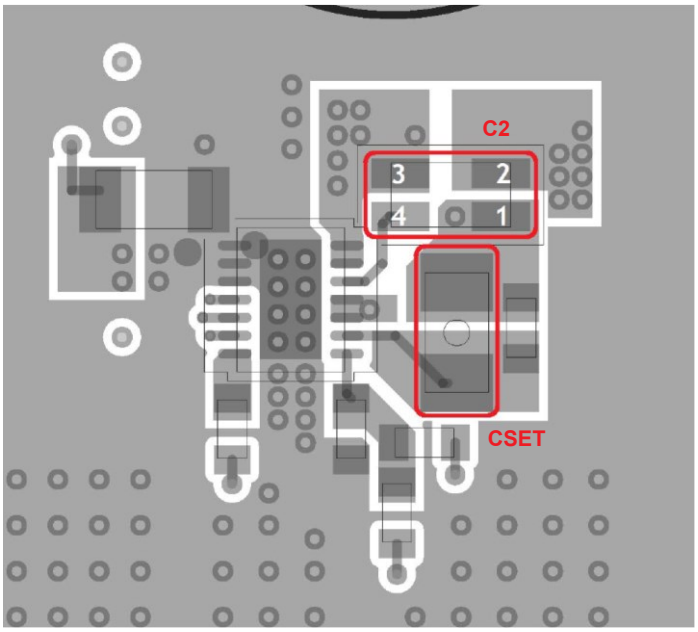

Figure 5. Split Pads for C2 on the Top Layer of EVAL-LT3099-AZ

Ordering Information

PART[1]	TYPE
EVAL-LT3099-AZ	Evaluation Board

[1]Z = RoHS Compliant Part.

EVAL-LT3099-AZ Bill of Materials

ITEM	QUANTITY	REFERENCE DESIGNATOR	PART DESCRIPTION	MANUFACTURER, PART NUMBER
REQUIRED CIRCUIT COMPONENTS				
1	1	C1	10µF capacitor, X7R, 25V, 10%, 1206	KEMET, C1206C106K3RACAUTO
2	1	C2	10µF capacitors, X7S, 25V, 10%, 1206	Murata, GCM31CC71E106KA03L
3	1	C3	4.7µF capacitor, X7R, 25V, 10%, 1206	Murata, GCJ31CR71E475KA12L
4	1	R1	33.2kΩ resistor, 1%, 1/10W, 0603	Vishay, CRCW060333K2FKEA
5	1	U1	-20V, 1A, ultra-low noise, ultra-high PSRR negative linear regulator	Analog Devices, Inc., LT3099ADE#PBF
OPTIONAL EVALUATION BOARD COMPONENTS				
1	1	CIN	22µF capacitor, 35V, 20%, 5mm x 5.4mm	KEMET, EDK226M035A9D
2	0	C4, C5, C6, C7	Capacitors, 1206, optional	
3	1	R2	0Ω, 1/10 W, 0603, AEC-Q200	Vishay, CRCW06030000Z0EA
4	1	R3	453kΩ resistor, 1%, 1/10W, 0603	Vishay, CRCW0603453KFKEA
5	1	R4	49.9kΩ resistor, 1%,1/10W, 0603	Vishay, CRCW060349K9FKEA
6	1	R5	100kΩ resistor, 1%, 1/10W, 0603	Vishay, CRCW0603100KFKEA
7	1	R7	100kΩ resistor, 5%, 1/10 W, 0603	Vishay, CRCW0603100KJNEA
8	0	R6, R8	Resistor, 0603, optional	
HARDWARE				
1	7	E1–E8	Test points, turret, 0.094" PBF	Mill-Max, 2501-2-00-80-00-00-07-0
2	2	J1, J2	Connector, RF, BNC, receptacle, jack, 5-pin, straight, through-hole, 50Ω	Amphenol RF, 112404
3	0	J3	Connector, RF, subminiature version A (SMA), receptacle, jack, 5-pin, end launch	Cinch, 142-0701-851
4	4	MP1 to MP4	Standoff, nylon, snap-on, 6.4mm	Würth Elektronik, 702931000

EVAL-LT3099-AZ Schematic

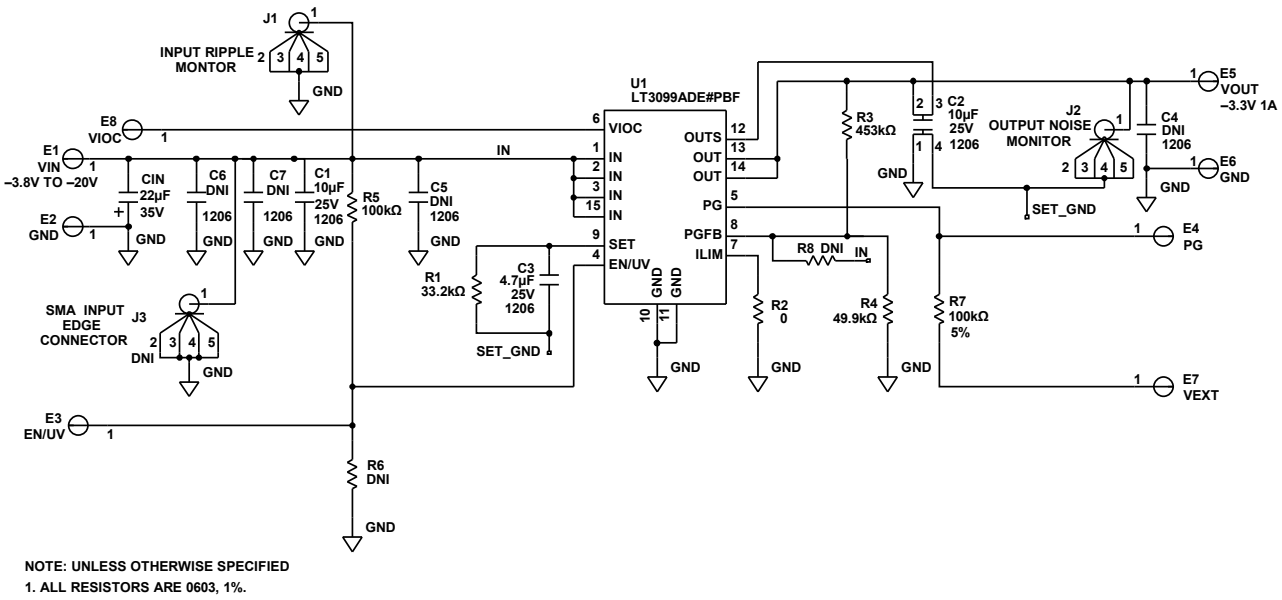

Figure 6. Schematic Diagram for the EVAL-LT3099-AZ

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	04/25	Initial release	—

Notes

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