ABFB10XC3A series

Low Skew, Low Additive Jitter, 10 Output LVPECL/LVDS/ HCSL Fanout Buffer with One LVCMOS Output

Description

The Abracon ABFB10XC3A series is a clock buffer, offering ten differential LVPECL/LVDS/HCSL outputs with one LVCMOS output and is available in a 48-pin 7mm x 7mm x 0.9mm VQFN package. This series features a wide frequency range from 0MHz to 1.6GHz, low output skew, and ultra-low additive jitter. The ABFB10XC3A series supports 2.5V or 3.3V supply voltage on the LVPECL/LVDS/HCSL outputs or 1.5V, 1.8V, 2.5V, or 3.3V supply voltage on the LVCMOS output; it has an embedded low drop out (LDO) voltage regulator that provides superior power supply noise rejection (PSNR). Its operation is ensured over the industrial temperature range -40°C to +85°C.

Features

- 3-to-1 Input Multiplexer: Two Inputs Accept Any Differential (LVPECL, HCSL, LVDS, SSTL, CML,
- LVCMOS) or a Single-Ended Signal and the Third Input Accepts a Crystal or a Single-Ended Signal
- Ten Differential LVPECL/LVDS/HCSL Outputs
- One LVCMOS Output
- Ultra-Low Additive Jitter: 24 fs (Integration Band: 12 kHz to 20 MHz at 625 MHz Clock Frequency)
- Supports Clock Frequencies from 0 to 1.6 GHz
- Supports 2.5V or 3.3V Power Supplies on LVPECL/LVDS/HCSL Outputs
- Supports 1.5V, 1.8V, 2.5V, or 3.3V on LVCMOS Output
- Embedded Low Dropout (LDO) Voltage Regulator Provides Superior Power Supply Noise Rejection
- Maximum Output to Output Skew of 40 ps
- Device Controlled via Control Pins
- REACH/RoHS II Compliant | MSL Level 3

Typical Applications

- PCIe Gen1/2/3/4/5/6 Clock Distribution
- Low-Jitter Clock Trees
- Logic Translation
- Clock and Data Signal Restoration
- Wired Communications: OTN, SONET/SDH, GE, 10GE, FC and 10G FC
- General Purpose Clock Distribution
- Wireless Communications
- High Performance Microprocessor Clock Distribution
- Test Equipment

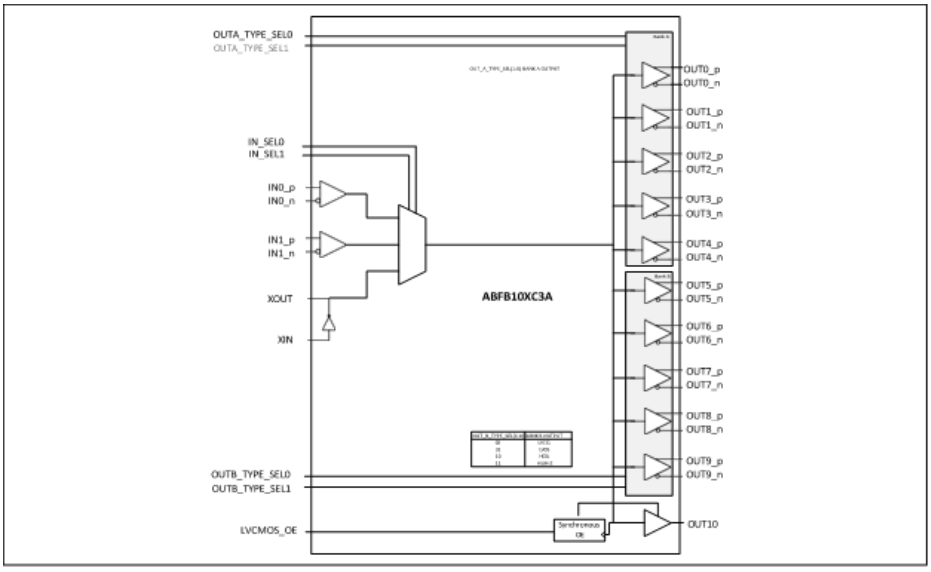

FIGURE 0.1: Functional Block Diagram.

Part Identification

ABFB10XC3A-□

Packaging
Blank: Bulk
T: 260/tray
T3: 3000/Reel (12 mm pocket pitch)

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1.0 PIN DESCRIPTION AND CONFIGURATION

The device is packaged in a 7 mm x 7 mm, 48-lead VQFN.

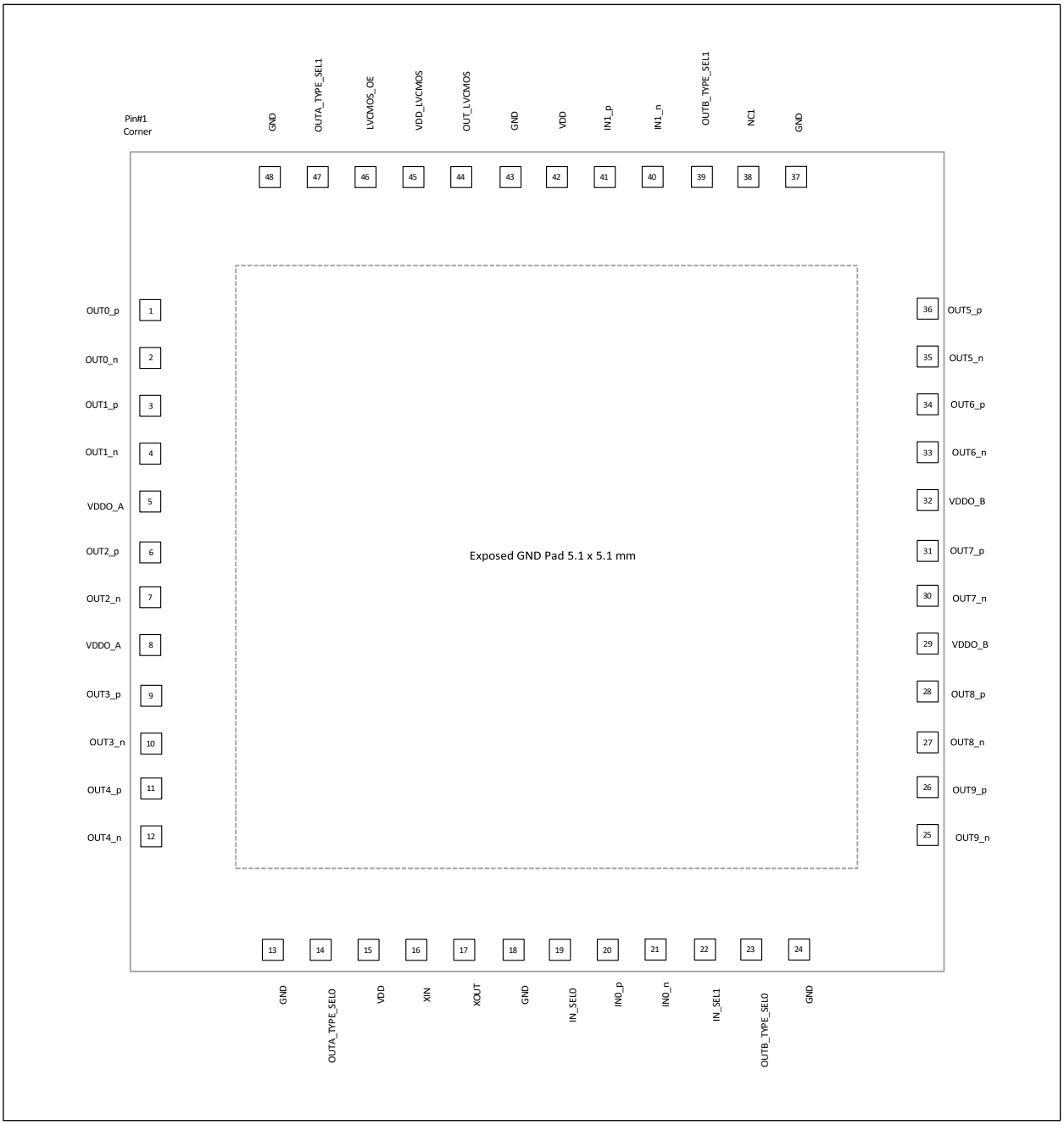


FIGURE *1.1*: 48-Lead 7 mm x 7 mm VQFN.

1.1 Pin Descriptions

All device inputs and outputs are LVPECL unless described otherwise. The I/O column uses the following symbols: I – input, IPU – input with 300 kΩ internal pull-up resistor, IPD – input with 300 kΩ internal pull-down resistor, IAPU – input with 31 kΩ internal pull-up resistor, IAPD – input with 30 kΩ internal pull-down resistor, IAPU/APD – input biased to VDD/2 with 60 kΩ internal pull-up and pull-down resistors (30 kΩ equivalent), O – output, I/O – Input/Output pin, NC – No connect, P – power supply pin.

TABLE 1.1: PIN DESCRIPTION

Pin Number	Pin Name	Type	Description
Input Reference			
20	IN0_p	I_{APD}	**Input Differential or Single-Ended References 0 and 1**
21	IN0_n	$I_{APU/APD}$	
41	IN1_p	I_{APD}	Input frequency range 0 Hz to 1.6 GHz.
40	IN1_n	$I_{APU/APD}$	Non-inverting inputs (_p) are pulled down with internal 30 kΩ pull-down resistors. Inverting inputs (_n) are pulled up and pulled down with 60 kΩ internal resistors (30 kΩ equivalent) to keep inverting input voltages at $V_{DD}/2$ when inverting inputs are left floating (device fed with a single-ended reference).
Output Clocks			
1	OUT0_p	O	**Ultra-Low Additive Jitter Differential LVPECL/HCSL/LVDS Outputs 0 to 9** Output frequency range 0 Hz to 1.6 GHz Type (LVPECL/HCSL/LVDS/High-Z) of each output bank is controlled via OUTA/B_TYPE_SEL0/1 pins.
2	OUT0_n		
3	OUT1_p		
4	OUT1_n		
6	OUT2_p		
7	OUT2_n		
9	OUT3_p		
10	OUT3_n		
11	OUT4_p		
12	OUT4_n		
36	OUT5_p		
35	OUT5_n		
34	OUT6_p		
33	OUT6_n		
31	OUT7_p		
30	OUT7_n		
28	OUT8_p		
27	OUT8_n		
26	OUT9_p		
25	OUT9_n		
44	OUT_LVCMOS	O	**Ultra-Low Additive Jitter LVCMOS Output 0 to 9** Output frequency range 0 Hz to 250 MHz

TABLE 1.1: PIN DESCRIPTION (CONTINUED)

Pin Number	Pin Name	Type	Description
Control			
19 22	IN_SEL0 IN_SEL1	I_{PD} or I_{PU}	**Input select pins.** Logic level on these pins selects which input will be passed to the output. **IN_SEL1** / **IN_SEL0** / **OUTN** 0 / 0 / Input 0 (IN0) 0 / 1 / Input 1 (IN1) 1 / X / Crystal Oscillator
14 47	OUTA_TYPE_SEL0 OUTA_TYPE_SEL1	I_{PD}	**Output Signal for Bank A:** Selects Type of the output for Bank A (Outputs 0 to 4). **OUTA_TYPE_SEL1** / **OUTA_TYPE_SEL0** / **Output 0 to 4** 0 / 0 / LVPECL 0 / 1 / LVDS 1 / 0 / HCSL 1 / 1 / High-Z (Disabled)
23 39	OUTB_TYPE_SEL0 OUTB_TYPE_SEL1	I_{PD}	**Output Signal for Bank B:** Selects Type of the output for Bank B (Outputs 5 to 9). **OUTB_TYPE_SEL1** / **OUTB_TYPE_SEL0** / **Output 5 to 9** 0 / 0 / LVPECL 0 / 1 / LVDS 1 / 0 / HCSL 1 / 1 / High-Z (Disabled)
46	LVCMOS_OE	I	**Output enable for LVCMOS outputs:** When high LVCMOS output is enabled. When low LVCMOS output is High-Z
Crystal Oscillator			
16	XIN	I	**Crystal Oscillator Input or Crystal Bypass Mode or Crystal Overdrive Mode** If crystal oscillator circuit is not used, connect a pull-down to this pin or connect it to ground.
17	XOUT	O	**Crystal Oscillator Output**
No Connect			
38	NC1	NC	**No Connect (not connected to the die)** Leave unconnected or connect to GND for mechanical support.
Power and Ground			
15 42	VDD	P	**Positive Supply Voltage.** Connect to 3.3V or 2.5V supply.
5 8	VDDO_A	P	**Positive Supply Voltage for Differential Outputs Bank A** Connect to 3.3V or 2.5V power supply. VDDO_A does not have to be connected to the same voltage level as VDD or VDDO_B. These pins power up differential outputs OUT[0:4]_p/n.
29 32	VDDO_B	P	**Positive Supply Voltage for Differential Outputs Bank B** Connect to 3.3V or 2.5V power supply. VDDO_B does not have to be connected to the same voltage level as VDD or VDDO_A. These pins power up differential outputs OUT[5:9]_p/n.
45	VDD_LVCMOS	P	**Power Supply Voltage for LVCMOS Output** Connect to 3.3V, 2.5V, 1.8V, or 1.5V power supply.

TABLE 1.1: PIN DESCRIPTION (CONTINUED)

Pin Number	Pin Name	Type	Description
13 18 24 43 37 48	GND	P	**Ground.** Connect to ground.
ePad	GND	P	**Ground.** Connect to ground.

2.0 FUNCTIONAL DESCRIPTION

The device is a low additive jitter, low power 3 x 10 LVPECL/HCSL/LVDS fanout buffer.

Two inputs can accept signal in differential (LVPECL, SSTL, LVDS, HSTL, CML) or single-ended (LVPECL or LVCMOS) format and the third input can accept a single-ended signal or it can be used to build a crystal oscillator by connecting an external crystal resonator between its XIN and XOUT pins.

The device has ten LVPECL/HCSL/LVDS outputs that can be powered from 3.3V or 2.5V supply. Each output bank (A and B) can be independently set to be LVPECL, HCSL, LVDS, or Hi-Z via control OUTA/B_TYPE_SEL0/1 pins.

The device operates from 2.5V±5% or 3.3V±5% supply. Its operation is ensured over the industrial temperature range of –40°C to +85°C.

2.1 Clock Inputs

The following blocks diagram shows how to terminate different signals fed to the device inputs.

Figure 2-1 shows how to terminate a single ended output such as LVCMOS. Resistors Ideally, resistors R1 and R2 should be 100Ω each and RO + RS should be 50Ω so that the transmission line is terminated at both ends with charac-teristic impedance. If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor RS should be increased. This will reduce the voltage swing at the input but this should be fine as long as the input voltage swing requirement is not violated (Table 4-4). The source resistors of RS = 270Ω could be used for stan-dard LVCMOS driver. This will provide 516 mV of voltage swing for 3.3V LVCMOS driver with load current of (3.3V/2) x (1/(270Ω + 50Ω)) = 5.16 mA.

For optimum performance both differential input pins (_p and _n) need to be DC biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4

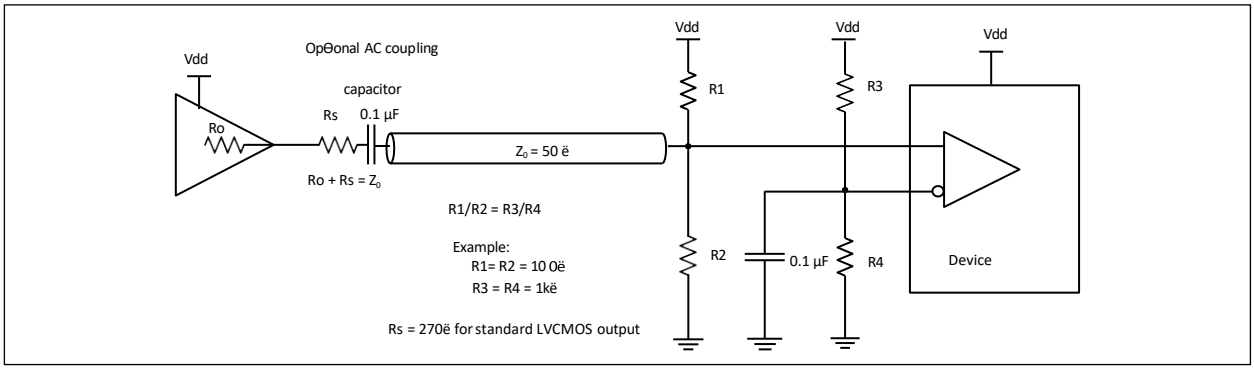


FIGURE 2.1: Input Driven by a Single-Ended Output.

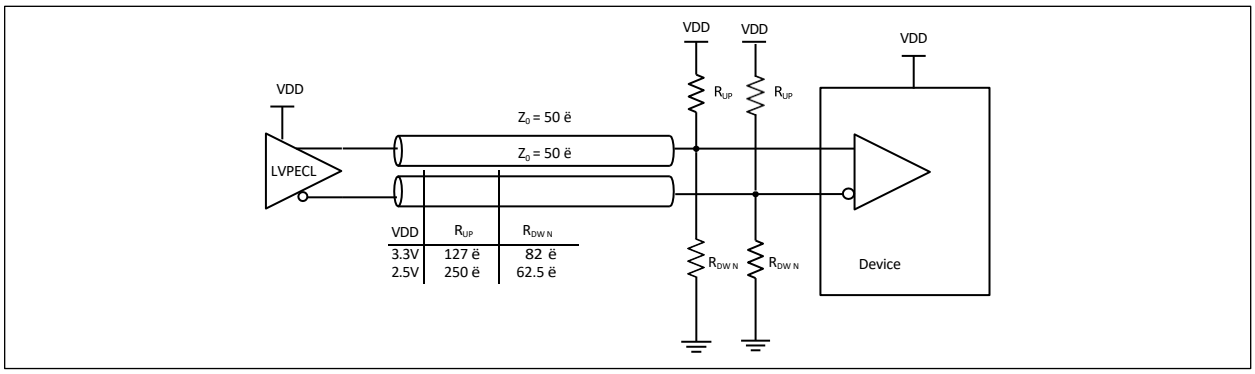


FIGURE 2.2: Input Driven by DC-Coupled LVPECL Output.

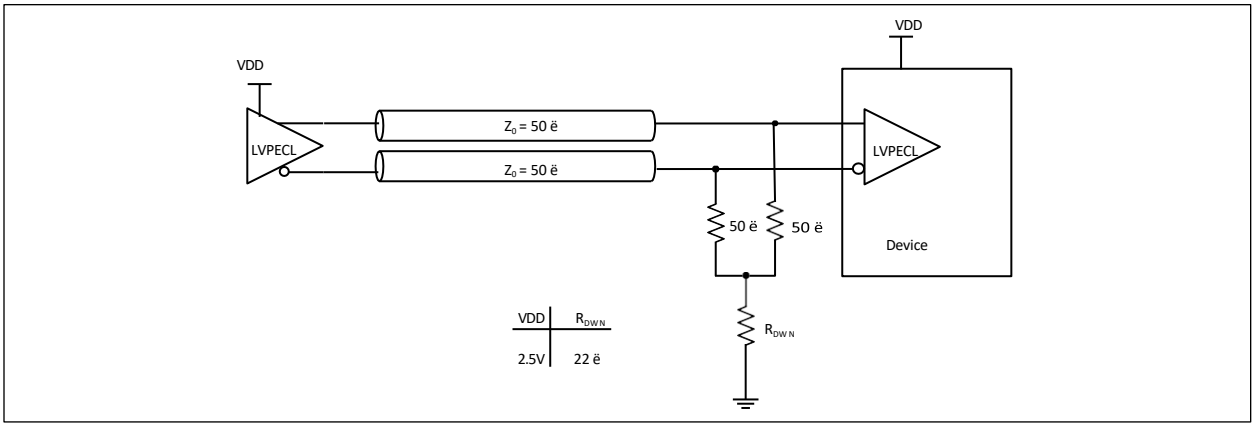


FIGURE 2.3: Input Driven by DC-Coupled LVPECL Output (Alternative Termination).

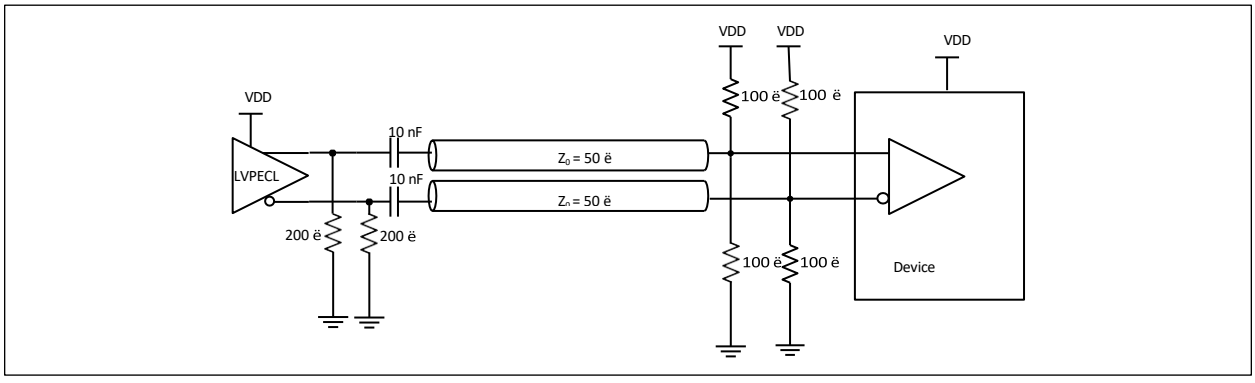


FIGURE 2.4: Input Driven by AC-Coupled LVPECL Output.

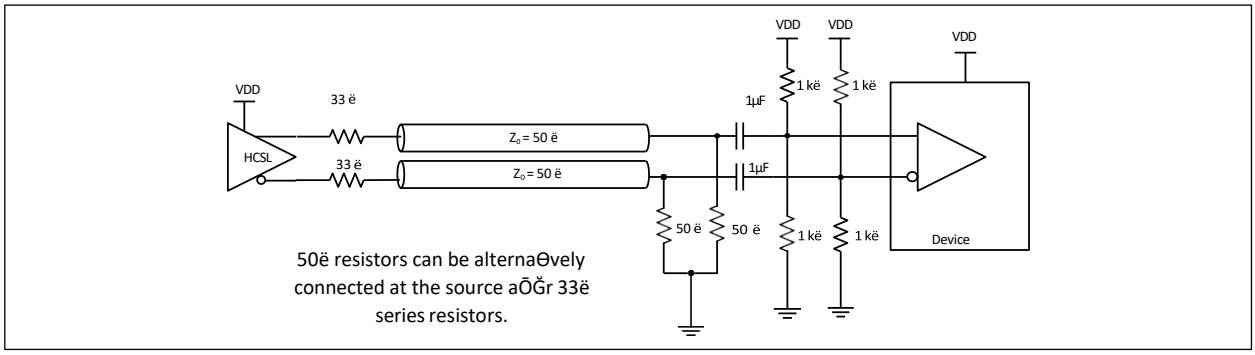


FIGURE 2.5: Input Driven by HCSL Output.

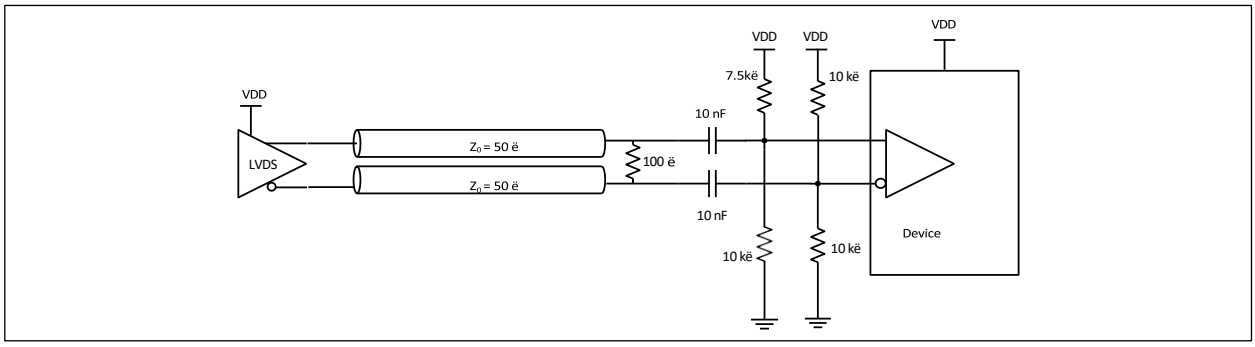


FIGURE 2.6: Input Driven by LVDS Output.

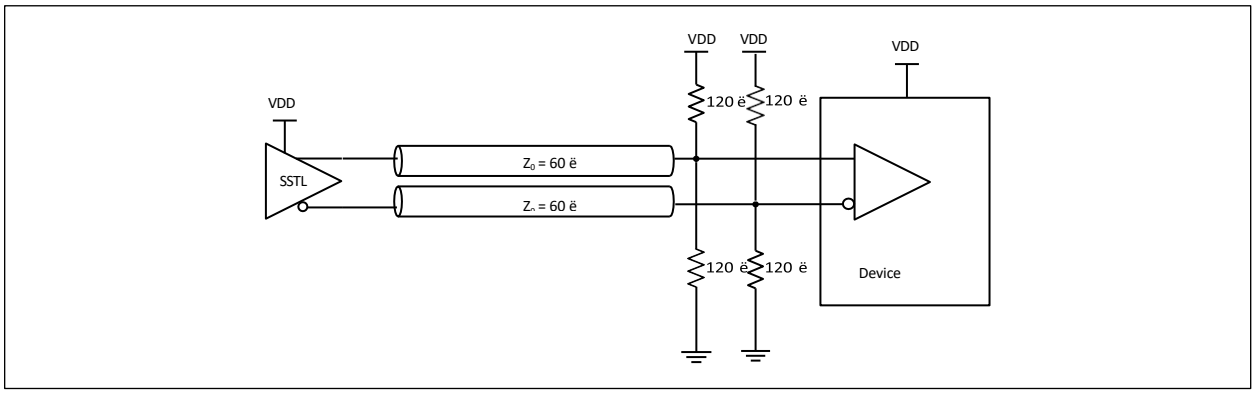


FIGURE 2.7: Input Driven by an SSTL Output.

2.2 Clock Outputs

The LVCMOS output (OUT10) requires only a series termination resistor whose value is dependent on the LVCMOS output voltage as shown in Figure 2-8.

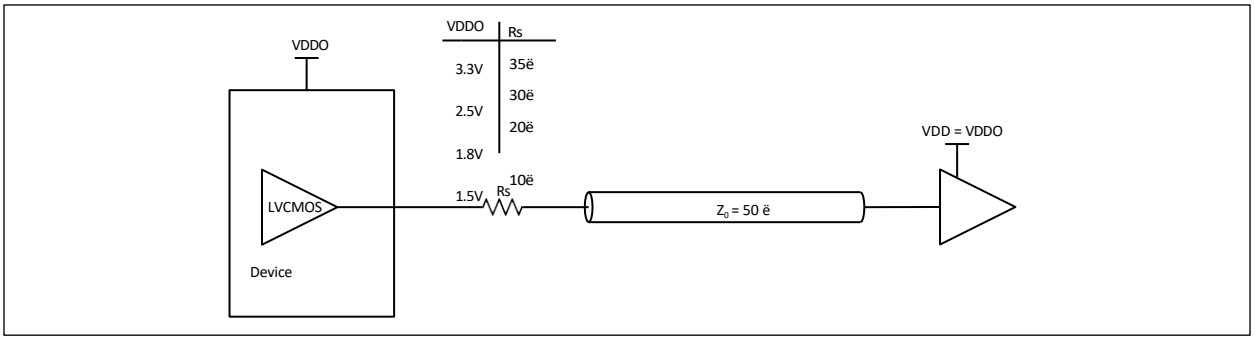


FIGURE 2.8: Termination for LVCMOS Output.

Differential outputs LVPECL and LVDS should have the same termination as their corresponding outputs described in the previous section. HCSL outputs should be terminated with 33Ω series resistors at the source and 50Ω shunt resis-tors at the source or at the end on the transmission line. AC coupling and re-biasing is not required at the outputs when driving native HCSL receivers.

The device is designed to drive the differential input of semiconductor devices. In applications that use a transformer to convert from the differential to the single-ended output (for example, driving an oscilloscope 50Ω input), a resistor larger than 10Ω should be added at the center tap of the primary winding to achieve optimum jitter performance as shown in Figure 2-9. This is to provide a nominal common mode impedance of 10Ω or higher, which is typical for differential ter-minations.

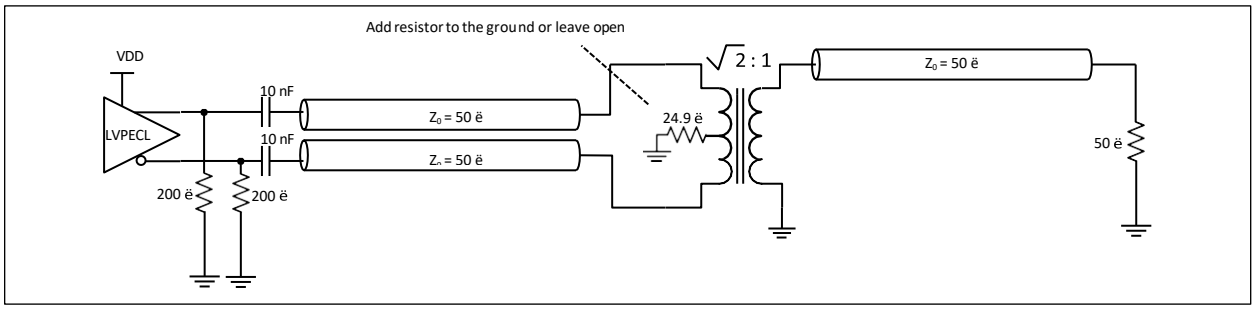


FIGURE 2.9: Driving a Load via Transformer.

2.3 Crystal Oscillator Input

The crystal oscillator circuit can work with crystal resonators from 8 MHz to 60 MHz. Load capacitors C1, C2, and series resistor RS shall be selected as per crystal vendor recommendation. A shunt resistor is implemented inside the device.

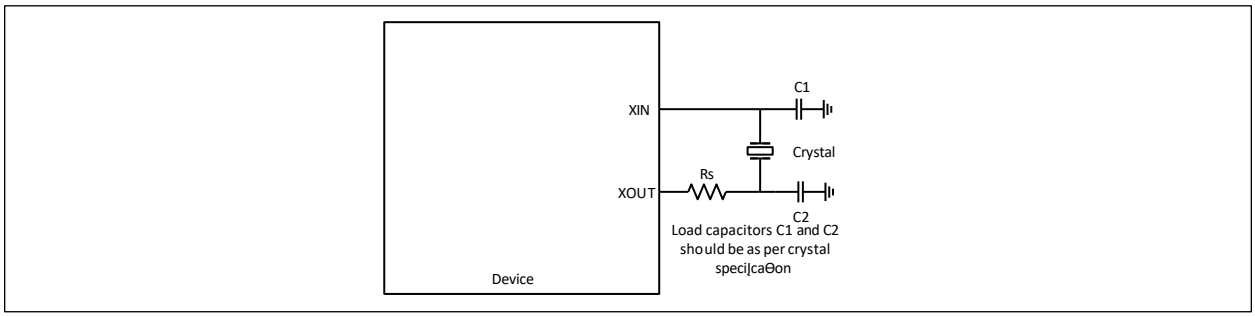


FIGURE 2.10: Crystal Oscillator Circuit.

2.4 Termination of Unused Inputs and Outputs

Unused inputs can be left unconnected or, alternatively, IN_0/1 can be pulled down by a 1 kΩ resistor. Unused outputs should be left unconnected.

2.5 Power Consumption

The device's total power consumption can be calculated as:

EQUATION 2-1:

$$P_T = P_S + P_{XTAL} + P_C + P_{O\_DIF} + P_{O\_LVCMOS}$$

Where:

$P_S = V_{DD} \times I_S$ — The core power when the XTAL is not used. The current is specified in Table 4-3. If the XTAL is running, this power should be set to zero.

$P_{XTAL} = V_{DD} \times I_{DD\_XTAL}$ — The core power when the XTAL is used. The current is specified in Table 4-3. If the XTAL is not used, this power should be set to zero.

$P_C = V_{DDO} \times I_{DD\_CM}$ — Common output power shared among all ten outputs. The current $I_{DD\ CM}$ is specified Table 4-3.

$P_{O\_DIF} = V_{DDO} \times (I_{DD\_LVDS} \times N_1 + I_{DD\_LVPECL} \times N_2 + I_{DD\_HCSL} \times N_3)$ — Output power where output current (I_{DD_LVDS}) is specified Table 4-3. For LVPECL or HCSL, just replace I_{DD_LVDS} with I_{DD_LVPECL} or I_{DD_HCSL}. N is the number of enabled differen-tial outputs and can either be 0, 5, or 10.

$P_{O\_LVCMOS} = V_{DD\_LVCMOS} \times (I_{DD} \times f / 100MHz + V_{DD\_LVCMOS} \times C_{LOAD} \times f)$ — Dynamic LVCMOS output power. I_{DD} is specified in Table 4-3. If LVCMOS output is disabled, this term is equal to zero.

Power dissipated inside the device can be calculated by subtracting the power dissipated in termination/biasing resistors from the power consumption.

EQUATION 2-2:

$$P_D = P_T - N_1 \times P_{LVPECL} - N_2 \times P_{LVDS} - N_3 \times P_{HCSL}$$

Where:

N_1, N_2, and N_3 are the number of enabled LVPECL, LVDS, and HSCL outputs, respectively. When both banks are enabled, N_1 + N_2 + N_3 equals 10 and one or two of N_1, N_2, and N_3 will equal 0.

$$P_{LVPECL} = (V_{OH} - V_B)^2 / 50\Omega + (V_{OL} - V_B)^2 / 50\Omega + (V_{OH} - V_B) \times V_B / 50\Omega + (V_{OL} - V_B) \times V_B / 50\Omega$$

V_{OH} and V_{OL} are the output high and low voltages respectively for LVPECL output.

V_B is LVPECL bias voltage equal to V_{DD} – 2V.

$$P_{LVDS} = V_{SW}^2 / 100\Omega$$

V_{SW} is the voltage swing of the LVDS output.

$$P_{HCSL} = (V_{SW} / 50\Omega)^2 \times (33\Omega + 50\Omega)$$

V_{SW} is the voltage swing of the HCSL output. 50Ω is the termination resis-tance and 33Ω is the series resistance of the HCSL output.

2.6 Power Supply Filtering

Each power pin (VDD and VDDO) should be decoupled with a 0.1 µF capacitor with minimum equivalent series resis-tance (ESR) and minimum series inductance (ESL). For example, 0402 X5R ceramic capacitors with 6.3V minimum rat-ing could be used. These capacitors should be placed as close as possible to the power pins. To reduce the power noise from adjacent digital components on the board, each power supply could be further insulated with a low resistance ferrite bead with two capacitors. The ferrite bead will also insulate adjacent components from the noise generated by the device. Figure 2-11 shows recommended decoupling for each power pin.

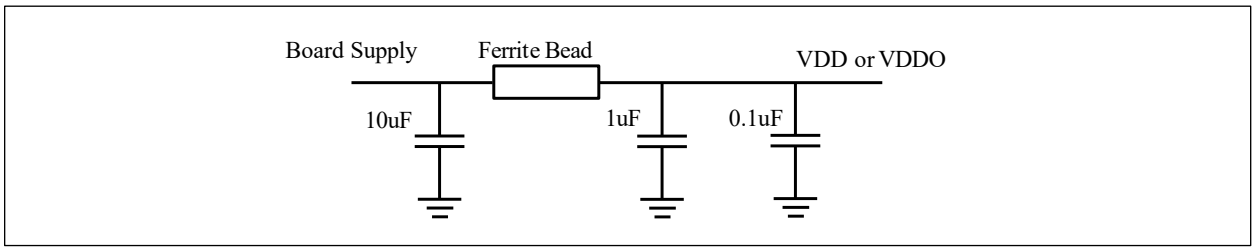


FIGURE 2.11: Power Supply Filtering.

2.7 Power Supplies and Power-Up Sequence

The device has four different power supplies: VDD, VDDO_A, VDDO_B, and VDD_LVCMOS which are mutually inde-pendent. Voltages supported by each of these power supplies are specified in Table 1-1.

The device is not sensitive to the power-up sequence. For example, a commonly used sequence where higher voltage comes up before or at the same time as the lower voltages can be used (or any other sequence).

2.8 Host Interface

ABFB10XC3A is controlled via Input Select (IN_SEL0/1) pins that select which one of three inputs is fed to the output and show in Table 2-1 and OUTA/B_TYPE_SEL0/1 pins that select signal level (LVPECL, LVDS, HCSL, or Hi-Z) for each of two (A and B) output banks as shown in Table 2-2.

All input control pins have a low input threshold voltage so they can be driven from the device with low output voltage (FPGA/CPLD). Supported voltages are between 1.2V and V_{DD} (2.5V or 3.3V).

TABLE 2.1: INPUT CLOCK SELECTION

IN_SEL1	IN_SEL0	Selected Input
0	0	IN0_p, IN0_n
0	1	IN1_p, IN1_n
1	X	XIN

TABLE 2.2: OUTPUT TYPE SELECTION

OUTA/B_TYPE_SEL1	OUTA/B_TYPE_SEL0	Output
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	High-Z (Output Disabled)

3.0 TYPICAL DEVICE PERFORMANCE

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

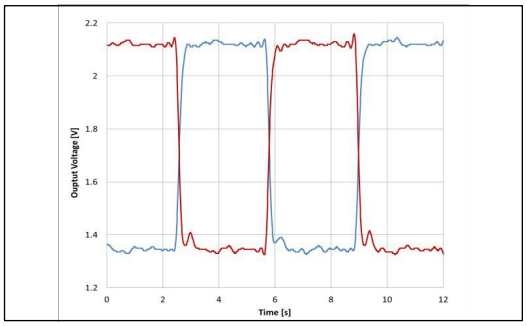


FIGURE 3.1: 156.25 MHz LVPECL.

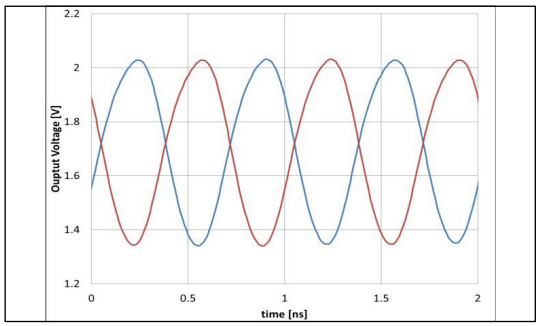


FIGURE 3.2: 1.5 GHz LVPECL.

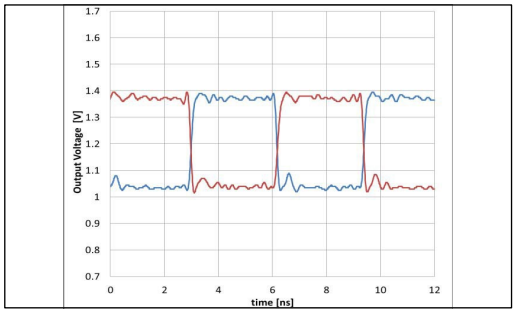


FIGURE 3.3: 156.25 MHz LVDS.

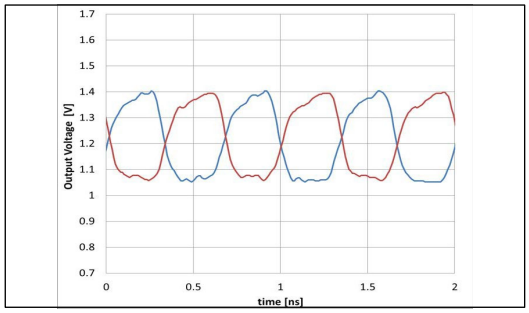


FIGURE 3.4: 1.5 GHz LVDS.

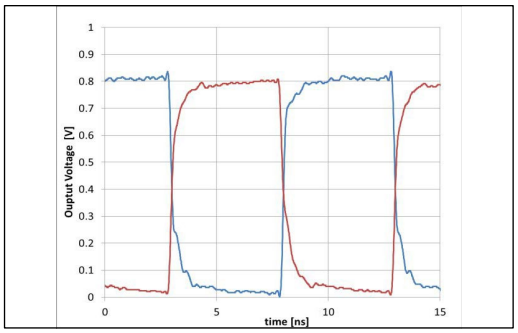


FIGURE 3.5: 100 MHz HCSL.

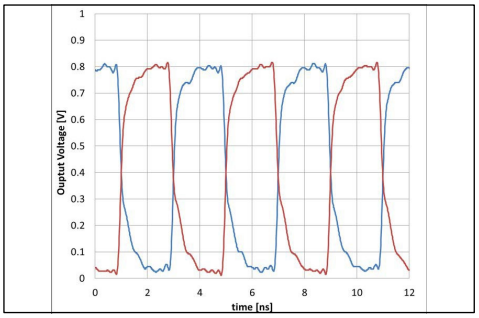


FIGURE 3.6: 250 MHz HCSL.

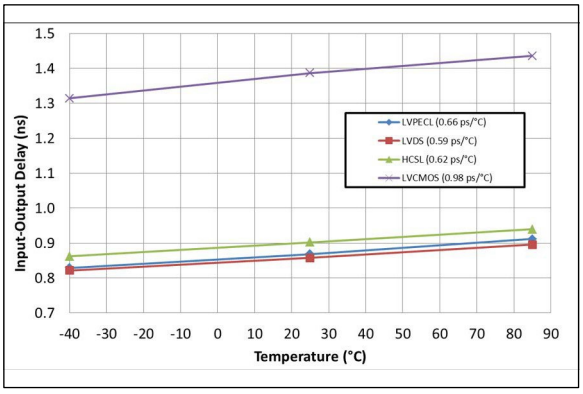


FIGURE 3.7: I/O Delay vs. Temperature.

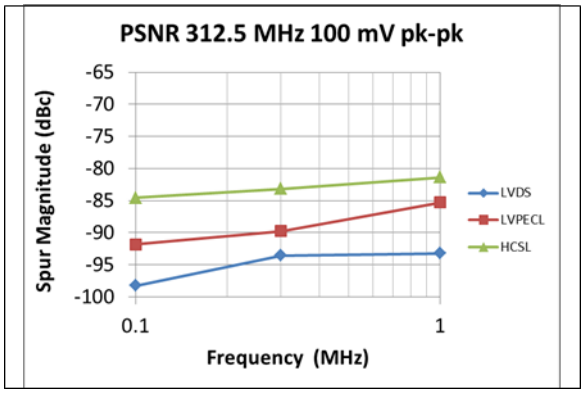


FIGURE 3.8: PSNR vs. Noise Frequency.

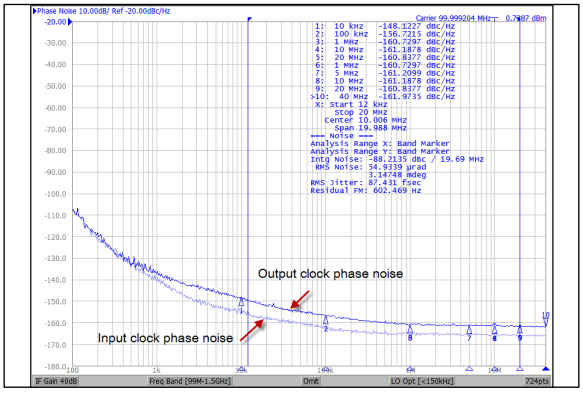


FIGURE 3.9: 100 MHz LVPECL Phase Noise.

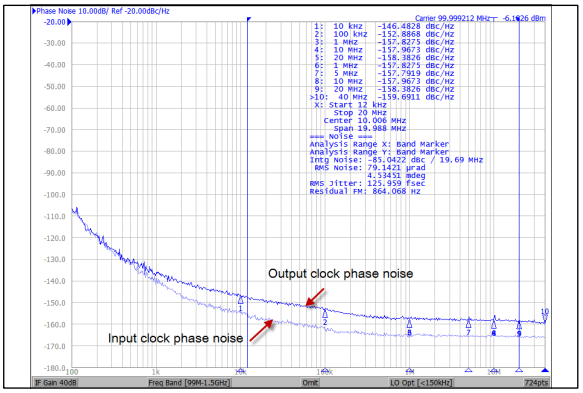


FIGURE 3.10: 100 MHz LVDS Phase Noise.

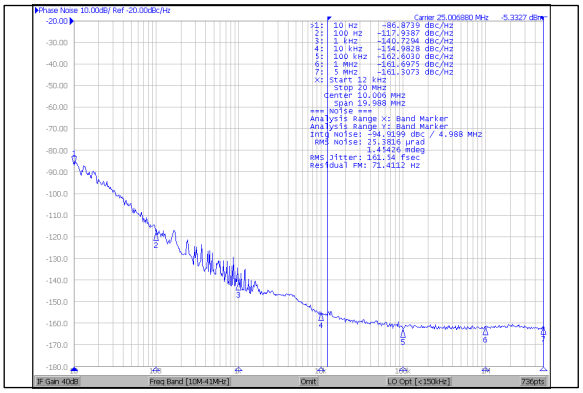


FIGURE 3.11: 25 MHz LVDS Phase Noise in XTAL Mode.

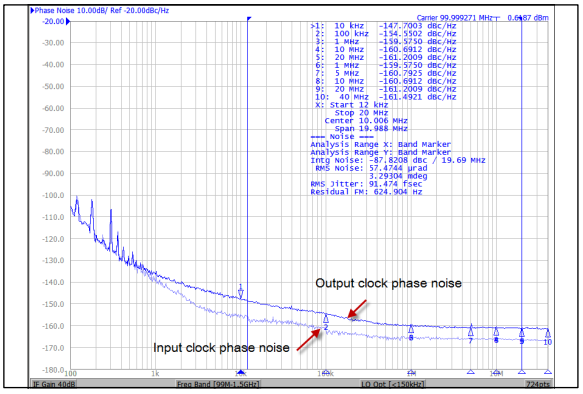


FIGURE 3.12: 100 MHz HCSL Phase Noise.

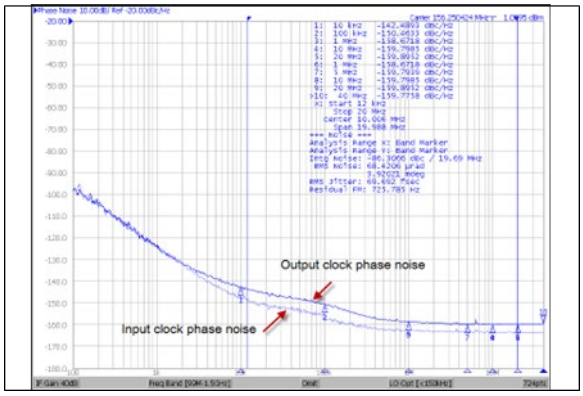


FIGURE 3.13: 156.25 MHz LVPECL Phase Noise.

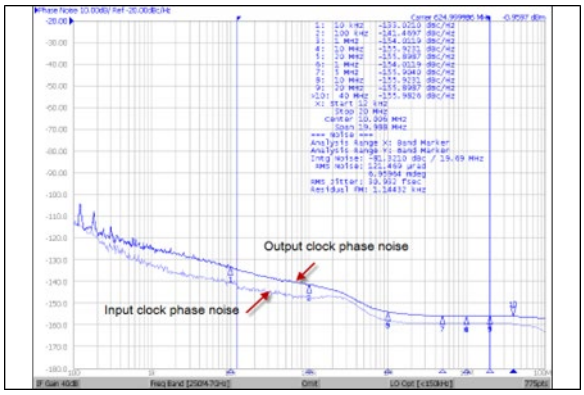


FIGURE 3.14: 625 MHz LVPECL Phase Noise.

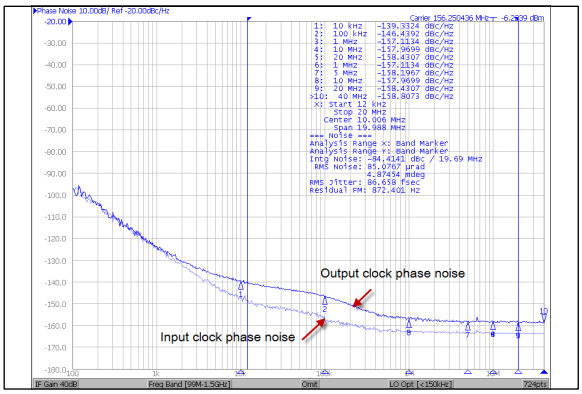


FIGURE 3.15: 156.25 MHz LVDS Phase Noise.

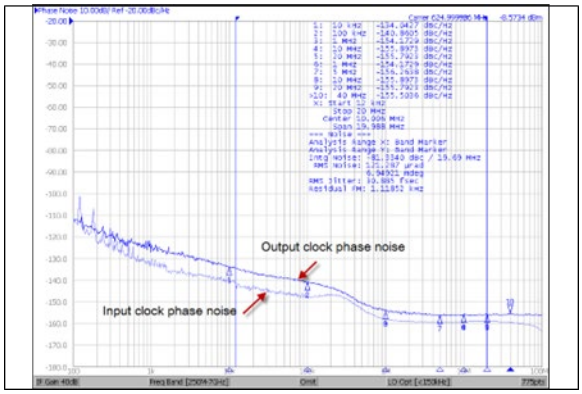


FIGURE 3.16: 625 MHz LVDS Phase Noise.

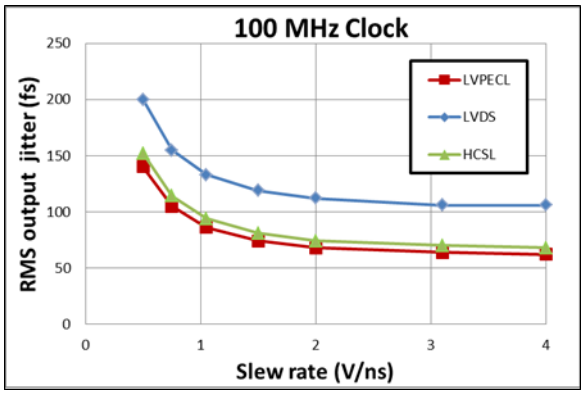


FIGURE 3.17: Output RMS Jitter (12 kHz to 20 MHz) vs. Input Clock Slew Rate.

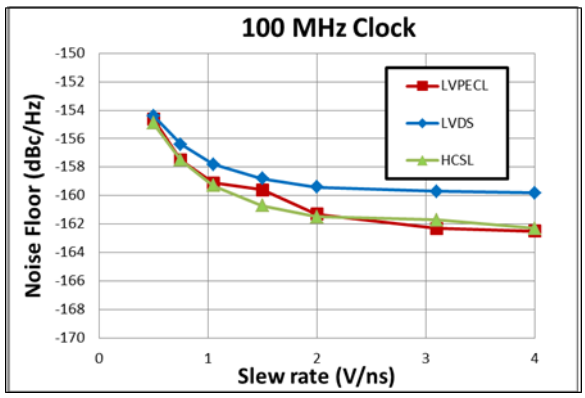


FIGURE 3.18: Output Clock Noise Floor vs. Input Clock Slew Rate.

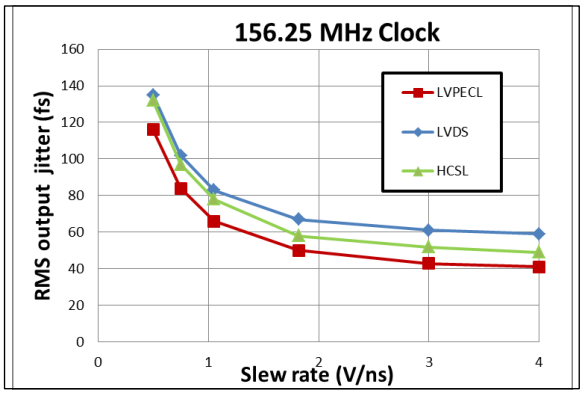


FIGURE 3.19: Output RMS Jitter (12 kHz to 20 MHz) vs. Input Clock Slew Rate.

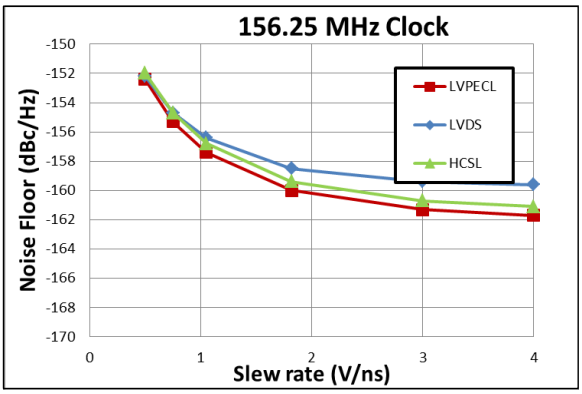


FIGURE 3.20: Output Clock Noise Floor vs. Input Clock Slew Rate.

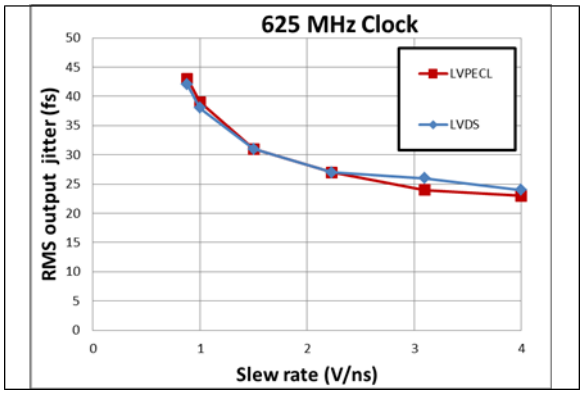


FIGURE 3.21: Output RMS Jitter (12 kHz to 20 MHz) vs. Input Clock Slew Rate.

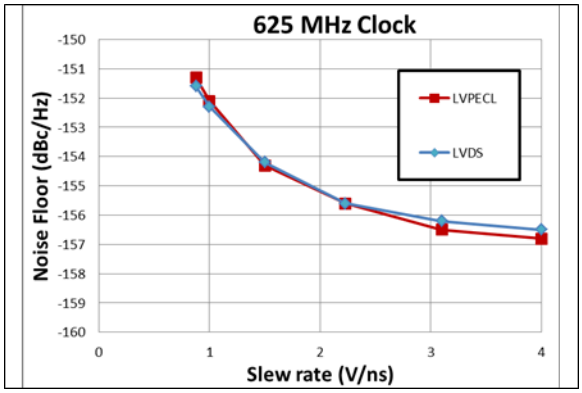


FIGURE 3.22: Output Clock Noise Floor vs. Input Clock Slew Rate.

4.0 ELECTRICAL CHARACTERISTICS

TABLE 4.1: ABSOLUTE MAXIMUM RATINGS

(Note 1, Note 2, Note 3)

Parameter	Symbol	Min.	Max.	Units.
Supply Voltage, 3.3V	V_{DD}/V_{DDO}	–0.5	4.6	V
Supply Voltage, 2.5V	V_{DD}/V_{DDO}	–0.5	3.5	V
Storage Temperature Range	T_{ST}	–55	125	°C

Note 1: Exceeding these values may cause permanent damage.
Note 2: Functional operation under these conditions is not implied.
Note 3: Voltages are with respect to ground (GND) unless otherwise stated.

TABLE 4.2: RECOMMENDED OPERATING CONDITIONS

(Note 1, Note 2, Note 3)

Parameter	Symbol	Min.	Typ.	Max.	Units.
Supply Voltage, 3.3V	$V_{DD}/V_{DDO}/ V_{DD\_LVCMOS}$	3.135	3.30	3.465	V
Supply Voltage, 2.5V	$V_{DD}/V_{DDO}/ V_{DD\_LVCMOS}$	2.375	2.50	2.625	V
Supply Voltage, 1.8V	V_{DD_LVCMOS}	1.6	1.8	2.0	V
Supply Voltage, 1.5V	V_{DD_LVCMOS}	1.35	1.5	1.65	V
Operating Temperature	T_A	–40	+25	+85	°C
Input Voltage	V_{DD-IN}	–0.3	—	V_{DD} + 0.3	V

Note 1: Voltages are with respect to ground (GND) unless otherwise stated.
Note 2: The device core supports two power supply modes (3.3V and 2.5V).

TABLE 4.3: CURRENT CONSUMPTION

Parameter	Symbol	Min.	Typ.	Max.	Units.	Condition.
Core device current (all outputs and XTAL disabled)	$I_{S\_3.3V}$	—	163	197	mA	V_{DD} = 3.3V+5%
	$I_{S\_2.5V}$	—	153	187	mA	V_{DD} = 2.5V+5%
Core device current (all outputs dis-abled) XTAL circuit enabled with 25 MHz Crystal connected between XIN and XOUT	$I_{DD\_XTAL\_3.3V}$	—	128	154	mA	V_{DD} = 3.3V+5%
	$I_{DD\_XTAL\_2.5V}$	—	124	150	mA	V_{DD} = 2.5V+5%
Common output current	$I_{DD\_CM\_3.3V}$	—	13.44	15.05	mA	V_{DDO} = 3.3V+5%
	$I_{DD\_CM\_2.5V}$	—	12.18	13.65	mA	V_{DDO} = 2.5V+5%
Dynamic LVCMOS output current (f = 100 MHz) Needs to be scaled for different frequencies by f/100 MHz	$I_{DD\_3.3V}$	—	2.38	2.68	mA	V_{DDO} = 3.3V+5%
	$I_{DD\_2.5V}$	—	1.74	1.96	mA	V_{DDO} = 2.5V+5%
Current dissipation per LVPECL output	$I_{DD\_LVPECL\_3.3V}$	—	19.36	23.26	mA	V_{DDO} = 3.3V+5%
	$I_{DD\_LVPECL\_2.5V}$	—	19.38	22.17	mA	V_{DDO} = 2.5V+5%
Current dissipation per LVDS output	$I_{DD\_LVDS\_3.3V}$	—	6.73	8.00	mA	V_{DDO} = 3.3V+5%
	$I_{DD\_LVDS\_2.5V}$	—	6.87	7.83	mA	V_{DDO} = 2.5V+5%
Current dissipation per HCSL output	$I_{DD\_HCSL\_3.3V}$	—	16.43	19.87	mA	V_{DDO} = 3.3V+5%
	$I_{DD\_HCSL\_2.5V}$	—	17.14	19.18	mA	V_{DDO} = 2.5V+5%

TABLE 4.4: INPUT CHARACTERISTICS

Note 1, Note 2, Note 3

Parameter	Symbol	Min.	Typ.	Max.	Units.	Condition.
CMOS high-level input voltage for control inputs	V_{CIH}	1.05	—	—	V	—
CMOS low-level input voltage for control inputs	V_{CIL}	—	—	0.45	V	—
CMOS input leakage current for control inputs (includes current due to pull-down resistors)	I_{IL}	–25	—	50	µA	$V_I = V_{DD}$ or 0V
Differential input common mode voltage for IN0_p/n and IN1_p/n	V_{CM}	1	—	2	V	—
Differential input voltage difference for IN0_p/n and IN1_p/n, f ≤1 GHz (Note 4)	V_{ID}	0.15	—	1.3	V	—
Differential input voltage difference for IN0_p/n and IN1_p/n for 1 GHz < f ≤ 1.6 GHz (Note 4)	V_{ID}	0.35	—	1.3	V	—
Differential input leakage current for IN0_p/n and IN1_p/n (includes current due to pull-up and pull-down resistors)	I_{IL}	–150	—	150	µA	V_I = 2V or 0V
Single-ended input voltage for IN0_p and IN1_p	V_{SI}	–0.3	—	2.7	V	V_{DD} = 3.3V or 2.5V
Single-ended input common mode voltage (IN0_p/n and IN1_p/n)	V_{SIC}	1	—	2	V	V_{DD} = 3.3V or 2.5V
Single-ended input voltage swing for IN0_p and IN1_p	V_{SID}	0.3	—	1.3	V	V_{DD} = 3.3V or 2.5V
Input frequency (differential)	f_{IN}	0	—	1600	MHz	—
Input frequency (LVCMOS)	f_{IN_CMOS}	0	—	250	MHz	—
Input duty cycle	dc	35%	—	65%	—	—
Input slew rate	Slew	—	2	—	V/ns	—
Input pull-up/ pull-down resistance	R_{PU}/R_{PD}	—	60	—	kΩ	—
Input pull-down resistance for INx_p	R_{PD}	—	30	—	kΩ	—
Input multiplexer isolation IN0_p/n to IN1_p/n and vice versa Power on both inputs 0 dBm, f_{OFFSET} > 50 kHz	I_{SO}	—	–84	—	dBc	f_{IN} = 100 MHz
		—	–82	—		f_{IN} = 200 MHz
		—	–71	—		f_{IN} = 400 MHz
		—	–67	—		f_{IN} = 800 MHz

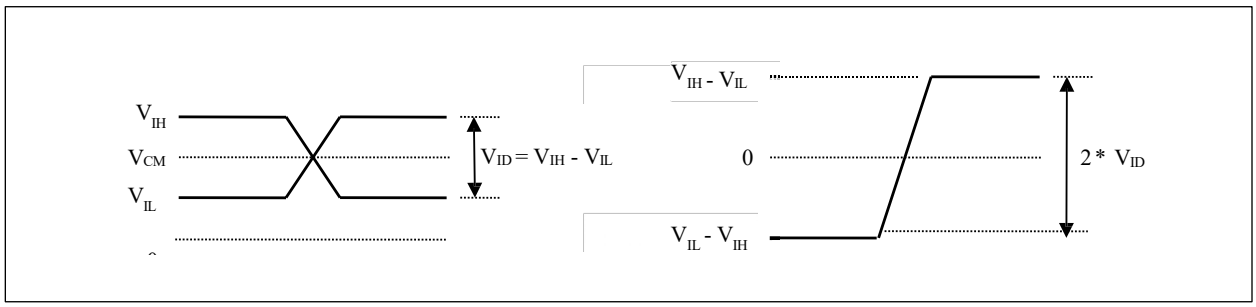


FIGURE 4.1: Differential Input Voltage Levels.

Note 1: Values are over recommended operating conditions.

Note 2: Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V).

Note 3: Input mux isolation is measured as amplitude of f_{OFFSET} spur in dBc on the output clock phase noise plot.

Note 4: Input differential voltage is calculated as $V_{ID} = V_{IH} – V_{IL}$ where V_{IH} and V_{IL} are input voltage high and low respectively. It should not be confused with $V_{ID} = 2 \times (V_{IH} – V_{IL})$ used in some data sheets. Please refer to Figure 4-1.

TABLE 4.5: CRYSTAL OSCILLATOR CHARACTERISTICS

Note 1, Note 2

Parameter	Symbol	Min.	Typ.	Max.	Units.	Condition.
Mode of oscillation	Mode		Fundamental		—	—
Frequency	f	8	—	160	MHz	—
On chip load capacitance	C_L	—	1	—	pF	—
On chip series resistor	R_S	—	0	—	Ω	—
On chip shunt resistor	R	—	500	—	kΩ	—
Frequency in overdrive mode Note 3	f_{OV}	0.1	—	250	MHz	Functional but may not meet AC parameters Minimum depends on AC coupling Capacitor (0.1 µF assumed)
Frequency in bypass mode Note 4	f_{BP}	0	—	250	MHz	Functional but may not meet AC parameters

Note 1: Values are over recommended operating conditions.
Note 2: Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V).
Note 3: Maximum input level is 2V.
Note 4: Maximum output level is V_{DD}.

TABLE 4.6: POWER SUPPLY REJECTION RATIO FOR V_{DD} = V_{DDO} = 3.3V

Note 1, Note 2, Note 3

Parameter	Symbol	Min.	Typ.	Max.	Units.	Condition.
PSRR for LVPECL output	$PSRR_{LVPECL}$	—	–71.75	—	dBc	f_{IN} = 156.25 MHz
			–84.45			f_{IN} = 312.5 MHz
			–82.11			f_{IN} = 625 MHz
PSRR for LVDS output	$PSRR_{LVDS}$	—	–95.16	—	dBc	f_{IN} = 156.25 MHz
			–97.77			f_{IN} = 312.5 MHz
			–79.23			f_{IN} = 625 MHz
PSRR for HCSL output	$PSRR_{HCSL}$	—	–77.15	—	dBc	f_{IN} = 100 MHz
			–76.75			f_{IN} = 156.25 MHz
			–80.44			f_{IN} = 312.5 MHz

Note 1: Values are over recommended operating conditions.
Note 2: Noise injected to VDDO power supply with frequency 100 kHz and amplitude 100 mVpp.
Note 3: PSRR is measured as amplitude of 100 kHz spur in dBc on the output clock phase noise plot.

TABLE 4.7: POWER SUPPLY REJECTION RATIO FOR VDD = VDDO = 2.5V

Note 1, Note 2, Note 3

Parameter	Symbol	Min.	Typ.	Max.	Units.	Condition.
PSRR for LVPECL output	$PSRR_{LVPECL}$	—	–73.68	—	dBc	f_{IN} = 156.25 MHz
			–78.88			f_{IN} = 312.5 MHz
			–71.82			f_{IN} = 625 MHz
PSRR for LVDS output	$PSRR_{LVDS}$	—	–90.04	—	dBc	f_{IN} = 156.25 MHz
			–79.99			f_{IN} = 312.5 MHz
			–73.45			f_{IN} = 625 MHz
PSRR for HCSL output	$PSRR_{HCSL}$	—	–92.16	—	dBc	f_{IN} = 100 MHz
			–74.08			f_{IN} = 156.25 MHz
			–91.88			f_{IN} = 312.5 MHz

Note 1: Values are over recommended operating conditions.
Note 2: Noise injected to VDDO power supply with frequency 100 kHz and amplitude 100 mVpp.
Note 3: PSRR is measured as amplitude of 100 kHz spur in dBc on the output clock phase noise plot.

TABLE 4.8: LVCMOS OUTPUT CHARACTERISTICS FOR V_{DDO} = 3.3V

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units.	Condition.
Output high voltage (1 mA load)	V_{OH}	V_{DDO} – 0.1	—	—	V	DC measurement
Output low voltage (1 mA load)	V_{OL}	—	—	0.1	V	DC measurement
Output High Current (Load adjusted to $V_{OUT} = V_{DDO}/2$)	I_{OH}	—	30	—	mA	DC measurement
Output Low Current (Load adjusted to $V_{OUT} = V_{DDO}/2$)	I_{OL}	—	34	—	mA	DC measurement
Output impedance	R_O	—	15	—	Ω	DC measurement
Rise time (20% to 80%)	t_R	—	220	310	ps	—
Fall time (20% to 80%)	t_F	—	320	365	ps	—
Output frequency	f_O	0	—	250	MHz	—
Input to output delay	t_{IOD}	1.07	1.28	2.07	ns	—
Output enable time	t_{EN}	—	—	3	cycles	—
Output disable time	t_{DIS}	—	—	3	cycles	—
Additive RMS jitter in 1 MHz to 5 MHz band	$T_{j\_1M\_5M}$	—	46	80	fs	Input Clock 25 MHz
Additive RMS jitter in 12 kHz to 5 MHz band	$t_{j\_12K\_5M}$	—	56	90	fs	Input Clock 25 MHz
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	60	79	fs	Input Clock 125 MHz
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	65	86	fs	Input Clock 125 MHz
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	61	94	fs	Input Clock 156.25
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	66	100	fs	Input Clock 156.25
Noise Floor	NF	—	–165	–162	dBc/Hz	Input clock: 25 MHz
		—	–160	–156		Input clock: 125 MHz
		—	–158	–153		Input clock: 156.25

Note 1: Values are over recommended operating conditions.

TABLE 4.9: LVCMOS OUTPUT CHARACTERISTICS FOR V_{DDO} = 2.5V

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units.	Condition.
Output high voltage (1 mA load)	V_{OH}	V_{DDO} – 0.1	—	—	V	DC measurement
Output low voltage (1 mA load)	V_{OL}	—	—	0.1	V	DC measurement
Output High Current (Load adjusted to $V_{OUT} = V_{DDO}/2$)	I_{OH}	—	21	—	mA	DC measurement
Output Low Current (Load adjusted to $V_{OUT} = V_{DDO}/2$)	I_{OL}	—	25	—	mA	DC measurement
Output impedance	R_O	—	15	—	Ω	DC measurement
Rise time (20% to 80%)	t_R	—	225	310	ps	—
Fall time (20% to 80%)	t_F	—	320	365	ps	—
Output frequency	f_O	0	—	250	MHz	—
Input to output delay	t_{IOD}	1.10	1.28	2.30	ns	—
Output enable time	t_{EN}	—	—	3	cycles	—
Output disable time	t_{DIS}	—	—	3	cycles	—
Additive RMS jitter in 1 MHz to 5 MHz band	$T_{j\_1M\_5M}$	—	51	104	fs	Input Clock 25 MHz
Additive RMS jitter in 12 kHz to 5 MHz band	$t_{j\_12K\_5M}$	—	62	111	fs	Input Clock 25 MHz
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	64	81	fs	Input Clock 125 MHz
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	70	88	fs	Input Clock 125 MHz
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	62	94	fs	Input Clock 156.25
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	68	100	fs	Input Clock 156.25
Noise Floor	NF	—	–164	–161	dBc/Hz	Input clock: 25 MHz
		—	–159	–155		Input clock: 125 MHz
		—	–158	–153		Input clock: 156.25

Note 1: Values are over recommended operating conditions.

TABLE 4.10: LVPECL OUTPUT CHARACTERISTICS FOR VDDO = 3.3V

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units.	Condition.
Output high voltage	V_{LVPECL_OH}	1.9	2.08	2.4	V	DC Measurement
Output low voltage	V_{LVPECL_OL}	1.2	1.36	1.7	V	DC Measurement
Output differential swing (Note 2)	V_{LVPECL_SW}	0.6	0.72	0.9	V	DC Measurement
Variation of V_{LVPECL_SW} for com-plementary output states	ΔV_{LVPECL_SW}	0	0.02	0.07	V	—
Common mode output	V_{CM}	1.6	1.72	2.1	V	—
Output frequency when $V_{LVPECL\_SW} \geq 0.6V$	$f_{MAX\_0.6VSW}$	—	—	800	MHz	—
Output frequency when $V_{LVPECL\_SW} \geq 0.4V$	$f_{MAX\_0.4VSW}$	—	—	1600	MHz	—
Rise or fall time (20% to 80%)	t_R/t_F	—	110	170	ps	—
Output frequency	f_O	0	—	1600	MHz	—
Output to output skew	t_{OOSK}	—	—	40	ps	—
Device to device output skew	t_{DOOSK}	—	—	120	ps	—
Input to output delay	t_{IOD}	0.73	0.87	1.1	ns	—
Output enable time	t_{EN}	—	—	3	cycles	—
Output disable time	t_{DIS}	—	—	3	cycles	—
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	68	96	fs	Input clock: 100 MHz
		—	50	64	fs	Input clock: 156.25 MHz
		—	20	32	fs	Input clock: 625 MHz
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	71	101	fs	Input clock: 100 MHz
		—	55	70	fs	Input clock: 156.25 MHz
		—	25	39	fs	Input clock: 625 MHz
Noise floor	N_F	—	–161	–159	dBc/Hz	Input clock: 100 MHz
		—	–160	–155	dBc/Hz	Input clock: 156.25 MHz
		—	–155	–151	dBc/Hz	Input clock: 625 MHz

Note 1: Values are over recommended operating conditions.

Note 2: Output differential swing is calculated as $V_{SW} = V_{OH} – V_{OL}$. It should not be confused with $V_{SW} = 2 \times (V_{OH} – V_{OL})$ used in some data sheets. Please refer to Figure 4-2.

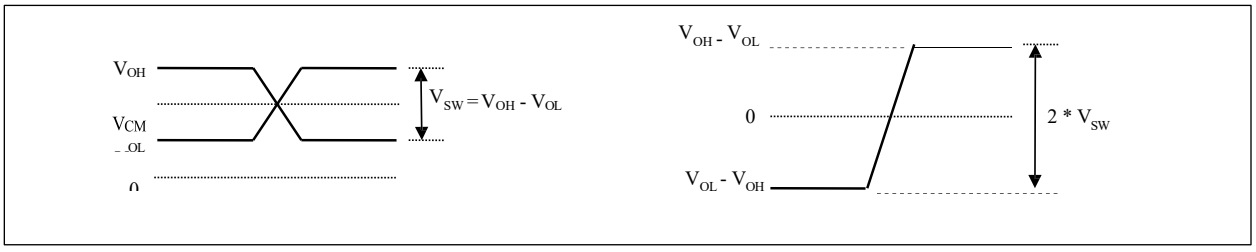


FIGURE 4.2: Differential Output Voltage Levels

TABLE 4.11: LVPECL OUTPUT CHARACTERISTICS FOR V_{DDO} = 2.5V

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units.	Condition.
Output high voltage	V_{LVPECL_OH}	1.1	1.28	1.7	V	DC Measurement
Output low voltage	V_{LVPECL_OL}	0.4	0.57	0.9	V	DC Measurement
Output differential swing (Note 2)	V_{LVPECL_SW}	0.6	0.71	0.9	V	DC Measurement
Variation of V_{LVPECL_SW} for com-plementary output states	ΔV_{LVPECL_SW}	0	0.02	0.05	V	—
Common mode output	V_{CM}	0.8	0.92	1.2	V	—
Output frequency when $V_{LVPECL\_SW} \geq 0.6V$	$f_{MAX\_0.6VSW}$	—	—	800	MHz	—
Output frequency when $V_{LVPECL\_SW} \geq 0.4V$	$f_{MAX\_0.4VSW}$	—	—	1600	MHz	—
Rise or fall time (20% to 80%)	t_R/t_F	—	120	170	ps	—
Output frequency	f_O	—	—	1600	MHz	—
Output to output skew	t_{OOSK}	—	—	40	ps	—
Device to device output skew	t_{DOOSK}	—	—	120	ps	—
Input to output delay	t_{IOD}	0.75	0.87	1.1	ns	—
Output enable time	t_{EN}	—	—	3	cycles	—
Output disable time	t_{DIS}	—	—	3	cycles	—
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	65	91	fs	Input clock: 100 MHz
		—	50	64	fs	Input clock: 156.25 MHz
		—	20	30	fs	Input clock: 625 MHz
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	69	99	fs	Input clock: 100 MHz
		—	54	75	fs	Input clock: 156.25 MHz
		—	26	41	fs	Input clock: 625 MHz
Noise floor	N_F	—	–161	–159	dBc/Hz	Input clock: 100 MHz
		—	–160	–155	dBc/Hz	Input clock: 156.25 MHz
		—	–155	–151	dBc/Hz	Input clock: 625 MHz

Note 1: Values are over recommended operating conditions.

Note 2: Output differential swing is calculated as $V_{SW} = V_{OH} – V_{OL}$. It should not be confused with $V_{SW} = 2 \times (V_{OH} – V_{OL})$ used in some data sheets. Please refer to Figure 4-2.

TABLE 4.12: LVDS OUTPUTS FOR VDDO = 3.3V

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units.	Condition.
Output high voltage	V_{LVDS_OH}	1.3	1.39	1.47	V	DC Measurement
Output low voltage	V_{LVDS_OL}	1.0	1.07	1.15	V	DC Measurement
Output differential swing (Note 2)	V_{LVDS_SW}	0.25	0.32	0.39	V	DC Measurement
Variation of V_{LVDS_SW} for comple-mentary output states	ΔV_{LVDS_SW}	0	0.002	0.01	V	—
Common mode output	V_{CM}	1.15	1.23	1.3	V	—
Variation of V_{CM} for complementary output states	ΔV_{CM}	0	0.001	0.01	V	—
Output frequency when $V_{LVDS\_SW} \geq 250$ mV	$f_{MAX\_0.25VSW}$	—	—	800	MHz	—
Output frequency when $V_{LVDS\_SW} \geq 200$ mV	$f_{MAX\_0.2VSW}$	—	—	1600	MHz	—
Rise or fall time (20% to 80%)	t_R/t_F	—	110	170	ps	—
Output frequency	f_O	0	—	1600	MHz	—
Output to output skew	t_{OOSK}	—	—	20	ps	—
Device to device output skew	t_{DOOSK}	—	—	130	ps	—
Input to output delay	t_{IOD}	0.76	0.86	1.1	ns	—
Output Short Circuit Current Single-Ended	I_S	–24	—	24	mA	Single-ended outputs
Output Short Circuit Current Differ-ential	I_{SD}	–24	—	24	mA	Complementary outputs
Output enable time	t_{EN}	—	—	3	cycles	—
Output disable time	t_{DIS}	—	—	3	cycles	—
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	110	144	fs	Input clock: 100 MHz
		—	63	81	fs	Input clock: 156.25 MHz
		—	21	33	fs	Input clock: 625 MHz
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	115	150	fs	Input clock: 100 MHz
		—	73	102	fs	Input clock: 156.25 MHz
		—	26	40	fs	Input clock: 625 MHz
Noise floor	N_F	—	–158	–156	fs	Input clock: 100 MHz
		—	–158	–155	fs	Input clock: 156.25 MHz
		—	–154	–151	fs	Input clock: 625 MHz

Note 1: Values are over recommended operating conditions.

Note 2: Output differential swing is calculated as $V_{SW} = V_{OH} – V_{OL}$. It should not be confused with $V_{SW} = 2 \times (V_{OH} – V_{OL})$ used in some data sheets. Please refer to Figure 4-2.

TABLE 4.13: LVDS OUTPUTS FOR VDDO = 2.5V

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units.	Condition.
Output high voltage	V_{LVDS_OH}	1.3	1.4	1.5	V	DC Measurement
Output low voltage	V_{LVDS_OL}	0.97	1.05	1.13	V	DC Measurement
Output differential swing (Note 2)	V_{LVDS_SW}	0.25	0.35	0.44	V	DC Measurement
Variation of V_{LVDS_SW} for comple-mentary output states	ΔV_{LVDS_SW}	0	0.001	0.01	V	—
Common mode output	V_{CM}	1.15	1.23	1.3	V	—
Variation of V_{CM} for complementary output states	ΔV_{CM}	0	0.001	0.01	V	—
Output frequency when $V_{LVDS\_SW} \geq 250$ mV	$f_{MAX\_0.25VSW}$	—	—	800	MHz	—
Output frequency when $V_{LVDS\_SW} \geq 200$ mV	$f_{MAX\_0.2VSW}$	—	—	1600	MHz	—
Rise or fall time (20% to 80%)	t_R/t_F	—	110	170	ps	—
Output frequency	f_O	0	—	1600	MHz	—
Output to output skew	t_{OOSK}	—	—	20	ps	—
Device to device output skew	t_{DOOSK}	—	—	130	ps	—
Input to output delay	t_{IOD}	0.78	0.86	1.12	ns	—
Output Short Circuit Current Single-Ended	I_S	–24	—	24	mA	Single-ended outputs shorted to GND
Output Short Circuit Current Differ-ential	I_{SD}	–24	—	24	mA	Complementary outputs shorted
Output enable time	t_{EN}	—	—	3	cycles	—
Output disable time	t_{DIS}	—	—	3	cycles	—
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	107	140	fs	Input clock: 100 MHz
		—	62	77	fs	Input clock: 156.25 MHz
		—	20	31	fs	Input clock: 625 MHz
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	111	146	fs	Input clock: 100 MHz
		—	66	83	fs	Input clock: 156.25 MHz
		—	24	36	fs	Input clock: 625 MHz
Noise floor	N_F	—	–158	–156	fs	Input clock: 100 MHz
		—	–159	–155	fs	Input clock: 156.25 MHz
		—	–155	–151	fs	Input clock: 625 MHz

Note 1: Values are over recommended operating conditions.

Note 2: Output differential swing is calculated as $V_{SW} = V_{OH} – V_{OL}$. It should not be confused with $V_{SW} = 2 \times (V_{OH} – V_{OL})$ used in some data sheets. Please refer to Figure 4-2.

TABLE 4.14: HCSL OUTPUTS FOR V_{DDO} = 3.3V

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units.	Condition.
Output high voltage	V_{HCSL_OH}	0.6	0.85	1.1	V	DC Measurement
Output low voltage	V_{HCSL_OL}	–0.05	0	0.05	V	DC Measurement
Output differential swing (Note 2)	V_{HCSL_SW}	0.6	0.85	1.1	V	DC Measurement
Variation of V_{HCSL_SW} for comple-mentary output states	ΔV_{HCSL_SW}	0	0.003	0.05	V	—
Common mode output	V_{CM}	0.28	0.43	0.55	V	—
Variation of V_{CM} for complementary output states	ΔV_{CM}	0	0.002	0.05	V	—
Absolute Crossing Voltage	V_{CROSS}	0.320	0.384	0.447	V	—
Total Variation of V_{CROSS}	ΔV_{CROSS}	—	—	0.127	V	—
Output frequency	f_{MAX}	0	—	400	MHz	—
Rise or fall time (20% to 80%)	t_R/t_F	—	143	309	ps	—
Output to output skew	t_{OOSK}	—	—	21	ps	—
Device to device output skew	t_{DOOSK}	—	—	129	ps	—
Input to output delay	t_{IOD}	0.73	0.90	1.08	ns	—
Output enable time	t_{EN}	—	—	3	cycles	—
Output disable time	t_{DIS}	—	—	3	cycles	—
Additive Jitter as per PCIe 3.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$t_{jPCIe\_3.0}$	—	20	40	fs	Input clock: 100 MHz
Additive Jitter as per PCIe 4.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$t_{jPCIe\_4.0}$	—	20	40	fs	Input clock: 100 MHz
Additive Jitter as per PCIe 5.0 (PLL_BW = 0.5 MHz to 1.8 MHz, CDR for 32 GT/s CC)	$t_{jPCIe\_5.0}$	—	13	19	fs	Input clock: 100 MHz
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	73	104	fs	Input clock: 100 MHz
		—	53	69	fs	Input clock: 156.25 MHz
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	77	112	fs	Input clock: 100 MHz
		—	64	100	fs	Input clock: 156.25 MHz
Noise floor	N_F	—	–161	–159	dBc/Hz	Input clock: 100 MHz
		—	–159	–155	dBc/Hz	Input clock: 156.25 MHz

Note 1: Values are over recommended operating conditions.

Note 2: Output differential swing is calculated as $V_{SW} = V_{OH} – V_{OL}$. It should not be confused with $V_{SW} = 2 \times (V_{OH} – V_{OL})$ used in some data sheets. Please refer to Figure 4-2.

TABLE 4.15: HCSL OUTPUTS FOR V_{DDO} = 2.5V

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units.	Condition.
Output high voltage	V_{HCSL_OH}	0.6	0.83	1.1	V	DC Measurement
Output low voltage	V_{HCSL_OL}	–0.05	0	0.05	V	DC Measurement
Output differential swing (Note 2)	V_{HCSL_SW}	0.6	0.83	1.1	V	DC Measurement
Variation of V_{HCSL_SW} for comple-mentary output states	ΔV_{HCSL_SW}	0	0.003	0.05	V	—
Common mode output	V_{CM}	0.28	0.42	0.55	V	—
Variation of V_{CM} for complementary output states	ΔV_{CM}	0	0.002	0.05	V	—
Absolute Crossing Voltage	V_{CROSS}	0. 260	0.316	0.372	V	—
Total Variation of V_{CROSS}	ΔV_{CROSS}	—	—	0.108	V	—
Output frequency	f_{MAX}	0	—	400	MHz	—
Rise or fall time (20% to 80%)	t_R/t_F	—	125	162	ps	—
Output to output skew	t_{OOSK}	—	—	21	ps	—
Device to device output skew	t_{DOOSK}	—	—	129	ps	—
Input to output delay	t_{IOD}	0.76	0.92	1.10	ns	—
Output enable time	t_{EN}	—	—	3	cycles	—
Output disable time	t_{DIS}	—	—	3	cycles	—
Additive Jitter as per PCIe 3.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$t_{jPCIe\_3.0}$	—	20	40	fs	Input clock: 100 MHz
Additive Jitter as per PCIe 4.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$t_{jPCIe\_4.0}$	—	20	40	fs	Input clock: 100 MHz
Additive Jitter as per PCIe 5.0 (PLL_BW = 0.5 MHz to 1.8 MHz, CDR for 32 GT/s CC)	$t_{jPCIe\_5.0}$	—	13	19	fs	Input clock: 100 MHz
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	68	95	fs	Input clock: 100 MHz
		—	52	66	fs	Input clock: 156.25 MHz
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	72	102	fs	Input clock: 100 MHz
		—	56	71	fs	Input clock: 156.25 MHz
Noise floor	N_F	—	–161	–158	dBc/Hz	Input clock: 100 MHz
		—	–160	–153	dBc/Hz	Input clock: 156.25 MHz

Note 1: Values are over recommended operating conditions.

Note 2: Output differential swing is calculated as $V_{SW} = V_{OH} – V_{OL}$. It should not be confused with $V_{SW} = 2 x (V_{OH} – V_{OL})$ used in some data sheets. Please refer to Figure 4-2.

TABLE 4.16: LVCMOS OUTPUT PHASE NOISE WITH 25 MHZ XTAL

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units.	Condition.
Jitter RMS in 12 kHz to 5 MHz band	$t_{j\_12k\_5M}$	—	103	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	117	—		V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise floor	NF	—	–75	—	dBc/Hz	V_{DD} = 3.3V, V_{DDO} = 3.3V @10 Hz
		—	–107	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 Hz
		—	–132	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 kHz
		—	–150	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 kHz
		—	–162	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 kHz
		—	–166	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 MHz
		—	–166	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @5 MHz
		—	–70	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 Hz
		—	–102	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 Hz
		—	–130	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 kHz
		—	–149	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 kHz
		—	–161	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 kHz
		—	–165	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 MHz
		—	–165	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @5 MHz

Note 1: Values are over recommended operating conditions.

TABLE 4.17: LVPECL OUTPUT PHASE NOISE WITH 25 MHZ XTAL

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units.	Condition.
Jitter RMS in 12 kHz to 5 MHz band	$t_{j\_12k\_5M}$	—	265	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	213	—		V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise floor	NF	—	–75	—	dBc/Hz	V_{DD} = 3.3V, V_{DDO} = 3.3V @10 Hz
		—	–107	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 Hz
		—	–133	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 kHz
		—	–152	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 kHz
		—	–157	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 kHz
		—	–158	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 MHz
		—	–157	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @5 MHz
		—	–71	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 Hz
		—	–103	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 Hz
		—	–130	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 kHz
		—	–151	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 kHz
		—	–158	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 kHz
		—	–160	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 MHz
		—	–159	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @5 MHz

Note 1: Values are over recommended operating conditions.

TABLE 4.18: LVDS OUTPUT PHASE NOISE WITH 25 MHZ XTAL

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units.	Condition.
Jitter RMS in 12 kHz to 5 MHz band	$t_{j\_12k\_5M}$	—	178	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	190	—		V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise floor	NF	—	–75	—	dBc/Hz	V_{DD} = 3.3V, V_{DDO} = 3.3V @10 Hz
		—	–107	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 Hz
		—	–133	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 kHz
		—	–154	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 kHz
		—	–161	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 kHz
		—	–161	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 MHz
		—	–160	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @5 MHz
		—	–68	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 Hz
		—	–103	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 Hz
		—	–130	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 kHz
		—	–152	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 kHz
		—	–161	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 kHz
		—	–160	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 MHz
		—	–159	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @5 MHz

Note 1: Values are over recommended operating conditions.

TABLE 4.19: HCSL OUTPUT PHASE NOISE WITH 25 MHZ XTAL

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units.	Condition.
Jitter RMS in 12 kHz to 5 MHz band	$t_{j\_12k\_5M}$	—	269	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	228	—		V_{DD} = 2.5V, V_{DDO} = 2.5V
Noise floor	NF	—	–76	—	dBc/Hz	V_{DD} = 3.3V, V_{DDO} = 3.3V @10 Hz
		—	–107	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 Hz
		—	–133	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 kHz
		—	–152	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @10 kHz
		—	–157	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @100 kHz
		—	–157	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @1 MHz
		—	–157	—		V_{DD} = 3.3V, V_{DDO} = 3.3V @5 MHz
		—	–73	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 Hz
		—	–105	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 Hz
		—	–131	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 kHz
		—	–151	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @10 kHz
		—	–158	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @100 kHz
		—	–159	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @1 MHz
		—	–159	—		V_{DD} = 2.5V, V_{DDO} = 2.5V @5 MHz

Note 1: Values are over recommended operating conditions.

THERMAL SPECIFICATIONS

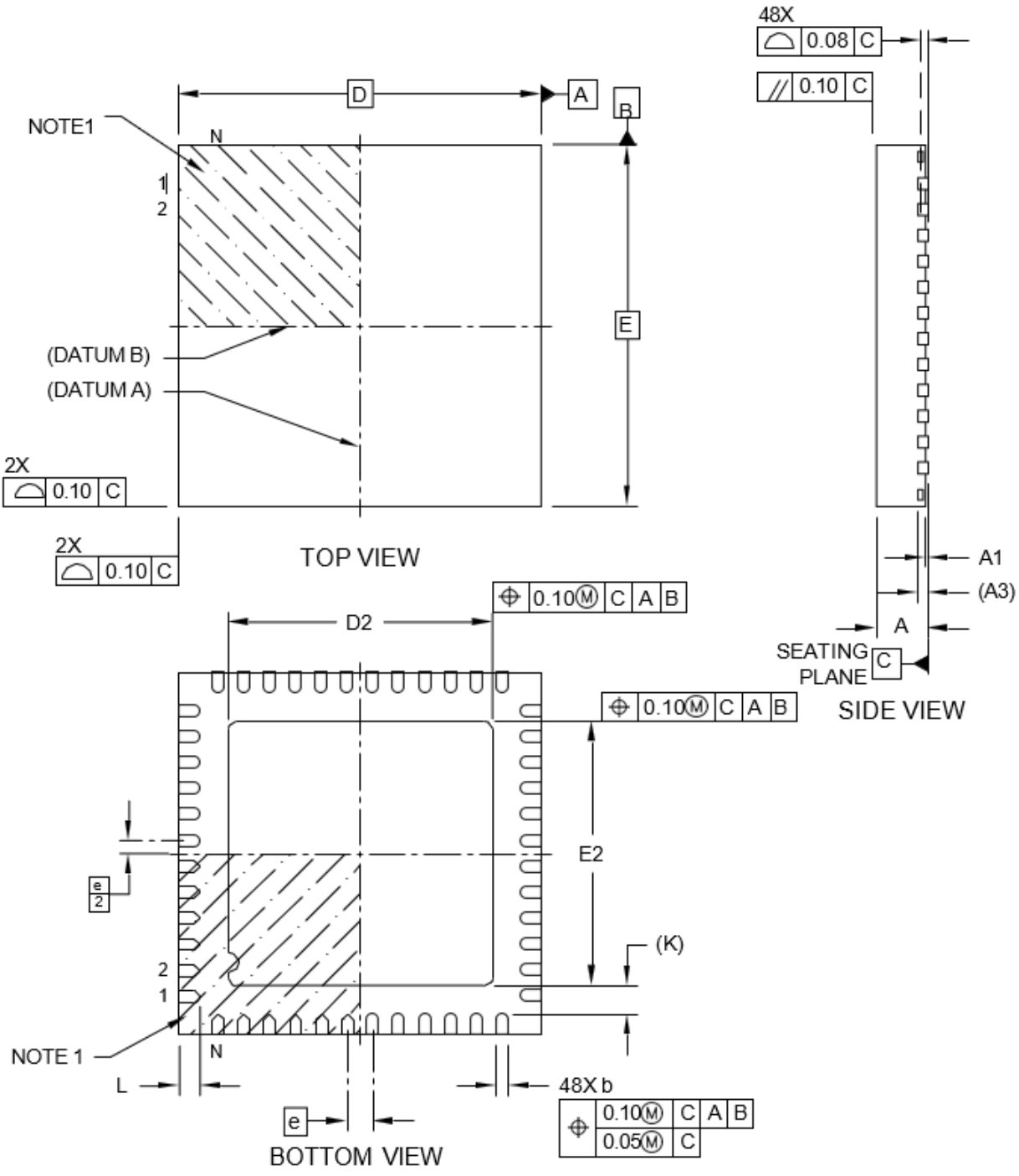
Parameter	Symbol	Condition.	Value	Units.
Maximum Ambient Temperature	T_A	—	85	°C
Maximum Junction Temperature	$T_{J(MAX)}$	—	125	°C
Package Thermal Resistance, 7x7 VQFN 48-Lead				
Junction to Ambient Thermal Resistance Note 1	θ_{JA}	Still air	21.1	°C/W
		1m/s airflow	16.6	°C/W
		2.5 m/s airflow	15.0	°C/W
Junction to Board Thermal Resistance	θ_{JB}	—	6.9	°C/W
Junction to Case Thermal Resistance	θ_{JC}	—	12.8	°C/W
Junction to Pad Thermal Resistance Note 2	θ_{JP}	Still air	3.9	°C/W
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	Still air	0.2	°C/W

Note 1: Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on an 4-layer JEDEC standard test board and dissipating maximum power.

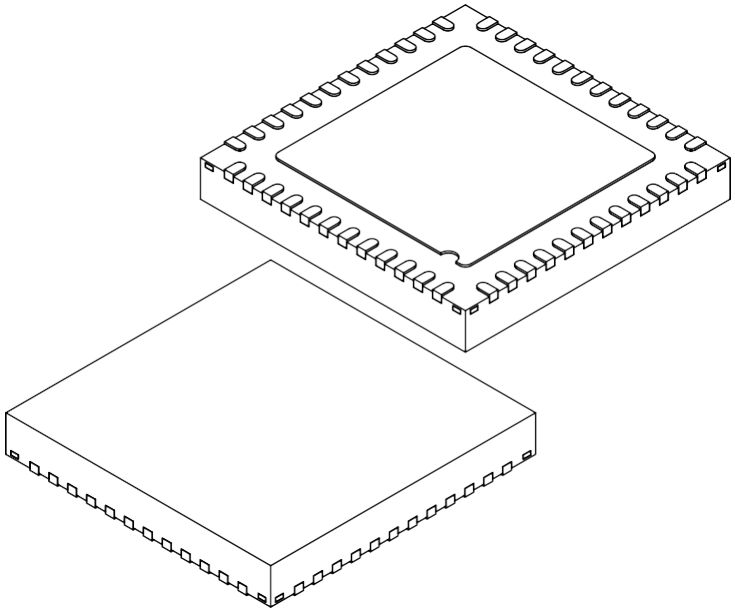
Note 2: Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package).

5.0 PACKAGE OUTLINE

48-Lead Very Thin Plastic Quad Flat, No Lead Package (MAC) - 7x7x1 mm Body [VQFN] With 5.1 mm Exposed Pad Package



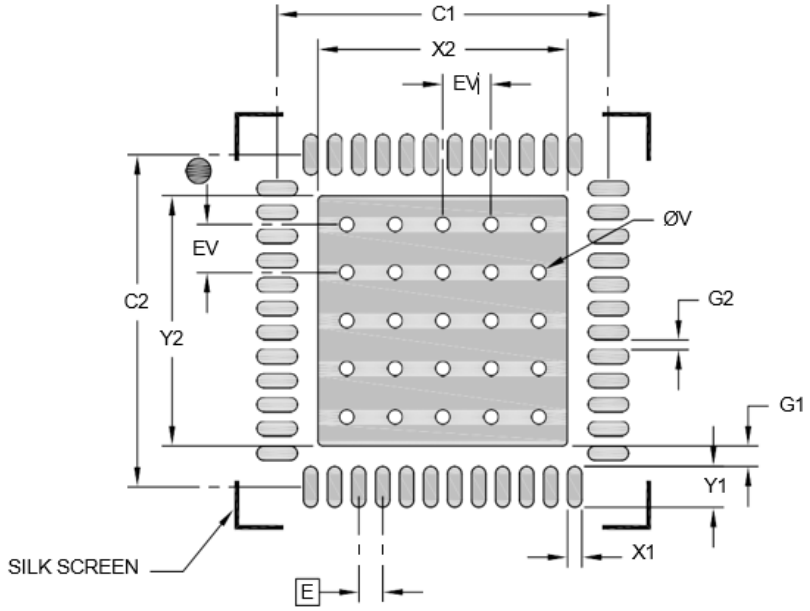
48-Lead Very Thin Plastic Quad Flat, No Lead Package (MAC) - 7x7x1 mm Body [VQFN] With 5.1 mm Exposed Pad Package



Units		Millimeters		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		48	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		7.00 BSC	
Exposed Pad Length	D2	5.00	5.10	5.20
Overall Width	E		7.00 BSC	
Exposed Pad Width	E2	5.00	5.10	5.20
Terminal Width	b	0.16	0.23	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.55 REF	

Note 1: Pin 1 visual index feature may vary, but must be located within the hatched area.
Note 2: Package is saw singulated
Note 3: Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

48-Lead Very Thin Plastic Quad Flat, No Lead Package (MAC) - 7x7x1 mm Body [VQFN] With 5.1 mm Exposed Pad Package



RECOMMENDED LAND PATTERN

Units		Millimeters		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			5.20
Optional Center Pad Length	Y2			5.20
Contact Pad Spacing	C1		6.90	
Contact Pad Spacing	C2		6.90	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.85
Contact Pad to Center Pad (Xnn)	G1	0.43		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Note 1: Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Note 2: For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process