Product Change Notification: SYST-07UAYP263

Date:

09-Jul-2026

Product Category:

Memory

Notification Subject:

Data Sheet - SST26VF016BEUI - 16-Mbit Serial Quad I/O™ (SQI™) Flash Memory with EUI-48 and EUI-64 Identifier

Affected CPNs:

SYST-07UAYP263_Affected_CPN_07092026.pdf
SYST-07UAYP263_Affected_CPN_07092026.csv

Notification Text:

SYST-07UAYP263
Microchip has released a new Datasheet for the SST26VF016BEUI - 16-Mbit Serial Quad I/O™ (SQI™) Flash Memory with EUI-48 and EUI-64 Identifier of devices. If you are using one of these devices please read the document located at **SST26VF016BEUI - 16-Mbit Serial Quad I/O™ (SQI™) Flash Memory with EUI-48 and EUI-64 Identifier**. **Notification Status:** Final **Description of Change:** Replaced incorrect packaging diagram with C04-00057 diagram; Editorial updates throughout the document. **Impacts to Data Sheet:** See above details **Reason for Change:** To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 09 Jul 2026

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

SST26VF016BEUI - 16-Mbit Serial Quad I/O™ (SQI™) Flash Memory with EUI-48 and EUI-64 Identifier

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Affected Catalog Part Numbers (CPN)

SST26VF016BEUI-104I/SN

SST26VF016BEUIT-104I/SN

SST26VF016BEUI

16-Mbit Serial Quad I/O™ (SQI™) Flash Memory with EUI-48 and EUI-64 Identifier

Features

- Factory-Programmed with EUI-48 and EUI-64 Globally Unique Identifier:
  - Secure, read-only access in Serial Flash Discoverable Parameter (SFDP) table
- Single Voltage Read and Write Operations:
  - 2.7V to 3.6V or 2.3V to 3.6V
- Serial Interface Architecture:
  - Nibble-wide multiplexed I/O's with SPI-like serial command structure:
    - Mode 0 and Mode 3
  - x1/x2/x4 Serial Peripheral Interface (SPI) Protocol
- High-Speed Clock Frequency:
  - 2.7V to 3.6V: 104 MHz maximum
  - 2.3V to 3.6V: 80 MHz maximum
- Burst Modes:
  - Continuous linear burst
  - 8/16/32/64 bytes linear burst with wrap-around
- Superior Reliability:
  - Endurance: 100,000 cycles (minimum)
  - Greater than 100 years data retention
- Low-Power Consumption:
  - Active Read current: 15 mA (typical @ 104 MHz)
  - Standby current: 15 µA (typical)
- Fast Erase Time:
  - Sector/Block Erase: 18 s (typical), 25 ms (maximum)
  - Chip Erase: 35 ms (typ), 50 ms (maximum)
- Page Program:
  - 256 bytes per page in x1 or x4 mode
- End-of-Write Detection:
  - Software polling the BUSY bit in STATUS register
- Flexible Erase Capability:
  - Uniform 4-Kbyte sectors
  - Four 8-Kbyte top and bottom parameter overlay blocks
  - One 32-Kbyte top and bottom overlay block
  - Uniform 64-Kbyte overlay blocks
- Write Suspend:
  - Suspend Program or Erase operation to access another block/sector
- Software Reset (RST) mode
- Software Write Protection:
  - Individual Block Write Protection with permanent lock-down capability:
    - 64-Kbyte blocks, two 32-Kbyte blocks and eight 8-Kbyte parameter blocks
  - Read Protection on top and bottom 8-Kbyte parameter blocks
- Security ID:
  - One-Time-Programmable (OTP) 2-Kbyte, Secure ID:
    - 64-bit unique, factory pre-programmed identifier
    - User-programmable area
- Temperature Range:
  - Industrial: -40°C to +85°C
- AEC Q-100 Automotive Qualified
- All devices are RoHS compliant

Packages

- 8-Lead SOIC (3.90 mm)

Product Description

The Serial Quad I/O™ (SQI™) family of Flash memory devices features a six-wire, 4-bit I/O interface that allows for low-power, high-performance operation in a low pin-count package.The SST26VF016BEUI also supports full command-set compatibility with the traditional Serial Peripheral Interface (SPI) protocol. System designs using SQI Flash devices occupy less board space and ultimately lower system costs.

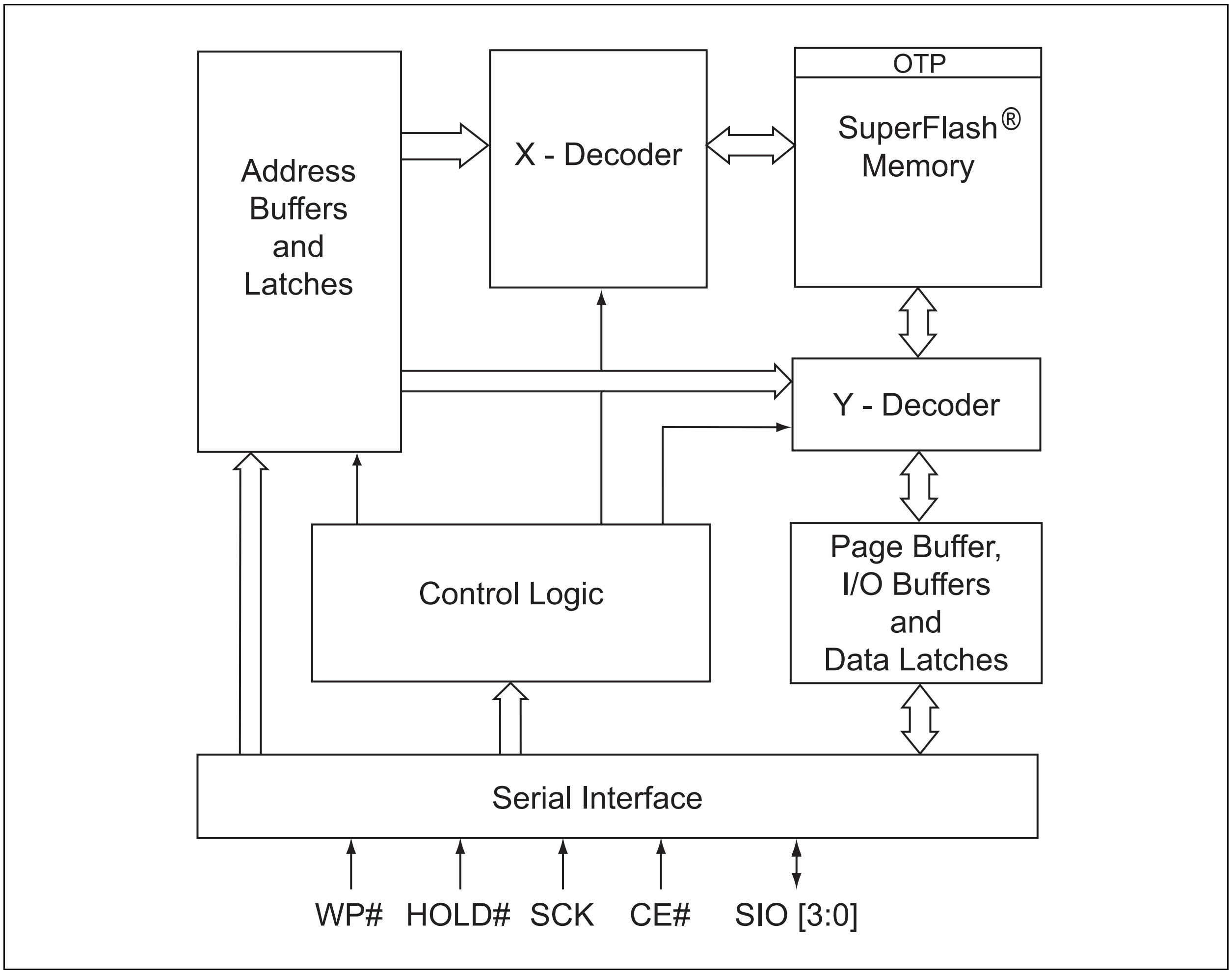
All members of the 26 Series, SQI™ family are manufactured with proprietary, high-performance CMOS SuperFlash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

The SST26VF016BEUI significantly improves performance and reliability while lowering power consumption. These devices write (Program or Erase) with a single power supply of 2.3V to 3.6V. The total energy consumed is a function of the applied voltage, current and time of application. Since, for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative Flash memory technologies.

See Figure 2-1 for pin assignments.

1.0 BLOCK DIAGRAM

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM



2.0 PIN DESCRIPTION

FIGURE 2-1: PIN DESCRIPTION FOR 8-LEAD SOIC

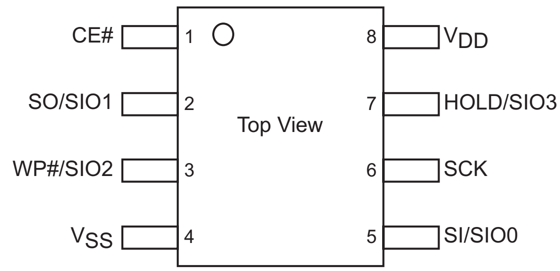


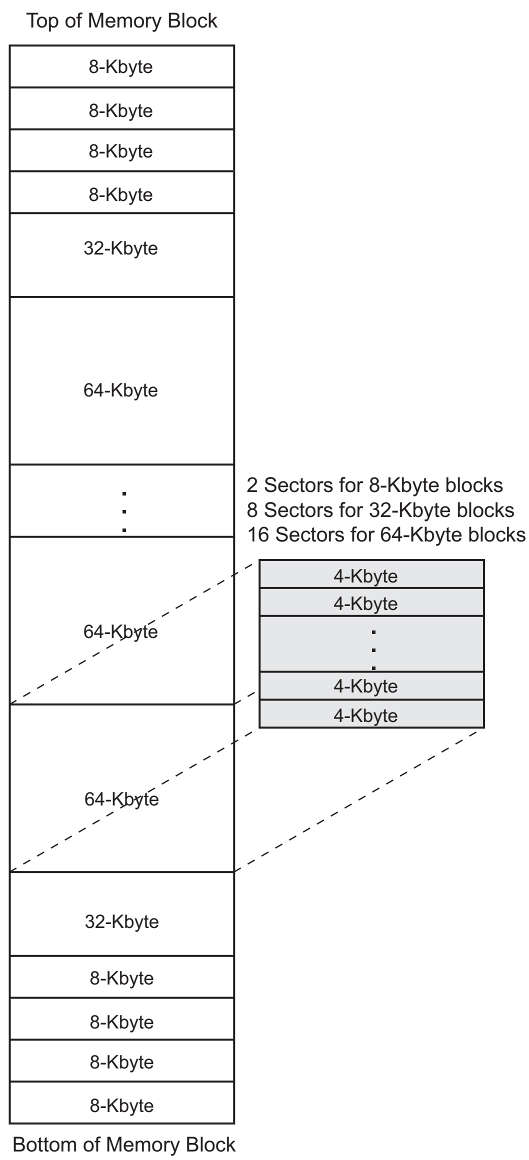
TABLE 2-1: PIN DESCRIPTION

Symbol	Pin Name	Functions
SCK	Serial Clock	Provides the timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data are shifted out on the falling edge of the clock input.
SIO[3:0]	Serial Data Input/Output	Transfers commands, addresses or data serially into the device or data out of the device. Inputs are latched on the rising edge of the serial clock. Data are shifted out on the falling edge of the serial clock. The Enable Quad I/O (`EQIO`) command instruction configures these pins for Quad I/O mode.
SI	Serial Data Input for SPI mode	Transfers commands, addresses or data serially into the device. Inputs are latched on the rising edge of the serial clock. SI is the default state after a Power-On Reset.
SO	Serial Data Output for SPI mode	Transfers data serially out of the device. Data are shifted out on the falling edge of the serial clock. SO is the default state after a Power-On Reset.
CE#	Chip Enable	The device is enabled by a high-to-low transition on CE#. CE# must remain low for the duration of any command sequence or, in the case of write operations, for the command/data input sequence.
WP#	Write Protect	Used in conjunction with the WPEN and IOC bits in the Configuration register to prohibit write operations to the Block-Protection register. This pin only works in SPI, single bit and dual bit Read mode.
HOLD#	Hold	Temporarily stops serial communication with the SPI Flash memory while the device is selected. This pin only works in SPI, single bit and dual bit Read mode and must be tied high when not in use.
V_{DD}	Power Supply	To provide power supply voltage.
V_{SS}	Ground	

3.0 MEMORY ORGANIZATION

The SST26VF016BEUI SQI memory array is organized in uniform 4-Kbyte erasable sectors with the following erasable blocks: eight 8-Kbyte parameter blocks, two 32-Kbyte overlay blocks and thirty 64-Kbyte overlay blocks (see Figure 3-1).

FIGURE 3-1: MEMORY MAP



4.0 DEVICE OPERATION

The SST26VF016BEUI supports both Serial Peripheral Interface (SPI) bus protocol and a 4-bit multiplexed SQI bus protocol. To provide backward compatibility with traditional SPI Serial Flash devices, the device's initial state after a Power-On Reset is SPI mode, which supports multi-I/O (x1/x2/x4) Read/Write commands. A command instruction configures the device to SQI mode. The dataflow in SQI mode is similar to that in SPI mode, except it uses four multiplexed I/O signals for command, address and data sequence.

SQI Flash Memory supports both Mode 0 (0,0) and Mode 3 (1,1) bus operations. The difference between the two modes is the state of the SCK signal when the bus host is in Standby mode and no data are being transferred. The SCK signal is low for Mode 0, and the SCK signal is high for Mode 3. For both modes, the Serial Data I/O (SIO[3:0]) is sampled at the rising edge of the SCK clock signal for input and driven after the falling edge of the SCK clock signal for output. The traditional SPI protocol uses separate input (SI) and output (SO) data signals, as shown in Figure 4-1. The SQI protocol uses four multiplexed signals, SIO[3:0], for both data in and data out, as shown in Figure 4-2. This means the SQI protocol quadruples the traditional bus transfer speed at the same clock frequency, without the need for more pins on the package.

The SST26VF016BEUI is pre-programmed with a globally unique EUI-48 and EUI-64 identifiers. The addresses are located in the Serial Flash Discoverable Parameters (SFDP) table and accessible via the SFDP read instruction. Refer to **Section 11.2 "Pre-Programmed EUI-48 and EUI-64 Address"** for address locations and description.

FIGURE 4-1: SPI PROTOCOL (TRADITIONAL 25 SERIES SPI DEVICE)

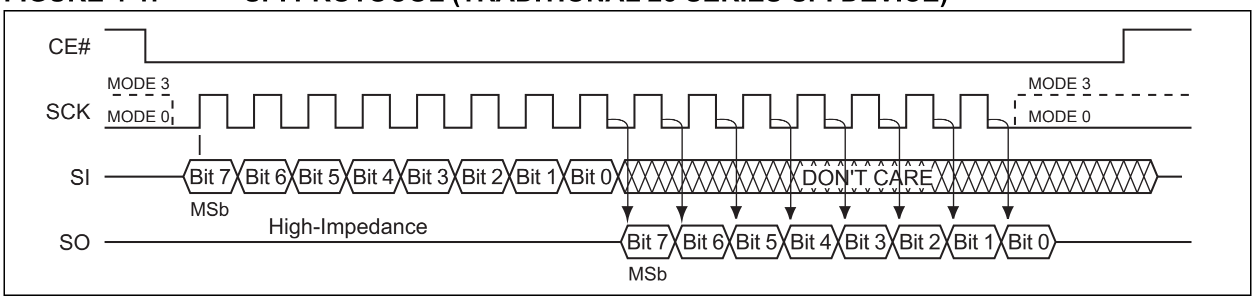
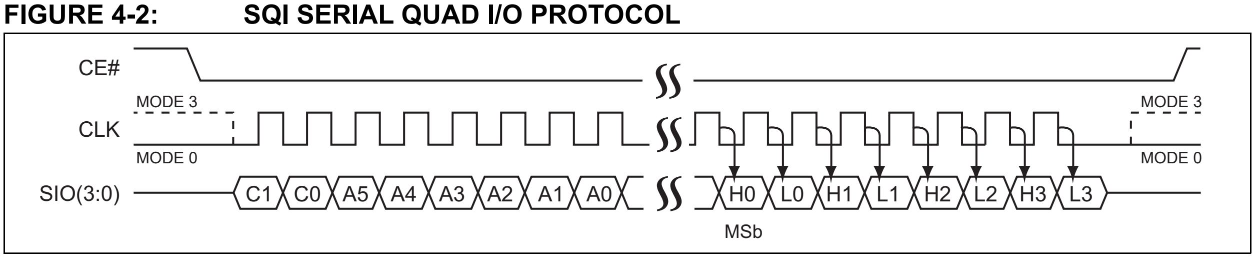


FIGURE 4-2: SQI SERIAL QUAD I/O PROTOCOL



4.1 Device Protection

The SST26VF016BEUI offers a flexible memory protection scheme that allows the protection state of each individual block to be controlled separately. In addition, the Write Protection Lock-Down register prevents any changes to the lock status during device operation. To avoid inadvertent writes during power-up, the device is write-protected by default after a Power-On Reset cycle. A Global Block Protection Unlock command provides a single command cycle that unlocks the entire memory array for faster manufacturing throughput.

For extra protection, there is an additional nonvolatile register that can permanently write-protect the Block Protection register bits for each individual block. Each of the corresponding lock-down bits is One-Time-Programmable (OTP) — once written, they cannot be erased. Data that have been previously programmed into these blocks cannot be altered by programming or erased and are not reversible.

4.1.1 INDIVIDUAL BLOCK PROTECTION

The SST26VF016BEUI has a Block Protection register that provides a software mechanism to write-lock the individual memory blocks and write-lock and/or read-lock, the individual parameter blocks. The Block Protection register is 48 bits wide: two bits each for the eight 8-Kbyte parameter blocks (write-lock and read-lock) and one bit each for the remaining 32-Kbyte and 64-Kbyte overlay blocks (write-lock). See Table 5-6 for address range protected per register bit.

Each bit in the Block Protection register (BPR) can be written to a '1' (protected) or '0' (unprotected). For the parameter blocks, the Most Significant bit is for read-lock and the Least Significant bit is for write-lock. Read-locking the parameter blocks provides additional security for sensitive data after retrieval, such as after initial boot. If a block is read-locked all read operations to the block will return data 00H.

The Write Block Protection Register command is a two-cycle command that requires that Write Enable (WREN) command to be executed prior to the Write Block Protection Register command. The Global Block Protection Unlock command clears all write protection bits in the Block Protection register.

4.1.2 WRITE PROTECTION LOCK-DOWN (VOLATILE)

To prevent changes to the Block Protection register, use the Lock-Down Block Protection Register (LBPR) command to enable Write Protection Lock-Down. Once Write Protection Lock-Down is enabled, the Block Protection register cannot be changed. To avoid inadvertent lock-down, the WREN command must be executed prior to the LBPR command.

To reset Write Protection Lock-Down, perform a power cycle on the device. The Write Protection Lock-Down status may be read from the Status register.

4.1.3 WRITE LOCK LOCK-DOWN (NONVOLATILE)

The nonvolatile Write Lock Lock-Down register is an alternate register that permanently prevents changes to the block-protect bits. The nonvolatile Write Lock Lock-Down register (nVWLDR) is 40 bits wide per device: one bit each for the eight 8-Kbyte parameter blocks and one bit each for the remaining 32-Kbyte and 64-Kbyte overlay blocks. See Table 5-6 for address range protected per register bit.

Writing '1' to any or all of the nVWLDR bits disables the change mechanism for the corresponding Write Lock bit in the BPR and permanently sets this bit to a '1' (protected) state. After this change, both bits will be set to '1', regardless of the data entered in subsequent writes to either the nVWLDR or the BPR. Subsequent writes to the nVWLDR can only alter available locations that have not been previously written to a '1'. This method provides write protection for the corresponding memory-array block by protecting it from future program or erase operations.

Writing a '0' in any location in the nVWLDR has no effect on either the nVWLDR or the corresponding Write Lock bit in the BPR.

Note that if the Block Protection register has been previously locked down (see **Section 4.1.2 "Write Protection Lock-Down (Volatile)"**), the device must be power-cycled before using the nVWLDR. If the Block Protection register is locked down and the Write nVWLDR command is accessed, the command will be ignored.

4.2 Hardware Write Protection

The hardware Write Protection pin (WP#) is used in conjunction with the WPEN and IOC bits in the Configuration register to prohibit write operations to the Block Protection and Configuration registers. The WP# pin function only works in SPI single-bit and dual-bit read modes when the IOC bit in the Configuration register is set to '0'.

The WP# pin function is disabled when the WPEN bit in the Configuration register is '0'. This allows installation of the SST26VF016BEUI in a system with a grounded WP# pin while still enabling writes to the Block Protection register. The Lock-Down function of the Block Protection Register supersedes the WP# pin, see Table 4-1 for Write Protection Lock-Down states.

The factory default setting at power-up of the WPEN bit is '0', disabling the Write Protect function of the WP# after power-up. WPEN is a nonvolatile bit; once the bit is set to '1', the Write Protect function of the WP# pin continues to be enabled after power-up. The WP# pin only protects the Block Protection Register and Configuration register from changes. Therefore, if the WP# pin is set to low before or after a Program or Erase command or while an internal Write is in progress, it will have no effect on the Write command.

The IOC bit takes priority over the WPEN bit in the Configuration register. When the IOC bit is '1', the function of the WP# pin is disabled and the WPEN bit serves no function. When the IOC bit is '0' and WPEN is '1', setting the WP# pin active low prohibits write operations to the Block Protection Register.

TABLE 4-1: WRITE PROTECTION LOCK-DOWN STATES

WP#	IOC	WPEN	WPLD	Execute WBPR Instruction	Configuration Register
L	0	1	1	Not Allowed	Protected
L	0	0	1	Not Allowed	Writable
L	0	1	0	Not Allowed	Protected
L	0(1)	0(2)	0	Allowed	Writable

Note 1: Default at power-up register settings.

2: Factory default setting is '0'. This is a nonvolatile bit; default at power-up is the value set prior to power-down.

TABLE 4-1: WRITE PROTECTION LOCK-DOWN STATES (CONTINUED)

H	0	X	1	Not Allowed	Writable
H	0	X	0	Allowed	Writable
X	1	X	1	Not Allowed	Writable
X	1	0(2)	0	Allowed	Writable

Note 1: Default at power-up register settings.

2: Factory default setting is '0'. This is a nonvolatile bit; default at power-up is the value set prior to power-down.

4.3 Security ID

The SST26VF016BEUI offers a 2-Kbyte Security ID (Sec ID) feature. The Security ID space is divided into two parts: a factory-programmed, 64-bit segment and a user programmable segment. The factory-programmed segment is programmed during manufacturing with a unique number and cannot be changed. The user-programmable segment is left unprogrammed, allowing the customer to program as desired.

Use the Program Security ID (`PSID`) command to program the Security ID using the address shown in Table 5-5. The Security ID can be locked using the Lockout Security ID (`LSID`) command, which prevents any future write operations to the Security ID.

The factory-programmed portion of the Security ID cannot be programmed by the user. Neither the factory-programmed nor the user-programmable areas can be erased.

4.4 Hold Operation

The HOLD# pin pauses active serial sequences without resetting the clocking sequence. **This pin becomes active after every power-up and only operates during SPI single bit and dual bit modes**.

The SST26VF016BEUI ships with the IOC bit set to '0' and the HOLD# pin function enabled. The HOLD# pin is always disabled in SQI mode and only works in SPI single-bit and dual-bit read modes.

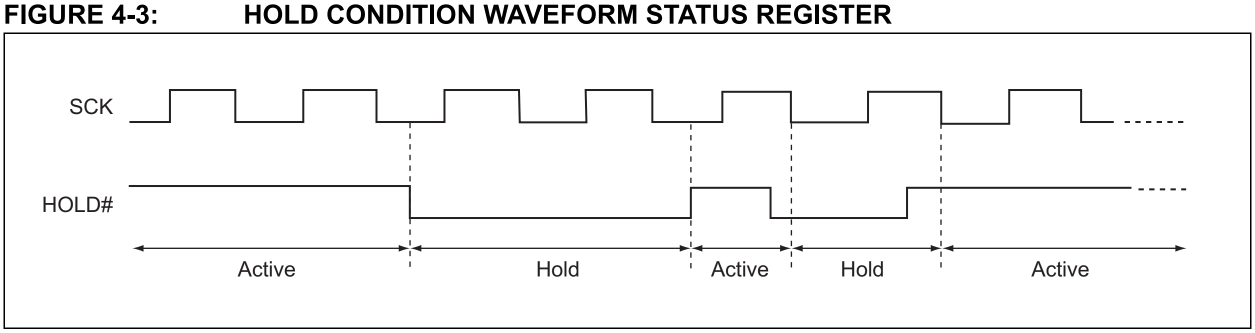
To activate Hold mode, CE# must be in active-low state. Hold mode begins when the SCK active-low state coincides with the falling edge of the HOLD# signal. Hold mode ends when the rising edge of the HOLD# signal coincides with the SCK active-low state.

If the falling edge of the HOLD# signal does not coincide with the SCK active-low state, then the device enters Hold mode when the SCK next reaches the active-low state. Similarly, if the rising edge of the HOLD# signal does not coincide with the SCK active-low state, then the device exits Hold mode when the SCK next reaches the active-low state. See Figure 4-3.

Once the device enters Hold mode, SO will be in high impedance state while SI and SCK can be V_{IL} or V_{IH}.

If CE# is driven active high during a Hold condition, it resets the internal logic of the device. As long as the HOLD# signal is low, the memory remains in the Hold condition. To resume communication with the device, HOLD# must be driven active-high and CE# must be driven active-low.

FIGURE 4-3: HOLD CONDITION WAVEFORM STATUS REGISTER



4.5 STATUS Register

The STATUS register is a read-only register that provides the following status information: whether the Flash memory array is available for any Read or Write operation, whether the device is write-enabled, whether an erase or program operation is suspended, and whether the Block Protection register and/or Security ID are locked down. During an internal Erase or Program operation, the STATUS register may be read to determine the completion of an operation in progress. Table 4-2 describes the function of each bit in the STATUS register.

TABLE 4-2: STATUS REGISTER

Bit	Name	Function	Default at Power-up	Read/Write (R/W)
0	BUSY	Write operation status 1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	Write-Enable Latch status 1 = Device is write enabled 0 = Device is not write enabled	0	R
2	WSE	Write Suspend Erase status 1 = Erase suspended 0 = Erase is not suspended	0	R
3	WSP	Write Suspend Program status 1 = Program suspended 0 = Program is not suspended	0	R
4	WPLD	Write Protection Lock Down status 1 = Write Protection Lock Down enabled 0 = Write Protection Lock Down disabled	0	R
5	SEC(1)	Security ID status 1 = Security ID space locked 0 = Security ID space not locked	0(1)	R
6	RES	Reserved for future use	0	R
7	BUSY	Write operation status 1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R

Note 1: The Security ID status will always be ‘1’ at power-up after a successful execution of the Lockout Security ID instruction. Otherwise the default at power-up is ‘0’.

4.5.1 WRITE ENABLE LATCH (WEL)

The Write Enable Latch (WEL) bit indicates the status of the internal memory’s Write Enable Latch. If the WEL bit is set to ‘1’, the device is write-enabled. If the bit is set to ‘**0**’ (reset), the device is not write-enabled and does not accept any memory Program or Erase, Protection Register Write, or Lock-Down commands. The Write Enable Latch bit is automatically reset under the following conditions:

- Power-up
- Reset
- Write Disable (WRDI) instruction
- Page Program instruction completion
- Sector Erase instruction completion
- Block Erase instruction completion
- Chip Erase instruction completion
- Write Block Protection register instruction
- Lock-Down Block Protection register instruction
- Program Security ID instruction completion
- Lockout Security ID instruction completion
- Write Suspend instruction
- SPI Quad Page program instruction completion
- Write Status Register

4.5.2 WRITE SUSPEND ERASE STATUS (WSE)

The Write Suspend Erase status (WSE) indicates when an Erase operation has been suspended. The WSE bit is ‘1’ after the host issues a suspend command during an Erase operation. Once the suspended Erase resumes, the WSE bit is reset to ‘0’.

4.5.3 WRITE SUSPEND PROGRAM STATUS (WSP)

The Write Suspend Program status (WSP) bit indicates when a Program operation has been suspended. The WSP is ‘1’ after the host issues a suspend command during the Program operation. Once the suspended Program resumes, the WSP bit is reset to ‘**0**’.

4.5.4 WRITE PROTECTION LOCK-DOWN STATUS (WPLD)

The Write Protection Lock-Down status (WPLD) bit indicates when the Block Protection register is locked down to prevent changes to the protection settings. The WPLD is ‘1’ after the host issues a Lock-Down Block Protection command. After a power cycle, the WPLD bit is reset to ‘0’.

4.5.5 SECURITY ID STATUS (SEC)

The Security ID Status (SEC) bit indicates when the Security ID space is locked to prevent a Write command. The SEC is '1' after the host issues a Lockout SID command. Once the host issues a Lockout SID command, the SEC bit can never be reset to '0.'

4.5.6 BUSY

The Busy bit determines whether there is an internal Erase or Program operation in progress. If the BUSY bit is '1', the device is busy with an internal Erase or Program operation. If the bit is '0', no Erase or Program operation is in progress.

4.6 Configuration Register

The Configuration register is a Read/Write register that stores a variety of configuration information. See Table 4-3 for the function of each bit in the register.

TABLE 4-3: CONFIGURATION REGISTER

Bit	Name	Function	Default at Power-up	Read/Write (R/W)
0	RES	Reserved	0	R
1	IOC	I/O Configuration for SPI Mode 1 = WP# and HOLD# pins disabled 0 = WP# and HOLD# pins enabled	0(1)	R/W
2	RES	Reserved	0	R
3	BPNV	Block Protection Volatility State 1 = No memory block has been permanently locked 0 = Any block has been permanently locked	1	R
4	RES	Reserved	0	R
5	RES	Reserved	0	R
6	RES	Reserved	0	R
7	WPEN	Write-Protection Pin (WP#) Enable 1 = WP# enabled 0 = WP# disabled	0(2)	R/W

Note 1: Default at Power-up is '0'.
2: Factory default setting. This is a nonvolatile bit; default at power-up will be the setting prior to power-down.

4.6.1 I/O CONFIGURATION (IOC)

The I/O Configuration (IOC) bit reconfigures the I/O pins. The IOC bit is set by writing a '1' to Bit 1 of the Configuration register. When the IOC bit is '0' the WP# pin and the HOLD# pin are enabled (SPI or Dual Configuration setup). When the IOC bit is set to '1', the SIO2 pin and SIO3 pins are enabled (SPI Quad I/O Configuration setup). The IOC bit must be set to '1' before issuing the following SPI commands: SQOR (6BH), SQIOR (EBH), RBSPI (ECH) and SPI Quad page program (32H). Without setting the IOC bit to '1', those SPI commands are not valid. The I/O configuration bit does not apply when in SQI mode. The default at power-up is '0'.

4.6.2 BLOCK PROTECTION VOLATILITY STATE (BPNV)

The Block Protection Volatility State bit indicates whether any block has been permanently locked with the nonvolatile Write Lock Lock-Down register (nVWLDR). When no bits in the nVWLDR have been set, the BPNV is '1'; this is the default state from the factory. When one or more bits in the nVWLDR are set to '1', the BPNV bit will be '0' from that point forward, even after power-up.

4.6.3 WRITE-PROTECT ENABLE (WPEN)

The Write-Protect Enable (WPEN) bit is a nonvolatile bit that enables the WP# pin.

The Write-Protect (WP#) pin and the Write-Protect Enable (WPEN) bit control the programmable hardware write-protect feature. Setting the WP# pin to low and the WPEN bit to '1', enables Hardware write protection. To disable hardware write protection, set either the WP# pin to high or the WPEN bit to '0'. There is latency associated with writing to the WPEN bit. Poll the BUSY bit in the Status register, or wait T_{WPEN}, for the completion of the internal, self-timed Write operation. When the chip is hardware write-protected, only Write operations to Block Protection and Configuration registers are disabled. See **Section 4.2 "Hardware Write Protection"** and Table 4-1 for more information about the functionality of the WPEN bit.

5.0 INSTRUCTIONS

Instructions are used to read, write (erase and program) and configure the SST26VF016BEUI. The complete list of the instructions is provided in Table 5-1.

TABLE 5-1: DEVICE OPERATION INSTRUCTIONS FOR SST26VF016BEUI

Instruction	Description	Command Cycle[1]	Mode		Address Cycle(s)[2, 3]	Dummy Cycle(s)[3]	Data Cycle(s)[3]	Max Freq.[4]
			SPI	SQI				
Configuration								
`NOP`	No Operation	00H	X	X	0	0	0	104 MHz/ 80 MHz
`RSTEN`	Reset Enable	66H	X	X	0	0	0	
`RST`[5]	Reset Memory	99H	X	X	0	0	0	
`EQIO`	Enable Quad I/O	38H	X		0	0	0	
`RSTQIO`[6]	Reset Quad I/O	FFH	X	X	0	0	0	
`RDSR`	Read Status Register	05H	X		0	0	1 to ∞	
				X	0	1	1 to ∞	
`WRSR`	Write Status Register	01H	X	X	0	0	2	
`RDCR`	Read Configuration Register	35H	X		0	0	1 to ∞	
				X	0	1	1 to ∞	
Read								
`Read`	Read Memory	03H	X		3	0	1 to ∞	40 MHz
`High-Speed Read`	Read Memory at Higher Speed	0BH		X	3	3	1 to ∞	104 MHz/ 80 MHz
			X		3	1	1 to ∞	
`SQOR`[7]	SPI Quad Output Read	6BH	X		3	1	1 to ∞	
`SQIOR`[8]	SPI Quad I/O Read	EBH	X		3	3	1 to ∞	
`SDOR`[9]	SPI Dual Output Read	3BH	X		3	1	1 to ∞	
`SDIOR`[10]	SPI Dual I/O Read	BBH	X		3	1	1 to ∞	
`SB`	Set Burst Length	C0H	X	X	0	0	1	
`RBSQI`	SQI Read Burst with Wrap	0CH		X	3	3	n to ∞	
`RBSPI`[8]	SPI Read Burst with Wrap	ECH	X		3	3	n to ∞	

Note 1: Command cycle is two clock periods in SQI mode and eight clock periods in SPI mode.
2: Address bits above the Most Significant bit of each density can be V_{IL} or V_{IH}.
3: Address, Dummy/Mode bits and Data cycles are two clock periods in SQI and eight clock periods in SPI mode.
4: The maximum frequency for all instructions is up to 104 MHz from 2.7V to 3.6V and up to 80 MHz from 2.3V to 3.6V, unless otherwise noted.
5: `RST` command only executed if **`RSTEN`** command is executed first. Any intervening command will disable Reset.
6: Device accepts eight-clock command in SPI mode or two-clock command in SQI mode.
7: Data cycles are two clock periods. IOC bit must be set to ‘1’ before issuing the command.
8: Address, Dummy/Mode bits and data cycles are two clock periods. IOC bit must be set to ‘1’ before issuing the command.
9: Data cycles are four clock periods.
10: Address, Dummy/Mode bits and Data cycles are four clock periods.
11: Sector Addresses: Use AMS-A12; the remaining address are “don’t care”, but must be set to V_{IL} or V_{IH}.
12: Blocks are 64-Kbyte, 32-Kbyte, or 8-Kbyte, depending on location. Block Erase Address: AMS-A16 for 64-Kbyte; AMS-A15 for 32-Kbyte; AMS-A13 for 8-Kbyte. Remaining addresses are “don’t care”, but must be set to V_{IL} or V_{IH}.

TABLE 5-1: DEVICE OPERATION INSTRUCTIONS FOR SST26VF016BEUI (CONTINUED)

Instruction	Description	Command Cycle[1]	Mode		Address Cycle(s)[2, 3]	Dummy Cycle(s)[3]	Data Cycle(s)[3]	Max Freq.[4]
			SPI	SQI				
Identification								
JEDEC-ID	JEDEC-ID Read	9FH	X		0	0	3 to ∞	104 MHz/ 80 MHz
Quad J-ID	Quad I/O J-ID Read	AFH		X	0	1	3 to ∞	
SFDP	Serial Flash Discoverable Parameters	5AH	X		3	1	1 to ∞	
Write								
WREN	Write Enable	06H	X	X	0	0	0	104 MHz/ 80 MHz
WRDI	Write Disable	04H	X	X	0	0	0	
SE[11]	Erase 4 Kbytes of Memory Array	20H	X	X	3	0	0	
BE[12]	Erase 64, 32 or 8 Kbytes of Memory Array	D8H	X	X	3	0	0	
CE	Erase Full Array	C7H	X	X	0	0	0	
PP	Page Program	02H	X	X	3	0	1 to 256	
SPI Quad PP[7]	SQI Quad Page Program	32H	X		3	0	1 to 256	

Note 1: Command cycle is two clock periods in SQI mode and eight clock periods in SPI mode.
2: Address bits above the Most Significant bit of each density can be V_{IL} or V_{IH}.
3: Address, Dummy/Mode bits and Data cycles are two clock periods in SQI and eight clock periods in SPI mode.
4: The maximum frequency for all instructions is up to 104 MHz from 2.7V to 3.6V and up to 80 MHz from 2.3V to 3.6V, unless otherwise noted.
5: RST command only executed if **RSTEN** command is executed first. Any intervening command will disable Reset.
6: Device accepts eight-clock command in SPI mode or two-clock command in SQI mode.
7: Data cycles are two clock periods. IOC bit must be set to '1' before issuing the command.
8: Address, Dummy/Mode bits and data cycles are two clock periods. IOC bit must be set to '1' before issuing the command.
9: Data cycles are four clock periods.
10: Address, Dummy/Mode bits and Data cycles are four clock periods.
11: Sector Addresses: Use AMS-A12; the remaining address are "don't care", but must be set to V_{IL} or V_{IH}.
12: Blocks are 64-Kbyte, 32-Kbyte, or 8-Kbyte, depending on location. Block Erase Address: AMS-A16 for 64-Kbyte; AMS-A15 for 32-Kbyte; AMS-A13 for 8-Kbyte. Remaining addresses are "don't care", but must be set to V_{IL} or V_{IH}.

TABLE 5-1: DEVICE OPERATION INSTRUCTIONS FOR SST26VF016BEUI (CONTINUED)

Instruction	Description	Command Cycle[1]	Mode		Address Cycle(s)[2, 3]	Dummy Cycle(s)[3]	Data Cycle(s)[3]	Max Freq.[4]
			SPI	SQI				
WRSU	Suspends Program/Erase	B0H	X	X	0	0	0	104 MHz/ 80 MHz
WRRE	Resumes Program/Erase	30H	X	X	0	0	0	
Protection								
RBPR	Read Block Protection Register	72H	X		0	0	1 to 6	104 MHz/ 80 MHz
				X	0	1	1 to 6	
WBPR	Write Block Protection Register	42H	X	X	0	0	1 to 6	
LBPR	Lock-Down Block Protection Register	8DH	X	X	0	0	0	
nVWLDR	Nonvolatile Write Lock-Down Register	E8H	X	X	0	0	1 to 6	
ULBPR	Global Block Protection Unlock	98H	X	X	0	0	0	
RSID	Read Security ID	88H	X		2	1	1 to 2048	
				X	2	3	1 to 2048	
PSID	Program User Security ID area	A5H	X	X	2	0	1 to 256	
LSID	Lockout Security ID Programming	85H	X	X	0	0	0	
Power Saving								
DPD	Deep Power-down Mode	B9H	X	X	0	0	0	104 MHz/ 80 MHz
RDPD	Release from Deep Power-down and Read ID	ABH	X	X	3	0	1 to ∞	

Note 1: Command cycle is two clock periods in SQI mode and eight clock periods in SPI mode.
2: Address bits above the Most Significant bit of each density can be V_{IL} or V_{IH}.
3: Address, Dummy/Mode bits and Data cycles are two clock periods in SQI and eight clock periods in SPI mode.
4: The maximum frequency for all instructions is up to 104 MHz from 2.7V to 3.6V and up to 80 MHz from 2.3V to 3.6V, unless otherwise noted.
5: RST command only executed if **RSTEN** command is executed first. Any intervening command will disable Reset.
6: Device accepts eight-clock command in SPI mode or two-clock command in SQI mode.
7: Data cycles are two clock periods. IOC bit must be set to ‘1’ before issuing the command.
8: Address, Dummy/Mode bits and data cycles are two clock periods. IOC bit must be set to ‘1’ before issuing the command.
9: Data cycles are four clock periods.
10: Address, Dummy/Mode bits and Data cycles are four clock periods.
11: Sector Addresses: Use AMS-A12; the remaining address are “don’t care”, but must be set to V_{IL} or V_{IH}.
12: Blocks are 64-Kbyte, 32-Kbyte, or 8-Kbyte, depending on location. Block Erase Address: AMS-A16 for 64-Kbyte; AMS-A15 for 32-Kbyte; AMS-A13 for 8-Kbyte. Remaining addresses are “don’t care”, but must be set to V_{IL} or V_{IH}.

5.1 No Operation (NOP)

The No Operation command only cancels a Reset Enable command. NOP has no impact on any other command.

5.2 Reset Enable (RSTEN) and Reset (RST)

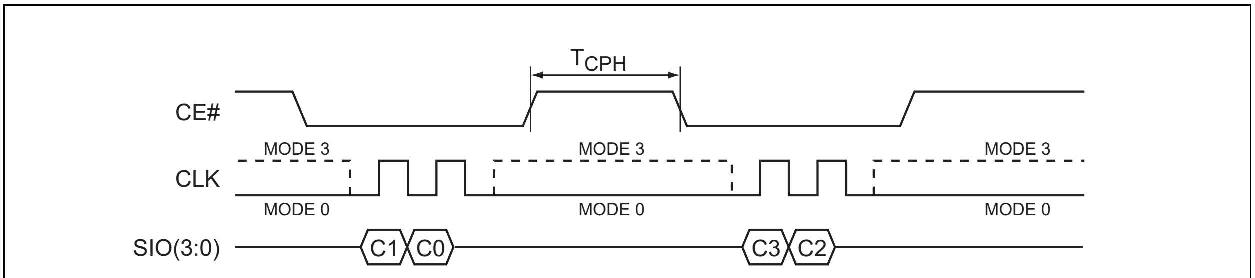
The Reset operation is used as a system (software) reset that puts the device in normal operating Ready mode. This operation consists of two commands: Reset-Enable (RSTEN) followed by Reset (RST).

To reset SST26VF016BEUI, the host drives CE# low, sends the Reset-Enable command (66H), and then drives CE# high. Next, the host drives CE# low again, sends the Reset command (99H), and drives CE# high (see Figure 5-1).

The Reset operation requires the Reset Enable command followed by the Reset command. Any command other than the Reset command after the Reset Enable command will disable the Reset Enable.

Once the Reset Enable and Reset commands are successfully executed, the device returns to normal operation Read mode and then performs the following actions: it resets the protocol to SPI mode, resets the burst length to 8 bytes, clears all the bits except for bit 4 (WPLD) and bit 5 (SEC), in the STATUS register to their default states and clears bit 1 (IOC) in the Configuration register to its default state. A device reset during an active Program or Erase operation aborts the operation, which can cause the data of the targeted address range to be corrupted or lost. Depending on the prior operation, the Reset timing may vary. Recovery from a Write operation requires more latency time than recovery from other operations. See Table 8-2 for Reset timing parameters.

FIGURE 5-1: RESET SEQUENCE



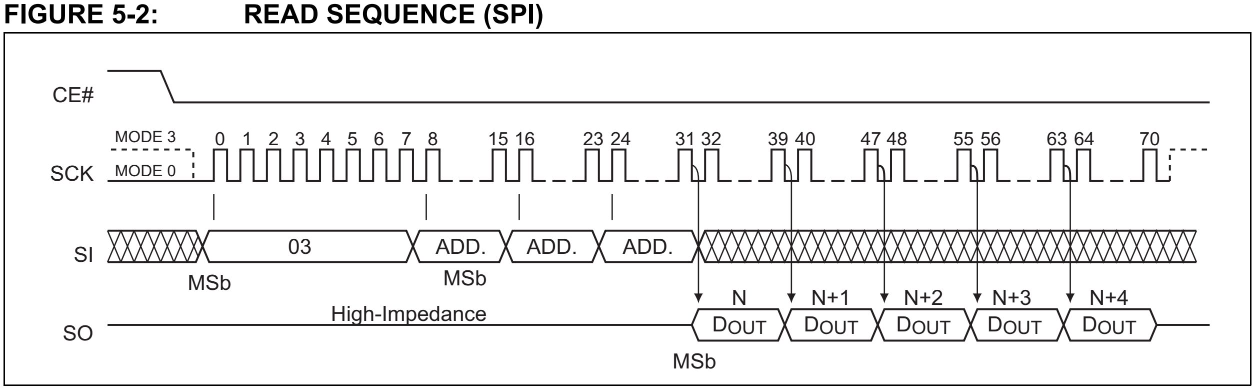
Note: C[1:0] = 66H; C[3:2] = 99H

5.3 Read (40 MHz)

The Read instruction, 03H, is supported in the SPI bus protocol with clock frequencies up to 40 MHz. This command is not supported in SQI bus protocol. The device outputs the data starting from the specified address location and then continuously streams the data output through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the Address Pointer will automatically return to the beginning (wrap-around) of the address space.

Initiate the Read instruction by executing an 8-bit command, 03H, followed by address bits A[23:0]. CE# must remain active-low for the duration of the Read cycle. See Figure 5-2 for the Read sequence.

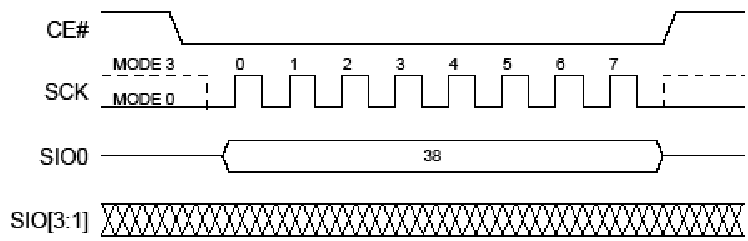
FIGURE 5-2: READ SEQUENCE (SPI)



5.4 Enable Quad I/O (EQIO)

The Enable Quad I/O (EQIO) instruction, 38H, enables the Flash device for SQI bus operation. Upon completion of the instruction, all instructions thereafter are expected to be 4-bit multiplexed input/output (SQI mode) until a power cycle or a "Reset Quad I/O instruction" is executed (see Figure 5-3).

FIGURE 5-3: ENABLE QUAD I/O SEQUENCE



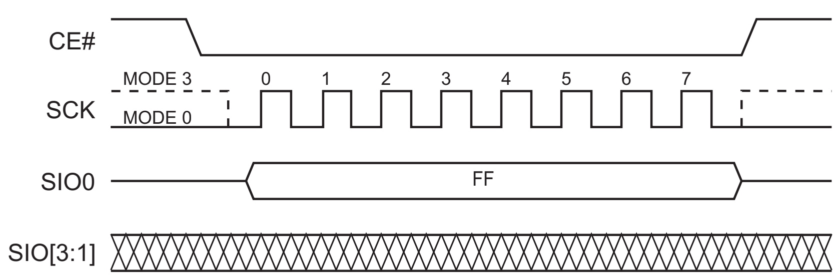
Note: SIO[3:1] must be driven VIH

5.5 Reset Quad I/O (RSTQIO)

The Reset Quad I/O instruction, FFH, resets the device to 1-bit SPI protocol operation or exits the Set Mode configuration during a read sequence. This command allows the Flash device to return to the default I/O state (SPI) without a power cycle and executes in either 1-bit or 4-bit mode. If the device is in the Set Mode configuration while in SQI High-Speed Read mode, the RSTQIO command will only return the device to a state where it can accept new command instructions. An additional RSTQIO is required to reset the device to SPI mode.

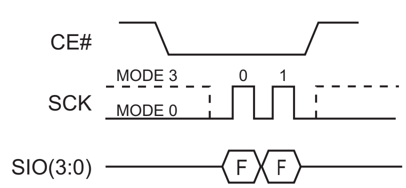
To execute a Reset Quad I/O operation, the host drives CE# low, sends the Reset Quad I/O command cycle (FFH), and then drive high. Execute the instruction in either SPI (8 clocks) or SQI (2 clocks) command cycles. For SPI, SIO[3:1] are don't care for this command, but should be driven to VIH or VIL. See Figure 5-4 and Figure 5-5.

FIGURE 5-4: RESET QUAD I/O SEQUENCE (SPI)



Note: SIO[3:1] must be driven VIH

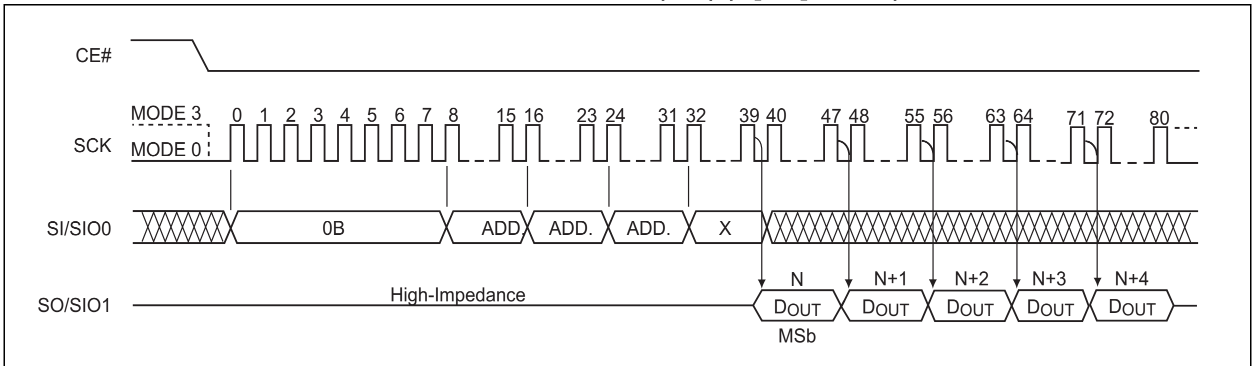
FIGURE 5-5: RESET QUAD I/O SEQUENCE (SQI)



5.6 High-Speed Read

The High-Speed Read instruction, 0BH, is supported in both SPI bus protocol and SQI protocol. This instruction supports frequencies of up to 80 MHz or 104 MHz with additional dummy input cycles prior to first data byte output. On power-up, the device is set to use SPI. Initiate a High-Speed Read by executing an 8-bit command, 0BH, followed by address bits A[23-0] and a dummy byte. CE# must remain active-low for the duration of the High-Speed Read cycle. See Figure 5-6 for the High-Speed Read sequence for SPI bus protocol.

FIGURE 5-6: HIGH-SPEED READ SEQUENCE (SPI) (C[1:0] = 0BH)



In SQI protocol, the host drives CE# low and then sends one High-Speed Read command cycle, 0BH, followed by three address cycles, a Set Mode Configuration cycle and two dummy cycles. Each cycle is two nibbles (clocks) long, with the most significant nibble first.

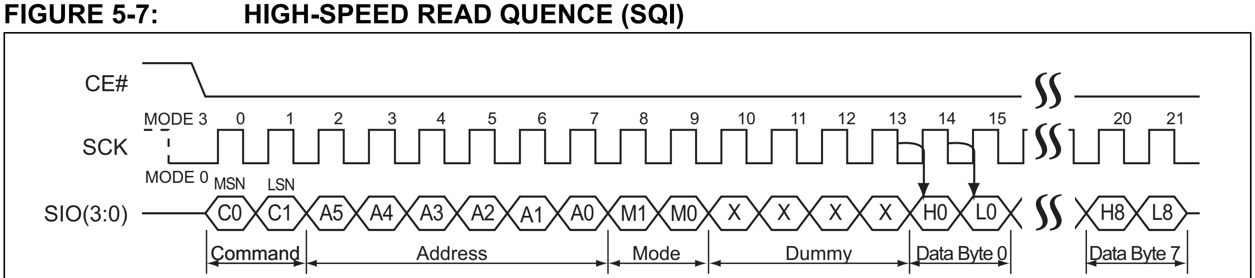
After the dummy cycles, the device outputs data on the falling edge of the SCK signal starting from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer automatically increments until the highest memory address is reached, at which point the Address Pointer returns to address location 000000H. During this operation, blocks that are Read-locked will output data 00H.

The Set Mode Configuration bit M[7:0] indicates if the next instruction cycle is another SQI High-Speed Read command. When M[7:0] = AXH, the device expects the next continuous instruction to be another Read command, 0BH, and does not require the op-code to be re-entered.

The host may initiate the next Read cycle by driving CE# low and then sending the four-bit input for address A[23:0], followed by the Set Mode configuration bits M[7:0] and two dummy cycles. After the two dummy cycles, the device outputs the data starting from the specified address location. There are no restrictions on address location access.

When M[7:0] is any value other than AXH, the device expects the next instruction initiated to be a command instruction. To reset/exit the Set Mode configuration, execute the Reset Quad I/O command, FFH. While in the Set Mode configuration, the `RSTQIO` command will only return the device to a state where it can accept a new command instruction. An additional `RSTQIO` is required to reset the device to SPI mode. See Figure 5-10 for the SPI Quad I/O Mode Read sequence when M[7:0] = AXH.

FIGURE 5-7: HIGH-SPEED READ QUENCE (SQI)



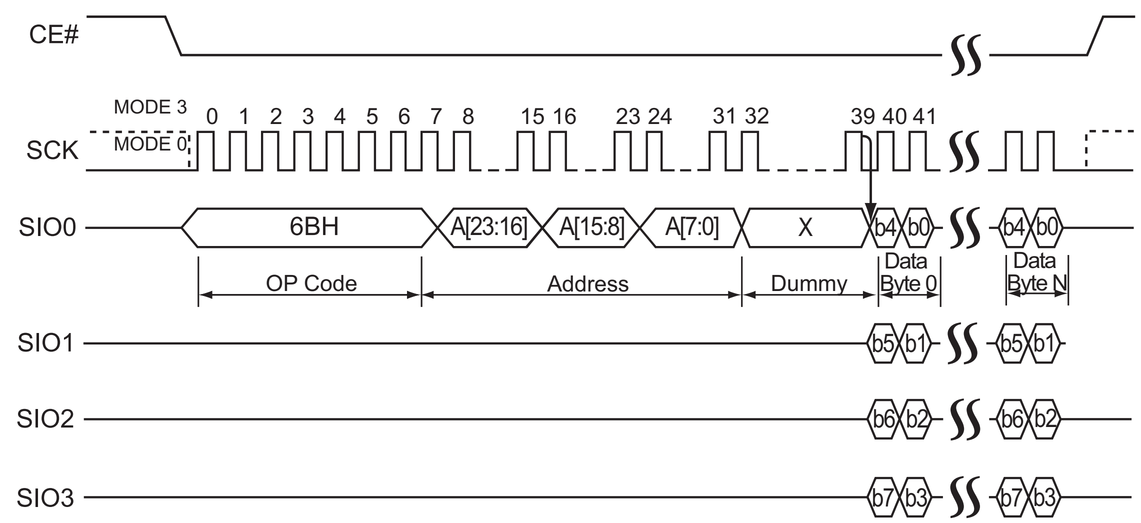
Note: MSN= Most Significant Nibble, LSN = Least Significant Nibble
Hx = High Data Nibble, Lx = Low Data Nibble C[1:0]=0BH

5.7 SPI Quad-Output Read

The SPI Quad Output Read instruction supports frequencies of up to 80 MHz or 104 MHz with additional dummy input cycles prior to first data byte output. The SST26VF016BEUI requires the IOC bit in the Configuration register to be set to '1' prior to executing the command. Initiate SPI Quad Output Read by executing an 8-bit command, 6BH, followed by address bits A[23-0] and a dummy byte. CE# must remain active-low for the duration of the SPI Quad Mode Read. See Figure 5-8 for the SPI Quad Output Read sequence.

Following the dummy byte, the device outputs data from SIO[3:0] starting from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer automatically increments until the highest memory address is reached, at which point the Address Pointer returns to the beginning of the address space.

FIGURE 5-8: SPI QUAD OUTPUT READ



Note: MSN= Most Significant Nibble, LSN = Least Significant Nibble

5.8 SPI Quad I/O Read

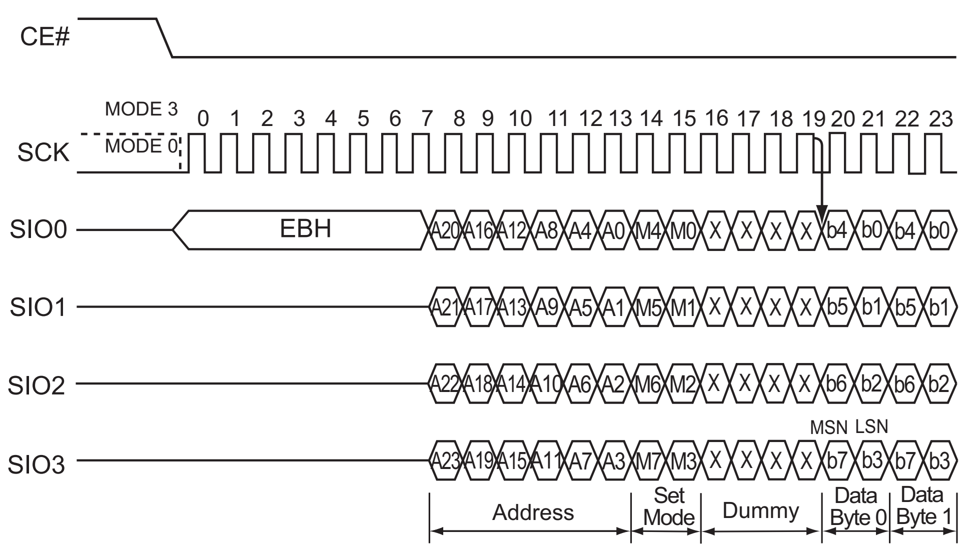
The SPI Quad I/O Read (SQIOR) instruction supports frequencies of up to 80 MHz or 104 MHz with additional dummy input cycles prior to first data byte output. The SST26VF016BEUI requires the IOC bit in the Configuration register to be set to '1' prior to executing the command. Initiate SQIOR by executing an 8-bit command, EBH. The device then switches to 4-bit I/O mode for address bits A[23-0], followed by the Set Mode configuration bits M[7:0] and two dummy bytes. CE# must remain active-low for the duration of the SPI Quad I/O Read. See Figure 5-9 for the SPI Quad I/O Read sequence.

Following the dummy bytes, the device outputs data from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer automatically increments until the highest memory address is reached, at which point the Address Pointer returns to the beginning of the address space.

The Set Mode Configuration bit M[7:0] indicates if the next instruction cycle is another SPI Quad I/O Read command. When M[7:0] = AXH, the device expects the next continuous instruction to be another Read command, EBH, and does not require the op-code to be entered again. The host may set the next SQIOR cycle by driving CE# low and then sending the four-bit-wide input for address A[23:0], followed by the Set Mode configuration bits M[7:0] and two dummy cycles. After the two dummy cycles, the device outputs the data starting from the specified address location. There are no restrictions on address location access.

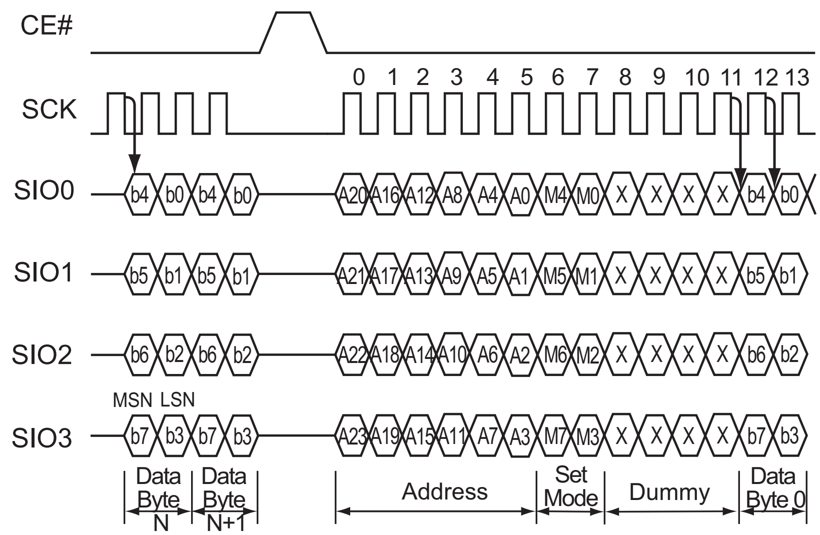
When M[7:0] is any value other than AXH, the device expects the next instruction initiated to be a command instruction. To reset/exit the Set Mode configuration, execute the Reset Quad I/O command, FFH. See Figure 5-10 for the SPI Quad I/O Mode Read sequence when M[7:0] = AXH.

FIGURE 5-9: SPI QUAD I/O READ SEQUENCE



Note: MSN= Most Significant Nibble, LSN = Least Significant Nibble

FIGURE 5-10: BACK-TO-BACK SPI QUAD I/O READ SEQUENCES WHEN M[7:0] = AXH



Note: MSN= Most Significant Nibble, LSN = Least Significant Nibble

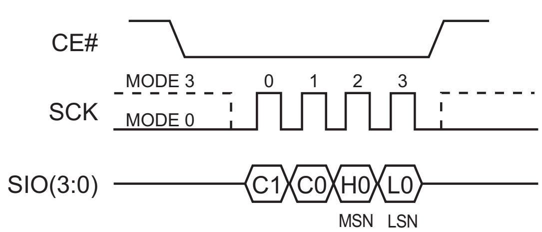
5.9 Set Burst

The Set Burst command specifies the number of bytes to be output during a Read Burst command before the device wraps around. It supports both SPI and SQI protocols. To set the burst length, the host drives CE# low, sends the Set Burst command cycle (C0H) and one data cycle, and then drives CE# high. After power-up or reset, the burst length is set to eight bytes (00H). See Table 5-2 for burst length data and Figures Figure 5-11 and Figure 5-12 for the sequences.

TABLE 5-2: BURST LENGTH DATA

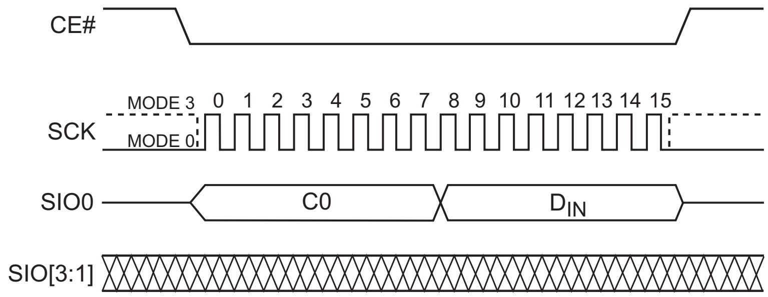
Burst Length	High Nibble (H0)	Low Nibble (L0)
8 Bytes	0h	0h
16 Bytes	0h	1h
32 Bytes	0h	2h
64 Bytes	0h	3h

FIGURE 5-11: SET BURST LENGTH SEQUENCE (SQI)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble, C[1:0]=C0H

FIGURE 5-12: SET BURST LENGTH SEQUENCE (SPI)



Note: SIO[3:1] must be driven V_{IH}.

5.10 SQI Read Burst with Wrap (RBSQI)

SQI Read Burst with Wrap is similar to High-Speed Read in SQI mode, except data will output continuously within the burst length until a low-to-high transition on CE#. To execute a SQI Read Burst operation, drive CE# low and then send the Read Burst command cycle (0CH), followed by three address cycles and then three dummy cycles. Each cycle is two nibbles (clocks) long, with the most significant nibble first.

After the dummy cycles, the device outputs data on the falling edge of the SCK signal starting from the specified address location. The data output stream is continuous across all addresses until terminated by a low-to-high transition on CE#.

During **RBSQI**, the internal Address Pointer automatically increments until the last byte of the burst is reached, at which point it wraps around to the first byte of the burst. All bursts are aligned to addresses within the burst length (see Table 5-3). For example, if the burst length is eight bytes and the start address is 06h, the burst sequence would be: 06h, 07h, 00h, 01h, 02h, 03h, 04h, 05h, 06h, etc. The pattern repeats until the command is terminated by a low-to-high transition on CE#.

During this operation, blocks that are read-locked will output data 00H.

5.11 SPI Read Burst with Wrap (RBSPI)

SPI Read Burst with Wrap (RBSPI) is similar to SPI Quad I/O Rea,d except the data will output continuously within the burst length until a low-to-high transition occurs on CE#. To execute a SPI Read Burst with Wrap operation, drive CE# low and then send the Read Burst command cycle (ECH), followed by three address cycles and then three dummy cycles.

After the dummy cycle, the device outputs data on the falling edge of the SCK signal starting from the specified address location. The data output stream are continuous through all addresses until terminated by a low-to-high transition on CE#.

During **RBSPI**, the internal Address Pointer automatically increments until the last byte of the burst is reached, at which point it wraps around to the first byte of the burst. All bursts are aligned to addresses within the burst length (see Table 5-3). For example, if the burst length is eight bytes and the start address is 06h, the burst sequence would be: 06h, 07h, 00h, 01h, 02h, 03h, 04h, 05h, 06h, etc. The pattern repeats until the command is terminated by a low-to-high transition on CE#.

During this operation, blocks that are read-locked will output data 00H.

TABLE 5-3: BURST ADDRESS RANGES

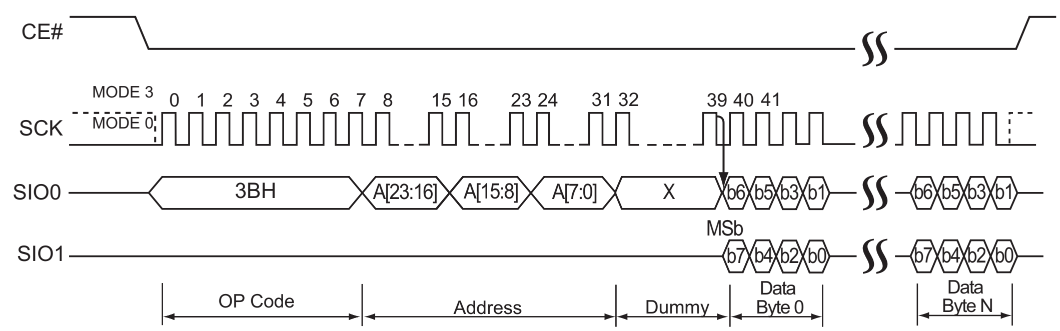
Burst Length	Burst Address Ranges
8 Bytes	00-07H, 08-0FH, 10-17H, 18-1FH...
16 Bytes	00-0FH, 10-1FH, 20-2FH, 30-3FH...
32 Bytes	00-1FH, 20-3FH, 40-5FH, 60-7FH...
64 Bytes	00-3FH, 40-7FH, 80-BFH, C0-FFH

5.12 SPI Dual Output Read

The SPI Dual Output Read instruction supports frequencies of up to 80 MHz or 104 MHz with additional dummy input cycles prior to first data byte output. Initiate a SPI Dual Output Read by executing an 8-bit command, 3BH, followed by address bits A[23-0] and a dummy byte. CE# must remain active-low for the duration of the SPI Dual Output Read operation. See Figure 5-13 for the SPI Quad Output Read sequence.

Following the dummy byte, the SST26VF016BEUI outputs data from SIO[1:0] starting from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer automatically increments until the highest memory address is reached, at which point the Address Pointer returns to the beginning of the address space.

FIGURE 5-13: FAST READ, DUAL OUTPUT SEQUENCE



Note: MSB = Most Significant bit.

5.13 SPI Dual I/O Read

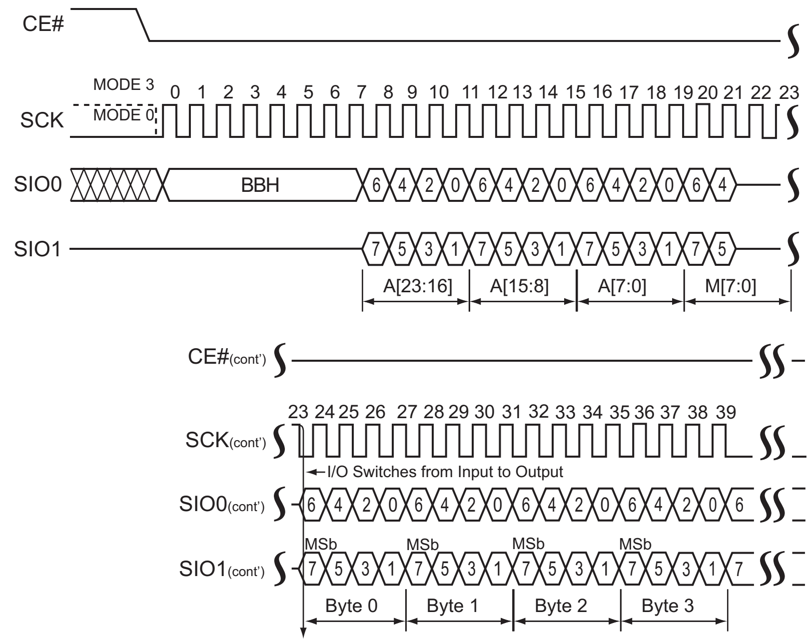
The SPI Dual I/O Read (`SDIOR`) instruction supports a frequency up to 80 MHz. Initiate `SDIOR` by executing an 8-bit command, BBH. The device then switches to 2-bit I/O mode for address bits A[23-0], followed by the Set Mode configuration bits M[7:0]. CE# must remain active-low for the duration of the SPI Dual I/O Read. See Figure 5-14 for the SPI Dual I/O Read sequence.

Following the Set Mode configuration bits, the SST26VF016BEUI outputs data from the specified address location. The device continuously streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer automatically increments until the highest memory address is reached, at which point the Address Pointer returns to the beginning of the address space.

The Set Mode Configuration bit M[7:0] indicates if the next instruction cycle is another SPI Dual I/O Read command. When M[7:0] = AXH, the device expects the next continuous instruction to be another `SDIOR` command, BBH, and does not require the op-code to be entered again. The host may set the next `SDIOR` cycle by driving CE# low and then sending the two-bit wide input for address A[23:0], followed by the Set Mode configuration bits M[7:0]. After the Set Mode configuration bits, the device outputs the data starting from the specified address location. There are no restrictions on address location access.

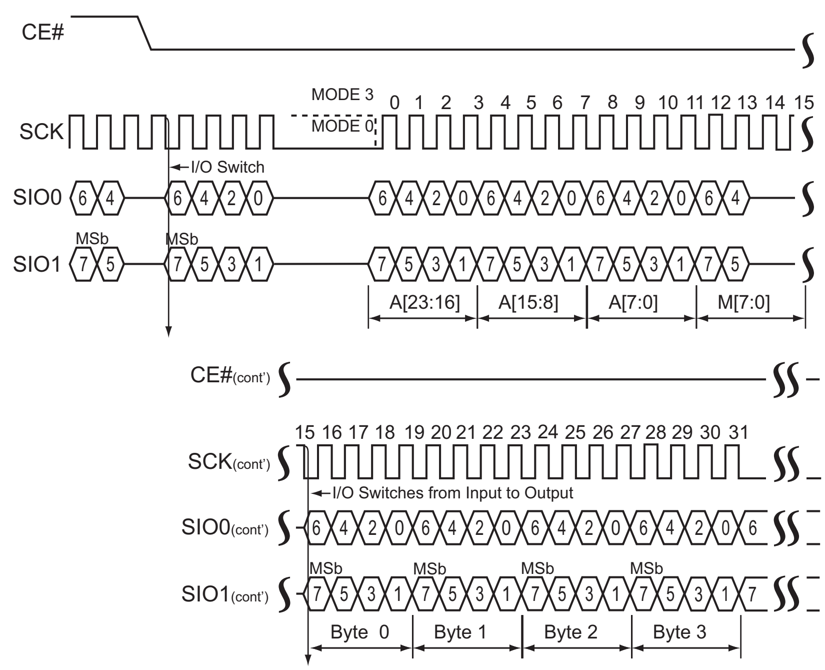
When M[7:0] is any value other than AXH, the device expects the next instruction initiated to be a command instruction. To reset or exit the Set Mode configuration, execute the Reset Quad I/O command, FFH. See Figure 5-15 for the SPI Dual I/O Read sequence when M[7:0] = AXH.

FIGURE 5-14: SPI DUAL I/O READ SEQUENCE



Note: MSB= Most Significant bit, LSB = Least Significant bit

FIGURE 5-15: BACK-TO-BACK SPI DUAL I/O READ SEQUENCES WHEN M[7:0] = AXH



Note: MSB= Most Significant bit, LSB = Least Significant bit

5.14 JEDEC ID Read (SPI Protocol)

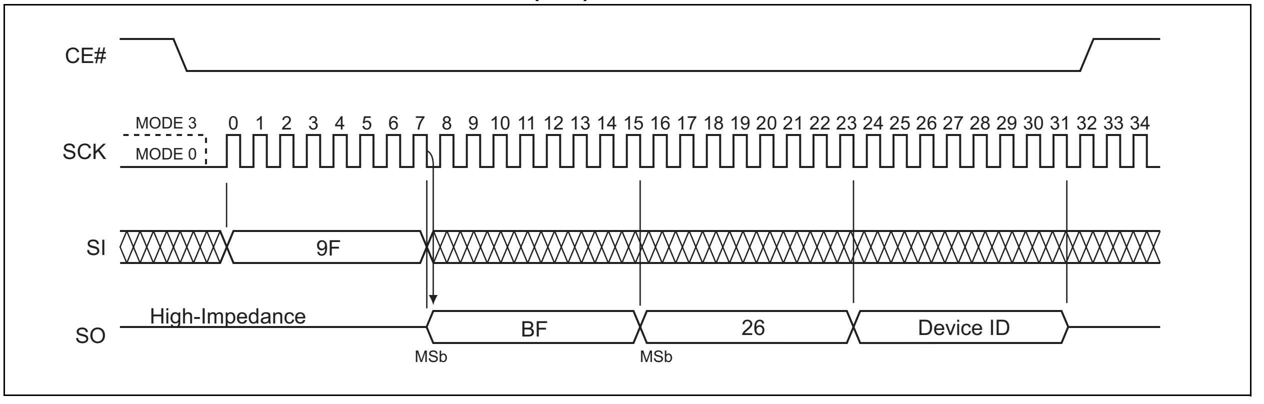
Using traditional SPI protocol, the JEDEC ID Read instruction identifies the device as SST26VF016BEUI and the manufacturer as Microchip. To execute a JEDEC ID operation, the host drives CE# low and then sends the JEDEC ID command cycle (9FH).

Immediately following the command cycle, the SST26VF016BEUI outputs data on the falling edge of the SCK signal. The data output stream is continuous until terminated by a low-to-high transition on CE#. The device outputs three bytes of data: manufacturer, device type and device ID (see Table 5-4). See Figure 5-16 for the instruction sequence.

TABLE 5-4: DEVICE ID DATA OUTPUT

Product	Manufacturer ID (Byte 1)	Device ID	
		Device Type (Byte 2)	Device ID (Byte 3)
SST26VF016BEUI	BFH	26H	41H

FIGURE 5-16: JEDEC ID SEQUENCE (SPI)

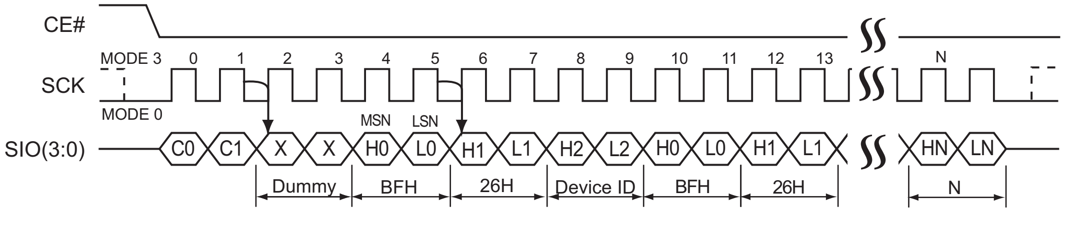


5.15 Read Quad J-ID Read (SQI Protocol)

The Read Quad-ID Read instruction identifies the device as SST26VF016BEUI and manufacturer as Microchip. To execute a Quad J-ID operation, the host drives CE# low and then sends the Quad J-ID command cycle (AFH). Each cycle is two nibbles (clocks) long, most significant nibble first.

Immediately following the command cycle and one dummy cycle, the SST26VF016BEUI outputs data on the falling edge of the SCK signal. The data output stream is continuous until terminated by a low-to-high transition of CE#. The device outputs three bytes of data: manufacturer, device type and device ID (see Table 5-4). See Figure 5-17 for the instruction sequence.

FIGURE 5-17: QUAD J-ID READ SEQUENCE



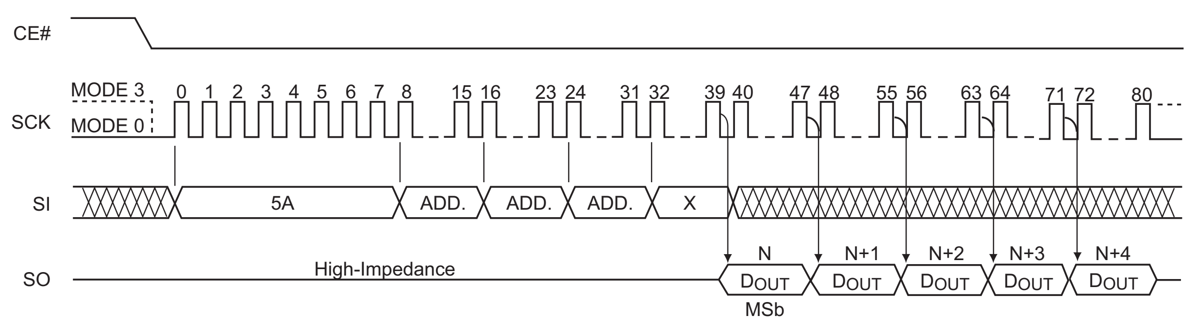
Note: MSN = Most Significant Nibble; LSN= Least Significant Nibble. C[1:0]=AFH

5.16 Serial Flash Discoverable Parameters (SFDP)

The Serial Flash Discoverable Parameters (SFDP) contain information describing the characteristics of the device. This allows device-independent, JEDEC ID-independent and forward/backward compatible software support for all future Serial Flash device families. See Table 11-1 for address and data values.

Initiate SFDP by executing an 8-bit command, 5AH, followed by address bits A[23-0] and a dummy byte. CE# must remain active-low for the duration of the SFDP cycle. For the SFDP sequence, see Figure 5-18.

FIGURE 5-18: SERIAL FLASH DISCOVERABLE PARAMETERS SEQUENCE

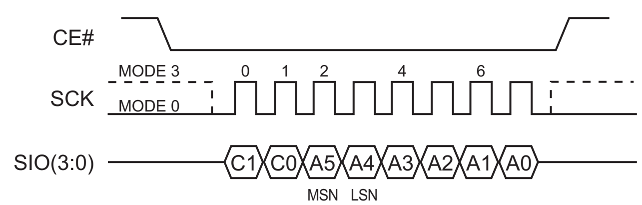


5.17 Sector Erase

The Sector Erase instruction clears all bits in the selected 4-Kbyte sector to '1', but it does not change a protected memory area. Prior to any write operation, the Write Enable (WREN) instruction must be executed.

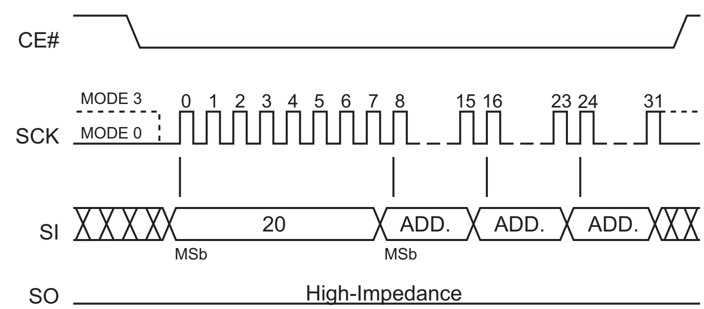
To execute a Sector Erase operation, the host drives CE# low and then sends the Sector Erase command cycle (20H) followed by three address cycles, and then drives CE# high. Address bits [A_{MS}:A_{12}] (A_{MS} = Most Significant Address) determine the sector address (SA_X); the remaining address bits can be V_{IL} or V_{IH}. To identify the completion of the internal, self-timed, write operation, poll the BUSY bit in the Status register or wait T_{SE}. See Figure 5-19 and Figure 5-20 for the Sector-Erase sequence.

FIGURE 5-19: 4-KBYTE SECTOR ERASE SEQUENCE (SQI)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble, C[1:0] = 20H

FIGURE 5-20: 4-KBYTE SECTOR ERASE SEQUENCE (SPI)

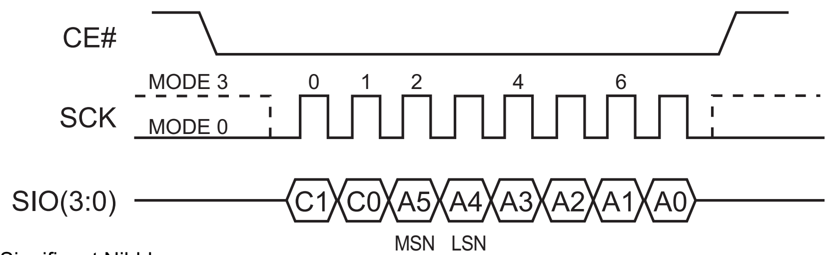


5.18 Block Erase

The Block Erase instruction clears all bits in the selected block to '1'. Block sizes can be 8-Kbyte, 32-Kbyte or 64-Kbyte, depending on address, see Figure 3-1 for details. A Block Erase instruction applied to a protected memory area will be ignored. Prior to any write operation, execute the WREN instruction. Keep CE# active-low for the duration of any command sequence.

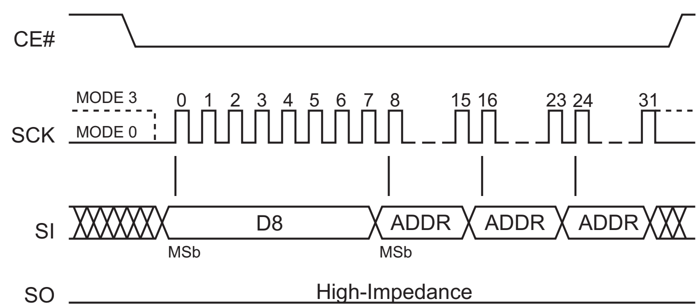
To execute a Block Erase operation, the host drives CE# low and then sends the Block Erase command cycle (D8H) followed by three address cycles, and then drives CE# high. Address bits A_{MS}-A_{13} determine the block address (BA_X); the remaining address bits can be V_{IL} or V_{IH}. For 32-Kbyte blocks, A14:A13 can be V_{IL} or V_{IH}; for 64-Kbyte blocks, A15:A13 can be V_{IL} or V_{IH}. Poll the BUSY bit in the STATUS register or wait T_{BE}, for the completion of the internal, self-timed, Block Erase operation. See Figure 5-21 and Figure 5-22 for the Block Erase sequence.

FIGURE 5-21: BLOCK ERASE SEQUENCE (SQI)



Note: MSN = Most Significant Nibble
LSN = Least Significant Nibble
C[1:0] = D8H

FIGURE 5-22: BLOCK ERASE SEQUENCE (SPI)

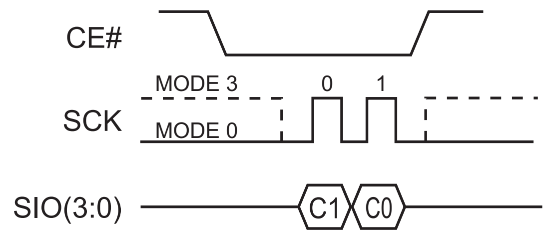


5.19 Chip Erase

The Chip Erase instruction clears all bits in the device to '1.' The Chip Erase instruction is ignored if any part of the memory area is protected. Prior to any write operation, execute the WREN instruction.

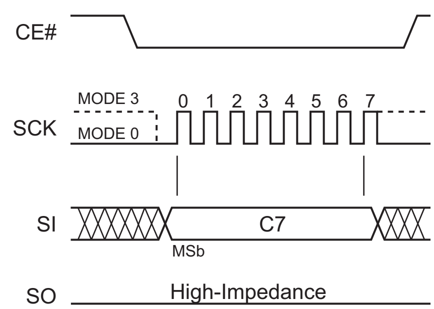
To execute a Chip Erase operation, the host drives CE# low, sends the Chip Erase command cycle (C7H), and then drives CE# high. Poll the BUSY bit in the STATUS register or wait $T_{SCE,}$ for the completion of the internal, self-timed, write operation. See Figure 5-23 and Figure 5-24 for the Chip Erase sequence.

FIGURE 5-23: CHIP ERASE SEQUENCE (SQI)



Note: C[1:0] = C7H

FIGURE 5-24: CHIP ERASE SEQUENCE (SPI)



5.20 Page Program

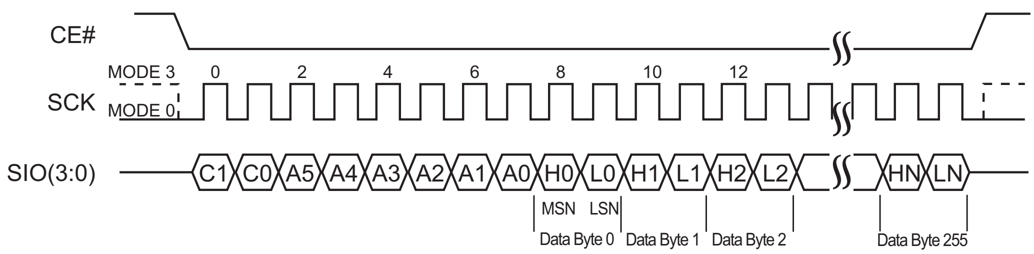
The Page Program instruction programs up to 256 bytes of data in the memory and supports both SPI and SQI protocols. The data for the selected page address must be in the erased state (FFH) before initiating the Page Program operation. A Page Program applied to a protected memory area will be ignored. Prior to the program operation, execute the **WREN** instruction.

To execute a Page Program operation, the host drives CE# low and then sends the Page Program command cycle (02H), followed by three address cycles and the data to be programmed, and then drives CE# high. The programmed data must be between one and 256 bytes and in whole byte increments; sending less than a full byte will cause the partial byte to be ignored.

Poll the BUSY bit in the STATUS register, or wait T_{PP}, for the completion of the internal, self-timed, Write operation. See Figure 5-25 and Figure 5-26 for the Page Program sequence.

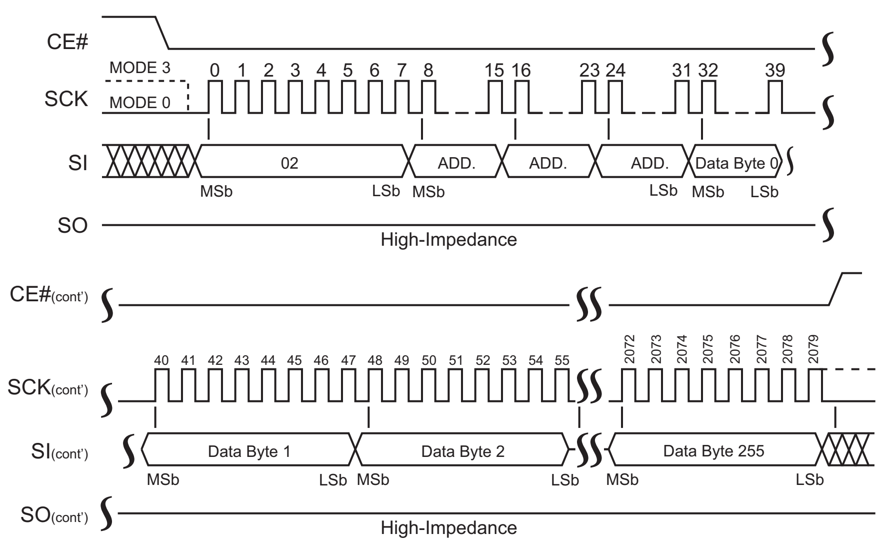
When executing Page Program, the memory range for the SST26VF016BEUI is divided into 256-byte page boundaries. The device handles the shifting of more than 256 bytes of data by maintaining the last 256 bytes of data as the correct data to be programmed. If the target address for the Page Program instruction is not at the beginning of the page boundary (A[7:0] are not all zero) and the number of bytes of data input exceeds or overlaps the end of the address of the page boundary, the excess data inputs wrap around and be programmed at the start of that target page.

FIGURE 5-25: PAGE PROGRAM SEQUENCE (SQI)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble
C[1:0] = 02H

FIGURE 5-26: PAGE PROGRAM SEQUENCE (SPI)



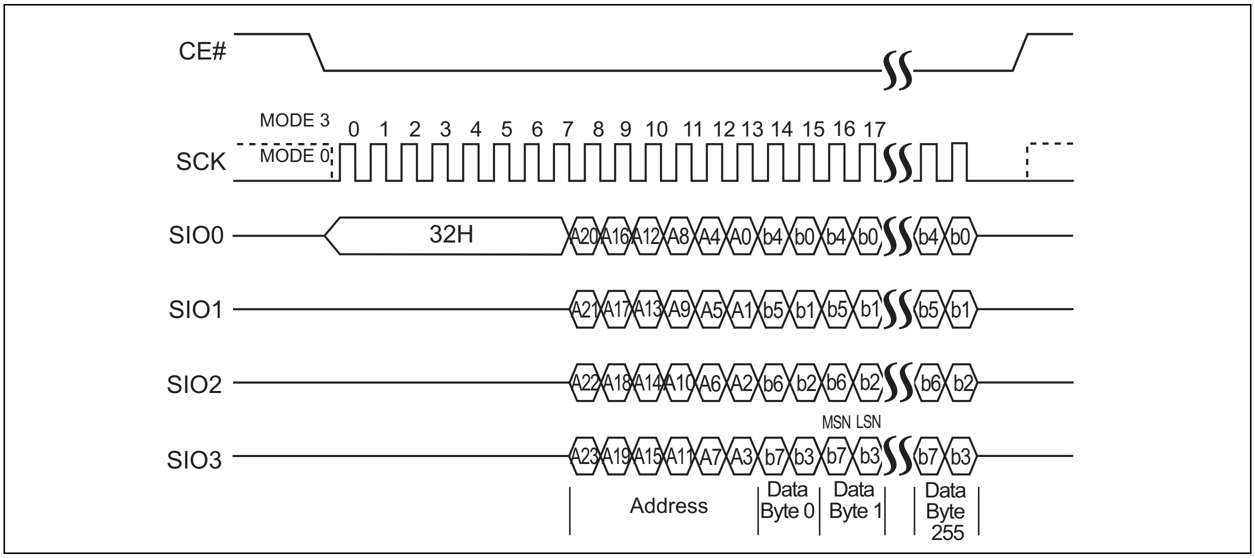
5.21 SPI Quad Page Program

The SPI Quad Page Program instruction programs up to 256 bytes of data in the memory. The data for the selected page address must be in the erased state (FFH) before initiating the SPI Quad Page Program operation. A SPI Quad Page Program applied to a protected memory area will be ignored. The SST26VF016BEUI requires the ICO bit in the Configuration register to be set to '1' prior to executing the command. Prior to the program operation, execute the WREN instruction.

To execute a SPI Quad Page Program operation, the host drives CE# low then sends the SPI Quad Page Program command cycle (32H), followed by three address cycles and the data to be programmed, and then drives CE# high. The programmed data must be between one and 256 bytes and in whole byte increments. The command cycle is eight clocks long, while the address and data cycles are each two clocks long, with the Most Significant bit first. Poll the BUSY bit in the STATUS register, or wait T_{PP}, for the completion of the internal, self-timed, write operation (see Figure 5-27).

When executing SPI Quad Page Program, the memory range for the SST26VF016BEUI is divided into 256-byte page boundaries. The device handles the shifting of more than 256 bytes of data by maintaining the last 256 bytes of data as the correct data to be programmed. If the target address for the SPI Quad Page Program instruction is not the beginning of the page boundary (A[7:0] are not all zero) and the number of bytes of data input exceeds or overlaps the end of the address of the page boundary, the excess data inputs will wrap around and be programmed at the start of that target page.

FIGURE 5-27: SPI QUAD PAGE-PROGRAM SEQUENCE



5.22 Write Suspend and Write Resume

Write Suspend allows the interruption of Sector Erase, Block Erase, SPI Quad Page Program or Page Program operations in order to erase, program or read data in another portion of memory. The original operation can be continued with the Write Resume command. This operation is supported in both SQI and SPI protocols.

Only one write operation can be suspended at a time; if an operation is already suspended, the device will ignore the Write Suspend command. Write Suspend during Chip Erase is ignored; Chip Erase is not a valid command while a write is suspended. The Write Resume command is ignored until any write operation (Program or Erase) initiated during the Write Suspend is complete. The device requires a minimum of 500 µs between each Write Suspend command.

5.23 Write Suspend During Sector Erase or Block Erase

Issuing a Write Suspend instruction during Sector Erase or Block Erase allows the host to program or read any sector that was not being erased. The device will ignore any programming commands pointing to the suspended sector(s). Any attempt to read from the suspended sector(s) will output unknown data because the Sector or Block Erase will be incomplete.

To execute a Write Suspend operation, the host drives CE# low, sends the Write Suspend command cycle (B0H), and then drives CE# high. The STATUS register indicates that the erase has been suspended by changing the WSE bit from '0' to '1', but the device will not accept another command until it is ready.

To determine when the device will accept a new command, poll the BUSY bit in the STATUS register or wait TWS.

5.24 Write Suspend During Page Programming or SPI Quad Page Programming

Issuing a Write Suspend instruction during Page Programming allows the host to erase or read any sector that is not being programmed. Erase commands pointing to the suspended sector(s) will be ignored. Any attempt to read from the suspended page will output unknown data because the program will be incomplete.

To execute a Write Suspend operation, the host drives CE# low, sends the Write Suspend command cycle (B0H), and then drives CE# high. The STATUS register indicates that the programming has been suspended by changing the WSP bit from '0' to '1', but the device will not accept another command until it is ready. To determine when the device will accept a new command, poll the BUSY bit in the STATUS register or wait TWS.

5.25 Write Resume

The Write Resume command restarts a write command that was suspended and changes the suspend status bit in the STATUS register (WSE or WSP) back to '0'.

To execute a Write Resume operation, the host drives CE# low, sends the Write Resume command cycle (30H), and then drives CE# high. To determine if the internal, self-timed Write operation completed, poll the BUSY bit in the STATUS register or wait the specified time TSE, TBE or TPP for Sector Erase, Block Erase, or Page Programming, respectively. The total write time before suspend and after resume will not exceed the uninterrupted write times TSE, TBE or TPP.

5.26 Read Security ID

The Read Security ID operation is supported in both SPI and SQI modes. To execute a Read Security ID (SID) operation in SPI mode, the host drives CE# low and then sends the Read Security ID command cycle (88H), followed by two address cycles and then one dummy cycle. To execute a Read Security ID operation in SQI mode, the host drives CE# low, and then sends the Read Security ID command, two address cycles and three dummy cycles.

After the dummy cycles, the device outputs data on the falling edge of the SCK signal, starting from the specified address location. The data output stream are continuous through all SID addresses until terminated by a low-to-high transition on CE#. See Table 5-5 for the Security ID address range.

5.27 Program Security ID

The Program Security ID instruction programs one to 2,040 bytes of data in the user-programmable, Security ID space. This Security ID space is One-Time-Programmable (OTP). The device ignores a Program Security ID instruction that points to an invalid or protected address (see Table 5-5). Prior to the program operation, execute WREN.

To execute a Program SID operation, the host drives CE# low and then sends the Program Security ID command cycle (A5H), followed by two address cycles and the data to be programmed, and then drives CE# high. The programmed data must be between one and 256 bytes and in whole byte increments.

The device handles the shifting of more than 256 bytes of data by maintaining the last 256 bytes of data as the correct data to be programmed. If the target address for the Program Security ID instruction is not at the beginning of the page boundary and the number of data input exceeds or overlaps the end of the address of the page boundary, the excess data inputs wrap around and will be programmed at the start of that target page.

The Program Security ID operation is supported in both SPI and SQI mode. To determine the completion of the internal, self-timed Program SID operation, poll the BUSY bit in the software STATUS register or wait TPSID for the completion of the internal self-timed Program Security ID operation.

TABLE 5-5: PROGRAM SECURITY ID

Program Security ID	Address Range
Unique ID Pre-Programmed at factory	0000–0007H
User Programmable	0008H–07FFH

5.28 Lockout Security ID

The Lockout Security ID instruction prevents any future changes to the Security ID and is supported in both SPI and SQI modes. Prior to the operation, execute WREN.

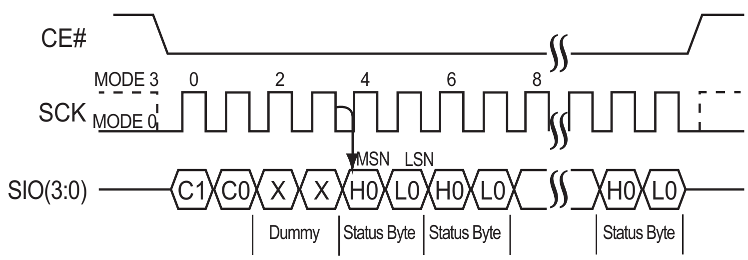
To execute a Lockout SID, the host drives CE# low, sends the Lockout Security ID command cycle (85H), and then drives CE# high. Poll the BUSY bit in the software STATUS register or wait TPSID for the completion of the Lockout Security ID operation.

5.29 Read Status Register (RDSR) and Read Configuration Register (RDCR)

The Read STATUS Register (RDSR) and Read Configuration Register (RDCR) commands output the contents of the STATUS and Configuration registers, respectively. These commands function in both SPI and SQI modes. The STATUS register can be read at any time, even during a Write operation. When a write is in progress, poll the BUSY bit before sending any new commands to ensure that the device properly receives the new commands.

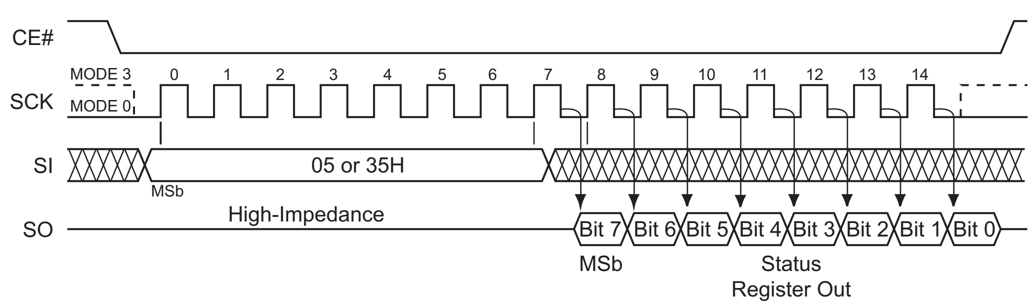
To read the STATUS or Configuration registers, the host drives CE# low, and then sends the Read STATUS Register command cycle (05H) or the Read Configuration Register command (35H). A dummy cycle is required in SQI mode. Immediately after the command cycle, the device outputs data on the falling edge of the SCK signal. The data output stream continues until terminated by a low-to-high transition on CE#. See Figure 5-28 and Figure 5-29 for the instruction sequence.

FIGURE 5-28: READ STATUS REGISTER AND READ CONFIGURATION REGISTER SEQUENCE (SQI)



Note: MSN = Most Significant Nibble; LSN = Least Significant Nibble, C[1:0]=05H or 35H

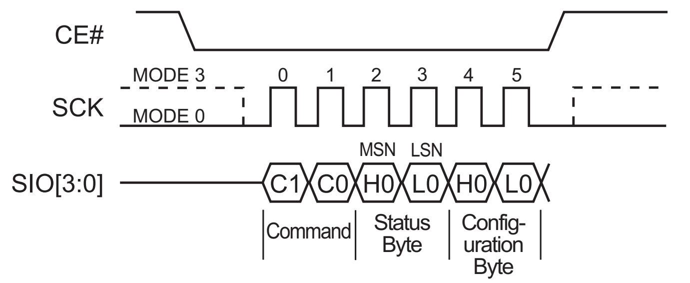
FIGURE 5-29: READ STATUS REGISTER AND READ CONFIGURATION REGISTER SEQUENCE (SPI)



5.30 Write STATUS Register (WRSR)

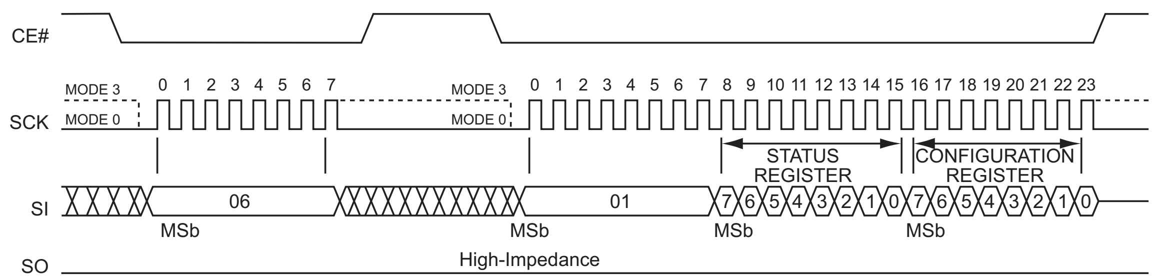
The Write STATUS Register (WRSR) command writes new values to the Configuration register. To execute a Write STATUS Register operation, the host drives CE# low and then sends the Write STATUS Register command cycle (01H), followed by two cycles of data, and then drives CE# high. Values in the second data cycle will be accepted by the device (see Figure 5-30 and Figure 5-31).

FIGURE 5-30: WRITE STATUS REGISTER SEQUENCE (SQI)



Note: MSN = Most Significant Nibble; LSN = Least Significant Nibble, XX = Don't Care, C[1:0]=01H

FIGURE 5-31: WRITE STATUS REGISTER SEQUENCE (SPI)



Note: XX = Don't Care

5.31 Write Enable (WREN)

The Write Enable (WREN) instruction sets the Write Enable Latch bit in the STATUS register to '1', allowing Write operations to occur. The WREN instruction must be executed prior to any of the following operations: Sector Erase, Block Erase, Chip Erase, Page Program, Program Security ID, Lockout Security ID, Write Block Protection Register, Lock-Down Block Protection Register, Nonvolatile Write Lock Lock-Down Register, SPI Quad Page program and Write STATUS Register. To execute a Write Enable, the host drives CE# low and then sends the Write Enable command cycle (06H), and then drives CE# high. See Figures Figure 5-32 and Figure 5-33 for the WREN instruction sequence.

FIGURE 5-32: WRITE ENABLE SEQUENCE (SQI)

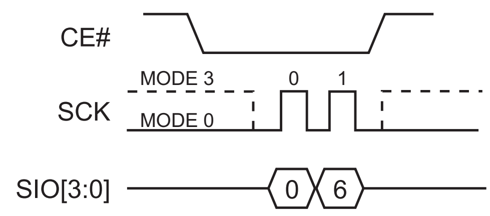
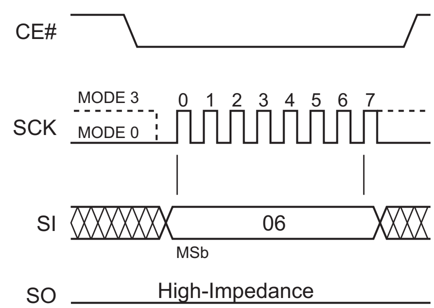


FIGURE 5-33: WRITE ENABLE SEQUENCE (SPI)



5.32 Write Disable (WRDI)

The Write Disable (WRDI) instruction sets the Write Enable Latch bit in the STATUS register to '0', preventing write operations. The WRDI instruction is ignored during any internal write operations. Any write operation started before executing WRDI will complete. Drive CE# high before executing WRDI.

To execute a Write Disable, the host drives CE# low, sends the Write Disable command cycle (04H), and then drives CE# high (see Figure 5-34 and Figure 5-35).

FIGURE 5-34: WRITE DISABLE (WRDI) SEQUENCE (SQI)

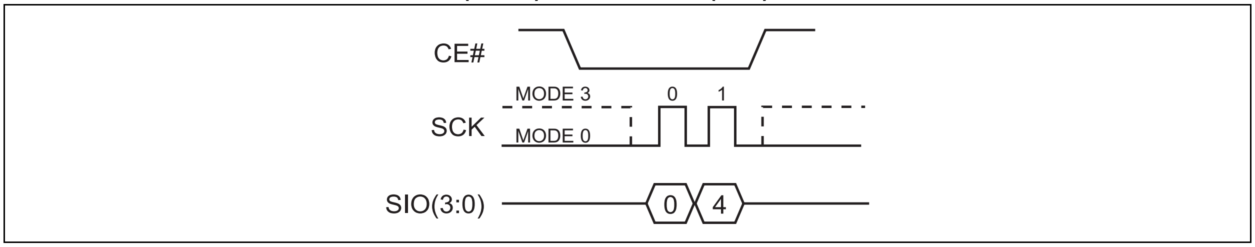
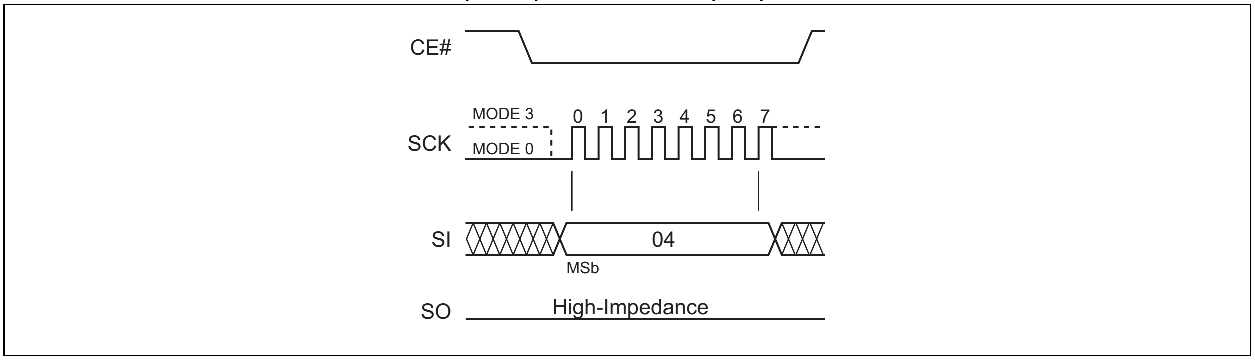


FIGURE 5-35: WRITE DISABLE (WRDI) SEQUENCE (SPI)

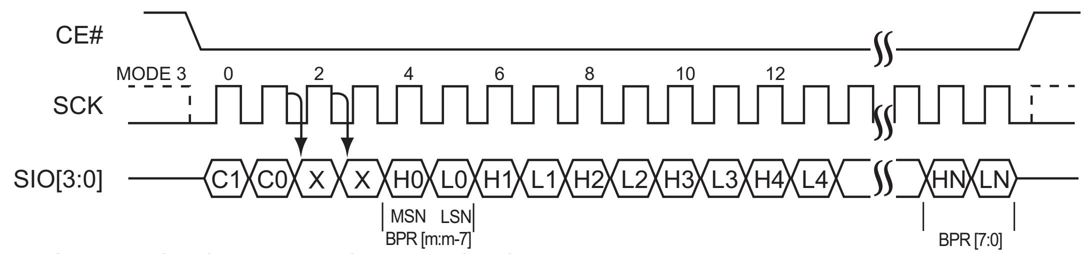


5.33 Read Block Protection Register (RBPR)

The Read Block Protection Register instruction outputs the Block Protection register data, which determines the protection status. To execute a Read Block Protection register operation, the host drives CE# low and then sends the Read Block Protection register command cycle (72H). A dummy cycle is required in SQI mode.

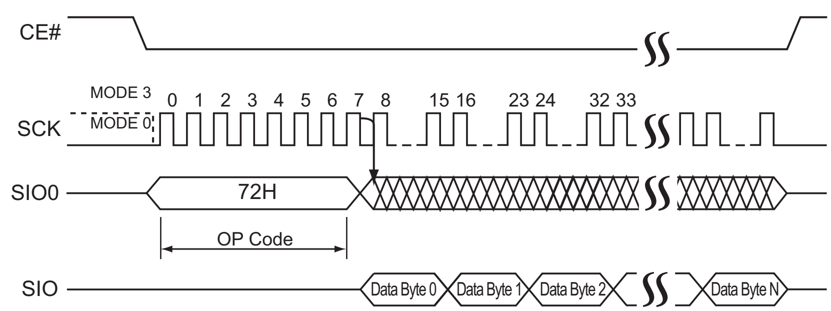
After the command cycle, the device outputs data on the falling edge of the SCK signal starting with the Most Significant bit(s); see Table 5-6 for definitions of each bit in the Block Protection register. The RBPR command does not wrap around. After all data have been output, the device will output 0H until terminated by a low-to-high transition on CE# (see Figure 5-36 and Figure 5-37).

FIGURE 5-36: READ BLOCK PROTECTION REGISTER SEQUENCE (SQI)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble
Block-Protection Register (BPR), m = 47 for SST26VF016BEUI, C[1:0]=72H

FIGURE 5-37: READ BLOCK PROTECTION REGISTER SEQUENCE (SPI)

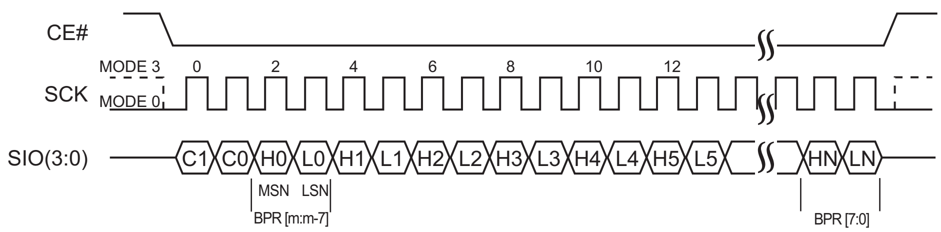


5.34 Write Block Protection Register (WBPR)

The Write Block Protection Register (WBPR) command changes the Block Protection register data to indicate the protection status. Execute WREN before executing WBPR.

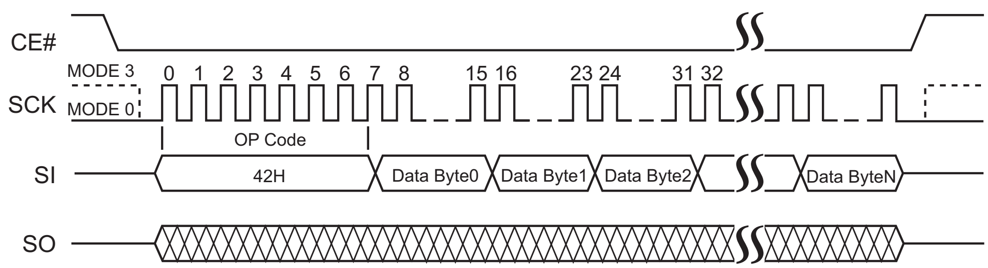
To execute a Write Block Protection register operation, the host drives CE# low, sends the Write Block Protection register command cycle (42H), sends 18 cycles of data, and finally drives CE# high. Data input must be Most Significant bit(s) first. See Table 5-6 for definitions of each bit in the Block Protection register (see Figure 5-38 and Figure 5-39).

FIGURE 5-38: WRITE BLOCK PROTECTION REGISTER SEQUENCE (SQI)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble
Block Protection Register (BPR) m = 47, C[1:0]=42H.

FIGURE 5-39: WRITE BLOCK PROTECTION REGISTER SEQUENCE (SPI).



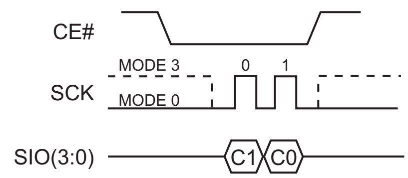
Note: C[1:0]=42H

5.35 Lock-Down Block Protection Register (LBPR)

The Lock-Down Block Protection register instruction prevents changes to the Block Protection register during device operation. Lock-Down resets after power cycling; this allows the Block Protection register to be changed. Execute WREN before initiating the Lock-Down Block Protection register instruction.

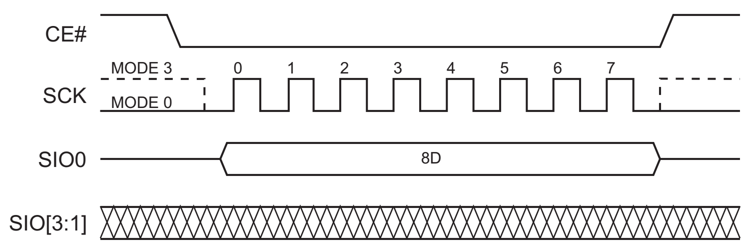
To execute a Lock-Down Block Protection Register instruction, the host drives CE# low, then sends the Lock-Down Block Protection register command cycle (8DH), and then drives CE# high.

FIGURE 5-40: LOCK-DOWN BLOCK PROTECTION REGISTER (SQI)



Note: C[1:0]=8DH

FIGURE 5-41: LOCK-DOWN BLOCK PROTECTION REGISTER (SPI)



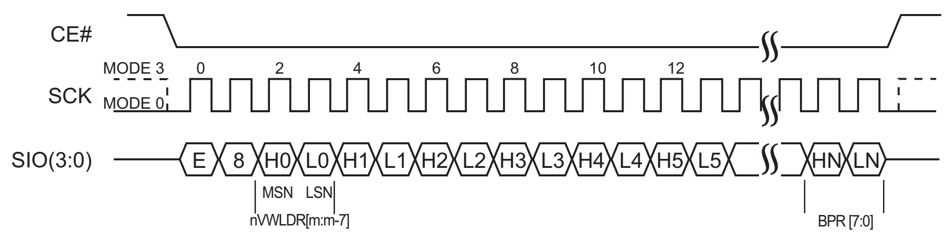
5.36 Nonvolatile Write Lock Lock-Down Register (nVWLDR)

The Nonvolatile Write Lock Lock-Down Register (nVWLDR) instruction controls the ability to change the Write-Lock bits in the Block Protection register. Execute WREN before initiating the nVWLDR instruction.

To execute nVWLDR, the host drives CE# low and then sends the nVWLDR command cycle (E8H), followed by 18 cycles of data, and then drives CE# high.

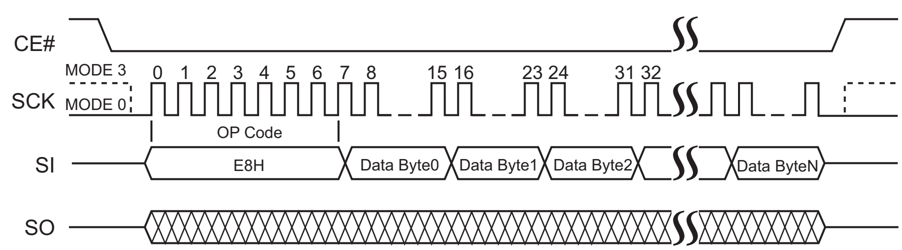
After CE# goes high, the nonvolatile bits are programmed and the programming time-out must complete before any additional commands, other than Read STATUS register, can be entered. Poll the BUSY bit in the STATUS register or wait TPP for the completion of the internal, self-timed, write operation. Data inputs must be Most Significant bit(s) first.

FIGURE 5-42: WRITE LOCK LOCK-DOWN REGISTER SEQUENCE (SQI)



Note: MSN= Most Significant Nibble; LSN = Least Significant Nibble
Write Lock Lock-Down Register (nVWLDR) m = 47

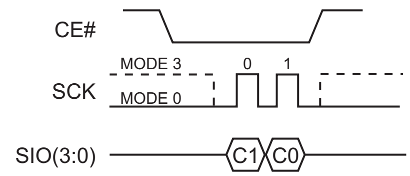
FIGURE 5-43: WRITE LOCK LOCK-DOWN REGISTER SEQUENCE (SPI)



5.37 Global Block Protection Unlock (ULBPR)

The Global Block Protection Unlock (ULBPR) instruction clears all write protection bits in the Block Protection register, except for those bits that have been locked down with the nVWLDR command. Execute WREN before initiating the ULBPR instruction. To execute a ULBPR instruction, the host drives CE# low, then sends the ULBPR command cycle (98H), and then drives CE# high.

FIGURE 5-44: GLOBAL BLOCK PROTECTION UNLOCK (SQI)



Note: C[1:0]=98H

FIGURE 5-45: GLOBAL BLOCK PROTECTION UNLOCK (SPI)

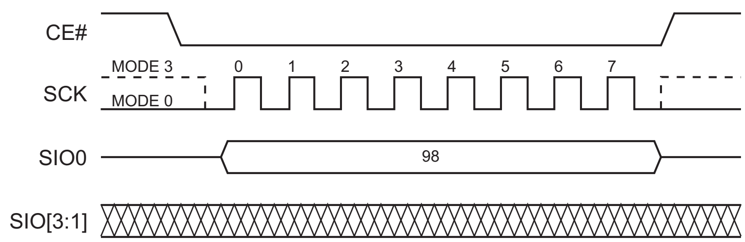


TABLE 5-6: BLOCK PROTECTION REGISTER FOR SST26VF016BEUI [(1)]

BPR Bits		Address Range	Protected Block Size
Read Lock	Write Lock/nVWLDR[(1)]		
47	46	1FE000H-1FFFFFH	8 Kbytes
45	44	1FC000H-1FDFFFH	8 Kbytes
43	42	1FA000H-1FBFFFH	8 Kbytes
41	40	1F8000H-1F9FFFH	8 Kbytes
39	38	006000H-007FFFH	8 Kbytes
37	36	004000H-005FFFH	8 Kbytes
35	34	002000H-003FFFH	8 Kbytes
33	32	000000H-001FFFH	8 Kbytes
	31	1F0000H-1F7FFFH	32 Kbytes
	30	008000H-00FFFFH	32 Kbytes
	29	1E0000H-1EFFFFH	64 Kbytes
	28	1D0000H-DFFFFH	64 Kbytes
	27	1C0000H-CFFFFH	64 Kbytes
	26	1B0000H-1BFFFFH	64 Kbytes
	25	1A0000H-1AFFFFH	64 Kbytes
	24	190000H-19FFFFH	64 Kbytes
	23	180000H-18FFFFH	64 Kbytes
	22	170000H-17FFFFH	64 Kbytes
	21	160000H-16FFFFH	64 Kbytes
	20	150000H-15FFFFH	64 Kbytes
	19	140000H-14FFFFH	64 Kbytes
	18	130000H-13FFFFH	64 Kbytes
	17	120000H-12FFFFH	64 Kbytes
	16	110000H-11FFFFH	64 Kbytes
	15	100000H-10FFFFH	64 Kbytes
	14	0F0000H-0FFFFFH	64 Kbytes
	13	0E0000H-0EFFFFH	64 Kbytes
	12	0D0000H-0DFFFFH	64 Kbytes
	11	0C0000H-0CFFFFH	64 Kbytes
	10	0B0000H-0BFFFFH	64 Kbytes
	9	0A0000H-0AFFFFH	64 Kbytes
	8	090000H-09FFFFH	64 Kbytes
	7	080000H-08FFFFH	64 Kbytes
	6	070000H-07FFFFH	64 Kbytes
	5	060000H-06FFFFH	64 Kbytes
	4	050000H-05FFFFH	64 Kbytes
	3	040000H-04FFFFH	64 Kbytes
	2	030000H-03FFFFH	64 Kbytes
	1	020000H-02FFFFH	64 Kbytes
	0	010000H-01FFFFH	64 Kbytes

Note 1: The default state after a Power-On Reset is write-protected BPR[47:0] = 5555 FFFF FFFF

5.38 Deep Power-Down

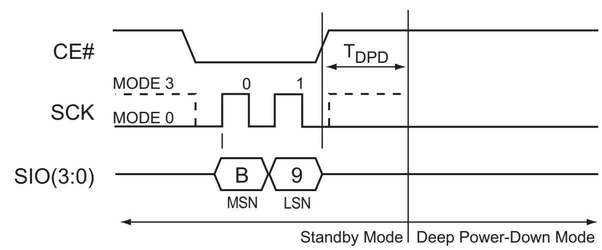
The Deep Power-down (DPD) instruction puts the device in the lowest power consumption mode: Deep Power-down mode. The Deep Power-down instruction is ignored during an internal write operation. While the device is in Deep Power-down mode, all instructions will be ignored except for the Release Deep Power-down instruction.

Enter Deep Power-down mode by initiating the Deep Power-down (DPD) instruction (B9H) while driving CE# low. CE# must be driven high before executing the DPD instruction. After CE# is driven high, it requires a delay of T_{DPD} before the standby current I_{SB} is reduced to deep power-down current I_{DPD}. See Table 5-7 for Deep Power-down timing. If the device is busy performing an internal erase or program operation, initiating a Deep Power-down instruction will not placed the device in Deep Power-down mode. See Figure 5-46 and Figure 5-47 for the DPD instruction sequence.

TABLE 5-7: DEEP POWER-DOWN

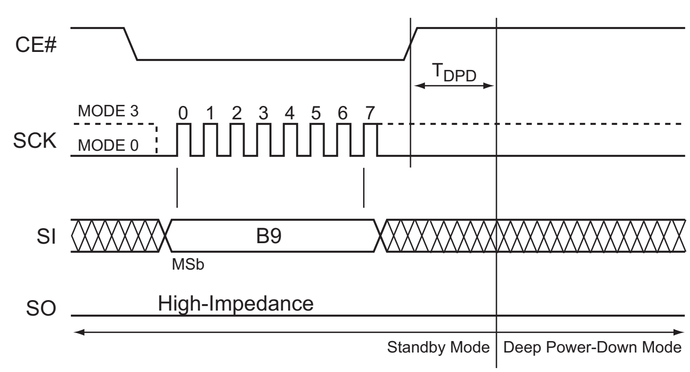
Symbol	Parameter	Minimum	Maximum	Units
TDPD	CE# High to Deep Power-down		3	µs
TSBR	CE# High to Standby Mode		10	µs

FIGURE 5-46: DEEP POWER-DOWN (DPD) SEQUENCE (SQI)



Note: MSN= Most Significant Nibble; LSN = Least Significant Nibble

FIGURE 5-47: DEEP POWER-DOWN (DPD) (SPI)

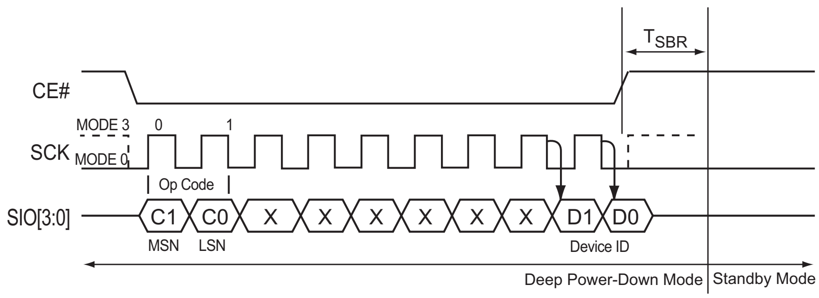


5.39 Release from Deep Power-Down and Read ID

Release from Deep Power-Down (`RDPD`) and Read ID instructions exit Deep Power-down mode. To exit Deep Power-down mode, execute the **`RDPD`** instruction. During this command, the host drives CE# low, then sends the Deep Power-down command cycle (ABH) and then drives CE# high. The device will return to Standby mode and be ready for the next instruction after T_{SBR}.

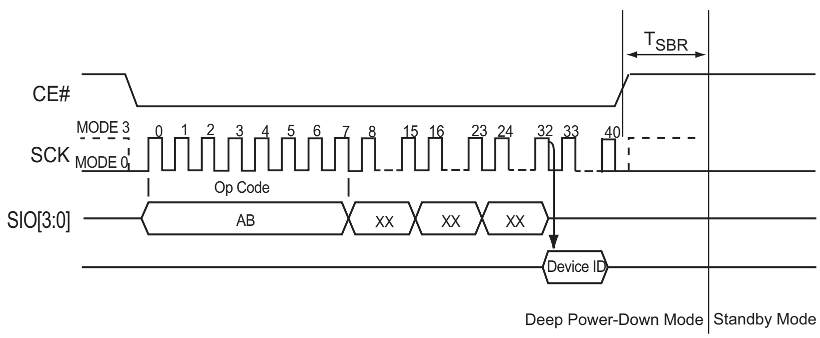
To execute `RDPD` and read the Device ID, the host drives CE# low, then sends the Deep Power-down command cycle (ABH), followed by three dummy clock cycles, and then drives CE# high. The device outputs the Device ID on the falling edge of the SCK signal following the dummy cycles. The data output stream is continuous until terminated by a low-to-high transition on CE# and will return to Standby mode and be ready for the next instruction after T_{SBR}. See Figure 5-48 and Figure 5-49 for the command sequence.

FIGURE 5-48: RELEASE FROM DEEP POWER-DOWN (RDPD) AND READ ID SEQUENCE (SQI)



Note: C[1:0]=ABH

FIGURE 5-49: RELEASE FROM DEEP POWER-DOWN (RDPD) AND READ ID SEQUENCE (SPI)



6.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (†)

Temperature under bias .... -55°C to +125°C
Storage temperature .... -65°C to +150°C
DC voltage on any pin to ground potential .... -0.5V to VDD+0.5V
Transient voltage (< 20 ns) on any pin to ground potential .... -2.0V to VDD+2.0V
Package Power Dissipation Capability (TA = +25°C) 1.0W
Surface mount solder reflow temperature .... +260°C for 10 seconds
Output short circuit current(1) .... 50 mA

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Output shorted for no more than one second. No more than one output shorted at a time.

TABLE 6-1: OPERATING RANGE

Range	Ambient Temp	V_{DD}
Industrial	-40°C to +85°C	2.3V-3.6V

TABLE 6-2: AC CONDITIONS OF TEST(1)

Input Rise/Fall Time	Output Load
3 ns	C_L = 30 pF

Note 1: See Figure 8-5.

6.1 Power-Up Specifications

All functionalities and DC specifications are specified for a V_{DD} ramp rate of greater than 1V per 100 ms (0V to 3.0V in less than 300 ms). See Table 6-3 and Figure 6-1 for more information.

When V_{DD} drops from the operating voltage to below the minimum V_{DD} threshold at power-down, all operations are disabled and the device does not respond to commands. Data corruption may result if a power-down occurs while a write registers, program, or erase operation is in progress (see Figure 6-2).

TABLE 6-3: RECOMMENDED SYSTEM POWER-UP/DOWN TIMINGS

Symbol	Parameter	Minimum	Maximum	Units	Condition
TPU-READ(1)	VDD Min to Read Operation	100	—	µs	
TPU-WRITE(1)	VDD Min to Write Operation	100	—	µs	
TPD(1)	Power-down Duration	100	—	ms	
VOFF	VDD off time	—	0.3	V	0V recommended

Note 1: This parameter is measured only for initial qualification and after a design or precess change that could affect this parameter.

FIGURE 6-1: POWER-UP TIMING DIAGRAM

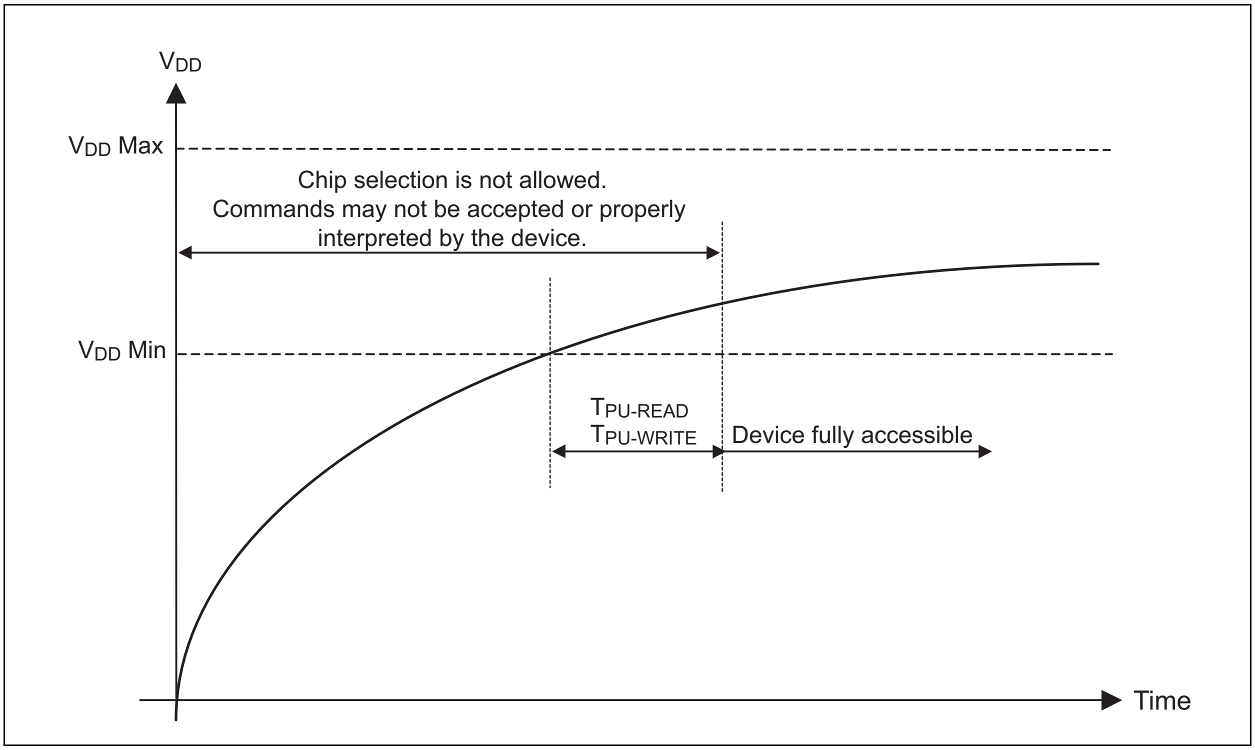
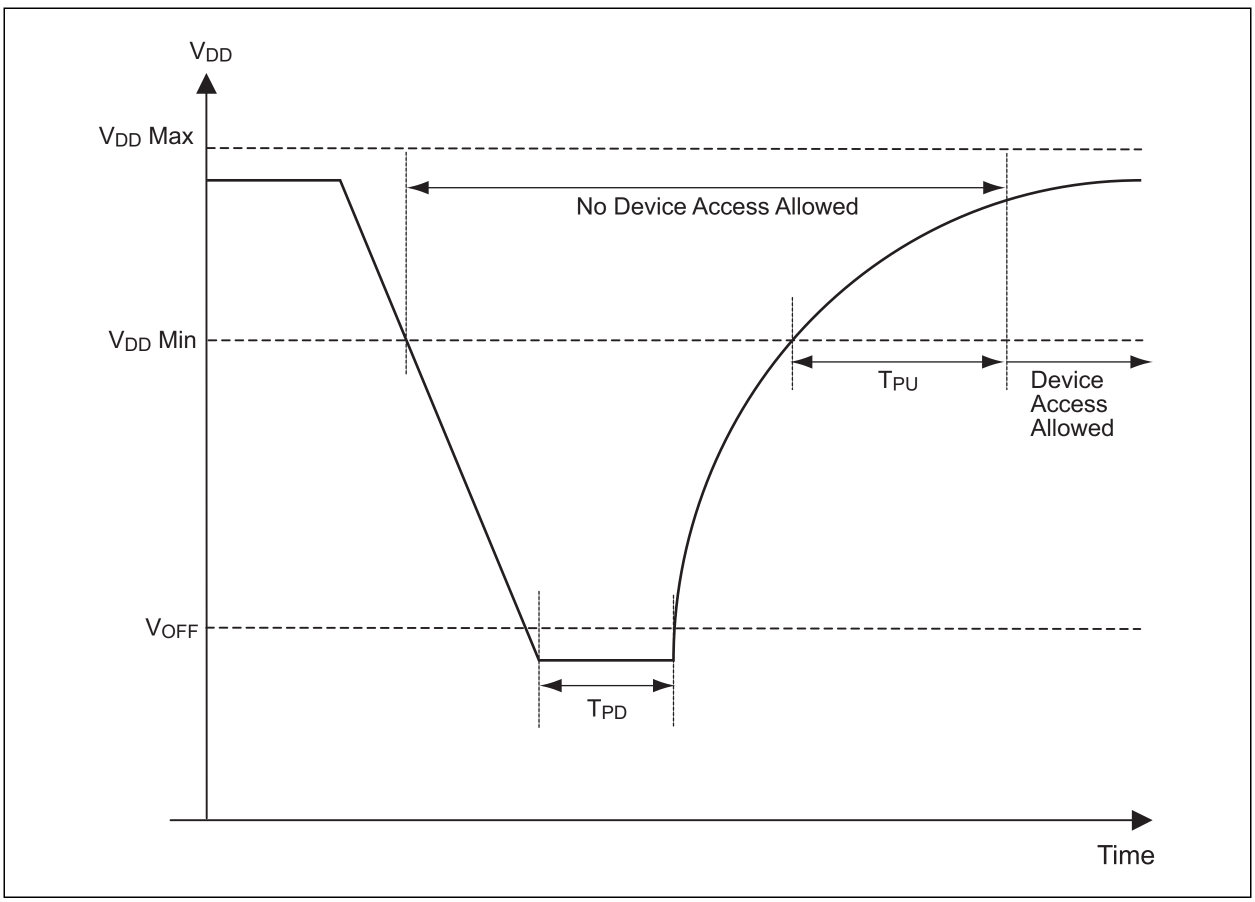


FIGURE 6-2: POWER-DOWN AND VOLTAGE DROP DIAGRAM



7.0 DC CHARACTERISTICS

TABLE 7-1: DC OPERATING CHARACTERISTICS (VDD = 2.3V-3.6V)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Units	
IDDR1	Read Current	—	8	15	mA	VDD=VDD maximum CE# = 0.1 VDD/0.9 VDD@40 MHz, SO = open
IDDR2	Read Current	—	—	20	mA	VDD = VDD maximum CE# = 0.1 VDD/0.9 VDD@104 MHz, SO = open
IDDW	Program and Erase Current	—	—	25	mA	VDD maximum
ISB1	Standby Current	—	15	45	µA	CE# = VDD, VIN = VDD or VSS@105°C
ISB2	Standby Current	—	—	80	µA	CE# = VDD, VIN = VDD or VSS@125°C
IDPD	Deep Power-down Current	—	8	25	µA	CE# = VDD, VIN = VDD or VSS
ILI	Input Leakage Current	—	—	2	µA	VIN = GND to VDD, VDD =VDD maximum
ILO	Output Leakage Current	—	—	2	µA	VOUT = GND to VDD, VDD = VDD maximum
VIL	Input Low-Voltage	—	—	0.8	V	VDD = VDD minimum
VIH	Input High-Voltage	0.7 VDD	—	—	V	VDD = VDD maximum
VOH	Output Low-Voltage	—	—	0.2	V	IOL = 100 µA, VDD = VDD minimum
VOH	Output High-Voltage	VDD-0.2	—	—	V	IOH = -100 µA, VDD = VDD minimum

TABLE 7-2: CAPACITANCE (TA = +25°C, F=1 MHZ, OTHER PINS OPEN)

Parameter	Description	Test Condition	Maximum
COUT(1)	Output Pin Capacitance	VOUT = 0V	8 pF
CIN(1)	Input Capacitance	VIN = 0V	6 pF

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 7-3: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
NEND(1)	Endurance	100,000	cycles	JEDEC Standard A117
TDR(1)	Data Retention	100	years	JEDEC Standard A103
ILTH(1)	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 7-4: WRITE TIMING PARAMETERS (VDD = 2.3V-3.6V)

Symbol	Parameter	Minimum	Maximum	Units
TSE	Sector Erase	—	25	ms
TBE	Block Erase	—	25	ms
TSCE	Chip Erase	—	50	ms
TPP(1)	Page Program	—	1.5	ms
TPSID	Program Security ID	—	1.5	ms
TWS	Write Suspend Latency	—	25	µs
TWPEN	Write Protection Enable Bit Latency	—	25	ms

Note 1: Estimate for typical conditions less than 256 bytes: Programming Time (µs) = 55 + (3.75 x # of bytes)

8.0 AC CHARACTERISTICS

TABLE 8-1: AC OPERATING CHARACTERISTICS (V_{DD}[1] = 2.3V-3.6V)

Symbol	Parameter	Limits - 40 MHz		Limits - 80 MHz[2]		Limits - 104 MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
F_{CLK}	Serial Clock Frequency	—	40	—	80	—	104	MHz
T_{CLK}	Serial Clock Period	—	25	—	12.5	—	9.6	ns
T_{SCKH}	Serial Clock High Time	11	—	5.5	—	4.5	—	ns
T_{SCKL}	Serial Clock Low Time	11	—	5.5	—	4.5	—	ns
T_{SCKR}[3]	Serial Clock Rise Time (slew rate)	0.1	—	0.1	—	0.1	—	V/ns
T_{SCKF}[3]	Serial Clock Fall Time (slew rate)	0.1	—	0.1	—	0.1	—	V/ns
T_{CES}[4]	CE# Active Setup Time	8	—	5	—	5	—	ns
T_{CEH}[4]	CE# Active Hold Time	8	—	5	—	5	—	ns
T_{CHS}[4]	CE# Not Active Setup Time	8	—	5	—	5	—	ns
T_{CHH}[4]	CE# Not Active Hold Time	8	—	5	—	5	—	ns
T_{CPH}	CE# High Time	25	—	12.5	—	12	—	ns
T_{CHZ}	CE# High to High-Z Output	—	19	—	12.5	—	12	ns
T_{CLZ}	SCK Low to Low-Z Output	0	—	0	—	0	—	ns
T_{HLS}	HOLD# Low Setup Time	8	—	5	—	5	—	ns
T_{HHS}	HOLD# High Setup Time	8	—	5	—	5	—	ns
T_{HLH}	HOLD# Low Hold Time	8	—	5	—	5	—	ns
T_{HHH}	HOLD# High Hold Time	8	—	5	—	5	—	ns
T_{HZ}	HOLD# Low-to-High-Z Output	—	8	—	8	—	8	ns
T_{LZ}	HOLD# High-to-Low-Z Output	—	8	—	8	—	8	ns
T_{DS}	Data In Setup Time	3	—	3	—	3	—	ns
T_{DH}	Data In Hold Time	4	—	4	—	4	—	ns
T_{OH}	Output Hold from SCK Change	0	—	0	—	0	—	ns
T_V	Output Valid from SCK	—	8/5 [5]	—	8/5 [5]	—	8/5 [5]	ns

Note 1: Maximum operating frequency for 2.7 to 3.6V is 104 MHz and for 2.3 to 3.6V is 80 MHz.
2: Maximum frequency for 125°C is 80 MHz.
3: Maximum Rise and Fall time may be limited by T_{SCKH} and Tsckl requirements.
4: Relative to SCK.
5: 30 pF/10 pF.

FIGURE 8-1: HOLD TIMING DIAGRAM

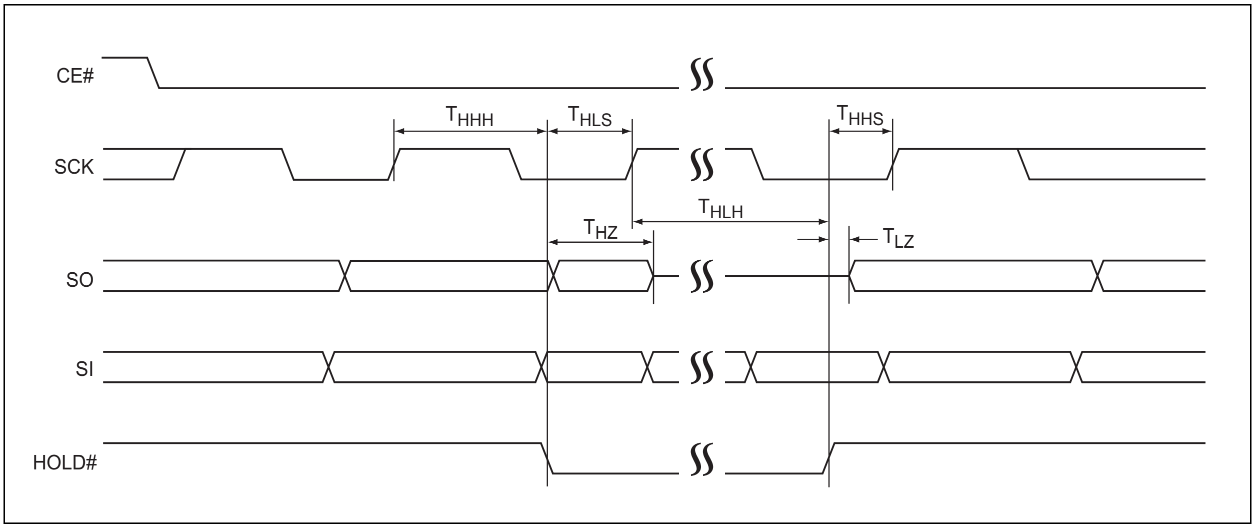


FIGURE 8-2: SERIAL INPUT TIMING DIAGRAM

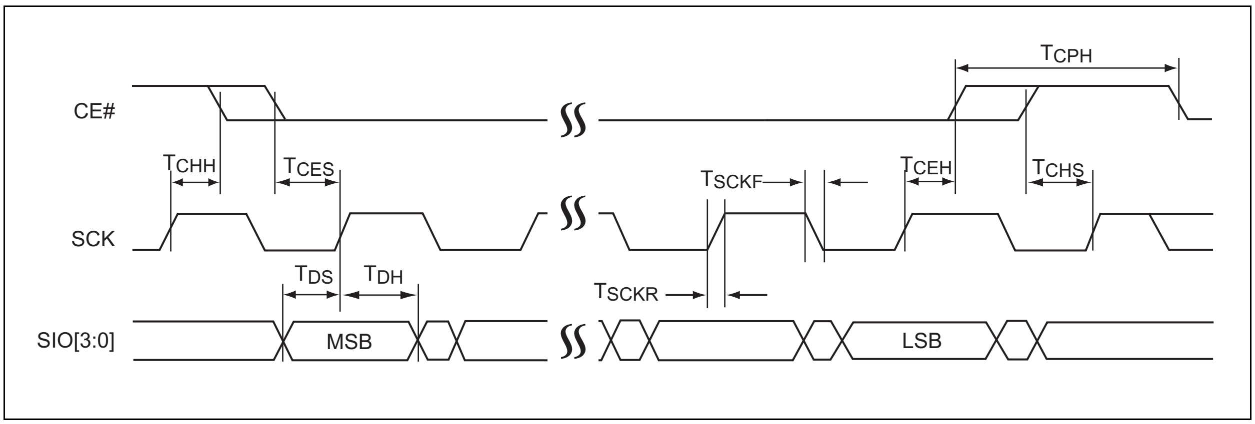


FIGURE 8-3: SERIAL OUTPUT TIMING DIAGRAM

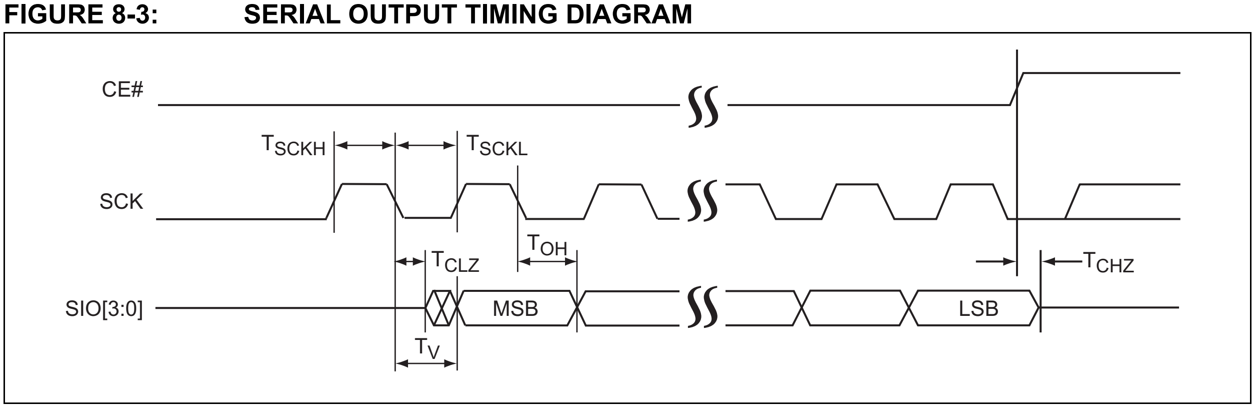
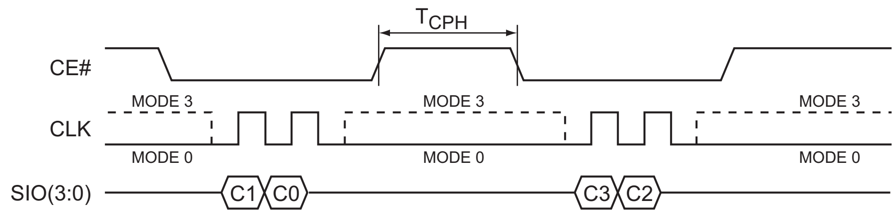


TABLE 8-2: RESET TIMING PARAMETERS

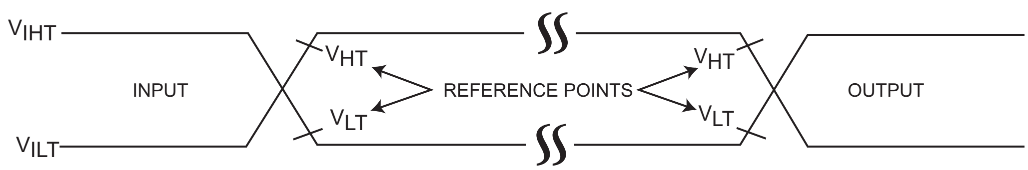
TR(I)	Parameter	Minimum	Maximum	Units
TR(O)	Reset to Read (non-data operation)	—	20	ns
TR(P)	Reset Recovery from Program or Suspend	—	100	µs
TR(E)	Reset Recovery from Erase	—	1	ms

FIGURE 8-4: RESET TIMING DIAGRAM



Note: C[1:0] = 66H; C[3:2] = 99H

FIGURE 8-5: AC INPUT/OUTPUT REFERENCE WAVEFORMS



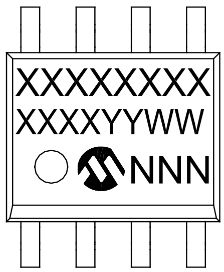
Note: AC test inputs are driven at V_{IHT} ($0.9V_{DD}$) for a logic ‘1’ and V_{ILT} ($0.1V_{DD}$) for a logic ‘0’. Measurement reference points for inputs and outputs are V_{HT} ($0.6V_{DD}$) and V_{LT} ($0.4V_{DD}$). Input rise and fall times (10% ↔ 90%) are <3 ns.

Note: V_{HT} = V_{HIGH} Test
V_{LT} = V_{LOW} Test
V_{HT} = V_{INPUT} HIGH Test
V_{ILT} = V_{INPUT} LOW Test

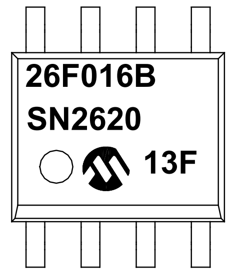
9.0 PACKAGING INFORMATION

9.1 Package Marking

8-Lead SOIC (3.90 mm)



Example



Part Number	1st Line Marking Codes
	SOIC
SST26VF016BEUI	26F016B

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)

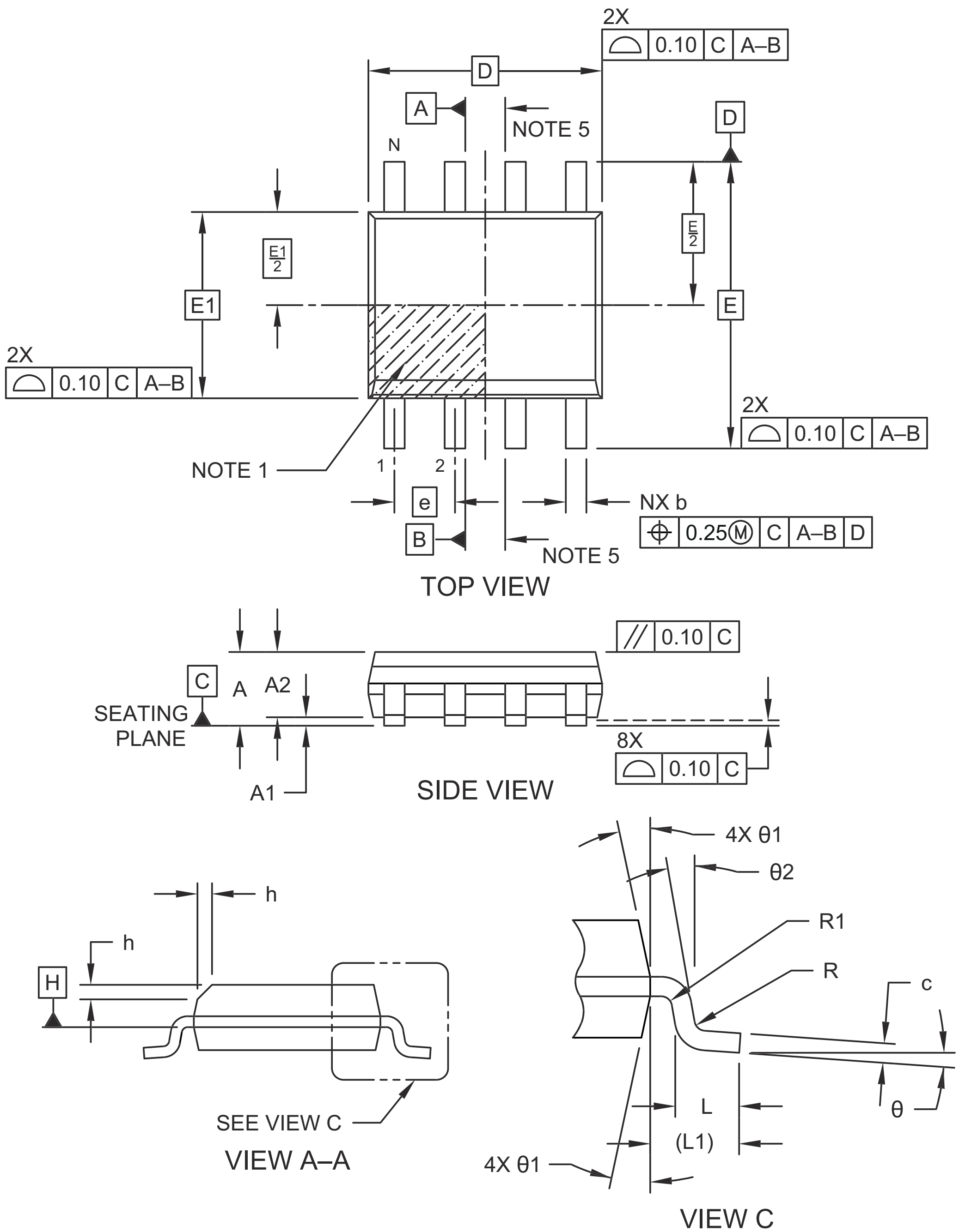
Note: For very small packages with no room for the Pb-free JEDEC® designator e3, the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

9.2 Packaging Diagrams

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

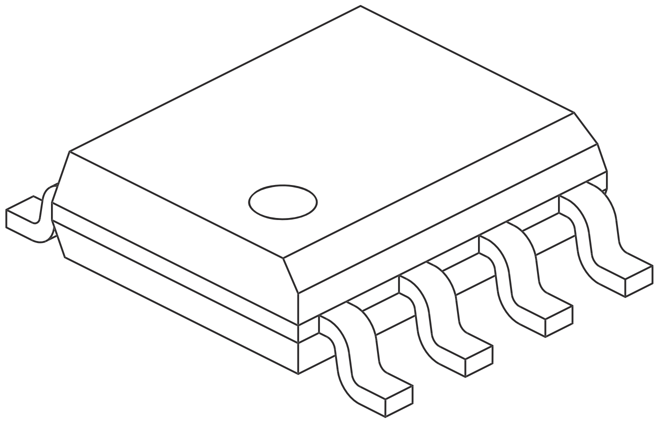
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-00057-SN Rev L Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

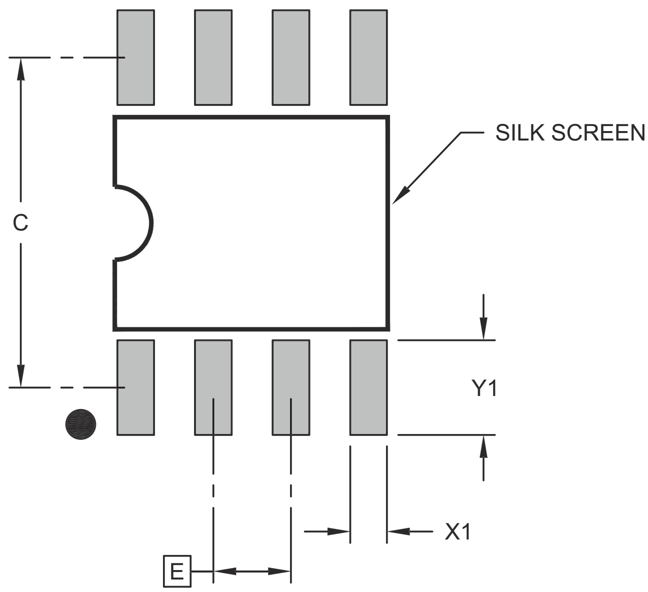
Notes:

1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-00057-SN Rev L Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-02057-SN Rev L

10.0 REVISION HISTORY

Revision C (July 2026)

Replaced incorrect packaging diagram with C04-00057 diagram; Editorial updates throughout the document.

Revision B (June 2024)

Updated section “Pre-Programmed EUI-48 and EUI-64 Address”; Editorial updates throughout the document.

Revision A (January 2019)

Initial release of the document.

11.0 APPENDIX

TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 1 OF 16)

Address	Bit Address	Data	Comments
SFDP Header			
SFDP Header: 1st DWORD			
00H	A7:A0	53H	SFDP Signature SFDP Signature=50444653H
01H	A15:A8	46H	
02H	A23:A16	44H	
03H	A31:A24	50H	
SFDP Header: 2nd DWORD			
04H	A7:A0	06H	**SFDP Minor Revision Number**
05H	A15:A8	01H	**SFDP Major Revision Number**
06H	A23:A16	02H	**Number of Parameter Headers (NPH) = 3**
07H	A31:A24	FFH	**Unused**. Contains FF and cannot be changed.
Parameter Headers			
JEDEC Flash Parameter Header: 1st DWORD			
08H	A7:A0	00H	**Parameter ID Least Significant Bit (LSb) Number** When this field is set to 00H, it indicates a JEDEC-specified header. For vendor-specified headers, this field must be set to the vendor's manufacturer ID.
09H	A15:A8	06H	**Parameter Table Minor Revision Number** Minor revisions are either clarifications or changes that add parameters in existing Reserved locations. Minor revisions do NOT change overall structure of SFDP. Minor Revision starts at 00H.
0AH	A23:A16	01H	**Parameter Table Major Revision Number** Major revisions are changes that reorganize or add parameters to locations that are NOT currently Reserved. Major revisions would require code (BIOS/firmware) or hardware change to get previously defined discoverable parameters. Major Revision starts at 01H.
0BH	A31:A24	10H	**Parameter Table Length** Number of DWORDs that are in the Parameter table.
JEDEC Flash Parameter Header: 2nd DWORD			
0CH	A7:A0	30H	**Parameter Table Pointer (PTP)** A 24-bit address that specifies the start of this header's Parameter table in the SFDP structure. The address must be DWORD-aligned.
0DH	A15:A8	00H	
0EH	A23:A16	00H	
0FH	A31:A24	FFH	**Parameter ID Most Significant Bit (MSb) Number**.
JEDEC Sector Map Parameter Header: 3rd DWORD			
10H	A7:A0	81H	**Parameter ID LSb Number**. Sector Map Function-Specific table is assigned 81H.
11H	A15:A8	00H	**Parameter Table Minor Revision Number** Minor revisions are either clarifications or changes that add parameters in existing Reserved locations. Minor revisions do NOT change overall structure of SFDP. Minor Revision starts at 00H.
12H	A23:A16	01H	**Parameter Table Major Revision Number** Major revisions are changes that reorganize or add parameters to locations that are NOT currently Reserved. Major revisions would require code (BIOS/firmware) or hardware change to get previously defined discoverable parameters. Major Revision starts at 01H.

TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 2 OF 16)

Address	Bit Address	Data	Comments
13H	A31:A24	06H	**Parameter Table Length** Number of DWORDs that are in the Parameter table.
JEDEC Flash Parameter Header: 4th DWORD			
14H	A7:A0	00H	**Parameter Table Pointer (PTP)** This 24-bit address specifies the start of this header's Parameter Table in the SFDP structure. The address must be DWORD-aligned.
15H	A15:A8	01H	
16H	A23:A16	00H	
17H	A31:A24	FFH	**Parameter ID MSb Number**
Microchip (Vendor) Parameter Header: 5th DWORD			
18H	A7:A0	BFH	**ID Number** Manufacture ID (vendor specified header)
19H	A15:A8	00H	**Parameter Table Minor Revision Number**
1AH	A23:A16	02H	**Parameter Table Major Revision Number,** Revision 2.0
1BH	A31:A24	1CH	**Parameter Table Length,** 28 Double Words
Microchip (Vendor) Parameter Header: 6th DWORD			
1CH	A7:A0	00H	**Parameter Table Pointer (PTP)** This 24-bit address specifies the start of this header's Parameter table in the SFDP structure. The address must be DWORD-aligned.
1DH	A15:A8	02H	
1EH	A23:A16	00H	
1FH	A31:A24	01H	**Used to indicate bank number (vendor specific)**
JEDEC Flash Parameter Table			
JEDEC Flash Parameter Table: 1st DWORD			
30H	A1:A0	FDH	**Block/Sector Erase Sizes** 00: Reserved **01: 4-Kbyte Erase** 10: Reserved 11: Use this setting only if the 4-Kbyte erase is unavailable
	A2		**Write Granularity** 0: Single-byte programmable devices or buffer programmable devices with buffer is less than 64 bytes (32 Words). **1: For buffer programmable devices when the buffer size is 64 bytes (32 Words) or larger**
	A3		**Volatile STATUS Register** 0: Target Flash has nonvolatile status bit. Write/Erase commands do not require STATUS register to be written on every power-on. **1: Target Flash has volatile Status bits**
	A4		**Write Enable Opcode Select for Writing to Volatile STATUS Register** 0: 0x50. Enables a status register write when bit 3 is set to 1. **1: 0x06. Enables a STATUS register write when bit 3 is set to 1**.
	A7:A5		**Unused**. Contains 111b and cannot be changed.
31H	A15:A8	20H	**4-Kbyte Erase Opcode**

TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 3 OF 16)

Address	Bit Address	Data	Comments
32H	A16	F1H	**Supports (1-1-2) Fast Read** 0: (1-1-2) Fast Read NOT supported **1: (1-1-2) Fast Read supported**
	A18:A17		**Address Bytes** Number of bytes used in addressing Flash array read, write and erase **00: 3-byte only addressing** 01: 3- or 4-byte addressing (e.g., defaults to 3-byte mode; enters 4-byte mode on command) 10: 4-byte only addressing 11: Reserved
	A19		**Supports Double Transfer Rate (DTR) Clocking** Indicates the device supports some type of double transfer rate clocking. **0: DTR NOT supported** 1: DTR Clocking supported
	A20		**Supports (1-2-2) Fast Read** Device supports single input opcode, dual input address and dual output data Fast Read. 0: (1-2-2) Fast Read NOT supported **1: (1-2-2) Fast Read supported**
	A21		**Supports (1-4-4) Fast Read** Device supports single input opcode, quad input address and quad output data Fast Read. 0: (1-4-4) Fast Read NOT supported **1: (1-4-4) Fast Read supported**
	A22		**Supports (1-1-4) Fast Read** Device supports single input opcode & address and quad output data Fast Read. 0: (1-1-4) Fast Read NOT supported **1: (1-1-4) Fast Read supported**
	A23		**Unused**. Contains ‘1’ can not be changed.
33H	A31:A24	FFH	**Unused**. Contains FF can not be changed.
JEDEC Flash Parameter Table: 2nd DWORD			
34H	A7:A0	FFH	**Flash Memory Density** SST26VF016BEUI = 00FFFFFFH
35H	A15:A8	FFH	
36H	A23:A16	FFH	
37H	A31:A24	00H	
JEDEC Flash Parameter Table: 3rd DWORD			
38H	A4:A0	44H	**(1-4-4) Fast Read Number of Wait states (dummy clocks) needed before valid output** 00100b: 4 dummy clocks (16 dummy bits) are needed with a quad input address phase instruction
	A7:A5		**Quad Input Address Quad Output (1-4-4) Fast Read Number of Mode Bits** 010b: 2 dummy clocks (8 mode bits) are needed with a single input opcode, quad input address and quad output data Fast Read Instruction.
39H	A15:A8	EBH	**(1-4-4) Fast Read Opcode** Opcode for single input opcode, quad input address and quad output data Fast Read.

TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 4 OF 16)

Address	Bit Address	Data	Comments
3AH	A20:A16	08H	**(1-1-4) Fast Read Number of Wait states (dummy clocks) needed before valid output** 01000b: 8 dummy bits are needed with a single input opcode and address and quad output data Fast Read Instruction.
	A23:A21		**(1-1-4) Fast Read Number of Mode Bits** 000b: No mode bits are needed with a single input opcode and address and quad output data Fast Read Instruction.
3BH	A31:A24	6BH	**(1-1-4) Fast Read Opcode** Opcode for single input opcode and address and quad output data Fast Read.
JEDEC Flash Parameter Table: 4th DWORD			
3CH	A4:A0	08H	**(1-1-2) Fast Read Number of Wait states (dummy clocks) needed before valid output** 01000b: 8 dummy clocks are needed with a single input opcode, address and dual output data fast read instruction.
	A7:A5		**(1-1-2) Fast Read Number of Mode Bits** 000b: No mode bits are needed with a single input opcode and address and quad output data Fast Read Instruction.
3DH	A15:A8	3BH	**(1-1-2) Fast Read Opcode** Opcode for single input opcode and address and dual output data Fast Read.
3EH	A20:A16	80H	**(1-2-2) Fast Read Number of Wait states (dummy clocks) needed before valid output** 00010b: 0 clocks of dummy cycle
	A23:A21		**(1-2-2) Fast Read Number of Mode Bits (in clocks)** 010b: 4 clocks of mode bits are needed
3FH	A31:A24	BBH	**(1-2-2) Fast Read Opcode** Opcode for single input opcode, dual input address and dual output data Fast Read.
JEDEC Flash Parameter Table: 5th DWORD			
40H	A0	FEH	**Supports (2-2-2) Fast Read** Device supports dual input opcode and address and dual output data Fast Read **0: (2-2-2) Fast Read NOT supported** 1: (2-2-2) Fast Read supported
	A3:A1		**Reserved**. Bits default to all 1's.
	A4		**Supports (4-4-4) Fast Read** Device supports Quad input opcode and address and quad output data Fast Read. 0: (4-4-4) Fast Read NOT supported **1: (4-4-4) Fast Read supported**
	A7:A5		**Reserved.** Bits default to all 1's.
41H	A15:A8	FFH	**Reserved**. Bits default to all 1's.
42H	A23:A16	FFH	**Reserved**. Bits default to all 1's.
43H	A31:A24	FFH	**Reserved**. Bits default to all 1's.
JEDEC Flash Parameter Table: 6th DWORD			
44H	A7:A0	FFH	**Reserved**. Bits default to all 1's.
45H	A15:A8	FFH	**Reserved**. Bits default to all 1's.

TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 5 OF 16)

Address	Bit Address	Data	Comments
46H	A20:A16	00H	**(2-2-2) Fast Read Number of Wait states (dummy clocks) needed before valid output** 00000b: No dummy bit is needed
	A23:A21		**(2-2-2) Fast Read Number of Mode Bits** 000b: No mode bits are needed.
47H	A31:A24	FFH	**(2-2-2) Fast Read Opcode** Opcode for dual input opcode and address and dual output data Fast Read (not supported).
JEDEC Flash Parameter Table: 7th DWORD			
48H	A7:A0	FFH	**Reserved**. Bits default to all 1's.
49H	A15:A8	FFH	**Reserved**. Bits default to all 1's.
4AH	A20:A16	44H	**(4-4-4) Fast Read Number of Wait states (dummy clocks) needed before valid output** `00100b`: 4 clocks dummy are needed with a quad input opcode and address and quad output data Fast Read Instruction.
	A23:A21		**(4-4-4) Fast Read Number of Mode Bits** `010b`: 2 clocks mode bits are needed with a quad input opcode & address and quad output data Fast Read Instruction.
4BH	A31:A24	0BH	**(4-4-4) Fast Read Opcode** Opcode for quad input opcode/address, quad output data Fast Read.
JEDEC Flash Parameter Table: 8th DWORD			
4CH	A7:A0	0CH	**Sector Type 1 Size** 4-Kbyte, Sector/block size = 2^N bytes
4DH	A15:A8	20H	**Sector Type 1 Opcode** Opcode used to erase the number of bytes specified by Sector Type 1 Size.
4EH	A23:A16	0DH	**Sector Type 2 Size** 8-Kbyte, Sector/block size = 2^N bytes
4FH	A31:A24	D8H	**Sector Type 2 Opcode** Opcode used to erase the number of bytes specified by Sector Type 2 Size.
JEDEC Flash Parameter Table: 9th DWORD			
50H	A7:A0	0FH	**Sector Type 3 Size** 32-Kbyte, Sector/block size = 2^N bytes
51H	A15:A8	D8H	**Sector Type 3 Opcode** Opcode used to erase the number of bytes specified by Sector Type 3 Size.
52H	A23:A16	10H	**Sector Type 4 Size** 64-Kbyte, Sector/block size = 2^N bytes
53H	A31:A24	D8H	**Sector Type 4 Opcode** Opcode used to erase the number of bytes specified by Sector Type 4 Size.

TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 6 OF 16)

Address	Bit Address	Data	Comments
JEDEC Flash Parameter Table: 10th DWORD			
54H	A3:A0	20H	**Multiplier from typical erase time to maximum erase time** Maximum time = 2*(count + 1)*Typical erase time Count = 0 **A3:A0 = 0000b**
	A7:A4		**Erase Type 1 Erase, Typical time** Typical Time = (count +1)*units 1 ms to 32 ms, 16 ms to 512 ms, 128 ms to 4096 ms, 1s to 32s 10:9 units (**000b: 1 ms**, 01b:16 ms, 10b:128 ms, 11b:1s) **A8:A4 count = 12 = 10010b** **A10:A9 unit = 1ms = 00b**
55H	A10:A8	91H	**A10:A8 = 001b**
	A15:A11		**Erase Type 2 Erase, Typical time** Typical time = (count+1)*units 1 ms to 32 ms, 16 ms to 512 ms, 128 ms to 4096 ms, 1s to 32s 17:16 units (**00b:1 ms**, 01b:16 ms, 10b:128 ms, 11b:1s) **A15:A11 count = 18 = 10010b** **A17:A16 unit = 1 ms = 00b**
56H	A17:A16	48H	**A17:A16 = 00b**
	A23:A18		**Erase Type 3 Erase, Typical time** Typical time = (count+1)*units 1 ms to 32 ms, 16 ms to 512 ms, 128 ms to 4096 ms, 1s to 32s 24:23 units (**00b:1 ms**, 01b:16 ms, 10b:128 ms, 11b:1s) **A22:A18 count = 18 = 10010b** **A24:A23 unit = 1 ms = 00b**
57H	A24	24H	**A24 = 0b**
	A31:A25		**Erase Type 4 Erase, Typical time** Typical time = (count+1)*units 1 ms to 32 ms, 16 ms to 512 ms, 128 ms to 4096 ms, 1s to 32s 31:30 units (**00b:1 ms**, 01b:16 ms, 10b:128 ms, 11b:1s) **A29:A25 count = 18 = 10010b** **A31:A30 unit = 1 ms = 00b**
JEDEC Flash Parameter Table: 11th DWORD			
58H	A3:A0	80H	**Multiplier from Typical Program Time to Maximum Program Time** Maximum time = 2*(count +1)*Typical program time **Count = 0** **A3:A0 = 0000b**
	A7:A4		**Page Size** Page size = 2^N bytes **N = 8** **A7:A4 = 000b**

TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 7 OF 16)

Address	Bit Address	Data	Comments
59H	A13:A8	6FH	**Page Program Typical time** Program time = (count+1)*units 13 units (0b: 8 µs, **1b: 64 µs**) **A12:A8 count = 11 = 01111b** **A13 unit = 64 µs = 1b**
	A15:A14		**Byte Program Typical time, first byte** Typical time = (count+1)*units 18 units (0b: 1 µs, **1b:8 µs**) **A17:A14 count = 5 = 0101b** **A18 = 8 µs = 1b**
5AH	A18:A16	1DH	**A18:A16 = 101b**
	A23:A19		**Byte Program Typical time, Additional Byte** Typical time = (count+1)*units 23 units (**0b:1 µs**, 1b:8 µs) **A22:A19 count = 0011b** **A23 = 1 µs = 0b**
5BH	A30:A:24	81H	**Chip Erase Typical Time** Typical time = (count+1)*units 16 ms to 512 ms, 256 ms to 8192 ms, 4s to 128s, 64s to 2048s **A28:A24 count = 1 = 00001b** **A30:A29 units =16 ms = 00b**
	A31		**Reserved** **A31 = 1b**
JEDEC Flash Parameter Table: 12th DWORD			
5CH	A3:A0	EDH	**Prohibited Operations During Program Suspend** xxx0b: May not initiate a new erase anywhere **xxx1b: May not initiate a new erase in the program suspended page size** **xx0xb: May not initiate a new page program anywhere** xx1xb: May not initiate a new page program in program suspended page size x0xxb: Refer to the Data Sheet **x1xxb: May not initiate a read in the program suspended page size** 0xxxb: Additional erase or program restrictions apply **1xxxb: The erase and program restrictions in bits 1:0 are sufficient**
	A7:A4		**Prohibited Operation During Erase Suspend** **xxx0b: May not initiate a new erase anywhere** xxx1b: May not initiate a new erase in the erase suspended page size xx0xb: May not initiate a new page program anywhere **xx1xb: May not initiate a new page program in erase suspended erase type size** x0xxb: Refer to the Data Sheet **x1xxb: May not initiate a read in the erase suspended page size** 0xxxb: Additional erase or program restrictions apply **1xxxb: The erase and program restrictions in bits 5:4 are sufficient**

TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 8 OF 16)

Address	Bit Address	Data	Comments
5DH	A8	0FH	**Reserved = 1b**
	A12:A9		**Program Resume to Suspend Interval** The device requires this typical amount of time to make progress on the program operation before allowing another suspend Interval = 500 µs Program resume to suspend interval = (count+1)*64µs A12:A9 = 7 = **0111b**
	A15:A13		**Suspend In-Progress Program Maximum Latency** Maximum time required by the Flash device to suspend an in-progress program and be ready to accept another command which accesses the Flash array. Max latency = 25 µs Program maximum latency = (count+1)*units Units (00b:128 ns, **01b:1 µs**, 10b:8 µs, 11b:64 µs) **A17:A13 = count = 24 = 11000b** **A19:A18 = 1 µs = 01b**
5EH	A19:A16	77H	**0111b**
	A23:A20		**Erase Resume to Suspend Interval** The device requires this typical amount of time to make progress on the erase operation before allowing another suspend. Interval = 500 µs Erase resume to suspend interval = (count+1)*64 µs A23:A20 = 7 = **0111b**
5FH	A30:A24	38H	**Suspend In-Progress Erase Maximum Latency** Maximum time required by the Flash device to suspend an in-progress erase and be ready to accept another command which accesses the Flash array. Maximum latency = 25 µs Erase maximum latency = (count+1)*units nits (00b:128 ns, **01b:1 µs**, 10b:8 µs, 11b:64 µs) **A28:A24 = count = 24 = 11000b** **A30:A29 = 1µs = 01b**
	A31		**Suspend/Resume supported** **0: Supported** 1: Not supported
JEDEC Flash Parameter Table: 13th DWORD			
60H	A7:A0	30H	**Program Resume Instruction**
61H	A15:A8	B0H	**Program Suspend Instruction**
62H	A23:A16	30H	**Resume Instruction**
63H	A31:A24	B0H	**Suspend Instruction**
JEDEC Flash Parameter Table: 14th DWORD			
64H	A1:A0	F7H	**Reserved** = 11b
	A7:A2		**Status Register Polling Device Busy** 111101b: Use of legacy polling is supported by reading the STATUS register with 05h instruction and checking WIP bit [0] (0 = ready, 1 = busy)

TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 9 OF 16)

Address	Bit Address	Data	Comments
65H	A14:A8	A9H	**Exit Deep Power-down to next operation delay: 10 µs** Delay = (count+1)*unit A12:A8 = count = 9 = 01001b A14:A13 units = 01b = 1 µs
	A15		**Exit Power-down Instruction: ABH = 10101011b** A15 = 1b
66H	A22:A16	D5H	**A22:A16 = 1010101b**
	A23		**Enter Power-down instruction: B9H = 010111001b** A23 = 1b
67H	A30:A24	5CH	**A30:A24 = 1011100**
	A31		**Deep Power-down Supported** 0: Supported **1: Not supported**
JEDEC Flash Parameter Table: 15th DWORD			
68H	A3:A0	29H	**4-4-4 Mode Disable Sequences** Xxx1b: issue FF instruction 1xxxb: issue the Soft Reset 66/99 sequence
	A7:A4		**4-4-4 Mode Enable Sequences** X_xx1xb: issue instruction 38h
69H	A8	C2H	**4-4-4 Mode Enable Sequences** A8 = 0
	A9		**0-4-4 Mode Supported** 0: Not supported **1: Supported**
	A15:A10		**0-4-4 Mode Exit Method** X1_xxxx: Mode Bit[7:0] Not= AXh 1x_xxxx: Reserved = 1
6AH	A19:A16	5CH	**0-4-4 Mode Entry Method** **X1xxb: M[7:0] = AXh** 1xxxb:Reserved = 1
	A22:A20		**Quad Enable Requirements (QER)** **101b: Quad Enable is bit 1 of the Configuration register**
	A23		**HOLD and Reset Disable** **0: Feature is not supported**
6BH	A31:A24	FFH	**Reserved bits** = 0xFF
JEDEC Flash Parameter Table: 16th DWORD			
6C	A6:A0	F0H	**Volatile or Nonvolatile Register and Write Enable Instructions for Status Register 1** Xx1_xxxxb: STATUS Register 1 contains a mix of volatile and nonvolatile bits. The 06h instruction is used to enable writing to the register. X1x_xxxxb: Reserved = 1 1xx_xxxxb: Reserved = 1
	A7		**Reserved** = 1b
6D	A13:A8	30H	**Soft Reset and Rescue Sequence Support** X1_xxxxb: reset enable instruction 66h is issued followed by Reset instruction 99h 1x_xxxxb: exit 0-4-4 mode is required prior to other Reset sequences
	A15:A14		**Exit 4-Byte Addressing** Not supported

TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 10 OF 16)

Address	Bit Address	Data	Comments
6E	A23:A16	C0H	**Exit 4-Byte Addressing** Not supported A21:A14 = 000000b A23 and A22 are Reserved bits which are = 1
6F	A31:A24	80H	**Enter 4-Byte Addressing** Not supported 1xxx_xxxx: Reserved = 1
JEDEC Sector Map Parameter Table			
100H	A7:A0	FFH	**Sector Map** A7:A2 = Reserved = 111111b A1 = Descriptor Type = Map = 1b A0 = Last map = 1b
101H	A15:A8	00H	**Configuration ID** = 00h
102H	A23:A16	04H	**Region Count** = 5 Regions
103H	A31:A24	FFH	**Reserved** = FFH
104H	A7:A0	F3H	**Region 0 supports 4-Kbyte erase and 8-Kbyte erase** A3:A0 = 0011b A7:A4 = Reserved = 1111b
105H	A15:A8	7FH	**Region 0 Size** 4 * 8 Kbytes = 32 Kbytes Count = 32 Kbytes/256 bytes = 128 Value = count -1 = 127 A31:A8 = 00007Fh
106H	A23:A16	00H	
107H	A31:A24	00H	
108H	A7:A0	F5H	**Region 1 supports 4-Kbyte erase and 32-Kbyte erase** A3:A0 = 0101b A7:A4 = Reserved = 1111b
109H	A15:A8	7FH	**Region 1 size** 1 * 32 Kbytes = 32 Kbytes Count = 32 Kbytes/256 bytes = 128 Value = count -1 = 127 A31:A8 = 00007Fh
10AH	A23:A16	00H	
10BH	A31:A24	00H	
10CH	A7:A0	F9H	**Region 2 supports 4-Kbyte erase and 64-Kbyte erase** A3:A0 = 1001b A7:A4 = Reserved = 1111b
10DH	A15:A8	FFH	**Region 2 size** 30 * 64 Kbytes = 1920 Kbytes Count = 1920 Kbytes/256 bytes = 7680 Value = count -1 = 7679 A31:A8 = 001DFFh
10EH	A23:A16	1DH	
10FH	A31:A24	00H	
110H	A7:A0	F5H	**Region 3 supports 4-Kbyte erase and 32-Kbyte erase** A3:A0 = 0101b A7:A4 = Reserved = 1111b

TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 11 OF 16)

<table>
<tr><th>Address</th><th>Bit Address</th><th>Data</th><th>Comments</th></tr>
<tr><td>111H</td><td>A15:A8</td><td>7FH</td><td>Region 3 size
1 * 32 Kbytes = 32 Kbytes
Count = 32 Kbytes/256 bytes = 128
Value = count -1 = 127
A31:A8 = 00007Fh</td></tr>
<tr><td>112H</td><td>A23:A16</td><td>00H</td><td></td></tr>
<tr><td>113H</td><td>A31:A24</td><td>00H</td><td></td></tr>
<tr><td>114H</td><td>A7:A0</td><td>F3H</td><td>Region 4 supports 4-Kbyte erase and 8-Kbyte erase
A3:A0 = 0011b
A7:A4 = Reserved = 1111b</td></tr>
<tr><td>115H</td><td>A15:A8</td><td>7FH</td><td>Region 4 Size
4 * 8 Kbytes = 32 Kbytes
Count = 32 Kbytes/256 bytes = 128
Value = count -1 = 127
A31:A8 = 00007Fh</td></tr>
<tr><td>116H</td><td>A23:A16</td><td>00H</td><td></td></tr>
<tr><td>117H</td><td>A31:A24</td><td>00H</td><td></td></tr>
<tr><td colspan="4">SST26VF016BEUI (Vendor) Parameter Table</td></tr>
<tr><td colspan="4">SST26VF016BEUI Identification</td></tr>
<tr><td>200H</td><td>A7:A0</td><td>BFH</td><td>Manufacturer ID</td></tr>
<tr><td>201H</td><td>A15:A8</td><td>26H</td><td>Memory Type</td></tr>
<tr><td>202H</td><td>A23:A16</td><td>41H</td><td>Device ID
SST26VF016BEUI = 41H</td></tr>
<tr><td>203H</td><td>A31:A24</td><td>FFH</td><td>Reserved. Bits default to all 1’s.</td></tr>
<tr><td colspan="4">SST26VF016BEUI Interface</td></tr>
<tr><td rowspan="4">204H</td><td>A2:A0</td><td rowspan="4">B9H</td><td>Interfaces Supported
000: SPI only
001: Power-up default is SPI; Quad can be enabled/disabled
010: Reserved
: :
111: Reserved</td></tr>
<tr><td>A3</td><td>Supports Enable Quad
0: Not supported
1: Supported</td></tr>
<tr><td>A6:A4</td><td>Supports Hold#/Reset# Function
000: Hold#
001: Reset#
010: HOLD/Reset#
011: Hold# & I/O when in SQI (4-4-4), 1-4-4 or 1-1-4 Read</td></tr>
<tr><td>A7</td><td>Supports Software Reset
0: Not supported
1: Supported</td></tr>
</table>

TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 12 OF 16)

Address	Bit Address	Data	Comments
205H	A8	DFH	**Supports Quad Reset** 0: Not supported **1: Supported**
	A10:A9		**Reserved**. Bits default to all 1's.
	A13:A11		**Byte Program or Page Program (256 bytes)** 011: Byte Program/Page Program in SPI and Quad Page Program once Quad is enabled.
	A14		**Program-Erase Suspend Supported** 0: Not Supported **1: Program/Erase Suspend Supported**
	A15		**Deep Power-Down Mode Supported** **0: Not Supported** 1: Deep Power-Down Mode Supported
206H	A16	FDH	**OTP Capable (Security ID) Supported** 0: Not supported **1: Supported**
	A17		**Supports Block Group Protect** **0: Not supported** 1: Supported
	A18		**Supports Independent Block-Protect** 0: Not supported **1: Supported**
	A19		**Supports Independent Nonvolatile Lock (Block or Sector becomes OTP)** 0: Not supported **1: Supported**
	A23:A20		**Reserved.** Bits default to all 1's.
207H	A31:A24	FFH	**Reserved.** Bits default to all 1's.
208H	A7:A0	30H	**VDD Minimum Supply Voltage** 2.3V (F230H)
209H	A15:A8	F2H	
20AH	A23:A16	60H	**VDD Maximum Supply Voltage** 3.6V (F360H)
20BH	A31:A24	F3H	
20CH	A7:A0	32H	**Typical time-out for Byte Program:** 50 µs Typical time-out for Byte Program is in µs. Represented by conversion of the actual time from the decimal to hexadecimal number.
20DH	A15:A8	FFH	Reserved. Bits default to all 1's.
20EH	A23:A16	0AH	**Typical time-out for page program**: 1.0 ms (xxH*(0.1 ms)
20FH	A31:A24	12H	**Typical time-out for Sector-Erase/Block Erase:** 18 ms Typical time-out for Sector/Block Erase is in ms. Represented by conversion of the actual time from the decimal to hexadecimal number.
210H	A7:A0	23H	**Typical time-out for Chip Erase:** 35 ms Typical time-out for Chip-Erase is in ms. Represented by conversion of the actual time from the decimal to hexadecimal number.
211H	A15:A8	46H	**Maximum time-out for Byte Program:** 70 µs Typical time-out for Byte Program is in µs. Represented by conversion of the actual time from the decimal to hexadecimal number.
212H	A23:A16	FFH	Reserved. Bits default to all 1's.
213H	A31:A24	0FH	**Maximum time-out for Page Program:** 1.5 ms Typical time-out for Page Program in xxH * (0.1 ms) ms

TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 13 OF 16)

Address	Bit Address	Data	Comments
214H	A7:A0	19H	**Maximum time-out for Sector Erase/Block Erase:** 25 ms Maximum time-out for Sector/Block Erase in ms
215H	A15:A8	32H	**Maximum time-out for Chip Erase**: 50 ms Maximum time-out for Chip Erase in ms
216H	A23:A16	0FH	**Maximum time-out for Program Security ID:** 1.5 ms Maximum time-out for Program Security ID in xxH*(0.1 ms) ms
217H	A31:A24	19H	**Maximum time-out for Write Protection Enable Latency:** 25 ms Maximum time-out for Write-Protection Enable Latency is in ms. Represented by conversion of the actual time from the decimal to hexadecimal number.
218H	A23:A16	19H	**Maximum time Write Suspend Latency:** 25 µs Maximum time-out for Write Suspend Latency is in µs. Represented by conversion of the actual time from the decimal to hexadecimal number.
219H	A31:A24	03H	**Maximum time to Deep Power-Down:** 3 µs = 03H
21AH	A23:A16	0AH	**Maximum time-out from Deep Power-Down mode to Standby mode** 10 µs = 0AH
21BH	A31:A24	FFH	**Reserved.** Bits default to all 1's.
21CH	A23:A16	FFH	**Reserved.** Bits default to all 1's.
21DH	A31:A24	FFH	**Reserved.** Bits default to all 1's.
21EH	A23:A16	FFH	**Reserved.** Bits default to all 1's.
21FH	A31:A24	FFH	**Reserved.** Bits default to all 1's.
Supported Instructions			
220H	A7:A0	00H	**No Operation**
221H	A15:A8	66H	**Reset Enable**
222H	A23:A16	99H	**Reset Memory**
223H	A31:A24	38H	**Enable Quad I/O**
224H	A7:A0	FFH	**Reset Quad I/O**
225H	A15:A8	05H	**Read STATUS Register**
226H	A23:A16	01H	**Write STATUS Register**
227H	A31:A24	35H	**Read Configuration Register**
228H	A7:A0	06H	**Write Enable**
229H	A15:A8	04H	**Write Disable**
22AH	A23:A16	02H	**Byte Program or Page Program**
22BH	A31:A24	32H	**SPI Quad Page Program**
22CH	A7:A0	B0H	**Suspends Program/Erase**
22DH	A15:A8	30H	**Resumes Program/Erase**
22EH	A23:A16	72H	**Read Block Protection register**
22FH	A31:A24	42H	**Write Block Protection Register**
230H	A7:A0	8DH	**Lock-Down Block Protection Register**
231H	A15:A8	E8H	**Nonvolatile Write Lock-Down Register**
232H	A23:A16	98H	**Global Block Protection Unlock**
233H	A31:A24	88H	**Read Security ID**
234H	A7:A0	A5H	**Program User Security ID Area**
235H	A15:A8	85H	**Lockout Security ID Programming**
236H	A23:A16	C0H	**Set Burst Length**
237H	A31:A24	9FH	**JEDEC ID**
238H	A7:A0	AFH	**Quad J-ID**

TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 14 OF 16)

<table>
<tr><th>Address</th><th>Bit Address</th><th>Data</th><th>Comments</th></tr>
<tr><td>239H</td><td>A15:A8</td><td>5AH</td><td>SFDP</td></tr>
<tr><td>23AH</td><td>A23:A16</td><td>B9H</td><td>Deep Power-Down Mode</td></tr>
<tr><td>23BH</td><td>A31:A24</td><td>ABH</td><td>Release Deep Power-Down Mode</td></tr>
<tr><td rowspan="2">23CH</td><td>A4:A0</td><td rowspan="2">06H</td><td>(1-4-4) SPI nB Burst with Wrap Number of Wait states (dummy clocks) needed before valid output
00110b: 6 clocks of dummy cycle</td></tr>
<tr><td>A7:A5</td><td>(1-4-4) SPI nB Burst with Wrap Number of Mode Bits
000b: Set Mode bits are not supported</td></tr>
<tr><td>23DH</td><td>A15:A8</td><td>ECH</td><td>(1-4-4) SPI nB Burst with Wrap Opcode</td></tr>
<tr><td rowspan="2">23EH</td><td>A20:A16</td><td rowspan="2">06H</td><td>(4-4-4) SQI nB Burst with Wrap Number of Wait states (dummy clocks) needed before valid output.
00110b: 6 clocks of dummy cycle</td></tr>
<tr><td>A23:A21</td><td>(4-4-4) SQI nB Burst with Wrap Number of Mode Bits
000b: Set Mode bits are not supported</td></tr>
<tr><td>23FH</td><td>A31:A24</td><td>0CH</td><td>(4-4-4) SQI nB Burst with Wrap Opcode</td></tr>
<tr><td rowspan="2">240H</td><td>A4:A0</td><td rowspan="2">00H</td><td>(1-1-1) Read Memory Number of Wait states (dummy clocks) needed before valid output
00000b: Wait states/dummy clocks are not supported</td></tr>
<tr><td>A7:A5</td><td>(1-1-1) Read Memory Number of Mode Bits
000b: Mode bits are not supported</td></tr>
<tr><td>241H</td><td>A15:A8</td><td>03H</td><td>(1-1-1) Read Memory Opcode</td></tr>
<tr><td rowspan="2">242H</td><td>A20:A16</td><td rowspan="2">08H</td><td>(1-1-1) Read Memory at Higher Speed Number of Wait states (dummy clocks) needed before valid output.
01000: 8 clocks (8 bits) of dummy cycle</td></tr>
<tr><td>A23:A21</td><td>(1-1-1) Read Memory at Higher Speed Number of Mode Bits
000b: Mode bits are not supported</td></tr>
<tr><td>243H</td><td>A31:A24</td><td>0BH</td><td>(1-1-1) Read Memory at Higher Speed Opcode</td></tr>
<tr><td>244H</td><td>A7:A0</td><td>FFH</td><td>Reserved. Bits default to all 1’s.</td></tr>
<tr><td>245H</td><td>A15:A8</td><td>FFH</td><td>Reserved. Bits default to all 1’s.</td></tr>
<tr><td>246H</td><td>A23:A16</td><td>FFH</td><td>Reserved. Bits default to all 1’s.</td></tr>
<tr><td>247H</td><td>A31:A24</td><td>FFH</td><td>Reserved. Bits default to all 1’s.</td></tr>
<tr><td colspan="4">Security ID</td></tr>
<tr><td>248H</td><td>A7:A0</td><td>FFH</td><td rowspan="2">Security ID size in bytes
Example: If the size is 2 Kbytes, this field will be 07FFH
<table><tr><th colspan="2">Security ID Range</th></tr><tr><td>Unique ID
(pre-programmed at factory)</td><td>0000H-0007H</td></tr><tr><td>User-programmable</td><td>0008H-07FFH</td></tr></table></td></tr>
<tr><td>249H</td><td>A15:A8</td><td>07H</td></tr>
<tr><td>24AH</td><td>A23:A16</td><td>FFH</td><td>Reserved. Bits default to all 1’s.</td></tr>
<tr><td>24BH</td><td>A31:A24</td><td>FFH</td><td>Reserved. Bits default to all 1’s.</td></tr>
<tr><td colspan="4">Memory Organization/Block Protection Bit Mapping</td></tr>
<tr><td>24CH</td><td>A7:A0</td><td>02H</td><td>Section 1: Sector Type Number:
Sector type in JEDEC Parameter Table (bottom, 8-Kbyte)</td></tr>
<tr><td>24DH</td><td>A15:A8</td><td>02H</td><td>Section 1 Number of Sectors
Four of 8 KB block (2^n)</td></tr>
</table>

TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 15 OF 16)

Address	Bit Address	Data	Comments
24EH	A23:A16	FFH	**Section 1 Block Protection Bit Start** $((2^m) +1)+ c$, c = FFH or -1, m = 5 for 16 Mb Odd address bits are Read Lock bit locations and even address bits are Write Lock bit locations. The Most Significant (leftmost) bit indicates the sign of the integer; sometimes called the sign bit. If the sign bit is zero, then the number is greater than or equal to zero or positive. If the sign bit is one then the number is less than zero or negative.
24FH	A31:A24	06H	**Section 1 (bottom) Block Protection Bit End** $((2^m) +1) + c$, c = 06H or 6, m = 5 for 16 Mb Odd address bits are Read Lock bit locations and even address bits are Write Lock bit locations. The Most Significant (leftmost) bit indicates the sign of the integer; sometimes called the sign bit. If the sign bit is zero, then the number is greater than or equal to zero or positive. If the sign bit is one, then the number is less than zero or negative.
250H	A7:A0	03H	**Section 2: Sector Type Number** Sector type in JEDEC Parameter Table (32 KB Block)
251H	A15:A8	00H	**Section 2 Number of Sectors** One of 32 KB Block (2^n, n = 0)
252H	A23:A16	FDH	**Section 2 Block Protection Bit Start** $((2^m) +1) + c$, c = FDH or -3, m = 5 for 16 Mb The Most Significant (leftmost) bit indicates the sign of the integer; sometimes called the sign bit. If the sign bit is zero, then the number is greater than or equal to zero or positive. If the sign bit is one, then the number is less than zero or negative.
253H	A31:A24	FDH	**Section 2 Block Protection Bit End** $((2^m) +1)+ c$, c = FDH or -3, m = 5 for 16 Mb The Most Significant (left-most) bit indicates the sign of the integer; sometimes called the sign bit. If the sign bit is zero, then the number is greater than or equal to zero or positive. If the sign bit is one, then the number is less than zero or negative.
254H	A7:A0	04H	**Section 3: Sector Type Number** Sector type in JEDEC Parameter Table (64 KB Block)
255H	A15:A8	05H	**Section 3 Number of Sectors** 126 of 64 KB Block (2^n-2, n = 5 for 16 Mb)
256H	A23:A16	00H	**Section 3 Block Protection Bit Start** Section 3 Block Protection Bit starts at 00H
257H	A31:A24	FCH	**Section 3 Block Protection Bit End** $((2^m) +1) + c$, c = FCH or -4, m = 5 for 16 Mb
258H	A7:A0	03H	**Section 4: Sector Type Number** Sector type in JEDEC Parameter Table (32 KB Block)
259H	A15:A8	00H	**Section 4 Number of Sectors** One of 32 KB Block (2^n, n = 0)
25AH	A23:A16	FEH	**Section 4 Block Protection Bit Start** $((2^m) +1) + c$, c = FEH or -2, m = 5 for 16 Mb The Most Significant (leftmost) bit indicates the sign of the integer; sometimes called the sign bit. If the sign bit is zero, then the number is greater than or equal to zero or positive. If the sign bit is one, then the number is less than zero or negative.

TABLE 11-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (SHEET 16 OF 16)

Address	Bit Address	Data	Comments
25BH	A31:A24	FEH	**Section 4 Block Protection Bit End** $((2^m) +1) + c$, c = FEH or -2, m = 5 for 16 Mb The Most Significant (leftmost) bit indicates the sign of the integer; it is sometimes called the sign bit. If the sign bit is zero, then the number is greater than or equal to zero, or positive. If the sign bit is one then the number is less than zero or negative.
25CH	A7:A0	02H	**Section 5 Sector Type Number** Sector type in JEDEC Parameter Table (top, 8-Kbyte)
25DH	A15:A8	02H	**Section 5 Number of Sectors** Four of 8 KB block (2^n)
25EH	A23:A16	07H	**Section 5 Block Protection Bit Start** $((2^m) +1) + c$, c = 07H or 7, m = 5 for 16 Mb Odd address bits are Read Lock bit locations and even address bits are Write Lock bit locations. The Most Significant (leftmost) bit indicates the sign of the integer; sometimes called the sign bit. If the sign bit is zero, then the number is greater than or equal to zero or positive. If the sign bit is one, then the number is less than zero or negative.
25FH	A31:A24	0EH	**Section 5 (bottom) Block Protection Bit End** $(((2^m) +1) + c$, c =0EH or 14, m = 5 for 16 Mb Odd address bits are Read Lock bit locations and even address bits are Write Lock bit locations. The Most Significant (leftmost) bit indicates the sign of the integer; sometimes called the sign bit. If the sign bit is zero, then the number is greater than or equal to zero or positive. If the sign bit is one, then the number is less than zero or negative.
EUI-48 and EUI-64 Information			
260H	A7:A0	30H	Indicates if EUI48 Mac address is being programmed in the next 6 address locations. 30H= 48 bits is programmed FFH = Not being programmed
261H	A15:A8	Octet 5	Mac address LSB-Octet 5
262H	A23:A16	Octet 4	Octet 4
263H	A31:A24	Octet 3	Octet 3
264H	A7:A0	Octet 2	Octet 2
265H	A15:A8	Octet 1	Octet 1
266H	A23:A16	Octet 0	Mac address MSB-Octet 0
267H	A31:A24	40H	Indicates if EUI64 Mac address is being programmed in the next 8 address locations. 40H = 64 bits is programmed FFH = Not being programmed
268H	A7:A0	Octet 7	Mac address LSB-Octet 7
269H	A15:A8	Octet 6	Octet 6
26AH	A23:A16	Octet 5	Octet 5
26BH	A31:A24	Octet 4	Octet 4
26CH	A7:A0	Octet 3	Octet 3
26DH	A15:A8	Octet 2	Octet 2
26EH	A23:A16	Octet 1	Octet 1
26FH	A31:A24	Octet 0	Mac address MSB-Octet 0

See **Section 11.1 “Mapping Guidance Details”** for more detailed mapping information.

11.1 Mapping Guidance Details

The SFDP Memory Organization/Block Protection Bit Mapping defines the memory organization, including uniform sector/block sizes and different contiguous sectors/blocks sizes.

In addition, this bit defines the number of these uniform and different sectors/blocks from address 000000H to the full range of Memory and the associated Block Locking Register bits of each sector/block.

Each major Section is defined as follows:

TABLE 11-2: SECTION DEFINITION

Major Section X	Section X: Sector Type Number
	Section X: Number of Sectors
	Section X: Block Protection Register Bit Start Location
	Section X: Block Protection Register Bit End Location

A Major Section consists of Sector Type Number, Number of Sectors of this type and the Block Protection Bit Start/End locations. This is tied directly to the JEDEC Flash Parameter Table Sector Size Type (in 7th DWORD and 8th DWORD sections). Note that the contiguous 4-Kbyte Sectors across the full memory range are not included on this section because they are not defined in the JEDEC Flash Parameter Table Sector Size Type section. Only the sectors/blocks that are dependent on the Block Protection Register bits are defined. A major section is a partition of contiguous same-size sectors/blocks. There will be several Major Sections as you dissect across memory from 000000h to the full range. Similar sector/block size that reappears may be defined as a different Major Section.

11.1.1 SECTOR TYPE NUMBER

Sector Type Number refers to the sector/block size type defined in JEDEC Flash Parameter Table: SFDP address locations 4CH, 4EH, 50H and 52H. Sector Type 1, represented by 01H, is located at address 4CH. Sector Type 2, represented by 02H, is located at address location 4EH. Sector Type 3, represented by 03H, is located at address location 50H. Sector Type 4, represented by 04H, is located at address location 52H. Contiguous Same Sector Type # Size can re-emerge across the memory range and this Sector Type # will indicate that it is a separate/independent Major Section from the previous contiguous sectors/blocks.

11.1.2 NUMBER OF SECTORS

Number of Sectors represents the number of contiguous sectors/blocks with similar size. A formula calculates the contiguous sectors/blocks with similar size. Given the sector/block size, type and number of sectors, the address range of these sectors/blocks can be determined, along with specific Block Locking Register bits that control the read/write protection of each sector/block.

11.1.3 BLOCK PROTECTION REGISTER BIT START LOCATION (BPSL)

The Block Protection Register Bit Start Location (BPSL) designates the start bit location in the Block Protection Register where the first sector/block of this Major Section begins. If the value of BPSL is 00H, this location corresponds to the 0 bit location. If the value is other than 0, then this value is a constant value adder (c) for a given formula, $\mathbf{(2^m + 1) + (c)}$ (see **Section 11.1.5 “Memory Configuration”**.

From the initial location, there will be a bit location for every increment by one until it reaches the Block Protection Register Bit End Location (BPEL). This number range from BPSL to BPEL will correspond to, and be equal to, the number of sectors/blocks on this Major Section.

11.1.4 BLOCK PROTECTION REGISTER BIT END LOCATION (BPEL)

The Block Protection Register Bit End Location designates the end bit location in the Block Protection Register bit where the last sector/block of this Major Section ends. The value in this field is a constant value adder (c) for a given formula or equation, $\mathbf{(2^m + 1) + (c)}$. (see **Section 11.1.5 “Memory Configuration”**.

11.1.5 MEMORY CONFIGURATION

For the SST26VF016BEUI family, the memory configuration is setup with different contiguous block sizes from bottom to the top of the memory. For example, starting from bottom of memory it has four 8-Kbyte blocks, one 32-Kbyte block, x number of 64-Kbyte blocks depending on memory size, then one 32-Kbyte block and four 8-Kbyte blocks on the top of the memory (see Table 11-3).

TABLE 11-3: MEMORY BLOCK DIAGRAM REPRESENTATION

8-Kbyte Bottom Block (from 000000H)	Section 1: Sector Type Number
	Section 1: Number of Sectors
	Section 1: Block Protection Register Bit Start Location
	Section 1: Block Protection Register Bit End Location
32-Kbyte	Section 2: Sector Type Number
	Section 2: Number of Sectors
	Section 2: Block Protection Register Bit Start Location
	Section 2: Block Protection Register Bit End Location
64-Kbyte	Section 3: Sector Type Number
	Section 3: Number of Sectors
	Section 3: Block Protection Register Bit Start Location
	Section 3: Block Protection Register Bit End Location
32-Kbyte	Section 4: Sector Type Number
	Section 4: Number of Sectors
	Section 4: Block Protection Register Bit Start Location
	Section 4: Block Protection Register Bit End Location
8-Kbyte (Top Block)	Section 5: Sector Type Number
	Section 5: Number of Sectors
	Section 5: Block Protection Register Bit Start Location
	Section 5: Block Protection Register Bit End Location

Classifying these sector/block sizes via the Sector Type derived from the JEDEC Flash Parameter Table: SFDP address locations 4EH, 50H and 52His as follows:

- 8-Kbyte Blocks are classified as Sector Type 2 (@4EH of SFDP)
- 32-Kbyte Blocks are classified as Sector Type 3 (@50H of SFDP)
- 64-Kbyte Blocks are classified as Sector Type 4 (@52H of SFDP)

For the Number of Sectors associated with the contiguous sectors/blocks, a formula is used to determine the number of sectors/blocks of these Sector Types:

- 8-Kbyte Block (Type 2) is calculated by 2^n, where n is a byte.
- 32-Kbyte Block (Type 3) is calculated by 2^n, where n is a byte.
- 64-Kbyte Block (Type 4) is calculated by (2m - 2), where m can either be a 4, 5, 6, 7 or 8, depending on the memory size. This m field is going to be used for the 64-Kbyte Block Section and will also be used for the Block Protection Register Bit Location formula.

m will have a constant value for specific densities and is defined as:

- 8-Mbit = 4
- 16-Mbit = 5
- 32-Mbit = 6
- 64-Mbit = 7
- 128-Mbit = 8

Block Protect Register Start/End Bits are mapped in the SFDP by using the formula **$(2^m + 1) + (c)$**. Here, “m” is a constant value that represents the different densities from 8 Mbits to 128 Mbits (used also in the formula calculating number of 64-Kbyte Blocks mentioned previously). The values to be placed in the Block Protection Bit Start/End field table are the constant value adder (c) in the formula and are represented in two’s compliment, except when the value is 00H. If the value is 00H, this location is the 0 bit location. If the value is other than 0, then this is a constant value adder (c) that will be used in the formula. The Most Significant (left ost) bit indicates the sign of the integer; sometimes referred to as the sign bit. If the sign bit is zero, the number is greater than or equal to zero, or positive. If the sign bit is one, then the number is less than zero, or negative.

See Table 11-4 for an example of this formula.

TABLE 11-4: BPSL/BPEL EQUATION WITH ACTUAL CONSTANT ADDER DERIVED FROM THE FORMULA (2^M + 1) + (C)

Block Size	8-Mbit to 128-Mbit	Comments
8-Kbyte (Type 2) Bottom	BPSL = (2^m + 1) + 0FFH BPEL = (2^m + 1) + 04H	0FFH = -1; 06H = 6 Odd address bits are Read Lock bit locations and even address bits are Write Lock bit locations.
32-Kbyte (Type3)	BPSL = BPEL= (2^m + 1) + 0FDH	0FDH = -3
64-Kbyte (Type 4)	BPSL = 00H BPEL = (2^m + 1) + 0FCH	00H is Block Protection Register bit 0 location; 0FCH = -4
32-Kbyte (Type 3)	BPSL = BPEL= (2^m + 1) + 0FEH	0FEH =-2
8-Kbyte (Type 2) Top	BPSL = (2^m + 1) + 07H BPEL = (2^m + 1) + 0EH	07H = 7; 0EH = 14 Odd address bits are Read Lock bit locations and even address bits are Write Lock bit locations.

11.2 Pre-Programmed EUI-48 and EUI-64 Address

The SST26VF016BEUI is programmed at the factory with a globally unique address stored in the SFDP vendor parameter table and it is permanently write-protected.

11.2.1 EUI-48 ADDRESS

The 6-byte EUI-48 address value of the SST26VF016BEUI is stored in the SFDP table at address locations 0x261 through 0x266, as shown in Table 11-5. The first three bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE® Registration Authority. The remaining three bytes are the Extension Identifier and are generated by Microchip to ensure a globally unique, 48-bit value.

11.2.2 ORGANIZATIONALLY UNIQUE IDENTIFIERS (OUI's)

Each OUI provides roughly 16M (2^{24}) addresses. Once the address pool for an OUI is exhausted, Microchip will acquire a new OUI from the IEEE to use for programming this model. For more information on past and current OUI's, see the Technical Brief, *"Organizationally Unique Identifiers for Preprogrammed EUI-48 and EUI-64 Address Devices"* (DS90003187).

Note: The OUI will change as addresses are exhausted. Customers are not guaranteed to receive a specific OUI and should design their application to accept new OUI's as they are introduced.

11.2.3 EUI-64 SUPPORT USING THE EUI-48

The pre-programmed EUI-48 address of the SST26VF016BEUI can easily be encapsulated at the application level to form a globally unique, 64-bit address for systems utilizing the EUI-64 standard. This is done when the application software inserts 0xFFFE between the OUI and the Extension Identifier, as shown in Table 11-5.

Note: As an alternative, the SST26VF016BEUI features an EUI-64 address that can be used in EUI-64 applications directly without the need for encapsulation, thereby simplifying system software. See **Section 11.2.4 "EUI-64 Address"** for details.

TABLE 11-5: EUI-48 ADDRESS PHYSICAL MEMORY MAP EXAMPLE

Octet	0	1	2	3	4	5
Description	24-bit Organizationally Unique Identifier			24-bit Extension Identifier		
Data	00h	04h	A3h	12h	34h	56h
SFDP Address	266h					261h

Corresponding EUI-48 Address: 00-04-A3-12-34-56

Corresponding EUI-64 Address after Encapsulation: 00-04-A3-FF-FE 12-34-56

Note: Encapsulation is performed by the application software.

11.2.4 EUI-64 ADDRESS

The 8-byte EUI-64 address value of the SST26VF016BEUI is stored in the SFDP table at address locations 0x268 through 0x26F, as shown in Table 11-6. The first three bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE Registration Authority. The remaining five bytes are the Extension Identifier and are generated by Microchip to ensure a globally unique, 64-bit value.

> **Note:** In conformance with IEEE guidelines, Microchip will not use the values 0xFFFE and 0xFFFF for the first two bytes of the EUI-64 Extension Identifier. These two values and specially reserved to allow applications to encapsulate EUI-48 addresses into EUI-64 addresses.

TABLE 11-6: EUI-64 ADDRESS PHYSICAL MEMORY MAP EXAMPLE

Octet	0	1	2	3	4	5	6	7
Description	24-bit Organizationally Unique Identifier			40-bit Extension Identifier				
Data	00h	04h	A3h	12h	34h	56h	78h	90h
SFDP Address	26Fh							268h

Corresponding EUI-64 Address: 00-04-A3-12-34-56-78-90

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X][(1)]	– XXX	X	/XX
Device	Tape and Reel Option	Operating Frequency	Temperature Range	Package

Device:	SST26VF016BEUI	= 16 Mbit, 2.5V/3.0V, SQI Flash Memory WP#/Hold# pin Enable at power-up
Tape and Reel Option:	Blank T	= Standard packaging (tube or tray) = Tape and Reel[(1)]
Operating Frequency:	104	= 104 MHz
Temperature Range:	I	= -40°C to +85°C
Package:	SN	= SOIC (3.90mm), 8-Lead

Valid Combinations[(2)]:

SST26VF016BEUI-104I/SN
SST26VF016BEUIT-104I/SN

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: Contact your Microchip Sales Office for Automotive AEC Q-100 ordering information. Valid automotive part numbers are not listed on this page.

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Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.