

Silicon carbide JFET

CoolSiC™ JFET 1200 V J1 in Q-PAK

The CoolSiC™ junction-gate field-effect transistor (JFET) is a normally on semiconductor and addresses the requirements of protection circuits in solid-state power distribution.

It offers low on-state resistance and high ruggedness; additionally, the top-side cooling package enables fully automated assembly and flexible cooling path design.

Features

- Low on-state resistance $R_{DS(on)}$
- High-current avalanche ruggedness
- Surge current ruggedness
- Linear mode capability
- Overload operation up to 200°C
- Compatible with automated assembly

Potential applications

- Solid-state circuit breaker (SSCB)
- Solid-state relay (SSR)
- High voltage e-fuse

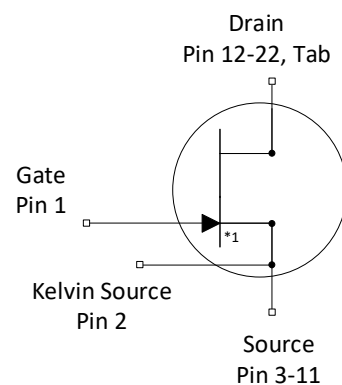
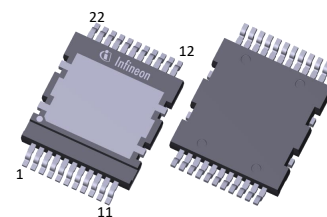
Product validation

Qualified according to relevant JEDEC tests.

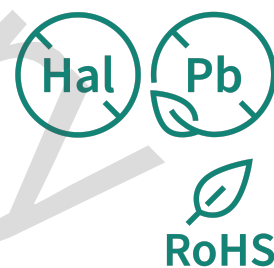
Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	1200	V
$R_{DS(on),typ}$	2.30	mΩ
I_{DM}	1313	A
I^2t	tbd	A ² s
I_{AS}	716	A

PG-HDSOP-22



*1: Internal gate diode



Part number	Package	Marking	Related links
IJCQ120RM23J1	PG-HDSOP-22	12RM23J1	see Appendix A

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1 Maximum ratings and recommendations

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source voltage	V_{DS}	-	-	1200	V	$V_{GS} = -18\text{ V}$, $T_j \geq 25^\circ\text{C}$
Continuous DC drain current	I_{DDC}	-	-	598	A	$V_{GS} = 2\text{ V}$, $T_c = 25^\circ\text{C}$, limited by bondwire
				422		$V_{GS} = 2\text{ V}$, $T_c = 105^\circ\text{C}$, limited by chip temperature
Peak drain current	I_{DM}	-	-	1313	A	$V_{GS} = 2\text{ V}$ pulse width t_p limited by $T_{j,max}$
i^2t	$\int i^2 dt$	-	-	tbd	A^2s	$V_{GS} = 2\text{ V}$, $T_j = 25^\circ\text{C}$, $t_p = 10\text{ms}$ (sine half wave)
						$V_{GS} = 2\text{ V}$, $T_j = 25^\circ\text{C}$, $t_p = 30\mu\text{s}$ (rectangular)
Avalanche energy, single pulse	E_{AS}	-	-	256	mJ	$I_D = 716\text{ A}$, $V_{GS} = -18\text{ V}$, $T_j = 25^\circ\text{C}$
Avalanche current, single pulse	I_{AS}	-	-	716	A	$V_{DD} = 100\text{ V}$, $L = 1\text{ }\mu\text{H}$, $V_{GS} = -18\text{ V}$, $T_j = 25^\circ\text{C}$
JFET dv/dt ruggedness	dv/dt	-	-	20	V/ns	$V_{GS} = -18\text{ V}$, $V_{DS} = 0\dots 850\text{V}$
Gate-source voltage	V_{GS}	-20	-	2.2	V	Static
Gate-source voltage	V_{GS}	-30	-	10	V	Transient
Power dissipation	P_{tot}	-	-	2380	W	$T_c = 25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j			175		
Operating junction temperature	T_j	-	-	200	$^\circ\text{C}$	Overload; cumulative max. 100h and max. 5000 cycles with $\Delta T \leq 100\text{K}$

Table 3 Recommended operating conditions

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate-source voltage	V_{GS}	0	2	-	V	Turn-on
		-	-18			Turn-off
Drain-source voltage	V_{DS}	-	-	850	V	Static

2 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{th(j-c)}$	-	0.045	0.063	K/W	-
Soldering temperature	T_{sold}	-	-	260	°C	Reflow soldering (MSL1 according to JEDEC J-STD-020)

3 Electrical characteristics

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSX}$	1200	-	-	V	$I_D = 55.5 \text{ mA}$, $V_{GS} = -18 \text{ V}$, $T_j = 25^\circ\text{C}$
Gate-source threshold voltage	$V_{GS(th)}$	-7.0	-5.0	-3.0	V	$I_D = 8.3 \text{ mA}$, $V_{DS} = 1 \text{ V}$, $T_j = 25^\circ\text{C}$
		-8.6	-6.5	-4.4		$I_D = 8.3 \text{ mA}$, $V_{DS} = 850 \text{ V}$, $T_j = 25^\circ\text{C}$
Drain cut-off current	$I_{D(off)}$	-	55.5	305.1	μA	$V_{DS} = 1200 \text{ V}$, $V_{GS} = -18 \text{ V}$, $T_j = 25^\circ\text{C}$
			111.0	-		$V_{DS} = 1200 \text{ V}$, $V_{GS} = -18 \text{ V}$, $T_j = 175^\circ\text{C}$
			2.8	6.1		$V_{DS} = 850 \text{ V}$, $V_{GS} = -18 \text{ V}$, $T_j = 25^\circ\text{C}$
			5.548	-		$V_{DS} = 850 \text{ V}$, $V_{GS} = -18 \text{ V}$, $T_j = 175^\circ\text{C}$
Reverse gate current	I_{GSS}	-	0.17	18.31	μA	$V_{DS} = 0 \text{ V}$, $V_{GS} = -18 \text{ V}$, $T_j = 25^\circ\text{C}$
			1.00	-		$V_{DS} = 0 \text{ V}$, $V_{GS} = -18 \text{ V}$, $T_j = 175^\circ\text{C}$
Forward gate current	I_{GF}	-	51	-	μA	$V_{DS} = 0 \text{ V}$, $V_{GS} = 2 \text{ V}$, $T_j = 25^\circ\text{C}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.70	-	$\text{m}\Omega$	$I_D = 55.0 \text{ A}$, $V_{GS} = 0 \text{ V}$, $T_j = 25^\circ\text{C}$
			2.30	-		$I_D = 55.0 \text{ A}$, $V_{GS} = 2 \text{ V}$, $T_j = 25^\circ\text{C}$
			4.30	-		$I_D = 55.0 \text{ A}$, $V_{GS} = 0 \text{ V}$, $T_j = 105^\circ\text{C}$
			3.70	-		$I_D = 55.0 \text{ A}$, $V_{GS} = 2 \text{ V}$, $T_j = 105^\circ\text{C}$
			5.80	7.40		$I_D = 55.0 \text{ A}$, $V_{GS} = 0 \text{ V}$, $T_j = 150^\circ\text{C}$
			5.00	6.50		$I_D = 55.0 \text{ A}$, $V_{GS} = 2 \text{ V}$, $T_j = 150^\circ\text{C}$
Internal gate resistance	$R_{G,int}$	-	0.4	-	Ω	$f = 1 \text{ MHz}$, $T_j = 25^\circ\text{C}$

Table 6 Dynamic characteristics

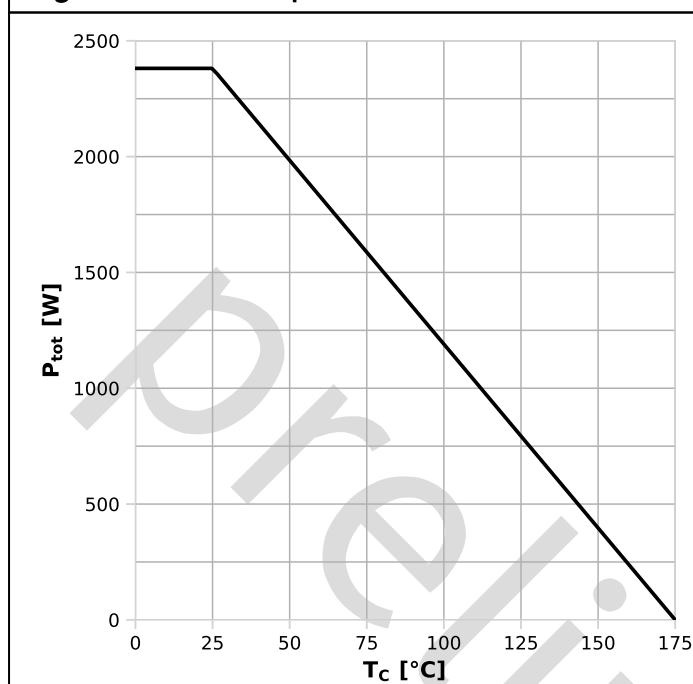
Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	9961	-	pF	$V_{GS} = -18 \text{ V}$, $V_{DS} = 850 \text{ V}$, $f = 100 \text{ kHz}$, $T_j = 25^\circ\text{C}$
Reverse transfer capacitance	C_{rss}		620			
Output capacitance	C_{oss}		630			
Turn-on delay time	$t_{d(on)}$	-	51	-	ns	$I_D = 55 \text{ A}$, $V_{DD} = 850 \text{ V}$, $V_{GS} = -18/2 \text{ V}$, $R_{G,ext} = 1.6 \Omega$, $T_j = 25^\circ\text{C}$, commutation against separate diode
Rise time	t_r		178		ns	
Turn-off delay time	$t_{d(off)}$		89		ns	
Fall time	t_f		99		ns	
Turn-on switching loss	E_{on}		4192		μJ	
Turn-off switching loss	E_{off}		2262		μJ	
Total switching loss	E_{tot}		6454		μJ	

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate-source charge below plateau	$Q_{GS(pl)}$	-	139	-	nC	$I_D = 55.0\text{ A}$, $V_{DD} = 850\text{ V}$, $V_{GS} = -18/2\text{ V}$, $T_j = 25^\circ\text{C}$
Gate-drain charge	Q_{GD}		801			
Total gate charge	Q_G		1404			

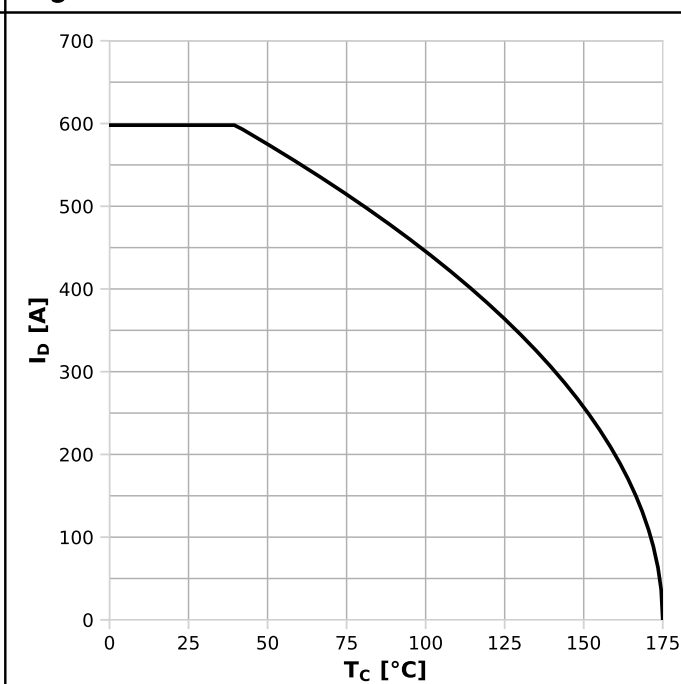
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



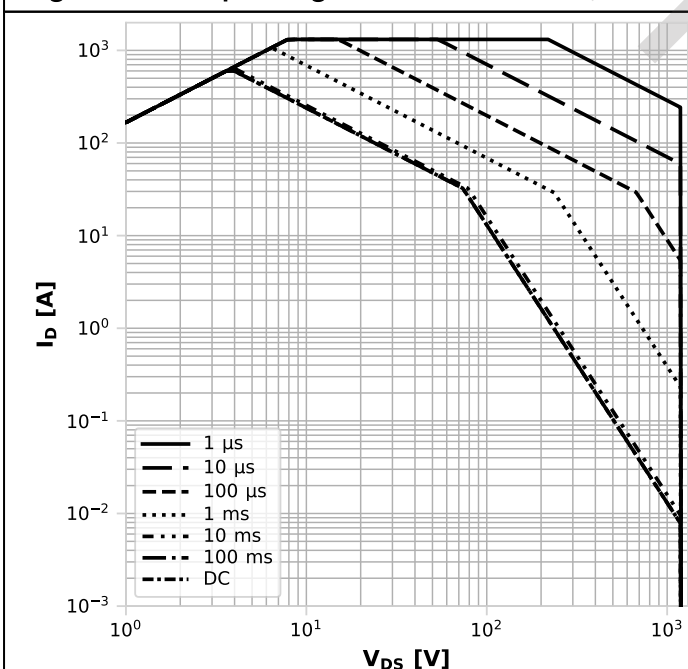
$$P_{\text{tot}} = f(T_c)$$

Diagram 2: Drain Current



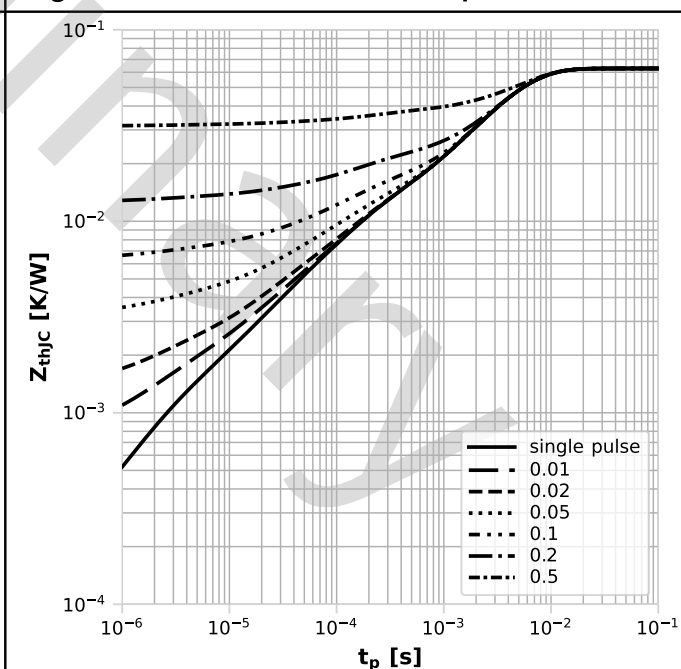
$$I_D = f(T_c); V_{GS} = 2 \text{ V}$$

Diagram 3: Safe operating area



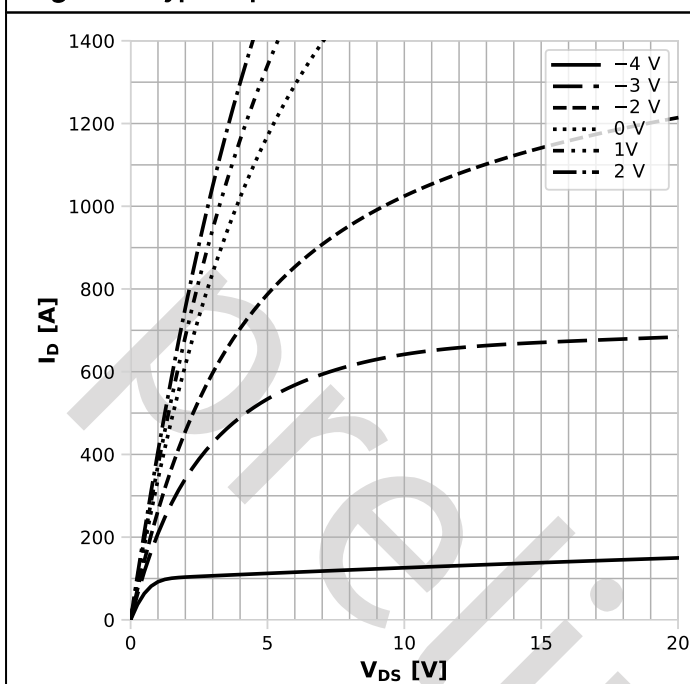
$$I_D = f(V_{DS}); T_c = 25 \text{ °C}; D = 0; \text{parameter: } t_p$$

Diagram 4: Max. transient thermal impedance



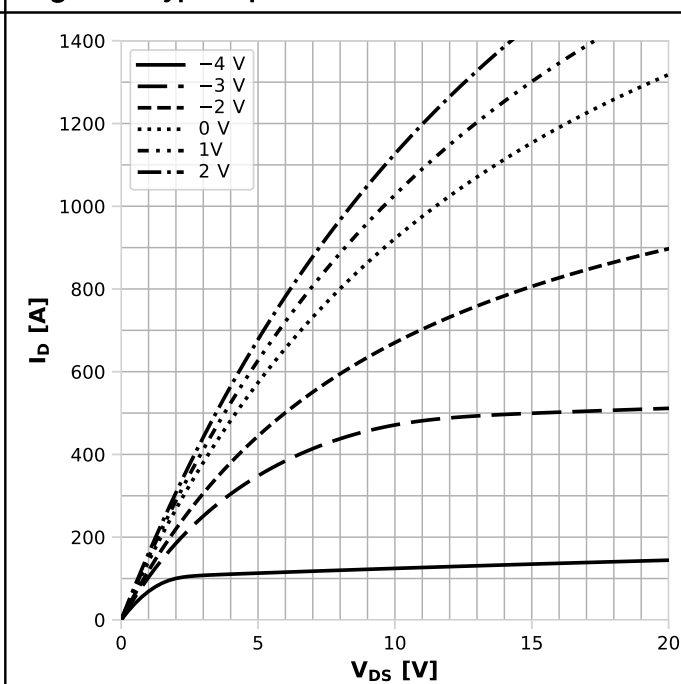
$$Z_{thJC} = f(t_p); \text{parameter: } D = t_p / T$$

Diagram 5: Typ. output characteristics



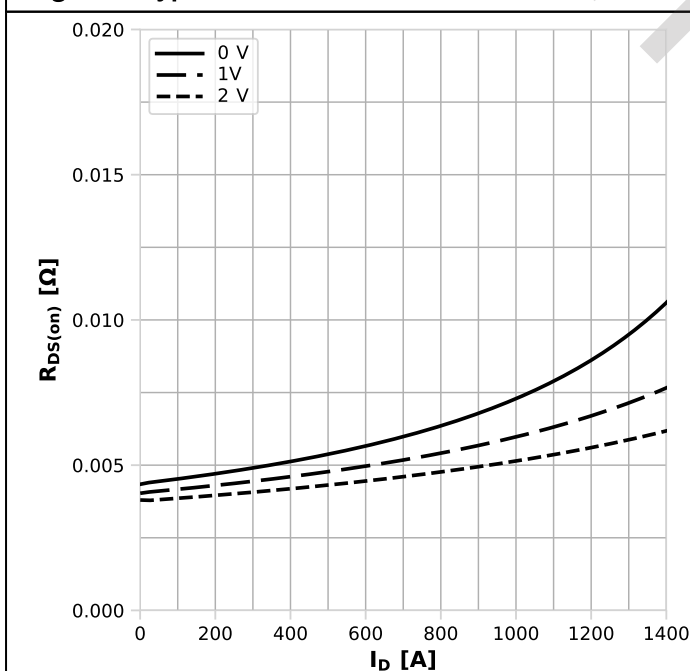
$I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



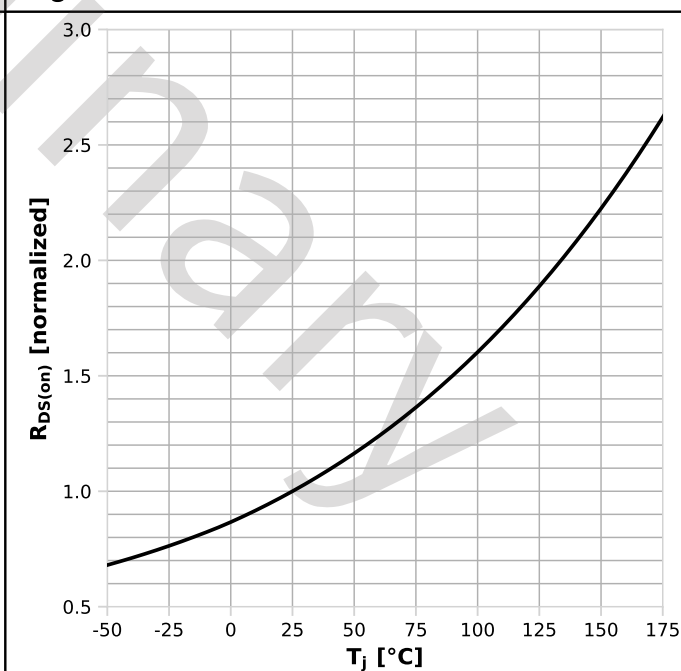
$I_D = f(V_{DS})$; $T_j = 175^\circ\text{C}$; parameter: V_{GS}

Diagram 7 Typ. drain-source on-state resistance



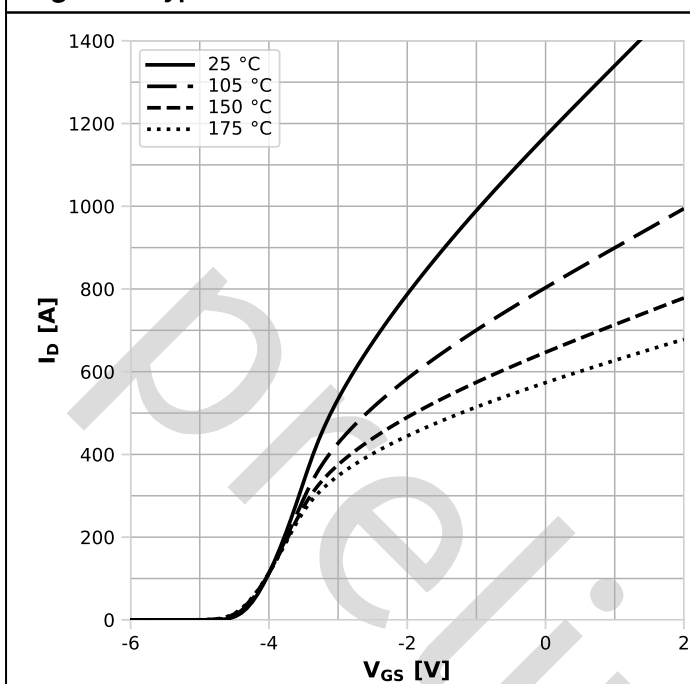
$R_{DS(on)} = f(I_D)$; $T_j = 105^\circ\text{C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



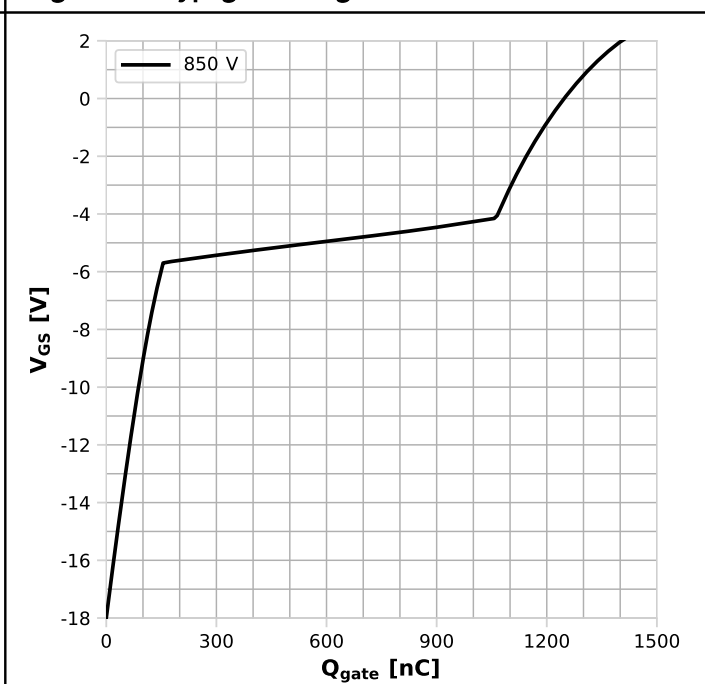
$R_{DS(on)} = f(T_j) / f(25^\circ\text{C})$; $I_D = 55.0\text{ A}$; $V_{GS} = 2\text{ V}$

Diagram 9: Typ. transfer characteristics



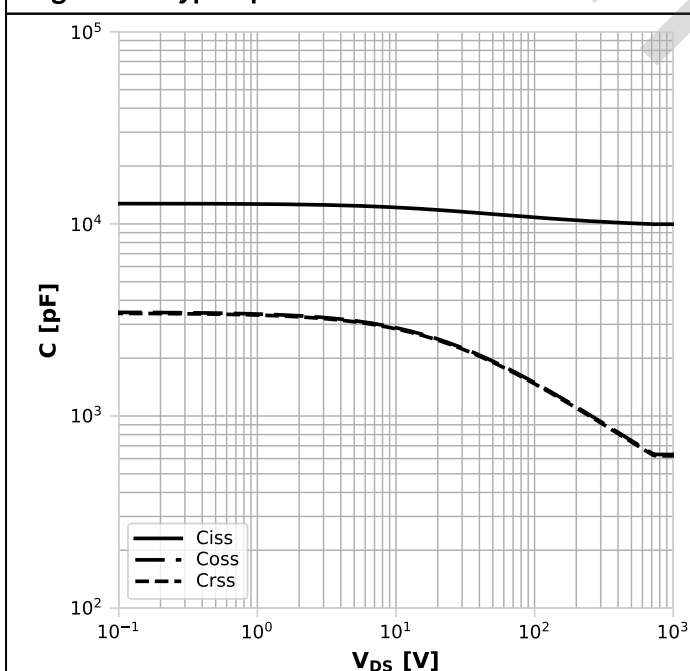
$I_D = f(V_{GS})$; $V_{DS} = 5 \text{ V}$; parameter: T_j

Diagram 10: Typ. gate charge



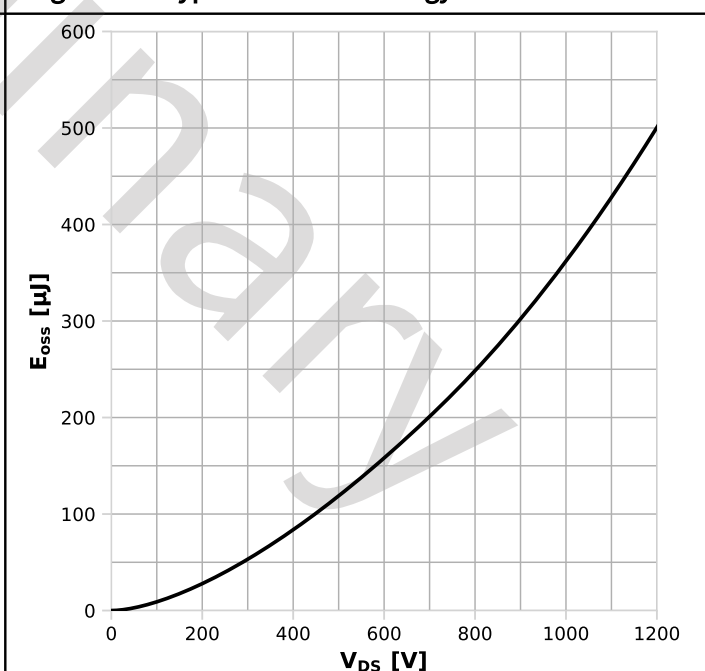
$V_{GS} = f(Q_{gate})$; $I_D = 55.0 \text{ A pulsed}$; $V_{DS} = -18 \text{ V}$; parameter: V_{DD}

Diagram 11: Typ. capacitances AC



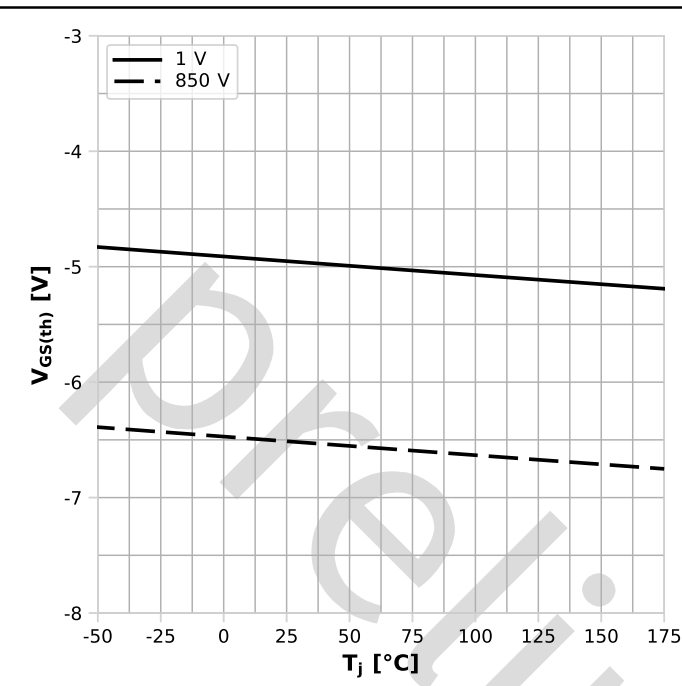
$C = f(V_{DS})$; $V_{GS} = -18 \text{ V}$; $f = 100 \text{ kHz}$

Diagram 12: Typ. Coss stored energy



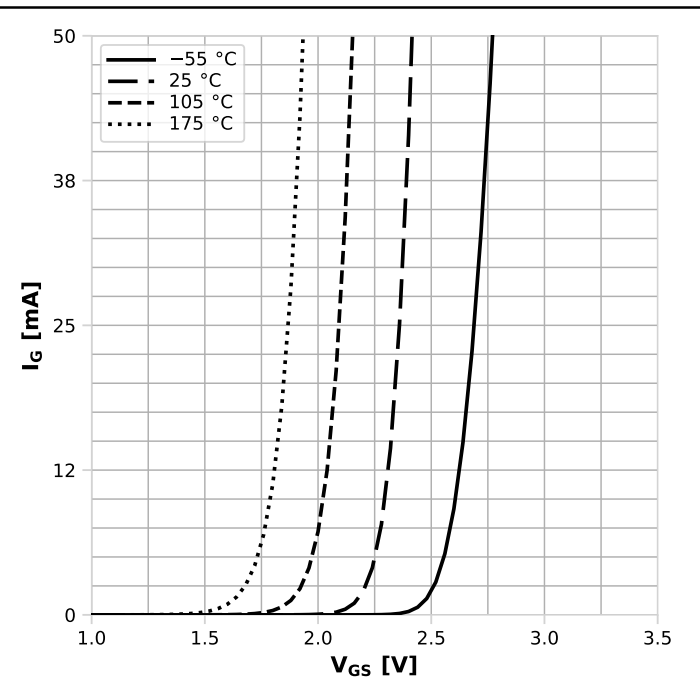
$E_{oss} = f(V_{DS})$; $V_{GS} = -18 \text{ V}$

Diagram 13: Typ. gate threshold voltage



$V_{GS(th)} = f(T_j)$, $I_D = 8.3$ mA; parameter: V_{DS}

Diagram 14: Typ. transfer gate forward current



$I_G = f(V_{GS})$; $V_{DS} = 0$ V; parameter: T_j

5 Test circuits

Table 8 Switching times

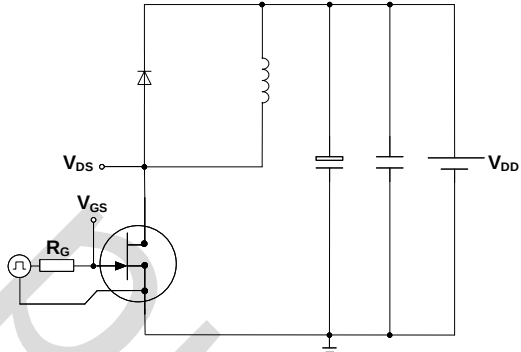
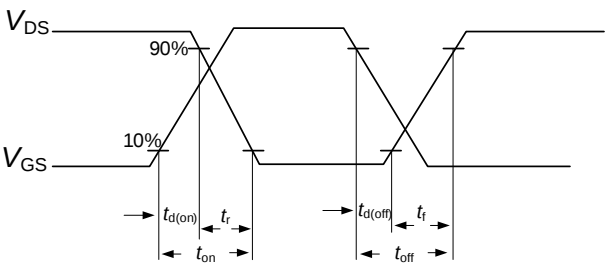
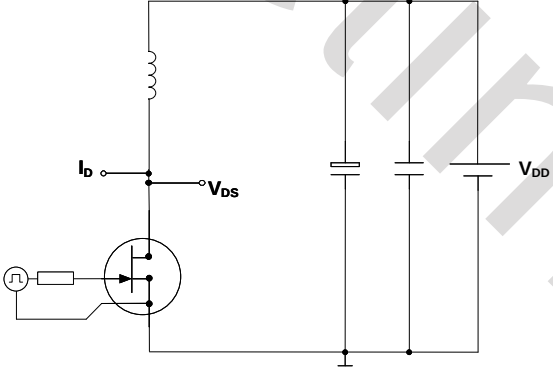
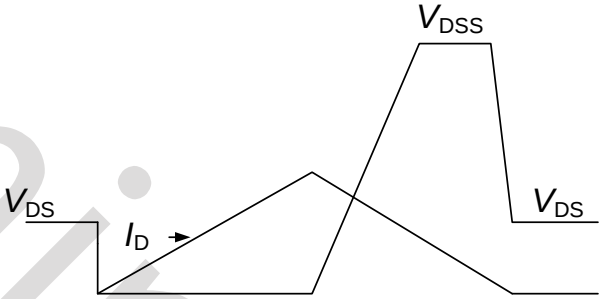
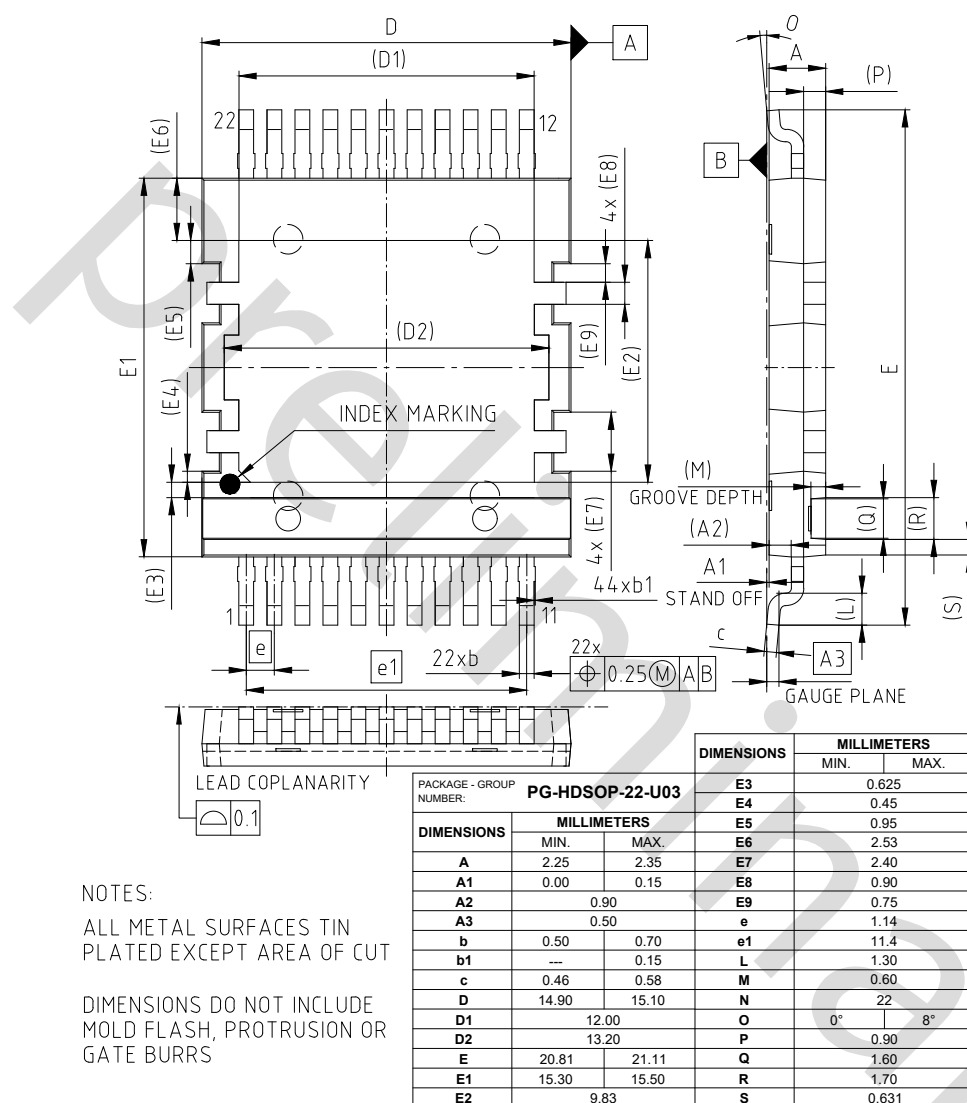
Switching times test circuit for inductive load	Switching times waveform
	

Table 9 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package outlines



NOTES:
ALL METAL SURFACES TIN
PLATED EXCEPT AREA OF CUT

DIMENSIONS DO NOT INCLUDE
MOLD FLASH, PROTRUSION OR
GATE BURRS

Figure 1 Outline PG-HDSOP-22, dimensions in mm

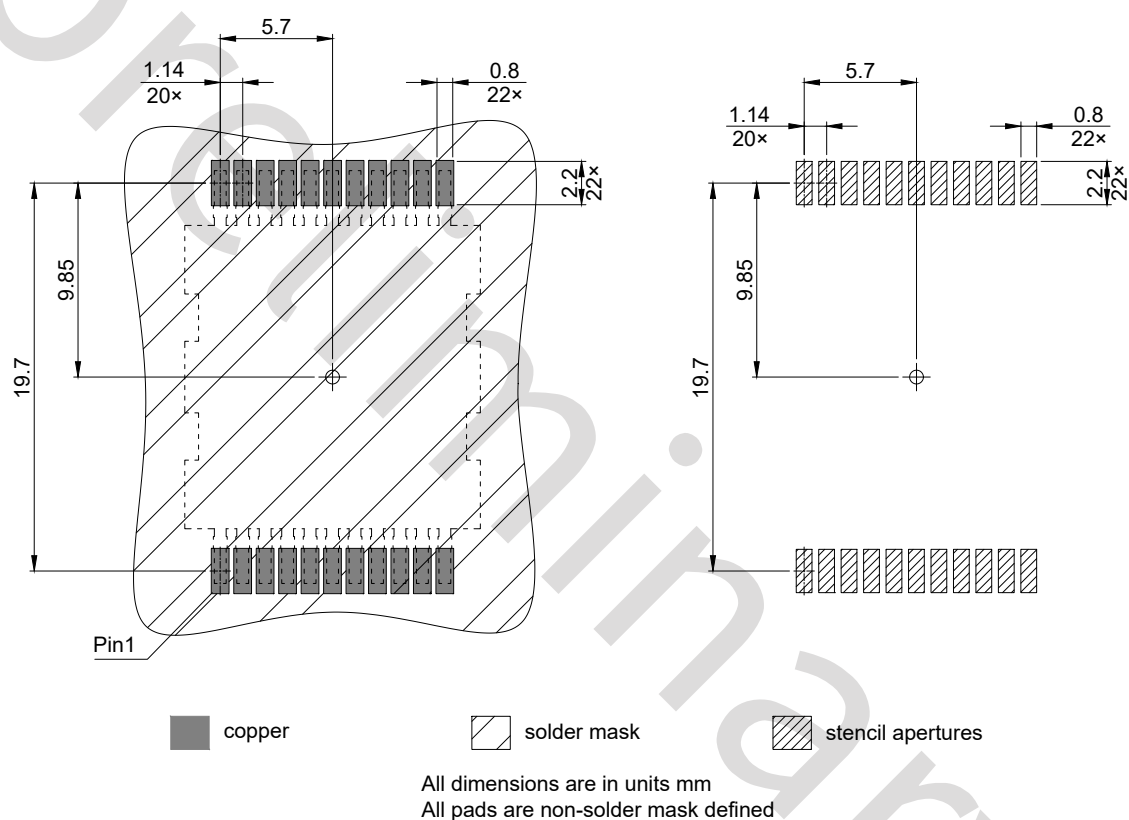


Figure 2 Footprint drawing PG-HDSOP-22, dimensions in mm

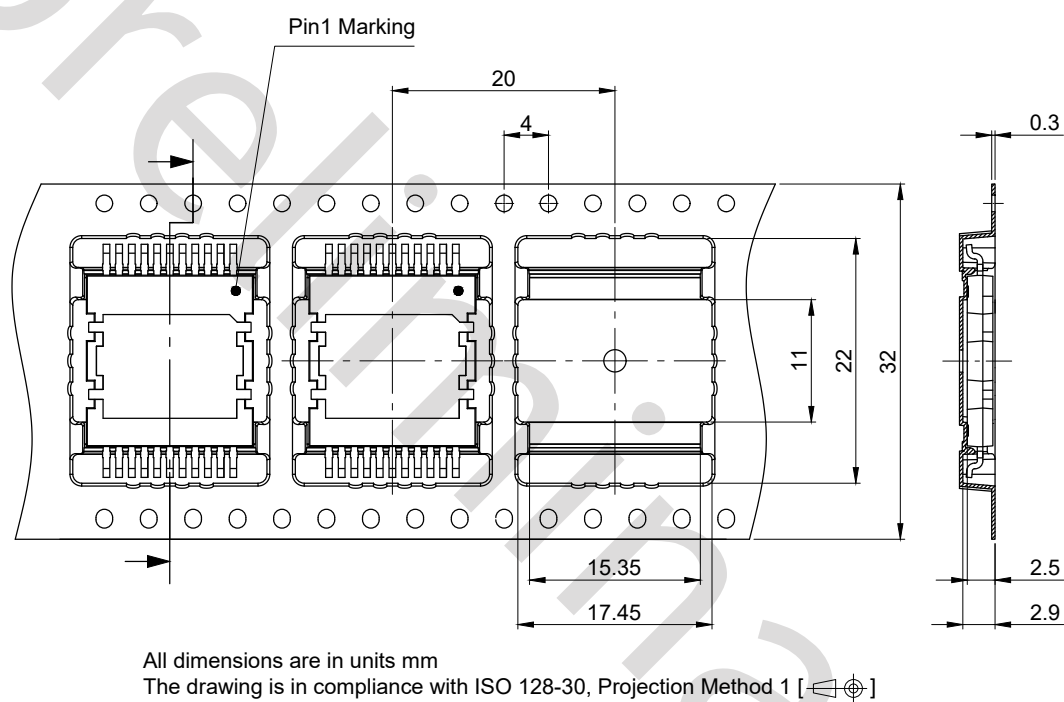


Figure 3 Packaging variant PG-HDSOP-22, dimensions in mm

7 Appendix A

Table 10 **Related links**

- [IFX CoolSiC™ JFET 1200 V J1 Webpage](#)
- [IFX CoolSiC™ JFET 1200 V J1 Application Note](#)
- [IFX CoolSiC™ JFET 1200 V J1 Simulation Model](#)
- [IFX Design tools](#)

Preliminary

Revision history

IJCQ120RM23J1

Revision 2026-06-08, Rev. 0.2

Previous revisions

Revision	Date	Subjects (major changes since last revision)
0.1	2026-04-23	Release of preliminary version
0.2	2026-06-08	updated DC conduction and SOA model

Preliminary

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