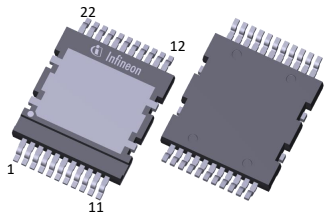
Silicon carbide JFET

CoolSiC™ JFET 1200 V J1 in Q-DPAK

PG-HDSOP-22

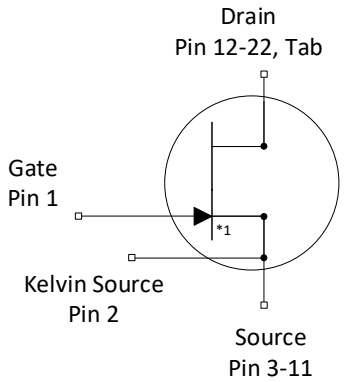


The CoolSiC™ junction-gate field-effect transistor (JFET) is a normally on semiconductor and addresses the requirements of protection circuits in solid-state power distribution.

It offers low on-state resistance and high ruggedness; additionally, the top-side cooling package enables fully automated assembly and flexible cooling path design.

Features

- Low on-state resistance $R_{DS(on)}$
- High-current avalanche ruggedness
- Surge current ruggedness
- Linear mode capability
- Overload operation up to 200°C
- Compatible with automated assembly



1: Internal gate diode

Potential applications

- Solid-state circuit breaker (SSCB)
- Solid-state relay (SSR)
- High voltage e-fuse

Product validation

Qualified according to relevant JEDEC tests.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	1200	V
$R_{DS(on),typ}$	6.10	mΩ
I_{DM}	504	A
i^2t	tbd	A^2s
I_{AS}	519	A

Hal Pb RoHS

Part number	Package	Marking	Related links
IJCQ120RM61J1	PG-HDSOP-22	12RM61J1	see Appendix A

Table of contents

1 Maximum ratings and recommendations

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source voltage	V_{DS}	-	-	1200	V	V_{GS} = -18 V, $T_j \geq$ 25°C
Continuous DC drain current	I_{DDC}	-	-	238	A	V_{GS} = 2 V, T_c = 25°C, limited by chip temperature
				162		V_{GS} = 2 V, T_c = 105°C, limited by chip temperature
Peak drain current	I_{DM}	-	-	504	A	V_{GS} = 2 V pulse width t_p limited by $T_{j,max}$
i^2t	$\int i^2\,dt$	-	-	tbd	A^2s	V_{GS} = 2 V, T_j = 25°C, t_p = 10ms (sine half wave)
						V_{GS} = 2 V, T_j = 25°C, t_p = 30µs (rectangular)
Avalanche energy, single pulse	E_{AS}	-	-	135	mJ	I_D = 519 A, V_{GS} = -18 V, T_j = 25°C
Avalanche current, single pulse	I_{AS}	-	-	519	A	V_{DD}= 100 V, L = 1 µH, V_{GS} = -18 V, T_j = 25°C
JFET *dv/dt* ruggedness	*dv/dt*	-	-	20	V/ns	V_{GS} = -18 V, V_{DS} = 0...850V
Gate-source voltage	V_{GS}	-20	-	2.2	V	Static
Gate-source voltage	V_{GS}	-30	-	10	V	Transient
Power dissipation	P_{tot}	-	-	931	W	T_C = 25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j			175		
Operating junction temperature	T_j	-	-	200	°C	Overload; cumulative max. 100h and max. 5000 cycles with ΔT ≤ 100K

Table 3 Recommended operating conditions

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate-source voltage	V_{GS}	0	2	-	V	Turn-on
		-	-18			Turn-off
Drain-source voltage	V_{DS}	-	-	850	V	Static

2 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{th(j-c)}$	-	0.115	0.161	K/W	-
Soldering temperature	T_{sold}	-	-	260	°C	Reflow soldering (MSL1 according to JEDEC J-STD-020)

3 Electrical characteristics

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSX}$	1200	-	-	V	I_D = 20.1 mA, V_{GS} = -18 V, T_j = 25°C
Gate-source threshold voltage	$V_{GS(th)}$	-7.0	-5.0	-3.0	V	I_D = 3.0 mA, V_{DS} = 1 V, T_j = 25°C
		-8.6	-6.5	-4.4		I_D = 3.0 mA V_{DS} = 850 V , T_j = 25°C
Drain cut-off current	$I_{D(off)}$	-	20.1	110.6	µA	V_{DS} = 1200 V, V_{GS} = -18 V, T_j = 25°C
			40.2	-		V_{DS} = 1200 V, V_{GS} = -18 V, T_j = 175°C
			1.0	2.2		V_{DS} = 850 V, V_{GS} = -18 V, T_j = 25°C
			2.011	-		V_{DS} = 850 V, V_{GS} = -18 V, T_j = 175°C
Reverse gate current	I_{GSS}	-	0.06	6.64	µA	V_{DS} = 0 V, V_{GS} = -18 V, T_j = 25°C
			0.36	-		V_{DS} = 0 V, V_{GS} = -18 V, T_j = 175°C
Forward gate current	I_{GF}	-	19	-	µA	V_{DS} = 0 V, V_{GS} = 2 V, T_j = 25°C
Drain-source on-state resistance	$R_{DS(on)}$	-	7.20	-	mΩ	I_D = 20.1 A, V_{GS} = 0 V, T_j = 25°C
			6.10	-		I_D = 20.1 A, V_{GS} = 2 V, T_j = 25°C
			11.70	-		I_D = 20.1 A, V_{GS} = 0 V, T_j = 105°C
			10.00	-		I_D = 20.1 A, V_{GS} = 2 V, T_j = 105°C
			15.60	20.10		I_D = 20.1 A, V_{GS} = 0 V, T_j = 150°C
			13.60	17.50		I_D = 20.1 A, V_{GS} = 2 V, T_j = 150°C
Internal gate resistance	$R_{G,int}$	-	1.1	-	Ω	f = 1 MHz, T_j = 25°C

Table 6 Dynamic characteristics

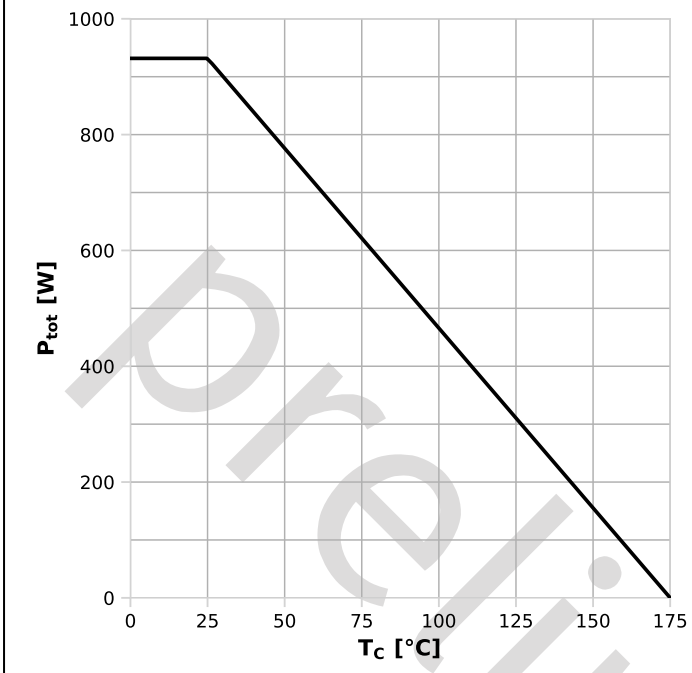
Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	3634	-	pF	V_{GS} = -18 V, V_{DS} = 850 V, f = 100 kHz, T_j = 25°C
Reverse transfer capacitance	C_{rss}		214			
Output capacitance	C_{oss}		218			
Turn-on delay time	$t_{d(on)}$	-	29	-	ns	I_D = 55 A, V_{DD} = 850 V, V_{GS} = -18/2 V, $R_{G,ext}$ = 1.6 Ω, T_j = 25°C, commutation against separate diode
Rise time	t_r		81		ns	
Turn-off delay time	$t_{d(off)}$		48		ns	
Fall time	t_f		53		ns	
Turn-on switching loss	E_{on}		1122		µJ	
Turn-off switching loss	E_{off}		118		µJ	
Total switching loss	E_{tot}		1240		µJ	

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate-source charge below plateau	$Q_{GS(pl)}$	-	50	-	nC	I_D = 20.1 A, V_{DD} = 850 V, V_{GS} = -18/2 V, T_j = 25°C
Gate-drain charge	Q_{GD}		274			
Total gate charge	Q_G		494			

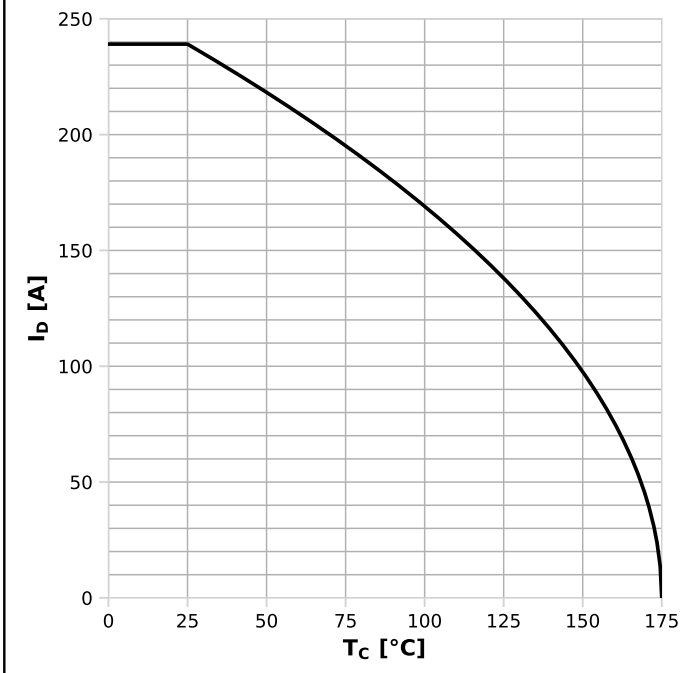
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



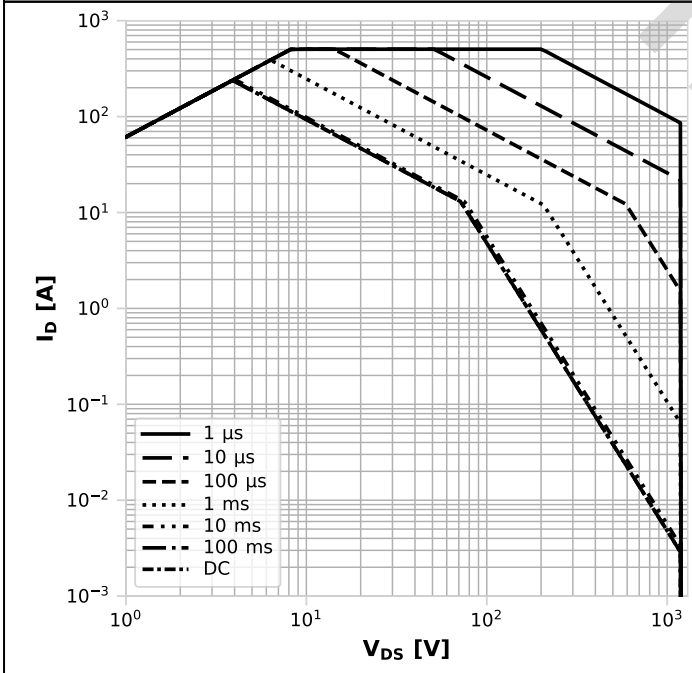
P_{tot}=f(T_C)

Diagram 2: Drain Current



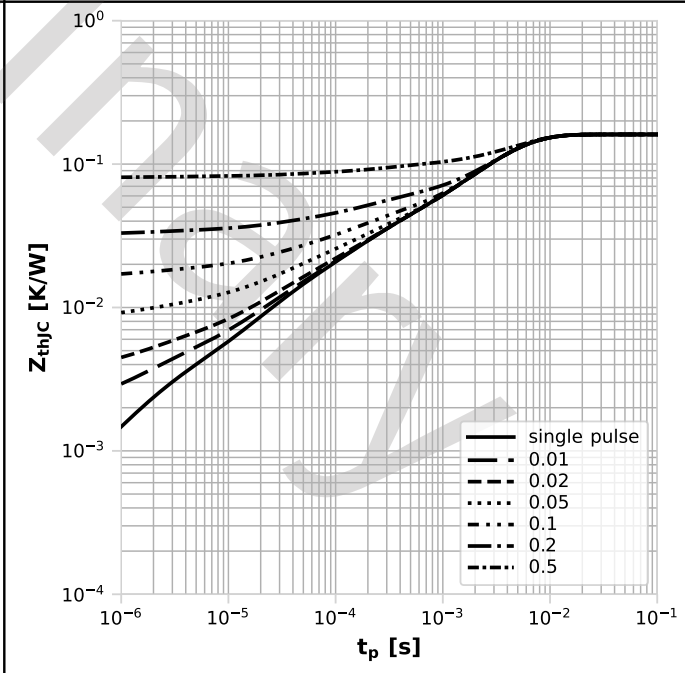
I_D=f(T_C); V_{GS}=2 V

Diagram 3: Safe operating area



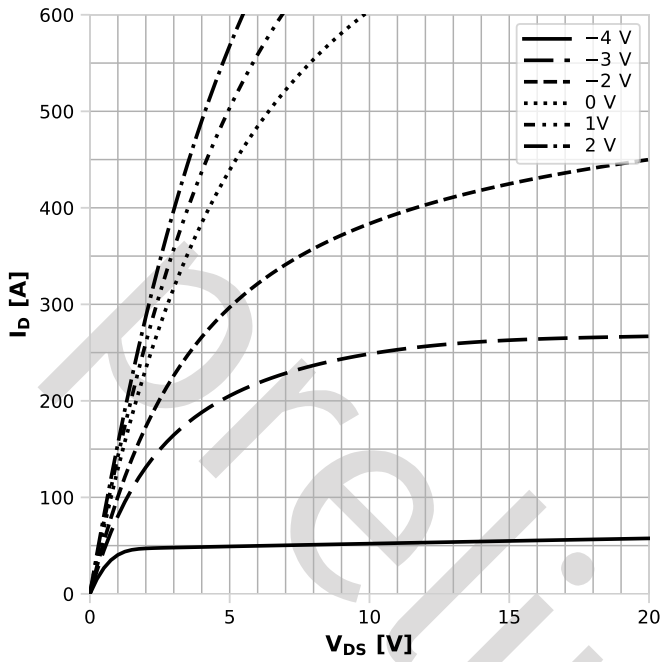
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



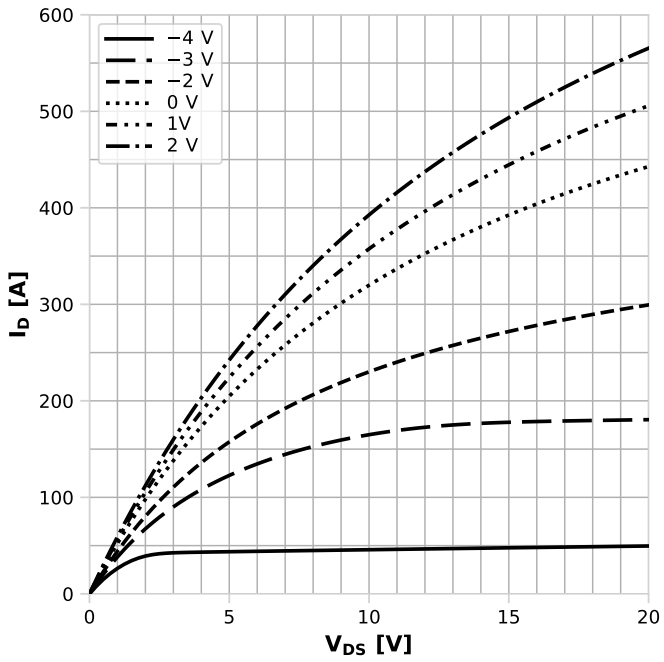
Z_{thJC} =f(t_P); parameter: D= t_p/T

Diagram 5: Typ. output characteristics



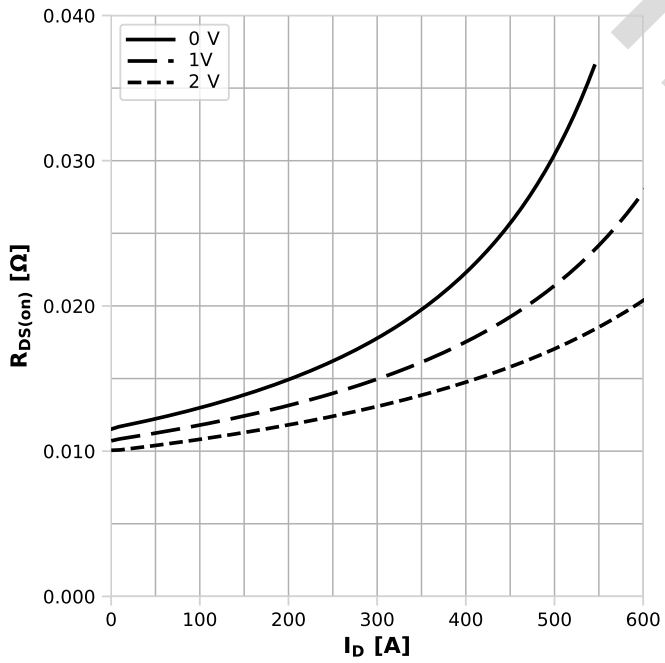
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



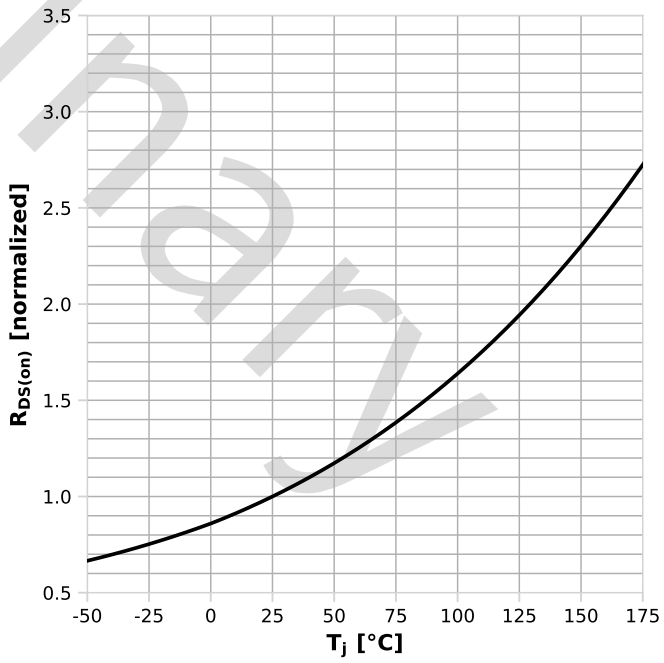
I_D=f(V_{DS}); T_j=175 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



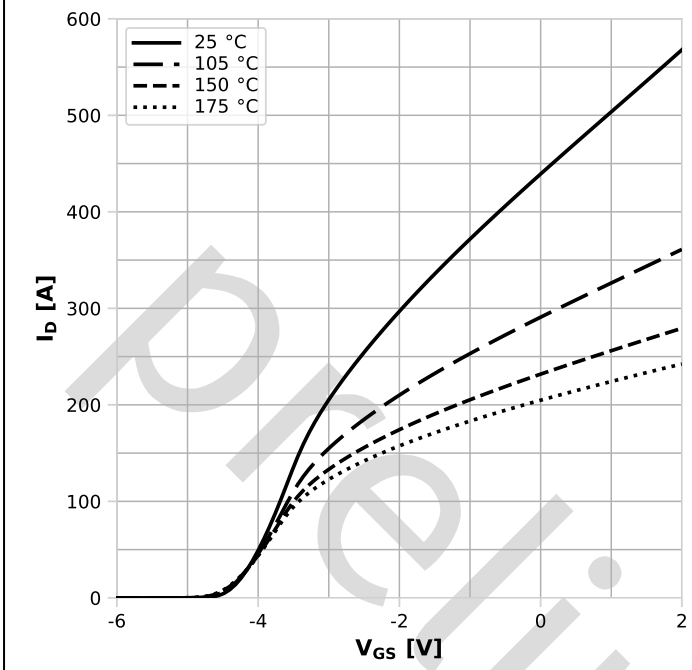
$R_{DS(on)}$=f(I_D); T_j=105 °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



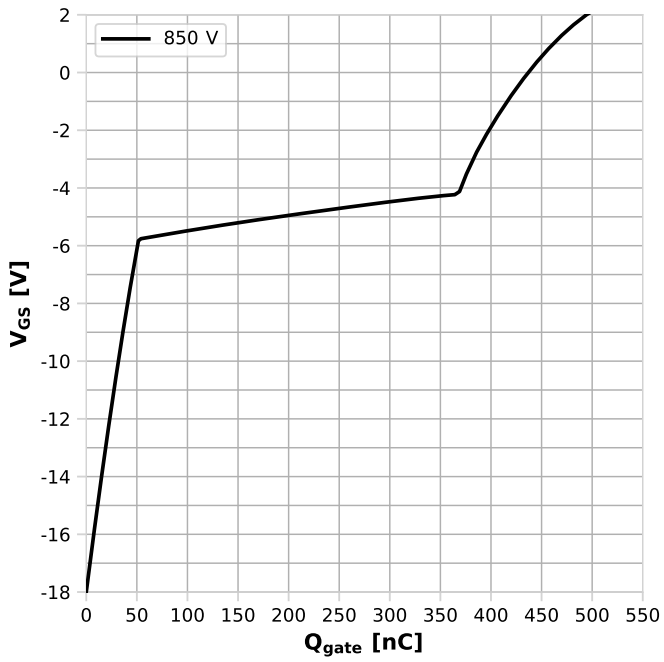
$R_{DS(on)}$=f(T_j)/f(25 °C); I_D=20.1 A; V_{GS}=2 V

Diagram 9: Typ. transfer characteristics



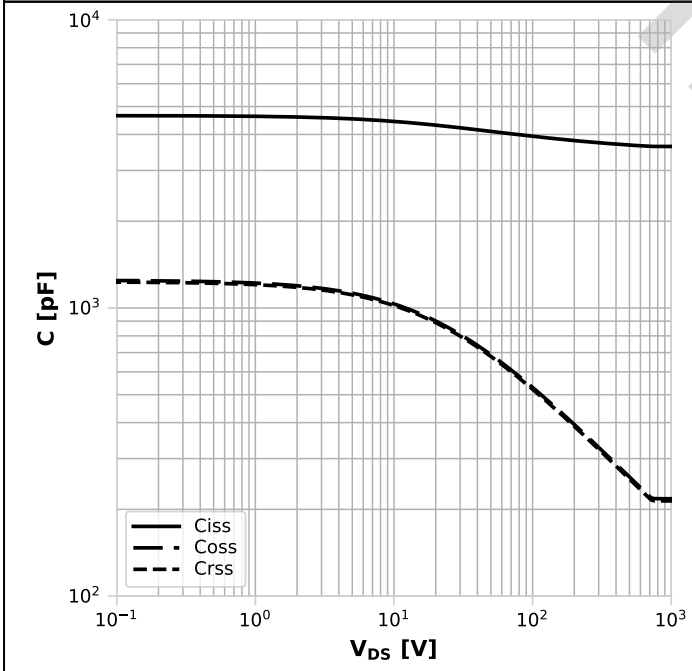
I_D=f(V_{GS}); V_{DS}=5 V; parameter: T_j

Diagram 10: Typ. gate charge



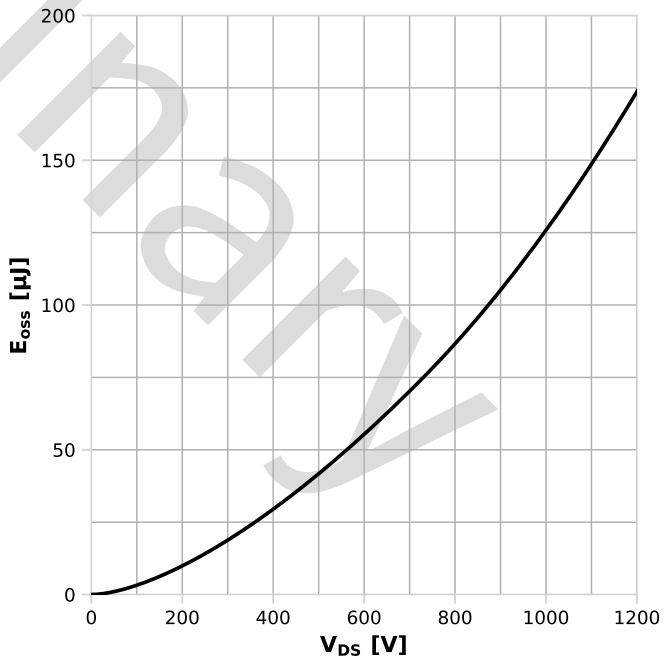
V_{GS}=f(Q_{gate}); I_D=20.1 A pulsed; V_{dr}=-18 V; parameter: V_{DD}

Diagram 11: Typ. capacitances AC

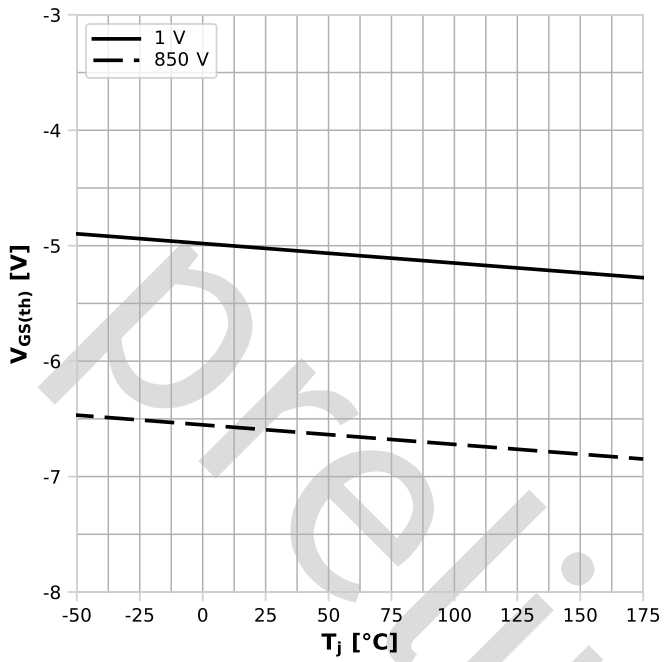
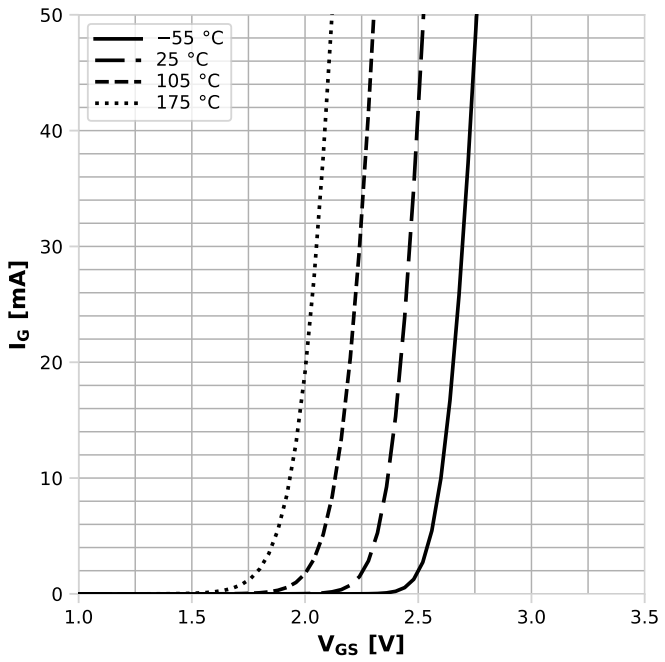


C=f(V_{DS}); V_{GS}=-18 V; f=100 kHz

Diagram 12: Typ. Coss stored energy



E_{oss}=f(V_{DS}); V_{GS}=-18 V

Diagram 13: Typ. gate threshold voltage	Diagram 14: Typ. transfer gate forward current
	
$V_{GS(th}$=f(T_j), I_D=3.0 mA; parameter: V_{DS}	I_G=f(V_{GS}); V_{DS}=0V; parameter: T_j

5 Test circuits

Table 8 Switching times

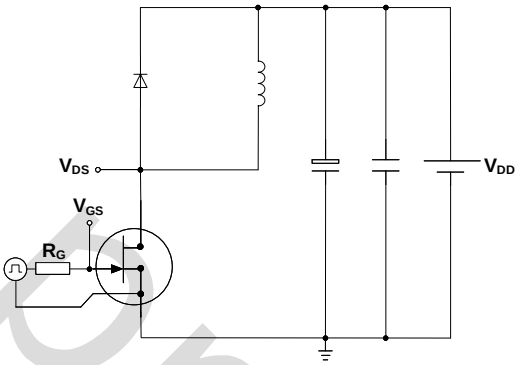
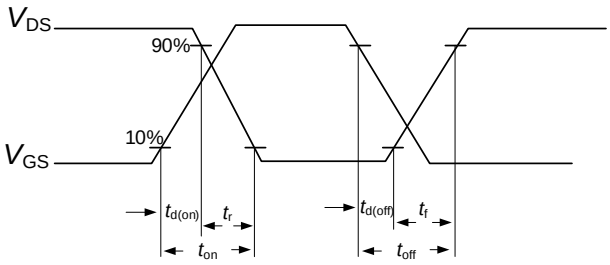
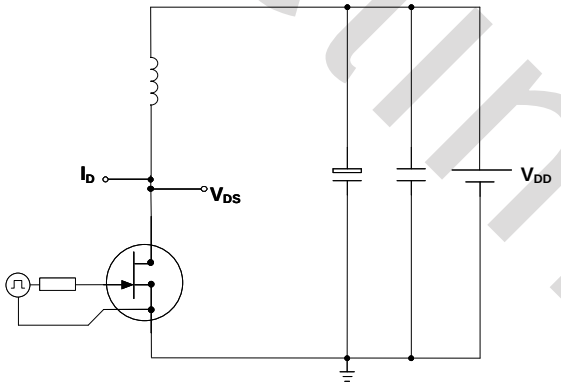
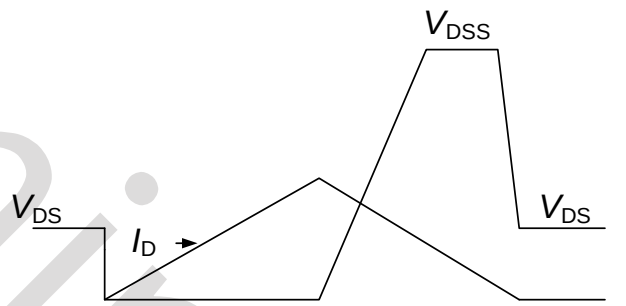
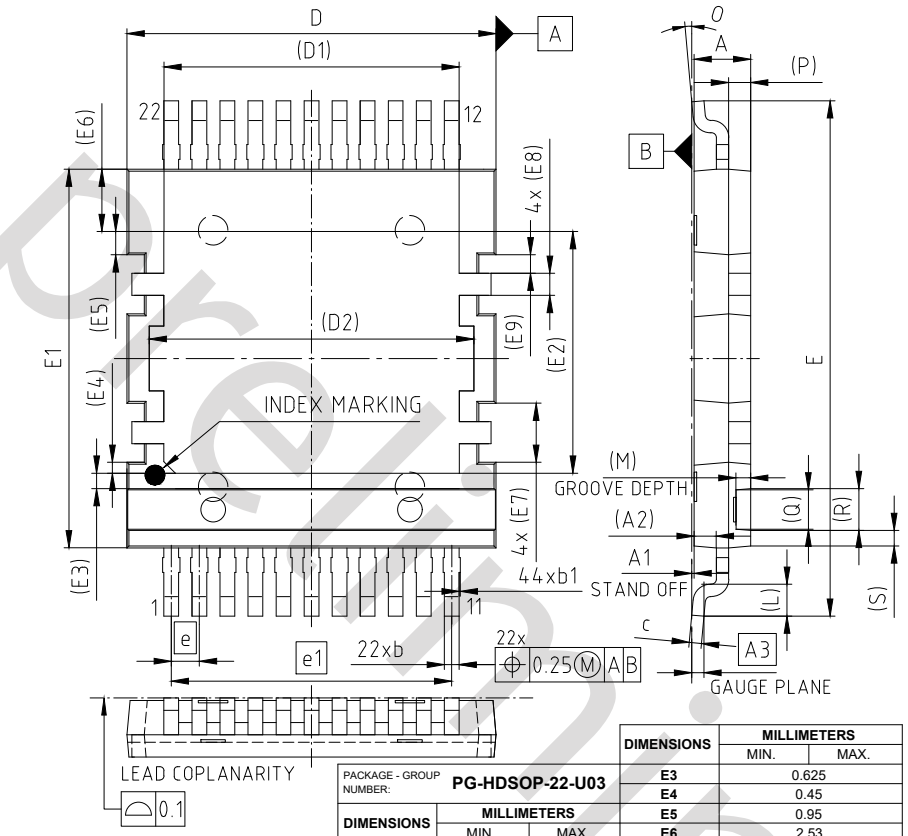
Switching times test circuit for inductive load	Switching times waveform
	

Table 9 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package outlines



NOTES:

ALL METAL SURFACES TIN PLATED EXCEPT AREA OF CUT

DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

PACKAGE - GROUP NUMBER: PG-HDSOP-22-U03

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.25	2.35
A1	0.00	0.15
A2	0.90	
A3	0.50	
b	0.50	0.70
b1	---	0.15
c	0.46	0.58
D	14.90	15.10
D1	12.00	
D2	13.20	
E	20.81	21.11
E1	15.30	15.50
E2	9.83	

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
E3	0.625	
E4	0.45	
E5	0.95	
E6	2.53	
E7	2.40	
E8	0.90	
E9	0.75	
e	1.14	
e1	11.4	
L	1.30	
M	0.60	
N	22	
O	0°	8°
P	0.90	
Q	1.60	
R	1.70	
S	0.631	

Figure 1 Outline PG-HDSOP-22, dimensions in mm

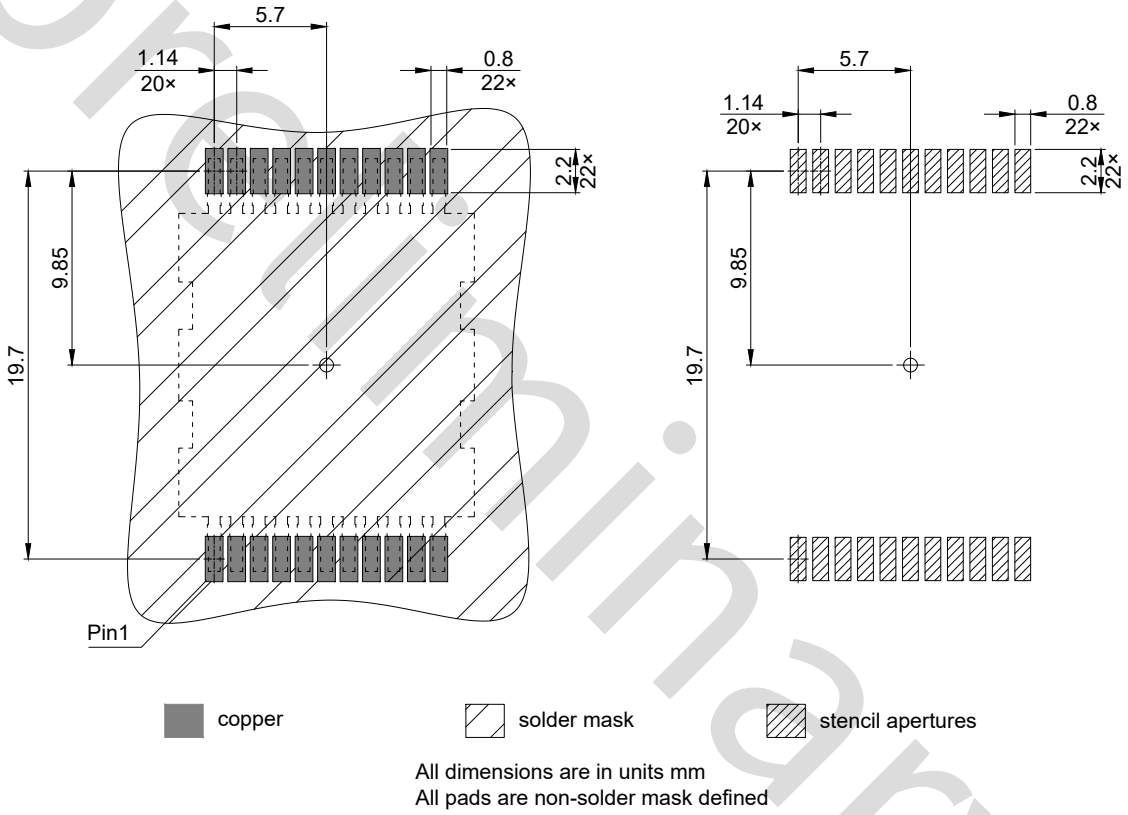


Figure 2 Footprint drawing PG-HDSOP-22, dimensions in mm

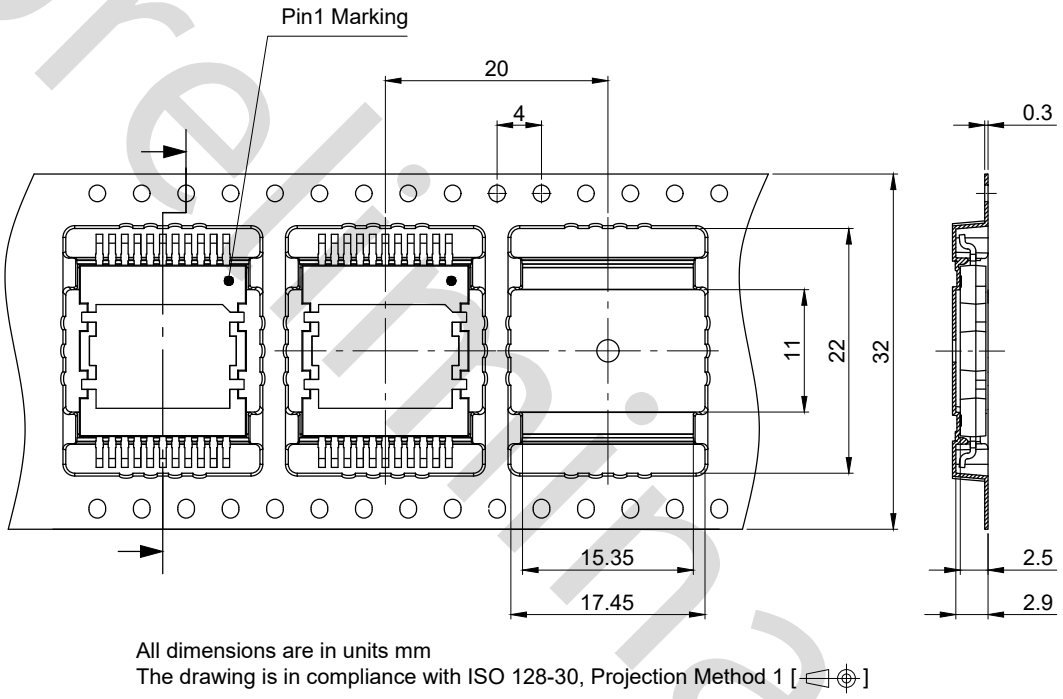


Figure 3 Packaging variant PG-HDSOP-22, dimensions in mm

7 Appendix A

Table 10 Related links

- IFX CoolSiC™ JFET 1200 V J1 Webpage
- IFX CoolSiC™ JFET 1200 V J1 Application Note
- IFX CoolSiC™ JFET 1200 V J1 Simulation Model
- IFX Design tools

Revision history

IJCQ120RM61J1

Revision 2026-06-08, Rev. 0.2

Previous revisions

Revision	Date	Subjects (major changes since last revision)
0.1	2026-05-07	Release of preliminary version
0.2	2026-06-08	updated DC conduction and SOA model

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