AIROC™ Bluetooth® & Bluetooth® Low Energy: CYW55310

Description

The AIROC™ CYW55310 is a single chip Bluetooth®, Low Energy Qualified against Bluetooth® Core 6.1-compliant, supporting basic rate, enhanced data rate (EDR), Bluetooth® Low Energy 2 Mbps, Bluetooth® Low Energy 1 Mbps, long-range (LR), and Low Energy Coded Phy with advertising coding selection. The device supports Bluetooth® Low Energy audio, with LC3 codec running on the device enabling typical Smart watch audio use cases. A pair of time-division multiplexing (TDM) interfaces enables a flexible interface for various audio use cases and a PDM interface is available for connecting digital microphones. The device includes on-chip power amplifiers supporting three different output power paths optimized for best efficiency; +4 dBm, +13 dBm, and +19 dBm path for driving poor antennas in wearable devices. 12-bit ADC with seven channel mux input for DC sensing. The +4 dBm path only supports BDR, LE1, LE2, LELR modulation schemes. The device also features a flexible Bluetooth® receiver offering a dedicated Bluetooth® LNA (dLNA) path. A 4-wire UART interface is available for interfacing with the host processor.

The CYW55310 family is designed to address the needs of the Internet of Things (IoT) devices that require minimal power consumption and compact size. It includes a power management unit (PMU) and requires a 37.4 MHz crystal which provides the system reference clock, and can operate from an external 32.768 kHz crystal (eLPO) for higher accuracy or from an external reference clock.

The CYW55310 family includes an advanced coexistence hardware mechanisms and algorithms to optimize Bluetooth® operation for maximum performance. In addition, the coexistence support is available for external radios such as (LTE, GPS, and ZigBee) via an external interface. CYW55310 family operates over the -40°C to +85°C temperature range and is available in a 0.35 mm pitch WLBGA package.

Functional block diagram

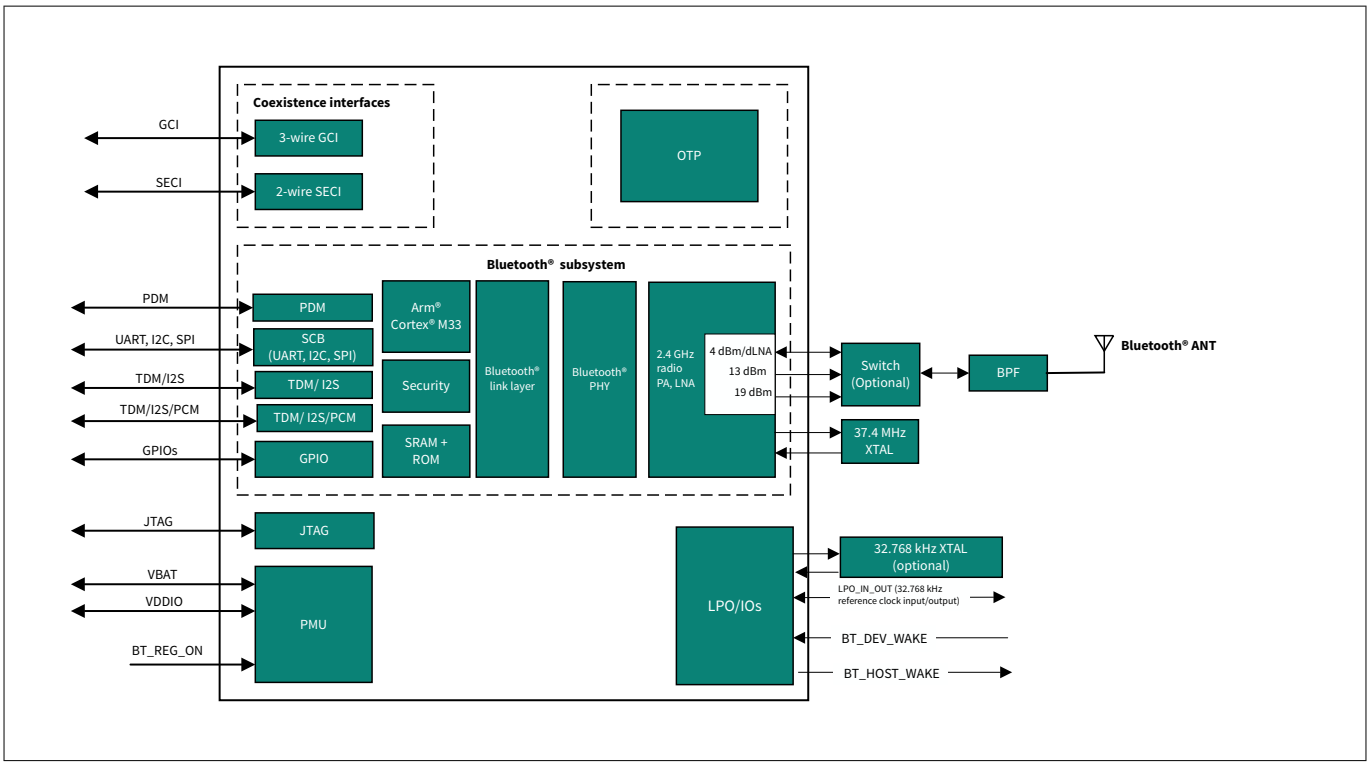


Figure 1 Functional block diagram

Features

- CYW55310 family supports Bluetooth®/Bluetooth® Low Energy (LE)
  - Qualified against Bluetooth® Core 5.0/5.1/5.2/5.3/5.4/6.0/6.1 features
    - LE long range (LR)
    - LE 2 Mbps
    - LE 1 Mbps
  - Advertising
    - Coding selection
  - LE audio:
    - LE audio with LC3 codec on the device (Offload mode)
    - LE audio with LC3 codec on the host (HCI mode)
    - LE isochronous channels
  - Dedicated Bluetooth® LNA for improved RF and coexistence performance (dLNA)
  - +4, +13, and +19 dBm Bluetooth® PA paths optimized for best efficiency, output power options adjustable in 4 dB steps
  - Receive sensitivity: Bluetooth® LE 125 kbps, (LR S = 8), -111 dBm
  - Bluetooth® UART Interface (4-wire)
- Serial Communication Block (SCB)
  - The SCB supports three serial communication protocols: SPI, UART, and I2C. Only one of the protocols is supported by the SCB at any given time
- 7 Channel 12-bit Sigma Delta ADC
  - 16 ksps, 7x DC sensing, 1x analog MIC for NTD
- Audio interfaces
  - Hands-free profile (HFP), Advanced Audio Distribution Profile (A2DP), and LE audio
  - TDM1, TDM2, each supporting I2S (2-channels) and TDM (8-channels), 8k to 96k sample rates and 16-, 24-, and 32-bit sample widths
  - Bidirectional PCM (TDM and I2S) with 8k, 16k sample rates, and 16-bit sample width for HFP. Multiplexed with TDM2
  - Single direction I2S with 44.1k, 48k sample rates and 16-bit sample width for A2DP. Multiplexed with TDM2
- General features
  - VBAT: 3.3 V typical, 3.0 V to 4.8 V operating range
  - VDDIO: 1.8 V typical
  - 0.35 mm pitch WLBGA package
  - Temperature range: -40°C to +85°C
  - External 32.768 kHz low-power oscillator (eLPO) with crystal or reference clock input for low-power consumption[1)]
- Security
  - Life cycle management
  - Crypto key establishment and management
  - Crypto offloads
  - Secure boot
  - Bluetooth® independent firmware authentication

1 External LPO is needed for Bluetooth® Low Energy to support low power mode

Features

  - Firmware encryption
  - Anti-rollback
- Applications
  - Smart watches
  - Smart glasses
  - Augmented reality/virtual reality glasses
  - Smart speakers

Table of contents

Table of contents

Table of contents

1 Overview

The AIROC™ CYW55310 family single-chip device provides the highest level of integration for commercial and consumer systems, with integrated programmable, Bluetooth® + EDR+LE. It provides a small form-factor solution with minimal external components to drive down cost and allows for platform design flexibility in size, form, and function.

1.1 Standards compliance

The AIROC™ CYW55310 family supports the following standards:

- Qualified against Bluetooth® Core 2.1, 3.0, 4.2, 5.0, 5.1, 5.2, 5.3, 5.4, 6.0, 6.1
- Security
  - Hardware accelerator (AES)

2 Power supplies and power management

2.1 Power supply topology

One buck regulator, multiple LDO regulators, and a PMU are integrated into the AIROC™ CYW55310 family. These blocks simplify power supply design for Bluetooth® functions in embedded designs. The CYW55310 family requires two power supplies, VBAT and VDDIO, which are provided with all additional voltages being generated by on-chip regulators.

BT_REG_ON signal is used to power-up the regulators and take the respective core out of reset. The core buck regulator, ABUCK, powers up when BT_REG_ON is asserted. All regulators, buck and LDO, are powered down when BT_REG_ON is deasserted.

The CYW55310 family allows for an extremely low power-consumption mode by completely shutting down ABUCK regulator.

2.2 AIROC™ CYW55310 PMU features

- Analog switching regulator (400 mA)
- BTLDO (400 mA)
- RFLDO (100 mA)
- CLDO (100 mA)

Figure 2 shows the typical power topology for the CYW55310 family. The shaded areas are external to the CYW55310 family.

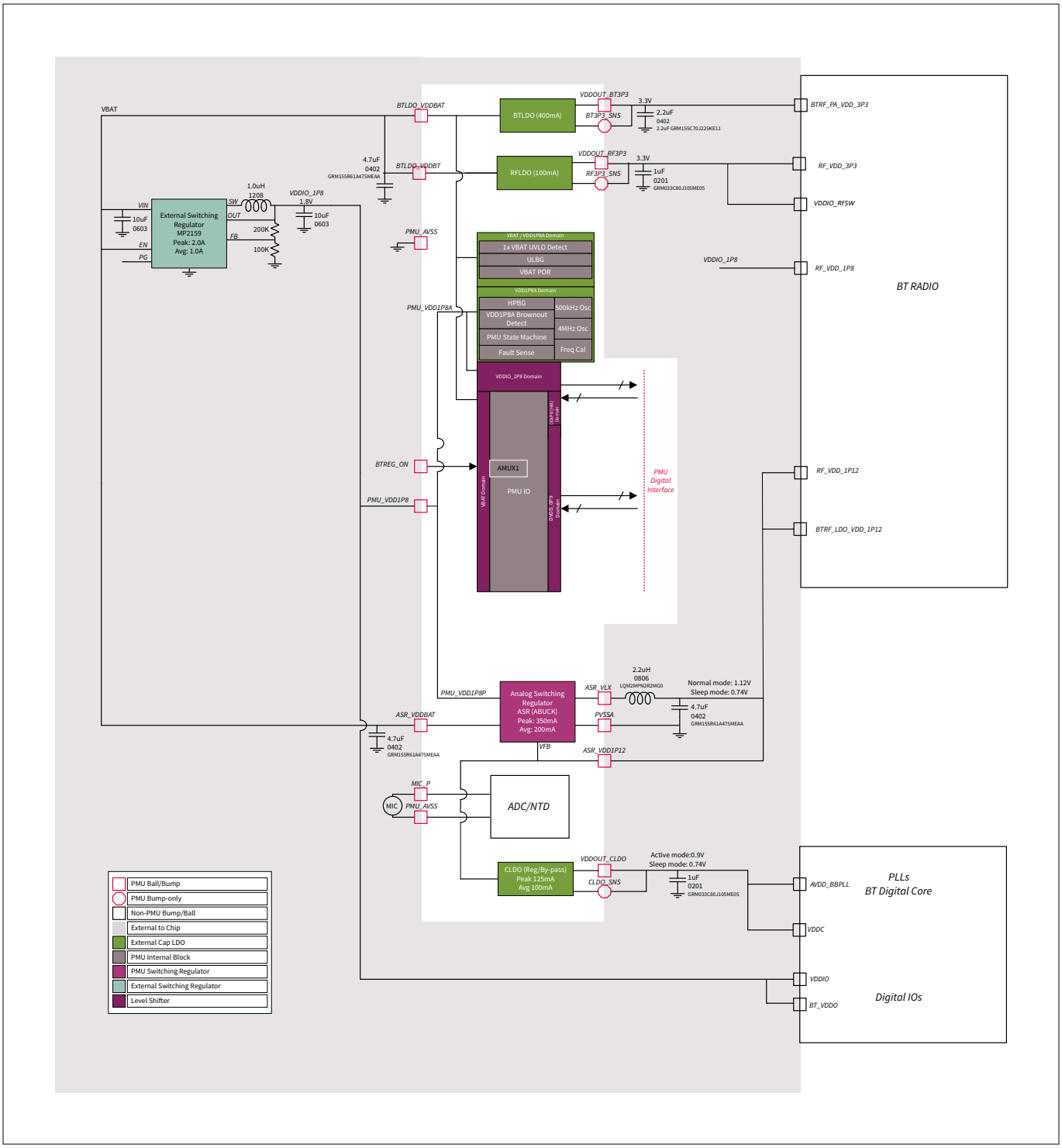


Figure 2 Typical power topology

2.3 PMU sequencing

The PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them.

Configurable, free-running counters (running at 32.768 kHz LPO clock) in the PMU sequencer are used to turn ON/turn OFF individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

2.4 Power-off shutdown

The AIROC™ CYW55310 family provides a low-power shutdown feature that allows the device to be turned OFF while the host and any other devices in the system remain operational. When the CYW55310 family is not needed in the system, VDDIO_RF and VDDC are shut down while VDDIO remains powered. This allows the CYW55310 family to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shutdown state, provided VDDIO remains applied to the CYW55310 family, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system and to enable the CYW55310 family to be fully integrated into an embedded device and take full advantage of the lowest power-saving modes.

When the CYW55310 family is powered ON from this state, it is the same as a normal power-up, and the device does not retain any information about its state from before it was powered down.

2.5 Power-up/power-down/reset circuits

The AIROC™ CYW55310 family has a signal that enable or disable Bluetooth® circuits and internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see Power-up sequence and timing.

Table 1 Power-up/power-down/reset control signals

Signal	Description
BT_REG_ON	This signal is used by the PMU to power up the Bluetooth® core. When this pin is HIGH, the regulators are enabled and the Bluetooth® core is out of reset. When this pin is low, the Bluetooth® core is in reset. If BT_REG_ON is LOW, all the regulators are disabled. This pin has an internal 50 kΩ pull-down resistor that is enabled by default and disabled upon recognizing high on this pin.

3 Frequency references

The AIROC™ CYW55310 family requires two reference frequencies: one is an external 37.4 MHz crystal for the RF section, and another is a 32.768 kHz reference oscillator for low-power operation.

3.1 Crystal interface and clock generation

The CYW55310 family can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Figure 3. See the reference design schematics for the latest configuration.

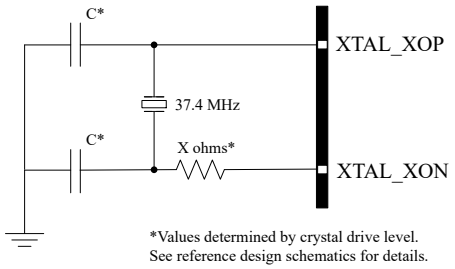


Figure 3 Recommended crystal oscillator configurator

The required default frequency reference is a 37.4 MHz crystal. The signal characteristics for the crystal oscillator interface are listed in Table 2.

Table 2 Crystal oscillator - Requirements and performance

Parameter	Conditions	Crystal[1)]			
		Min.	Typ.	Max	Unit
Frequency	–	–	37.4	–	MHz
Frequency tolerance over the lifetime of the equipment, including temperature[2)]	Without trimming	–20.0	–	20.0	ppm
Crystal load capacitance	–	–	12.0	–	pF
ESR	–	–	–	60.0	Ω
Drive level	External crystal must be able to tolerate this drive level.	200	–	–	µW
Input impedance XTAL_XOP	Resistive	–	–	–	kΩ
	Capacitive	–	–	7.5	pF

1) Use XTAL_XOP and XTAL_XON.
2) It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.

3.2 External frequency reference

As an alternative to a crystal, an external precision frequency reference can be provided. The required default frequency is 37.4 MHz, and it must meet the requirements listed in Table 3. The external frequency reference should be connected to the XTAL_XOP pin through an external 1000 pF coupling capacitor, as shown in Figure 4.

The internal clock buffer connected to this pin will be turned OFF when the AIROC™ CYW55310 family goes into Sleep mode. When the clock buffer turns ON and OFF there will be a small impedance variation. Power must be supplied to the BTRF_LDO_VDD_1P12 pin.

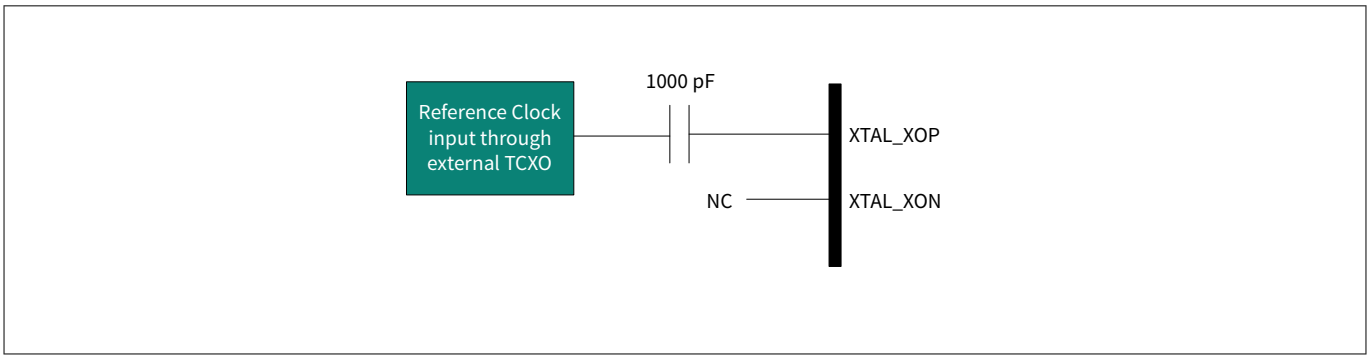


Figure 4 Recommended circuit to use with an external reference clock

Table 3 External clock - Requirements and performance

Parameter	Conditions	External frequency reference			Unit
Frequency	–	–	37.4	–	MHz
Frequency tolerance over the lifetime of the equipment, including temperature[1)]	Without trimming	–20.0	–	20	ppm
Input impedance (XTAL_XOP)	Resistive	30	100	–	kΩ
	Capacitive	–	–	7.5	pF
XTAL_XOP input low level	DC-coupled digital signal	0	–	0.2	V
XTAL_XOP input high level	DC-coupled digital signal	0.8	–	1	V
XTAL_XOP input voltage	AC-coupled analog signal	400	–	1000	mVp-p
Duty cycle	37.4 MHz clock	40	50	60	%

1) It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.

3.3 32.768 kHz low-power oscillator

The CYW55310 family requires a 32.768 kHz reference oscillator for the sleep clock. The possible clock configurations are as below (for low-power):

- External LPO (eLPO) with external crystal connected to LHL_XTALI, LHL_XTALO. In case 32.768 kHz clock source is not from the eLPO with an external crystal, then LHL_XTALI should be connected to GND
- External LPO clock connected to LPO_IN_OUT, digital 32.768 kHz clock input. In case 32.768 kHz clock source is not from the external LPO clock, then LPO_IN_OUT should be connected to GND. This is a free-running clock as long as the BT_REG_ON device is ON
- An external 32.768 kHz precision oscillator that meets the requirements listed in Table 4 must be used

Table 4 External 32.768 kHz sleep clock specifications

Parameter	LPO clock	Unit
Nominal input frequency	32.768	KHz

(table continues...)

3 Frequency references

Table 4 (continued) External 32.768 kHz sleep clock specifications

Parameter	LPO clock	Unit
Frequency accuracy	+/- 250	ppm
Duty cycle	30–70	%
Input signal amplitude	200–1800	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance[1)]	> 100k < 5	Ω pF
Clock jitter[2)] (during initial startup)	< 10,000	ppm

1) When power is applied or switched OFF.
2) The LPO_IN input receiver has ac-coupled capacitance on the input with the feedback resistor to maintain the common mode around VDDIO/2, and power supply noise should be maintained less than 100 mV to avoid any false glitches before the time constant (ac-coupled capacitance * feedback resistor, that is, 100 µs) settles down.

The LPO_OUT feature is primarily used to provide clock input to an external chip if required. On POR, the LPO_IN_OUT pin functions only as an input for eLPO. Software configuration of the pins is needed to enable it as a clock output or as a GPIO. Please note that clock output or GPIO feature can be used only if eLPO is not connected to CYW55310 family and an external 32.768 kHz crystal is available.

Table 5 32 kHz crystal specification

Parameter	Crystal			
	Min.	Typ.	Max.	Unit
Frequency	_	32.768	_	KHz
Frequency tolerance	–20	_	+20	ppm
Crystal load capacitance	_	6.0	_	pF
Equivalent Series Resistance	_	_	90	kΩ
Drive Level	_	0.1	0.5	µW

4 Bluetooth® subsystem overview

The AIROC™ CYW55310 family is a Bluetooth® + EDR-compliant, baseband processor and 2.4-GHz transceiver. It features the highest level of integration and eliminates the need for all critical external components, so minimizing the footprint, power consumption, and system cost of a Bluetooth® solution. The CYW55310 family is the optimal solution for any Bluetooth® voice and/or data application. The Bluetooth® subsystem presents a standard Host Controller Interface (HCI) via a high-speed UART and two TDM interfaces for audio. The CYW55310 family incorporates all Bluetooth® features, including LE-Audio and LE isochronous channels.

The Bluetooth® transmitter also features a power amplifier with programmable Class 1 and Class 2 capabilities with three output paths supporting +4 dBm, +13 dBm, or +19 dBm output power.

4.1 Features

- Supports features of Bluetooth® core specification v6.1:
  - Randomized RPA Updates
- Supports features of Bluetooth® core specification v6.0:
  - Supports ISOAL Enhancements
- Supports features of Bluetooth® core specification v5.4:
  - Advertising code selection for LE coded PHY
- Supports features of Bluetooth® core specification v5.3:
  - LE connection subrating
  - LE channel classification
  - Periodic advertising ADI support
  - Host controller encryption key control enhancements
- Supports features of Bluetooth® core specification v5.2:
  - LE isochronous channels
  - LE power control
  - Enhanced Attribute protocol (eATT)
  - Generic attribute (GATT) Caching
- Supports features of Bluetooth® core specification v5.1:
  - Control protocol data unit (PDU) extension
  - Periodic advertising sync transfer (PAST)
- Supports features of Bluetooth® core specification v5.0:
  - LE 2 Mbps
  - LE long range (LE-LR)
  - LE advertising extension
  - Slot availability masks (SAM)
  - Channel selection algorithm #2
  - High duty cycle non-connectable advertising
- Supports features of Bluetooth® core specification v4.0 + EDR:
  - Adaptive Frequency Hopping (AFH)
  - Quality of Service (QoS)
  - Extended synchronous connections (eSCO)—Voice connections
  - Fast Connect (interlaced page and inquiry scans)
  - Secure simple pairing (SSP)

  - Sniff subrating (SSR)
  - Encryption pause resume (EPR)
  - Extended inquiry response (EIR)
  - Link supervision timeout (LST)
- Supports the mandatory codecs (SBC, CVSD and LC3 for LE audio) and AAC-Decoder
- UART baud rates up to 4 Mbps
- Supports Bluetooth® 4.2, 5.0, 5.1, 5.2, 5.3, 5.4, 6.0, 6.1 packet types
- Supports maximum Bluetooth® data rates over HCI UART
- Multipoint operation with up to seven connections as the central
  - Maximum of seven simultaneous active ACL links
  - Maximum of three simultaneous active SCO and eSCO connections with scatternet support
- Maximum of seven EDR connections as central
- Maximum BLE connections - eight in central and four in peripheral roles simultaneously
- Narrowband and wideband packet loss concealment
- Scatternet operation with up to four active piconets with background scan and support for scatter mode
- High-speed HCI UART transport support with low-power out-of-band BT_DEV_WAKE and BT_HOST_WAKE signaling (see Host controller power management)
- Channel quality driven data rate and packet type selection
- Standard Bluetooth® test modes
- Extended radio and production test mode features
- Full support for power savings modes
  - Bluetooth® clock request
  - Bluetooth® standard sniff
  - Deep Sleep modes and software regulator shutdown

4.2 Bluetooth® radio

CYW55310 family has an integrated radio transceiver that has been optimized for use in 2.4-GHz Bluetooth® wireless frequency band. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4-GHz unlicensed ISM band. It is fully compliant with the Bluetooth® radio specification and EDR specification and meets or exceeds the requirements to provide the highest communication link Quality of service.

4.2.1 Transmit (TX)

The AIROC™ CYW55310 family features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates π/4-DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support EDR. The transmitter is compatible with Bluetooth® Low Energy specification. The transmitter PA can be programmed to provide Bluetooth® Class 1 or Class 2 operation. The device has fully integrated power amplifiers, supporting 3 output power paths: +4 dBm shared with the Bluetooth® dLNA receive path, +13 dBm, and +19 dBm. The +4 dBm output power path only supports BDR, LE1, LE2, LELR modulation schemes.

4.2.2 Digital modulator

The digital modulator performs the data modulation and filtering required for the GFSK, π/4-DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

4.2.3 Digital demodulator and bit synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

4.2.4 Power amplifier (PA)

The fully integrated power amplifier supports Class 1 and Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. For applications in which Bluetooth® is integrated next to a cellular radio, external filtering can be applied to achieve near-thermal noise levels for spurious and radiated noise emissions. The +13 dBm and +19 dBm transmitters features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

4.2.5 Receiver (RX)

The receiver path uses a low-IF scheme to down-convert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology with built-in out-of-band attenuation enables the AIROC™ CYW55310 family to be used in most applications with minimal off-chip filtering. For applications in which the Bluetooth® function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

4.2.6 Digital demodulator and bit synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

4.2.7 Receiver signal strength indicator (RSSI)

The radio portion of CYW55310 provides a receiver signal strength indicator signal to the baseband, so that the controller can take part in a Bluetooth® power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

4.2.8 Local oscillator (LO) generation

TheLO generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels.

The LO generation sub-block employs an architecture for high immunity to LO pulling during PA operation. CYW55310 uses an internal RF and IF loop filter.

4.2.9 Calibration

CYW55310 radio transceiver features an automated calibration scheme that is fully self contained in the radio. No user interaction is required during normal operation or during manufacturing to provide the optimal performance. Calibration optimizes the performance of all the major blocks within the radio to within 2% of

optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation.

Calibration occurs transparently during normal operation during the settling time of the hops and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

5 Bluetooth® Baseband Core (BBC)

The BBC implements all of the time-critical functions required for high-performance Bluetooth® operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth® slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

The following Tx and Rx functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter

5.1 Bluetooth® features

The BBC supports Bluetooth® features, with the following benefits:

- Dual-mode Bluetooth® Low Energy (Bluetooth® & Bluetooth® LE operation)
- Bluetooth® LE -2 Mbps mode, LE-long range mode, advertising extensions, slot availability masks
- TRX scheduler for LE audio
- Extended inquiry response (EIR): Shortens the time to retrieve the device name, specific profile, and operating mode
- Encryption pause resume (EPR): Enables the use of Bluetooth® technology in a much more secure environment
- Sniff subrating (SSR): Optimizes power consumption for low duty cycle asymmetric data flow, which subsequently extends battery life
- Secure simple pairing (SSP): Reduces the number of steps for connecting two devices, with minimal or no user interaction required
- Link supervision time out (LSTO): Additional commands added to HCI and link management protocol (LMP) for improved link timeout supervision
- QoS enhancements: Changes to data traffic control, which results in better link performance. Audio, human interface device (HID), bulk traffic, SCO, and enhanced SCO (eSCO) are improved with the erroneous data (ED) and packet boundary flag (PBF) enhancements

5.2 Test mode support

CYW5531x family fully supports Bluetooth® Test mode as described in the Bluetooth® system specification. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence. In addition to the standard Bluetooth® Test mode, CYW55310 family also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing.

These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin

  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

5.3 Bluetooth® power management unit (PMU)

The Bluetooth® PMU provides power management features that can be invoked by either software through power management registers or packet handling in the baseband core. The power management functions provided by CYW55310 family are:

- RF power management
- Host controller power management
- BBC power management

5.3.1 RF power management

The BBC generates power-down control signals for the TX path, RX path, PLL, and PA to the 2.4-GHz transceiver. The transceiver then processes the power-down functions accordingly.

5.3.2 Host controller power management

When running in UART mode, CYW55310 may be configured so that dedicated signals are used for power management hand-shake between CYW55310 and host. The basic power saving functions supported by those hand-shake signals include the standard Bluetooth® defined Power Savings modes and Standby modes of operation.

Table 6 describes the power-control hand-shake signals used with the UART interface.

Table 6 Power control pin description

Signal	Type	Description
BT_DEV_WAKE	I	Bluetooth® device wake up: Signal from host to CYW55310 indicating that the host requires attention. **Asserted**: The Bluetooth® device must wake-up or remain awake. **Deasserted**: The Bluetooth® device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted HIGH or LOW.
BT_HOST_WAKE	O	Host wake up: Signal from CYW55310 to the host indicating that CYW55310 requires attention. **Asserted**: Host device must wake-up or remain awake. **Deasserted**: Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted HIGH or LOW.

5.3.3 BBC power management

The following are low-power operations for the BBC:

- Physical layer packet-handling turns the RF on and off dynamically within TX/RX packets

- Bluetooth®-specified low-power connection modes: sniff, hold, and park. While in these modes, CYW55310 runs on the low-power oscillator and wakes up after a predefined time period
- A low-power shutdown feature allows the device to be turned OFF while the host and any other devices in the system remain operational

When CYW55310 is not needed in the system, the RF and core supplies are shut down while the I/O remains powered. This allows CYW55310 to effectively be OFF while keeping the I/O pins powered so they do not draw extra current from any other devices connected to the I/O.

During the low-power shut-down state, provided VDDIO remains applied to CYW55310, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system and enables CYW55310 to be fully integrated in an embedded device to take full advantage of the lowest power-saving modes.

Two CYW55310 input signals are designed to be HIGH-Z inputs that do not load the driving signal even if the chip does not have VDDIO power supplied to it: the frequency reference input (XTAL_XOP) and the 32.768 kHz input (LPO_IN_OUT). When CYW55310 is powered ON from this state, it is the same as a normal power-up, and the device does not contain any information about its state from the time before it was powered down.

5.3.4 Wideband speech

CYW55310 provides support for wideband speech (WBS) using on-chip SmartAudio technology. CYW55310 can perform subband codec (SBC), as well as mSBC, encoding and decoding of linear 16 bits at 16 kHz (256 Kbps rate) transferred over the PCM bus.

5.3.5 Packet loss concealment (PLC)

The PLC improves apparent audio quality for systems with marginal link performance. Bluetooth® messages are sent in packets. When a packet is lost, it creates a gap in the received audio bit-stream. Packet loss can be mitigated in several ways:

- Fill in zeros
- Ramp down the output audio signal toward zero (this is the method used in current Bluetooth® headsets)
- Repeat the last frame (or packet) of the received bit-stream and decode it as usual (frame repeat)

These techniques cause distortion and popping in the audio stream. CYW55310 uses a proprietary waveform extension algorithm to provide dramatic improvement in the audio quality. Figure 5 and Figure 6 show audio waveforms without and with PLC. Infineon PLC/BEC algorithms also support wideband speech.

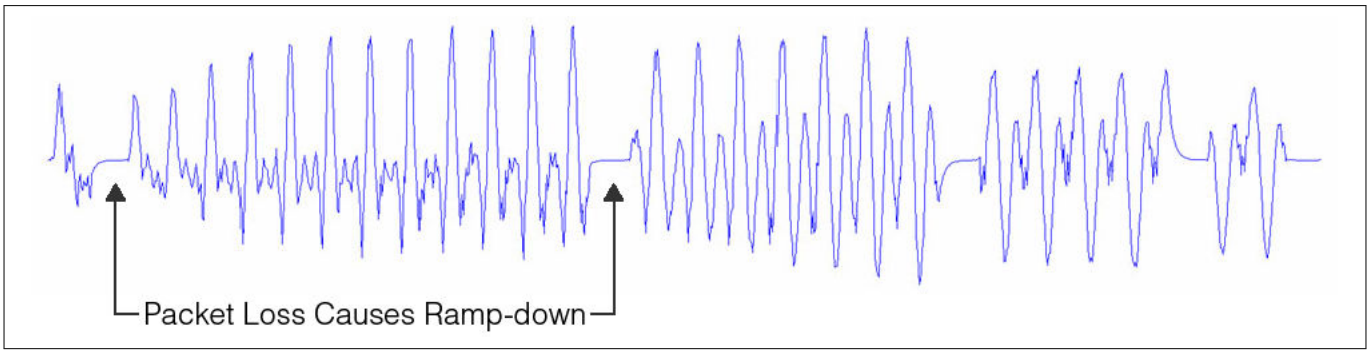


Figure 5 CVSD decoder output waveform without PLC

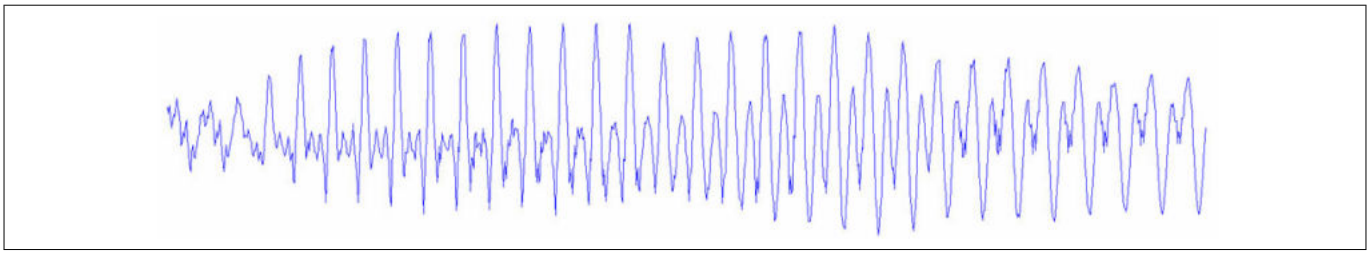


Figure 6 CVSD decoder output waveform after applying PLC

5.3.6 Audio rate-matching algorithms

CYW55310 has an enhanced rate-matching algorithm that uses interpolation algorithms to reduce audio stream jitter that may be present when the rate of audio data coming from the host is not the same as the Bluetooth® data rates.

5.3.7 Codec support

LC3 codec is available for LE Audio and is supported in the ROM in offload mode. CYW55310 can support AAC decoder, SBC for A2DP, and mSBC encoding and decoding for wideband speech.

5.3.8 Multiple simultaneous A2DP audio stream

CYW55310 has the ability to take a single audio stream and output it to multiple Bluetooth® devices simultaneously. This allows a user to share his or her music (or any audio stream) with a friend.

5.3.9 Burst buffer operation

CYW55310 has a data buffer that can buffer data being sent over the HCI and audio transports, then send the data at an increased rate. This mode of operation allows the host to sleep for the maximum amount of time, dramatically reducing system current consumption.

5.4 Adaptive frequency hopping

CYW55310 gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency-hop map.

5.5 Fast connection (interlaced page and inquiry scans)

CYW55310 supports page scan and inquiry scan modes that significantly reduce the average inquiry response and connection times. These scanning modes are compatible with the Bluetooth® v2.1 page and inquiry procedures.

6 Microprocessor and memory unit for Bluetooth®

The Bluetooth® microprocessor core is based on the Arm® Cortex®-M33 with UART for firmware loading and JTAG interface unit for debugging. The Arm® core is paired with a memory unit that contains 2 MB of ROM memory for program storage and boot ROM, and 768 KB of RAM for data scratch-pad and patch RAM code. At power-up, the lower-layer protocol stack is executed from the internal ROM memory. External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or features additions. These patches may be downloaded from the host to CYW55310 through the UART transports or shared SDIO transports.

6.1 RAM, ROM, and patch memory

CYW55310 Bluetooth® core has 768 KB of internal RAM which is mapped between general purpose scratch pad memory and patch memory and 2 MB of ROM used for the lower-layer protocol stack, test mode software, and boot ROM. The patch memory capability enables the addition of code changes for purposes of feature additions and bug fixes to the ROM memory.

6.2 Reset

CYW55310 has an integrated power-on reset (POR) circuit that resets all circuits to a known power-on state. The Bluetooth® POR circuit is out of reset after BT_REG_ON goes HIGH. If BT_REG_ON is LOW, then the POR circuit is held in reset.

7 Bluetooth® peripheral transport units

7.1 Media transports

The AIROC™ CYW55310 family supports HFP, A2DP, and LE audio with optimized I2S, TDM, and PCM transports for Bluetooth® audio. LC3 codec controllers are used in offline mode.

7.1.1 TDM

- A pair of TDM interfaces (TDM1, TDM2) are available, and each TDMx (TX, RX) consists of a TDM transmitter and a TDM receiver
- The transmitter and receiver can function simultaneously and have a dedicated clock control
- The transmitter and receiver have a dedicated FIFO interrupt and FIFO trigger
- Both transmitter and receiver support master and slave functionality
- TDM features
  - Supports I2S and TDM/PCM functionality
  - Full-duplex transmitter and receiver operation
  - Supports up to eight channels. Each channel can be individually enabled/disabled
  - Programmable Interface clock
  - Programmable half-cycle delayed sampling support
  - Programmable late capture extra delay of 1, 2, or 3 cycles, for multi-cycle round-trip latencies in receiver master mode
  - Programmable PCM sample formatting (8, 10, 12, 14, 16, 18, 20, 24, 32 bits)
  - Supports all common sampling frequencies: 4/8/11.025/12/16/20/22.05/24/30/32/40/44.1/48/60/96 kHz
  - 8-channel (each 32-bit) TDM can operate at a maximum data rate of 48 kHz for Tx and Rx
  - Programmable synchronization pulse type
  - Left-aligned and right-aligned sample formatting
  - Test mode (transmitter to receiver loopback)

7.1.1.1 Operating modes

TDM tx/rx has two possible configurations: Master and Slave. Masters output the TDM clock and Frame sync, and slaves on the other hand take the same signals as inputs.

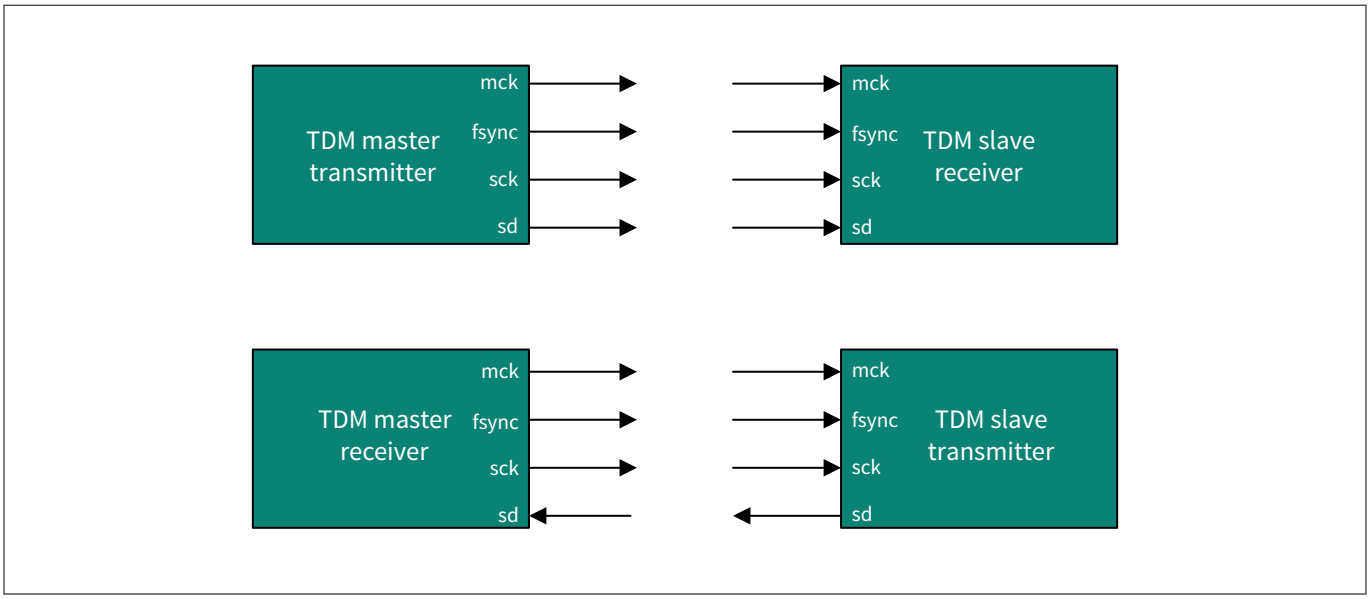


Figure 7 Operating modes

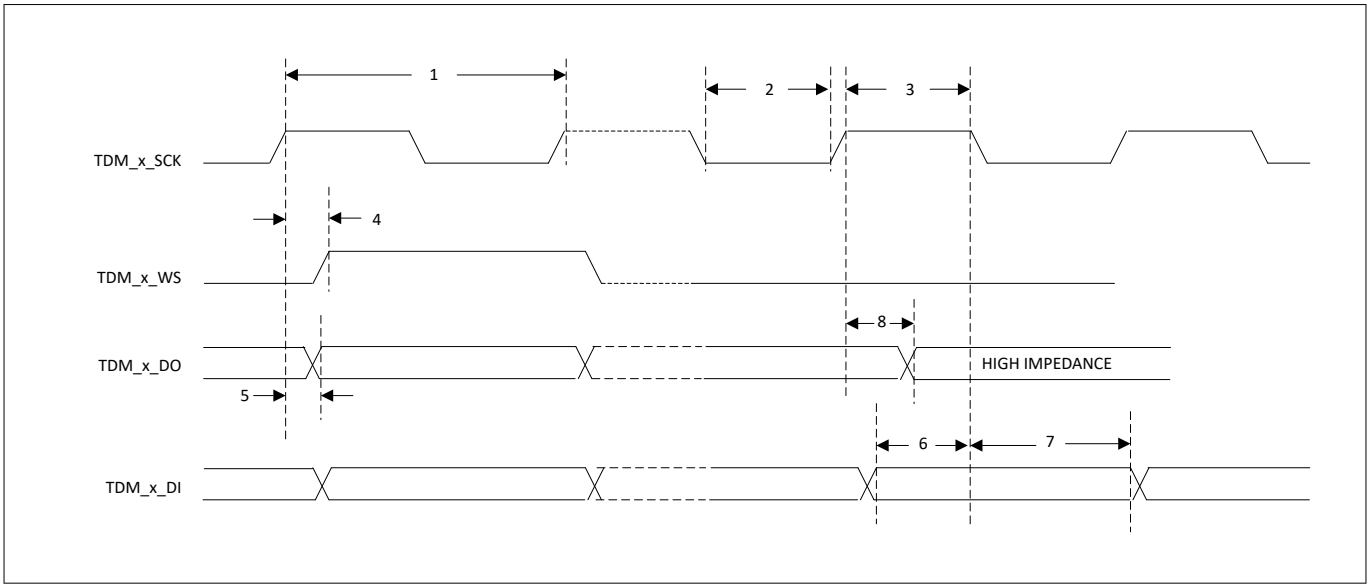


Figure 8 TDM interface timing (Short frame sync, master mode)

Table 7 TDM interface timing specifications (short frame sync, master mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	TDM bit clock frequency	–	–	12.0	MHz
2	TDM bit clock LOW	41.0	–	–	ns
3	TDM bit clock HIGH	41.0	–	–	ns
4	TDM SYNC delay	0	–	25.0	ns
5	TDM_OUT delay	0	–	25.0	ns
6	TDM IN setup	8.0	–	–	ns
7	TDM IN hold	8.0	–	–	ns

(table continues...)

Table 7 (continued) TDM interface timing specifications (short frame sync, master mode)

Reference	Characteristics	Min	Typ	Max	Unit
8	Delay from the rising edge of TDM_CLK during the last bit period to TDM_OUT becoming HIGH-Z	0	–	25.0	ns

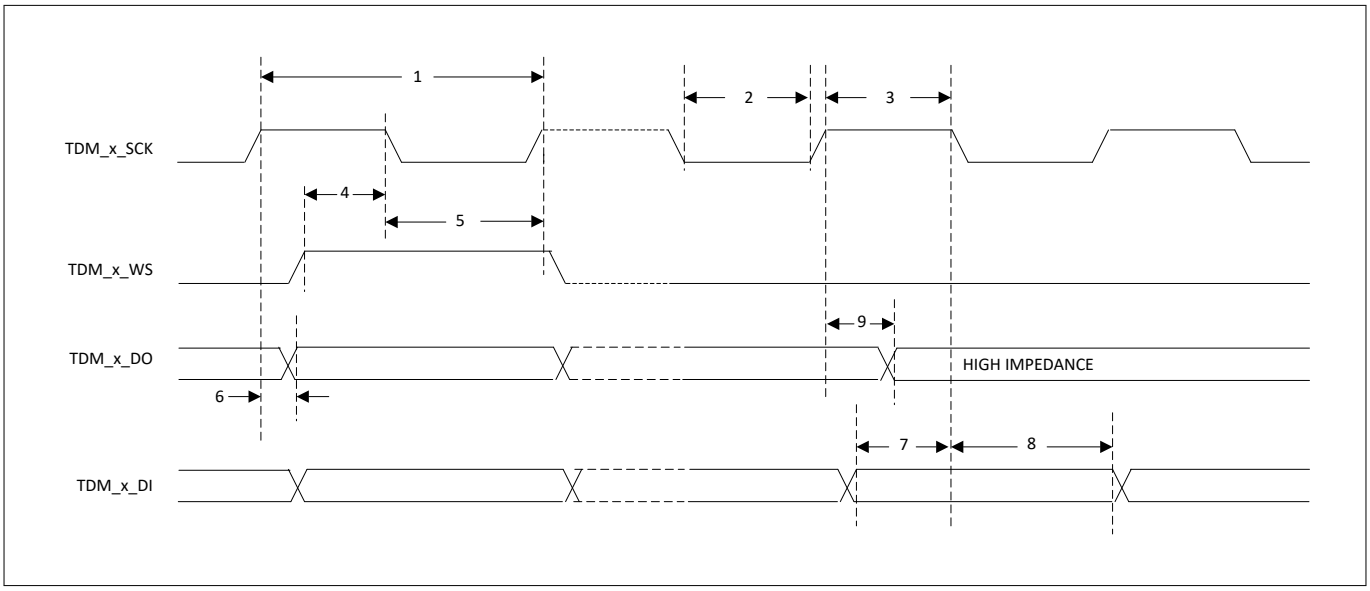


Figure 9 TDM interface timing (Short frame sync, slave mode)

Table 8 TDM interface timing specifications (short frame sync, slave mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	TDM bit clock frequency	–	–	12.0	MHz
2	TDM bit clock LOW	41.0	–	–	ns
3	TDM bit clock HIGH	41.0	–	–	ns
4	TDM_SYNC setup	8.0	–	–	ns
5	TDM_SYNC hold	8.0	–	–	ns
6	TDM_OUT delay	0	–	25.0	ns
7	TDM_IN setup	8.0	–	–	ns
8	TDM_IN hold	8.0	–	–	ns
9	Delay from the rising edge of TDM_CLK during the last bit period to TDM_OUT becoming HIGH-Z	0	–	25.0	ns

7.1.2 HFP codec interface controller

- Supported by PCM and I2S transports and bidirectional operations
- PCM
  - Sample rates 8k for NBS and 16k for wideband speech (WBS) supported
  - Dual stream use cases can concurrently use Narrowband speech (NBS) and WBS
  - Sample width is limited to 16 bits

  - Synchronization clock width of 1 or 3 (short or long)
  - Bit clocks of 128k, 256k, 512k, 1024k and 2024k, the only difference being the number of 16-bit slots
  - HFP samples can be taken from any available slot. Slot 0 is the default slot
- I2S
  - Supports bit clocks of 256k (NBS) and 512K (WBS)
  - HFP samples can be taken from either left or right. Left is the default

7.1.3 A2DP codec controller

- Supported by I2S transport in a single direction, either in or out but not both
- Two channels, left and right. Mono is not supported
- Sample rates: 44.1k or 48k
- Sample width is limited to 16 bits
- Supports bit clocks of 32 times the sample rate, 1411200 (44.1k) or 1536000 (48k), and is not adjustable

7.1.4 PCM interface

CYW55310 has two TDM interfaces that support I2S/TDM/PCM protocols independently. The PCM interface on CYW55310 can connect to linear PCM codec devices in master/Slave mode. In Master mode, CYW55310 generates the BT_PCM_CLK and BT_PCM_SYNC signals, and in Slave mode, these signals are provided by another master on the PCM interface and are inputs to CYW55310.

The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

7.1.4.1 Slot mapping

CYW55310 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8- kHz or 16-kHz audio sample interval is divided into as many as sixteen slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. The transmit and receive PCM data from a SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

7.1.4.2 Frame synchronization

CYW55310 supports both short and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a HIGH on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

7.1.4.3 Data formatting

CYW55310 may be configured to generate and accept several different data formats. For a conventional Narrowband Speech mode, CYW55310 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are

ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked most significant bit (MSb) first.

7.1.4.4 Wideband speech support

When the host encodes WBS packets in Transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in Master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 Kbps bit rate. CYW55310 also supports slave Transparent mode using a proprietary rate-matching scheme. In SBC mode, linear 16-bit data at 16 kHz (256 Kbps rate) is transferred over the PCM bus.

7.1.5 PDM

CYW55310 supports digital PDM microphone interface and provides support for 512 kHz, 1 MHz, and 2 MHz microphone clock. Internally, the PDM samples are captured and converted to 16 bit PCM samples. The PDM to PCM conversion block supports both 16 kHz and 8 kHz data rates. CYW55310 supports the following digital mic configurations.

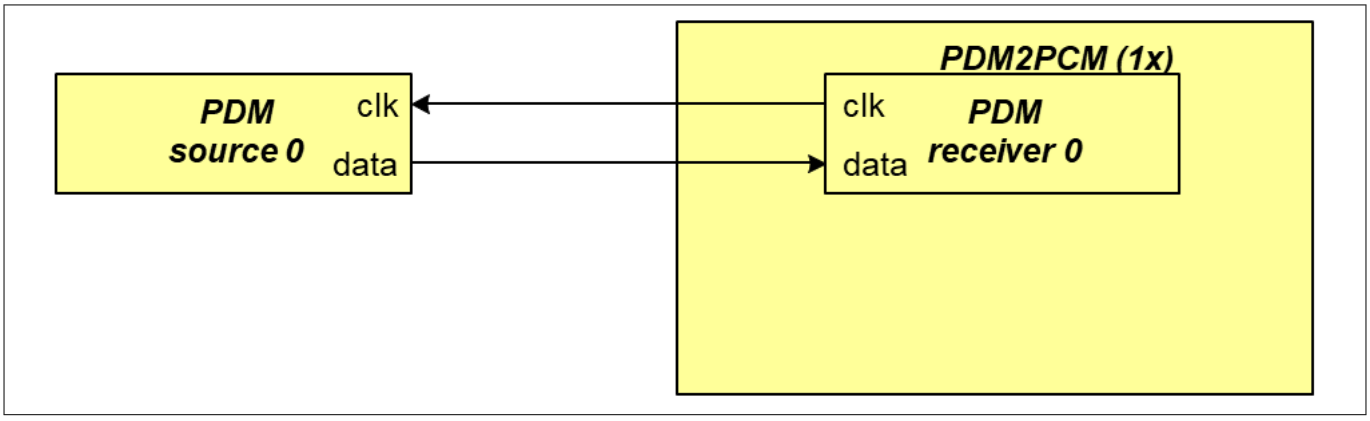


Figure 10 Single mono configuration

A pair of microphones, but only one mic is selectable at a time internally.

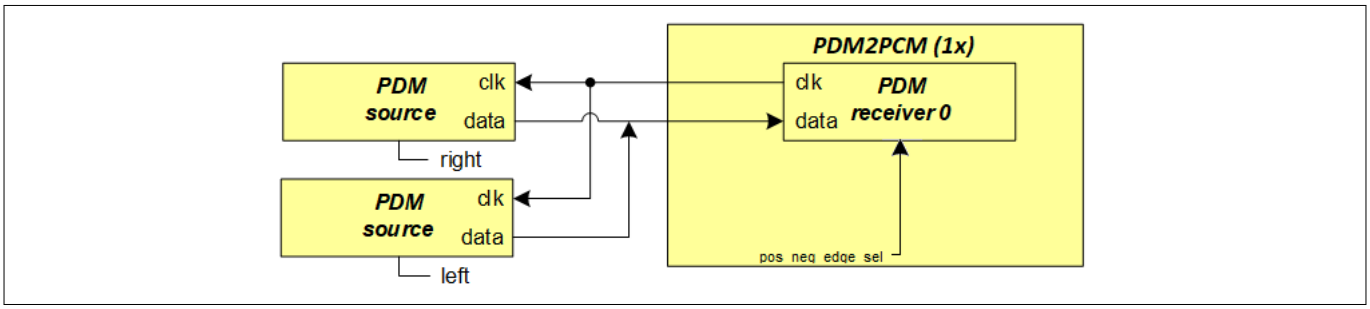


Figure 11 Selectable mono (L or R) (Shared data line)

7.2 UART interface

The CYW55310 UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps.

The baud rate may be selected through a vendor-specific UART HCI command. The UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA/CPU. The UART supports the Bluetooth® HCI UART specification. The default baud rate is 115.2 Kbaud. CYW55310 UART can perform XON/XOFF flow control and includes hardware support for the

Serial Line Input Protocol (SLIP). Normally, the UART baud rate is set by a configuration record downloaded after device reset and the host does not need to adjust the baud rate. Supports in changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the BaudRate registers. CYW55310 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Table 9 Example of common baud rates

Desired rate	Actual rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

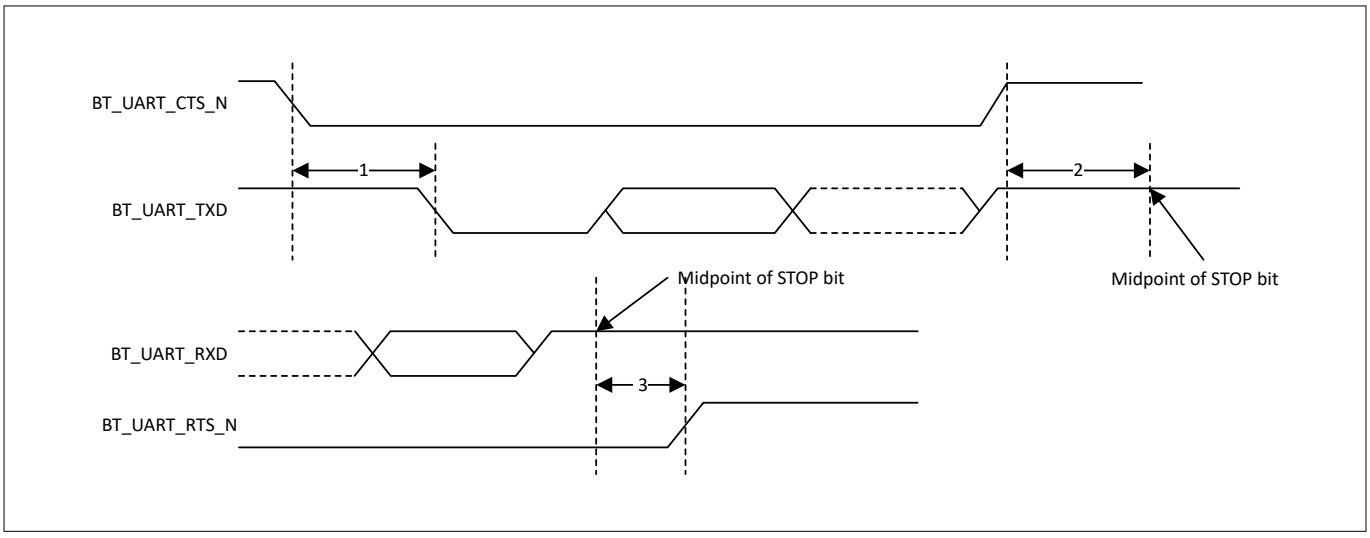


Figure 12 UART timing

Table 10 UART timing specification

Reference	Characteristics	Min	Typ	Max	Unit
1	Delay time, BT_UART_CTS_N LOW to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N HIGH before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N HIGH	–	–	0.5	Bit periods

7.3 ADC and low-power comparator

CYW55310 consists of two low-power comparators (LPCOMP), and a 7-channel 12-bit ΔΣ ADC to provide sensing and monitoring of input signals connected to the GPIO and connection of a single-ended analog microphone. The LPCOMPs and ADC each has its own control signals to allow measurement configuration flexibilities and power saving when not in use. The ADC and LPCOMP are powered by a single supply voltage of 1.8 V.

The following are the general features for ADC:

- Third order 1-bit continuous-time ΔΣ
- Output sampling rate 16 ksps
- MIC bias reference at 1.8 V
- MIC PGA gain range 0-18 dB (eight linear steps)

LPCOMP features a programmable noise threshold in 16 linear steps. The system supports two modes of operations:

- DC mode
- Noise threshold detection (NTD) mode

In DC mode, DC input signals are routed through the 7-GPIO pins. This mode can be used for sampling sensors like thermistors and so on.

In NTD mode, the audio signal is routed from the analog microphone to the microphone input through an AC coupling capacitor.

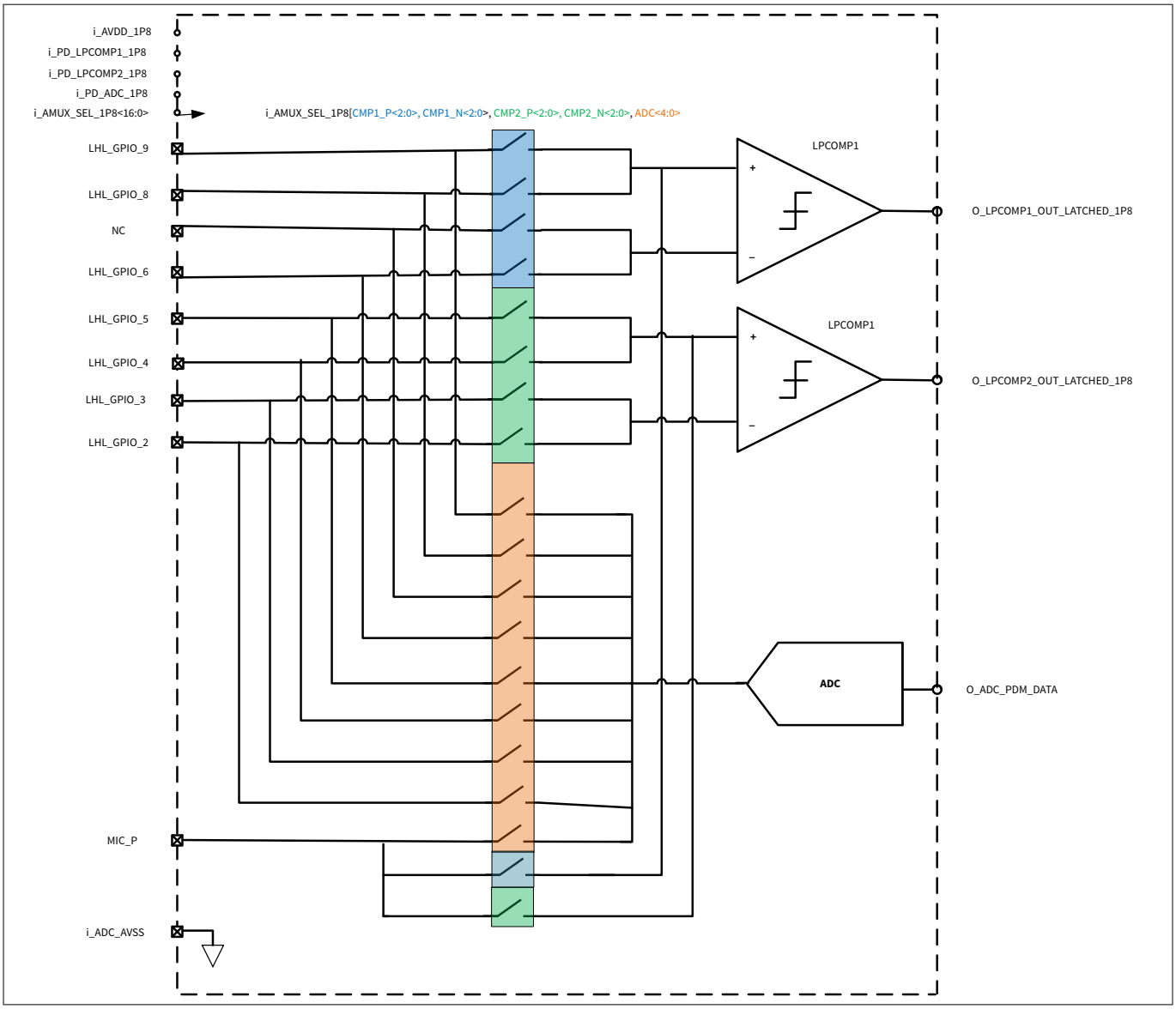


Figure 13 ADC block diagram

Table 11 ADC block diagram pin description

Pin name	I/O	Description
i_AVDD_1P8	I	System 1.8 V supply from an external SR
I_ADC_AVSS	I	Low-impedance direct ground reference to ADC
i_PD_LPCOMP1_1P8	I	Default: 1. LPCOMP1 power up/down controlled by 1.8 V power up/down signal: 0: LPCOMP1 is powered up 1: LPCOMP1 is powered down (default)

(table continues...)

Table 11 (continued) ADC block diagram pin description

Pin name	I/O	Description
i_PD_LPCOMP2_1P8	I	Default: 1. LPCOMP2 power up/down controlled by 1.8 V power up/down signal: 0: LPCOMP2 is powered up 1: LPCOMP2 is powered down (default)
i_PD_ADC_1P8	I	Default: 1. ADC power up/down controlled by 1.8 V power up/down signal: 0: ADC is powered up 1: ADC is powered down (default)
i_AMUX_SEL_1P8<16:0>	I	Multiplexer configuration (see mapping in Table 12)
LHL_GPIO_<9:2>	I	GPIO inputs for DC input signals
i_MIC	I	AC input signal from analog microphone or AC source, Rin = 375 kΩ
o_LPCOMPn_OUT_LATCHED_1P8 (n = 1,2)	O	Latched LPCOMPn output (1.8 V) when noise above threshold is detected
o_ ADC_PDM_DATA	O	ADC PDM bitstream

Table 12 Multiplexer register configuration mapping

	Value	MUX input	MUX output
i_AMUX_SEL_1P8<16:0>	-	-	-
CMP1_P<2:0>	000	LHL_GPIO_<8>	LPCOMP1_P
	001	LHL_GPIO_<9>	LPCOMP1_P
	01x	i_MIC	LPCOMP1_P
	1xx	OPEN	LPCOMP1_P
CMP1_N<2:0>	000	LHL_GPIO_<6>	LPCOMP1_N
	001	LHL_GPIO_<7>[1)]	LPCOMP1_N
	-	OPEN	LPCOMP1_N
	1xx	OPEN	LPCOMP1_N
CMP2_P<2:0>	000	LHL_GPIO_<4>	LPCOMP2_P
	001	LHL_GPIO_<5>	LPCOMP2_P
	01x	PDM_DMIC	LPCOMP2_P
	1xx	OPEN	LPCOMP2_P
CMP2_N<2:0>	000	LHL_GPIO_<2>	LPCOMP2_N
	001	LHL_GPIO_<3>	LPCOMP2_N

(table continues...)

Table 12 (continued) Multiplexer register configuration mapping

	Value	MUX input	MUX output
	01x	OPEN	LPCOMP2_N
	1xx	OPEN	LPCOMP2_N
ADC<4:0>	00000	LHL_GPIO_<2>	ADC
	00001	LHL_GPIO_<3>	ADC
	00010	LHL_GPIO_<4>	ADC
	00011	LHL_GPIO_<5>	ADC
	00100	LHL_GPIO_<6>	ADC
	00101	LHL_GPIO_<7>[1)]	ADC
	00110	LHL_GPIO<8>	ADC
	00111	LHL_GPIO_<9>	ADC
	01xxx	PDM_DMIC	ADC
	1xxxx	OPEN	ADC

1) LHL_GPIO7 is reserved as not available for user, making the total available channels to seven.

8 Pinout and signal descriptions

8.1 CYW55310 WLBGA package ball map

	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
10	RSVD	RF_GND	RF_GND	RF_VDD_1P12	RF_GND	NC7	RFSW_CTRL7	VDDIO_RFSW	GPIO_0	GPIO_4	VDDOUT_RF3P3	BTLDO_VDDBT	BTLDO_VDDBAT	ASR_VDDBAT	ASR_VLX	10
9	RSVD	RF_GND	BTRF_GPAIO				RFSW_CTRL6	VSSC	GPIO_2	GPIO_6	PMU_VDD1P8	NC10	VDDOUT_BT3P3	VDDOUT_CLDO	PVSSA	9
8	RF_GND	NC11	RF_GND	RF_VDD_3P3	RF_GND	NC8	RFSW_CTRL5	VDDC	GPIO_3	GPIO_5	MIC_P	PMU_AVSS	BTREG_ON	ASR_VDD1P12	VSSC	8
7	RSVD	RF_GND	RF_GND	RF_VDD_3P3	RF_VDD_1P12	RFSW_CTRL4	LHL_XTALI	LHL_XTALO	BT_UART_RTS_N	BT_UART_TXD	VSSC	BT_GPIO_5	NC	NC	NC	7
6	RSVD	RF_GND	NC6	RF_GND	RF_VDD_1P12	RFSW_CTRL3	VDDC	LHL_GPIO_2	BT_UART_RXD	BT_UART_CTS_N	BT_GPIO_6	VDDIO	NC	NC	NC	6
5	BTRF_RF_OP	BTRF_VSS	BTRF_IF_VSS	RF_VDD_1P8	RF_GND	RFSW_CTRL2	LPO_IN_OUT	LHL_GPIO_3	AVDD_BBPLL	BT_GPIO_4	BT_GPIO_3	VDDC	SMIF_SPHB_DQ3	SMIF_SPHB_DQ2	SMIF_SPHB_CK	5
4	BTRF_VSS	BTRF_TEST	BTRF_PLL_VSS	BTRF_RX_DVSS	RFSW_CTRL1	RFSW_CTRL0	VSSC	LHL_GPIO_4	VSSC	BT_VDDO	BT_GPIO_2	TDM1_DI	SMIF_SPHB_CS0_N	SMIF_SPHB_DQ1	SMIF_SPHB_DQ0	4
3	BTRF_13DBM_OP	BTRF_VCO_VSS		BTRF_LDO_VDD_1P12		JTAG_SEL	BT_DEV_WAKE	LHL_GPIO_5	SMIF_SPHB_CS1_N	TDM1_DO	TDM1_SCK	TDM1_WS	BT_GPIO_17	BT_GPIO_16	BT_GPIO_7	3
2		BTRF_PA_VSS	BTRF_TX_VSS	BTRF_TX_DVSS	XTAL_GND	VDD_XTAL	VSSC	VDDC	LHL_GPIO_8	BT_HOST_WAKE	TDM1_MCK	TDM2_DI	VSSC	VDDC	TDM2_WS	2
1	BTRF_20DBM_OP	BTRF_PA_VSS	BTRF_PA_VDD_3P3	BTRF_TXIF_VSS	XTAL_XON	XTAL_XOP		LHL_GPIO_9	LHL_GPIO_6	BT_GPIO_0	DMIC_DQ	DMIC_CK	TDM2_DO	TDM2_MCK	TDM2_SCK	1
	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

Figure 14 WLBGA package ball map

8.2 WLBGA package signal descriptions

Table 13 WLBGA signal description

Ball #	Ball name	Type	Description
R10[1)]	RSVD	–	No Connect
R9 [1)]	RSVD	–	No Connect
R8	RF_GND	GND	RF Ground
R7[1)]	RSVD	–	No Connect
R6 [1)]	RSVD	–	No Connect
P10	RF_GND	GND	RF Ground
P9	RF_GND	GND	RF Ground
P8	NC11	_	No Connect
P7	RF_GND	GND	RF Ground
P6	RF_GND	GND	RF Ground
N10	RF_GND	GND	RF Ground
N9	BTRF_GPAIO	–	BT Radio GPAIO
N8	RF_GND	GND	RF Ground
N6	NC6[2)]	–	No Connect
M10	RF_VDD_1P12	PWR	Radio 1.12 V supply
M8	RF_VDD_3P3	PWR	Radio 3.3 V supply

(table continues...)

Table 13 (continued) WLBGA signal description

Ball #	Ball name	Type	Description
M7	RF_VDD_3P3	PWR	Radio 3.3 V supply
M6	RF_GND	GND	RF Ground
M5	RF_VDD_1P8	PWR	Radio 1.8 V supply
L10	RF_GND	GND	RF Ground
L8	RF_GND	GND	RF Ground
L7	RF_VDD_1P12	PWR	Radio 1.12 V supply
L6	RF_VDD_1P12	PWR	Radio 1.12 V supply
L5	RF_GND	GND	RF Ground
K2	VDD_XTAL	PWR	Xtal oscillator 1.0 V supply
K1	XTAL_XOP	I	Xtal oscillator Input
J7	LHL_XTALI	I	32.768 kHz crystal oscillator input
L2	XTAL_GND	GND	Xtal oscillator ground
L1	XTAL_XON	O	Xtal oscillator output
H7	LHL_XTALO	O	32.768 kHz crystal oscillator output
R5	BTRF_RF_OP	O	Low Power TX output/dLNA RX input
R4	BTRF_VSS	GND	Bluetooth® Radio ground
R3	BTRF_13DBM_OP	O	Bluetooth® Radio (13 dBm) output
R1	BTRF_20DBM_OP	O	Bluetooth® Radio (20 dBm) output
P5	BTRF_VSS	GND	Bluetooth® Radio ground
P4	BTRF_TEST	I/O	Bluetooth® Radio test input/output pin
P3	BTRF_VCO_VSS	GND	Bluetooth® Radio VCO Ground
P2	BTRF_PA_VSS	GND	Bluetooth® Radio PA Ground
P1	BTRF_PA_VSS	GND	Bluetooth® Radio PA Ground
N5	BTRF_IF_VSS	GND	Bluetooth® Radio IF Ground
N4	BTRF_PLL_VSS	GND	Bluetooth® Radio PLL Ground
N2	BTRF_TX_VSS	GND	Bluetooth® Radio TX Ground
N1	BTRF_PA_VDD_3P3	PWR	Bluetooth® Radio PA 3.3 V supply
M4	BTRF_RX_DVSS	GND	Bluetooth® Radio RX Ground
M3	BTRF_LDO_VDD_1P12	PWR	Bluetooth® Radio 1.12 V supply
M2	BTRF_TX_DVSS	GND	Bluetooth® Radio TX Ground
M1	BTRF_TXIF_VSS	GND	Bluetooth® Radio TX IF Ground

(table continues...)

Table 13 (continued) WLBGA signal description

Ball #	Ball name	Type	Description
C8	BTREG_ON	I	Used by the PMU to power up or power down the internal CYW8x310 regulators used by the Bluetooth® section. When deasserted, this pin holds the Bluetooth® section in reset. This pin has an internal 50 kΩ pull-down resistor that is auto enabled/disabled by programming.
G7	BT_UART_RTS_N	O	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. Bluetooth® LED control pin.
G6	BT_UART_RXD	I	UART serial input. Serial data input for the HCI UART interface.
F7	BT_UART_TXD	O	UART serial output. Serial data output for the HCI UART interface.
F6	BT_UART_CTS_N	I	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
F4	BT_VDDO	PWR	1.8-V IO supply for Bluetooth® GPIOs
F3	TDM1_DO	I/O	Bluetooth® TDM1 Interface Data Out
F2	BT_HOST_WAKE	I/O	Bluetooth® HOST WAKE
L4	RFSW_CTRL1	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
K7	RFSW_CTRL4	O	
K6	RFSW_CTRL3	O	
K5	RFSW_CTRL2	O	
K4	RFSW_CTRL0	O	
J10	RFSW_CTRL7	O	
J9	RFSW_CTRL6	O	
J8	RFSW_CTRL5	O	
F5	BT_GPIO_4	I/O	Bluetooth® general purpose I/O
A3	BT_GPIO_7	I/O	
E6	BT_GPIO_6	I/O	
E5	BT_GPIO_3	I/O	
E4	BT_GPIO_2	I/O	
F1	BT_GPIO_0	I/O	
D7	BT_GPIO_5	I/O	
C3	BT_GPIO_17	I/O	
B3	BT_GPIO_16	I/O	
H6	LHL_GPIO_2	I/O	Miscellaneous general purpose I/O
H5	LHL_GPIO_3	I/O	
H4	LHL_GPIO_4	I/O	

(table continues...)

Table 13 (continued) WLBGA signal description

Ball #	Ball name	Type	Description
H3	LHL_GPIO_5	I/O	
G3	SMIF_SPHB_CS1_N	I/O	Serial memory interface chip select1
G2	LHL_GPIO_8	I/O	Miscellaneous general purpose I/O
G1	LHL_GPIO_6	I/O	
H1	LHL_GPIO_9	I/O	
G10	GPIO_0	I/O	–
G9	GPIO_2	I/O	
G8	GPIO_3	I/O	
F10	GPIO_4	I/O	
F9	GPIO_6	I/O	
F8	GPIO_5	I/O	
C7	NC	–	No Connect
C6	NC	–	
B7	NC	–	
B6	NC	–	
A7	NC	–	
A6	NC	–	
A2	TDM2_WS	I/O	TDM2 Interface Word Select
A1	TDM2_SCK	I/O	TDM2 Interface Slave Clock
E3	TDM1_SCK	I/O	TDM1 Interface Slave Clock
E2	TDM1_MCK	I/O	TDM1 Interface Master Clock
D4	TDM1_DI	I/O	TDM1 Interface Data In
D3	TDM1_WS	I/O	TDM1 Interface WordSelect
D2	TDM2_DI	I/O	TDM2 Interface Data In
C1	TDM2_DO	I/O	TDM2 Interface Data Out
B1	TDM2_MCK	I/O	TDM2 Interface Master Clock
C5	SMIF_SPHB_DQ3	I/O	Serial memory interface data line3
B5	SMIF_SPHB_DQ2	I/O	Serial memory interface data line2
B4	SMIF_SPHB_DQ1	I/O	Serial memory interface data line1
A4	SMIF_SPHB_DQ0	I/O	Serial memory interface data line0
C4	SMIF_SPHB_CS0_N	O	Serial memory interface chip select0
A5	SMIF_SPHB_CK	O	Serial memory interface clock
K10	NC7	–	No Connect

(table continues...)

Table 13 (continued) WLBGA signal description

Ball #	Ball name	Type	Description
K8	NC8	–	
D6	VDDIO	PWR	1.8 V IO supply for GPIOs
H8	VDDC	PWR	0.9 V digital core supply
H2	VDDC	PWR	
D5	VDDC	PWR	
C10	BTLDO_VDDBAT	PWR	Battery supply Input for Bluetooth® PA LDO
C9	VDDOUT_BT3P3	PWR	3.3 V output to supply Bluetooth® PA
B10	ASR_VDDBAT	PWR	Battery supply input for ASR power stage
B9	VDDOUT_CLDO	O	Output of CLDO
B8	ASR_VDD1P12	I	Sense or feedback input of ASR power stage
D10	BTLDO_VDDBT	PWR	Battery supply input for RF LDO
D9	NC10	–	No Connect
D8	PMU_AVSS	GND	PMU analog ground
A10	ASR_VLX	O	ASR power stage output to inductor
A9	PVSSA	GND	Ground input of ASR power stage
B2	VDDC	PWR	0.9 V digital core supply
K3	JTAG_SEL	I	JTAG select input: Pull high to select the JTAG interface. If the JTAG interface is not used this pin should be connected to ground.
J6	VDDC	PWR	0.9 V Digital Core supply
J5	LPO_IN_OUT	I/O	Based on configuration it can be either **1.** As an external 32 KHz clock source input **2.** As a 32 KHz Clock output if XTAL is connected (XTAL_IN, XTAL_OUT). **3.** LHL_GPIO_10 similar to other LHL GPIOs
J4	VSSC	GND	Core Ground for Bluetooth®
J3	BT_DEV_WAKE	I/O	Bluetooth® DEVICE WAKE
J2	VSSC	GND	Core Ground
H10	VDDIO_RFSW	PWR	IO supply for RF switch control pads
H9	VSSC	GND	Core Ground for Bluetooth®
G4	VSSC	GND	Core Ground for Bluetooth®
E7	VSSC	GND	Core Ground for Bluetooth®
C2	VSSC	GND	Core Ground for Bluetooth®
G5	AVDD_BBPLL	PWR	Baseband PLL 0.9 V supply
E10	VDDOUT_RF3P3	PWR	Radio 3.3V supply

(table continues...)

Table 13 (continued) WLBGA signal description

Ball #	Ball name	Type	Description
E9	PMU_VDD1P8	PWR	1.8 V PMU supply input
E8	MIC_P	I	ADC microphone positive input
E1	DMIC_DQ	I/O	Digital mic data
D1	DMIC_CK	I/O	Digital mic clock

1) Need to be terminated in 50 Ω.
2) Do not route under these balls.

8.3 Bluetooth® GPIO signals and strapping options

Table 14 GPIO strap pins

Pad name	Default pull during strapping	All packages
sdiod_data[2]	1	1=SDIOD, 0 = gSPI

8.4 GPIO alternative signal functions

Table 15 GPIO alternate signal functions

Pad name	Function sel									
	Function# 0	**Function# 1**	**Function# 2**	**Function# 3**	**Function# 4**	**Function# 5**	**Function# 6**	**Function# 7**	**Function# 8**	**Function# 9**
GPIO_0	TRISTATE_IND	–	–	–	GCI_GPIO_0	–	–	BT_DEV_WAKE	–	–
GPIO_2	JTAG_SEL : ARM DAP TCK	–	–	–	GCI_GPIO_2	–	UART_DBG_RX	BTS_BT_GPIO_2(o/p only)	–	–
GPIO_3	JTAG_SEL : ARM DAP TMS	–	–	–	GCI_GPIO_3	–	UART_DBG_TX	BTS_BT_GPIO_3(o/p only)	–	–
GPIO_4	JTAG_SEL : ARM DAP TDI	–	–	–	GCI_GPIO_4	–	–	BTS_BT_GPIO_4(o/p only)	–	–
GPIO_5	JTAG_SEL : ARM DAP TDO	–	–	–	–	GCI_GPIO_5	–	BTS_BT_GPIO_5(o/p only)	–	–
GPIO_6	JTAG_SEL : ARM DAP TRST_L	–	–	–	GCI_GPIO_1	–	–	BTS_BT_GPIO_11(o/p only)	–	–
SDIO_CLK	SDIO_CLK	–		–	–	–	–	BTS_BT_GPIO_15(o/p only)	–	–
SDIO_CMD	SDIO_CMD	–		–	GCI_GPIO_0	GCI_GPIO_15	–	BTS_BT_GPIO_16(o/p only)	–	–
SDIO_DATA_0	SDIO_DATA_0	–		–	GCI_GPIO_1	–	–	BTS_BT_GPIO_17(o/p only)	–	–

(table continues...)

Table 15 (continued) GPIO alternate signal functions

Pad name	Function sel									
	Function# 0	Function# 1	Function# 2	Function# 3	Function# 4	Function# 5	Function# 6	Function# 7	Function# 8	Function# 9
SDIO_DATA_1	SDIO_DATA_1	–		–	GCI_GPIO_2	–	–	–	–	–
SDIO_DATA_2	SDIO_DATA_2	–		–	GCI_GPIO_3	–	–	–	–	–
SDIO_DATA_3	SDIO_DATA_3	–	–	–	GCI_GPIO_4	–	–	–	–	–
RF_SW_CTRL_0	RF_SW_CTRL_0	–	–	–	–	–	–	–	–	–
RF_SW_CTRL1	RF_SW_CTRL1	–	–	–	–	–	–	–	–	–
RF_SW_CTRL2	RF_SW_CTRL2	–	–	–	–	–	–	–	–	–
RF_SW_CTRL3	RF_SW_CTRL3	–	–	–	–	–	–	–	–	–
RF_SW_CTRL4	RF_SW_CTRL4	–	–	–	–	–	–	–	–	–
RF_SW_CTRL5	RF_SW_CTRL5	–	–	–	–	–	–	–	–	–
RF_SW_CTRL6	RF_SW_CTRL6	–	–	–	–	GCI_GPIO_8	UART_DBG_RX	–	–	–
RF_SW_CTRL7	RF_SW_CTRL7	–	–	–	–	GCI_GPIO_9	UART_DBG_TX	–	–	–
BT_UART_CTS_N	–	UART_CTS_N	SCB0-UART_CTS	–	–	–	–	–	–	–

(table continues...)

Table 15 (continued) GPIO alternate signal functions

Pad name	Function sel									
	Function# 0	Function# 1	Function# 2	Function# 3	Function# 4	Function# 5	Function# 6	Function# 7	Function# 8	Function# 9
BT_UART_RTS_N	–	UART_RTS_N	SCB0-UART_RTS	–	–	–	–	–	–	–
BT_UART_RXD	–	UART_RXD	SCB0-UART_RXD	–	–	–	UART_DBG_RX	–	–	–
BT_UART_TXD	–	UART_TXD	SCB0-UART_TXD	–	–	–	UART_DBG_TX	–	–	–
BT_GPIO_0	BT_GPIO_0	DEV_WAKE	–		GCI_GPIO_0	–	–	SCB2-SPI_SEL3	–	DEV_WAKE
HOST_WAKE	BT_GPIO_1	HOST_WAKE	–	–	GCI_GPIO_1	–	–	–	–	HOST_WAKE
BT_GPIO_2	BT_GPIO_2	GPIO[2]	–	SCB1-UART_RXD	–	SCB0-SPI_SEL3	UART_DBG_RX	SCB1-SDA	SCB1-SPI_SEL3	–
BT_GPIO_3	BT_GPIO_3	GPIO[3]	–	SCB1-UART_TXD	–	–	UART_DBG_TX	SCB1-SCL	SCB1-SPI_SEL2	–
BT_GPIO_4	BT_GPIO_4	TCPWM_OUT_11	–	SCB1-UART_CTS	–	SCB0-SPI_SEL2	TCPWM_OUT_11	SCB0-SDA	SCB1-SPI_SEL1	DBG_TXD
BT_GPIO_5	BT_GPIO_5	TCPWM_OUT_12	–	SCB1-UART_RTS	–	SCB0-SPI_SEL1	TCPWM_OUT_12	SCB0-SCL	–	DBG_RXD
BT_GPIO_6	BT_GPIO_6	TCPWM_OUT_21	–	SCB2-SDA	–	–	TCPWM_OUT_21	–	–	DBG_SPI_CLK
BT_GPIO_7	BT_GPIO_7	TCPWM_OUT_22	–	SCB2-SCL	GCI_GPIO_2	–	TCPWM_OUT_22	–	–	DBG_SPI_MOSI
BT_GPIO_16	A_GPIO[0]	SCB1_CSN	–	–	GCI_GPIO_3	TCPWM_COMP_OUT_12	TCPWM_OUT_12	SCB1-SCL	SCB1-SPI_SEL0	I2C_SCL

(table continues...)

Table 15 (continued) GPIO alternate signal functions

Pad name	Function sel									
	Function# 0	Function# 1	Function# 2	Function# 3	Function# 4	Function# 5	Function# 6	Function# 7	Function# 8	Function# 9
BT_GPIO_17	A_GPIO[1]	SCB1_CK	–	–	GCI_GPIO_4	TCPWM_COMP_OUT_21	TCPWM_OUT_11	SCB1-SDA	SCB1-SPI_CLK	I2C_SDA
TDM1_WS	TDM1_WS	I2S_WS	–	–	–	–	–	–	–	–
TDM1_SCK	TDM1_SCK	I2S_SCK	–	–	–	–	–	–	–	–
TDM1_MCK	TDM1_MCK	A_GPIO[4]	–	–	–	SCB0-SPI_SEL2	–	–	–	–
TDM1_DI	TDM1_DI	I2S_DI	–	–	–	–	–	–	–	–
TDM1_DO	TDM1_DO	I2S_DO	–	–	–	–	–	–	–	–
TDM2_WS	TDM2_WS	I2S_WS	–	–	–	–	–	–	–	–
TDM2_SCK	TDM2_SCK	I2S_SCK	–	–	–	–	–	SCB2-SPI_SEL1	–	–
TDM2_MCK	TDM2_MCK	A_GPIO[4]	–	–	–	SCB0-SPI_SEL1	–	SCB2-SPI_SEL2	–	–
TDM2_DI	TDM2_DI	I2S_DI	–	–	–	–	–	SCB2-SPI_MOSI	–	–
TDM2_DO	TDM2_DO	I2S_DO	–	–	–	–	–	SCB2-SPI_MISO	–	–
DMIC_CK	DMIC_CK	DMIC_CK	–	–	–	–	–	SCB2-SPI_CLK	–	–

(table continues...)

Table 15 (continued) GPIO alternate signal functions

Pad name	Function sel									
	Function# 0	Function# 1	Function# 2	Function# 3	Function# 4	Function# 5	Function# 6	Function# 7	Function# 8	Function# 9
DMIC_DQ	DMIC_DQ	DMIC_DQ	–	–	–	–	–	SCB2-SPI_SEL0	–	–
SMIF_SPHB_CK	SMIF_SPHB_CK	–	–	–	–	–	–	–	–	–
SMIF_SPHB_DQ3	SMIF_SPHB_DQ3	–	–	–	GCI_CPIO_0	GCI_GPIO_11	–	BT_GPIO_3(o/p only)	–	–
SMIF_SPHB_DQ2	SMIF_SPHB_DQ2	–	–	–	GCI_CPIO_1	GCI_GPIO_12	–	BT_GPIO_4(o/p only)	–	–
SMIF_SPHB_DQ1	SMIF_SPHB_DQ1	–	–	–	GCI_CPIO_2	GCI_GPIO_13	–	BT_GPIO_5(o/p only)	–	–
SMIF_SPHB_DQ0	SMIF_SPHB_DQ0	–	–	–	GCI_CPIO_3	GCI_GPIO_14	–	BT_GPIO_6(o/p only)	–	–
SMIF_SPHB_CS0_N	SMIF_SPHB_CS0_N	–	–	–	GCI_CPIO_4	GCI_GPIO_15	–	BT_GPIO_7(o/p only)	–	–
LPO_IN_OUT	LPO_IN_OUT	–	–	–	–	–	–	–	–	–
LHL_XTALI	LHL_XTALI	–	–	–	–	–	–	–	–	–
LHL_XTALO	LHL_XTALO	–	–	–	–	–	–	–	–	–
JTAG_SEL	JTAG_SEL	–	–	–	–	–	–	–	–	–
BT_DEV_WAKE	BT_DEV_WAKE	–	–	–	–	–	–	–	–	–

(table continues...)

Table 15 (continued) GPIO alternate signal functions

Pad name	Function sel									
	Function# 0	Function# 1	Function# 2	Function# 3	Function# 4	Function# 5	Function# 6	Function# 7	Function# 8	Function# 9
LHL_GPIO_2	ADCIn0	RF_SW_CTRL8	–	SCB1-UART_TXD	–	B_GPIO[0]	TCPWM_TR_ALL_1	–	–	–
LHL_GPIO_3	ADCIn1	RF_SW_CTRL9	–	SCB1-UART_RXD	–	B_GPIO[1]	TCPWM_TR_ALL_2	–	–	–
LHL_GPIO_4	ADCIn2	RF_SW_CTRL10	SCB0_DO	SCB1-UART_CTS	–	B_GPIO[2]	TCPWM_TR_ALL_4	DMIC_CK	SCB0-SPI_MOSI	–
LHL_GPIO_5	ADCIn3	RF_SW_CTRL11	SCB0_DI	SCB1-UART_RTS	–	B_GPIO[3]	TCPWM_TR_ALL_3	DMIC_DI	SCB0-SPI_MISO	–
LHL_GPIO_6	ADCIn4	RF_SW_CTRL12	SCB0_CSN	SCB0-SCL	SCB2-UART_CTS	B_GPIO[4]	TCPWM_TR_ALL_2	SCB1-SPI_SEL0	SCB0-SPI_SEL0	–
SMIF_SPHB_CS1_N	SMIF_SPHB_CS1_N	–	–	–	–	–	–	–	–	–
LHL_GPIO_8	ADCIn6	RF_SW_CTRL14	SCB1_DO	SCB1-SPI_MOSI	SCB2-UART_RXD	B_GPIO[6]	TCPWM_COMP_OUT_21	SCB1-SPI_MOSI	–	–
LHL_GPIO_9	ADCIn7	RF_SW_CTRL15	SCB1_DI	SCB1-SPI_MISO	SCB2-UART_TXD	B_GPIO[7]	TCPWM_COMP_OUT_22	SCB1-SPI_MISO	–	–

8.5 I/O states

The following notations are used in Table 16.

I: Input signal

O: Output signal

I/O: Input/Output signal

PU = Pulled up

PD = Pulled down

NoPull = Neither pulled up nor pulled down

Where applicable, the default value is shown in bold brackets (for example, **[default value]**).

Table 16 I/O states

Name	I/O	Keeper	Active mode	Low-power state/ sleep (All power present)	Power down (BT_REG_ ON)	Out of reset; Before SW Download (BT_REG_ON HIGH)	(BT_REG_ON = 0) and VDDIOs are present	Power rail
BT_REG_ON	I	N	I: PD Pull down auto disabled	I: PD Pull down auto disabled	I: PD (of 50K)	I: PD (of 50K)	I: PD (of 50K)	–
GPIO_0	I/O	Y	I/O: PU, PD, NoPull Programmable [PD]	I/O: PU, PD, NoPull Programmable [PD]	High-Z, NoPull	High-Z, NoPull	High Z, NoPull	VDDIO
GPIO_2	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I:PU	I:PU	VDDIO
GPIO_3	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I:PU	I:PU	VDDIO
GPIO_4	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I:PU	I:PU	VDDIO
GPIO_5	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull[13]	I: NoPull	VDDIO
GPIO_6	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: PU	I:PU	VDDIO
RF_SW_CTRL _X	O	N	O: NoPull	O: NoPull	High-Z, NoPull	O: NoPull	O: NoPull	VDDIO_RFS W
SMIF_SPHB_ CK	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO

(table continues...)

Table 16 (continued) I/O states

Name	I/O	Keeper	Active mode	Low-power state/ sleep (All power present)	Power down (BT_REG_ ON)	Out of reset; Before SW Download (BT_REG_ON HIGH)	(BT_REG_ON = 0) and VDDIOs are present	Power rail
SMIF_SPHB_ DQ3	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
SMIF_SPHB_ DQ2	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
SMIF_SPHB_ DQ1	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
SMIF_SPHB_ DQ0	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
SMIF_SPHB_ CS0_N	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
SMIF_SPHB_ CS1_N	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
BT_GPIO_0	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
BT_GPIO_2	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO

(table continues...)

Table 16 (continued) I/O states

Name	I/O	Keeper	Active mode	Low-power state/ sleep (All power present)	Power down (BT_REG_ ON)	Out of reset; Before SW Download (BT_REG_ON HIGH)	(BT_REG_ON = 0) and VDDIOs are present	Power rail
BT_GPIO_3	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PU	I: PU	BT_VDDO
BT_GPIO_4	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PU	I: PU	BT_VDDO
BT_GPIO_5	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PU	I: PU	BT_VDDO
BT_GPIO_6	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
BT_GPIO_7	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
BT_GPIO_16	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
BT_GPIO_17	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
TDM1_WS	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO

(table continues...)

Table 16 (continued) I/O states

Name	I/O	Keeper	Active mode	Low-power state/ sleep (All power present)	Power down (BT_REG_ ON)	Out of reset; Before SW Download (BT_REG_ON HIGH)	(BT_REG_ON = 0) and VDDIOs are present	Power rail
TDM1_SCK	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
TDM1_MCK	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
TDM1_DI	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
TDM1_DO	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
TDM2_WS	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
TDM2_SCK	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
TDM2_MCK	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
TDM2_DI	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO

(table continues...)

Table 16 (continued) I/O states

Name	I/O	Keeper	Active mode	Low-power state/ sleep (All power present)	Power down (BT_REG_ ON)	Out of reset; Before SW Download (BT_REG_ON HIGH)	(BT_REG_ON = 0) and VDDIOs are present	Power rail
TDM2_DO	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
DMIC_CK	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
DMIC_DQ	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
BT_HOST_WAKE	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
BT_DEV_WAKE	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO
LHL_GPIO2	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO
LHL_GPIO3	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO
LHL_GPIO4	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO

(table continues...)

8 Pinout and signal descriptions

Table 16 (continued) I/O states

Name	I/O	Keeper	Active mode	Low-power state/ sleep (All power present)	Power down (BT_REG_ ON)	Out of reset; Before SW Download (BT_REG_ON HIGH)	(BT_REG_ON = 0) and VDDIOs are present	Power rail
LHL_GPIO5	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO
LHL_GPIO6	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO
LHL_GPIO8	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO
LHL_GPIO9	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO

8 Pinout and signal descriptions

***Note**: When JTAG is not enabled on the GPIO.*

9 DC characteristics

9.1 Absolute maximum ratings

Table 17 Absolute maximum ratings

Parameter	Symbol	Value	Unit
DC supply for VBAT and PA driver supply	ASR_VDDBAT, BTLDO_VDDBAT, WLLDO_VDDBAT	–0.5 to +6.0	V
DC supply voltage for digital I/O	VDDIO, BT_VDDO, PMU_VD1P8	–0.5 to 2.2	V
DC supply voltage for RF switch I/Os	VDDIO_RFSW	–0.5 to 3.9	V
DC supply voltage for core	VDDC, AVDD_BBPLL	0.9	V
Maximum undershoot voltage for I/O[1)]	Vundershoot	–0.5	V
Maximum overshoot voltage for I/O[1)]	Vovershoot	VDDIO + 0.5	V
Maximum junction temperature	Tj	125	°C
Maximum input power for RX input ports[2)]	–	13	dBm

1) Duration not to exceed 25% of the duty cycle.
2) Devices incur a maximum of 3 dB reduction in LNA gain with a maximum input level of 13 dBm at a 1.5% duty-cycle derated from a 7-year lifetime.

9.2 Environmental ratings

The environmental ratings are shown in Table 18.

Table 18 Environmental ratings

Characteristic	Value	Unit	Conditions/comments
Ambient temperature (T_A)	–40 to +85	°C	Functional operation[1)]
Storage temperature	–5 to +40	°C	–
Relative humidity	Less than 60	%	Storage
	Less than 85	%	Operation

1) The device is functional across this range of temperature. The device autonomously monitors its junction temperature and employs transmit throughput throttling to regulate power dissipation and ensure that the junction temperature is held below maximum ratings for device reliability.

9.3 Recommended operating conditions and DC characteristics

Warning: ***Functional operation is not guaranteed outside of the limits shown in Table 19, and operation outside these limits for extended periods can adversely affect long-term reliability of the device.***

9 DC characteristics

Table 19 Recommended operating conditions and DC characteristics

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
DC supply voltage for VBAT	ASR_VDDBAT, BTLDO_VDDBAT, WLLDO_VDDBAT	3.0[1)]	3.3	4.8[2)]	V
DC supply voltage for core	VDDC, AVDD_BBPLL	0.86	0.9	0.94	V
DC supply voltage for digital I/O	VDDIO, BT_VDDO, PMU_VDD1P8	1.71	1.8	1.89	V
DC supply voltage for RF switch I/Os when supporting 3.3 V RF_SW_CTRL pads	VDDIO_RFSW	3.13	3.3	3.47	V
External TSSI input	TSSI	0.15	–	0.95	V
Internal POR threshold	Vth_POR	0.4	–	0.7	V
Digital I/O pins[3)]					
For VDDIO, BT_VDDO = 1.8 V					
Input high voltage	VIH	0.65 × VDDIO	–	–	V
Input low voltage	VIL	–	–	0.35 × VDDIO	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.40	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
RF switch control output pins[3)]					
For VDDIO_RFSW = 3.3 V					
Output high voltage @ 2 mA	VOH	VDDIO_RFSW – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.4	V
BT_REG_ON Pins					
Input capacitance	CIN	–	–	5	pF
Input high voltage	VIH	1.2	–	VBAT	V
Input low voltage	VIL	–	–	0.3	V
Pull down resistance	R_{PD}	–	50	–	kΩ

1) CYW55310 is functional across this range of voltages. Optimal RF performance specified in the datasheet, however, is guaranteed only for 3.13 V < VBAT < 3.6 V.
2) The maximum continuous voltage is 5.25 V. Voltage transients up to 6.0 V for up to 10 s, cumulative duration over the lifetime of the device, are allowed. The voltage transients as high as 5.5 V for up to 250 seconds, cumulative duration over the lifetime of the device, are allowed.
3) Programmable 2 mA to 16 mA drive strength, default is 10 mA.

9.4 Electrostatic discharge (ESD) specifications

Extreme caution must be exercised to prevent electrostatic discharge damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 20 ESD specifications

Pin type	Symbol	Conditions	ESD rating	Unit
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	±2	kV
CDM	ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	±300[1)]	V
Latch-up	–	At 125°C	±200	mA

1) BTRF_13dBm and 20dBm pass at 250V.

10 Bluetooth® RF specifications

Unless otherwise stated, limit values apply for the conditions specified in Table 22 and Table 27. Typical values apply for an ambient temperature of +25°C. Unless otherwise stated, the values in this section are design targets, to be confirmed by silicon characterization. Figure 15 shows the RF port locations for testing Bluetooth® in a system configuration with two antennas. Only one of the two system antennas is available to Bluetooth® in this configuration.

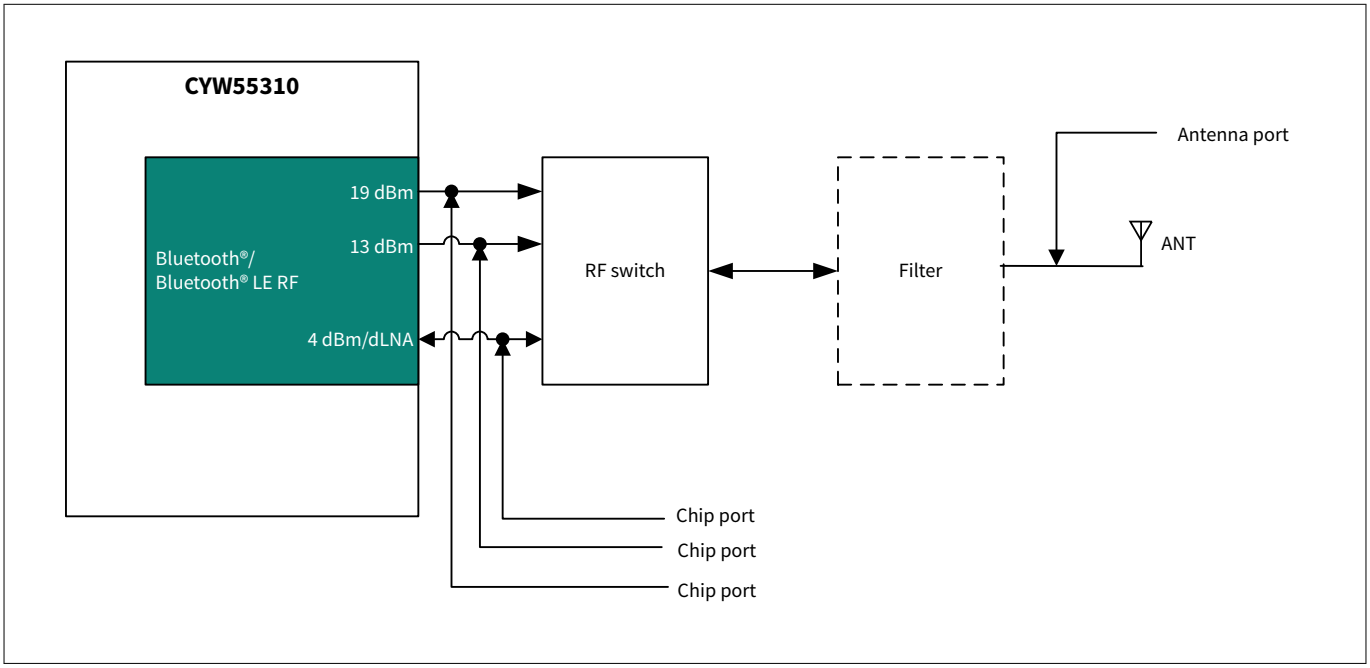


Figure 15 RF port locations for Bluetooth® testing in a single antenna system - Bluetooth® dedicated LNA with dedicated antenna configuration

10.1 Bluetooth® receiver RF specifications

Table 21 Bluetooth® receiver RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
***Note**: The specifications in this table are measured at the chip port output unless otherwise specified.*					
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity	GFSK, 0.1% BER, 1 Mbps	–	–95.0	–	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	–	–97.0	–	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–91.0	–	dBm
Maximum input	–	–	–20	–	dBm
Maximum RX LO leakage					
2.4 GHz band	–	–	–80.0	–	dBm
Interference performance[1)]					

(table continues...)

Table 21 (continued) Bluetooth® receiver RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
C/I co-channel	GFSK, 0.1% BER	–	8.5	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–5.0	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–35.0	–30	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER	–	–45.5	–40	dB
C/I image channel	GFSK, 0.1% BER	–	–31.5	–9.0	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	–	–38.5	–20	dB
C/I co-channel	π/4-DQPSK, 0.1% BER	–	10.5	13.0	dB
C/I 1 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–7.5	0	dB
C/I 2 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–35.0	–30.0	dB
C/I ≥ 3 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–47.0	–40.0	dB
C/I image channel	π/4-DQPSK, 0.1% BER	–	–30.0	–7.0	dB
C/I 1 MHz adjacent to image channel	π/4-DQPSK, 0.1% BER	–	–42.0	–20.0	dB
C/I co-channel	8-DPSK, 0.1% BER	–	18.5	21.0	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	–	–0.5	5.0	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	–	–34.0	–25.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–41.5	–33.0	dB
C/I Image channel	8-DPSK, 0.1% BER	–	–20.0	0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	–	–35.0	–13.0	dB
Out-of-band blocking performance (CW)					
30–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27.0	–	dBm
2498–3000 MHz	0.1% BER	–	–27.0	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm
GFSK (1 Mbps)[2]					
698–716 MHz	WCDMA	–	–13.0	–	dBm
776–849 MHz	WCDMA	–	–14.0	–	dBm
824–849 MHz	GSM850	–	–13.0	–	dBm
824–849 MHz	WCDMA	–	–14.0	–	dBm
880–915 MHz	E-GSM	–	–13.0	–	dBm
880–915 MHz	WCDMA	–	–13.0	–	dBm
1710–1785 MHz	GSM1800	–	–18.0	–	dBm

(table continues...)

Table 21 (continued) Bluetooth® receiver RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
1710–1785 MHz	WCDMA	–	–17.0	–	dBm
1850–1910 MHz	GSM1900	–	–19.0	–	dBm
1850–1910 MHz	WCDMA	–	–19.0	–	dBm
1880–1920 MHz	TD-SCDMA	–	–20.0	–	dBm
1920–1980 MHz	WCDMA	–	–20.0	–	dBm
2010–2025 MHz	TD-SCDMA	–	–20.0	–	dBm
2500–2570 MHz	WCDMA	–	–26.0	–	dBm
2510 MHz	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2530 MHz	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2550 MHz	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2570 MHz	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2310 MHz	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2330 MHz	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2350 MHz	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2370 MHz	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2570–2620 MHz[3]	Band 38	–	–33.0	–	dBm
2545–2575 MHz[4]	XGP Band	–	–33.0	–	dBm
π/4-DPSK (2 Mbps)[5]					
698–716 MHz	WCDMA	–	–10.0	–	dBm
776–794 MHz	WCDMA	–	–10.0	–	dBm
824–849 MHz	GSM850	–	–11.0	–	dBm
824–849 MHz	WCDMA	–	–11.0	–	dBm
880–915 MHz	E-GSM	–	–10.0	–	dBm
880–915 MHz	WCDMA	–	–10.0	–	dBm
1710–1785 MHz	GSM1800	–	–16.0	–	dBm
1710–1785 MHz	WCDMA	–	–15.0	–	dBm
1850–1910 MHz	GSM1900	–	–17.0	–	dBm
1850–1910 MHz	WCDMA	–	–16.0	–	dBm
1880–1920 MHz	TD-SCDMA	–	–18.0	–	dBm
1920–1980 MHz	WCDMA	–	–17.0	–	dBm
2010–2025 MHz	TD-SCDMA	–	–19.0	–	dBm
2500–2570 MHz	WCDMA	–	–23.0	–	dBm
2510 MHz	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm

(table continues...)

Table 21 (continued) Bluetooth® receiver RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
2530 MHz	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2550 MHz	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2570 MHz	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2310 MHz	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2330 MHz	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2350 MHz	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2370 MHz	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2570–2620 MHz[3)]	Band 38	–	–33.0	–	dBm
2545–2575 MHz[4)]	XGP Band	–	–33.0	–	dBm
8-DPSK (3 Mbps)[6)]					
698–716 MHz	WCDMA	–	–13.0	–	dBm
776–794 MHz	WCDMA	–	–13.0	–	dBm
824–849 MHz	GSM850	–	–13.0	–	dBm
824–849 MHz	WCDMA	–	–14.0	–	dBm
880–915 MHz	E-GSM	–	–13.0	–	dBm
880–915 MHz	WCDMA	–	–13.0	–	dBm
1710–1785 MHz	GSM1800	–	–18.0	–	dBm
1710–1785 MHz	WCDMA	–	–17.0	–	dBm
1850–1910 MHz	GSM1900	–	–19.0	–	dBm
1850–1910 MHz	WCDMA	–	–19.0	–	dBm
1880–1920 MHz	TD-SCDMA	–	–19.0	–	dBm
1920–1980 MHz	WCDMA	–	–19.0	–	dBm
2010–2025 MHz	TD-SCDMA	–	–20.0	–	dBm
2500–2570 MHz	WCDMA	–	–23.0	–	dBm
2510 MHz	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2530 MHz	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2550 MHz	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2570 MHz	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2310 MHz	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2330 MHz	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2350 MHz	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2370 MHz	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2570–2620 MHz[3)]	Band 38	–	–33.0	–	dBm

(table continues...)

Table 21 (continued) Bluetooth® receiver RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
2545–2575 MHz[4)]	XGP Band	–	–33.0	–	dBm
Spurious emissions					
30 MHz–1 GHz		–	–95.0	-	dBm
1–12.75 GHz		–	–70.0	-	dBm
851–894 MHz		–	–147.0	–	dBm/Hz
925–960 MHz		–	–147.0	–	dBm/Hz
1805–1880 MHz		–	–147.0	–	dBm/Hz
1930–1990 MHz		–	–147.0	–	dBm/Hz
2110–2170 MHz		–	–147.0	–	dBm/Hz

1) The maximum value represents the actual Bluetooth® specification required for Bluetooth® qualification as defined in the version 4.0 specification.
2) Bluetooth® reference level for the wanted signal at the Bluetooth® chip port = –92 dBm.
3) Interferer: 2580 MHz, BW = 10 MHz; measured at 2480 MHz.
4) Interferer: 2555 MHz, BW = 10 MHz; measured at 2480 MHz.
5) Bluetooth® reference level for the wanted signal at the Bluetooth® chip port = –94 dBm.
6) Bluetooth® reference level for the wanted signal at the Bluetooth® chip port = –88 dBm.

10.2 Bluetooth® TX13 transmitter RF specifications

Table 22 Bluetooth® TX13 transmitter RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
***Note**: The specifications in this table are measured at the chip port output unless otherwise specified.*					
General					
Frequency range		2402	–	2480	MHz
Basic rate (GFSK) TX power at Bluetooth®		–	13.0	–	dBm
QPSK TX power at Bluetooth®		–	9.0	–	dBm
8PSK TX power at Bluetooth®		–	9.0	–	dBm
Power control step		_	4	_	dB
Minimum power control range		_	28	_	dB
***Note**: Output power is with TCA and TSSI enabled.*					
GFSK in-band spurious emissions					
–20 dBc BW		–	0.93	1	MHz
EDR in-band spurious emissions					
1.0 MHz < |M – N| < 1.5 MHz	M – N = the frequency range for which the spurious emission is	–	–45.0	–26.0	dBc

(table continues...)

Table 22 (continued) Bluetooth® TX13 transmitter RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
1.5 MHz < |M – N| < 2.5 MHz	measured relative to the transmit center frequency.	–	–31.0	–20.0	dBm
|M – N| ≥ 2.5 MHz[1)]		–	–45.0	–40.0	dBm
TX harmonics (HD2, HD3, HD4) chip Pout = 13 dBm in BDR and Bluetooth® LE mode	HD2	–	-10.0	–	dBm
	HD3	–	-23.0	–	dBm
	HD4	–	-34.0	–	dBm
GLONASS BAND spurious emissions					
FDMA L1 Band 1598.0625-1606.375 MHz	–	–	-111	–	dBm/Hz
FDMA L2 Band 1242.9375-1248.625 MHz	–	–	-160	–	dBm/Hz
CDMA L1 Signal 1202.025 MHz	–	–	-161	–	dBm/Hz
CDMA L2 Signal 1248.06 MHz	–	–	-160	–	dBm/Hz
CDMA L3 Signal 1202.025 MHz	–	–	-161	–	dBm/Hz
GPS band spurious emissions					
CDMA L1 Signal 1575.42 MHz	–	–	-156	–	dBm/Hz
CDMA L2 Signal 1227.60 MHz	–	–	-161	–	dBm/Hz
Out-of-band noise floor[2)]					
65–108 MHz	FM RX	–	–160	–	dBm/Hz
776–794 MHz	CDMA2000	–	–150	–	dBm/Hz
869–960 MHz	cdmaOne, GSM850	–	–150	–	dBm/Hz
925–960 MHz	E-GSM	–	–150	–	dBm/Hz
1570–1580 MHz	GPS	–	–155	–	dBm/Hz
1805–1880 MHz	GSM1800	–	–147	–	dBm/Hz
1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–147	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–138	–	dBm/Hz
2500–2570 MHz	Band 7	–	–134	–	dBm
2300–2400 MHz	Band 40	–	–133	–	dBm
2570–2620 MHz	Band 38	–	–135	–	dBm
2545–2575 MHz	XGP Band	–	–135	–	dBm

1) The typical number is measured at ± 3 MHz offset.
2) Transmitted power in cellular and FM bands at the Bluetooth® antenna port. See Figure 15 for location of the port.

10.3 Local oscillator performance

Table 23 Local oscillator performance

Parameter	Min	Typ	Max	Unit
LO performance				
Initial carrier frequency tolerance	–	±15.0	±75.0	kHz
Frequency drift	–	–	–	–
DH1 packet	–	±12.0	±25.0	kHz
DH3 packet	–	±12.0	±40.0	kHz
DH5 packet	–	±12.0	±40.0	kHz
Drift rate	–	10.0	20.0	kHz/50 µs
Frequency deviation				
00001111 sequence in payload[1)]	140	153	175	kHz
10101010 sequence in payload[2)]	115	145	–	kHz
Channel spacing	–	1	–	MHz

1) This pattern represents and average deviation in payload.
2) Pattern represents the maximum deviation in payload for 99.9% of all the frequency deviations.

10.4 Bluetooth® TX0 transmitter RF specifications

The TX0 transmitter only supports BDR, LE1, LE2 and LELR modulations.

Table 24 Bluetooth® TX0 transmitter RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
***Note**: The specifications in this table are measured at the chip port output unless otherwise specified.*					
General					
Frequency range		2402	–	2480	MHz
Basic rate (GFSK) TX power at Bluetooth®		–	4.0	–	dBm
Power control step		_	4	_	dB
Minimum power control range		_	28	_	dB
GFSK in-band spurious emissions					
–20 dBc BW		–	0.93	1	MHz
Out-of-band spurious emissions					
TX harmonics (HD2, HD3, HD4)	HD2	–	-11	–	dBm
	HD3	–	-12	–	dBm

(table continues...)

Table 24 (continued) Bluetooth® TX0 transmitter RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
chip Pout = 4 dBm in BDR and Bluetooth® LE mode	HD4	–	-18	–	dBm
GLONASS BAND spurious emissions					
FDMA L1 Band 1598.0625-1606.375 MHz	–	–	-111	–	dBm/Hz
FDMA L2 Band 1242.9375-1248.625 MHz	–	–	-160	–	dBm/Hz
CDMA L1 Signal 1202.025 MHz	–	–	-161	–	dBm/Hz
CDMA L2 signal 1248.06 MHz	–	–	-160	–	dBm/Hz
CDMA L3 signal 1202.025 MHz	–	–	-161	–	dBm/Hz
GPS band spurious emissions					
CDMA L1 signal 1575.42 MHz	–	–	-156	–	dBm/Hz
CDMA L2 signal 1227.60 MHz	–	–	-161	–	dBm/Hz
Out-of-band noise floor[1)]					
65–108 MHz	FM RX	–	–160	–	dBm/Hz
776–794 MHz	CDMA2000	–	–150	–	dBm/Hz

1) Transmitted power in cellular and FM bands at the Bluetooth® antenna port. See Figure 15 for location of the port.

10.5 Bluetooth® TX19 transmitter RF specifications

Table 25 Bluetooth® TX19 transmitter RF specifications

Parameter	Conditions	Min	Typ	Max	Unit

***Note**: The specifications in this table are measured at the Chip port output unless otherwise specified.*

General				
Frequency range	2402	–	2480	MHz
Basic rate (GFSK) TX power at Bluetooth®	–	19.0	–	dBm
QPSK TX power at Bluetooth®	–	13.0	–	dBm
8PSK TX power at Bluetooth®	–	13.0	–	dBm
Power control step	–	4	–	dB
Minimum power control range	_	6 (BDR), 4 (EDR)	_	dB

(table continues...)

Table 25 (continued) Bluetooth® TX19 transmitter RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
***Note**: Output power is with TCA and TSSI enabled.*					
GFSK in-band spurious emissions					
–20 dBc BW		–	0.93	1	MHz
EDR in-band spurious emissions					
1.0 MHz < |M – N| < 1.5 MHz	M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency.	–	–53.0	–26.0	dBc
1.5 MHz < |M – N| < 2.5 MHz		–	–30.0	–20.0	dBm
|M – N| ≥ 2.5 MHz[1)]		–	–45.0	–40.0	dBm
Out-of-band spurious emissions					
TX harmonics (HD2, HD3, HD4) chip Pout = 19 dBm in BDR and Bluetooth® LE mode	HD2	–	-7.0	–	dBm
	HD3	–	-21.0	–	dBm
	HD4	–	-32.0	–	dBm
GLONASS BAND spurious emissions					
FDMA L1 band 1598.0625-1606.375 MHz	–	–	-114	–	dBm/ Hz
FDMA L2 band 1242.9375-1248.625 MHz	–	–	-160	–	dBm/ Hz
CDMA L1 signal 1202.025 MHz	–	–	-161	–	dBm/ Hz
CDMA L2 signal 1248.06 MHz	–	–	-160	–	dBm/ Hz
CDMA L3 signal 1202.025 MHz	–	–	-161	–	dBm/ Hz
GPS band spurious emissions					
CDMA L1 signal 1575.42 MHz	–	–	-156	–	dBm/ Hz
CDMA L2 Signal 1227.60 MHz	–	–	-161	–	dBm/ Hz
Out-of-band noise floor[2)]					

(table continues...)

Table 25 (continued) Bluetooth® TX19 transmitter RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
65–108 MHz	FM RX	–	–160	–	dBm/Hz
776–794 MHz	CDMA2000	–	–150	–	dBm/Hz

1) The typical number is measured at ± 3 MHz offset.
2) Transmitted power in cellular and FM bands at the Bluetooth® antenna port. See Figure 15 for location of the port.

10.6 Bluetooth® LE receiver and TX13 transmitter specifications

Table 26 Bluetooth® LE receiver and TX13 transmitter specifications

Parameter	Conditions	Min	Typ	Max	Unit
***Note**: The specifications in this table are measured at the Chip port output unless otherwise specified.*					
Frequency range	–	2402	–	2480	MHz
RX sensitivity[1)]	GFSK, 1 Mbps	–	–101.0	–	dBm
	GFSK, 2 Mbps	–	–97.0	–	dBm
	GFSK, 500 Kbps	–	–106.0	–	dBm
	GFSK, 125 Kbps	–	–111.0	–	dBm
Interference performance [2)]					
C/I co-channel	uncoded 1Ms/S, 30.8% PER	–	8.5	21	dB
C/I 1 MHz adjacent channel	uncoded 1Ms/S, 30.8% PER	–	-2.5	15	dB
C/I 2 MHz adjacent channel	uncoded 1Ms/S, 30.8% PER	–	-34	-17	dB
C/I ≥ 3 MHz adjacent channel	uncoded 1Ms/S, 30.8% PER	–	-39	-27	dB
C/I image channel	uncoded 1Ms/S, 30.8% PER	–	-30	-9	dB
C/I 1 MHz adjacent to image channel	uncoded 1Ms/S, 30.8% PER	–	-42	-15	dB
C/I co-channel	2Ms/S, 30.8% PER	–	7.5	21	dB
C/I 2 MHz adjacent channel	2Ms/S, 30.8% PER	–	0	15	dB
C/I 4 MHz adjacent channel	2Ms/S, 30.8% PER	–	-41	-17	dB
C/I ≥ 6 MHz adjacent channel	2Ms/S, 30.8% PER	–	-51	-27	dB
C/I image channel	2Ms/S, 30.8% PER	–	-31	-9	dB
C/I 2 MHz adjacent to image channel	2Ms/S, 30.8% PER	–	-37	-15	dB
C/I co-channel	LE coded (S=2), 30.8% PER	–	4.0	17	dB
C/I 1 MHz adjacent channel	LE coded (S=2), 30.8% PER	–	-11	11	dB

(table continues...)

Table 26 (continued) Bluetooth® LE receiver and TX13 transmitter specifications

Parameter	Conditions	Min	Typ	Max	Unit
C/I 2 MHz adjacent channel	LE coded (S=2), 30.8% PER	–	-51	-21	dB
C/I ≥ 3 MHz adjacent channel	LE coded (S=2), 30.8% PER	–	-53	-31	dB
C/I Image channel	LE coded (S=2), 30.8% PER	–	-35	-13	dB
C/I 1 MHz adjacent to image channel	LE coded (S=2), 30.8% PER	–	-49	-19	dB
C/I co-channel	LE coded (S=8), 30.8% PER	–	6.5	12	dB
C/I 1 MHz adjacent channel	LE coded (S=8), 30.8% PER	–	-16	6	dB
C/I 2 MHz adjacent channel	LE coded (S=8), 30.8% PER	–	-51	-26	dB
C/I ≥ 3 MHz adjacent channel	LE coded (S=8), 30.8% PER	–	-61	-36	dB
C/I Image channel	LE coded (S=8), 30.8% PER	–	-34	-18	dB
C/I 1 MHz adjacent to image channel	LE coded (S=8), 30.8% PER	–	-49	-24	dB
TX power	–	–	13.0	–	dBm
Power control step	_	_	4	_	dB
Minimum power control range	_`	_	28	_	dB
Mod Char: delta F1 average	GFSK, 1 Mbps	225	250	275.0	kHz
Mod Char: delta F2 max	GFSK, 1 Mbps	185	240	–	kHz
Mod Char: ratio	GFSK, 1 Mbps	0.8	1.0	–	no unit
Mod Char: delta F1 average	GFSK, 2 Mbps	450	500	550	kHz
Mod Char: delta F2 max	GFSK, 2 Mbps	370	460	–	kHz
Mod Char: ratio	GFSK, 2 Mbps	0.8	0.95	–	no unit
Mod Char: delta F1 average	GFSK, 125 kbps	225	250	275	kHz

1) With stable mod index and 37 byte packet length.
2) The maximum value represents the actual Bluetooth® specification required for Bluetooth® qualification as defined in the v4.0 specification.

10.7 Bluetooth® LE TX0 transmitter specifications

Table 27 Bluetooth® LE TX0 transmitter specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	–	2402		2480	MHz
TX power	–	–	4.0	–	dBm
Power control step	_	_	4	_	dB
Minimum power control range	_	_	28	_	dB
Mod Char: delta F1 average	GFSK, 1 Mbps	225	250	275.0	kHz

(table continues...)

Table 27 (continued) Bluetooth® LE TX0 transmitter specifications

Parameter	Conditions	Min	Typ	Max	Unit
Mod Char: delta F2 max	GFSK, 1 Mbps	185	240	–	kHz
Mod Char: ratio	GFSK, 1 Mbps	0.8	1.05	–	no unit
Mod Char: delta F1 average	GFSK, 2 Mbps	450	500	550	kHz
Mod Char: delta F2 max	GFSK, 2 Mbps	370	460	–	kHz
Mod Char: ratio	GFSK, 2 Mbps	0.8	0.95	–	no unit
Mod Char: delta F1 average	GFSK, 125 kbps	225	250	275	kHz

10.8 Bluetooth® TX19 LE transmitter RF specifications

Table 28 Bluetooth® TX19 LE transmitter RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	–	2402	–	2480	MHz
TX power	–	–	19	–	dBm
Power control step	_	_	4	_	dB
Minimum power control range	_	_	6	_	dB
Mod Char: delta F1 average	GFSK, 1 Mbps	225	250	275.0	kHz
Mod Char: delta F2 max	GFSK, 1 Mbps	185	242	–	kHz
Mod Char: ratio	GFSK, 1 Mbps	0.8	1.0	–	no unit
Mod Char: delta F1 average	GFSK, 2 Mbps	450	500	550	kHz
Mod Char: delta F2 max	GFSK, 2 Mbps	370	470	–	kHz
Mod Char: ratio	GFSK, 2 Mbps	0.8	1.0	–	no unit
Mod Char: delta F1 average	GFSK, 125 kbps	225	250	275	kHz

11 Internal regulator electrical specifications

Functional operation is not guaranteed outside of the specification limits provided in this section.

11.1 Main PMU

Table 29 PMU specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input supply voltage	V_{BAT}	–	3.0	3.3	4.8	V
I/O supply voltage	V_{DDIO}	–	1.71	1.80	1.89	V
V_{BAT} UVLO threshold	V_{UVLO_RISE} V_{UVLO_FALL}	Rising (UVLO clear) Falling (UVLO set)	2.32 2.20	2.48 2.34	2.62 2.44	V
V_{DDIO} brownout threshold	V_{BRWO_RISE} V_{BRWO_FALL}	Rising (brownout clear) Falling (brownout set)	1.44 1.38	1.51 1.44	1.58 1.51	V

11.2 Analog switching regulator specifications

Table 30 Analog switching regulator specifications

Specification	Symbol	Notes	Min	Typ	Max	Unit
Switching frequency	F_{SW}	With calibration (PWM mode only) programming range	3.04 2.8	3.2	3.36 5.0	MHz
Output current	I_{OUT}	PWM mode, max DC at Tj 125°C	–	–	400	mA
Output voltage	V_{OUT}	Active LP Sleep Programming range	0.64	1.12 1.12 0.74	1.26	V
DC accuracy	ΔV_{OUT_ERR}	Untrimmed Trimmed (PWM mode)	-4 -2	–	4 2	%
Ripple voltage	V_{RIPPLE}	PWM mode PFM mode Measured 20 MHz BW limit, static load	–	5 7	10 20	mVpp
Power up time	T_{PU_CSR}	V_{BAT} and V_{DDIO} as always ON, ULBG ON REG_ON < asr_pok	–	472	–	µs
External inductor	L	See External components section for more details	–	2.2	–	µH
External output capacitor	C_O	See External components section for more details	–	4.7	–	µF
External input capacitor	C_{IN}	See External components section for more details	–	4.7	–	µF

11.3 CLDO

Table 31 CLDO specifications

Specification	Symbol	Notes	Min	Typ	Max	Unit
Input voltage	V_{IN}	$V_{IN} = V_{OUT} + V_{DROPOUT}$	0.74	1.12	1.26	V
Output voltage	V_{OUT}	–	_	0.900	_	V
Output voltage accuracy	–	–	-4	–	4	%
Dropout voltage	$V_{DROPOUT}$	I_{OUT} = 125 mA	80	–	–	mV
Output current	I_{OUT}	T ≤ 25°C	0.01	–	125	mA
		T > 25°C	0.06	–	125	
Line regulation	–	1.12 ≤ V_{IN} ≤ 1.26 V V_{OUT} = 0.9 V I_{OUT} = 125 mA.	–	–	3	mV/V
Load regulation	–	V_{IN} = 1.12 V V_{OUT} = 0.9 V 1 mA ≤ I_{OUT} ≤ 125 mA	–	–	0.125	mV/mA
Load step error	–	V_{IN} = 1.12 V V_{OUT} = 0.9 V I_{OUT} step from 1 mA to 125 mA in 200 ns C_{OUT} = 1.0 µF[1)]	–	–	70	mV
PSRR	–	100 Hz ≤ f ≤ 100 kHz V_{IN} = 1.12 V V_{OUT} = 0.9 V I_{OUT} = 125 mA	20	–	–	dB
Turn-on time[2)]	T_{ON}	Time from enable to V_{OUT} = 855 mV I_{OUT} = 60 µA V_{OUT} = 0.9 V C_{OUT} = 1.0 µF[1)]	–	40	–	µs
In-rush current	I_{INRUSH}	I_{OUT} = 60 µA V_{OUT} = 0.9 V C_{OUT} =1.0 µF[1)]	–	–	60	mA
Output capacitor	C_{OUT}	6.3 V, 0201, ±20%	–	1	–	µF

1) Output capacitor is Murata GRM033C80J105ME05.
2) Refer to register map for actual inrush delay setting.

11.4 BTLDO

Table 32 BTLDO specifications

Specification	Symbol	Notes	Min	Typ	Max	Unit
Input supply voltage	V_{BAT}	Range	3.0	3.3	4.8	V
Nominal output voltage	V_{OUT}	–	–	2.915[1)]	–	V
Output voltage accuracy	–	–	-4	–	4	%
Dropout voltage	–	I_{OUT} = 400 mA	200	–	–	mV
Output current	I_{OUT}	–	0.2		400	mA
Line regulation	–	3.5 V ≤ V_{BAT} ≤ 4.8 VI_{OUT} = 400 mA, V_{OUT} = 3.3 V	–	–	3	mV/V
Load regulation	–	1 mA ≤ I_{OUT} ≤ 400 mAV_{BAT} = 3.7 V, V_{OUT} = 3.3 V	–	–	0.3	mV/mA
Load step error	–	Load step from 1 mA to 200 mA in 1 µs, V_{BAT} = 3.7 V, V_{OUT} = 3.3 V, C_{OUT} = 2.2 µF	–	–	72	mV
PSRR	–	100 Hz ≤ f_{TEST} ≤ 100 kHz I_{OUT} = 200 mA	20	–	–	dB
Turn-on time[2)]	T_{ON}		–	–	80	µs
Output current limit	$I_{OUT(LIMIT)}$		–	–	1.1	A
In-rush current	I_{INRUSH}		–	–	193	mA
Output capacitor	C_{OUT}	6.3 V, 0402, ±10%	–	2.2		µF

1) LDO output voltage is configured to 2.915 V with a minimum headroom (VBAT-LDO OUTPUT) of 120 mV,
2) Refer to register map for actual inrush delay setting.

11.5 RFLDO

Table 33 RFLDO specifications

Specification	Symbol	Notes	Min	Typ	Max	Unit
Input supply voltage	V_{BAT}	Range	3.0	3.3	4.8	V
Nominal output voltage	V_{OUT}	–	–	2.915[1)]	–	V
Output voltage accuracy	–	–	–4	–	4	%
Dropout voltage	–	I_{OUT} = 100 mA	–	127	200	mV
Output current	I_{OUT}	–	0.1	–	100	mA
Line regulation	–	3.5 V ≤ V_{BAT} ≤ 4.8 VI_{OUT} = 100 mA, V_{OUT} = 3.3 V	–	–	3	mV/V

(table continues...)

Table 33 (continued) RFLDO specifications

Specification	Symbol	Notes	Min	Typ	Max	Unit
Load regulation	–	1 mA ≤ I_{OUT} ≤ 100 mAV_{BAT} = 3.7 V, V_{OUT}=3.3 V	–	–	0.3	mV/mA
Load step error	–	Load step from 1 mA to 100 mA in 1 µs, V_{BAT} = 3.7 V, V_{OUT} = 3.3 V, C_{OUT} = 1 µF	–	–	55	mV
PSRR	–	100 Hz ≤ f_{TEST} ≤ 100 kHz I_{OUT} = 100 mA, V_{BAT} = 3.7 V, V_{OUT} = 3.3 V, C_{OUT} = 1 µF	–	–	-20	dB
Turn-on time [2)]	T_{ON}		–	–	145	µs
Output current limit	$I_{OUT(LIMIT)}$		–	–	250	mA
In-rush current	I_{INRUSH}		–	–	60	mA
Output capacitor	C_{OUT}	1 mF, 6.3 V, 0201, ±20%	–	1.0	2.2	µF

1) LDO output voltage is configured to 2.915 V with a minimum headroom (VBAT-LDO OUTPUT) of 120 mV.
2) Refer to the register map for the actual inrush delay setting.

11.6 External components

Choice of inductor depends on DCR, ACR, saturation currents, temperature rise criteria, and footprint/height. Use of smaller components may negatively impact overall efficiency performance.

Table 34 Inductor

Vendor	Part #	L (µH)	Tol (%)	DCR_{max} (mΩ)	DCR_{AVG} (mΩ)	Current rating (A)	Size (in)	Purpose
Murata	DFE201610E_2R2M	2.2	±20	140	117	1.7	0806	ASR Output Inductor
Murata	LQM2MPN2R2MG0	2.2	±20	138	110	1.2	0806	
Murata	WIP201610S-2R2ML	2.2	±20	140	117	2.0	0806	

Recommended capacitor options are as follows:

Table 35 Capacitor

Vendor	Part	C (µF)	Tol (%)	Voltage (V)	Temp rating	Size (in)	Purpose
Murata	GRM033R60J224ME15	0.22	±20	6.3	X5R	0201	PMU input bypass
Murata	GRM033R60J105MEA2D	1.0	±20	6.3	X5R	0201	CLDO, RFLDO output
Murata	GRM033C80J105ME05	1.0	±20	6.3	X6S	0201	
Murata	GRM155C70J225KE11	2.2	±10	6.3	X7S	0402	BTLDO, PALDO Outputs
Murata	GRM155R61C225KE11	2.2	±10	16	X5R	0402	
Murata	GRM155R61A475MEAA	4.7	±20	10	X5R	0402	ASR, PMU input bypass
Murata	GRM188R60J475ME84	4.7	±20	6.3	X5R	0603	

(table continues...)

11 Internal regulator electrical specifications

Table 35 (continued) Capacitor

Vendor	Part	C (µF)	Tol (%)	Voltage (V)	Temp rating	Size (in)	Purpose
Murata	GRM188R60J475KE19	4.7	±10	6.3	X5R	0603	
Murata	GRM188R61C106KAAL	10	±10	16	X5R	0603	

12 System power consumption

12.1 Bluetooth® current consumption

The Bluetooth® and Bluetooth® Low energy current consumption measurements are shown in Table 36.

Note:
- *The Bluetooth® current consumption numbers are measured based on BLE/BDR GFSK TX output power = 13 dBm*
- *All data are taken with 384KB SRAM and 64 KB PRAM in retention mode, with dLNA mode and Processor speed : 48 MHz.*

Table 36 Bluetooth® and Bluetooth® LE current consumption

Operating mode	VBAT(VBAT = 3.3 V) typical	VDDIO (VDDIO = 1.8 V)typical	Unit
Sleep	31.27	7.56	µA
Standard 1.28 s inquiry scan	135.65	10.97	µA
500 ms sniff central	110.14	10.71	µA
DM1/DH1 central TXRX	15.57	0.31	mA
DM1/DH1 peripheral TXRX	15.54	0.31	mA
DM3/DH3 central TXRX	18.33	0.33	mA
DM3/DH3 peripheral TXRX	18.30	0.33	mA
DM5/DH5 central TXRX	18.81	0.34	mA
DM5/DH5 peripheral TXRX	18.79	0.34	mA
3DH5/3DH1 central TXRX	17.65	0.43	mA
3DH5/3DH1 peripheral TXRX	17.61	0.43	mA
SCO HV3 central	7.73	0.25	mA
Bluetooth® LE scan	145.68	11	µA
Bluetooth® LE nonconnectable 1.28 s ADV (3-channels)	69.16	8.51	µA
Bluetooth® LE nonconnectable 1.28 s ADV (3-channels) (low-power TX path)	62.54	8.45	µA
Bluetooth® LE 300 ms connected peripheral	147.34	12.25	µA
Bluetooth® LE 300 ms connected peripheral (+4 dBm low-power TX path)	141.17	12.38	µA
Bluetooth® LE 1 s connected peripheral	75.81	8.97	µA
Transmit packet current - BDR	30.3	0.3	mA
Transmit packet current - EDR	27.5	0.3	mA
Transmit packet current - LE	30.6	0.3	mA
Receive packet current - BR/EDR	10.0	0.3	mA
Receive packet current - LE	10.4	0.3	mA

12 System power consumption

Table 37 Bluetooth® and Bluetooth® LE current consumption (Tx19 high power Tx path)

Operating mode	VBAT (VBAT = 3.3 V) Typical	VDDIO (VDDIO = 1.8 V) Typical	Unit
Sleep	31.37	7.73	µA
Standard 1.28 s inquiry scan	135.89	10.90	µA
500 ms sniff central	144.43	10.77	µA
DM1/DH1 central TXRX	50.15	0.31	mA
DM1/DH1 peripheral TXRX	49.92	0.31	mA
DM3/DH3 central TXRX	65.04	0.34	mA
DM3/DH3 peripheral TXRX	65.14	0.34	mA
DM5/DH5 central TXRX	67.79	0.34	mA
DM5/DH5 peripheral TXRX	67.88	0.34	mA
3DH5/3DH1 central TXRX	81.77	0.43	mA
3DH5/3DH1 peripheral TXRX	81.69	0.43	mA
SCO HV3 central	20.06	0.25	mA
Bluetooth® LE scan (Passive, Scan Int: 1.28 sec, Scan Window: 11.25 ms)	147	11.03	µA
Bluetooth® LE non-connectable 1.28 sec ADV (3 Channels)	110.47	8.62	µA
Bluetooth® LE 300 ms connected peripheral	170.93	12.45	µA
Bluetooth® LE 1 sec connected peripheral	81.96	9.15	µA
Transmit packet current - BDR	126.4	0.3	mA
Transmit packet current - EDR	153.7	0.3	mA
Transmit packet current - LE	126.6	0.3	mA
Receive packet current - BR/EDR	9.9	0.3	mA
Receive packet current - LE	10.2	0.3	mA

13 Power-up sequence and timing

13.1 Sequencing of reset and regulator control signals

The AIROC™ CYW55310 has a signal that allow the host to control power consumption by enabling or disabling the Bluetooth®, and internal regulator blocks. Additionally, diagrams are provided to indicate proper sequencing of the signal for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

13.1.1 Description of control signals

BT_REG_ON: Used by the PMU to power up the internal CYW55310 regulators. When this pin is LOW the Bluetooth® section is in reset and the regulators are disabled.

Note:
- *VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.*
- *VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.*

13.1.2 Control signal timing diagrams

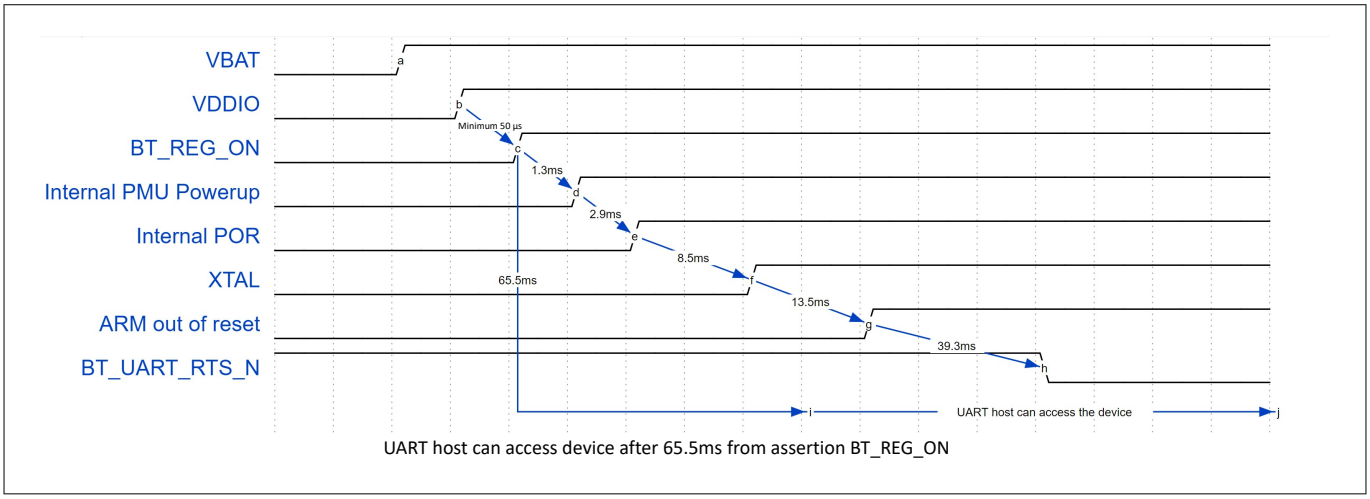


Figure 16 Bluetooth® subsystem bootup sequence

14 Package information

14.1 Package thermal characteristics

The information in Table 38 is based on the following conditions:

- Absolute junction temperature 125°C limit is maintained through active thermal monitoring, throttling, and turning OFF one of the TX chains or both

Table 38 WLBGA package thermal characteristics

Characteristic	WLBGA
θ_{JA} (°C/W) (value in still air)	23.0
θ_{JB} (°C/W)	7.30
θ_{JC} (°C/W)	0.10
Ψ_{JT} (°C/W)	0.02

14.2 Junction temperature estimation and PSIJT versus ThetaJC

The package thermal characterization parameter PSI_{JT} (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) than using the junction-to-case thermal resistance parameter $Theta_{JC}$ (θ_{JC}). The reason for this is that θ_{JC} is based on the assumption that all the power is dissipated through the top surface of the package case. In actual applications, however, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account the power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is: $T_J = T_T + P \times \psi_{JT}$

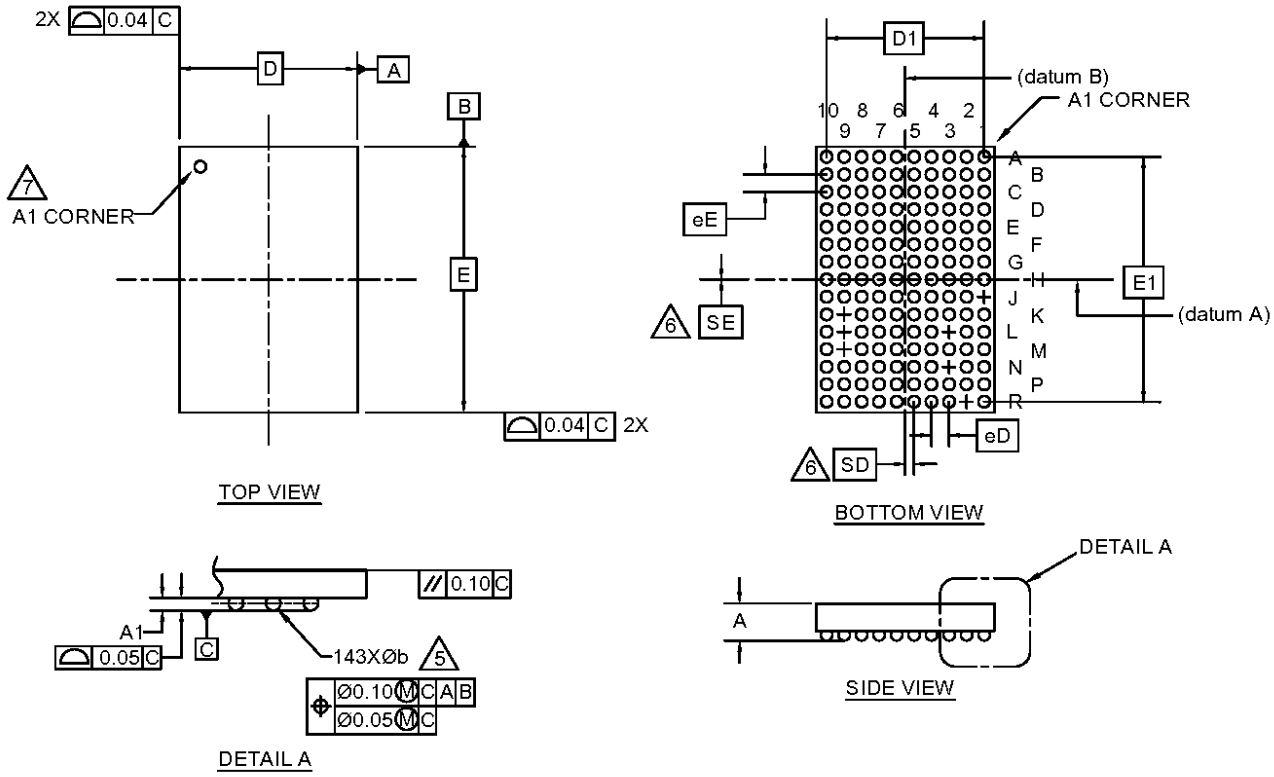
Where,

- T_J = Junction temperature at steady-state condition (°C)
- T_T = Package case top center temperature at steady-state condition (°C)
- P = Device power dissipation (Watts)
- Ψ_{JT} = Package thermal characteristics; no airflow (°C/W)

14.3 Environmental characteristics

For environmental characteristics data, see Table 18.

14.4 Package diagram



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.45
A1	0.14	-	-
D	3.57 BSC		
E	5.32 BSC		
D1	3.15 BSC		
E1	4.90 BSC		
MD	10		
ME	15		
N	143		
Ø b	0.18	0.23	0.28
eD	0.35 BSC		
eE	0.35 BSC		
SD	0.175 BSC		
SE	0.00 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
7. A1 CORNER TO BE IDENTIFIED BY LASER MARK
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : N/A.

002-33373 *D

Figure 17 Package outline, 143-ball WLBGA 3.57 × 5.32 × 0.45 mm (0.35 mm ball pitch)

14.5 Tape, reel and packing specification

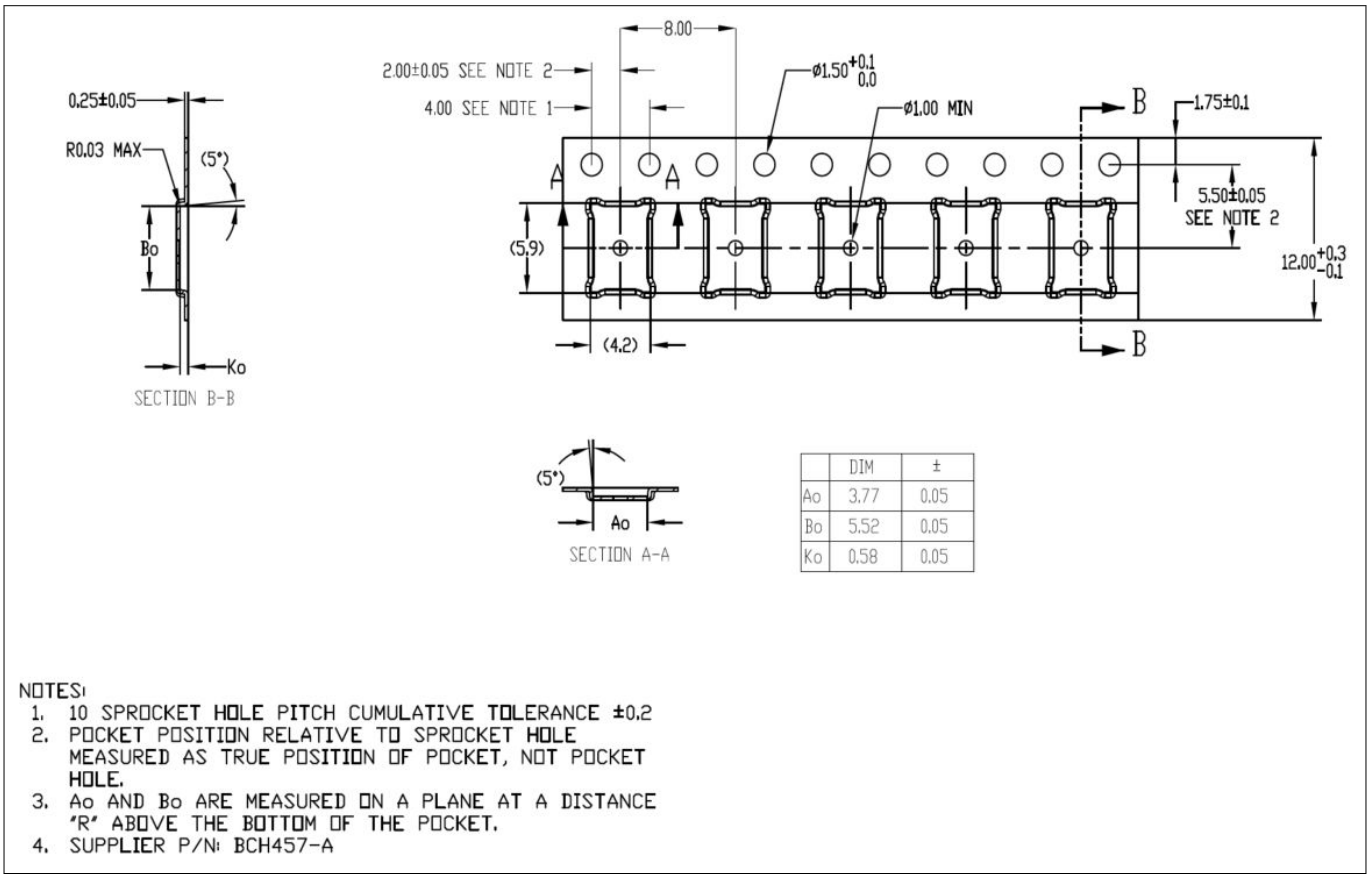


Figure 18 Tape WLBGA

15 Ordering information

Table 39 Ordering information

Product	Package	Description	Operating ambient temperature
CYW55310IUBGT	143-ball WLBGA (3.57 mm × 5.32 mm × 0.35 mm pitch)	Bluetooth®/Bluetooth® LE 6.0 tape and reel	-40°C to 85°C

Acronyms

Acronym	Description
AES	Advanced Encryption Standard
BDR	basic data rate
BLE	Bluetooth® Low Energy
C	celsius
Codec	coder decoder
Coex	coexistence
dB	decibel
dBm	decibel milliwatts
DSSS	direct sequence spread spectrum
EDR	Enhanced Data Rate
EIRP	effective isotropic radiated power
HCI	host controller interface
HE	high efficiency
HFP	Hands-Free profile
I2S	inter-IC sound
IEEE	Institute of electrical and electronics engineers
Kbps	kilobits per second
LC3	Low Complexity Communication Codec
LE	Low Energy
LNA	low-noise amplifier
LTE	long term evolution
MAC	medium access controller
Mbps	mega-bits per second
MCS	Modulation and coding scheme
PA	power amplifier
PCM	pulse code modulation
PDM	pulse density modulation
PHY	physical layer
QOS	Quality of service
RIFS	Reduced Interframe Space
ROM	read-only memory
RTS	request-tro-send
SRAM	serial random access memory
TDM	time division multiplexing

Acronyms

Acronym	Description
TKIP	temporal key integrity protocol
UART	universal asynchronous receiver transmitter
WLBGA	Wafer-level Ball Grid Array

Revision history

Document revision	Date	Description of changes
**	2023-02-01	Initial release
*A	2025-12-17	Updated the following: • Figure 1 • Overview • Power supplies and power management • Frequency references • Bluetooth® subsystem overview • Bluetooth® Baseband Core (BBC) • Microprocessor and memory unit for Bluetooth® • Bluetooth® peripheral transport units • Pinout and signal descriptions • DC characteristics • Bluetooth® RF specifications • Internal regulator electrical specifications • System power consumption • Power-up sequence and timing • Package information
*B	2026-04-08	Updated the following: • Description • Features • Overview • Bluetooth® subsystem overview • Features • Absolute maximum ratings • Environmental ratings

Trademarks

The Bluetooth® word mark and logos are registered trademarks owned by Bluetooth® SIG, Inc., and any use of such marks by Infineon is under license.

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2026-04-08

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference
IFX-eoy1721116335695

Important notice

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Warnings

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.