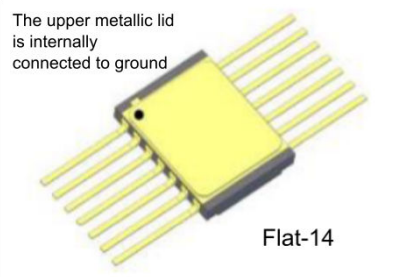
RHFAHC00

Datasheet

Rad-hard, quad high-speed NAND gate



Product status link
RHFAHC00

Features

- 1.8 V to 3.3 V nominal supply
- 3.6 V max. operating
- 4.8 V AMR
- Very high-speed: propagation delay of 3 ns maximum guaranteed
- Pure CMOS process
- CMOS output
- Ultra-low power
- 300 krad TID targeted
- No SEL at 125 MeV.cm^2/mg
- No SEL at 62.5 MeV.cm^2/mg
- SMD : 5962F18202
- Mass : 0.55 g

Applications

- Oscillators in space applications
- FPGA
- Microcontrollers

Description

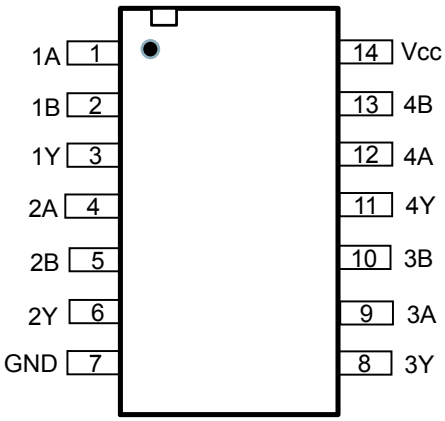
The RHFAHC00 device is a very high-speed pure CMOS quad 2-input NAND gate, designed for radiation hardness and characterized in total ionization dose (TID) and single event effect (SEE).

It is available in die-form and in hermetic ceramic Flat 14-lead screened as per MIL-PRF-38535 to comply with the needs of space applications. It can work from -55 °C to +125 °C ambient temperature.

1 Pin description

1.1 Pin description

Figure 1. Pin description



Note: Pin 7 (GND) is electrically connected to the metallic lid.

Figure 2. Schematic

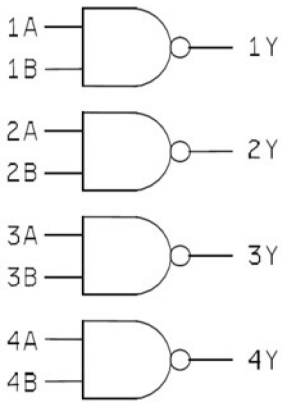


Table 1. Truth table

Inputs		Outputs
mA	mB	mY
L	L	H
H	L	H
L	H	H
H	H	L

Note: H = high voltage level; L= low voltage level. This truth table is functionally tested with a square signal of 150 MHz between 0 V (low input level) and Vcc (high input level), from 1.65 V to 3.6 V power supply, from -55 °C to 125 °C ambient temperature.

2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameters	Value	Units
V_{cc} (1)	Maximum power supply between V_{cc} and GND	-0.3 to 4.8	V
T_{stg}	Maximum temperature storage	-65 to +150	°C
T_j	Maximum junction temperature	+150	°C
R_{thjc} (2)	Junction-to-case thermal resistance	22	°C/W
R_{thja}	Junction-to-ambient thermal resistance	125	°C/W
V_i	Max. voltage on any pin	-0.3 to V_{cc}+0.3 (and 4.8 V max.)	V
I_i	Max. input current at any pin	±10	mA
I_{out}	DC output diode current	±50	mA
ESD	HBM on all pins (human body model)	4 k	V
	CDM on all pins (charged device model)	1 k	V

1. *All voltages refer to ground level.*
2. *Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on outputs.*

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 3. Operating conditions

Symbol	Parameters	Min.	Max.	Units
V_{cc}	Supply voltage	1.65	3.6	V
V_{IN}	Input voltage	0	V_{cc}	V
Δt/Δv	Minimum input rise of fall rate	10		ns/V
T_{amb}	Ambient temperature range	-55	+125	°C

3 Electrical characteristics

T_{amb} = -55 °C to +125 °C, unless otherwise specified.

Table 4. DC electrical characteristics

Symbol	Parameters	Test conditions	V_{cc} (V)	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage		1.65	1			V
			2.3	1.7			V
			3.0	2			V
V_{IL}	Low level input voltage		1.65			0.5	V
			2.3			0.7	V
			3.0			0.8	V
I_{IL}	Input leakage current low	V_{in} = 0 V	1.8			-0.1	µA
			2.5			-0.1	µA
			3.3			-0.1	µA
I_{IH}	Input leakage current high	V_{in} = Vcc-0.3 V	1.8			0.1	µA
			2.5			0.1	µA
			3.3			0.1	µA
I_{CCH}	Quiescent current, output high	V_{in}=V_{cc} or GND I_{out} = 0 A	3.3			50	µA
I_{CCL}	Quiescent current, output low	V_{in} = V_{cc} or GND I_{out} = 0 A	3.3			50	µA
C_{in}	Input capacitance(1)	f = 1 MHz, T_{amb} = 25 °C				2	pF
V_{OH}	High level output voltage	I_{OH}= -2 mA	1.65	1.2			V
			2.3	1.7			V
			3.0	2.4			V
		I_{OH}= -100 uA	1.65	1.45			V
			2.3	2.1			V
			3.0	2.8			V
V_{OL}	Low level output voltage	I_{OL}= +2 mA	1.65			450	mV
			2.3			430	mV
			3.0			400	mV
		I_{OL}= +100 uA	1.65			200	mV
			2.3			200	mV
			3.0			200	mV

1. *Guaranteed by design and characterization.*

Table 5. AC electrical characteristics

Symbol	Parameters	Test conditions	V_{cc} (V)	Min.	Typ.	Max.	Unit
C_{pd}	Power dissipation capacitance $C_{pd} = I_{ccrms}/(V_{cc}*F)$ (1)(2)	F=1 MHz, Load=10 pF	1.8			5	pF
			3.3			7	
T_{phl}	Propagation delay mA or mB to mY	Load=10 pF to GND	1.8	1.5		5.5	ns
			2.5	1.2		3.5	
			3.3	1		3	
T_{plh}	Propagation delay mA or mB to mY		1.8	1.5		5.5	ns
			2.5	1.2		3.5	
			3.3	1		3	
T_r	Output rise time		1.8		1.9		ns
			2.5		1.4		
			3.3		1.3		
T_f	Output fall time		1.8		1.9		ns
			2.5		1.4		
			3.3		1.3		

1. *Guaranteed by design and characterization.*
2. *Power dissipation capacitance (C_{pd}) determines both the power consumption (P_D) and dynamic current consumption (I_S). Where: $P_D = (C_{pd} + C_{Load})\ (V_{CC} \times V_{CC})\ x\ f + (I_{CC} \times V_{CC})$ $I_S = (C_{pd} + C_{Load})\ V_{CC}\ x\ f + I_{CC}$, where f is the frequency of the input signal and C_{Load} is the external output load capacitance.*

4 Radiations

Total dose (MIL-STD-883 TM 1019):

The products guaranteed in radiation within the RHA QML-V system fully comply with the MIL-STD-883 TM 1019 specifications.

The RHFAHC00 is RHA QML-V, tested and characterized in full compliance with the MIL-STD-883 specifications, between 50 and 300 rad/s only (full CMOS technology).

All parameters, provided in Table 4. DC electrical characteristics and Table 5. AC electrical characteristics, apply to both pre- and post-irradiation, as follows:

- All tests are performed in accordance with MIL-PRF-38535 and test method 1019 of MIL-STD-883 for total ionizing dose (TID)
- The initial characterization is performed in qualification only on both biased and unbiased parts
- Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification

Heavy-ions

The behavior of the product when submitted to heavy-ions is not tested in production. Heavy-ion trials are performed on qualification lots only.

Table 6. Radiation

Type	Characteristics	Value	Unit
TID(1)	High-dose rate (50 rad(Si)/s) and low-dose rate (0.086 rad(Si)/s)	300	krad
Heavy-ions	SEL(2) immune up to: (with a particle angle of 60 ° at 125 °C) and a fluence of 1e+7 cm^{-2})	125	MeV.cm²/mg
	SEL immune up to: (with a particle angle of 0 ° at 125 °C) and a fluence of 1e+7 cm^{-2})	62.5	
	SET(3) immune up to: (at 25 °C, and a fluence of 1e6 cm^{-2})		

1. *A total ionizing dose (TID) of 300 krad(Si) is equivalent to 3000 Gy(Si), (1 gray = 100 rad).*
2. *SEL: single event latch-up.*
3. *SET: single event transient*

5 Test circuit for AC characteristics

Figure 3. Test configuration

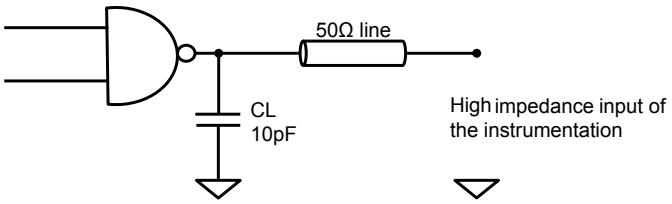


Figure 4. Timings

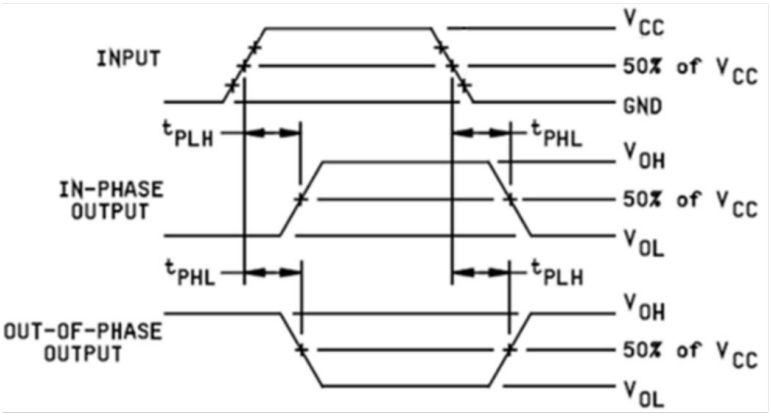
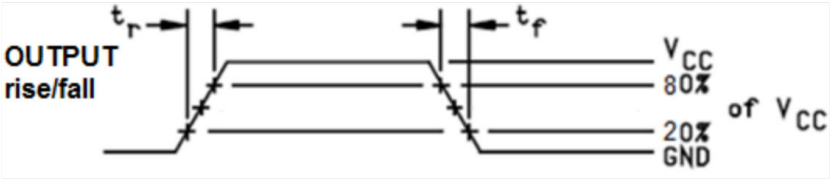


Figure 5. Output timings



Note:
1. *C_L = 10 pF or equivalent (includes probe and jig capacitance).*
2. *Timing parameters are tested at a minimum input frequency of 1 MHz.*
3. *The outputs are measured one at a time with one transition per measurement.*

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

6.1 Flat-14 package information

Figure 6. Flat-14 package outline

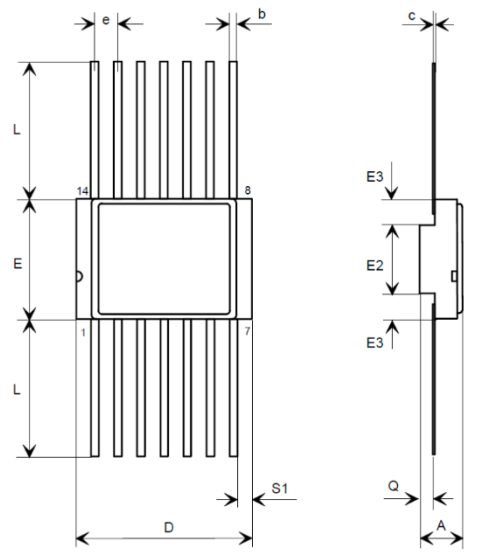


Table 7. Flat-14 package mechanical data

Ref.	Drawing mm			Drawing inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.31		2.72	.091		.107
b	0.38		0.48	.015		.019
c	0.10		0.18	.004		.007
D	9.27		9.73	.365		.383
E	6.19		6.50	.244		.256
E2		3.68			.145	
E3	0.76			.030		
e		1.27			.050	
L	6.86		7.62	.250		.300
Q	0.66		1.14	.026		.045
S1	0.13			.005		

7 Ordering information

Table 8. Order code

Order code	SMD[1]	Quality level	Package	Lead finish	Marking[2]	Packing
RH-AHC00K1	-	Engineering model	Flat-14 (grounded lid)	Gold	RH-AHC00K1	Tray
RHFAHC00K01V	5962F18202	QML-V flight			5962F1820201VXC	

1. *Standard microcircuit drawing.*
2. *Specific marking only. Complete marking includes the following:*
   - *ST logo*
   - *Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)*
   - *Country of origin (FR = France)*

Note: Contact your ST sales office for information about the specific conditions for products in die form.

Other information

Date code:

The date code is structured as engineering model: EM xyywwz

Where:

x = 3 (EM only), assembly location Rennes (France)

yy = last two digits of the year

ww = week digits

z = lot index of the week

Product documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in the table below.

The certificate of conformance is provided on paper whatever the quality level. For QML parts, complete documentation, including the certificate of conformance, is provided on a CDROM.

Table 9. Product documentation

Quality level	Item
Engineering model	Certificate of conformance including : Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code Reference to ST datasheet Reference to TN1181 on engineering models ST Rennes assembly lot ID
QML-V Flight	Certificate of Conformance including: Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code

Quality level	Item
QML-V Flight	Serial numbers Group C reference Group D reference Reference to the applicable SMD ST Rennes assembly lot ID
	Quality control inspection (groups A, B, C, D, E)
	Screening electrical data in/out summary
	Precap report
	PIND (particle impact noise detection) test
	SEM (scanning electronic microscope) inspection report
	X-ray plates

Revision history

Table 10. **Document revision history**

Date	Version	Changes
28-Feb-2018	1	Initial release.
16-Jul-2018	2	Updated Table 2. Absolute maximum ratings, Table 3. Operating conditions, Table 4. DC electrical characteristics, Table 5. AC electrical characteristics, Table 6. Radiation, Table 8. Order code. Minor text changes throughout the document.
13-Apr-2026	3	Changed packing from Strip pack to Tray in Table 8.

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