Product Change Notification: SYST-11TGLL206

Date:

20-Jul-2026

Product Category:

8-Bit Microcontrollers

Notification Subject:

PIC16F18114/15/24/25/44/45 Silicon Errata and Data Sheet Clarifications

Affected CPNs:

SYST-11TGLL206_Affected_CPN_07202026.pdf
SYST-11TGLL206_Affected_CPN_07202026.csv

Notification Text:

SYST-11TGLL206

Microchip has released a new Document for the PIC16F18114/15/24/25/44/45 Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at **PIC16F18114/15/24/25/44/45 Silicon Errata and Data Sheet Clarifications**.

Notification Status: Final

Description of Change:

Updated data sheet revision letter to ‘D’; added silicon issues 1.7.1, 1.8.1, and 1.9.1.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 20 Jul 2026

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC16F18114/15/24/25/44/45 Silicon Errata and Data Sheet Clarifications

Please contact your local **Microchip sales office** with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC16F18114-E/MD

PIC16F18114-E/P

PIC16F18114-E/SN

PIC16F18114-I/MD

PIC16F18114-I/P

PIC16F18114-I/SN

PIC16F18114T-I/MD

PIC16F18114T-I/SN

PIC16F18115-E/MD

PIC16F18115-E/MDVAO

PIC16F18115-E/P

PIC16F18115-E/SN

PIC16F18115-I/MD

PIC16F18115-I/P

PIC16F18115-I/SN

PIC16F18115T-E/MDVAO

PIC16F18115T-I/MD

PIC16F18115T-I/SN

PIC16F18124-E/7N

PIC16F18124-E/P

PIC16F18124-E/SL

PIC16F18124-E/ST

PIC16F18124-E/STVAO

PIC16F18124-I/7N

PIC16F18124-I/P

PIC16F18124-I/SL

PIC16F18124-I/ST

PIC16F18124T-E/STVAO

PIC16F18124T-I/7N

PIC16F18124T-I/SL

PIC16F18124T-I/ST

PIC16F18125-E/7N

PIC16F18125-E/7NVAO

PIC16F18125-E/P

PIC16F18125-E/SL

PIC16F18125-E/SLVAO

PIC16F18125-E/ST

PIC16F18125-I/7N

PIC16F18125-I/P

PIC16F18125-I/SL

PIC16F18125-I/ST

PIC16F18125T-E/7NVAO

PIC16F18125T-I/7N

PIC16F18125T-I/SL

PIC16F18125T-I/ST

PIC16F18144-E/6N

PIC16F18144-E/P

PIC16F18144-E/SO

PIC16F18144-E/SS

PIC16F18144-E/SSVAO

PIC16F18144-I/6N

PIC16F18144-I/P

PIC16F18144-I/SO

PIC16F18144-I/SS

PIC16F18144T-E/SSVAO

PIC16F18144T-I/6N

PIC16F18144T-I/SO

PIC16F18144T-I/SS

PIC16F18145-E/6N

PIC16F18145-E/P

PIC16F18145-E/SO

PIC16F18145-E/SS

PIC16F18145-I/6N

PIC16F18145-I/P

PIC16F18145-I/SO

PIC16F18145-I/SS

PIC16F18145T-I/6N

PIC16F18145T-I/SO

PIC16F18145T-I/SS

PIC16F18114/15/24/25/44/45 Silicon Errata and Data Sheet Clarifications

PIC16F18114/15/24/25/44/45

Product Page Links

Introduction

The PIC16F18114/15/24/25/44/45 devices that you have received conform functionally to the current device data sheet (DS40002404**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC16F18114/15/24/25/44/45 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID				
		B0	B2	B3	B4	D2
PIC16F18114	0x3107	0xA040	0xA042	0xA043	0xA044	0xA0C2
PIC16F18115	0x310C	0xA040	0xA042	0xA043	0xA044	0xA0C2
PIC16F18124	0x3108	0xA040	0xA042	0xA043	0xA044	0xA0C2
PIC16F18125	0x310D	0xA040	0xA042	0xA043	0xA044	0xA0C2
PIC16F18144	0x3109	0xA040	0xA042	0xA043	0xA044	0xA0C2
PIC16F18145	0x310E	0xA040	0xA042	0xA043	0xA044	0xA0C2

Important: Refer to the **Device/Revision ID** section in the device data sheet for more detailed information on Device Identification and Revision IDs for your specific device.

Silicon Issue Summary

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions				
				B0	B2	B3	B4	D2
Analog-to-Digital Converter with Computation (ADCC)	Double Sample Conversions	1.1.1	An unexpected acquisition time is added between the first and second conversions	X				
	Acquisition Time	1.1.2	Acquisition time cannot be changed through either the ADACQ or ADPRE registers	X	X			
Comparator (CMP)	Comparator 2	1.2.1	Comparator 2 is not available on 8-pin devices	X				
Host Synchronous Serial Port (MSSP)	I^2C Start and Stop Interrupt Function	1.3.1	A race condition can cause the Start and/or Stop flags to be set when I^2C is enabled	X				
Configuration Words (CONFIG)	Sleep	1.4.1	Waking from Sleep may cause unexpected behavior	X				
Digital-to-Analog Converter (DAC)	DAC Auto Enable	1.5.1	Mid-band voltage spike at code 128 may occur when $\overline{\text{DACAUTOEN}}$ is enabled and the application is incrementing the DACxDATL register from 127 to 129	X	X			
Fixed Voltage Reference (FVR)	ADC Buffer	1.6.1	Power-down current (I_{PD}) for the ADC FVR Buffer may be higher than the current data sheet limits			X		
Charge Pump	CPON	1.7.1	The CPON Bits Incorrectly Default to OFF Mode	X	X	X	X	X
Timer1	Timer1 Gate Source	1.8.1	Changing the Timer1 Gate Source May Cause Unexpected Interrupts	X	X	X	X	
Capture/ Compare/PWM (CCP)	Compare Toggle Mode	1.9.1	CCP Compare Toggle Output Mode Does Not Work as Expected	X	X	X	X	X

Note: Only those issues indicated in the last column apply to the current silicon revision.

1. Silicon Errata Issues

NOTICE This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1. Module: Analog-to-Digital Converter with Computation (ADCC)

1.1.1. An Unexpected Acquisition Time is Added Between the First and Second Conversions

When enabling a Double Sample Conversion (DSEN = 1) with no precharge time (ADPRE = 0) and no acquisition time (ADACQ = 0), the maximum number of cycles of acquisition time is inserted prior to the second conversion. The first conversion will be performed as expected with no precharge time and no acquisition time. It is only between the first and second conversions where a maximum number of cycles of acquisition time are performed unexpectedly.

Work Around
Method 1:

Disable Double Sample Conversion (DSEN = 0) and perform two single conversions back to back.

Method 2:

If adding acquisition time is acceptable, then select no precharge time along with the desired acquisition time.

Affected Silicon Revisions

B0	B2	B3	B4	**D2**			
X							

1.1.2. Acquisition Time Cannot Be Changed through Either the ADACQ or the ADPRE Registers

ADC acquisition (sample) time cannot be modified by writing to either the ADPRE or ADACQ registers. Writes to the ADPRE or ADACQ registers will correctly delay the next conversion but will have no affect on increasing the actual sample time of the current conversion. For example, if the ADCRC is used as the clock source, the sample time will be nominally 3.33 µs, regardless of the values in either of the ADACQ or ADPRE registers.

Work around

There is essentially no work around for increasing the sample times via the ADPRE or ADACQ registers; however, there are various work arounds and/or techniques that can be implemented to acquire a more accurate ADC measurement.

- If the ADC is using the F_{OSC}, reducing the clock speed at the time of measurement will increase the overall sampling time.
  - Use the NOSC/NDIV bits of OSCCON1 to reduce the oscillator speed
  - Adjust the ADCLK divider value to reduce the oscillator speed
  - Switch the ADC clock to the ADCRC
- The source input impedance (R_S) directly effects the amount of time it takes to charge the C_{HOLD} capacitor. Reducing the input impedance to a minimum will help reduce the sample time needed for the ADC measurement.

Affected Silicon Revisions

B0	B2	B3	B4	**D2**			
X	X						

1.2. Module: Comparator (CMP)

1.2.1. Comparator 2 Is Not Available

Comparator 2 is not available on 8-pin devices.

Work around

None.

Affected Silicon Revisions

B0	B2	B3	B4	**D2**			
X							

1.3. Module: MSSP

1.3.1. The I²C Start and/or Stop Flags May Be Set When I²C Is Enabled

When I²C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I²C interrupts, if enabled.

Work Around

Use the following procedure to correctly detect the Start and Stop conditions:

1. Disable the Start and Stop conditions interrupt functions.
2. Enable the I²C module.
3. Wait 250 ns + six instruction cycles (F_{OSC}/4).
4. Clear the Start and Stop conditions interrupt flags.
5. Enable the Start and Stop conditions interrupt functions, if used.

```
SSPxCON3bits.SCIE = 0;          // Disable Start condition interrupt
SSPxCON3bits.PCIE = 0;          // Disable Stop condition interrupt
SSPxCON1bits.SSPEN = 1;         // Enable I2C
Delay();                        // Wait for 250 ns + 6 instruction cycles (Fosc/4)
PIRxbits.SSPxIF = 0;            // Clear the MSSP interrupt flag
SSPxCON3bits.SCIE = 1;          // Enable Start condition interrupt if used
SSPxCON3bits.PCIE = 1;          // Enable Stop condition interrupt if used
```

Affected Silicon Revisions

B0	B2	B3	B4	**D2**			
X							

1.4. Module: Configuration Words (CONFIG)

1.4.1. Waking from Sleep May Cause Unexpected Behavior

Waking from Sleep may cause unexpected behavior.

Work around

Do not use the `SLEEP` instruction. If clock switching is available and there is a need for reduced current consumption, switch to the slowest system clock.

Affected Silicon Revisions

B0	B2	B3	B4	**D2**			
X							

1.5. Module: Digital-to-Analog Converter (DAC)

1.5.1. Mid-band Voltage Spike at Code 128 May Occur When $\overline{\text{DACAUTOEN}}$ Is Enabled and the Application Is Incrementing the DACxDATL Register from 127 to 129

When the $\overline{\text{DACAUTOEN}}$ bit is enabled, a voltage glitch on the DACxOUT pin may occur at code 128 when the application is incrementing the DACxDATL register from 127 to 129 and the alternate DACxOUT pin is either tied to GND or V_{DD}. If the alternate pin is tied to V_{DD}, the glitch will be positive; if the pin is tied to GND, the glitch will be negative.

Work around

None.

Affected Silicon Revisions

B0	B2	B3	B4	**D2**			
X	X						

1.6. Module: Fixed Voltage Reference (FVR)

1.6.1. Power-down Current (I_{PD}) for the ADC FVR Buffer May Be Higher than the Current Data Sheet Limits

When using the ADC FVR Buffer as an ADC reference, the I_{PD} current may be higher than the current data sheet limits. The parameters for B3 silicon are as follows:

Param. No.	Sym.	Device Characteristics	Min.	Typ.†	Max. +85°C	Max. +125°C	Units	Conditions	
								V_{DD}	Note
D204	$I_{PD\_FVR\_BUF1}$	FVR Buffer 1 (ADC)	—	**171**	**420**	**485**	µA	3.0V	

Work around

None.

Affected Silicon Revisions

B0	B2	B3	B4	**D2**			
		X					

1.7. Module: Charge Pump (CP)

1.7.1. The CPON Bits Incorrectly Default to OFF Mode

The CPON bits incorrectly default to OFF mode (CPON = `00`) instead of AUTO mode (CPON = `01`) upon power-up or device Reset.

Work around

User software must configure the charge pump to operate in AUTO mode by writing '`01`' to the CPON bits of the CPCON register.

Affected Silicon Revisions

B0	B2	B3	B4	**D2**			
X	X	X	X	**X**			

1.8. Module: Timer1

1.8.1. Changing the Timer1 Gate Source May Cause Unexpected Interrupts

When a new value is written into the Timer1 Gate Source Select (GSS) bits of the TxGATE register, the TMRxGIF interrupt flag may be set unexpectedly. If the TMRxGIE bit is set, an unexpected interrupt will occur.

Work around

User software must clear the TMRxGIF bit immediately after writing the new value to the GSS bits.

Affected Silicon Revisions

B0	B2	B3	B4	**D2**			
X	X	X	X				

1.9. Module: Capture/Compare/PWM Module (CCP)

1.9.1. CCP Compare Toggle Output Mode Does Not Work as Expected

The CCP module's Compare Toggle Output Mode (MODE[3:0] = `'b0001`) does not work as expected. When the TMRx resource matches the value in the CCPRx registers, the output may toggle randomly or not at all.

Work Around

None

Affected Silicon Revisions

B0	B2	B3	B4	**D2**			
X	X	X	X	**X**			

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002404**D**):

Note:
Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1. None

There are no known data sheet clarifications as of this publication date.

3. Appendix A: Revision History

Doc. Rev.	Date	Comments
F	07/2026	Updated data sheet revision letter to 'D'; added silicon issues 1.7.1, 1.8.1, and 1.9.1.
E	01/2024	Added new silicon revision D2.
D	12/2023	Added new silicon revision B4.
C	08/2023	Added new silicon revision B3; updated data sheet revision letter to 'C'; added silicon issues 1.1.2, 1.5.1, and 1.6.1.
B	09/2022	Added new silicon revision B2; updated data sheet revision letter to 'B'; adding silicon issue 1.4.1.
A	03/2022	Initial release of this document.

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