Three-Phase Brushless Motor Gate Driver SBC

MCP8048/MCP8049

Description

The MCP8048/MCP8049 are Functional Safety Compliant Three-Phase Brushless Motor Gate Driver System Basis Chips (SBC) for brushless motor control, designed using advanced Silicon on Insulator (SOI technology). In combination with a microcontroller and six discrete power MOSFETs, the SBC forms a brushless DC motor control unit. The Gate Driver Units (GDU) are controlled independently through six dedicated parallel inputs. Charge pumps for low and high-side gate drive allow duty cycle operations from 0% to 100%. In addition, the SBC provides 5V and 3.3V low dropout voltage regulators, current-sensing operational amplifiers, an integrated Back-EMF (BEMF in the Block Diagram) detection module and a window watchdog. The microcontroller controls the MCP8048/MCP8049 using a Serial Peripheral Interface (SPI).

The MCP8049 is available in a 40-pin VQFN package, including two operational amplifiers. The MCP8048 is available in a 48-pin VQFN package and integrates three operational amplifiers and a physical LIN bus interface and the option to disable the LIN dominant timeout which allows PWM operation.

Naming Convention:

- MCP8048/MCP8049 refers to the all devices, with and without a LIN transceiver, with the option of disabling the TXD timeout timer
- MCP8049 are only the devices without LIN transceiver
- MCP8048 are only the devices with LIN transceiver, with the option to disable the TXD timeout timer

Features

General

- Power Supply Voltage Range From 3V to 42V
- Sleep (Deep Sleep) Mode With Maximum 20 µA Current Consumption With Full Wake-Up Capability (Local Wake-Up)
- 3.3V or 5V Microcontroller Interface
- Up to 4 MHz SPI Bus for Device Configuration and Register Access
- SPI Frame Error Detection
- Dedicated NIRQ Pin for MCU External Interrupt in Order to Report Events Directly
- Input-Output Reset Pin (NRES) With Variable Reset Length to Support a Wide Variety of Microcontrollers
- Selectable TXD Dominant Timeout Timer Disable for PWM Communication via LIN Transceiver (MCP8048)
- Available in AEC-Q100 Grade 0, High Temperature Range (H): -40°C to 150°C
- Packages: VQFN48, VQFN40 With Wettable Flanks and Exposed Pad, Both Have Moisture Sensitivity Level (MSL) 1

Motor Gate Driver Unit (GDU)

- VDH Motor Operating Voltage Range From 4.9V to 32V (Overvoltage Lockout Level)
  - VS Undervoltage
  - VDH Overvoltage Lockout Selectable

- Individual Driving of Six External NMOS Transistors or Complementary Driving of Three Half-Bridges With Three Pairs of PWM Input Pins
- Maximum Switching Frequency of 50 kHz With 100 nC Gate Charge per MOSFET
- Charge Pumps for Supporting Crank Pulse Voltage Operation and 100% PWM Duty Cycle Control
- MOSFET VGS Undervoltage Monitoring, Configurable Undervoltage Lockout Level
- MOSFET VDS Monitoring, Configurable Short-Circuit Detection Levels
- Cross-Conduction Protection Timer
- Programmable Deadtime Insertion or Adaptive Deadtime Control
- Failure Detection Blanking Time for All Protection Features
- Configurable Fault Filter Times for VGSUV, ILIM and SCP

Current Sense Amplifier (CSA)

- Three Integrated High-Performance CSA With Configurable Gain and Output Offset
- One Advanced Power Stage Current Limitation Using Op Amp Output and Integrated DAC

Back-EMF Detection

- Back-EMF Feedback Detector Including Motor Neutral Point Emulation

Voltage Regulators

- VDD1: 5V/3.3V, 100 mA
  - ±2% Accuracy
  - Foldback Short-circuit Limit (I_{VDD1} + I_{VDD2} = 105 - 135 mA)
  - Short-circuit Protection
  - Undervoltage Detection
  - Overvoltage Protection and Detection
- VDD2: 3.3V, 70 mA
  - ±2% Accuracy
  - Current Limitation: 75 mA
  - Short-circuit protection
  - Undervoltage detection
  - Overvoltage Protection and Detection
- High-Voltage Output INH for Controlling an External Component, like a Voltage Regulator (VDD2 Not Available in This Variant)

LIN Transceiver

- Compliant With IEC 62228-2:2016 and SAE J2602-2:2019 and Conformance According to ISO 17897-4:2025
- TXD Dominant Timeout Function
- Disabling of TXD Dominant Timeout Function
- LIN Bus Short-Circuit Protection Against GND and Battery
- LIN Bus Remote Wake-Up

Watchdog

- Window and Timeout Modes
- Optional Cyclic Wake-Up in Timeout Mode
- Configurable Period and Reset Pulse Length
- Limp Home (LH): High-Voltage Failure Output

Functional Safety Support

- ISO 26262:2018 Functional Safety: ASIL B Compliant
- IEC 61508:2010 Functional Safety: SIL 2 Compliant

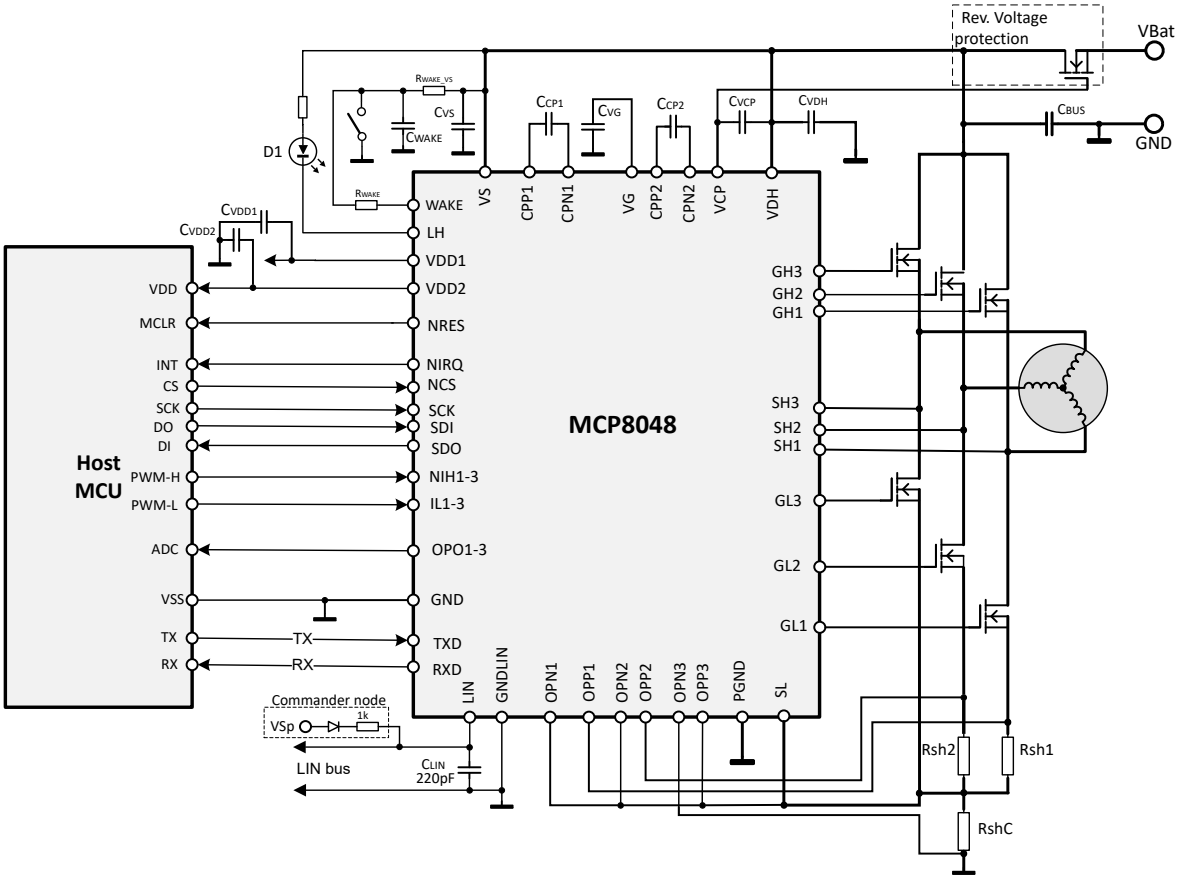
Applications

- Automotive — Fuel, Water or Oil Pumps, Cooling Fans, Roots Blowers, Steering, Sunroof, Trunk Opening, Seat Adjustment
- Home Appliances Using BLDC Motor Control
- Power Tool Motors
- Hobby Aircraft, Boats, Drones or Vehicles

1. Typical Application Circuit(s)

This typical application shows a two-shunt system configuration and a third shunt as a current limit sensor.

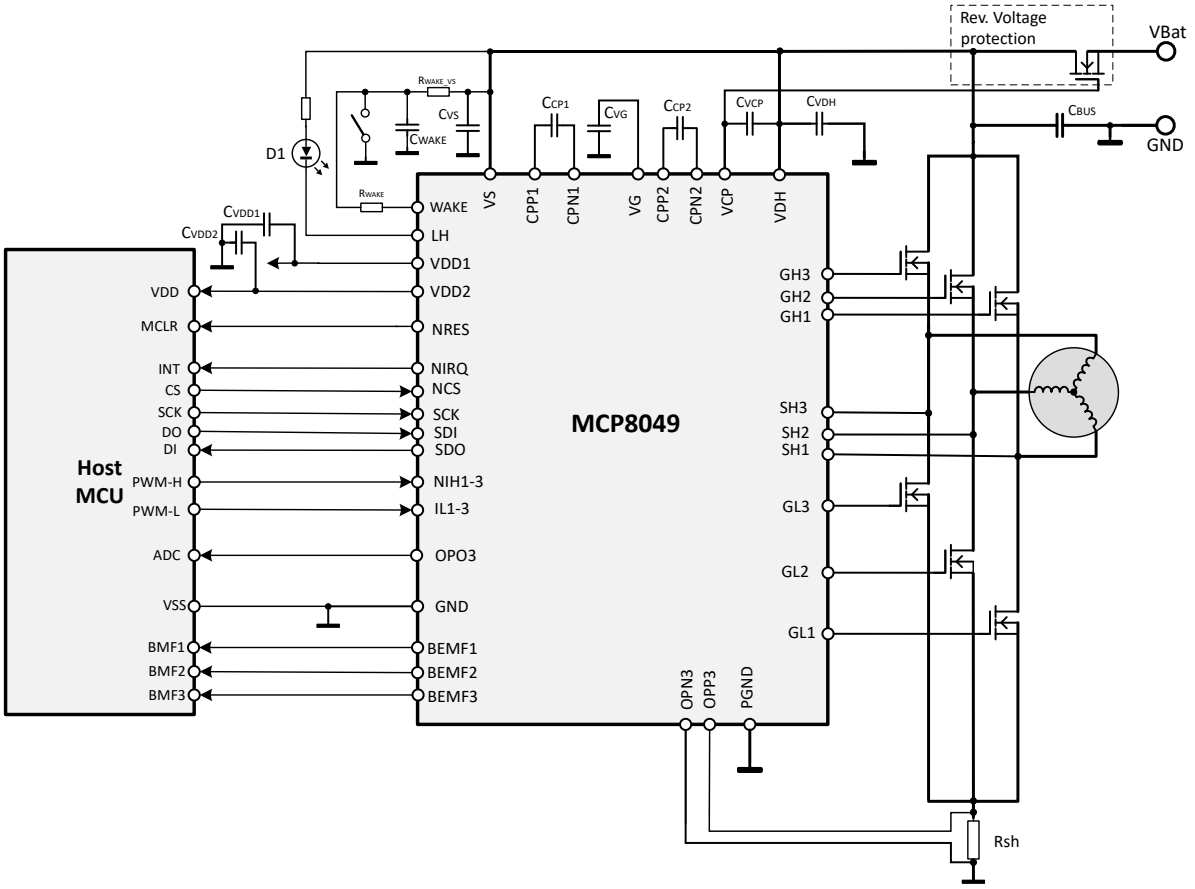
Figure 1-1. Typical Application Schematic: MCP8048



- R_{WAKE} = 2,7kΩ
- C_{WAKE} = 100nF
- R_{WAKE_VS} = 10kΩ
- C_{VDD1} = C_{VDD2} = 2.2µF
- C_{VS} = 10uF || 100nF
- C_{VDH} = 4.7uF || 100nF
- C_{CP1} = 330nF
- C_{CP2} = 220nF
- C_{VG} = C_{VCP} = 3.3µF

The typical application shows a Back-EMF system configuration for a 6-step trapezoidal application and a shunt as a current limit sensor. The application circuit is also suited for a single-shunt FOC application, with the current limitation functionality of the single shunt and detection of wind milling via the Back-EMF sampler. The charge pump output (VCP) controls the reverse polarity protection N-channel MOSFET.

Figure 1-2. Typical Application Schematic: MCP8049



- R_{WAKE} = 2.7 kΩ
- C_{WAKE} = 100 nF
- R_{WAKE_VS} = 10 kΩ
- C_{VDD1} = C_{VDD2} = 2.2 µF
- C_{VS} = 10 µF || 100 nF
- C_{VDH} = 4.7 µF || 100 nF
- C_{CP1} = 330 nF
- C_{CP2} = 220 nF
- C_{VG} = C_{VCP} = 3.3 µF

2. Product Family

The name, features and package types of each device are listed in the following table. All devices integrate six dedicated parallel gate drivers and a Back-EMF comparator.

Table 2-1. MCP8048/MCP8049 Family Overview

Product Name	VDD1 LDO Note 1	VDD2 LDO Note 1	INH	LIN	Disable TXD	OpAmps / OpAmps+ Back-EMF Note 2	OpAmp Output Rail, MCU Interface Voltage [VIO]	Package
MCP8048-5050	5V 100 mA	3.3V 70 mA		x		3 / 2 +1	5V	48-VQFN
MCP8048-3333	3.3V 100 mA		x	x		3 / 2 + 1	3.3V	48-VQFN
MCP8048-5033	5V 100 mA	3.3V 70 mA		x		3 / 2 + 1	3.3V	48-VQFN
MCP8049-5050	5V 100 mA	3.3V 70 mA				2 / 1 + 1	5V	40-VQFN
MCP8049-3333	3.3V 100 mA		x			2 / 1 + 1	3.3V	40-VQFN
MCP8049-5033	5V 100 mA	3.3V 70 mA				2 / 1 + 1	3.3V	40-VQFN

Notes:

1. Sum current (I_{VDD1} + I_{VDD2}) maximum 100 mA
2. Selectable via SPI:
   MCP8048: Three OpAmps or Two OpAmps plus One Back-EMF sampler
   MCP8049: Two OpAmps or One OpAmp plus One Back-EMF sampler

3. Block Diagram

Figure 3-1. MCP8048-5050, MCP8048-5033

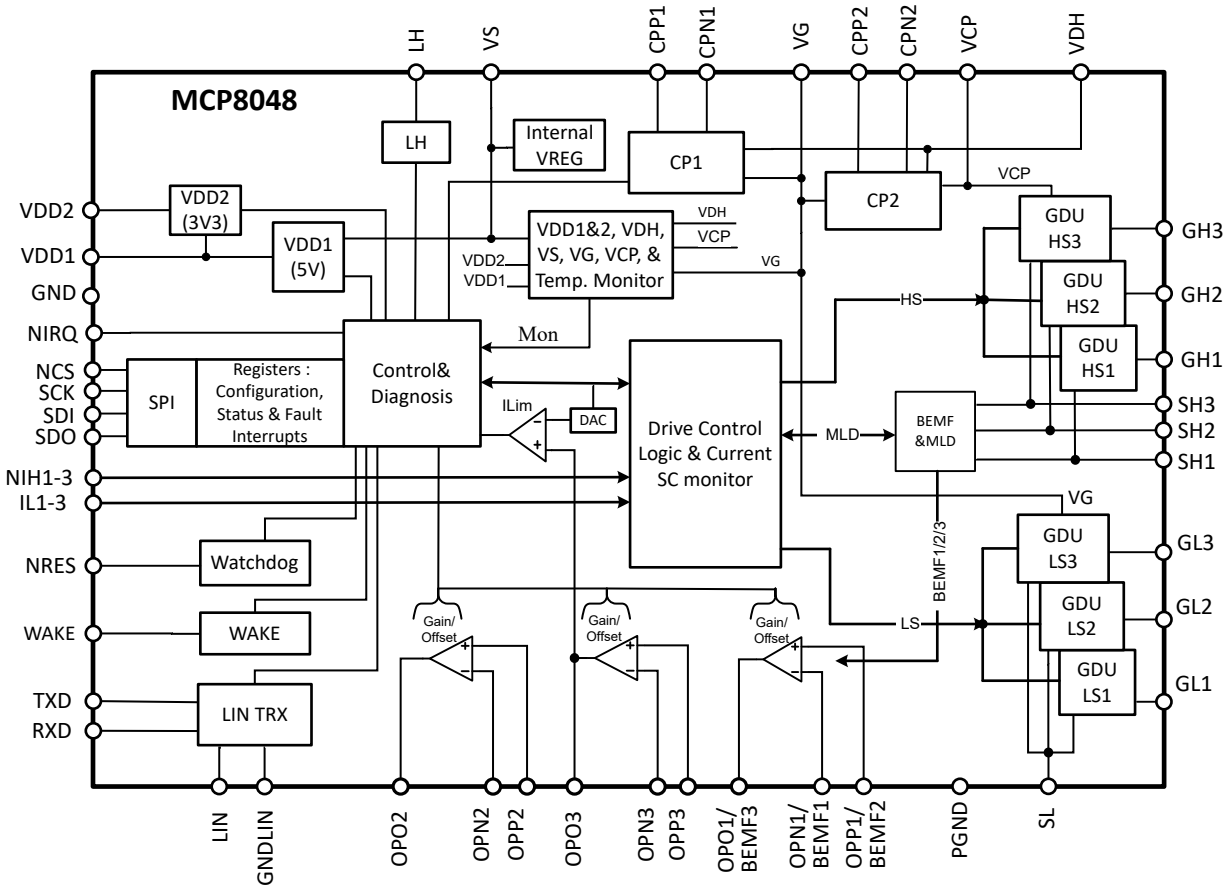


Figure 3-2. MCP8049-5050, MCP8049-5033

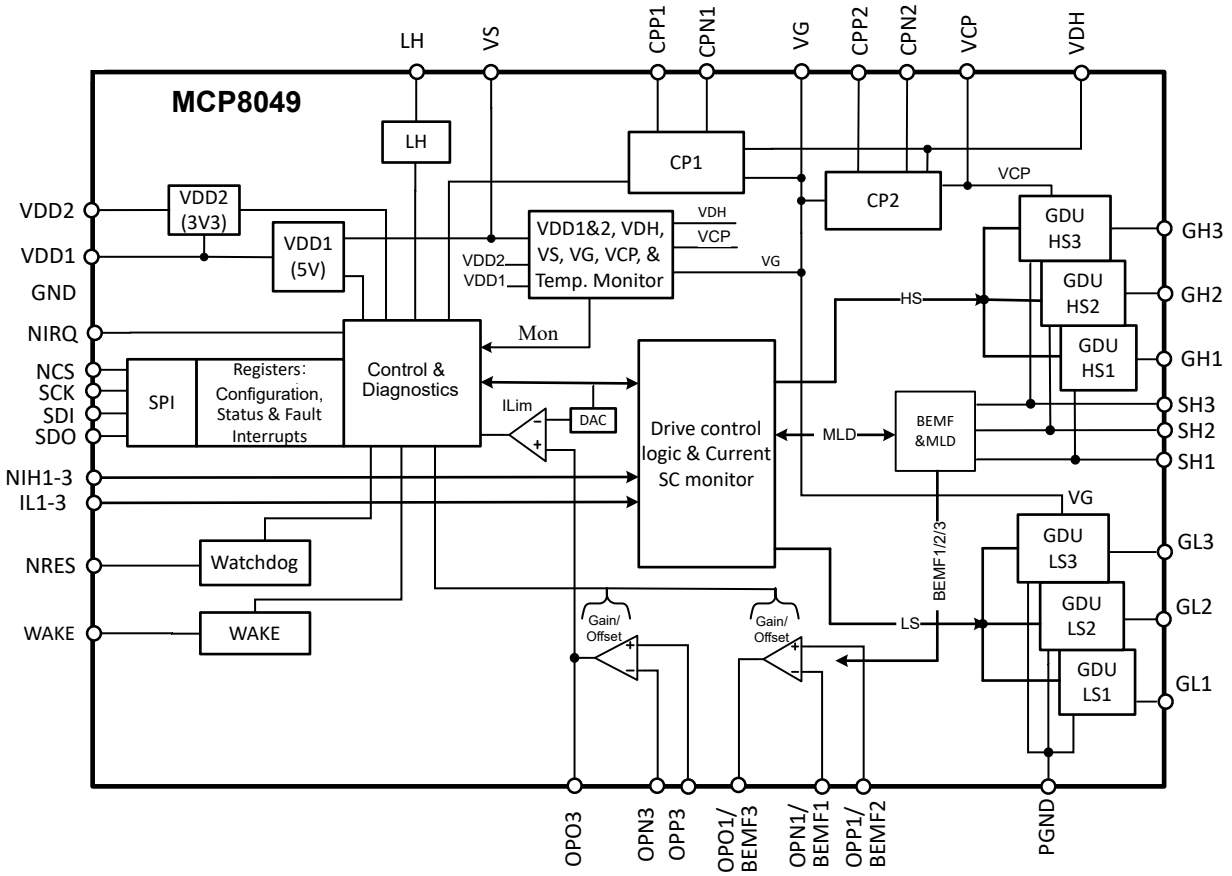


Figure 3-3. MCP8048-3333

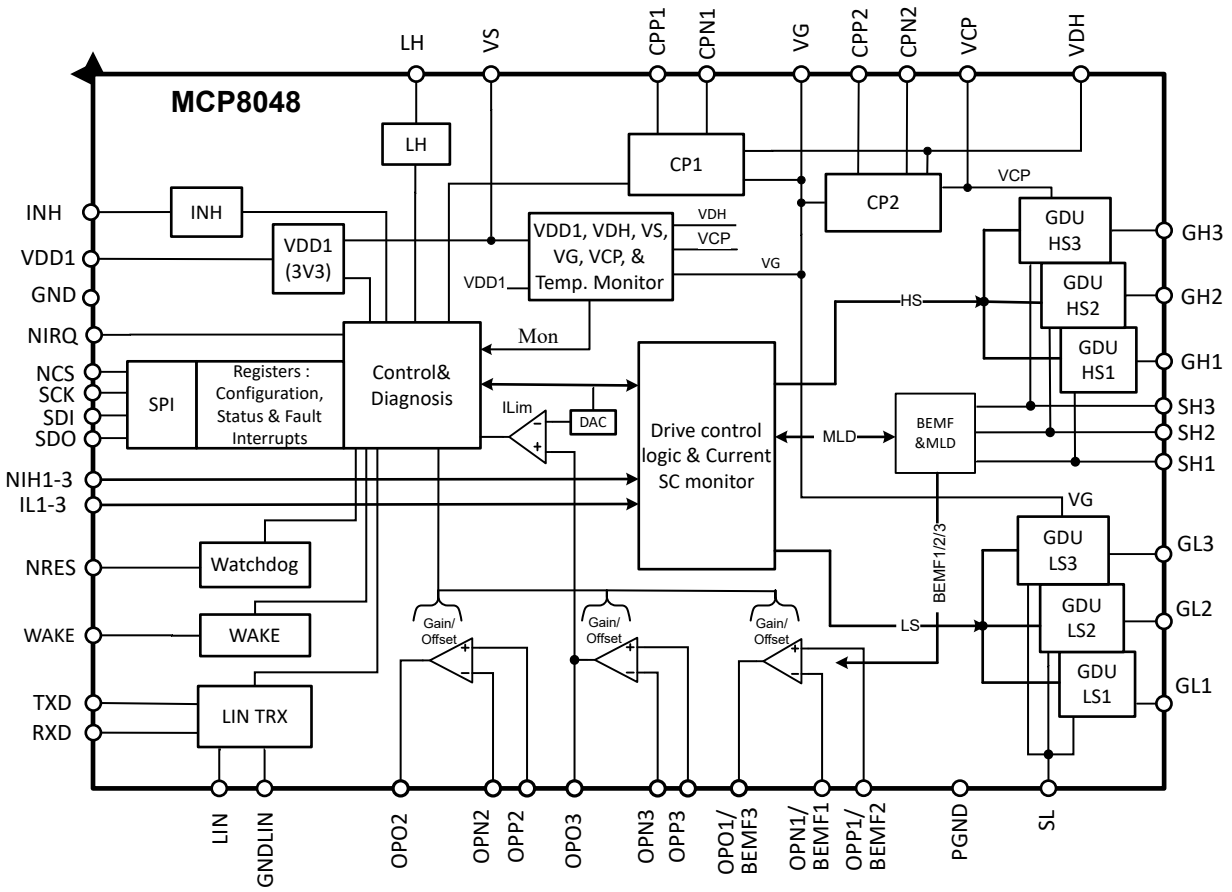
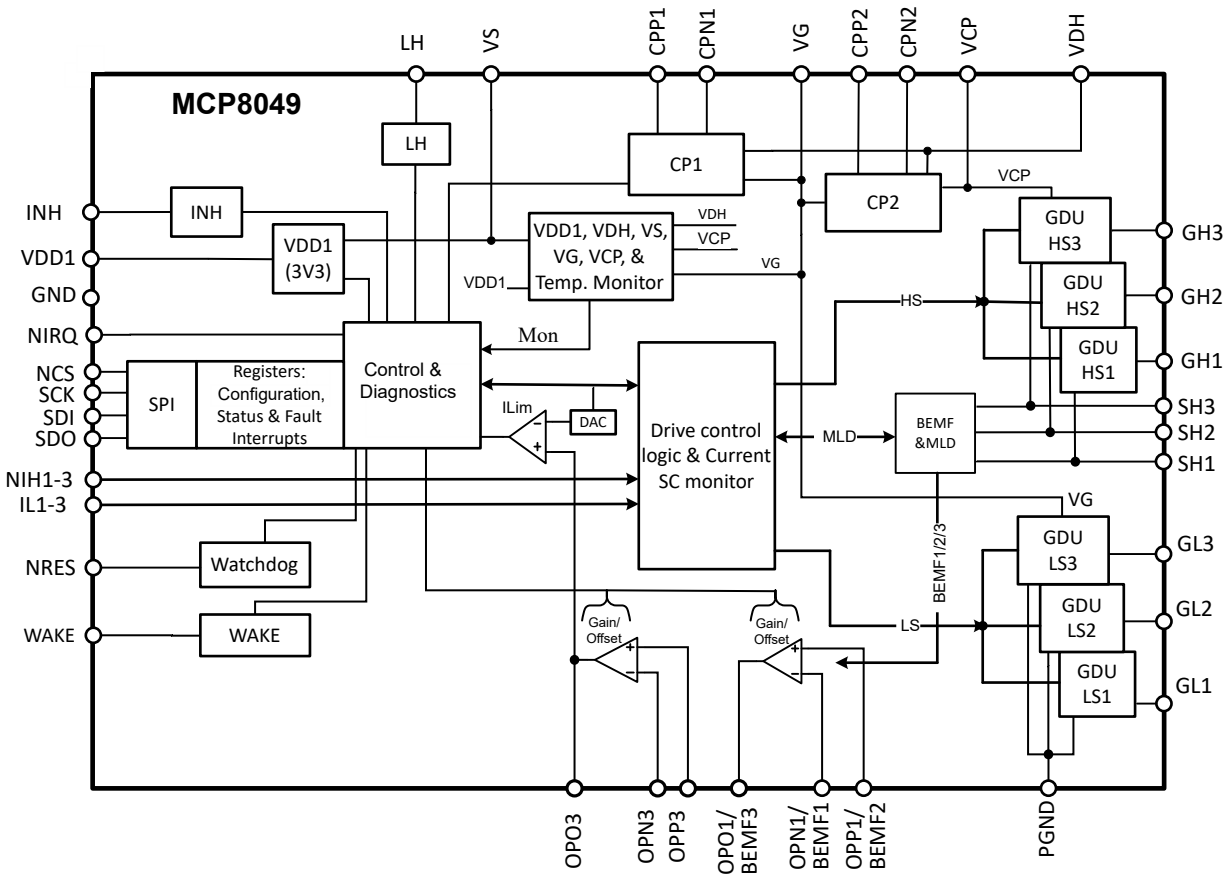


Figure 3-4. MCP8049-3333



4. Pin Configuration

Pin Name	48 Pin	40 Pin	Pin Description
VDD2/INH	1	1	70 mA, 3.3V supply voltage/INH is the high-voltage output designed to control an external voltage regulator
LH	2	2	Limp Home – High-voltage failure output, Open drain
VS	3	3	Battery supply pin
WAKE	4	4	High-voltage input for local wake-up
GNDLIN	5	—	LIN transceiver ground
LIN	6	—	LIN bus interface
GND	7	5	LDO and analog ground
SL	8	—	Low-side MOSFET source terminal, in 40 pin package internally connected to PGND
VG	9	6	12V gate drive regulator/charge pump 1 output
GL1	10	7	Gate driver output for low-side MOSFET, phase 1
GL2	11	8	Gate driver output for low-side MOSFET, phase 2
GL3	12	9	Gate driver output for low-side MOSFET, phase 3
CPP1	13	10	Charge pump 1 flying capacitor positive connection 1
CPN1	14	11	Charge pump 1 flying capacitor negative connection 1
VDH	15	12	Supply for VG and charge pump, high-side drain-source voltage monitoring reference, reference voltage level for charge pump 2 reservoir capacitor
CPN2	16	13	Charge pump 2 flying capacitor negative connection 2
CPP2	17	14	Charge pump 2 flying capacitor positive connection 2
VCP	18	15	Charge pump 2 reservoir capacitor, gate drive supply of high-side MOSFET gate drivers
SH1	19	16	Motor connection terminal 1 and phase 1 high-side MOSFET source terminal
GH1	20	17	Gate driver output for high-side MOSFET, phase 1
SH2	21	18	Motor connection terminal 2 and phase 2 high-side MOSFET source terminal
GH2	22	19	Gate driver output for high-side MOSFET, phase 2
SH3	23	20	Motor connection terminal 3 and phase 3 high-side MOSFET source terminal
GH3	24	21	Gate driver output for the high-side MOSFET, phase 3
OPN3	25	22	Current sense OpAmp 3 inverting input
OPP3	26	23	Current sense OpAmp 3 non-inverting input
OPO3	27	24	Current sense OpAmp 3 output
OPN2	28	—	Current sense OpAmp 2 inverting input
OPP2	29	—	Current sense OpAmp 2 non-inverting input
OPO2	30	—	Current sense OpAmp 2 output
OPN1/BEMF1	31	25	Current sense OpAmp 1 inverting input/Back-EMF feedback phase 1
OPP1/BEMF2	32	26	Current sense OpAmp 1 non-inverting input/Back-EMF feedback phase 2
OPO1/BEMF3	33	27	Current sense OpAmp 1 output/Back-EMF feedback phase 3
NRES	34	28	Input/output pin for resetting microcontroller, pull-up to VIO, active low
IL1	35	29	Low-side digital driver input – use in direct control mode to activate GL1 or in complementary control mode as enable line for phase 1

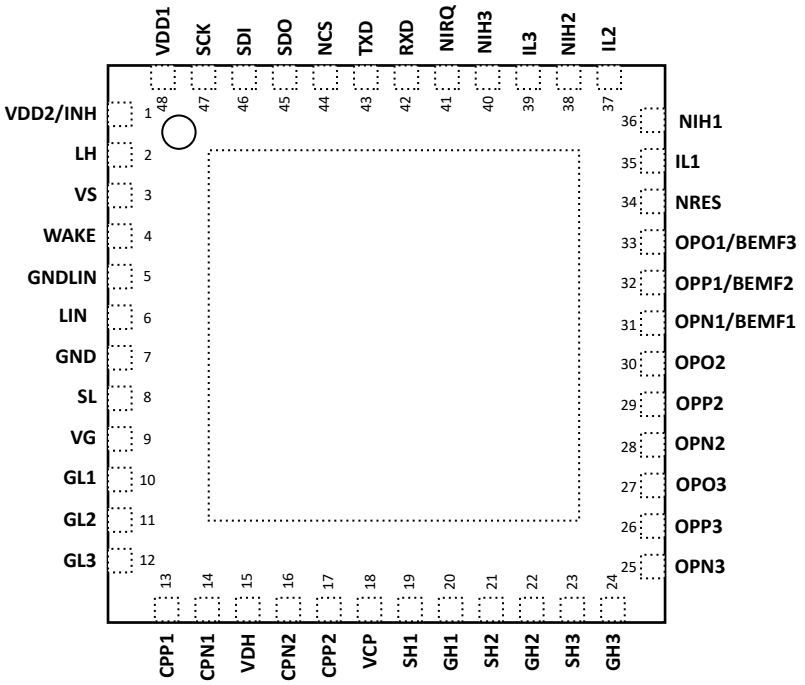
Pin Configuration (continued)

Pin Name	48 Pin	40 Pin	Pin Description
NIH1	36	30	**Inverted (active low)** High-side digital driver input – use in direct control mode to activate GH1 or in complementary control mode as PWM input for phase 1
IL2	37	31	Low-side digital driver input – use in direct control mode to activate GL2 or in complementary control mode as enable line for phase 2
NIH2	38	32	**Inverted (active low)** High-side digital driver input – use in direct control mode to activate GH2 or in complementary control mode as PWM input for phase 2
IL3	39	33	Low-side digital driver input – use in direct control mode to activate GL3 or in complementary control mode as enable line for phase 3
NIH3	40	34	**Inverted (active low)** High-side digital driver input – use in direct control mode to activate GH3 or in complementary control mode as PWM input for phase 3
NIRQ	41	35	Interrupt output, pull-up to VIO, active low
RXD	42	—	Receive data output from LIN transceiver
TXD	43	—	Transmit data input into LIN transceiver
NCS	44	36	SPI chip-select, active low
SDO	45	37	SPI Serial Data Output
SDI	46	38	SPI Serial Data Input
SCK	47	39	SPI Clock Input
VDD1	48	40	100 mA, 5V/3.3V supply voltage
PGND	EP	EP	Exposed Thermal Pad: Heat slug, general device ground

4.1. Packages

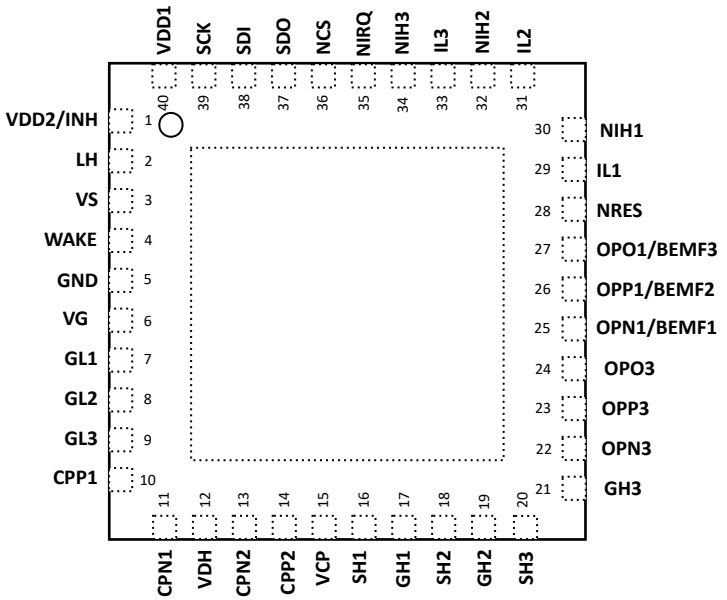
Available packages.

Figure 4-1. 48-VQFN (6x6x0.9 mm)



VQFN48-EP

Figure 4-2. 40-VQFN (5x5x0.9 mm)



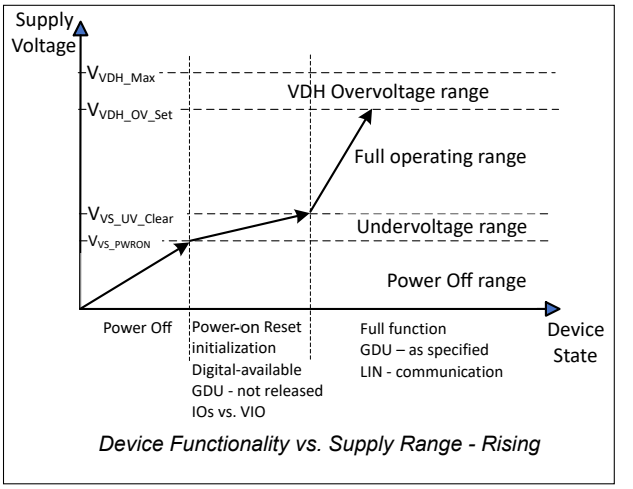
5. Functional Description

Safe operation is assured by a wide variety of integrated diagnostic and protection features.

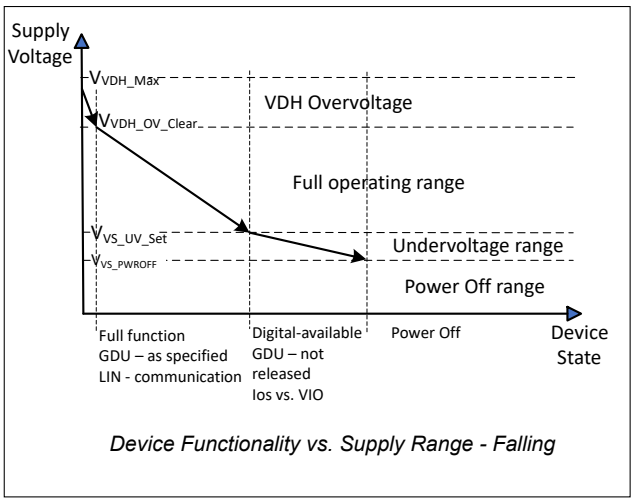
The device has a wide operating voltage range and offers several power-saving operating modes for battery-based applications.

5.1. Supply Voltage Range vs. Device Functionality

Figure 5-1. Supply Voltage Range vs. Device Functionality



Device Functionality vs. Supply Range - Rising



Device Functionality vs. Supply Range - Falling

5.2. Device Operating Modes

Initialization

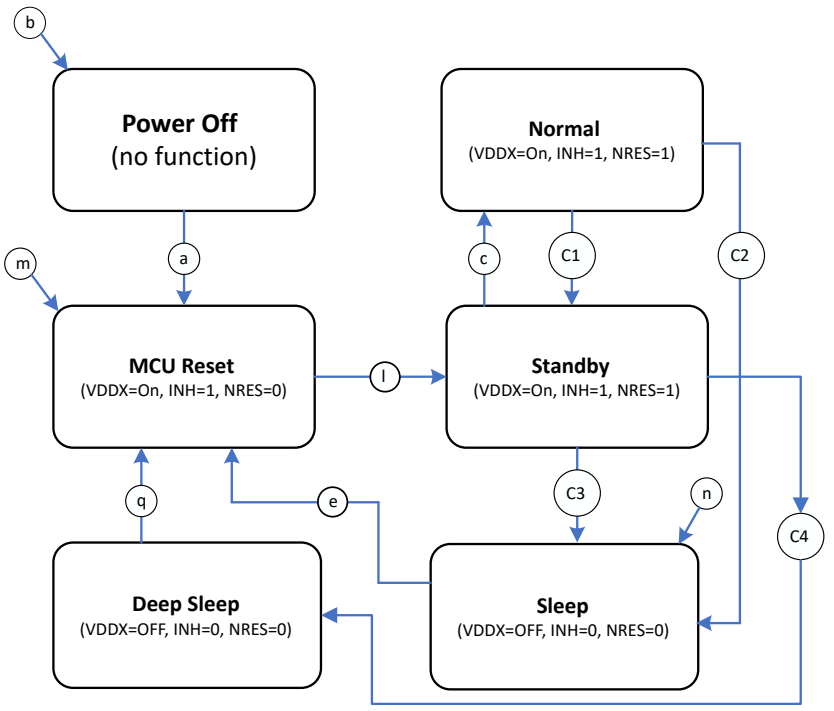
The device mode control unit of the MCP8048 implements six different modes (see Device Operating Modes):

- MCU Reset
- Normal
- Power Off
- Standby
- Deep Sleep
- Sleep

Table 5-1. Device States Table

Safe State	GDU HSx/LSx	CPx	VDDxINH	SPI	CSA / ZCD	LIN	WAKE	Watchdog
Power Off Mode	Off	Off	Off	Off	Off	Off	Off	Off
MCU Reset Mode	Off	Off	**On**	Off	Off	Off	Off	Off
Normal Mode	Switchable On/Off	On	On	On	Switchable On/Off	Switchable On/Off	On	On/Off as configured
Standby Mode	Off	Off	On	On	Off	Off	On	Switchable On/Off
Sleep Mode	Off	Off	Off	Off	Off	Off	**On**	**On** if WDSLP=1
Deep Sleep Mode	Off	Off	Off	Off	Off	Off	**On**	Off

Figure 5-2. Device Operating Modes (DOPM)



- a: $V_{VS} \geq V_{VS\_PWRON}$ (4.2V...4.55V)

- b: $V_{VS} < V_{VS\_PWROFF}$ (2.8V...3V)
- c: DOPM = Normal
- e: Wake-up/interrupt event
- f: DOPM = Standby
- g: DOPM = Sleep
- h: No wake-up and interrupt event pending
- j: Illegal DOPM code configuration via SPI
- k: Number of enabled wake-up sources ≥ 1
- l:
  - MCP8048/49-5050: Reset pulse time expired **&** NRES not driven low externally **&** ((RSTLVL = 0 **&** $V_{VDD1} > V_{VDD1\_UV\_IO\_Clear}$) **||** (RSTLVL = 1 **&** $V_{VDD1} > V_{VDD1\_UV\_Clear}$))
  - MCP8048/49-3333: Reset pulse time expired **&** NRES not driven low externally **&** $V_{VDD1} > V_{VDD1\_UV\_IO\_Clear}$
  - MCP8048/49-5033: Reset pulse time expired **&** NRES not driven low externally **&** $V_{VDD2} > V_{VDD2\_UV\_IO\_Clear}$
- m:
  - MCP8048/MCP8049: Watchdog activated **&** any Reset event
  - MCP8048/49-5050: ($V_{VDD1} < V_{VDD1\_UV\_Set}$ **&** RSTLVL = 1) **||** $V_{VDD1} < V_{VDD1\_UV\_IO\_Set}$
  - MCP8048/49-3333: $V_{VDD1} < V_{VDD1\_UV\_IO\_Set}$
  - MCP8048/49-5033: $V_{VDD2} < V_{VDD2\_UV\_IO\_Set}$
  - MCP8048/MCP8049: NRES pulled low externally
- n: VDDIOOVSD = 1 **&** VDDIO overvoltage has been detected
- p: DOPM = Deep Sleep
- q: Local wake-up has been detected
- r: Local wake-up enabled

- C1 = f **||** j **||** g **&** (!h **||** !k)
- C2 = g **&** h **&** k
- C3 = g **&** h **&** k
- C4 = p **&** r **&** h

Notes:

- Mode switching triggered by condition a or q will not activate the LH pin.
- If DOPM = Normal mode and the CSCR [CSA1/2/3EN] bits are set, then CSA1/2/3 are enabled.
- LIN communication is available only if DOPM = Normal and LIN Operation Mode (LOPM) is activated (default: LIN is in Standby mode).

LH (Limp Home) will be activated in MCU Reset mode when:

- A watchdog failure event has been detected (Watchdog timeout in Sleep mode will not activate LH).
- The device enters MCU Reset mode due to a VDDx undervoltage event.
- VDDx undervoltage has been detected for longer than t_{Reset} after entering MCU Reset mode, triggered by (e).

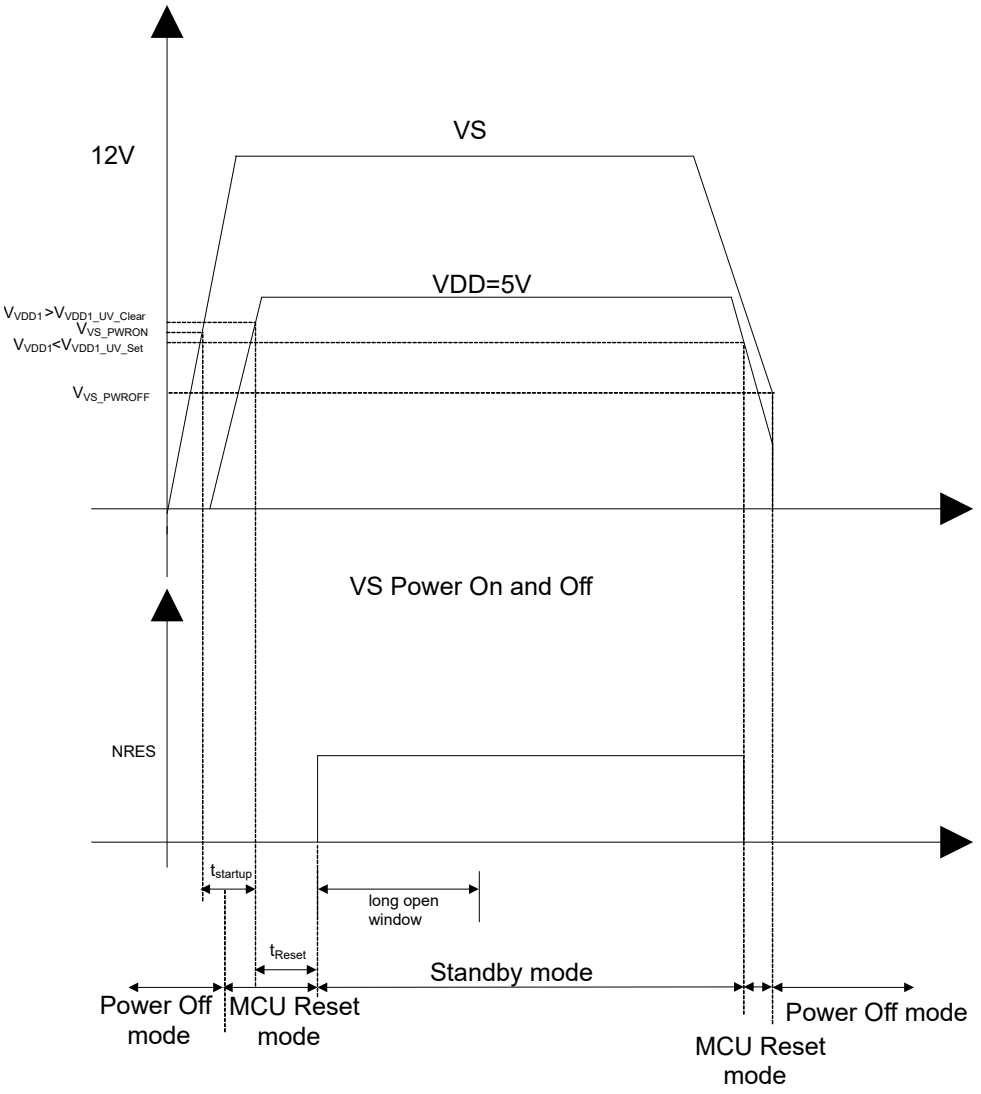
5.2.1. POWER OFF MODE

The MCP8048/MCP8049 is in Power OFF mode as long as the supply voltage of the device (V_{VS}) is lower than the Power OFF Detection Voltage Threshold (V_{VS_PWROFF}).

- The integrated LIN transceiver is in LIN Unpowered mode (see LIN Transceiver).
- The watchdog is inactive.
- The LDO(s) is/are inactive.

As soon as V_{VS} rises above the Power ON Detection Threshold (V_{VS_PWRON}), the device starts transitioning to MCU Reset mode. The device is reset, initialized and the VDDx LDOs are enabled, see Figure 5-3, "Mode Switching During Power ON Start and Power OFF (MCP8048/49-5050, RSTLVL = '1')".

Figure 5-3. Mode Switching During Power ON Start and Power OFF (MCP8048/49-5050, RSTLVL = '1')



5.2.2. MCU RESET MODE

The MCU Reset mode is the default mode of the MCP8048 after a Power-On Reset. It is the Reset execution state of the device. This mode ensures that the NRES pin is pulled down for a defined time to allow the microcontroller to be reset in a controlled manner.

The INH pin, if available, is driven high.

In the MCU Reset mode, the LIN transceiver is unable to transmit or receive data (LIN Standby mode, see Section LIN Transceiver). The gate drive unit is in GDU OFF mode. The SPI is disabled. All registers will be reset to initial value. If the mode transition was triggered by the NRES pin being driven externally, the SPI communication is disabled only until t_{Reset} expires. The LDO voltage regulators (VDDx) and the overtemperature detection are active. The watchdog is disabled.

In the MCU Reset mode, the DOPMCR Register cannot be programmed and is set to Standby.

The following events will cause the MCP8048 to transition to MCU Reset mode:

- Transitioning from Sleep mode or Deep Sleep mode after detecting a wake-up event or interrupt event.
- After a watchdog timeout or when the watchdog in Window mode is triggered too early.
- An attempt is made to reconfigure the watchdog control register while the MCP8048 is in Normal mode.
- For the MCP8048/49-5050: If the RSTLVL bit in the DOPMCR register has been set to '1' and $V_{VDD1} < V_{VDD1\_UV\_Set}$
- For the MCP8048/49-5050, MCP8048/49-3333: $V_{VDD1} < V_{VDD1\_UV\_IO\_Set}$
- For the MCP8048/49-5033: $V_{VDD2} < V_{VDD2\_UV\_IO\_Set}$

5.2.2.1. MCU Reset Mode and VDD Undervoltage Events

For MCP8048/49-5050, if the RSTLVL bit is set to '1' (default), the device will enter MCU Reset mode after detecting a VDD1 undervoltage ($V_{VDD1} < V_{VDD1\_UV\_Set}$).

The device will stay in the MCU Reset mode until VDD1 recovers ($V_{VDD1} > V_{VDD1\_UV\_Clear}$) and then resets, restarting the Reset pulse length timer.

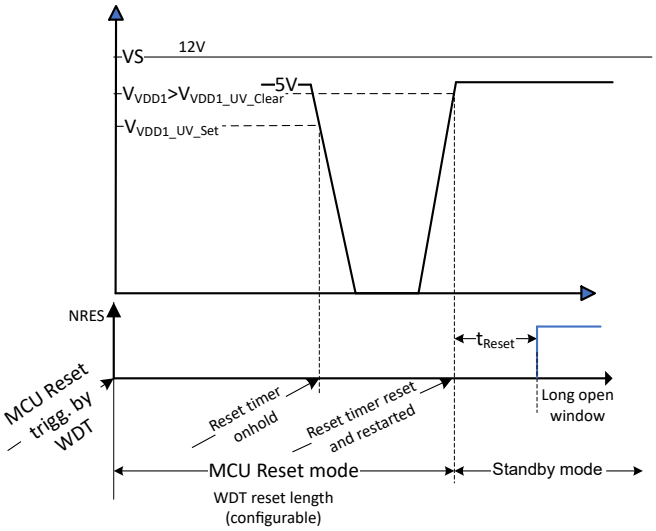
If VDD1 undervoltage is detected when the device is in MCU Reset mode, the Reset pulse length timer will remain on hold until VDD1 recovers and will then be reset and restarted.

The MCP8048 device will leave the MCU Reset mode and enter Standby mode after the t_{Reset} time expires (see Device Operating Modes).

For MCP8048/49-3333 or MCP8048/49-5050, the device will enter MCU Reset mode only after Power-on start-up, after detecting a Watchdog Reset event, or after detecting $V_{VDD1} < V_{VDD1\_UV\_IO\_Set}$, independent of the value of RSTLVL bit from the DOPMCR register. In this case, the device will start the Reset pulse length timer after the device enters the MCU Reset mode and $V_{VDD1} > V_{VDD1\_UV\_IO\_Clear}$ has been detected. As soon as the timer has expired, the device will transition to Standby mode.

For MCP8048/49-5033, the device will enter MCU Reset mode only after Power-on start-up, after detecting a Watchdog Reset event, or after detecting $V_{VDD2} < V_{VDD2\_UV\_IO\_Set}$. In this case, the device will start the Reset pulse length timer after the device enters the MCU Reset mode and $V_{VDD2} > V_{VDD2\_UV\_IO\_Clear}$ has been detected. As soon as the timer has expired, the device will transition to Standby mode.

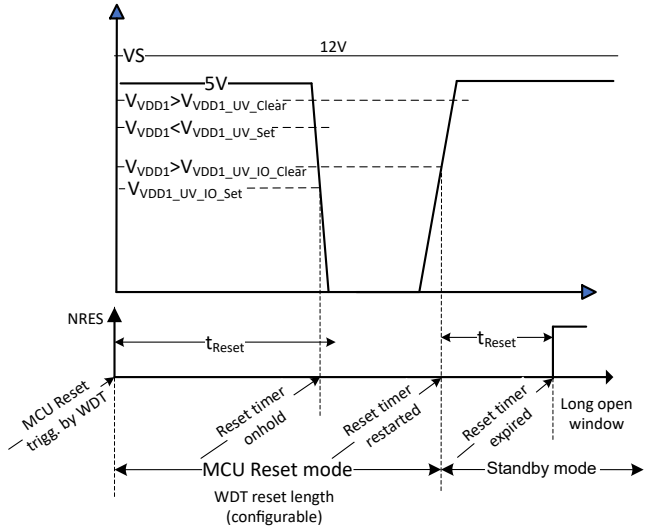
Figure 5-4. VDD1 Undervoltage (V_{VDD1} < $V_{VDD1\_UV\_Set}$) in the MCU Reset Mode, RSTLVL = '1', MCP8048/49-5050



5.2.2.2. Reset Input and Output (NRES)

The NRES pin is asserted when the MCP8048 enters MCU Reset mode. The MCP8048 also enters MCU Reset mode when the NRES pin is pulled low externally. The MCP8048 can only exit MCU Reset mode when the NRES pin is not driven "low" externally.

Figure 5-5. MCU Reset Mode during VDD Undervoltage (V_{VDD1} < $V_{VDD1\_UV\_IO\_Set}$) when, RSTLVL = '0', MCP8048/49-5050



5.2.3. STANDBY MODE

In Standby mode, the gate drive unit is in GDU OFF mode. The integrated LIN transceiver is in LIN Standby mode and is unable to transmit or receive data. All available VDDx regulators are active. The INH pin, if available, is driven high. The watchdog is set to active by default.

A transition into Normal mode only can be achieved by setting the DOPM bits to '111'.

The MCP8048 provides various interrupt registers. Register bits (see SIR1 Register to SIR4 Register) are set to '1' by the device if a corresponding event has been detected. The detection of a wake-up or interrupt event is signaled via the NIRQ pin. The NIRQ pin voltage in high level (logic status '1') is the same as VIO voltage and will be forced to low (logic status '0') if an event has been captured

and the corresponding interrupt mask bit is not set. The SPI interrupt registers can be read out to determine the corresponding trigger source.

The device will enter Standby mode in the following cases (see Device Operating Modes):

- From MCU Reset mode, after reset pulse length time expired.
- When DOPM is set to Sleep mode and a wake-up event occurs or all wake-up sources are disabled.
- From Normal mode, when DOPM is set to Standby mode via SPI.
- From Normal mode, when an invalid DOPM code was selected.

5.2.3.1. Watchdog During Standby Mode

By default, the watchdog is activated when switching into Standby mode. The watchdog will start in Timeout mode by default. As a safety feature, the watchdog can **only** be configured in Standby mode. The intention is to avoid unwanted watchdog reconfiguration.

After start-up, the microcontroller is expected to initialize the MCP8048 registers. First, the microcontroller must write a valid watchdog trigger sequence (`WDTRIG = 0x55`).

5.2.4. SLEEP MODE

In Sleep mode, all available VDDx regulators are deactivated. The INH pin (if available) is high ohmic. The LIN transceiver is in LIN Standby mode (see LIN Transceiver) and the gate drive unit is in GDU OFF mode (see GDU OPERATION MODES). The device reacts to LIN bus wake-up, local wake-up and system interrupt events. Before entering Sleep mode, at least one wake-up mechanism must be unmasked to allow proper wake-up.

The device exits Sleep mode if either a LIN bus wake-up or a local wake up (WAKE) is detected. It will also exit Sleep mode as soon as an interrupt event or a Watchdog Reset occurs.

The device will enter Sleep mode in the following cases (see Device Operating Modes):

- From **Normal Mode** or **Standby Mode** via the DOPM SPI command `010` = Sleep mode, if no wake-up event is pending and at least one wake-up source is enabled. All interrupt flags must be cleared before the device can enter Sleep mode.
- From all modes when a VIO overvoltage has been detected and the VDDIOOVSD bit is set to '`1`'.

In case of sending a SPI command during the process of going to sleep, the process will get corrupted.

5.2.5. DEEP SLEEP MODE

The MCP8048 has the lowest current consumption in Deep Sleep mode. All functional blocks are deactivated, except for local wake up and VS Power OFF capture. The INH pin (if available) is high ohmic. All registers are reset.

Deep Sleep mode can only be entered from Standby mode, but not directly from Normal mode.

Any interrupt must be cleared before entering Deep Sleep mode.

The local wake up (LOCWUE) must be activated.

Switching into Deep Sleep mode is initiated by setting the DOPM bits in the DOPMCR Register to `001` = Deep Sleep mode.

After detecting a wake-up event, the device is reset, initialized and enters MCU Reset Mode. The wake-up event initiating the wake up out of the Deep Sleep mode will be registered in the corresponding registers (SIR1 and SIR5 registers).

In case of sending a SPI command during the process of going to deep sleep, the process will get corrupted.

5.2.6. NORMAL MODE

In Normal mode, the MCP8048 provides full functionality. All available VDDx regulators are active. The INH pin (if available) is driven high.

Depending on the GDUOPM bits and failure detection status, the gate drive unit can be in GDU OFF, GDU Standby or GDU Normal mode (see GDU FSM in GDU OPERATION MODES).

The LIN transceiver can be in LIN Standby mode or LIN Normal mode, depending on the LIN Operation Mode register LOPM bits and LIN failure detection status (see LIN Transceiver).

5.2.7. Device Operation Mode Control Register

Name: DOPMCR
Offset: 0x01
Reset: 0x84
Property: R/W

Bit	7	6	5	4	3	2	1	0
	RSTLVL	VDDIOOVSD	Reserved[5:3]			DOPM [2:0]		
Access	R/W	R/W	R	R	R	R/W	R/W	R/W
Reset	1	0	0	0	0	1	0	0

Bit 7 – RSTLVL

This bit is unimplemented for MCP8048/49-3333 and MCP8048/49-5033. For MCP8048/49-5050 :

Value	Description
1	When set to '1', a VDD1 undervoltage ($V_{VDD1} < V_{VDD1\_UV\_Set}$) will trigger a mode switch to MCU Reset mode.
0	When set to '0', $V_{VDD1} < V_{VDD1\_UV\_IO\_Set}$ will trigger a mode switch to MCU Reset mode.

Bit 6 – VDDIOOVSD

The microcontroller should set the bit to '1' to enable a VDD µC supply overvoltage shutdown when an overvoltage in VDD (µC supply, the LDO connected to VIO) has been detected. If VDDIOOVSD=1 the device will go in Sleep mode, and if VDDIOOVSD=0 the part will go in MCU reset mode. In both cases Limp Home will be activated.
VDD µC supply:

- MCP8048/49-3333 / MCP8048/49-5050: VIO = VDD1
- MCP8048/49-5033: VIO = VDD2

Bits 5:3 – Reserved[5:3]

Reserved, **do not modify reset value!**

Bits 2:0 – DOPM [2:0]

Select Device Operating mode (see Device Operating Modes):

Value	Description
'3'b001'	Deep Sleep mode
'3'b010'	Sleep mode
'3'b100'	Standby mode
'3'b111'	Normal mode
Other	Invalid mode selection

5.3. Gate Drive Unit (GDU)

5.3.1. GDU FEATURES

The Gate Drive Unit connects three low-side gate drive outputs (GLx) and three high-side gate drive outputs (GHx) to three gate drive half bridges. For VGSUV monitoring, the high-side gate drivers use the signals between the VCP and VDH pins as a reference, whereas the low-side gate drivers use the VG voltage as a reference.

The GDU monitors the voltage drop between the drain and source of the MOSFET for short-circuit events.

The Slew Rate Control unit optimizes EMC performance. This feature allows the control of the gate drive current injected into external MOSFET gates at four configurable levels. The slew rate of

both high-side and low-side gate controls are configurable individually to achieve the best trade-off between EMC performance and drive efficiency.

The module combines the following sub-modules:

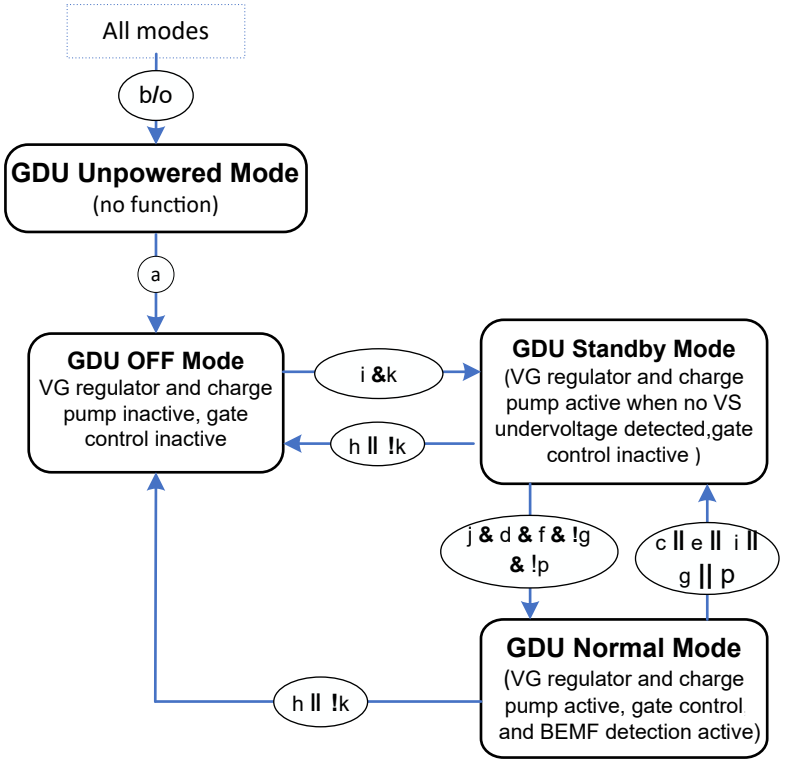
- High-side gate drive unit, including control logic, an adaptive dead-time unit, slew rate control unit, level shifter and gate driver
- Low-side gate drive unit, including control logic, an adaptive dead-time unit, slew rate control unit, level shifter and gate driver
- VDS monitoring unit
- Temperature monitoring sensors

5.3.2. GDU OPERATION MODES

- **GDU OFF mode:** VG, VCP and Gate Control are deactivated.
- **GDU Standby mode:** VG and VCP are active as long as VS undervoltage has not been detected.
- **GDU Normal mode:** VG, VCP and Gate Control are active. Also, if selected, Back-EMF is active.

The state diagram is illustrated below.

Figure 5-6. GDU Operating Modes



- a: Power-on Reset
- b: Device in Power Off ($V_{VS} < V_{VS\_PWROFF}$)
- c: $V_{VG} < V_{VGS\_UV\_Set}$ || ($V_{VCP} - V_{VDH}$) < $V_{VGS\_UV\_Set}$, when VGS undervoltage monitoring is active
- d: No VG and VCP undervoltage detected
- e: $V_{VS} < V_{VS\_UV\_Set}$
- f: No VS undervoltage detected
- g: Any GDU related failure registered (overcurrent with ILIMSDEN=1 and/or short-circuit event with SCSDEN=1 and/or overtemperature shutdown, etc.)

- h: GDUOPM = GDU OFF mode
- i: GDUOPM = GDU Standby mode
- j: GDUOPM = GDU Normal mode and device is in Normal mode
- k: DOPM = Normal mode
- o: Device is in Deep Sleep mode
- p: VDH overvoltage & VDHOVSD = 1

Notes:

- VG and VCP are enabled at GDU transition from Off to Standby (default). The DSR1.GDUS flag is available if GDUOPM = Normal.
- CSA1/2/3 is available when DOPMCR.DOPM = Normal and CSCR.CSA1/2/3EN bits are activated.
- GDU = Normal mode can be written in any state of DOPM, but it will not be active if DOPM is switched in Normal mode while GDU = Normal. To activate the GDU, it is necessary to manually switch the GDU back into Standby and then into Normal.

5.3.3. GDU OPERATION MODE CONTROL REGISTERS

The GOPMCR Register is a control register. Therefore, the state of the GDU will not be mirrored in this register. GDUOPM bits only define the expected state of the transceiver. In addition to setting up the GDUOPM appropriately, all conditions for entering the corresponding GDU Operation modes must be fulfilled before the mode transition occurs. The GDU can also leave the expected Operation mode if the conditions to stay cannot be fulfilled. The finite state machine shown in LIN Transceiver Operating Modes will not change the GDUOPM bits.

5.3.3.1. GDU Operation Mode Control Register

Name: GOPMCR
Offset: 0x03
Reset: 0x01
Property: R/W

Bit	7	6	5	4	3	2	1	0
	Reserved[7:3]					GDUOPM [2:0]		
Access	R	R	R	R	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bits 7:3 – Reserved[7:3]
Reserved, **do not modify reset value!**

Bits 2:0 – GDUOPM [2:0]
Select GDU Operation mode, as shown below:

Value	Description
`'3'b001'`	GDU OFF mode
`'3'b100'`	GDU Standby mode
`'3'b111'`	GDU Normal mode
`Other`	Invalid mode selection

5.3.3.2. GDU Control Register 1

Name: GDUCR1
Offset: 0x05
Reset: 0x1E
Property: R/W

Bit	7	6	5	4	3	2	1	0
	CCPT [7:2]						CCEN	BEMFEN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	1	1	1	0

Bits 7:2 – CCPT [7:2]

Cross Conduction Protection Timer bits. The cross conduction protection time can be calculated as follows: t_{CC} = 100 ns × N, N = 0 to 63 [0x00 to 0x3F]. The role of the CCPT is to prevent shoot-through currents in the external MOSFET transistors (see CROSS CONDUCTION PROTECTION).

Bit 1 – CCEN

Cross Conduction Protection Enable bit. The CCEN bit enables the cross conduction protection feature. Disabling cross conduction protection results in the disabling of both the cross conduction timer and adaptive dead-time generation.

Value	Description
1	Cross conduction protection is enabled.
0	Cross conduction protection is disabled; hence, the cross conduction protection timer and adaptive dead-time timer are also disabled.

Bit 0 – BEMFEN

Back-EMF Comparator Enable bit. If both the current sense amplifier '1' (CSA1EN = '1') and the Back-EMF comparator (BEMFEN = '1') are enabled, then Back-EMF detection and current sense amplifier 1 will be disabled.

Value	Description
1	It will activate Back-EMF detection. The BEMF1, BEMF2 and BEMF3 pins are activated and signal the current ZCD state.
0	It disables the Back-EMF detection. The BEMFx pins are then released for OpAmp1 operation.

5.3.3.3. GDU Control Register 2

Name: GDUCR2
Offset: 0x06
Reset: 0x11
Property: R/W

Bit	7	6	5	4	3	2	1	0
	HSOFF	LSOFF	TSWTO [5:4]		EGBLT [3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	0	0	0	1

Bit 7 – HSOFF

High-Side Gate Driver Inactive Mode State bit.

Value	Description
1	The microcontroller will set the bit to '1' if high-side gate drivers should be driven low in GDU Standby mode.
0	The microcontroller will set this bit to '0' if high-side gate drivers should become tri-state when GDU is in GDU Standby mode.

Bit 6 – LSOFF

Low-Side Gate Driver Inactive Mode State bit.

Value	Description
1	The microcontroller will set the bit to '1' if low-side gate drivers should be driven low in GDU Standby mode.
0	The microcontroller will set this bit to '0' if low-side gate drivers should become tri-state when GDU is in GDU Standby mode.

Bits 5:4 – TSWTO [5:4]

Forces Switch Delay Time Control bits. For the definition of the delay, refer to CROSS CONDUCTION PROTECTION. Force to switch delay is set in ns, as shown below:

Value	Description
2'b00'	225 ns
2'b01'	475 ns
2'b10'	975 ns
2'b11'	1975 ns

Bits 3:0 – EGBLT [3:0]

The Edge Blanking Time Control bits. The edge blanking time can be configured as shown in Current Limitation Detection/Short Circuit Detection Time. Edge blanking time starts after the cross conduction time expires and the corresponding gate control input becomes active (NIHx = '0' or ILx = '1'). VDS monitoring is blanked out during this time.

5.3.3.4. GDU Control Register 3

Name: GDUCR3
Offset: 0x07
Reset: 0x0
Property: R/W

Note: Pay attention to the impact of the slew rate when handling negative voltage at phase pins.

Bit	7	6	5	4	3	2	1	0
	ADDTHS [7:6]		ADDTLS [5:4]		HSSRC [3:2]		LSSRC [1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:6 – ADDTHS [7:6]
Adaptive Dead-Time Configuration bits (high-side). Can be set as shown below:

Value	Description
'2'b00'	Disabled
'2'b01'	50–160 ns
'2'b10'	150–210 ns
'2'b11'	300–360 ns

Bits 5:4 – ADDTLS [5:4]
Adaptive Dead-Time Configuration bits (low-side). Can be set as shown below:

Value	Description
'2'b00'	Disabled
'2'b01'	50–160 ns
'2'b10'	150–210 ns
'2'b11'	300–360 ns

Bits 3:2 – HSSRC [3:2]
High-Side Slew Rate Control bits. Can be set as shown below (Note):

Value	Description
'2'b00'	Full speed
'2'b01'	50% of full speed
'2'b10'	25% of full speed
'2'b11'	12.5% of full speed

Bits 1:0 – LSSRC [1:0]
Low-Side Slew Rate Control bits. Can be set as shown below (Note):

Value	Description
'2'b00'	Full speed
'2'b01'	50% of full speed
'2'b10'	25% of full speed
'2'b11'	12.5% of full speed

5.3.3.5. GDU Control Register 4

Name: GDUCR4
Offset: 0x08
Reset: 0x78
Property: R/W

Bit	7	6	5	4	3	2	1	0
	COMPEN	VDHOVSD	UVVGSEN	UVVGSLVL	VGSUVFLT [3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	1	1	1	0	0	0

Bit 7 – COMPEN

Complementary Control Enable bit.

Value	Description
1	The microcontroller will set this bit to '1' if the complementary control of external MOSFETs is activated.
0	The microcontroller will set this bit to '0' if the external MOSFETs are controlled individually (direct) with the six gate control input signals (NIHx and ILx).

Bit 6 – VDHOVSD

VDH Overvoltage Shutdown Enable bit.

Value	Description
1	The microcontroller will set this bit to '1' when a VDH overvoltage event triggers a shutdown of the VG and VCP regulator (triggers transition from GDU Normal mode to GDU Standby mode).
0	The microcontroller will set this bit to '0' if a VDH overvoltage event will not trigger a shutdown of VG and VCP regulator.

Bit 5 – UVVGSEN

VGS Undervoltage Detection Enable bit. The bit enables/disables both VCP and VG monitoring.

Value	Description
1	The microcontroller will set this bit to '1' when VGS monitoring is active.
0	The microcontroller will set this bit to '0' when VGS monitoring is not active.

5.3.3.5.4. UVVGSLVL

VGS/VG Undervoltage Detection Level Selection bit.

Value	Description
1	The microcontroller will set this bit to '1' when the higher detection level ($V_{VGS\_UV\_Set\_H}$) is used.
0	The microcontroller will set this bit to '0' when the lower detection level ($V_{VGS\_UV\_Set\_L}$) is used.

Bits 3:0 – VGSUVFLT [3:0]

VGS undervoltage filter time ($t_{VGS\_UV\_Blank}$). The filter time can be configured as follows: 770 ns × N, N = 1 to 16 [0x0 to 0x0F]. Filter time starts after an undervoltage event has been detected (comparator output changes to high). If VG and VCP voltage rise above the detection threshold during filter time, filter time will be reset and it will be restarted after VGS undervoltage occurs again.

5.4. Charge Pumps (CP1 and CP2)

The MCP8048/MCP8049 supports 100% duty cycle operation by using two charge pumps. CP1 supplies the low-side gate drivers, and its input voltage is generated from the battery supply pin VDH. CP2 supplies the high-side gate drivers and is generated out of the charge pump output of VG. Each charge pump (CP1 and CP2) charges from its input supply via an external flying capacitor into an external storage capacitor. VG is the output pin of CP1, whereas VCP is the output pin of CP2.

After the GDU transitions into Standby mode, CP1 is turned on if VDH < VCP_START to power the 12V LDO. In case VDH > VCP_STOP, the 12V LDO will be supplied directly from VDH, bypassing the charge pump to limit VG voltage to 12V.

The second charge pump, CP2, provides the high-side gate driver biasing and is active when the GDU is in Standby or Normal mode.

The module monitors the output voltages and delivers an undervoltage detection event, which is notified in the SIR3 Register, through the VCPUV and VGUV bits.

The output of CP2 may serve as a control output pin for a reverse voltage polarity protection MOSFET, see Figure 1-1.

5.5. Low Dropout Voltage Regulator (VDD1)

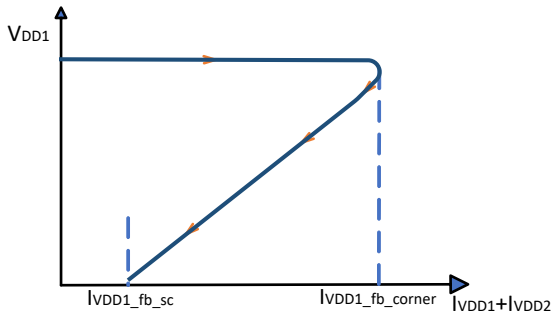
Depending on the product, the VDD1 pin has a nominal voltage output level of 5V or 3.3V, see Product Family.

The voltage regulator needs an external capacitor to compensate for and smooth any disturbances. It is recommended to use an MLC capacitor connected in parallel with a 100 nF ceramic capacitor.

During a short circuit at VDD1, the output current is limited to $I_{VDD1\_fb\_sc}$. If the LDO temperature exceeds the T_{OT_sdwn} threshold, the VDD1 output will be switched off. As soon as the junction temperature decreases below $T_{OT\_release}$, the regulator will be switched on again.

Exceeding the maximum sum load current of VDD1 and VDD2 [I_{VDD1} + I_{VDD2}] beyond the output current foldback corner threshold $I_{VDD1\_fbcorner}$ leads to a current limitation of LDO1. The current is limited down to the foldback short circuit limit $I_{VDD1\_fb\_sc}$ with decreasing load resistance. This feature reduces the dissipated power in overloading or short circuit conditions and prevents LDO damage. This principle is illustrated in the Principle Foldback Current Waveform (Figure 5-7).

Figure 5-7. Principle Foldback Current Waveform



A proper connection between the exposed pad and a heat sink is recommended to ensure sufficient power dissipation.

If the supply voltage (VS) is below the nominal output voltage of VDD1, the foldback current limitation is disabled and replaced with the standard current limitation ($I_{VDD1lim}$).

5.6. Low Dropout Voltage Regulator (VDD2)

MCP8048/49-5050 and MCP8048/49-5033 provide a voltage regulator with an output voltage of V_{VDD2} = 3.3V. The VDD2 is powered from the 5V output of the VDD1 regulator. The maximum output current is limited to $I_{VDD2lim}$.

The MCP8048/49-3333 provides an inhibit output pin, **INH**. The purpose of the INH pin is to control external devices, such as external voltage regulators.

When inactive, the INH pin output level is high ohmic. When active, the INH voltage is on VS level.

5.7. PWM Inputs Pins

MCP8048/MCP8049 has three input pins for PWM low: IL1 to IL3, which are active at a high logic level. For high side, there are three available pins, nIH1 to nIH3, which are active at a low logic level. This configuration is valid when the COMPEN bit in the GDUCR4 register is in the Low state (see GUDUCR4 Register).

When the COMPEN bit is set (High state), the complementary mode is selected. In this mode, the PWMs are applied only to the nIHx pins, and the ILx pins become enabling inputs for the corresponding PWM. See Table 5-2.

Table 5-2. PWM Input Pins Truth Table

		GDUCR4.COMPEN = 0 (Direct Mode)		GDUCR4.COMPEN = 1 (Complementary Mode)	
Ilx	**nIHx**	**GLx**	**GHx**	**GLx**	**GHx**
Low	Low	0	1	-	-
Low	High	0	0	-	-
High	Low	x	x	0	1
High	High	1	0	1	0

Table 5-3. Legend

-	Outputs are floating (disabled)
x	Outputs remain in previous state until dead time has expired
0	Output is in Low state
1	Output is in High state

5.8. Current Sense Amplifier (CSA)

The MCP8048 provides three fully integrated operational amplifiers, tailored for measuring power stage currents by sensing currents across the shunt resistors. The gain and output offset voltage are configurable by setting the corresponding bits in the CSCR register via the SPI interface.

Optionally, the CSAs can be disabled.

The CSA output voltage range is adapted to the VIO voltage.

The CSA3 output voltage can be monitored with the ILim module, see OUTPUT CURRENT LIMITATION.

5.8.1. Current Sensing OpAmp Control Register

Name: CSCR
Offset: 0x0C
Reset: 0xE0
Property: R/W

Bit	7	6	5	4	3	2	1	0
	CSA3EN	CSA2EN	CSA1EN	Reserved	OFFSET [3:2]		GAIN [1:0]	
Access	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset	1	1	1	0	0	0	0	0

Bit 7 – CSA3EN

Enable Current Sense Amplifier 3 bit. The CSA is enabled when the device is in Normal mode and the corresponding enable bit is set to '1'. All current sense amplifiers will need a maximum of 20 µs to settle their output voltage after the enable signal is set to '1'.

Bit 6 – CSA2EN

Enable Current Sense Amplifier 2 bit. The CSA is enabled when the device is in Normal mode and the corresponding enable bit is set to '1'. All current sense amplifiers will need a maximum of 20 µs to settle their output voltage after the enable signal is set to '1'.

Bit 5 – CSA1EN

Enable Current Sense Amplifier 1 bit. The CSA is enabled when the device is in Normal mode and the corresponding enable bit is set to '1'. If current sense amplifier 1 (CSA1EN = '1') is enabled and BEMFEN (in GDUCR1) is enabled, then both Back-EMF detection and current sense amplifier 1 will be disabled. All current sense amplifiers will need a maximum of 20 µs to settle their output voltage after the enable signal is set to '1'.

Bit 4 – Reserved

Reserved, **do not modify reset value!**

Bits 3:2 – OFFSET [3:2]

Current Sensing Amplifier Output Offset Set Point bits.

Value	Description
'2'b00'	V_{VIO}/16
'2'b01'	V_{VIO}/8
'2'b10'	V_{VIO}/4
'2'b11'	V_{VIO}/2

5.8.1.5. GAIN [1:0]

Current Sensing OpAmp Gain Set Point bits.

Value	Description
'2'b00'	8
'2'b01'	16
'2'b10'	32
'2'b11'	64

5.9. Back-EMF Sampler and Back-EMF Detection

The MCP8048/MCP8049 comes with a fully-integrated Back-EMF detection module, which converts the motor phase voltages into digital feedback signals. The Back-EMF unit includes a resistor network and three high-speed, Zero-Cross Detection comparators (ZCD). The scaled phase signals

V_{SHx} are compared with the emulated motor neutral point voltage for estimating the virtual zero crossing. The ZCD comparator outputs provide three digital feedback signals via the BEMF1, BEMF2 and BEMF3 pins.

Back-EMF detection is activated using the GDUCR1 Register.

5.10. Motor Line Diagnostics

While the motor is not in operation, the Back-EMF module can be used for motor line diagnostics. GDU must be in GDU Standby mode. Motor line (SHx) short to GND, short to VDH and open load can be evaluated, see Motor Line Diagnostics Setup. The MLDCR register is used to control the motor line diagnostics. As soon as the diagnostics are activated, the outputs of the diagnostics comparators will continuously update the MLDRR register. Enabling the motor line diagnostics disables the NIHX and ILx PWM input pins.

Figure 5-8. Motor Line Diagnostics Setup

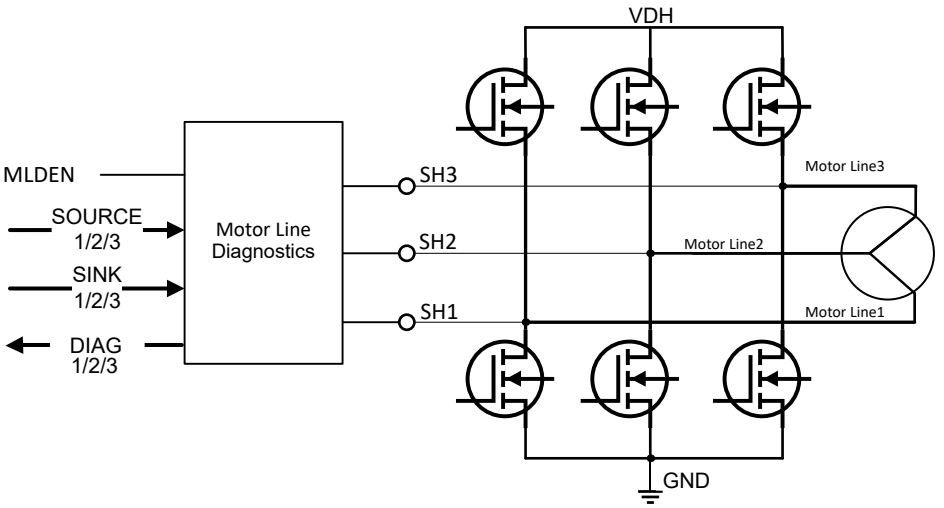
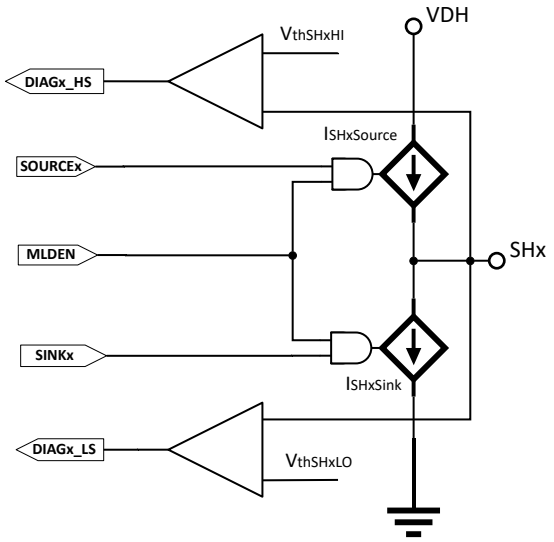


Figure 5-9. Motor Line Diagnostics Diagram



Motor Line Short to GND and Supply Test and Motor Line Open Connection Test show the motor clamp short to GND, short to V_{BUS} or open-load failure detection.

Figure 5-10. Motor Line Short to GND and Short to VDH Test

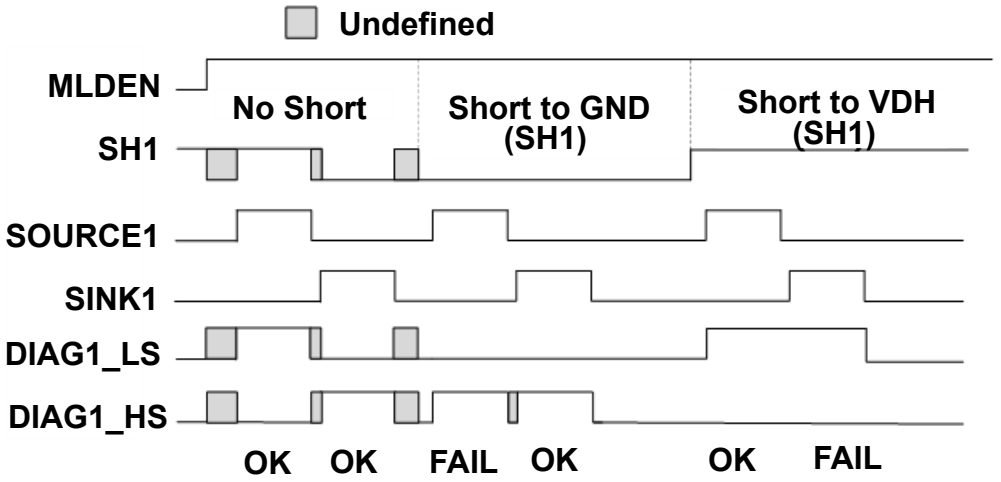
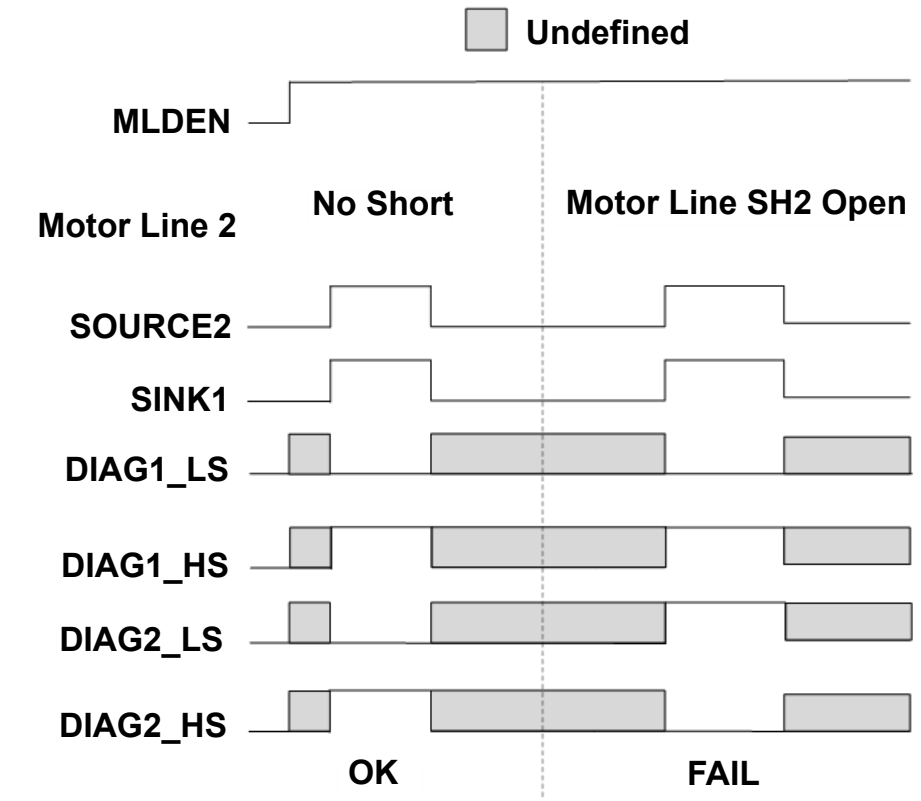


Figure 5-11. Motor Line Open Load Test



A sufficient delay time is required before evaluating the MLDRR register, to account for parasitic board and power MOSFET capacitances, as well as the limited current capability of the diagnostic current sources.

Motor line diagnostics can be activated when VS is within the valid operating range, the MCP8048 is in Normal mode and the GDU is in GDU Standby mode.

5.10.1. Motor Line Diagnostics Control Register

Name: MLDCR
Offset: 0x0E
Reset: 0x0
Property: R/W

Bit	7	6	5	4	3	2	1	0
	Reserved	SOURCE3	SINK3	SOURCE2	SINK2	SOURCE1	SINK1	MLDEN
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – Reserved
Reserved, **do not modify reset value!**

5.10.1.1. SOURCE3

Phase 3 Source Current Control bit

Value	Description
1	Enables source current source 3
0	Disables source current source 3

Bit 5 – SINK3
Phase 3 Sink Current Control bit

Value	Description
1	Enables sink current source 3
0	Disables sink current source 3

Bit 4 – SOURCE2
Phase 2 Source Current Control bit

Value	Description
1	Enables source current source 2
0	Disables source current source 2

Bit 3 – SINK2
Phase 2 Sink Current Control bit

Value	Description
1	Enables sink current source 2
0	Disables sink current source 2

Bit 2 – SOURCE1
Phase 1 Source Current Control bit

Value	Description
1	Enables source current source 1
0	Disables source current source 1

5.10.1.6. SINK1

Phase 1 Sink Current Control bit

Value	Description
1	Enables sink current source 1
0	Disables sink current source 1

Bit 0 – MLDEN

Motor Line Diagnostics in GDU Standby Mode bit

Value	Description
1	Enables motor line diagnostics (only in GDU Standby mode)
0	Disables motor line diagnostics (only in GDU Standby mode, default)

5.10.2. Motor Line Diagnostics Results Register

Name: MLDRR
Offset: 0x12
Reset: 0x0
Property: R

The motor-line diagnostics results can be read from the MLDRR register. The register is accessed via SPI. The results are available after each change in the MLDCR register.

Bit	7	6	5	4	3	2	1	0
	Reserved[7:6]		DIAG3_HS	DIAG3_LS	DIAG2_HS	DIAG2_LS	DIAG1_HS	DIAG1_LS
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:6 – Reserved[7:6]
Reserved, **do not modify reset value!**

Bit 5 – DIAG3_HS
Diagnostics Result Register bit. Interprets the results as described in Motor Line Short to GND and Short to VDH Test and Motor Line Open Load Test.

Bit 4 – DIAG3_LS
Diagnostics Result Register bit. Interprets the results as described in Motor Line Short to GND and Short to VDH Test and Motor Line Open Load Test.

Bit 3 – DIAG2_HS
Diagnostics Result Register bit. Interprets the results as described in Motor Line Short to GND and Short to VDH Test and Motor Line Open Load Test.

Bit 2 – DIAG2_LS
Diagnostics Result Register bit. Interprets the results as described in Motor Line Short to GND and Short to VDH Test and Motor Line Open Load Test.

Bit 1 – DIAG1_HS
Diagnostics Result Register bit. Interprets the results as described in Motor Line Short to GND and Short to VDH Test and Motor Line Open Load Test.

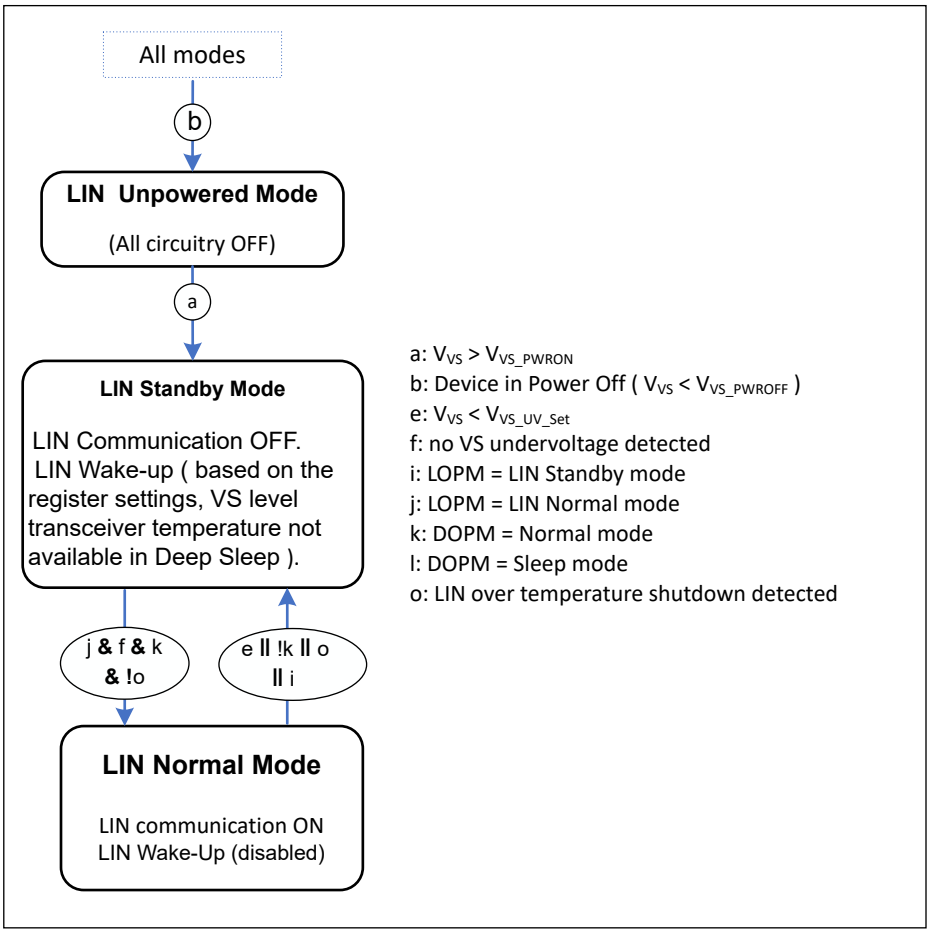
Bit 0 – DIAG1_LS
Diagnostics Result Register bit. Interprets the results as described in Motor Line Short to GND and Short to VDH Test and Motor Line Open Load Test.

5.11. LIN Transceiver

The integrated LIN transceiver in the MCP8048 provides low-speed data communication in BLDC applications. It is designed in compliance with ISO 17987-4 and SAE J2602-2. It implements the LIN electrical physical layer. Improved slope control at the LIN bus ensures data communication up to 20 kbaud.

The integrated LIN transceiver supports the following operating modes: LIN Normal and LIN Standby. The LIN transceiver operating mode depends on the device operating mode and the setting of the LOPM bits in the LIN Transceiver Operating Mode Control register. When the device is in Normal mode, the two operating modes can be selected via the LOPM bits in the LOPMCR Register.

Figure 5-12. LIN Transceiver Operating Modes



5.11.1. LIN Normal Mode

This is the normal transmission and receiving mode of the LIN interface. LIN bus wake up is not active in LIN Normal mode.

As shown in Figure 5-12, the LIN transceiver will enter the LIN Normal mode in the following case:

- From LIN Standby mode, when the device operating mode is set to Normal mode **AND** no VS undervoltage is detected **AND** no LIN transceiver overtemperature shutdown is detected **AND** LOPM is set to LIN Normal mode.

5.11.2. LIN Standby Mode

The LIN transceiver automatically switches to the LIN Standby mode after system power-up. In this mode, LIN communication is disabled. The internal strong pull-up resistor between the LIN pin and VS pin is disabled to minimize the current consumption in case the LIN pin is short-circuited to GND. Only a weak pull-up current (typically 10 µA) between the LIN pin and the VS pin is present.

Depending on the setting of the LINWUE bit (LIN bus wake-up event detection enable, see WUCR Register), the LIN bus wake-up can be activated or deactivated. If the bit is set to '1', a LIN bus voltage below the pre-wake detection LIN (V_{LINH}) activates a strong pull-up current between VS and LIN to stabilize the recessive output voltage at the LIN pin. At the same time, an internal LIN receiver is activated and the wake-up detection timer is started. If a valid LIN bus wake-up is detected, the register bit LINWU will be set to '1'. The microcontroller will be notified via the NIRQ pin. The strong pull-up current will be switched off again when the LIN transceiver is in LIN Standby mode

and the bit LINWU is reset by the microcontroller. LIN wake-up is disabled during a LIN transceiver overtemperature shutdown.

As shown in Figure 5-12, the LIN transceiver will enter LIN Standby mode in the following situations:

1. From LIN Unpowered mode after device Power-on Reset.
2. From LIN Normal mode when VS undervoltage has been detected **OR** the device has been switched to Deep Sleep/Sleep/Standby/MCU Reset mode **OR** LIN transceiver overtemperature shutdown has been detected **OR** LOPM is set to Standby mode.

5.11.3. LIN Transceiver Behavior under Low Supply Voltage Condition

After supplying power to the device, the voltage at the VS pin increases according to the connected blocking capacitor. If V_{VS} is higher than the minimum VS operating threshold V_{VS_PWRON}, the LIN Transceiver mode changes from LIN Unpowered mode to LIN Standby mode. As soon as V_{VS} exceeds the undervoltage threshold $V_{VS\_UV\_Clear}$, the LIN transceiver can be activated when the device is in Normal mode.

If, during LIN Standby mode, the supply voltage on the VS pin drops below the VS operating threshold V_{VS_PWROFF}, then the LIN transceiver switches to LIN Unpowered mode.

If, during LIN Normal mode, the voltage level on the VS pin drops below the VS undervoltage detection threshold $V_{VS\_UV\_Set}$, the LIN transceiver switches to LIN Standby mode. As a result, the LIN transceiver is disabled in order to avoid malfunctions and false bus messages. If the VDD1 or VDD2 voltage drops below the corresponding undervoltage threshold, $V_{VDD1\_UV\_Set}$, $V_{VDD1\_UV\_IO\_Set}$, $V_{VDD2\_UV\_IO\_Set}$, the LIN transceiver will also switch to LIN Standby mode, as the device will transition to MCU Reset mode. LIN bus wake-up is not possible while a VS undervoltage is detected.

5.11.4. LIN TRX Operation Mode Control Register

Name: LOPMCR
Offset: 0x02
Reset: 0x01
Property: R/W

Bit	7	6	5	4	3	2	1	0
	Reserved[7:3]					LTXD_DIS	LOPM [1:0]	
Access	R	R	R	R	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bits 7:3 – Reserved[7:3]
Reserved, **do not modify reset value!**

Bit 2 – *LTXD_DIS* Disable LIN_TX_DOM – Timeout Timer (MCP8048)
The **LTXD_DIS** bit is used to enable or disable the LIN TXD timeout timer function.
By default (i.e., following a reset), this bit is set to **0**, indicating that the LIN TXD timeout timer function is **enabled** and actively monitoring for timeouts.
Setting the **LTXD_DIS** bit to **1** disables the timeout timer function, meaning no timeout monitoring will occur.
In order to set **LTXD_DIS** bit to **1**, both conditions should be matched:

- device should be in LIN standby mode
- LTXD_DIS + LIN Normal mode commands should be sent together

Value	Description
0	LIN TXD Timeout Timer is active
1	LIN TXD Timeout Timer is disabled

Bits 1:0 – LOPM [1:0]
Selects LIN Transceiver operation modes.

Value	Description
'2'b01'	LIN Standby mode
'2'b10'	LIN Normal mode
Other	Invalid mode selection

5.12. Wake-up Sources

Wake-up is required to exit both deep sleep and Sleep modes. The wake-up sources, LIN remote wake-up or local wake-up, can be selected in the Wake-up Control register, WUCR. If a wake-up occurrs, the wake-up source can be determined in the SIR5 Register, bits 4 and 5.

5.12.1. LIN REMOTE WAKE-UP

Depending on the setting of the LINWUE bit (LIN bus wake-up event detection enable, see WUCR Register), the LIN bus wake-up capability is activated or deactivated. If the bit is set to '1', a LIN bus voltage level below the LIN driver dominant threshold will activate the internal LIN receiver and start the wake-up detection timer.

A dominant bus level maintained for a certain duration (> t_{bus}) and the following rising edge at the LIN pin result in a remote wake-up request. If a valid LIN bus wake-up is detected, the LINWU register bit will be set to '1'. A strong pull-up current between VS and LIN is activated to stabilize the recessive output voltage at the LIN pin.

The event will be signaled to a microcontroller via the NIRQ pin. The strong pull-up current will be switched OFF again when the LIN transceiver switches into LIN Standby mode and the LINWU bit is reset by the microcontroller.

5.12.2. LOCAL WAKE-UP VIA WAKE PIN

The MCP8048 provides a high-voltage input pin (WAKE) with the purpose of waking up the device.

The local wake up is active after enabling it via the LOCWUE bit.

A local wake-up request is detected when a falling edge has been detected on the WAKE pin and the logic level on the pin has been stable for at least t_{local_wu}. The event will be signaled via the NIRQ pin in all Device Operation Modes (DOPM).

In Deep Sleep mode the local wake up is always active, independent of the LOCWUE bit value, as all SPI registers are cleared upon entering Deep Sleep mode. However, Deep Sleep mode cannot be entered without LOCWUE = '1'.

5.12.3. CYCLIC WAKE-UP VIA WATCHDOG

To keep the watchdog active when the device is in Sleep mode, the WDSLP bit of the Watchdog Configuration Register 1 must be set to '1'. When the device goes into Sleep mode with WDSLP = 1, the Watchdog Timer gets reset and restarts immediately. The sleep period is given by the WWDP bits from the WDCR2 register, multiplied with the presacale factor selected with the WDPRE bits from the WDCR1 register. The NRES reset pulse length is defined by the WRPL bits from the WDCR2 register.

When the Watchdog is activated during Sleep mode, the Sleep mode current consumption increases by about 20 µA compared to I_{VS_SLP}.

5.12.4. Wake-up Control Register

Name: WUCR
Offset: 0x04
Reset: 0x03
Property: R/W

Bit	7	6	5	4	3	2	1	0
	Reserved[7:2]						LINWUE	LOCWUE
Access	R	R	R	R	R	R	R/W	R/W
Reset	0	0	0	0	0	0	1	1

Bits 7:2 – Reserved[7:2]
Reserved, **do not modify reset value!**

Bit 1 – LINWUE
LIN Bus Remote Wake-Up Enable Control bit.

Value	Description
1	Activates the LIN bus remote wake-up.
0	Disables the LIN bus remote wake-up.

Bit 0 – LOCWUE
Local Wake-Up Enable Control bit.

Value	Description
1	Enables local wake up via the WAKE pin.
0	Disables local wake up via the WAKE pin.

5.13. Watchdog

The watchdog is used to monitor the proper functioning of the microcontroller and to trigger a reset if the microcontroller stops serving the watchdog due to a software lock-up or other malfunction. The NRES pin is pulled to low when a watchdog reset event is detected.

5.13.1. WATCHDOG BEHAVIOR DURING POWER-ON AND AFTER MCU RESET

For a safe start-up, the microcontroller must issue a watchdog trigger command, followed by the configuration of the watchdog via the WDCR registers. Following this, the device enters Device Standby mode. As soon as the MCP8048 enters Standby mode, the watchdog starts with a long open window (t_{LW}). **Within this long open window, the watchdog must be triggered.** If the watchdog trigger is missing, the watchdog will generate a Reset via the NRES pin. In case of a correct first trigger within the long open window time, the watchdog starts its normal operation.

The watchdog cannot be disabled and configured in the following cases:

- After the power-on of the device and before it receives the first trigger in Long Open Window mode.
- In all other cases when the watchdog is enabled and the device moves from MCU Reset mode to Standby mode, before the watchdog receives the first trigger.

If the WDLW bit from the Watchdog Control Register 1 is set to '1' (default value), the watchdog timer will always be reset when the Reset pulse time expires and starts the long open window after the device enters Standby mode. Otherwise, the watchdog will continue with its normal operation immediately and skip the long window.

5.13.2. WATCHDOG REGISTERS AND FEATURES

The built-in watchdog is activated by default and starts after powering on the device. The watchdog can be reconfigured or disabled only after power-on AND the first trigger.

The watchdog supports two operating modes:

- Window mode

  In Window mode, a watchdog trigger event within the watchdog trigger window resets the Watchdog Timer.

  The Window mode is only available in Normal mode.

- Timeout mode

  In Timeout mode, the watchdog can be triggered any time within the trigger range by a watchdog trigger.

Figure 5-13. Window Watchdog in Window Mode

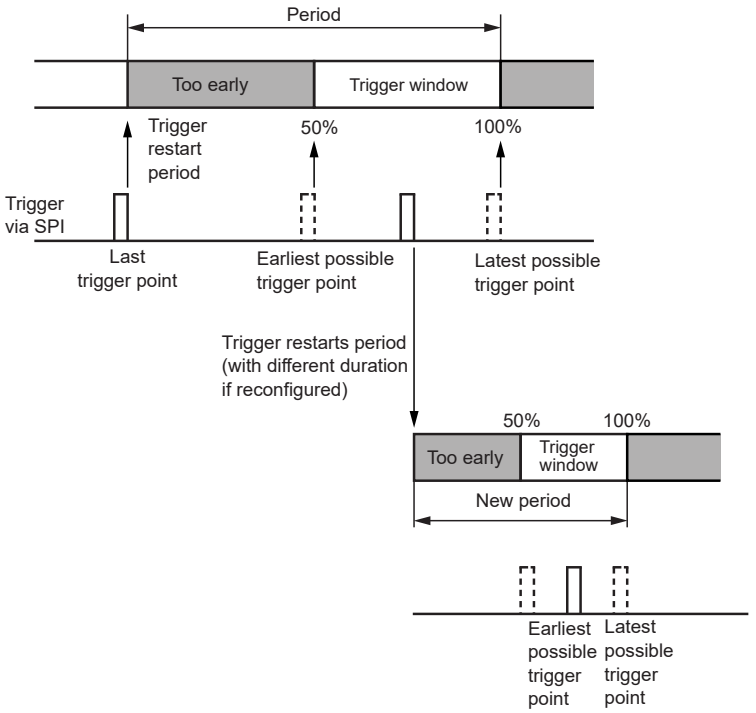
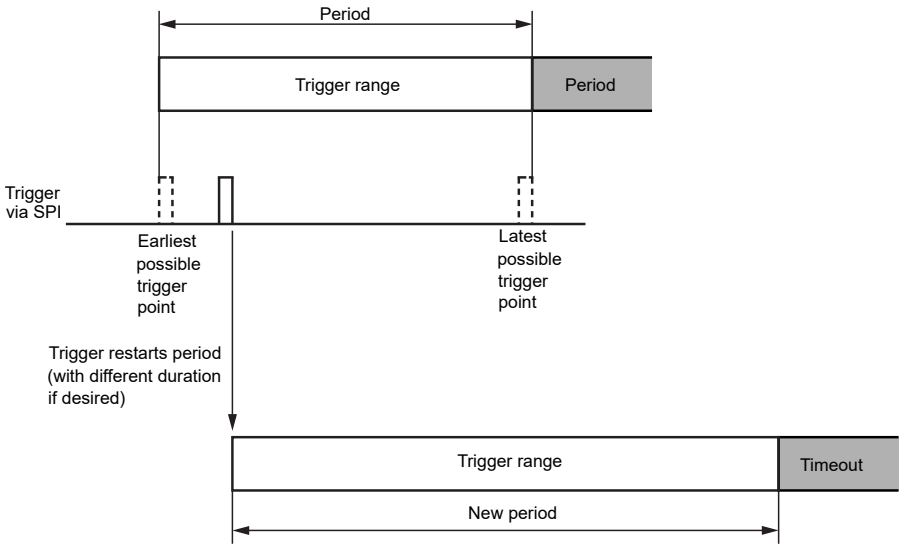


Figure 5-14. Window Watchdog in Timeout Mode



In order to avoid unwanted configuration of the watchdog, the MCP8048/MCP8049 only allows configuration of the watchdog (write access to WDCR1 and WDCR2 registers) when the device is in Standby mode.

Every write access to the WDCR1 and WDCR2 registers via SPI will reset the Watchdog Timer and immediately apply the changes.

If Window mode is selected (WDC = `100`), the watchdog will remain in (or switch to) Timeout mode until the device enters Normal mode (Window mode is only supported when the device is in Normal mode).

Any attempt to configure the watchdog (write access to WDCR1 register and WDCR2 register) while the device is not in Standby mode will trigger a reset of the microcontroller, and the device will set the ILLCON bit in the Watchdog Status register, WDSR (illegal watchdog configuration).

The MCP8048 watchdog supports eight watchdog periods. The watchdog period is programmable via the Watchdog Period bits (WWDP) in the Watchdog Control Register 2 (WDCR2). The selected period is valid for both Window and Timeout modes. The default watchdog period value is 128 ms.

A watchdog trigger event (an SPI write access to the WDTRIG register with the pattern (`01010101`) resets the Watchdog Timer. The Watchdog Reset pulse width is configured via the WRPL bits in the WDCR2 register.

The watchdog is an important safety mechanism that must be configured correctly. Two mechanisms are provided to prevent watchdog parameters from being changed by mistake.

- All configuration bitfields in the registers WDC, WWDP and WRPL have a Hamming distance of at least two for valid states.
- Reconfiguration protection: The configuration is only possible in Standby mode.

Having a Hamming distance of at least two for all valid states for the control bitfields, WDC, WWDP and WRPL, ensures that a single bit error cannot cause the watchdog to be configured incorrectly (at least two bits must be flipped to reconfigure WDC, WWDP or WRPL). If an attempt is made to write an invalid code to the WDCR1 register or WDCR2 register, the SPI write to the WDCRx register is ignored and the CACC bit in the Watchdog Status register is set.

Writing '`1`' to the corresponding bit of the Watchdog Status register will reset the bit.

A microcontroller reset is triggered immediately in response to an illegal watchdog configuration (configuration of the watchdog in Normal or Sleep mode), an incorrect watchdog trigger event

in Window mode (watchdog overflow or triggered too early) or when the watchdog overflows in Timeout mode. If a reset is triggered by the window watchdog the Window Watchdog Reset Event register will be set. The device will enter the µC Reset mode and enter Standby mode after the reset is finished.

If a reset is triggered by the watchdog, the respective reset event register will be set. The device will enter the MCU Reset mode, followed by Standby mode, after the reset takes place.

If there is a corrupted write access to the watchdog configuration registers and/or an illegal configuration of watchdog control register occurred when the watchdog is in OFF mode, the corresponding status register bit will be set.

If the fault register bits (CACC, ILLCON, OF, OFSLP and ETRIG bits – see WDSR) are not reset to zero before enabling the window watchdog, an MCU Reset will be triggered immediately after enabling the watchdog.

5.13.2.1. Watchdog Configuration Register 1

Name: WDCR1
Offset: 0x21
Reset: 0x42
Property: R/W

Bit	7	6	5	4	3	2	1	0
	WDC [7:5]			WDPRE [4:3]		WDSLP	WDLW	Reserved
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset	0	1	0	0	0	0	1	0

Bits 7:5 – WDC [7:5]
Watchdog Mode Control bits, set using the following bitfield values:

Value	Description
001	OFF mode
010	Timeout mode (default)
100	Window mode

Bits 4:3 – WDPRE [4:3]
Watchdog Period Control bits, set using the following bitfield values (extend watchdog period by the factor defined below) :

Value	Description
00	Watchdog prescale factor 1 (default)
01	Watchdog prescale factor 1.5
10	Watchdog prescale factor 2.5
11	Watchdog prescale factor 3.5

Bit 2 – WDSLP
Watchdog Control in Sleep Mode bit

Value	Description
1	Set to '1' to let the window watchdog run in Sleep mode.
0	Set to '0' to stop the window watchdog from running in Sleep mode.

5.13.2.1.4. WDLW

Trigger Window Length Control bit

Value	Description
1	After LH is released, the WDT is reset, and the first trigger window is long (t_{LW}).
0	After LH is released, the WDT is reset, and the first trigger window is standard (as configured by WDPRE and WWDP).

Bit 0 – Reserved
Reserved, **do not modify reset value!**

5.13.2.2. Watchdog Configuration Register 2

Name: WDCR2
Offset: 0x22
Reset: 0x41
Property: R/W

Bit	7	6	5	4	3	2	1	0
	WWDP [7:4]				WRPL [3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	1

Bits 7:4 – WWDP [7:4]
Watchdog Period Configuration bits (in ms, prescale factor = 1, ±20%):

Value	Description
1000	8 ms
0001	16 ms
0010	32 ms
1011	64 ms
0100	128 ms (default)
1101	256 ms
1110	1024 ms
0111	4096 ms

Bits 3:0 – WRPL [3:0]
Watchdog Reset Pulse Length bits (in ms, ±20%):

Value	Description
1000	1.25 ms
0001	4.3 ms (default)
0010	11.25 ms
1011	22.5 ms
0100	45 ms
1101	67.5 ms
1110	112.5 ms
0111	170 ms

5.13.2.3. Watchdog Status Register

Name: WDSR
Offset: 0x23
Reset: 0x0
Property: R, R/W

Bit	7	6	5	4	3	2	1	0
	OFF	CACC	ILLCON	TRIGS	OF	OFSLP	ETRIG	Reserved
Access	R	R/W	R/W	R	R/W	R/W	R/W	R
Reset	0	0	0	0	0	0	0	0

Bit 7 – OFF

Value is '1' when watchdog is OFF.

Value	Description
1	Watchdog is OFF.
0	Watchdog is ON.

Bit 6 – CACC

Corrupted write access to the watchdog configuration registers

Bit 5 – ILLCON

An attempt is made to reconfigure the watchdog control register while the device is not in Standby mode.

Bit 4 – TRIGS

Shows watchdog Window mode progress. If the watchdog is not in Window mode, this bit will always be set to '0'.

Value	Description
1	The device sets this bit to '1' if the Window mode watchdog is in the first half of the window.
0	The device sets this bit to '0' if the Window mode watchdog is in the second half of the window.

Bit 3 – OF

Watchdog overflow (Timeout/Window mode in Standby or Normal mode)

Bit 2 – OFSLP

Watchdog overflow in Sleep mode (Timeout mode)

Bit 1 – ETRIG

Watchdog triggered too early (Window mode)

Bit 0 – Reserved

Reserved, **do not modify reset value!**

5.13.2.4. Watchdog Trigger Register

Name: WDTRIG
Offset: 0x20
Reset: 0x0
Property: R/W

A watchdog trigger is an 8-bit wide SPI pattern written to the WDTRIG register. A valid watchdog trigger event resets the Watchdog Timer.

Bit	7	6	5	4	3	2	1	0
	WDTRIG [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – WDTRIG [7:0]
The only valid trigger pattern is **0b01010101**.

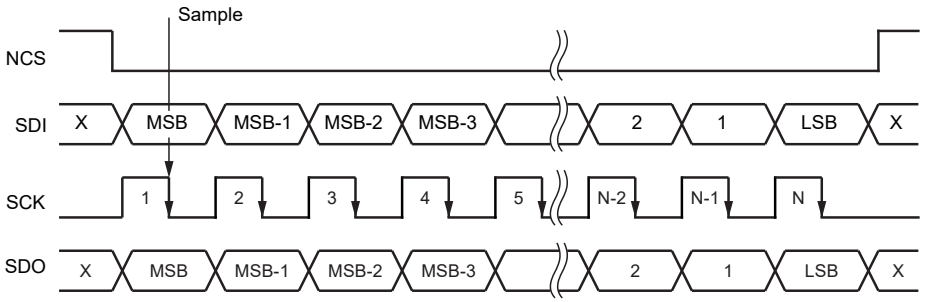
5.14. Serial Peripheral Interface (SPI)

The SPI is used to communicate with a host microcontroller. The MCP8048/MCP8049 is configured and operated using SPI transfers. SPI transfers are disabled in Sleep and Deep Sleep modes.

The SPI allows full-duplex data transfer. Status information is returned when new control data are shifted in. The interface also offers read-only access, allowing registers to be read back without changing the register content.

Bit sampling is performed on the falling edge of the clock pin (SCK) and data is shifted in/out on the rising edge (see the figure below).

Figure 5-15. SPI Timing Protocol.



The SPI data is stored in dedicated 8-bit registers, and each register is assigned a unique 7-bit address. Sixteen bits must be transmitted to the device for a single register write operation.

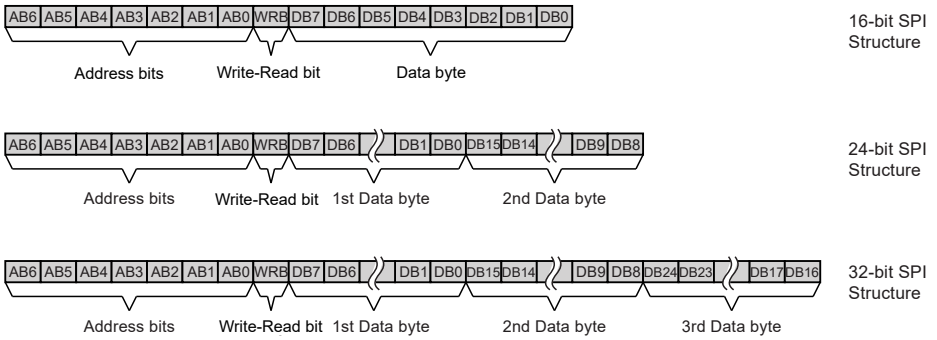
The **first byte** contain the 7-bit address along with a 'read/write' bit (the LSB). The write/read bit (WRB) must be '0' to indicate a write operation. If this bit is '1', a read operation is performed and any data after this bit is ignored.

The **second byte** contain the data meant to be written to the register. The contents of the addressed register(s) are returned via the SDO pin, while a read or write operation is performed.

For faster programming, 16, 24 and 32-bit read and write operations are supported. For 24 and 32-bit operations, the register address is automatically incremented: once for a 24-bit operation and twice for a 32-bit operation.

Attempting to write to a non-existing register is not prohibited. If the available address space is exceeded during a write operation, the data beyond the valid address range is ignored without generating an SPI failure event.

Figure 5-16. SPI Transfer Data Structure



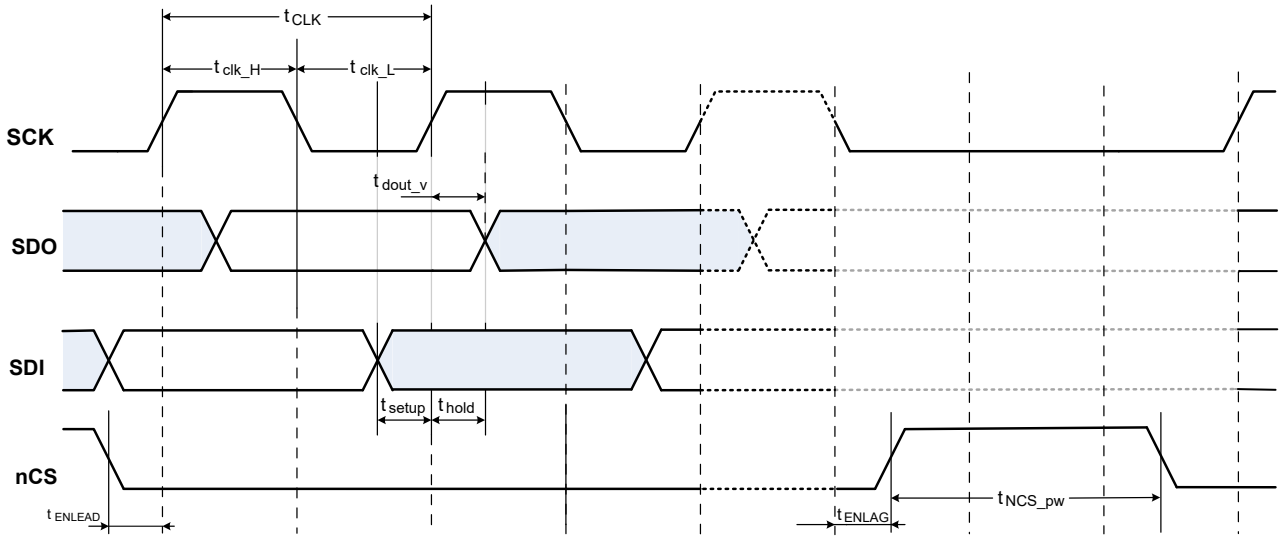
The number of transmitted SPI bits is monitored during SPI transfers. If the number of bits is not equal to 16, 24 or 32, the transfer is aborted.

An SPI failure event is captured (SPIF = '1', see SIR1 Register) if the SPI failure detection is enabled (SPIFECE = '1') and at least one of the following SPI failures is detected:

- SPI clock count error: only 16, 24 and 32-bit commands are valid for both read and write operation
- Illegal DOPM code (see DOPMCR Register)
- Attempted write access to locked register

If more than 32 bits are clocked in on the SDI pin during a read and write operation, the data stream on the SDI pin is looped back on the SDO pin from bit 33 onwards.

Figure 5-17. SPI Timing Diagram



SPI timing parameters can be found in SPI Timing section

For the full list of registers, see Register Summary.

5.15. Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	Reserved									
0x01	DOPMCR	7:0	RSTLVL	VDDIOOVSD	Reserved[5:3]			DOPM [2:0]		
0x02	LOPMCR	7:0	Reserved[7:3]					LTXD_DIS	LOPM [1:0]	
0x03	GOPMCR	7:0	Reserved[7:3]					GDUOPM [2:0]		
0x04	WUCR	7:0	Reserved[7:2]						LINWUE	LOCWUE
0x05	GDUCR1	7:0	CCPT [7:2]						CCEN	BEMFEN
0x06	GDUCR2	7:0	HSOFF	LSOFF	TSWTO [5:4]		EGBLT [3:0]			
0x07	GDUCR3	7:0	ADDTHS [7:6]		ADDTLS [5:4]		HSSRC [3:2]		LSSRC [1:0]	
0x08	GDUCR4	7:0	COMPEN	VDHOVSD	UVVGSEN	UVVGSLVL	VGSUVFLT [3:0]			
0x09	ILIMCR	7:0	ILIMEN	ILIMFLT [6:3]				ILIMSDEN	Reserved[1:0]	
0x0A	ILIMTH	7:0	Reserved	DAC [6:0]						
0x0B	SCPCR	7:0	SCSDEN	SCFLT [6:3]				SCTHSEL [2:0]		
0x0C	CSCR	7:0	CSA3EN	CSA2EN	CSA1EN	Reserved	OFFSET [3:2]		GAIN [1:0]	
0x0D	Reserved									
0x0E	MLDCR	7:0	Reserved	SOURCE3	SINK3	SOURCE2	SINK2	SOURCE1	SINK1	MLDEN
0x0F	RWPCR	7:0	Reserved[7:1]							WP0
0x10	DSR1	7:0	SMTS	VDD2OTPWS	VDD1OTPWS	GDUOTPWS	LOTPWS	GDUS	LTXDOUTS	LTXS
0x11	DSR2	7:0	Reserved	VDD2OVS	VDD1OVS	VDD2UVS	VDD1UVHS	VDD1UVLS	VGUVS	VCPUVS
0x12	MLDRR	7:0	Reserved[7:6]		DIAG3_HS	DIAG3_LS	DIAG2_HS	DIAG2_LS	DIAG1_HS	DIAG1_LS
0x13	SIR1	7:0	VSUPF	WAKE	SYS	ILIM	LDOF	OVTF	VDSSC	VGSUV
0x14	SIR2	7:0	Reserved	VDD2OV	VDD1OV	VDD2UV	VDD1UVH	VDD1UVL	Reserved[1:0]	
0x15	SIR3	7:0	VGUV	VCPUV	SCHS3	SCHS2	SCHS1	SCLS3	SCLS2	SCLS1
0x16	SIR4	7:0	OVTSDVDD2	OVTSDVDD1	OVTSDGDU	OVTSDL	OVTPWVDD2	OVTPWVDD1	OVTPWGDU	OVTPWL
0x17	SIR5	7:0	VDHOV	VSUV	LOCWU	LINWU	SPIF	PWRON	SYSERR	OSCF
0x18	SIECER1	7:0	GSCECE	VDHOVECE	ILIMECE	Reserved[4:3]		VSUVECE	SPIFECE	OVTPWECE
0x19	SIECER2	7:0	Reserved[7:5]			VDD2UVECE	VDD1UVHECE	VDD1UVLECE	VDD2OVECE	VDD1OVECE
0x1A ... 0x1F	Reserved									
0x20	WDTRIG	7:0	WDTRIG [7:0]							
0x21	WDCR1	7:0	WDC [7:5]			WDPRE [4:3]		WDSLP	WDLW	Reserved
0x22	WDCR2	7:0	WWDP [7:4]				WRPL [3:0]			
0x23	WDSR	7:0	OFF	CACC	ILLCON	TRIGS	OF	OFSLP	ETRIG	Reserved

5.16. Diagnostics and Protections

5.16.1. SLEEP MODE PROTECTION

The event detection should be configured correctly to ensure the response of the part to a wake-up event, from the Sleep mode or Deep Sleep mode. To avoid potential system deadlocks, at least one regular wake-up event must be enabled. All interrupt bits must be cleared before the device transitions into Sleep or Deep Sleep mode. In Deep Sleep mode, only local wake-up is supported. Otherwise, the device will switch to Standby mode in response to a Go-to-Sleep or Go-to-Deep-Sleep command (if DOPM = Sleep or Deep Sleep, see Device Operating Modes).

5.16.2. VS SUPPLY UNDERVOLTAGE PROTECTION

If $V_{VS} < V_{VS\_UV\_Set}$ has been detected, the device will:

- will switch the LIN transceiver to LIN Standby mode in case it worked in LIN Normal mode.
- Switch the GDU to GDU Standby mode, if it was in GDU Normal mode.
- Set the flag interrupt bit, VSUV (see SIR5 Register).
- In case the event capture enable register bit (VSUVECE) is set to '1' (see SIECER1 Register), an NIRQ interrupt will be generated.

5.16.3. VDH SUPPLY OVERVOLTAGE PROTECTION

The VDH supply overvoltage protection is active when setting the VDHOVSD bit to '1'. If a $V_{VDH} > V_{VDH\_OV\_Set}$ event occurs, the device will switch the GDU to GDU Standby mode (when in GDU Normal mode) and the charge pump will be deactivated (as long as the overvoltage condition is valid).

If the VDHOVSD bit is set to '0', the device will not react to the overvoltage event, the GDU will remain in Normal mode and the charge pump will keep operating. Only an NIRQ interrupt event will be generated, presuming the VDHOVECE bit is set to '1'.

The device will set the flag interrupt bit (VDHOV, see the SIR1 Register), presuming the VDHOVECE bit is set to '1', and an NIRQ interrupt event will be generated. Set the VDHOVECE bit to '0' to disable VDH overvoltage event capture.

VDH overvoltage monitoring is only active in Normal mode.

5.16.4. VDD1/VDD2 UNDERVOLTAGE AND OVERVOLTAGE PROTECTION

The MCP8048 provides various levels of VDD1 and VDD2 undervoltage monitoring. The feature is enabled by the RSTLVL bit.

If an undervoltage event has been detected at the VDD1 or VDD2 pin, the following will happen:

- The status bit VDDxUV (x = 1 or 2) and/or VDD1UVL (see SIR2 Register) will be set presuming the VDD1UVHECE or VDD2UVECE or VDD1UVLECE bit (see SIECER2 Register) is set to `1'.
- The NIRQ pin will be asserted if the corresponding interrupt event capture enable register bit is set (see SIR2 Register).
- The device will switch to MCU Reset mode, causing the GDU and the LIN transceiver to switch into GDU Standby mode.

If an overvoltage event has been detected at the VDD1 or VDD2 pin and if the VDDx is not used as VIO, the following will happen:

- The status bit VDDxOV (x = 1 or 2) (see SIR2 Register) will be set, presuming that the VDD1OVECE or VDD2OVECE bit (see SIECER2 Register) is set to '1'.

If an overvoltage event has been detected at the VDD1 or VDD2 pin when VDDIOOVSD is '0', and if the VDDx is used as VIO, the following will happen:

- The NIRQ pin will be asserted.
- The device will go in MCU Reset Mode

If an overvoltage event has been detected at the VDD1 or VDD2 pin (used as VIO) for longer than the overvoltage detection debouncing time, $t_{VDD1\_OV\_deb}$ or $t_{VDD2\_OV\_deb}$, the device is forced into Sleep mode, given that VDDIOOVSD is set to '1'. A number of actions are taken while switching into Sleep mode:

- All previously captured system interrupt events are cleared before the device switches to Sleep mode.
- Local wake up is enabled.
- LIN wake-up is enabled.
- Status bit SMTS is set to '1' (see DSR1 Register).
- The control register bit VDDIOOVSD (see DOPMCR Register) will be cleared, presuming the VDD1OVECE or VDD2OVECE bit is set to '1'.
- The status bit VDDxOV (x = 1 or 2) (see SIR2 Register) will be set, presuming that the VDD1OVECE or VDD2OVECE bit (see SIECER2 Register) is set to '1'.
- The NIRQ pin will be asserted. Setting the VDD1OVECE and/or VDD2OVECE bits to '0' will disable VDD1 and/or VDD2 overvoltage event capture, respectively.

5.16.5. VGS MONITORING AND EXTERNAL MOSFET PROTECTION

The MCP8048 monitors the gate supply voltage for each of the low and high-side external MOSFETs. The VG pin buffers the low-side gate supply voltage, whereas the VCP pin buffers the high-side gate supply voltage. The device provides two undervoltage detection thresholds, valid for both low and high-side gate supply voltages. The used threshold can be selected via the UVVGSLVL bit (see GDUCR4 Register).

A gate supply undervoltage condition for the low-side gate drivers occurs if $V_{VG} - V_{GND} < V_{VGS\_UV\_Set\_x}$.

A gate supply undervoltage condition for the high-side gate drivers occurs if $V_{VCP} - V_{VDH} < V_{VGS\_UV\_Set\_x}$.

In both cases:

- The GDU will be switched into GDU Standby mode.
- The gate control inputs NIHx and ILx are ignored.
- The according flag interrupt bit(s) VGUV and/or VCPUV will be set (see the SIR3 Register).
- The NIRQ pin will be asserted.

The external MOSFET gate source (VGS) undervoltage monitoring is active as soon as the VG and VCP regulators are enabled, and the UVVGSEN bit is set (see GDUCR4 Register). Both the VG and VCP regulators start operating when the transition to GDU Normal mode occurs. Transitioning to GDU Standby mode is not possible unless VG and VCP are within the valid range. The status of both VG and VCP output regulators can be seen in the DSR2 register (see DSR2 Register).

The VGS undervoltage event capturing is active in GDU Standby mode and GDU Normal mode. In GDU Standby mode, the VGS undervoltage event is filtered with $t_{VGS\_UV\_Blank\_ADO}$, ensuring the VG and VCP regulators ramp up properly. The delay filter is activated only once, when both VG and VCP regulators are activated. In case the VG and/or VCP regulator/s are not able to reach the requested voltage level (undervoltage level) within the filter time, NIRQ will be asserted.

UVVGSEN	VGS Monitoring
0	VGS monitoring deactivated – GDU state machine ignores all VGS UV events.
1	VGS monitoring activated – GDU switches into GDU Normal mode only if no VGS undervoltage has been detected.

5.16.6. OUTPUT CURRENT LIMITATION

The MCP8048 provides an output current limitation feature for monitoring the external power MOSFETs sum current. The output of OpAmp3 is internally connected to a comparator. The limitation voltage is set in the ILIMTH Register. The limitation feature is active in Device Normal mode as soon as it is activated via the ILIMEN bit, see the ILIMCR Register below.

On a current limitation event, different reactions can be configured, as follows:

- If the ILIMSDEN bit is set to '1' (latched behavior), the interrupt event is latched and the GDU will switch into GDU Standby mode.
- If the ILIMSDEN bit is set to '0' (unlatched behavior), GDU Normal mode is maintained, but the six GHx and GLx gate driver outputs are deactivated until ILIM condition is resolved.

The interrupt register bit "ILIM" (see SIR1 Register) will be set, and an interrupt will be generated under the following conditions:

- Unlatched fault handling (ILIMEN = '1' AND ILIMSDEN = '0') and ILIMECE bit is set to '1'; or
- Latched fault handling (ILIMEN = '1' AND ILIMSDEN = '1')

The interrupt register bit "ILIM" will be cleared under the following conditions:

- When any of the six gate driver outputs become active while the unlatched fault handling is enabled; or

- When the ILIM bit is set to '1' via SPI.

The MCP8048 will ignore any current limitation event if the ILIMEN bit is set to '0'.

The current limitation detection delay filter can be configured using ILIMFLT in the ILIMCR Register. The following table explains the ILIM control bits in more detail:

ILIMEN	ILIMECE	ILIMSDEN	Device Behavior
0	0/1	0	No action on current limitation events
0	0/1	1	No action on current limitation events
1	1	0	Interrupt generation, unlatched automatic fault handling, interrupt event delay is inactive as soon as the interrupt bit is reset by the gate control.
1	0	0	No interrupt, unlatched automatic fault handling
1	0/1	1	Interrupt generation and latched fault handling

5.16.6.1. Current Limitation Control Register

Name: ILIMCR
Offset: 0x09
Reset: 0xC4
Property: R/W

Bit	7	6	5	4	3	2	1	0
	ILIMEN	ILIMFLT [6:3]				ILIMSDEN	Reserved[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Reset	1	1	0	0	0	1	0	0

Bit 7 – ILIMEN

Current Limitation Enable bit

Value	Description
1	Activates the current limitation
0	Deactivates the current limitation

Bits 6:3 – ILIMFLT [6:3]

Current Limitation Filter Time bits: The filter times are configured according to Current Limitation Detection/Short Circuit Detection Time. The filter time starts after the current limitation threshold has been reached. If the sensed current drops below the detection threshold during the filter time, the filter time will be reset and restarted.

Bit 2 – ILIMSDEN

Current Limitation Shutdown Enable bit

Value	Description
1	The device will switch to GDU Standby mode and disable all gate drive outputs when a current limitation event has been detected.
0	The GDU stays in Normal mode when a current limitation event has been detected. In this case, the unlatched automatic fault handling is activated.

Bits 1:0 – Reserved[1:0]

Reserved, **do not modify reset value!**

5.16.6.2. Current Limitation Threshold Register

Name: ILIMTH
Offset: 0x0A
Reset: 0x0
Property: R/W

The formula used to calculate the current threshold through the external power MOSFETs:

$$V_{ILIM\_TH} = V_{DACd0} + \frac{V_{DACd127} - V_{DACd0}}{127} \sum_{x=0}^{6} DAC_x \times 2^x$$

Bit	7	6	5	4	3	2	1	0
	Reserved	DAC [6:0]						
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – Reserved

Reserved, **do not modify reset value!**

Bits 6:0 – DAC [6:0]

Current limitation threshold DAC input.

5.16.7. VDS DRAIN-SOURCE VOLTAGE MONITORING AND POWER STAGE SHORT CIRCUIT PROTECTION

Short circuits in the half-bridge circuitry are monitored by sensing the voltage drop across the drain source of the external high-side and low-side MOSFETs. Comparators monitor the voltage drop between the drain (VDH) and the source terminals (SHx) of the external high-side MOSFET transistors, as well as between the external low-side MOSFET transistors drain (SHx) and source (GND in MCP8049 or SL in MCP8048). The voltage drop is monitored during the ON phase of the MOSFET, according to the ILx and NIHx pins.

The voltage drop is compared with the reference voltage. As soon as one of the drain-source voltage drops exceed the V_{SCREF} threshold, a short circuit in this branch is detected.

The Short Circuit Reference Threshold (V_{SCREF}) can be configured via SPI, using the SCTHSEL [2:0] bits (see table Short Circuit Detection Threshold).

The following actions occur in case of a short circuit event. The corresponding interrupt register will be set according to the SIR3 Register. The short circuit event will be signaled at the interrupt output pin (NIRQ). The GDU will be switched to GDU Standby mode, and all gate driver outputs will be disabled if SCSDEN bit is set to '1'. If the SCSDEN bit is set to '0', the device will only indicate the event at the NIRQ pin, and the gate control will not be disabled.

To prevent false short circuit triggering, a VDS Drain-Source Short Circuit event is blanked out with the edge blanking time using the EGBLT bits (GDUCR2 Register). Furthermore, the VDS short circuit event is filtered, and the filter time can be configured using the SCFLT[3:0] bits (see the SCPCR Register).

5.16.7.1. Short Circuit Protection Control Register

Name: SCPCR
Offset: 0x0B
Reset: 0x40
Property: R/W

Bit	7	6	5	4	3	2	1	0
	SCSDEN	SCFLT [6:3]				SCTHSEL [2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

Bit 7 – SCSDEN

Short Circuit Shutdown Enable bit

Value	Description
1	All gate driver outputs are disabled as soon as a short circuit failure is detected.
0	The short circuit event will only be indicated through the NIRQ pin.

Bits 6:3 – SCFLT [6:3]

Short Circuit Filter Time bits: The filter time needs to be configured according to Current Limitation Detection/Short Circuit Detection Time. The filter time starts after the edge blanking time (t_{EG_Blank}) has expired and a VDS voltage larger than V_{SCREF} has been detected. If the sensed voltage drops below the detection threshold during the filter time, the filter timer will be reset and will restart when another short circuit event occurs.

Bits 2:0 – SCTHSEL [2:0]

Short Circuit Detection Threshold bits (V_{SCREF}), in mV

Value	Description
3'b000	125 mV (default)
3'b001	250 mV
3'b010	500 mV
3'b011	750 mV
3'b100	1000 mV
3'b101	1250 mV
3'b110	1500 mV
3'b111	1750 mV

5.16.8. TEMPERATURE MONITORING AND OVERTEMPERATURE PROTECTION

The device offers two overtemperature detection thresholds, a pre-warning and a shutdown threshold. Thermal sensors are placed at different locations on the die: LIN transceiver, VDD1 LDO, VDD2 LDO and GDU.

If the temperature of one or more of the thermal sensors exceeds the overtemperature pre-warning threshold ($T_J > T_{OT\_PREW\_Set}$), the device will set the common pre-warning bit (OTPWS = '1', see DSR1 Register) and the corresponding interrupt bits (VDD1OTPWS and/or VDD2OTPWS and/or GDUOTPWS, see DSR1 Register). An overtemperature pre-warning interrupt will be generated at the NIRQ pin when the corresponding interrupt event capture enable register is set (see SIECER1 Register). The OTPWS bit is not latched and will be set to '0' as soon as the temperature of all monitored circuit parts decreases below the overtemperature protection pre-warning threshold.

If the temperature of one or more of the thermal sensors exceeds the overtemperature shutdown threshold (T_{OT_sdwn}), the overtemperature shutdown protection will be triggered for the corresponding circuit parts. This will trigger the following events:

- The integrated LIN transceiver switches into LIN Standby mode if the LIN transceiver overtemperature shutdown has been triggered.
- The VDD1 regulator is disabled if the VDD1 regulator overtemperature shutdown has been triggered.
- The VDD2 regulator, if available, is disabled when the VDD2 regulator overtemperature shutdown has been triggered.
- The GDU is switched to GDU Standby mode when the GDU overtemperature shutdown has been triggered.
- At the same time, the corresponding overtemperature shutdown interrupt register will be set (see SIR4 Register).
- NIRQ pin will be asserted.

Wake-up events are still detected in case of an overtemperature occurrence. A wake-up event will be signaled by asserting the NIRQ pin.

5.16.9. INTERRUPT/WAKE-UP EVENT DELAY (NIRQ)

Frequent interrupt or wake-up events can require significant microcontroller processing time because the NIRQ pin is asserted each time an interrupt/wake-up event is generated. Therefore, the device incorporates an interrupt/wake-up delay timer ($t_{d\_evt\_cap}$) to limit the frequency of interrupt events.

When one of the event capture status bits is cleared, the NIRQ pin is deasserted, and the event delay timer starts. If further events occur while the event delay timer is running, the relevant status bits are set and NIRQ stays deasserted. As soon as the event timer expires, and one or more events are pending, the NIRQ pin is asserted again to alert the microcontroller.

We use the term microcontroller often in this data sheet without referring to a host. Mentioning a host is only necessary when discussing the SPI host.

This way, the microcontroller is interrupted only once to process several events, rather than several times to process each individual event. If the microcontroller has cleared all active event capture bits before the event delay timer expires, the NIRQ pin remains deasserted, presuming no new or pending events occurred.

The event capture registers can be read at any time.

5.16.10. LOSS OF POWER AT PIN VS

In case of a loss of power at the pin VS, the LIN bus and the I/O pins are tri-stated. No reverse currents will flow from the LIN bus into the device. There will be no backward supply from the LIN pin into the MCP8048.

5.16.11. PROTECTION AND FAULT EVENT REGISTERS

There are several types of registers:

- System Interrupt Event Capture Enable Registers used for interrupt configuration: SIECER1 and SIECER2
- System Interrupt Registers used for diagnostics feedback: SIR1-SIR5
- Device Status Registers used for hardware fault status feedback: DSR1 and DSR2

The registers are accessible via the SPI interface.

5.16.11.1. System Interrupt Event Capture Enable Register 1

Name: SIECER1
Offset: 0x18
Reset: 0xE7
Property: R/W

Bit	7	6	5	4	3	2	1	0
	GSCECE	VDHOVECE	ILIMECE	Reserved[4:3]		VSUVECE	SPIFECE	OVTPWECE
Access	R/W	R/W	R/W	R	R	R/W	R/W	R/W
Reset	1	1	1	0	0	1	1	1

Bit 7 – GSCECE
General Short Circuit Failure Event Capture Enable bit. Default value '1'. By clearing the **GSCECE** bit, the short circuit fault capture for all branches of the external MOSFET bridge will be disabled.

Bit 6 – VDHOVECE
VDH Overvoltage Failure Event Capture Enable bit ($V_{VDH} > V_{VDH\_OV\_Set}$)

Value	Description
1	Enables VDH overvoltage event capture
0	Disables VDH overvoltage event capture

Bit 5 – ILIMECE
Current Limitation Event Capture Enable Register bit

Value	Description
1	Enables current limitation event capture
0	Disables current limitation event capture

Bits 4:3 – Reserved[4:3]
Reserved, **do not modify reset value!**

Bit 2 – VSUVECE
VS Undervoltage Failure Event Capture Enable bit ($V_{VS} < V_{VS\_UV\_Set}$)

Value	Description
1	Enables VS undervoltage event capture
0	Disables VS undervoltage event capture

Bit 1 – SPIFECE
SPI Failure Event Capture Enable Register bit

Value	Description
1	Enables SPI failure interrupt
0	Disables SPI failure interrupt

Bit 0 – OVTPWECE
Overtemperature Pre-warning Event Capture Enable bit

Value	Description
1	Enables overtemperature pre-warning event capture
0	Disables overtemperature pre-warning event capture

5.16.11.2. System Interrupt Event Capture Enable Register 2

Name: SIECER2
Offset: 0x19
Reset: 0x1F
Property: R/W

Bit	7	6	5	4	3	2	1	0
	Reserved[7:5]			VDD2UVECE	VDD1UVHECE	VDD1UVLECE	VDD2OVECE	VDD1OVECE
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	1	1	1	1

Bits 7:5 – Reserved[7:5]
Reserved, **do not modify reset value!**

Bit 4 – VDD2UVECE
VDD2 Undervoltage Event Capture Enable bit ($V_{VDD2} < V_{VDD2\_UV\_IO\_Set}$)

Value	Description
1	Enables VDD2 undervoltage event capture
0	Disables VDD2 undervoltage event capture

Bit 3 – VDD1UVHECE
VDD1 Undervoltage ($V_{VDD1} < V_{VDD1\_UV\_Set}$) Event Capture Enable bit

Value	Description
1	Enables VDD1 undervoltage event capture
0	Disables VDD1 undervoltage event capture

Bit 2 – VDD1UVLECE
VDD1 IO Undervoltage ($V_{VDD1} < V_{VDD1\_UV\_IO\_Set}$) Event Capture Enable bit

Value	Description
1	Enables VDD1 IO undervoltage event capture
0	Disables VDD1 IO undervoltage event capture

Bit 1 – VDD2OVECE
VDD2 Overvoltage Event Capture Enable bit ($V_{VDD2} > V_{VDD2\_OV\_Set}$).

Value	Description
1	Enables VDD2 overvoltage event capture
0	Disables VDD2 overvoltage event capture

Bit 0 – VDD1OVECE
VDD1 Overvoltage Event Capture Enable bit ($V_{VDD1} > V_{VDD1\_OV\_Set}$).

Value	Description
1	Enables VDD1 overvoltage event capture
0	Disables VDD1 overvoltage event capture

5.16.11.3. System Interrupt Register 1

Name: SIR1
Offset: 0x13
Reset: 0x20
Property: R, R/W

The SIR1 register shows the overall failure interrupt events. The bits are not latched, except for bit 4 (ILIM). The state of these flags is the result of the OR-ed operation with the latched bits from SIR2, SIR3, SIR4 and SIR5. The SIR1 bits will be automatically cleared after the corresponding SIR2-SIR5 bits are cleared.

Bit	7	6	5	4	3	2	1	0
	VSUPF	WAKE	SYS	ILIM	LDOF	OVTF	VDSSC	VGSUV
Access	R	R	R	R/W	R	R	R	R
Reset	0	0	1	0	0	0	0	0

Bit 7 – VSUPF

IC Supply Failure Event Interrupt bit

Value	Description
1	SIR5[7] and/or SIR5[6] bits are set to '1'.
0	Both SIR5[7] and SIR5[6] bits are cleared.

Bit 6 – WAKE

Wake-Up Event Interrupt bit

Value	Description
1	SIR5[5] and/or SIR5[4] bits are set to '1'.
0	Both SIR5[5] and SIR5[4] are cleared.

Bit 5 – SYS

System Event Interrupt bit

Value	Description
1	SIR5[3] and/or SIR5[2] and/or SIR5[1] bits are set to '1'.
0	SIR5[3:1] is cleared.

Bit 4 – ILIM

Power Stage Current Limitation Interrupt bit

Value	Description
1	A power stage current limitation event has been detected.
0	The bit is reset to '0' by writing a '1' to the bit or, when unlatched current limitation handling has been enabled, the ILIM bit will be cleared when any of the six gate control driver outputs are activated.

Bit 3 – LDOF

LDO Failure Event Interrupt bit

Value	Description
1	Any SIR2 register bits are set to '1'.
0	All of the SIR2 register bits are reset to '0'.

Bit 2 – OVTF

Overtemperature Failure Event Interrupt bit

Value	Description
1	Any of the SIR4 register bits are set to '1'.
0	All of the SIR4 register bits are reset to '0'.

Bit 1 – VDSSC

Drain-Source Monitoring VDS Short Circuit Interrupt bit

Value	Description
1	A VDS short circuit failure has been detected by at least one bit in SIR3[5:0] (at least one bit is set to '1').
0	All of the bits in SIR3[5:0] are cleared.

5.16.11.3.8. VGSUV

Gate-Source Monitoring VGS Undervoltage Interrupt bit

Value	Description
1	A VGS undervoltage failure has been detected by at least one bit in SIR3[7:6] (at least one bit is set to '1').
0	Both of the bits in SIR3[7:6] are cleared.

5.16.11.4. System Interrupt Register 2

Name: SIR2
Offset: 0x14
Reset: 0x0
Property: R/W

Bit	7	6	5	4	3	2	1	0
	Reserved	VDD2OV	VDD1OV	VDD2UV	VDD1UVH	VDD1UVL	Reserved[1:0]	
Access	R	R/W	R/W	R/W	R/W	R/W	R	R
Reset	0	0	0	0	0	0	0	0

Bit 7 – Reserved
Reserved, **do not modify reset value!**

Bit 6 – VDD2OV
VDD2 Overvoltage Event Interrupt bit

Value	Description
1	An overvoltage event has been detected at the VDD2 pin **AND** the VDD2OVECE bit set to '1'.
0	The bit is reset to '0' by writing a '1' to it.

Bit 5 – VDD1OV
VDD1 Overvoltage Event Interrupt bit

Value	Description
1	An overvoltage event has been detected at the VDD1 pin **AND** the VDD1OVECE bit set to '1'.
0	The bit is reset to '0' by writing a '1' to it.

Bit 4 – VDD2UV
VDD2 Undervoltage Event Interrupt bit

Value	Description
1	An undervoltage event has been detected at the VDD2 pin **AND** the VDD2UVECE bit set to '1'.
0	The bit is reset to '0' by writing a '1' to it.

Bit 3 – VDD1UVH
VDD1 Undervoltage Event Interrupt bit ($V_{VDD1} < V_{VDD1\_UV\_Set}$)

Value	Description
1	An undervoltage event has been detected at the VDD1 pin **AND** the VDD1UVHECE bit set to '1'.
0	The bit is reset to '0' by writing a '1' to it.

Bit 2 – VDD1UVL
VDD1 IO Undervoltage Event Interrupt bit ($V_{VDD1} < V_{VDD1\_UV\_IO\_Set}$)

Value	Description
1	An undervoltage event has been detected at the VDD1 pin **AND** the VDD1UVLECE bit set to '1'.
0	The bit is reset to '0' by writing a '1' to it.

Bits 1:0 – Reserved[1:0]
Reserved, **do not modify reset value!**

5.16.11.5. System Interrupt Register 3

Name: SIR3
Offset: 0x15
Reset: 0x0
Property: R/W

Bit	7	6	5	4	3	2	1	0
	VGUV	VCPUV	SCHS3	SCHS2	SCHS1	SCLS3	SCLS2	SCLS1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – VGUV

VG Undervoltage Interrupt bit ($V_{VG} - V_{GND}$) < $V_{VGS\_UV\_Set\_x}$

Value	Description
1	A VG undervoltage event has been detected.
0	The bit is reset to '0' by writing a '1' to it.

Bit 6 – VCPUV

VCP Undervoltage Interrupt bit ($V_{VCP} - V_{VDH}$) < $V_{VGS\_UV\_Set\_x}$

Value	Description
1	A VCP undervoltage event has been detected.
0	The bit is reset to '0' by writing a '1' to it.

Bit 5 – SCHS3

Power Stage High-Side External MOSFET Short Circuit Interrupt bit

Value	Description
1	A short circuit has been detected for the corresponding external MOSFET (HS3).
0	The bit is reset to '0' by writing a '1' to it.

Bit 4 – SCHS2

Power Stage High-Side External MOSFET Short Circuit Interrupt bit

Value	Description
1	A short circuit has been detected for the corresponding external MOSFET (HS2).
0	The bit is reset to '0' by writing a '1' to it.

Bit 3 – SCHS1

Power Stage High-Side External MOSFET Short Circuit Interrupt bit

Value	Description
1	A short circuit has been detected for the corresponding external MOSFET (HS1).
0	The bit is reset to '0' by writing a '1' to it.

Bit 2 – SCLS3

Power Stage Low-Side External MOSFET Short Circuit Interrupt bit

Value	Description
1	A short circuit has been detected for the corresponding external MOSFET (LS3).
0	The bit is reset to '0' by writing a '1' to it.

Bit 1 – SCLS2

Power Stage Low-Side External MOSFET Short Circuit Interrupt bit

Value	Description
1	A short circuit has been detected for the corresponding external MOSFET (LS2).
0	The bit is reset to '0' by writing a '1' to it.

Bit 0 – SCLS1

Power Stage Low-Side External MOSFET Short Circuit Interrupt bit

Value	Description
1	A short circuit has been detected for the corresponding external MOSFET (LS1).
0	The bit is reset to '0' by writing a '1' to it.

5.16.11.6. System Interrupt Register 4

Name: SIR4
Offset: 0x16
Reset: 0x0
Property: R/W

Bit	7	6	5	4	3	2	1	0
	OVTSDVDD2	OVTSDVDD1	OVTSDGDU	OVTSDL	OVTPWVDD2	OVTPWVDD1	OVTPWGDU	OVTPWL
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – OVTSDVDD2

VDD2 Regulator Overtemperature Shutdown Interrupt bit

Value	Description
1	The bit is set to '1' if the VDD2 regulator junction temperature exceeds the overtemperature shutdown threshold (T_{OT_sdwn}).
0	The bit is reset to '0' by writing a '1' to it.

Bit 6 – OVTSDVDD1

VDD1 Regulator Overtemperature Shutdown Interrupt bit

Value	Description
1	The bit is set to '1' if the VDD1 regulator junction temperature exceeds the overtemperature shutdown threshold (T_{OT_sdwn}).
0	The bit is reset to '0' by writing a '1' to it.

Bit 5 – OVTSDGDU

GDU Overtemperature Shutdown Interrupt bit

Value	Description
1	The bit is set to '1' if the GDU junction temperature exceeds the overtemperature shutdown threshold (T_{OT_sdwn}).
0	The bit is reset to '0' by writing a '1' to it.

Bit 4 – OVTSDL

LIN Transceiver Overtemperature Shutdown Interrupt bit

Value	Description
1	The bit is set to '1' if the LIN transceiver junction temperature exceeds the overtemperature shutdown threshold (T_{OT_sdwn}).
0	The bit is reset to '0' by writing a '1' to it.

Bit 3 – OVTPWVDD2

VDD2 Regulator Overtemperature Prewarning Interrupt bit

Value	Description
1	The bit is set to '1' if the VDD2 regulator junction temperature exceeds the overtemperature prewarning threshold ($T_{OT\_PREW\_Set}$).
0	The bit is reset to '0' by writing a '1' to it.

Bit 2 – OVTPWVDD1

VDD1 Regulator Overtemperature Prewarning Interrupt bit

Value	Description
1	The bit is set to '1' if the VDD1 regulator junction temperature exceeds the overtemperature prewarning threshold ($T_{OT\_PREW\_Set}$).
0	The bit is reset to '0' by writing a '1' to it.

Bit 1 – OVTPWGDU

GDU Overtemperature Prewarning Interrupt bit

Value	Description
1	The bit is set to '1' if the GDU junction temperature exceeds the overtemperature prewarning threshold ($T_{OT\_PREW\_Set}$) **AND** the OVTPWECE bit is set to '1'.
0	The bit is reset to '0' by writing a '1' to it.

Bit 0 – OVTPWL

LIN Transceiver Overtemperature Prewarning Interrupt bit

Value	Description
1	The bit is set to '1' if the LIN transceiver junction temperature exceeds the overtemperature prewarning threshold ($T_{OT\_PREW\_Set}$) **AND** the OVTPWECE bit is set to '1'.
0	The bit is reset to '0' by writing a '1' to it.

5.16.11.7. System Interrupt Register 5

Name: SIR5
Offset: 0x17
Reset: 0x04
Property: R/W

Bit	7	6	5	4	3	2	1	0
	VDHOV	VSUV	LOCWU	LINWU	SPIF	PWRON	SYSERR	OSCF
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	0	0

Bit 7 – VDHOV
VDH Overvoltage Interrupt bit

Value	Description
1	The bit is set to '1' if a VDH overvoltage event occurs **AND** the VDHOVECE bit is set to '1'.
0	The bit is reset to '0' by writing a '1' to it.

5.16.11.7.2. VSUV
VS Undervoltage Interrupt bit

Value	Description
1	The bit is set to '1' if VS drops below the threshold $V_{VS\_UV\_Set}$ for longer than the fault blanking time **AND** the VSUVECE bit is set to '1'.
0	The bit is reset to '0' by writing a '1' to it.

Bit 5 – LOCWU
Local Wake-Up Interrupt bit

Value	Description
1	The bit is set to '1' if a local wake-up event occurs **AND** the local wake-up detection is enabled.
0	The bit is reset to '0' by writing a '1' to it.

Bit 4 – LINWU
LIN Bus Wake-Up Interrupt bit

Value	Description
1	The bit is set to '1' if a LIN wake-up event occurs **AND** the LIN bus wake-up detection is enabled.
0	The bit is reset to '0' by writing a '1' to it.

Bit 3 – SPIF
SPI Failure Interrupt bit

Value	Description
1	The bit is set to '1' if an SPI failure has been detected **AND** the SPIFECE bit is set to '1'.
0	The bit is reset to '0' by writing a '1' to it.

Bit 2 – PWRON
Power-On Interrupt bit

Value	Description
1	The bit is set to '1' if the device is no longer in the Power OFF mode.
0	The bit is reset to '0' by writing a '1' to it.

Bit 1 – SYSERR

Internal System Error Status bit

Value	Description
1	The bit is set to '1' in the following cases: • The parity check to IC trimming data registers has failed. • An internal voltage regulator failure has been detected. • An illegal internal digital state has been detected. The NIRQ pin is asserted as long as the bit is set to '1'.
0	The bit is not latched and will automatically reset to '0' if the fault is no longer present.

Bit 0 – OSCF

Internal System Clock Failure Status bit

Value	Description
1	The bit is set to '1' if the system clock is missing. Interrupt at the NIRQ pin will be generated even without an internal system clock. The bit can be read via SPI.
0	The bit is not latched and will automatically reset to '0' as soon as the internal system clock recovers.

5.16.11.8. Device Status Register 1

Name: DSR1
Offset: 0x10
Reset: 0x0
Property: R

Bit	7	6	5	4	3	2	1	0
	SMTS	VDD2OTPWS	VDD1OTPWS	GDUOTPWS	LOTPWS	GDUS	LTXDOUTS	LTXS
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 7 – SMTS

Sleep Mode Transition Status bit

Value	Description
1	The prior transition to Sleep mode was forced by a VIO overvoltage event.
0	The prior transition to Sleep mode was triggered by an SPI command.

Bit 6 – VDD2OTPWS

VDD2 Regulator Overtemperature Prewarning Status bit

Value	Description
1	The junction temperature of the VDD2 regulator exceeds the overtemperature prewarning level ($T_{OT\_PREW\_Set}$).
0	The bit is reset to '0' as soon as the junction temperature drops below the overtemperature prewarning clear level ($T_{OT\_PREW\_Clear}$).

Bit 5 – VDD1OTPWS

VDD1 Regulator Overtemperature Prewarning Status bit

Value	Description
1	The junction temperature of the VDD1 regulator exceeds the overtemperature pre-warning level ($T_{OT\_PREW\_Set}$).
0	The bit is reset to '0' as soon as the junction temperature drops below the overtemperature pre-warning clear level ($T_{OT\_PREW\_Clear}$).

Bit 4 – GDUOTPWS

GDU Overtemperature Prewarning Status bits

Value	Description
1	The junction temperature of the GDU exceeds the overtemperature pre-warning level ($T_{OT\_PREW\_Set}$).
0	The bit is reset to '0' as soon as the junction temperature drops below the overtemperature pre-warning clear level ($T_{OT\_PREW\_Clear}$).

Bit 3 – LOTPWS

LIN Transceiver Overtemperature Prewarning Status bit

Value	Description
1	The junction temperature of the LIN transceiver exceeds the overtemperature pre-warning level ($T_{OT\_PREW\_Set}$).
0	The bit is reset to '0' as soon as the junction temperature drops below the overtemperature pre-warning clear level ($T_{OT\_PREW\_Clear}$).

Bit 2 – GDUS

GDU Status bit

Value	Description
1	Set to '1' as soon as the GDU is ready to drive the gate of the external MOSFETs.
0	Indicates the GDU is not ready yet to drive the gate of the external MOSFETs.

Bit 1 – LTXDOUTS

TXD Timeout Status bit

Value	Description
1	The LIN transceiver is disabled due to a TXD dominant timeout event.
0	Indicates no TXD dominant timeout event is present.

Bit 0 – LTXS

LIN Transceiver Status bit

Value	Description
1	The LIN transceiver is ready to transmit and receive data.
0	Indicates no TXD the LIN transceiver is not ready yet to transmit and receive data.

5.16.11.9. Device Status Register 2

Name: DSR2
Offset: 0x11
Reset: 0x0
Property: R

Bit	7	6	5	4	3	2	1	0
	Reserved	VDD2OVS	VDD1OVS	VDD2UVS	VDD1UVHS	VDD1UVLS	VGUVS	VCPUVS
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 7 – Reserved

Reserved, **do not modify reset value!**

Bit 6 – VDD2OVS

VDD2 Overvoltage Status bit

Value	Description
1	VDD2 overvoltage is detected.
0	VDD2 voltage is below the overvoltage clear level.

Bit 5 – VDD1OVS

VDD1 Overvoltage Status bit

Value	Description
1	VDD1 overvoltage is detected.
0	VDD1 voltage is below the overvoltage clear level.

Bit 4 – VDD2UVS

VDD2 Undervoltage Status bit

Value	Description
1	VDD2 undervoltage is detected.
0	VDD2 voltage is above the undervoltage clear level.

Bit 3 – VDD1UVHS

VDD1 Undervoltage Status bit ($V_{VDD1} < V_{VDD1\_UV\_Set}$)

Value	Description
1	VDD1 undervoltage is detected.
0	VDD1 voltage is above the undervoltage clear level ($V_{VDD1} > V_{VDD1\_UV\_Clear}$).

Bit 2 – VDD1UVLS

VDD1 IO Undervoltage Status bit ($V_{VDD1} < V_{VDD1\_UV\_IO\_Set}$)

Value	Description
1	VDD1 IO undervoltage is detected,
0	VDD1 voltage is above the undervoltage clear level ($V_{VDD1} > V_{VDD1\_UV\_IO\_Clear}$),

Bit 1 – VGUVS

VG Undervoltage Status bit

Value	Description
1	VG undervoltage is detected.
0	VG voltage level is higher than the $V_{VGS\_UV\_Clear\_H}$ threshold.

Bit 0 – VCPUVS

VCP Undervoltage Status bit

Value	Description
1	VCP undervoltage is detected.
0	VCP voltage level is higher than the $V_{VGS\_UV\_Clear\_H}$ threshold.

5.16.11.10. Register Write Protection Control Register

Name: RWPCR
Offset: 0x0F
Reset: 0x0
Property: R/W

Sections of the register address area can be write-protected to prevent unintended modifications.

Bit	7	6	5	4	3	2	1	0
	Reserved[7:1]							WP0
Access	R	R	R	R	R	R	R	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:1 – Reserved[7:1]
Reserved, **do not modify reset value!**

Bit 0 – WP0
Write Protection Settings bit

Value	Description
1	Disables register write access to register address areas 0x01 to 0x0E, 0x21 and 0x22.
0	Enables write access to the registers above.

5.16.12. CROSS CONDUCTION PROTECTION

Static Cross Conduction Timers

Cross conduction timers at every drive stage prevent switching ON any output driver for a time (t_{CC}) after the counterpart driver in the same phase has been switched OFF. The cross conduction timers are also active in case a short circuit is detected.

The edge blanking time can be configured as shown in the table below:

Table 5-4. Current Limitation Detection/Short Circuit Detection Time

ILIMFLT [3:0], SCFLT [3:0], EGBLT [3:0]	Blanking/Filter time (ns), typical (±5%)
4'b0000	0 ns
4'b0001	250 ns
4'b0010	500 ns
4'b0011	750 ns
4'b0100	1000 ns
4'b0101	1250 ns
4'b0110	1500 ns
4'b0111	1750 ns
4'b1000	2000 ns
4'b1001	2500 ns
4'b1010	3000 ns
4'b1011	3500 ns
4'b1100	4000 ns
4'b1101	5000 ns
4'b1110	6000 ns
4'b1111	8000 ns

Adaptive Dead-Time Control

The static cross conduction timers can be replaced by adaptive dead-time control. The adaptive dead-time comparators monitor voltages on the gate drive outputs and switch node to determine when to switch the MOSFETs ON and OFF.

To prevent cross conduction when turning ON high side switches, the MCP8048/MCP8049 monitors the low side MOSFETs gate source voltage (V_{GLx} – V_{SL}(MCP8048) or V_{GND}(MCP8049)) and prevents turning ON the high side MOSFET in the same branch until the gate source voltage of the low-side switch is lower than V_{LOOFF}.

To prevent cross conduction when switching ON low-side switches, the MCP8048/MCP8049 monitors the voltage on the SHx switching node. The low-side gate drive can only be switched on when the SHx switching node voltage drops below V_{SWTH}. Once the low-side gate drive is switched on, it is latched until the NIHx signal goes low. This prevents any ringing or oscillations on the switch node or the SHx pin from turning OFF the GSx driver. If the NIHx pin goes high and the voltage on the SHx pin does not cross the V_{SWTH} threshold, the low-side gate drive is deactivated automatically after the Adaptive Deadtime Force To Switch Delay Time (t_{SWTO}) has passed.

Figure 5-18. Adaptive Dead Time Timing Diagram

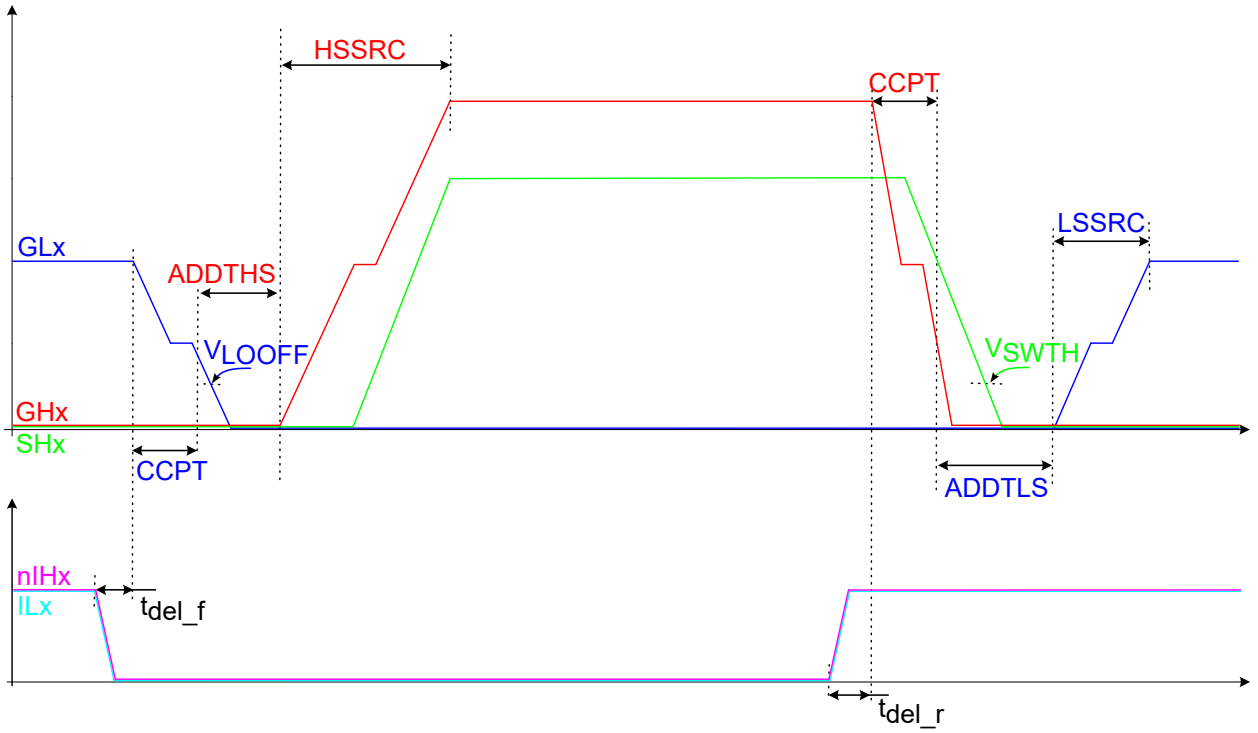


Figure 5-19. MCP8048/MCP8049 Output Stage

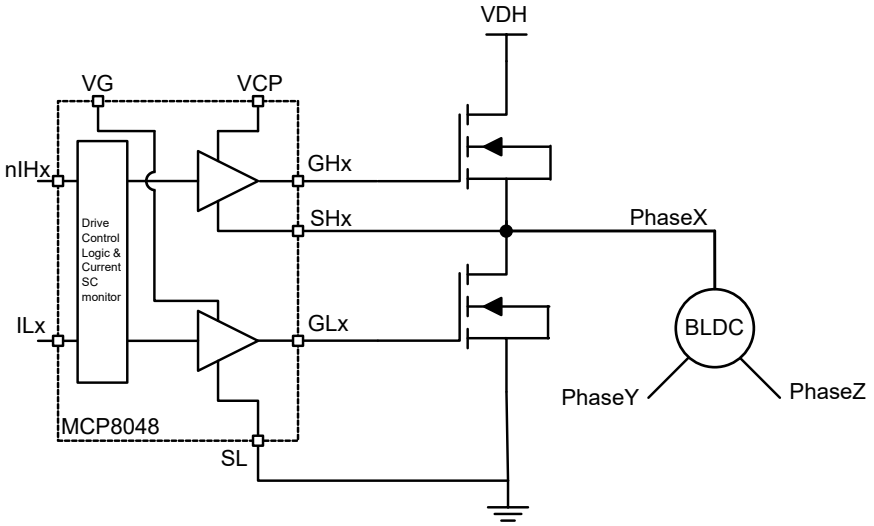
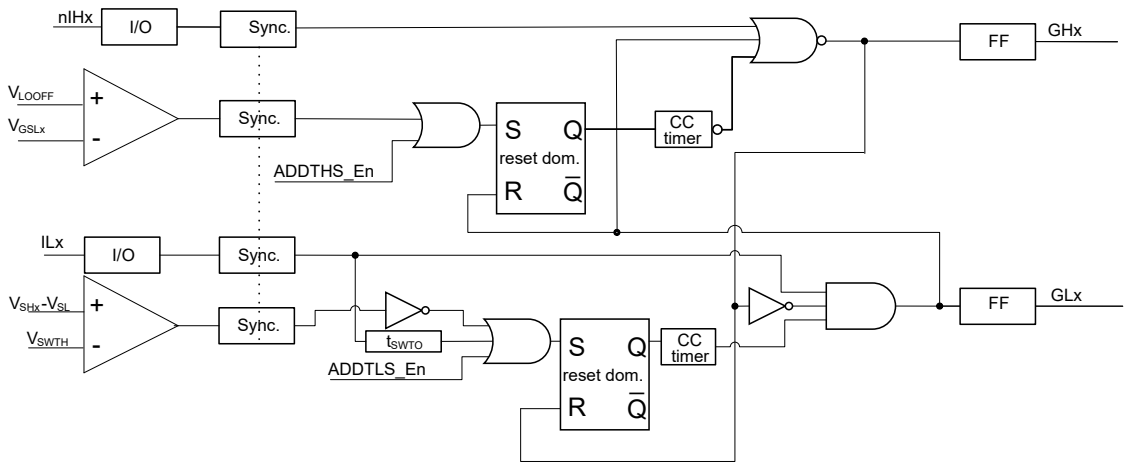


Figure 5-20. Adaptive Dead Time Logic Diagram



5.16.13. LIN transceiver TXD pin dominant timeout function

An internal timer prevents the LIN bus line from being driven permanently in the dominant state. If TXD is forced low longer than $t_{to(dom)\_LIN}$, the LIN transceiver will be disabled. The transceiver state can be checked in the DSR1 register, LTXDOUTS bit. Furthermore, to ensure that the transceiver is not disabled, the LTXS bit from the DSR1 Register needs to be checked before any operation. To reactivate the LIN transceiver, TXD must be switched to high for longer than 10 µs.

If the TXD pin stays at low level while switching into LIN Normal mode, it must be pulled to high level longer than 10 µs before the LIN driver can be activated. This feature prevents the bus line from being accidentally driven to the dominant state after normal mode has been activated (also in case of a short circuit at TXD to GND).

TXD Dominant Timeout function is activated in LIN Normal mode.

5.17. Limp Home

The Limp Home function is a high-voltage output pin used for signaling unexpected system errors. The LH pin is driven by an open-drain NMOS switch and is activated by the following events:

- A watchdog failure or Reset event. A watchdog timeout event in Sleep mode will not activate LH.
- If the device is in Standby or Normal mode:
- $V_{VDD1} < V_{VDD1\_UV\_Set}$ and RSTLVL bit = '1' (MCP8048/49-5050) **or**
  $V_{VDD1} < V_{VDD1\_UV\_IO\_Set}$ (MCP8048/49-5050 / MCP8048/49-3333) **or**
  $V_{VDD2} < V_{VDD2\_UV\_IO\_Set}$ (MCP8048/49-5033) has been detected for longer than t_{Reset} after entering MCU Reset mode, triggered by a wake-up or interrupt event (see cases **e** AND **i** in Device Operating Modes).
- VDDIO overvoltage event has been detected .

Releasing the LH pin to high ohmic, after the MCP8048/MCP8049 transitions from MCU Reset mode into Standby mode, requires receiving three valid watchdog trigger values (0x55) via SPI.

6. Electrical Characteristics

6.1. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
Junction Temperature	T_J	-40	170	°C
Storage Temperature	T_S	-55	150	°C
DC Voltage on the VS, VDH, INH, LH pins	V_{VS}, V_{VDH}, V_{INH}, V_{LH}	-0.3	42	V
LIN • DC Voltage • Pulse time < 500 ms	V_{LIN}	-27	+42 +43.5	V
DC Voltage on the WAKE pin	V_{WAKE}	-1.5	42	V
DC Voltage on the TXD, RXD, NIRQ, SDO, SDI, NCS, SCK, NIHx, ILx pins	V_X	-0.3	V_{VIO} + 0.3	V
DC Voltage on the NRES pin	V_{NRES}	-0.3	10	V
DC Voltage on the VDD1 pin	V_{VDD1}	-0.3	5.85	V
DC Voltage on the VDD2 pin	V_{VDD2}	-0.3	5.5	V
DC Common Mode Voltage on the OPPx, OPNx pins	V_{OPPX}, V_{OPNX}	-5.5	5.5	V
DC Voltage on the BEMFx, OPOx pins	V_{BEMFX}, V_{OPOX}	-0.3	V_{VIO} + 0.3	V
DC Voltage on the VG, CPN2 pins	V_{VG}, V_{CPN2}	-0.3	15	V
DC Voltage on the GHx to SHx pins	V_{GHX}-V_{SHX}	-0.3	15	V
DC Voltage on the GHx pin	V_{GHX}	V_{SHX} – 0.3	V_{VCP} + 0.3	V
DC Voltage on the SHx pin	V_{SHX}	-5.5	V_{VDH}+2	V
Pulse Voltage on the SHx pin, Transient <500ns	V_{SHX}	V_{SL} - 5.5 (MCP8048)	V_{VDH}+5.5	V
DC Voltage on the GLx pin	V_{GLx}	V_{GND} or V_{SL}– 0.3	V_{VG} + 0.3	V
DC Voltage on the GLx to GND pins (MCP8049)	V_{GLx}-V_{GND} (MCP8049)	-0.3	15	V
DC Voltage on the GLx to SL pins (MCP8048)	V_{GLx}-V_{SL}(MCP8048)	-0.3	15	V
DC Voltage on the SL pin (MCP8048)	V_{SL} (MCP8048)	-5.5	5.5	V
Differential DC Voltage between GND , GNDLIN and GNDEP (exposed die pad)	—	-0.3	0.3	V
DC Voltage on CPN1, CPP1	V_{CPN1}, V_{CPP1}	-0.3	42	V
DC Voltage on CPP2, VCP	V_{CPP2}, V_{VCP}	-0.3	55	V
DC Voltage on the VCP to VDH	V_{VCP}-V_{VDH}	-0.3	15	V
ESD following IEC 62228-2: (330Ω/150 pF) • Pins VS, VDH, WAKE to GND • Pins LIN to GND	—	 -8 -8	 +8 +8	 kV kV
HBM JESD22-A114/AEC-Q100-002 (1.5 kΩ/100 pF) • All pins • Pins VS, VDH, WAKE to GND • LIN to GND	—	 -2 -4 -8	 +2 +4 +8	 kV kV kV

Absolute Maximum Ratings (continued)				
Parameters	**Symbol**	**Min.**	**Max.**	**Unit**
Charge Device Model ESD AEC-Q100-011 - All pins	—	-750	750	V

Attention: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device within these or any other conditions beyond those indicated in the DC/AC Characteristics of this datasheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2. DC/AC Characteristics

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; H Variant: –40°C ≤ T_J ≤ 150°C; Typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	**Symbol**	**Pin/s**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**	**Type**
VS, VDH								
Supply Voltage Threshold for Power-On Detection	V_{VS_PWRON}	VS	4.2	—	4.55	V	VS rising	A
Supply Voltage Threshold for Power OFF Detection	V_{VS_PWROFF}	VS	2.8	—	3	V	V_{VS} falling	A
VS Undervoltage Detection Clear	$V_{VS\_UV\_Clear}$	VS	4.6	—	4.9	V	V_{VS} rising	A
VS Undervoltage Detection Set	$V_{VS\_UV\_Set}$	VS	4.2	—	4.55	V	V_{VS} falling	A
VS + VDH Quiescent Current in Deep Sleep Mode	I_{VS_DSLP}	VS	—	8	12	µA	Deep Sleep mode (WAKE wake up only), overvoltage detection OFF, T_J < 25°C	A
			—	—	20	µA	Deep Sleep mode (WAKE wake up only), overvoltage detection OFF, No temperature limitation	A
VS + VDH Current in Sleep Mode	I_{VS_SLP}	VS & VDH	—	15	35	µA	Sleep mode, (LIN wake up and WAKE wake up), overvoltage detection OFF See Figure 7-8	A
VS + VDH Current in Sleep Mode with Watchdog activated	$I_{VS\_SLP\_WD}$	VS	—	35	—	µA	Sleep mode (Watchdog enabled in Sleep mode (WDSLP=1)), overvoltage detection OFF	C
VS Current in Standby Mode	I_{VS_STB}	VS	—	—	95	µA	Standby mode LDO active	A
VS Current in Normal Mode with LIN Recessive	$I_{VS\_NORM\_REC}$	VS	—	4.9	5.1	mA	Normal mode, LIN recessive, GDU Standby, 7V < V_{VS} < 18V	A
VS Current in Normal Mode with LIN Dominant	$I_{VS\_NORM\_DOM}$	VS	—	5.3	6.0	mA	Normal mode, LIN dominant, GDU Standby, 7V < V_{VS} < 18V	A
VDH Current in Normal Mode Without Gate Driving	$I_{VDH\_GDU\_STB}$	VDH	—	—	8.2	mA	Normal mode, GDU Standby mode, 4.2V < V_{VDH} < 12V	A
VDH Overvoltage Detection Set	$V_{VDH\_OV\_Set}$	VDH	32.5	—	34.7	V	V_{VDH} Rising	A
VDH Overvoltage Detection Clear	$V_{VDH\_OV\_Clear}$	VDH	32	—	34	V	V_{VDH} Falling	A

DC/AC Characteristics (continued)

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; H Variant: –40°C ≤ T_J ≤ 150°C; Typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
VDH Current in Standby Mode	I_{VDH_STB}	VDH	—	1	—	µA	LIN wake-up and WAKE wake up, overvoltage detection OFF	A
VDD1 5V: MCP8048/49-5050, MCP8048/49-5033								
Output Voltage	$V_{VDD1nom}$	VDD1	4.9	5	5.1	V	V_{VS} > 5.5V (I_{VDD1} = 0 to -100 mA DC)	A
Output Voltage at Low VS	$V_{VDD1low}$	VDD1	V_{VS}-V_{Dx}	—	5.1	V	3V < V_{VS} < 5.35V, (I_{VDD1} = 0 to 100 mA)	A
Regulator Drop Voltage at Low VS	V_{D1}	VDD1	—	—	100	mV	3V < V_{VS} < 5.35V, I_{VDD1} = 20 mA	A
	V_{D2}	VDD1	—	—	250	mV	3V < V_{VS} < 5.35V, I_{VDD1} = 50 mA	A
	V_{D3}	VDD1	—	—	500	mV	3V < V_{VS} < 5.35V, I_{VDD1} = 100 mA	A
Line Regulation Maximum	$V_{VDD1line}$	VDD1	—	—	0.2	%	5.5V < V_{VS} < 40V, 1mA < I_{VDD1} < 100 mA	A
Load Regulation Maximum	$V_{VDD1load}$	VDD1	—	—	1	%	5.5V < V_{VS} < 40V, 5 mA < I_{VDD1} < 100 mA	A
Power Supply Ripple Reject	PSRR	VDD1	40	60	—	dB	1 V_{PP} @100 Hz, 10 kHz, 100 kHz; I_{VDD1} = 10 mA, 50 mA, 100 mA; V_{VS} = 13.8V	D
Output Current Limitation	$I_{VDD1lim}$	VDD1	100	—	145	mA	V_{VS} = 4.9V	A
Phase Margin	PM	VDD1	35	—	—	Deg.	V_{VS} > 5.5V, I_{VDD1} < 100 mA	D
Load Capacity	C_{VDD1}	VDD1	1.87	2.2	—	µF	MLC capacitor	D
Ramp-up Time	$t_{VDD1\_startup}$	VDD1	—	—	0.5	ms	V_{VS} > 5.5V, from enable regulator to V_{VDD1} = 99.5% stable value, C_{VDD1} = 2.7-3.9 µF, I_{VDD1} = 25 mA	C
VDD1 Undervoltage Set Threshold	$V_{VDD1\_UV\_Set}$	VDD1	4.5	—	4.7	V	V_{VDD1} falling	A
VDD1 Undervoltage Clear Threshold	$V_{VDD1\_UV\_Clear}$	VDD1	4.6	—	4.8	V	V_{VDD1} rising	A
VDD1 Undervoltage Hysteresis	$V_{VDD1\_UV\_HYS}$	VDD1	0.08	0.1	0.12	V		C
VDD1 IO Undervoltage Set	$V_{VDD1\_UV\_IO\_Set}$	VDD1	2.4	—	2.7	V	V_{VDD1} falling	A
VDD1 IO Undervoltage Clear	$V_{VDD1\_UV\_IO\_Clear}$	VDD1	2.5	—	2.8	V	V_{VDD1} rising	A
VDD1 IO Undervoltage Hysteresis	$V_{VDD1\_UV\_IO\_HYS}$	VDD1	0.08	0.1	0.12	V		C
Debouncing Time for Detecting VDD1 IO Undervoltage	$t_{VDD1\_UV\_IO\_deb}$	VDD1	6	—	54	µs		A
Output Current Foldback Corner	$I_{VDD1\_fbcorner}$	VDD1	105	—	135	mA	IC in Standby mode	A
Output Current Foldback Short Circuit Current	$I_{VDD1\_fb\_sc}$	VDD1	—	—	30	mA		A
VDD1 Overvoltage Set	$V_{VDD1\_OV\_Set}$	VDD1	5.5	5.68	5.85	V		A
VDD1 Overvoltage Clear	$V_{VDD1\_OV\_Clear}$	VDD1	5.45	5.58	5.75	V		A
Debouncing Time for Detecting VDD1 Overvoltage	$t_{VDD1\_OV\_deb}$	VDD1	6	—	54	µs		A

DC/AC Characteristics (continued)

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; H Variant: –40°C ≤ T_J ≤ 150°C; Typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
Debouncing Time for Detecting VDD1 Undervoltage	$t_{VDD1\_uv\_deb}$	VDD1	6	—	54	µs		A
VDD1 5V Output Voltage Load Step	$V_{VDD1loadStep}$	VDD1	-2	—	2	%	I_{VDD1} = 0 to 100 mA, I_{VDD1}= 100 to 0 mA Loadstep transient	C
VDD1 3.3V: MCP8048/49-3333								
Output Voltage	$V_{VDD1nom}$	VDD1	3.234	3.3	3.366	V	V_{VS} > 3.8V, (I_{VDD1} = 0 to 100 mA)	A A
Output Voltage at Low VS	$V_{VDD1low}$	VDD1	V_{VS}-V_{Dx}	—	3.37	V	3V < V_{VS} < 3.7V, (I_{VDD1} = 0 to 100 mA)	A
Regulator Drop Voltage at Low VS	V_{D1}	VDD1	—	—	100	mV	3V < V_{VS} < 3.7V, I_{VDD1} = 20 mA	A
	V_{D2}	VDD1	—	—	250	mV	3V < V_{VS} <3.7V, I_{VDD1} = 50 mA	A
	V_{D3}	VDD1	—	—	500	mV	3V <V_{VS} < 3.7V, I_{VDD1} = 100 mA	A
Line Regulation Maximum	$V_{VDD1line}$	VDD1	—	—	0.2	%	3.8V < V_{VS} < 40V, 1 mA < I_{VDD1} < 100 mA	A
Load Regulation Maximum	$V_{VDD1load}$	VDD1	—	—	1	%	3.8V < V_{VS} < 40V, 5 mA < I_{VDD1} < 100 mA	A
Power Supply Ripple Reject	PSRR	VDD1	40	60	—	dB	1 V_{PP} @100 Hz, 10 kHz, 100 kHz; V_{VS} = 13.8V I_{VDD1} = 10 mA, 50 mA, 100 mA	D
Output Current Limitation	IVDD1lim	VDD1	100	—	145	mA	V_{VS} = 3.2V	A
Phase Margin	PM	VDD1	25	—	—	Deg.	V_{VS} > 3.8V, I_{VDD1} < 100 mA	D
Load Capacity	C_{VDD1}	VDD1	1.87	2.2	—	µF	MLC capacitor	D
Ramp-up Time	$t_{VDD1\_startup}$	VDD1	—	—	0.5	ms	V_{IN} > 3.8V, from enable regulator to V_{VDD} = 99.5% stable value, C_{VDD1} = 2.2 µF, I_{VDD1} = 25 mA	D
VDD1 IO Undervoltage Set	$V_{VDD1\_UV\_IO\_Set}$	VDD1	2.4	—	2.7	V	V_{VDD1} falling	A
VDD1 IO Undervoltage Clear	$V_{VDD1\_UV\_IO\_Clear}$	VDD1	2.5	—	2.8	V	V_{VDD1} rising	A
VDD1 IO Undervoltage Hysteresis	$V_{VDD1\_UV\_IO\_HYS}$	VDD1	0.08	0.1	0.12	V		C
Debouncing Time for Detecting VDD1 Interface Undervoltage	$t_{VDD1\_UV\_IO\_deb}$	VDD1	6	—	54	µs		A
Output Current Foldback Corner	$I_{VDD1\_fbcorner}$	VDD1	105	—	135	mA	IC in Standby mode	A
Output Current Foldback Short Circuit Current	$I_{VDD1\_fb\_sc}$	VDD1	—	—	30	mA		A
VDD1 Overvoltage Set	$V_{VDD1\_OV\_Set}$	VDD1	3.64	3.75	3.86	V		A
VDD1 Overvoltage Clear	$V_{VDD1\_OV\_Clear}$	VDD1	3.54	3.65	3.76	V		A
Debouncing Time for Detecting VDD1 Overvoltage	$t_{VDD1\_OV\_deb}$	VDD1	6	—	54	µs		A
VDD1 3.3V Output Voltage Load Step	$V_{VDD1loadStep}$	VDD1	-2	—	2	%	I_{VDD1} = 0 to 100 mA, I_{VDD1}= 0 to 100 mA. Load step transient included.	C

DC/AC Characteristics (continued)

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; H Variant: –40°C ≤ T_J ≤ 150°C; Typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
VDD2 3.3V: MCP8048/49-5050, MCP8048/49-5033								
Output Voltage	$V_{VDD2nom}$	VDD2	3.234	3.3	3.366	V	V_{VDD1} > 4.5V, (I_{VDD2} = 0 to 70 mA)	A
Output Voltage at Low VDD2	$V_{VDD2low}$	VDD2	V_{VDD1}-V_{Dx}	—	3.37	V	V_{VDD1} < 4.5V, (I_{VDD2} = 0 to 70 mA)	A
Regulator Drop Voltage at Low VDD1	V_{D1}	VDD2	—	—	0.3	V	I_{VDD2} = 20 mA	A
	V_{D2}	VDD2	—	—	0.6	V	I_{VDD2} = 40 mA	A
	V_{D3}	VDD2	—	—	1.05	V	I_{VDD2} = 70mA	A
Line Regulation Maximum	$V_{VDD2line}$	VDD2	—	—	0.2	%	4.5 V < V_{VDD1} < 5.5V, 1 mA < I_{VDD2} < 70 mA	C
Load Regulation Maximum	$V_{VDD2load}$	VDD2	—	—	1.0	%	4.5 V < V_{VDD1} < 5.5V, 5 mA < I_{VDD2} < 70 mA	A
Power Supply Ripple Reject	PSRR	VDD2	40	60	—	dB	1 V_{PP} @100 Hz, 10 kHz, 100 kHz; I_{VDD2} = 10 mA, 50 mA, 70 mA; V_{VDD1} = 5V	D
Phase Margin	PM	VDD1	40	—	—	Deg.	V_{VS} > 4.5V, I_{VDD2} = 70 mA	D
Output Current Limitation	$I_{VDD2lim}$	VDD2	75	—	100	mA		A
Load Capacity	C_{VDD2}	VDD2	1.87	2.2	—	µF	MLC capacitor	D
Ramp-up Time	$t_{VDD2\_startup}$	VDD2	—	—	0.5	ms	V_{IN} > 4.5V, from enable regulator to V_{VDD} = 99.5% stable value, C_{VDD2} = 2.7-3.9 µF, I_{VDD2} = 25 mA	C
VDD2 IO Undervoltage Set	$V_{VDD2\_UV\_IO\_Set}$	VDD2	2.4	—	2.7	V	V_{VDD2} falling	A
VDD2 IO Undervoltage Clear	$V_{VDD2\_UV\_IO\_Clear}$	VDD2	2.5	—	2.8	V	V_{VDD2} rising	A
VDD2 IO Undervoltage Hysteresis	$V_{VDD2\_UV\_IO\_HYS}$	VDD2	0.08	0.1	0.12	V		C
Debouncing Time for Detecting VDD2 Interface Undervoltage	$t_{VDD2\_UV\_IO\_deb}$	VDD2	6	—	54	µs		A
VDD2 Overvoltage Set	$V_{VDD2\_OV\_Set}$	VDD2	3.64	3.75	3.86	V		A
VDD2 Overvoltage Clear	$V_{VDD2\_OV\_Clear}$	VDD2	3.54	3.65	3.76	V		A
Debouncing Time for Detecting VDD2 Overvoltage	$t_{VDD2\_OV\_deb}$	VDD2	6	—	54	µs		A
VDD2 3.3V Output Voltage Load Step	$V_{VDD2loadStep}$	VDD2	-2	—	2	%	I_{VDD2} = 0 to 70 mA, I_{VDD2} = 70 to 0 mA. Load step.	C
VG Regulator (Regulated Charge Pump)								
VG Output Voltage	V_{VG}	VG	11.5	12	12.5	V	V_{VDH} > V_{CP_STOP}, I_{VG} < 30 mA	B
VG Output Voltage	V_{VG}	VG	7.8	—	—	V	V_{VDH} > 5.1V, I_{VG} < 21 mA	A
Charge Pump Start	V_{CP_START}	VDH	12.5	—	13	V	V_{VDH} falling	A
Charge Pump Stop	V_{CP_STOP}	VDH	13	—	13.5	V	V_{VDH} rising	A

DC/AC Characteristics (continued)

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; H Variant: –40°C ≤ T_J ≤ 150°C; Typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
Charge Pump Frequency	f_{CP_VG}	CPN1, CPN2	360	380	400	kHz	V_{VDH} < 13V	A
Output Current Limit	I_{LIM_VG}		35	60	85	mA		A
Line Regulation Maximum	V_{VGline}	VG	—	—	0.2	%	13.8V ≤ V_{VDH} < 36V, 1 mA < I_{VG} < 30 mA	B
Load Regulation Maximum	V_{VGload}	VG	—	—	0.5	%	13.8V ≤ V_{VDH} < 36V, 5 mA < I_{VG} < 30 mA	B
Power Supply Ripple Reject	PSRR	VG	30	60	—	dB	1 V_{PP} @100 Hz, 10 kHz, 100 kHz; I_{VG} = 1 mA, 10 mA, 30 mA; V_{VS} > 13.8V	D
Phase Margin	PM	VG	35	—	—	Deg.	V_{VDH} ≥ 13.8V, I_{VDD1} < 30 mA	D
VCP Charge Pump								A
Charge Pump Output Voltage	V_{VCP}	VCP	12.2	—	—	V	V_{VDH} > 5.1V, V_{VG} > 7.8V, I_{VCP} = 10.6 mA	A
Charge Pump Output Voltage	V_{VCP}	VCP	24	—	—	V	V_{VDH} > 13.8V, V_{VG} > 11.5V, I_{VCP} = 15 mA	B
Gate Drive Unit								
Output Driver Source Resistance	R_{source}	GH/Lx	—	—	27	Ω	I_{GHx}/I_{GLx} = 100 mA	A
Output Driver Sink Resistance	R_{sink}	GH/Lx	—	—	10	Ω	I_{GHx}/I_{GLx} = -100 mA	A
Rising Edge Propagation Delay	t_{del_r}	GH/Lx	—	—	240	ns	C_{load} = 0, NIHx 30% to VGHx-VSHx or ILx 70% to V_{GLx} - V_{GND}(MCP8049) or V_{GLx} - V_{SL}(MCP8048) , reaches 10% of final V_{GS} level (slew rate control disabled)	C
Falling Edge Propagation Delay	t_{del_f}	GH/Lx	—	—	240	ns	C_{load} = 0, NIHx 70% to VGHx - VSHx or ILx 30% to V_{GLx} - V_{GND}(MCP8049) or V_{GLx} - V_{SL}(MCP8048) , reaches 90% of final V_{GS} level (slew rate control disabled)	C
Propagation Delay Mismatch	t_{del_mis}	GHx, GLx	0	—	100	ns	Absolute high-side edge and low-side edge propagation delay mismatch	C
			0	—	50	ns	Absolute high-side edge and low-side edge propagation delay mismatch in complementary mode	C

DC/AC Characteristics (continued)

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; H Variant: –40°C ≤ T_J ≤ 150°C; Typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
Slew Rate Control	SR100	GH/Lx	—	100%	—	full speed	HSSRC/LSSRC = `2'b00`	A
	SR50	GH/Lx	—	50%	—	full speed	HSSRC/LSSRC = `2'b01`	A
	SR25	GH/Lx	—	25%	—	full speed	HSSRC/LSSRC = `2'b10`	A
	SR125	GH/Lx	—	12.50 %	—	full speed	HSSRC/LSSRC = `2'b11`	A
VGS Undervoltage Detection Clear	$V_{VGS\_UV\_Clear\_H}$	GH/Lx	6.1	—	6.55	V	Higher level selected, UVVGSLVL = `1'b1`	A
VGS Undervoltage Detection Clear	$V_{VGS\_UV\_Clear\_L}$	GH/Lx	4.6	—	4.9	V	Lower level selected, UVVGSLVL = `1'b0`	A
VGS Undervoltage Detection Set	$V_{VGS\_UV\_Set\_H}$	GH/Lx	5.6	—	6.0	V	Higher level selected, UVVGSLVL = `1'b1`	A
VGS Undervoltage Detection Set	$V_{VGS\_UV\_Set\_L}$	GH/Lx	4.2	—	4.55	V	Lower level selected, UVVGSLVL = `1'b0`	A
Short Circuit Detection Voltage Threshold Range (Drain-Source Monitoring)	V_{SC_TH}	VDH, SHx, GND (MCP8049) or SL (MCP8048)	See SCPCR Register			mV	Configurable via SPI	A
Short Circuit Detection Reference Voltage Accuracy (Drain-Source Monitoring)	dV_{SC_TH500}	VDH, SHx, GND (MCP8049) or SL (MCP8048)	-5%	—	5%	—	V_{SC_TH} ≥ 500 mV	B
	dV_{SC_TH250}		-8%	—	8%	—	V_{SC_TH} = 250 mV	B
	dV_{SC_TH125}		-15%	—	15%	—	V_{SC_TH} = 125 mV, T_J < 25°C	B
			-15%	—	25%	—	V_{SC_TH} = 125 mV	B
VDS Voltage Blanking Time	t_{VDS_Blank}	GH/Lx	See GDUCR2 Register			µs	Configurable via SPI	B
VGS Undervoltage Voltage Detection Blanking Time	$t_{VGS\_UV\_Blank}$	GH/Lx	See GDUCR2 Register			µs	Configurable via SPI	B
VGS Undervoltage Voltage Detection Blanking Time Accuracy	$dt_{VGS\_UV\_Blank}$	GH/Lx	-10%	—	10%	—		B
VGS Undervoltage Voltage Detection Add-on Blanking Time in GDU Standby Mode	$t_{VGS\_UV\_Blank\_ADO}$	GH/Lx	—	2000	—	µs		B
Current Limitation Detection Blanking Time	t_{OC_BT}	GH/Lx	See ILIMCR Register			µs	Configurable via SPI	B
Current Limitation Detection Blanking Time Accuracy	dt_{OC_BT}	GH/Lx	-5%	—	5%	—		B
Edge Blanking Time	t_{EG_Blank}	GH/Lx	See GDUCR2 Register			µs	Configurable via SPI	B
Edge Blanking Time Accuracy	dt_{EG_Blank}	GH/Lx	-5%	—	5%	—		B

DC/AC Characteristics (continued)

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; H Variant: –40°C ≤ T_J ≤ 150°C; Typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
Cross Conduction Protection Time	t_{CC}	GH/Lx	See GDUCR1 Register			µs	Configurable via SPI	B
Cross Conduction Protection Time Accuracy	dt_{CC}	GH/Lx	-5%	—	5%	—		B
Adaptive Deadtime High-side ON Delay Time Range	t_{HON_DEL}	—	See GDUCR3 Register			ns	Configurable via SPI	A
Adaptive Deadtime High-side ON Delay Time Range Accuracy	dt_{HON_DEL}	—	-5%	—	5%	—		A
Adaptive Deadtime Low-side ON Delay Time Range	t_{LON_DEL}	—	See GDUCR3 Register			ns	Configurable via SPI	A
Adaptive Deadtime Low-side ON Delay Time Range Accuracy	dt_{LON_DEL}	—	-5%	—	5%	—		A
Adaptive Deadtime Force to Switch Delay Time	t_{SWTO}	—	See GDUCR2 Register			ns	Configurable via SPI	A
Adaptive Deadtime Force to Switch Delay Time Accuracy	dt_{SWTO}	—	-5%	—	5%	—		A
Low-side Gate-Source Threshold Voltage for Low-side Gate OFF Detection	V_{LOOFF}	GLx / GND (MCP8049) or SL (MCP8048)	1.6	1.8	2	V		C
Low-side Drain-Source Threshold Voltage for High-side Gate OFF Detection	V_{SWTH}	SHx	1.6	1.8	2	V		C
VDS Short Circuit Detection Delay	t_{VDS_DEL}	—	—	—	130	ns	Analog delay for detection VDS short circuit	D
Low-side Gate Drive Voltage	$V_{LOOUTLO}$	—	7.8	—	—	—	V_{VDH} > 5.1V	B
	$V_{LOOUTTYP}$	—	11.5	—	12.5	V	V_{VDH} > 13.8V	B
High-side Gate Drive Voltage	$V_{HIOUTLO}$	—	7.1	—	—	V	V_{VDH} > 5.1V, V_{VG} > 7.8V	B
	$V_{HIOUTTYP}$	—	10.5	—	—	V	V_{VDH} > 13.8V, V_{VG} > 11.5V	B
DAC								
V_{VIO} = 3.3V: MCP8048/49-3333, MCP8048/49-5033								
Resolution	—	—	—	7	—	bits		D
Current Limitation Comparator Reference DAC Output Voltage Range	$V_{DACRANGE}$	—	0.35	—	2.97	V		C
Current Limitation Comparator Reference DAC Output Voltage	V_{DACd0}	—	—	0.35	—	V	DAC = `d0`	A
	V_{DACd31}	—	—	0.99	—	V	DAC = `d31`	B
	V_{DACd63}	—	—	1.65	—	V	DAC = `d63`	B
	$V_{DACd127}$	—	—	2.97	—	V	DAC = `d127`	A
Differential Nonlinearity	DNL	—	-50%	—	+50%	LSB		C
Integral Nonlinearilty	INL	—	-0.5%	—	0.5%	FSR	FSR = Full Scale Range	C

DC/AC Characteristics (continued)

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; H Variant: –40°C ≤ T_J ≤ 150°C; Typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
Input to Output Delay	t_{delay}	—	—	—	50	µs		C
V_{VIO} = 5V: MCP8048/49-5050								
Resolution	—	—	—	7	—	bits		D
Current Limitation Comparator Reference DAC Output Voltage Range	$V_{DACRANGE}$	—	0.53	—	4.5	V		C
Current Limitation Comparator Reference DAC Output Voltage	V_{DACd0}	—	—	0.53	—	V	DAC = d0	A
	V_{DACd31}	—	—	1.5	—	V	DAC = d31	B
	V_{DACd63}	—	—	2.5	—	V	DAC = d63	B
	$V_{DACd127}$	—	—	4.5	—	V	DAC = d127	A
Differential Nonlinearity	DNL	—	-50%	—	+50%	LSB		C
Integral Nonlinearity	INL	—	-0.50 %	—	0.50%	FSR		C
Input to Output Delay	t_{delay}	—	—	—	50	µs		C
Current Sense Amplifier and Comparator								
Input Offset Voltage (Initial)	V_{OFS_INIT}	OPPx, OPNx	-3	0	+3	mV		A
Input Offset Temperature Drift	V_{OFS_DRIFT}	OPPx, OPNx	-1	—	+1	mV	0 < V_{CM} < 2V	C
Common Mode Input Range	V_{IN_CM}	OPPx, OPNx	-0.3	—	+2	V		C
Common Mode Rejection Ratio	CMRR	OPPx, OPNx	—	80	—	dB	20 * log((V_{OUT_diff}/V_{IN_diff}) * (V_{IN_CM} / V_{OUT_CM})), 10 kHz	C
Current Sense Amplifier Input Resistance	R_{IN}	OPPx, OPNx	8.2	—	18	kΩ		A
Output Voltage Range	V_{OPO_CMR}	OPOx	0.15	—	V_{VIO} – 0.15	V	I_{OUT} = ±200 µA	A
Output Voltage Offset	V_{OPO_OFS}	OPOx	—	VIO/16	—	V	OFFSET = 2'b00 (default)	A
		OPOx	—	VIO/8	—	V	OFFSET = 2'b01	A
		OPOx	—	VIO/4	—	V	OFFSET = 2'b10	A
		OPOx	—	VIO/2	—	V	OFFSET = 2'b11	A
Gain	Av	OPOx	—	8	—	V/V	GAIN = 2'b00, VDIFF = ±180 mV, V_{VIO} = 3.3V	B
		OPOx	—	16	—	V/V	GAIN = 2'b01, VDIFF = ±90 mV, V_{VIO} = 3.3V	B
		OPOx	—	32	—	V/V	GAIN = 2'b10, VDIFF =± 45 mV, V_{VIO} = 3.3V	B
		OPOx	—	64	—	V/V	GAIN = 2'b11, VDIFF = ±22.5 mV, V_{VIO} = 3.3V	B

DC/AC Characteristics (continued)

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; H Variant: –40°C ≤ T_J ≤ 150°C; Typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
Settling Time	t_{settle}	OPOx	—	—	300	ns	Rise/Fall times for VDIFF = ±1V condition, settling time measured from VDIFF applied from/to 20/80% of the final value be reached, gain = 8	A
Gain Accuracy	dAv	OPOx	-1.5	—	2	%	GAIN = 16, GAIN = 32, GAIN = 64,	C
			-1.5	—	4	%	GAIN = 8	C
Gain Bandwidth Product of CSA OpAmp	GBWP	—	—	40	—	MHz		D
Current Limitation Detection Comparator Hysteresis	$V_{OV\_COMP\_HYS}$	—	—	10	—	mV		C
Current Limitation Detection Comparator Common Mode Input Range	$V_{OV\_COMP\_CMR}$	—	0.15	—	V_{VIO} – 0.15	V		C
Current Limitation Detection Comparator Input Offset	$V_{OV\_COMP\_OFSET}$	—	-6	—	+6	mV		A
CSA OFF-state Leakage Current	I_{leak_CSAx}	OPOx	-0.5	—	+0.5	µA		A
CSA Start-up Time	t_{CSA_START}	—	—	—	20	µs		D
Back-EMF								
Input to Output Delay	—	—	—	—	500	ns	V_{SHx} with 500 mV steps	C
BEMFx High-level Output Voltage	V_{BEMFx_H}	BEMFx	V_{VIO} – 0.4	—	V_{VIO}	V	I = -1 mA	A
BEMFx Low-level Output Voltage	V_{BEMFx_L}	BEMFx	-	—	0.4	V	I = 1 mA	A
OFF-state Leakage Current	I_{leak_BEMFx}	BEMFx	-0.5	—	+0.5	µA		A
Total Back EMF Detection Input Offset Error		SHx	-200	—	+200	mV		C
LIN Bus Driver (MCP8048)								
Bus load conditions: 4.9V<VS<18V; Load 1 (Small): 1 nF, 1 kΩ; Load 2 (Large): 10 nF, 500Ω; CRXD = 20 pF, Load 3 (Medium): 6.8 nF, 660Ω characterized on samples								
Driver Recessive Output Voltage	V_{BUSrec}	LIN	0.9 × V_{VS}	—	V_{VS}	V	Load1/Load2	A
Driver-dominant Voltage	$V_{\_LoSUP}$	LIN	—	—	1.2	V	V_{VS} = 7V; R_{load} = 500Ω	A
Driver-dominant Voltage	$V_{\_HiSUP}$	LIN	—	—	2	V	V_{VS} = 18V; R_{load} = 500Ω	A
Driver-dominant Voltage	$V_{\_LoSUP\_1k}$	LIN	0.6	—	—	V	V_{VS} = 7V; R_{load} = 1000Ω	A
Driver-dominant Voltage	$V_{\_HiSUP\_1k}$	LIN	0.8	—	—	V	V_{VS} = 18V; R_{load} = 1000Ω	A
Pull-up Resistor to V_{VS}	R_{LIN}	LIN	27.66	37	47	KΩ	The serial diode is mandatory	A
Voltage Drop at the Serial Diodes	$V_{SerDiode}$	LIN	0.4	—	1	V	In pull-up path with Rclient. $I_{SerDiode}$ = 10 mA	D
LIN Current Limitation V_{LIN} = V_{VS_max}	I_{BUS_LIM}	LIN	40	120	200	mA		A
Input Leakage Current at the Receiver Including Pull-up Resistor as Specified	$I_{BUS\_PAS\_dom}$	LIN	-1	-0.35	—	mA	Input leakage current V_{LIN} = 0V; V_{VS} = 12V	A

DC/AC Characteristics (continued)

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; H Variant: –40°C ≤ T_J ≤ 150°C; Typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
Leakage Current LIN Recessive	$I_{BUS\_PAS\_rec}$	LIN	—	10	20	µA	Driver off; 8V < V_{VS} < 18V; 8V < V_{LIN} < 18V; V_{LIN} ≥ V_{VS}	A
Leakage Current When Control Unit Disconnected from Ground. Loss of Local Ground Must Not Affect Communication in the Residual Network.	$I_{BUS\_NO\_gnd}$	LIN	-10	0.5	10	µA	GND Device = V_{VS}; V_{VS} = 12V; 0V < V_{LIN} < 18V	A
Leakage Current at Disconnected Battery. Node Must Sustain the Current that Can Flow Under this Condition. Bus Must Remain Operational Under this Condition.	$I_{BUS\_NO\_bat}$	LIN	—	0.1	2	µA	VS connected to ground. 0V < V_{LIN} < 18V	A
Capacitance on the LIN Pin to GND	C_{LIN}	LIN	—	—	20	pF		D
Center of Receiver Threshold	V_{BUS_CNT}	LIN	0.475 ×V_{VS}	0.5 × V_{VS}	0.525 × V_{VS}	V	V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2	A
Receiver Dominant State	V_{BUSdom}	LIN	-27	—	0.4 × V_{VS}	V		A
Receiver Recessive State	V_{BUSrec}	LIN	0.6 x V_{VS}	—	V_{VS}	V		A
Receiver Input Hysteresis	V_{BUShys}	LIN	0.028 × V_{VS}	0.1×V_{VS}	0.175 × V_{VS}	V	V_{hys} = V_{th_rec} – V_{th_dom}	A
Pre-wake Detection LIN High-level Input Voltage	V_{LINH}	LIN	V_{VS} – 2	—	—	V		A
Pre-wake Detection LIN Low-level Input Voltage	V_{LINL}	LIN	—	—	V_{VS} – 3.3	V	Activates the LIN receiver	A
SDI, SCK, NCS, NIHx, ILx, TXD (V_{VIO} refers to the selected µC supply)								
High-level Input Voltage	V_{SDI_H}, V_{SCK_H}, V_{NCS_H}, V_{NIHx_H}, V_{ILx_H}, V_{TXD_H}	SDI, SCK, NCS, NIHx, ILx, TXD	0.7 × V_{VIO}	—	V_{VIO} + 0.3	V		A
Low-level Input Voltage	V_{SDI_L}, V_{SCK_L}, V_{NCS_L}, V_{NIHx_L}, V_{ILx_L}, V_{TXD_L}	SDI, SCK, NCS, NIHx, ILx, TXD	-0.3	—	0.3 × V_{VIO}	V		A
Input Current	I_{leak_SDI}, I_{leak_SCK}, I_{leak_NCS}, I_{leak_NIHx}, I_{leak_ILx}, I_{leak_TXD}	SDI, SCK, NCS, NIHx, ILx, TXD	-5	—	+5	µA		A
Pull-up Resistance on the Pins NCS, NIHx, TXD	R_{PU_NCS}, R_{PU_NIHx}, R_{PU_TXD}	NCS, NIHx, TXD	40	60	80	kΩ		A

DC/AC Characteristics (continued)

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; H Variant: –40°C ≤ T_J ≤ 150°C; Typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
Pull-down Resistance on the SCK Pin, ILx	R_{PD_SCK}, RP_{D_ILx}	SCK, ILx	40	60	80	kΩ		A
SDO, RXD (V_{VIO} refers to the selected µC supply)								
High-level Output Voltage	V_{SDO_H}, V_{RXD_H}	SDO, RXD	V_{VIO} - 0.4	—	—	V	I = -4 mA	A
Low-level Output Voltage	V_{SDO_L}, V_{RXD_L}	SDO, RXD	—	—	0.4	V	I = 4 mA	A
Off-state Leakage Current	I_{leak_SDO}, I_{leak_RXD}	SDO, RXD	-5	—	5	µA		A
WAKE								
Input Rising Threshold	$V_{WAKE\_H\_TH}$	WAKE	1	1.6	2.05	V		A
Input Falling Threshold	$V_{WAKE\_L\_TH}$	WAKE	0.75	1.05	1.5	V		A
Input Hysteresis	V_{WAKE_HYS}	WAKE	200	—	600	mV		A
WAKE Leakage Current	I_{leak_WAKE}	WAKE	-2	—	+2	µA	VLIN = VVS = 32V	A
Wake Pull-up Resistor	—	—	—	1000	—	kΩ		A
Filter Time Delay	t_{local_wu}	—	40	—	180	µs		A
NRES, NIRQ (internally pull-up to V_{VIO})								
Low-level Output Voltage	V_{NRESL}, V_{NIRQL}	NRES, NIRQ	—	0.2	0.4	V	I_{NRES} = 2 mA, I_{NIRQ} = 2 mA	A
Watchdog Reset Time	t_{Reset}	NRES	According to the setting in the WDCR2 Register			ms	C_{NRES} = 20 pF	B
Pull-up Resistance	R_{PU}	NRES, NIRQ	6.5	10	13.5	kΩ	Diode in series with pull-up resistance, V_{NRES} < 2V	A
High-level Input Voltage	V_{NRES_H}	NRES	0.7 × V_{VIO}	—	—	V		A
Low-level Input Voltage	V_{NRES_L}	NRES	—	—	0.3 × V_{VIO}	V		A
Input Pulse Length	t_{NRES_input}	NRES	75	—	—	µs		B
Watchdog Long Open Window	t_{LW}	NRES	560	—	700	ms		B
Event Capture Delay Time	$t_{d\_evt\_cap}$	NIRQ	0.9	—	1.1	ms		B
Limp Home								
Low-level Output Voltage	V_{LH}	LH	—	—	0.2	V	V_{VS} > 4.2V, I_{LH} = 4 mA	A
Leakage Current	I_{leak_LH}	LH	—	—	2	µA	V_{LH} < 40V	A
INH								
Output ON Voltage	V_{INH_ON}	INH	V_{VS} – 0.8	—	V_{VS}	V	I_{INH} = -180 µA	A
Leakage Current	I_{leak_INH}	INH	—	—	2	µA	Leakage of grounded INH pin in OFF Mode	A
SPI Timing (see SPI Timing Diagram)								
Clock Cycle Time	t_{clk}	SPI	250	—	—	ns	Normal/Standby	D
SPI Enable Lead Time	t_{ENLEAD}	SPI	50	—	—	ns	Normal/Standby	D

DC/AC Characteristics (continued)

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; H Variant: –40°C ≤ T_J ≤ 150°C; Typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
SPI Enable Lag Time	t_{ENLAG}	SPI	50	—	—	ns	Normal/Standby	D
Clock HIGH Time	t_{clk_H}	SPI	125	—	—	ns	Normal/Standby	D
Clock LOW Time	t_{clk_L}	SPI	125	—	—	ns	Normal/Standby	D
Data Input Set-up Time	t_{setup}	SPI	50	—	—	ns	Normal/Standby	D
Data Input Hold Time	t_{hold}	SPI	50	—	—	ns	Normal/Standby	D
Data Output Valid Time	t_{dout_v}	SPI	—	—	50	ns	Normal/Standby	D
Chip Select Pulse Width HIGH	t_{NCS_pw}	SPI	250	—	—	ns	Normal/Standby, SDO pin; CL = 20 pF	D
LIN-, VDD- Timings								
Startup Time After Power-on	$t_{startup}$	VS	—	2.8	4.7	ms	From V_{VS} rises above the power-on detection threshold V_{VS_PWRON} until $V_{VDD1} > V_{VDD1\_UV\_Clear}$ or $V_{VDD2} > V_{VDD2\_UV\_IO\_Clear}$	C
Dominant Time for Wake-up via LIN Bus	t_{bus}	LIN	50	100	150	µs	V_{LIN} = 0V	A
TXD Dominant Timeout Time	$t_{to(dom)\_LIN}$	TXD	20	40	60	ms	V_{TXD} = 0V	A
Duty Cycle 1 Timing parameter for proper operation at 20 kb/s	D1	LIN	0.396	—	—	s/s	$TH_{Rec(max)}$ = 0.744 × V_{VS}; $TH_{Dom(max)}$ = 0.581 × V_{VS}; V_{VS} = 7.0V to 18V; t_{Bit} = 50 µs; D1 = $t_{bus\_rec(min)}$/(2 × t_{Bit})	A
Duty Cycle 2 Timing parameter for proper operation at 20 kb/s	D2	LIN	—	—	0.581	s/s	$TH_{Rec(min)}$ = 0.422 × V_{VS}; $TH_{Dom(min)}$ = 0.284 × V_{VS}; V_{VS} = 7.6V to 18V; t_{Bit} = 50 µs; D2 = $t_{bus\_rec(max)}$/(2×t_{Bit})	A
Duty Cycle 3 Timing parameter for proper operation at 10.4 kb/s	D3	LIN	0.417	—	—	s/s	$TH_{Rec(max)}$ = 0.778×V_{VS}; $TH_{Dom(max)}$ =0.616×V_{VS}; V_{VS} = 7.0V to 18V; t_{Bit} = 96 µs; D3 = $t_{bus\_rec(min)}$/(2 × t_{Bit})	A
Duty Cycle 4 Timing parameter for proper operation at 10.4 kb/s	D4	LIN	—	—	0.59	s/s	$TH_{Rec(min)}$ = 0.389 × V_{VS}; $TH_{Dom(min)}$ = 0.251 × V_{VS}; V_{VS} = 7.6V to 18V; t_{Bit} = 96 µs; D4 = $t_{bus\_rec(max)}$/(2 × t_{Bit})	A
TXD Release Time after Dominant Timeout Detection	t_{DTOrel}	TXD	10	—	20	µs		B
Propagation Delay of Receiver	t_{rx_pd}	RXD	—	—	6	µs	Receiver Electrical AC Parameters of the LIN Physical Layer LIN Receiver, RXD Load Conditions: CRXD = 20 pF; VS = 7.0V to 18V; t_{rx_pd} = max(t_{rx_pdr}, t_{rx_pdf})	A
Symmetry of Receiver Propagation Delay Rising Edge Minus Falling Edge	t_{rx_sym}	RXD	-2	—	2	µs	Receiver Electrical AC Parameters of the LIN Physical Layer LIN Receiver, RXD Load Conditions: C_{RXD} = 20 pF; V_{VS} = 7.0V to 18V; t_{rx_sym} = t_{rx_pdr} – t_{rx_pdf}	A

DC/AC Characteristics (continued)

All parameters valid for 4.9V ≤ V_{VS} ≤ 32V; all voltages are defined with respect to ground; H Variant: –40°C ≤ T_J ≤ 150°C; Typical values are given at V_{VS} = 13V, T_J = 25°C; unless otherwise noted.

Parameters	Symbol	Pin/s	Min.	Typ.	Max.	Unit	Conditions	Type
Temperature Protection								
Overtemperature Protection Shutdown Threshold	T_{OT_sdwn}	—	170	180	190	°C	Junction Temperature	B
Overtemperature Protection Release Threshold	$T_{OT\_release}$	—	155	165	175	°C	Junction Temperature	B
Overtemperature Protection Prewarning Set Threshold	$T_{OT\_PREW\_Set}$	—	150	160	170	°C	Junction Temperature	B
Overtemperature Protection Prewarning Clear Threshold	$T_{OT\_PREW\_Clear}$	—	135	145	155	°C	Junction Temperature	B
Motor Line Diagnostic								
Logic High Detection Threshold	$V_{thSHxHI}$	SHx	—	V_{VDH} – 1.75	—	V	Set MLDCR MLDEN Check MLDRR DIAG_xx	A
Logic Low Detection Threshold	$V_{thSHxLO}$	SHx	—	1.75	—	V	Set MLDCR MLDEN Check MLDRR DIAG_xx	A
Sink Current	$I_{SHxSink}$	SHx	4.4	—	7.2	mA	Set MLDCR SINKx and MLDCR MLDEN V_{SHx} > 3V	A
Source Current	$I_{SHxSource}$	SHx	1	—	1.85	mA	Set MLDCR SOURCEx MLDCR MLDEN V_{SHx} < V_{VDH} – 3V	A

PARAMETER TYPE LEGEND: A = 100% Tested, B = 100% Tested through indirect testing or calculation, C = Characterized, not production tested, D = Simulated, not production tested

6.3. Thermal Characteristics

Parameters	Symbol	Min.	Typical	Max.	Unit
Package (no. of pins)					
6.0 mm x 6.0 mm VQFN (48L)	R_{thJA}		30		°C/W
	R_{thJC}		10		
5.0 mm x 5.0 mm VQFN (40L)	R_{thJA}	—	35	—	°C/W
	R_{thJC}	—	10	—	

Note 1: 4-Layer JC51-5 standard board, natural convection.

7. Typical Performance Curves

Figure 7-1. Current Sense Amplifiers Gain Accuracy

Gain (Av) vs. Temperature (GAIN = 8, 16, 32, 64, CSA = 1, 2, 3)

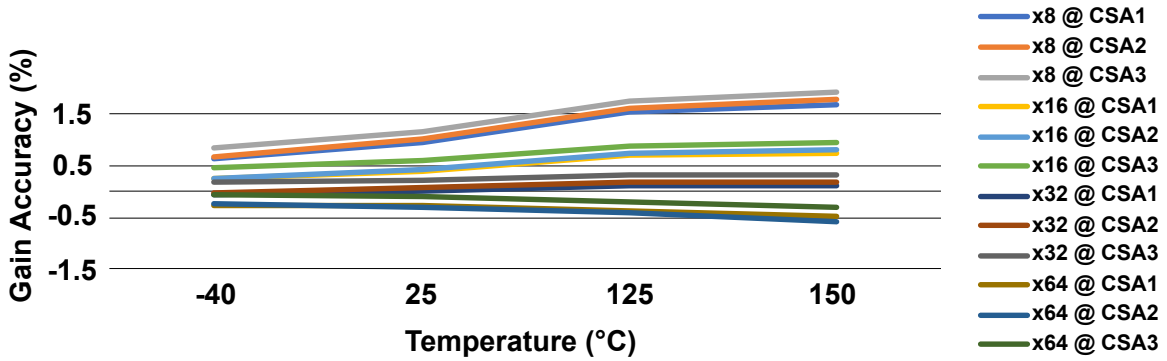


Figure 7-2. Current Sense Amplifiers Gain Mismatch

Gain Accuracy (dAv) vs. Temperature (OFFSET = 1.65V, GAIN = 8, 16, 32, 64)

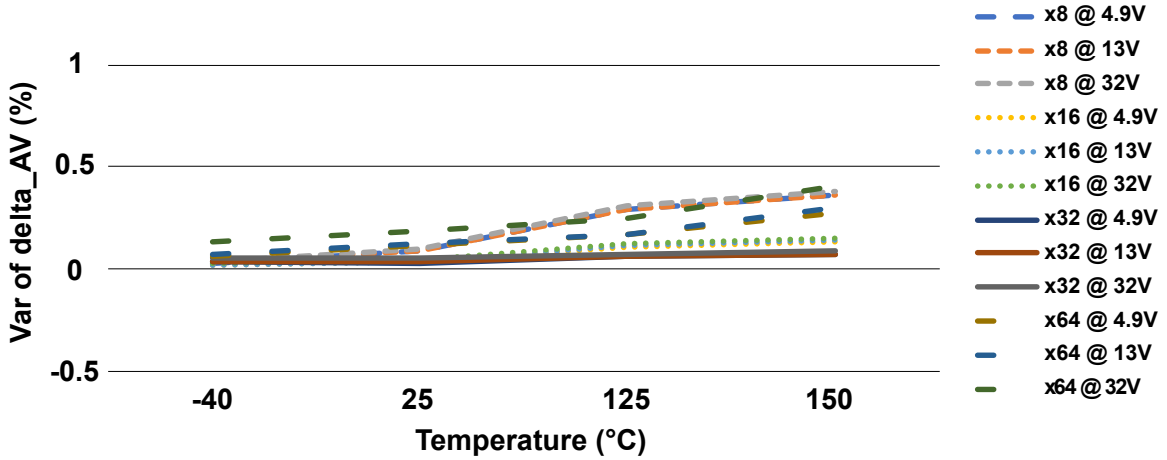


Figure 7-3. Current Sense Amplifiers Output Offset Mismatch

Average Output Offset Ratio (V_{VIO}/V_{OPO_OFS}) vs. Temperature

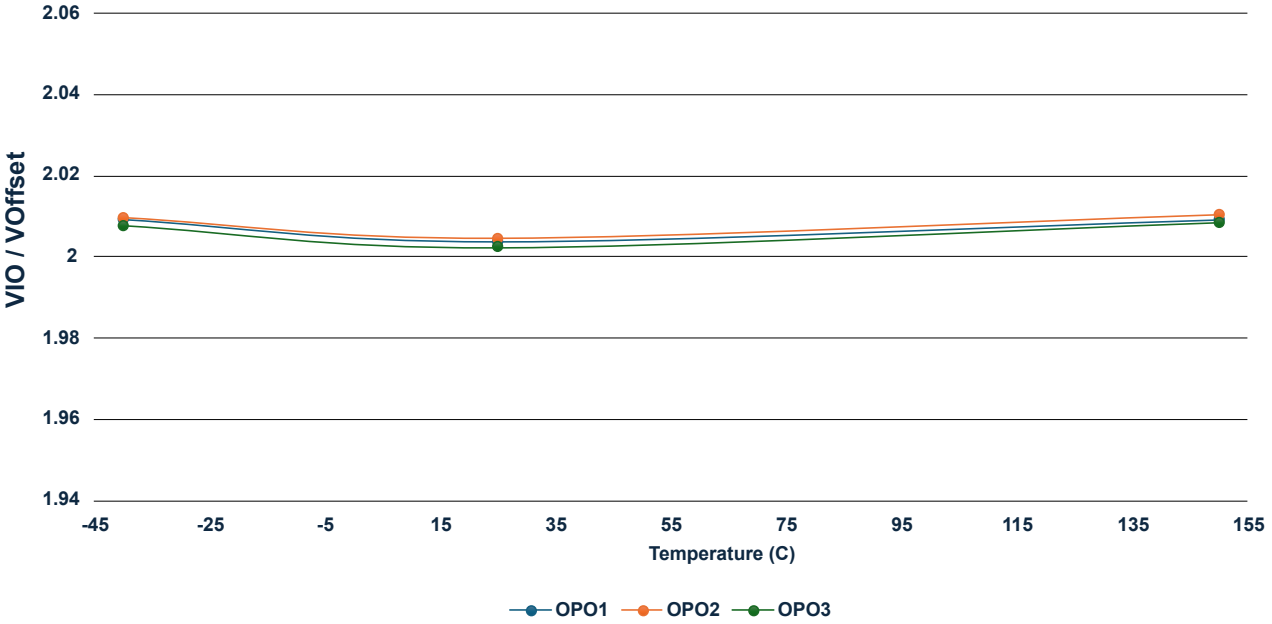
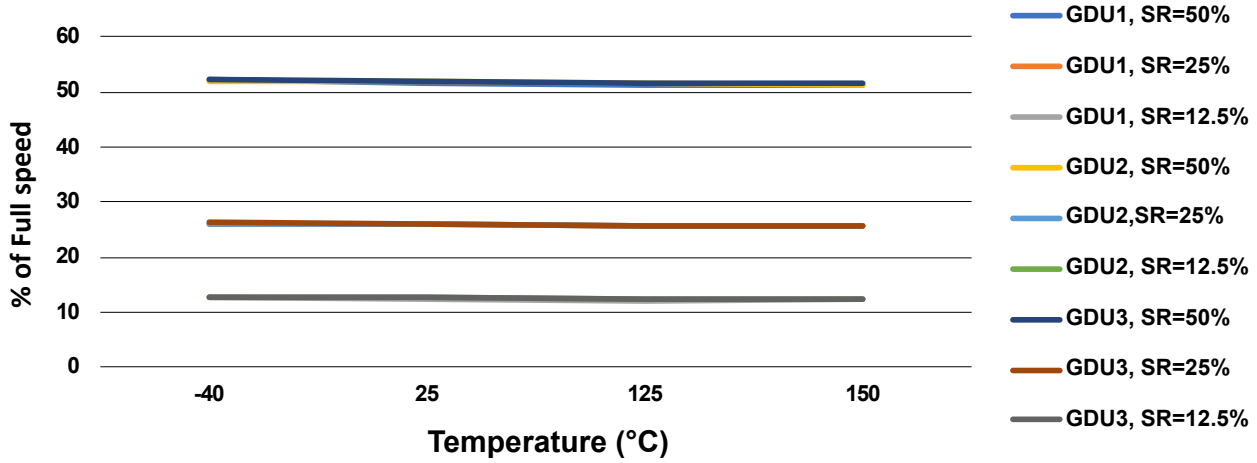


Figure 7-4. Gate Driver Unit Slew Rate Control

High-Side Slew Rate Control vs. Temperature (HSSRC = 0, 1, 2, 3, GDU = 1, 2, 3)



Low-Side Slew Rate Control vs. Temperature (LSSRC = 0, 1, 2, 3, GDU = 1, 2, 3)

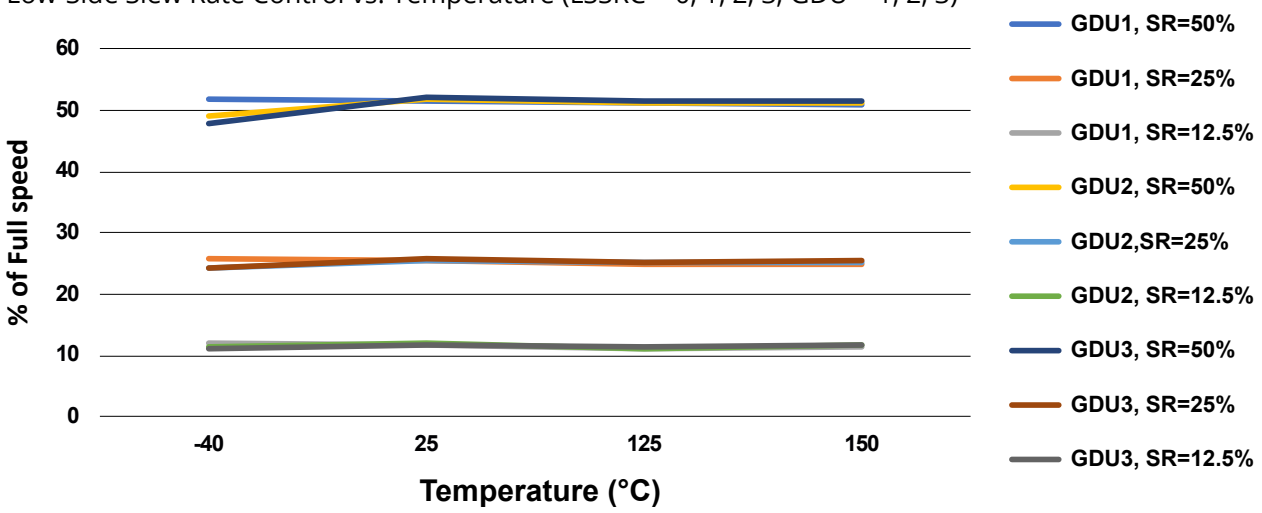
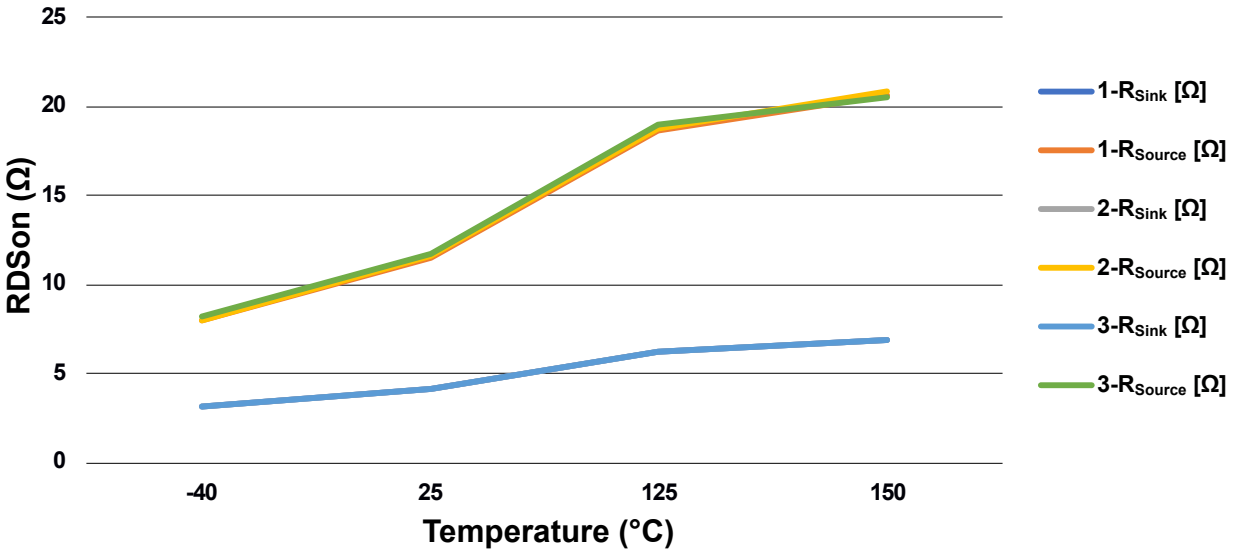


Figure 7-5. Gate Driver Unit Sink/Source ON Resistance vs Temperature

GDU HS Source/Sink Resistance (R_{Source}/R_{Sink}) vs. Temperature (I_{GHx} = 100 mA, GDU = 1, 2, 3)



GDU LS Source/Sink Resistance (R_{Source}/R_{Sink}) vs. Temperature (I_{GLx} = -100 mA, GDU = 1, 2, 3)

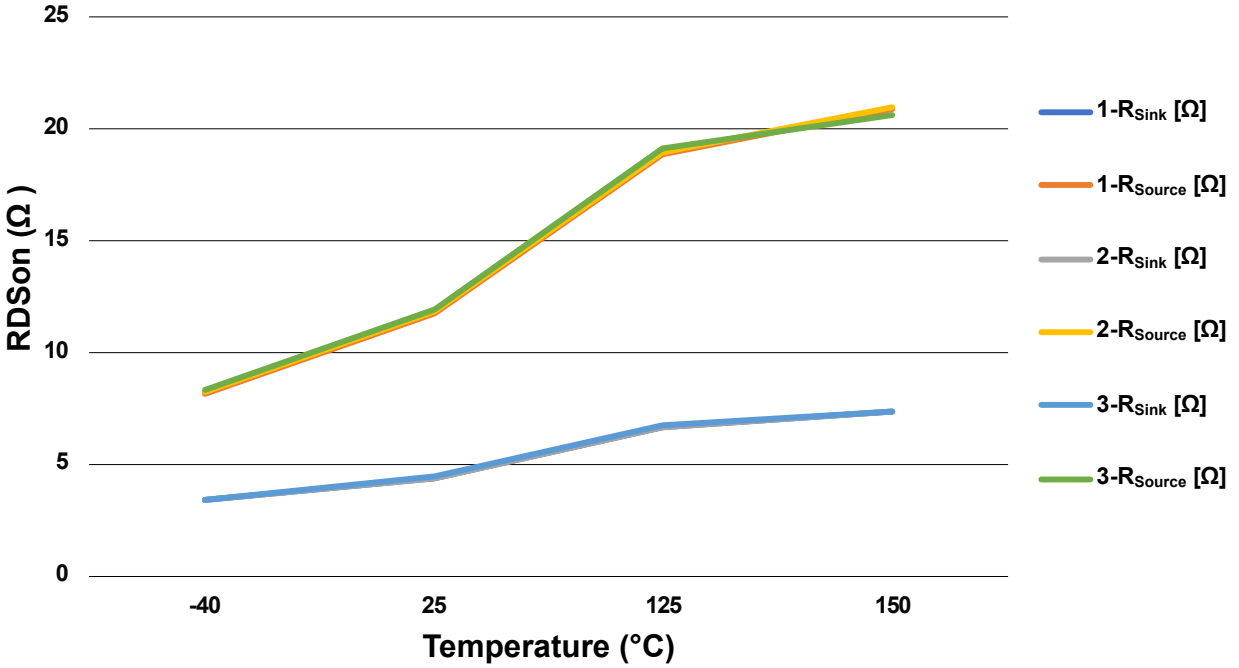
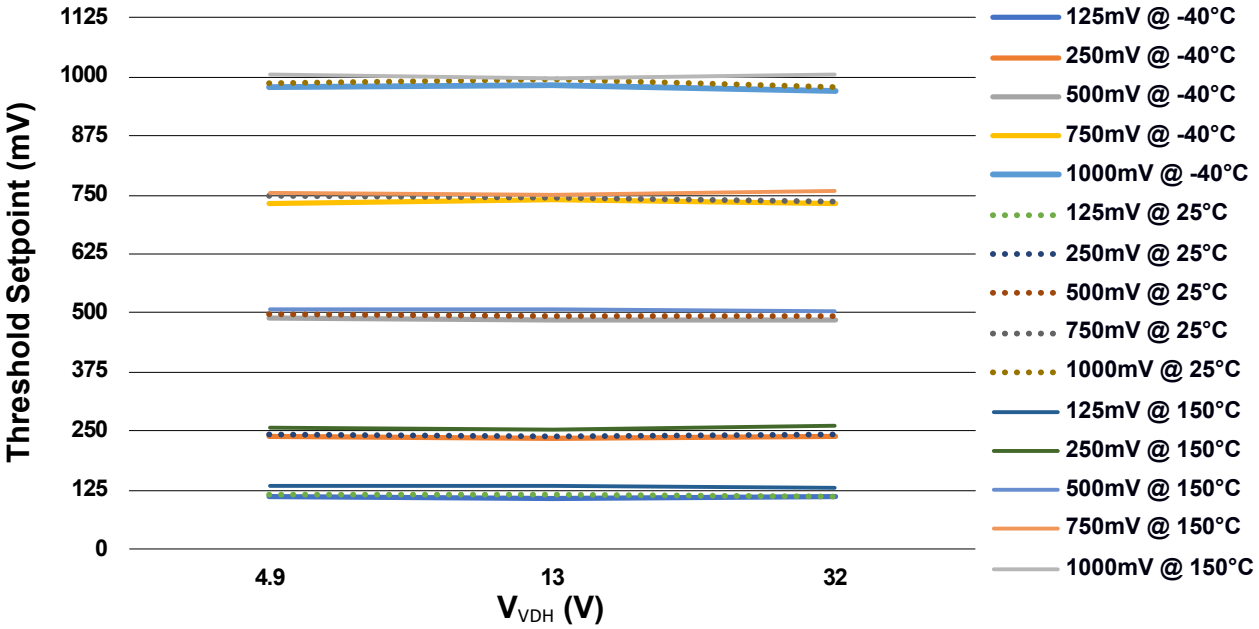


Figure 7-6. Gate Driver Unit Short Circuit Protection Threshold

HS Short Circuit Threshold (V_{SC_TH}) vs. V_{VDH} (SCTHSEL = 0, 1, 2, 3, 4, T = –40, 25, 150)



LS Short Circuit Threshold (V_{SC_TH}) vs. Temperature (SCTHSEL = 0, 1, 2, 3, 4, T = –40, 25, 150)

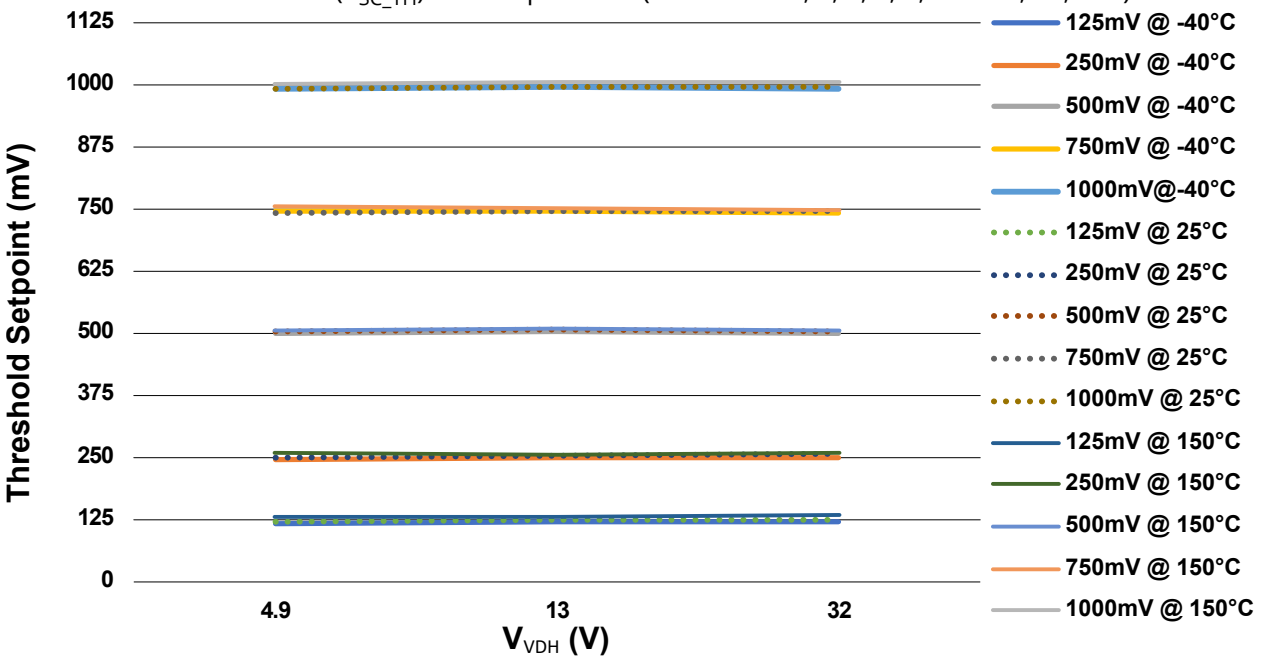
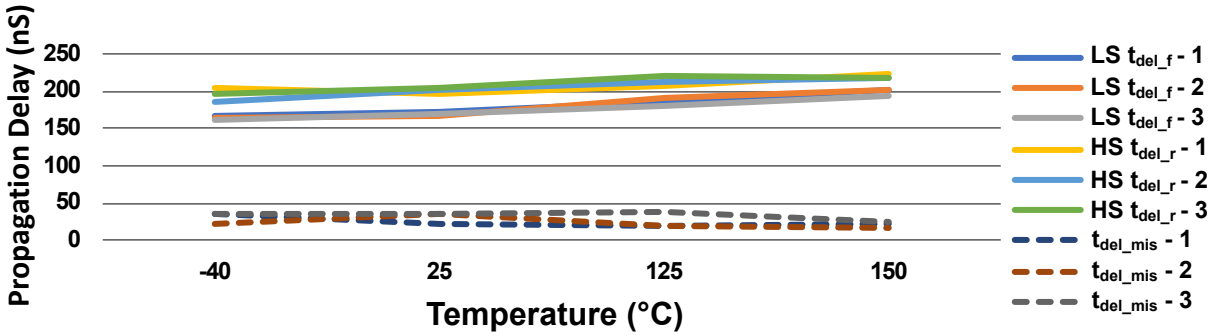


Figure 7-7. Gate Driver Unit Propagation and Mismatch Delay, Rising/Falling Edges (t_{del_f}, t_{del_r}, t_{del_mis})

Low-Side is falling, High-Side is rising

Propagation Delay vs. Temperature (V_{VDH} = 13V, Side = LS, HS, GDU = 1, 2, 3)



Low-Side is rising, High-Side is falling

Propagation Delays vs. Temperature (V_{VDH} = 13V, GDU = 1, 2, 3)

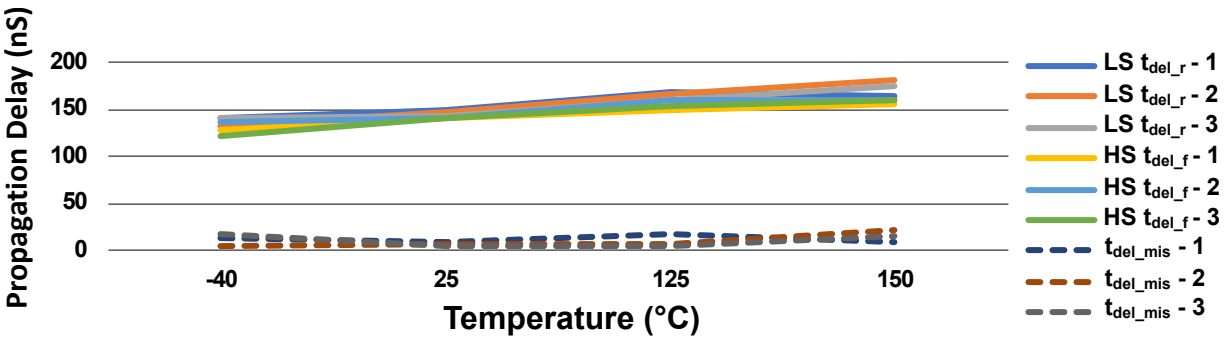
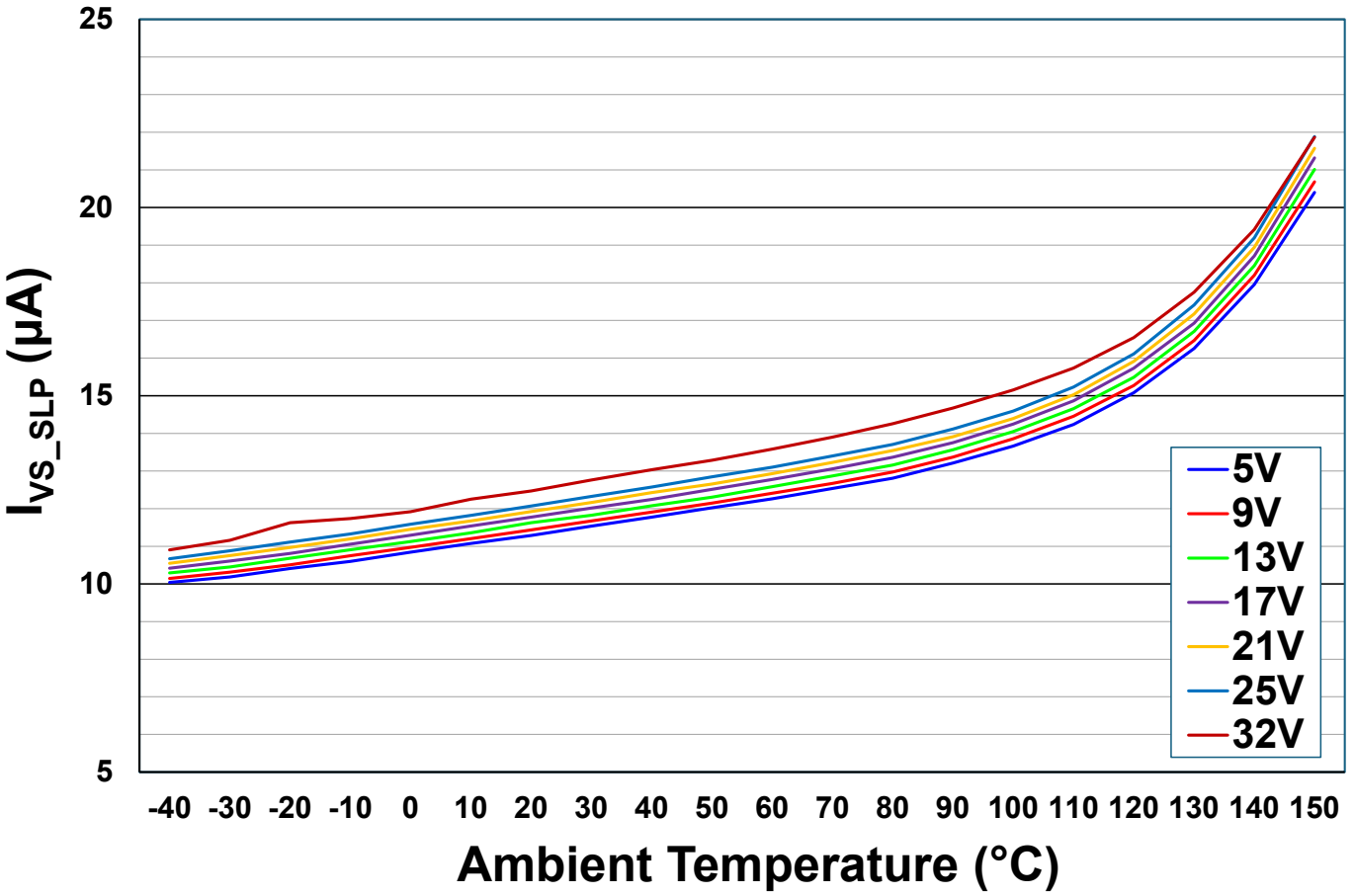


Figure 7-8. Total Sleep Current versus Temperature

Sleep Current (I_{VS_SLP}) vs. Temperature (V_{VS} = V_{VDH} = 5, 9, 13, 17, 21, 25V, 32V)



8. Application Information

8.1. Startup Initialization

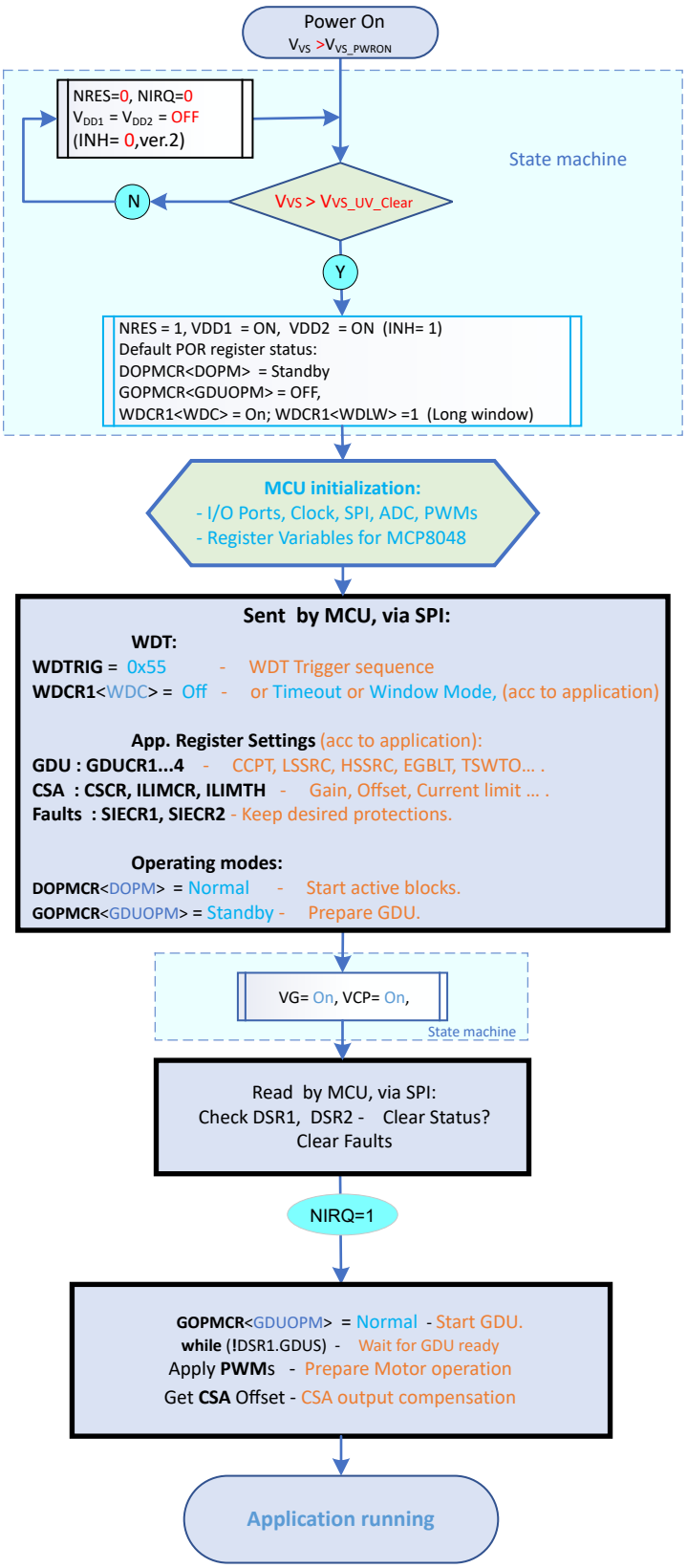
By default, the MCP8048 starts with the watchdog enabled. It is necessary to follow the start-up procedure to enter a normal operation or to reconfigure the watchdog.

As soon as the microcontroller output voltage rises up to the valid operating range, the MCP8048 transitions to Standby mode and deasserts the NRES pin. By default, the WDT starts in Timeout mode. The first microcontroller must trigger the watchdog within the long open window (t_{LW}).

After the first watchdog trigger, the MCP8048 is ready for configuration via SPI. The application should follow the following start-up sequence:

- Once the microcontroller SPI has been initialized, a valid WDT trigger sequence must be sent to the MCP8048 (WDTRIG = `0x55`).
- The watchdog must be configured according to application requirements.
- The remaining MCP8048 configuration registers must be set according to application requirements.

Figure 8-1. MCP8048 Simplified Start-up Procedure



8.2. Back-EMF Motor Control Mode

The closed loop of a BLDC motor control is a Phase-Locked Loop (PLL) based on the rotor position. Note that this inner loop does not attempt to modify the position of the rotor; instead, it modifies the commutation times to match whatever position the rotor has. An outer speed loop changes the rotor velocity, and the commutation loop locks to the rotor position to commutate the phases at the correct trigger times.

The Back-EMF sampler monitors the motor phase voltages. The neutral point Virtual Null simulator calculates the neutral point of the motor based on the following equation:

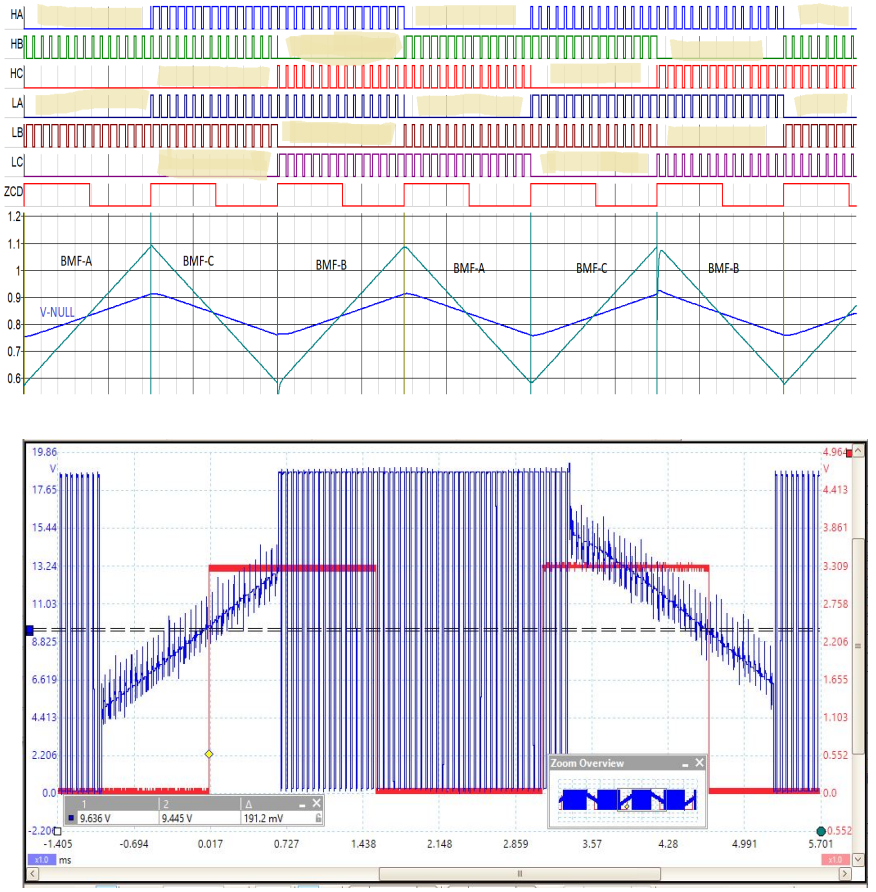
$$VN = (Ph_A + Ph_B + Ph_C)/3$$

The three motor phase voltages are compared with the neutral point. The outputs of the three comparators are available synchronously for estimating the zero-crossing time events accordingly. In '*Star wound* ' motor configuration, no extra wire connection is required. For '*Delta wound* ' motors, there is no physical neutral point available, so the reference point must be estimated.

As the microcontroller knows which motor phase is floating and which two phases are driven to low and high, it is always capable of monitoring the comparator output of the floating phase.

When the Back-EMF signal crosses the neutral point or Virtual Null (VN), the Zero-Crossing Detector (ZCD) will switch the ZC_X signal. The MCU may use this signal as a '*30 degrees before crossing* ' reference point. The MCU must commutate the system after 30 degrees of electrical rotation have occurred. See Figure 8-2.

Figure 8-2. Basic Principles



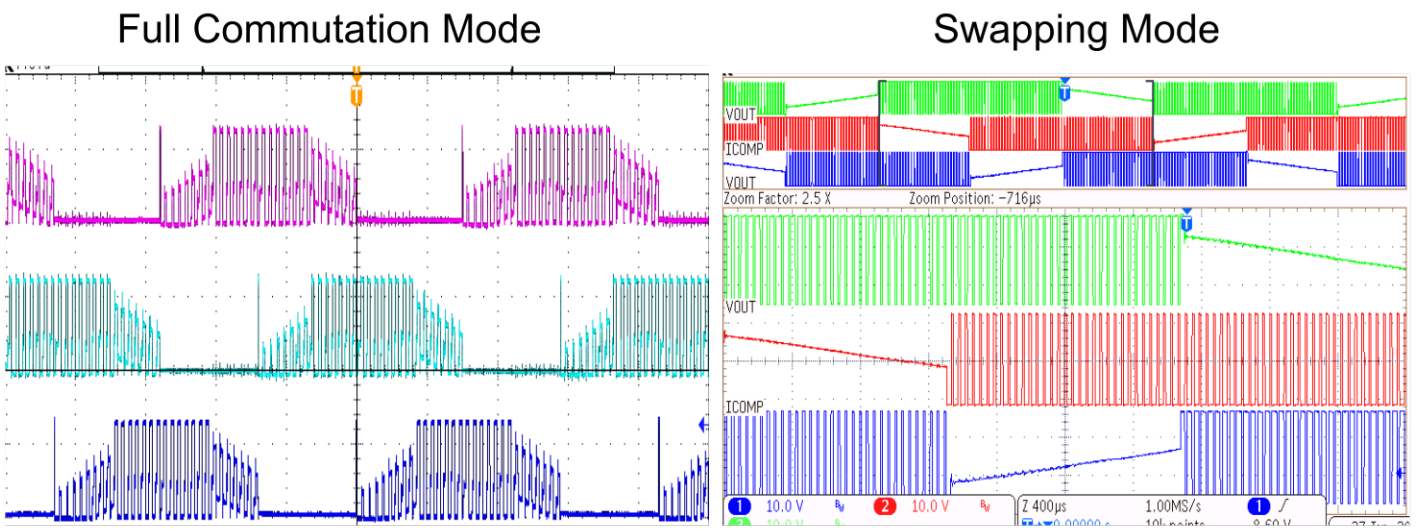
The Zero-Crossing Detection (ZCD) method is typically used in *six-step per electrical revolution* commutation strategies. The motor is driven by energizing two windings at a time. One winding stays unenergized at all times, and the voltage (Back-EMF) on that unenergized winding can be monitored to determine the rotor position.

For more accuracy in rotor angle estimation, it is recommended to use complementary PWMs for the H/L side MOSFET bridge. The comparative Back-EMF waveforms are shown below.

When the motor being driven is at rest, the Back-EMF voltage is equal to zero. The motor rotor needs to be initially rotated for the Back-EMF sensor to lock onto the rotor position and commutate the motor. It is necessary to bring the rotor from rest up to a speed fast enough to generate sufficient Back-EMF voltage (enough to allow the Back-EMF sampler to send it).

Depending on the motor construction and the rotor speed, filtering algorithms are required for stable Zero-Crossing Detection (ZCD).

Figure 8-3. Full Commutation and Swapping Modes

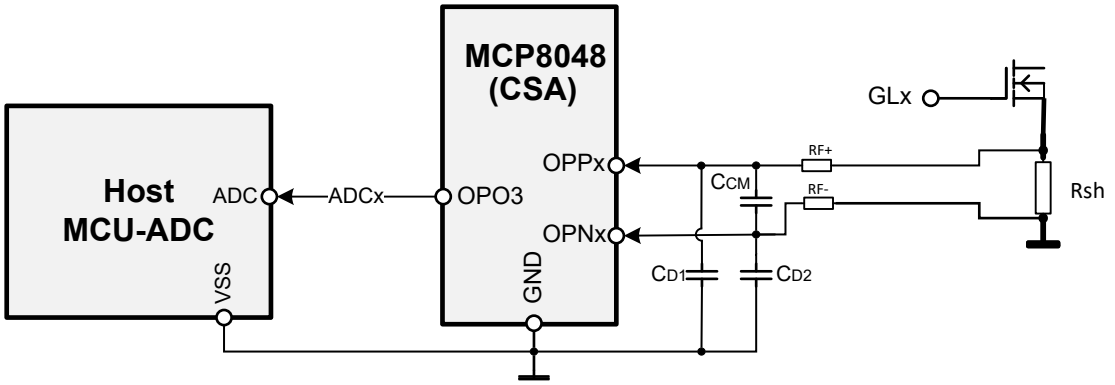


8.3. Current Sense Amplifier Signal Filtering

For high current MC applications, it is required to use a small current sense shunt and a low gain for CSA, in order to match the output signal with the MCU's ADC range.

Due to the CSA's large bandwidth, the sharp parasitic current spikes induced by the external MOSFET bridge commutation can cause the output to be clamped at the rail limits and affect the motor control processing. A filtering method for the signal can be implemented (see CSA Filtering Circuit).

Figure 8-4. CSA Filtering Circuit



Recommended values for filter passives :

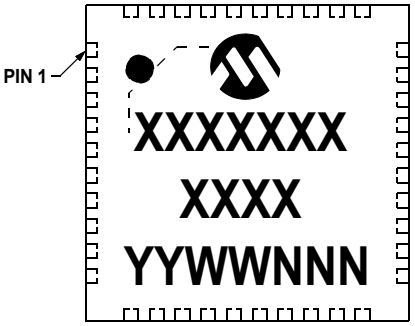
- CCM = 33 nF to 100 nF
- CD1 = CD2 = 12nF to 22 nF
- RF+ = RF- = 4.7Ω to 10Ω

For high efficiency, the filter components should be placed near the CSA inputs. In order to not affect the differential gain and the initial settled offset, the input resistor should stay as low as possible (4.7-10Ω). The filter component selection is based on a 20 kHz PWM frequency.

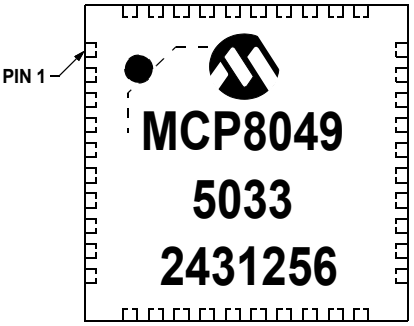
9. Package Information

Package Marking Information

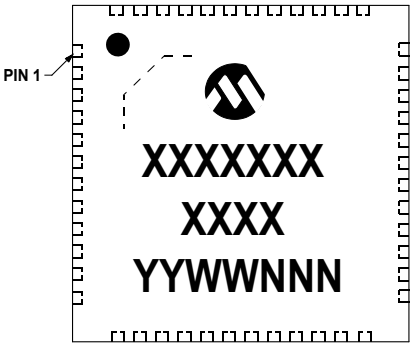
40-VQFN (5 × 5 × 0.9 mm)



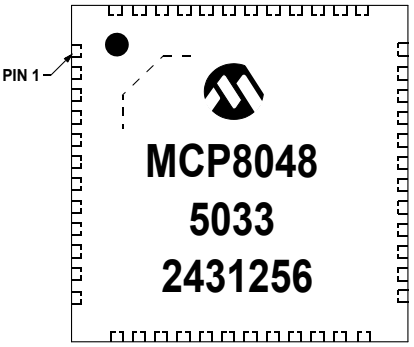
Example:



48-VQFN (6 × 6 × 0.9 mm)



Example:

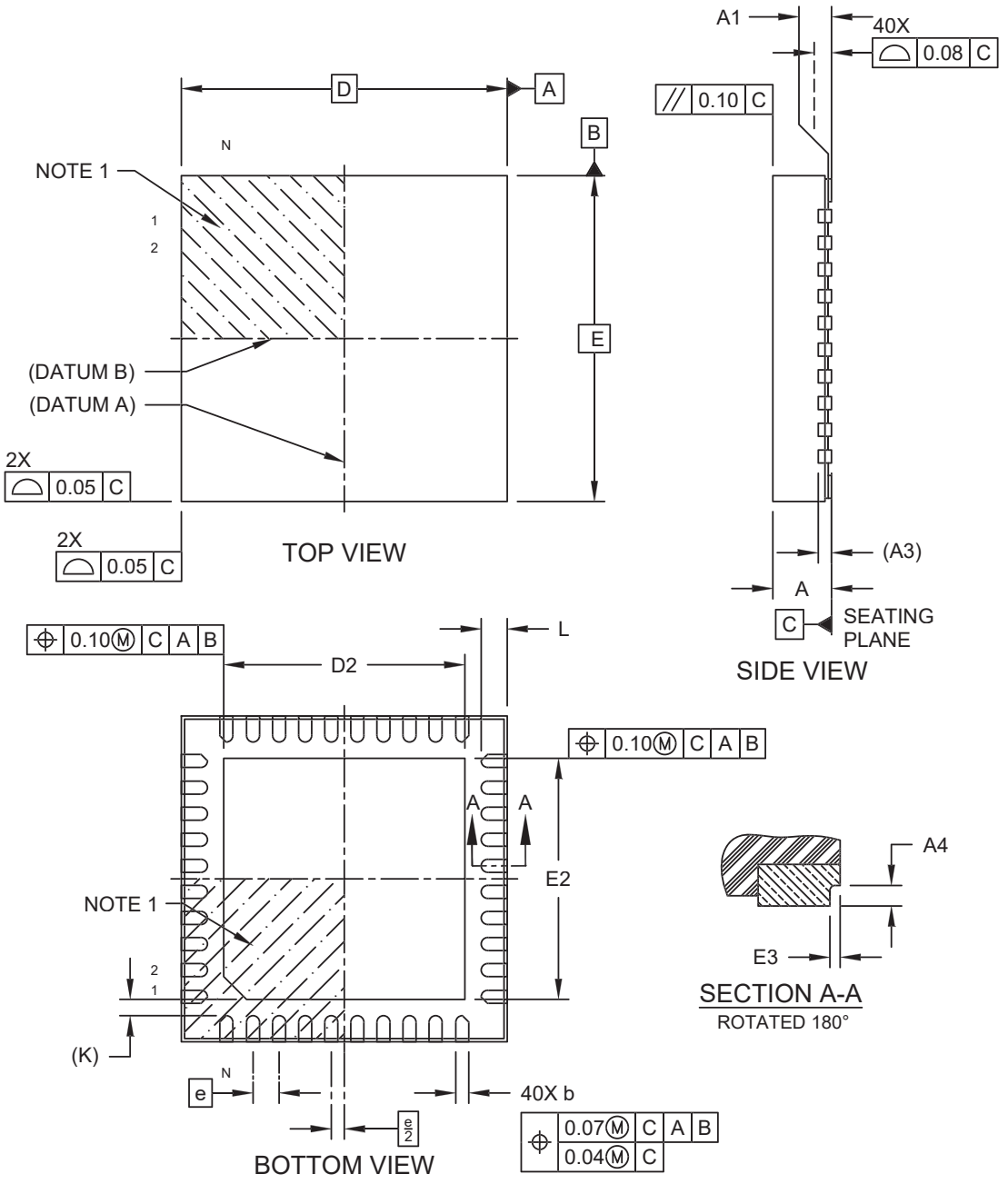


Legend:	XX...X	Product Code or Customer-specific information
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.

40-Lead Very Thin Plastic Quad Flat, No Lead Package (NHX) - 5x5x1 mm Body [VQFN] With 3.7x3.7 mm Exposed Pad and Wettable Flanks

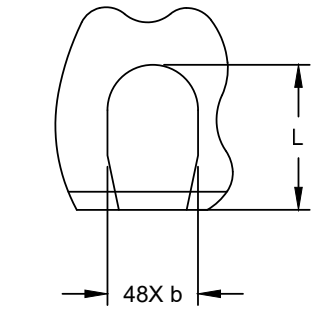
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



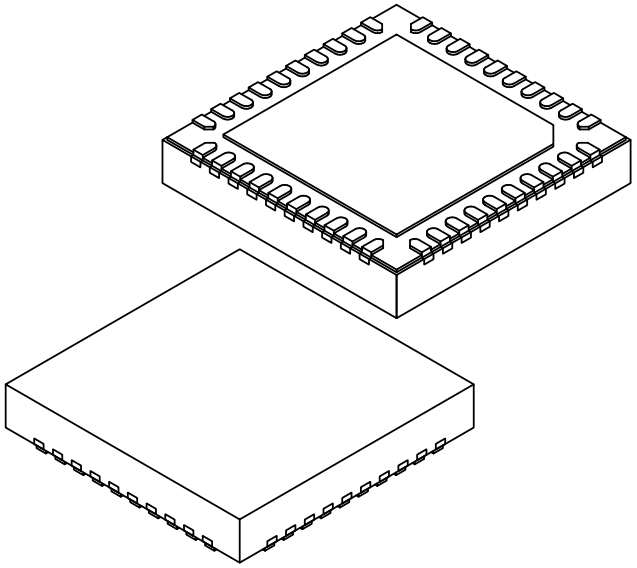
Microchip Technology Drawing C04-00425 Rev E Sheet 1 of 2

40-Lead Very Thin Plastic Quad Flat, No Lead Package (NHX) - 5x5x1 mm Body [VQFN] With 3.7x3.7 mm Exposed Pad and Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL B
ALTERNATE TERMINAL CONFIGURATION



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		40	
Pitch	e		0.40 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.60	3.70	3.80
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.60	3.70	3.80
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.30	0.40	0.50
Wettable Flank Height	A4	0.10	–	0.19
Wettable Flank Width	E3	–	–	0.085
Terminal-to-Exposed-Pad	K		0.25 REF	

Notes:

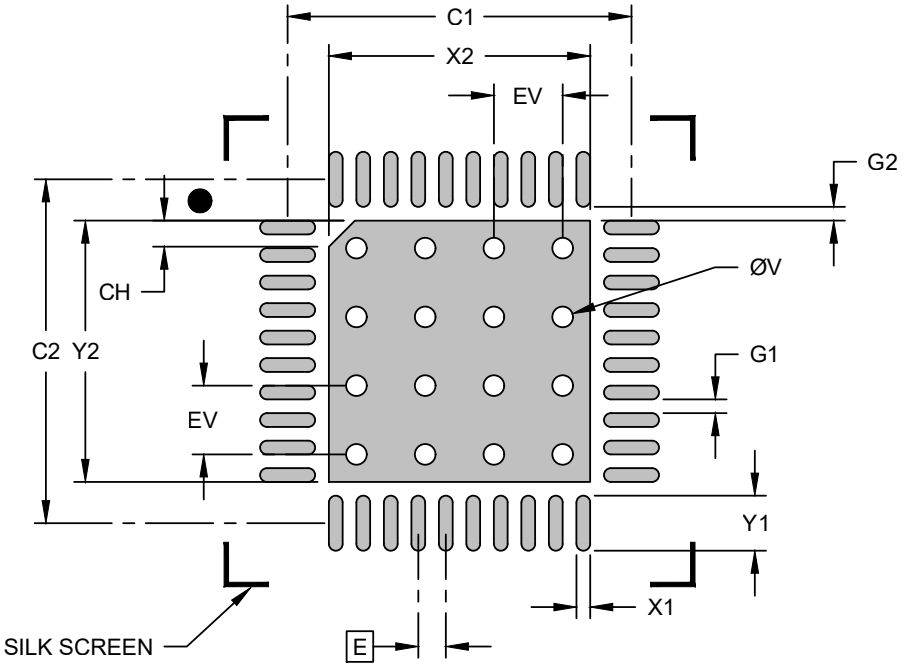
1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. The package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-00425 Rev E Sheet 2 of 2

40-Lead Very Thin Plastic Quad Flat, No Lead Package (NHX) - 5x5x1 mm Body [VQFN] With 3.7x3.7 mm Exposed Pad and Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	X2			3.80
Optional Center Pad Length	Y2			3.80
Chamfer	CH		0.38	
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X40)	X1			0.20
Contact Pad Length (X40)	Y1			0.80
Contact Pad to Pad (X36)	G1	0.20		
Contact Pad to Center Pad (X40)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

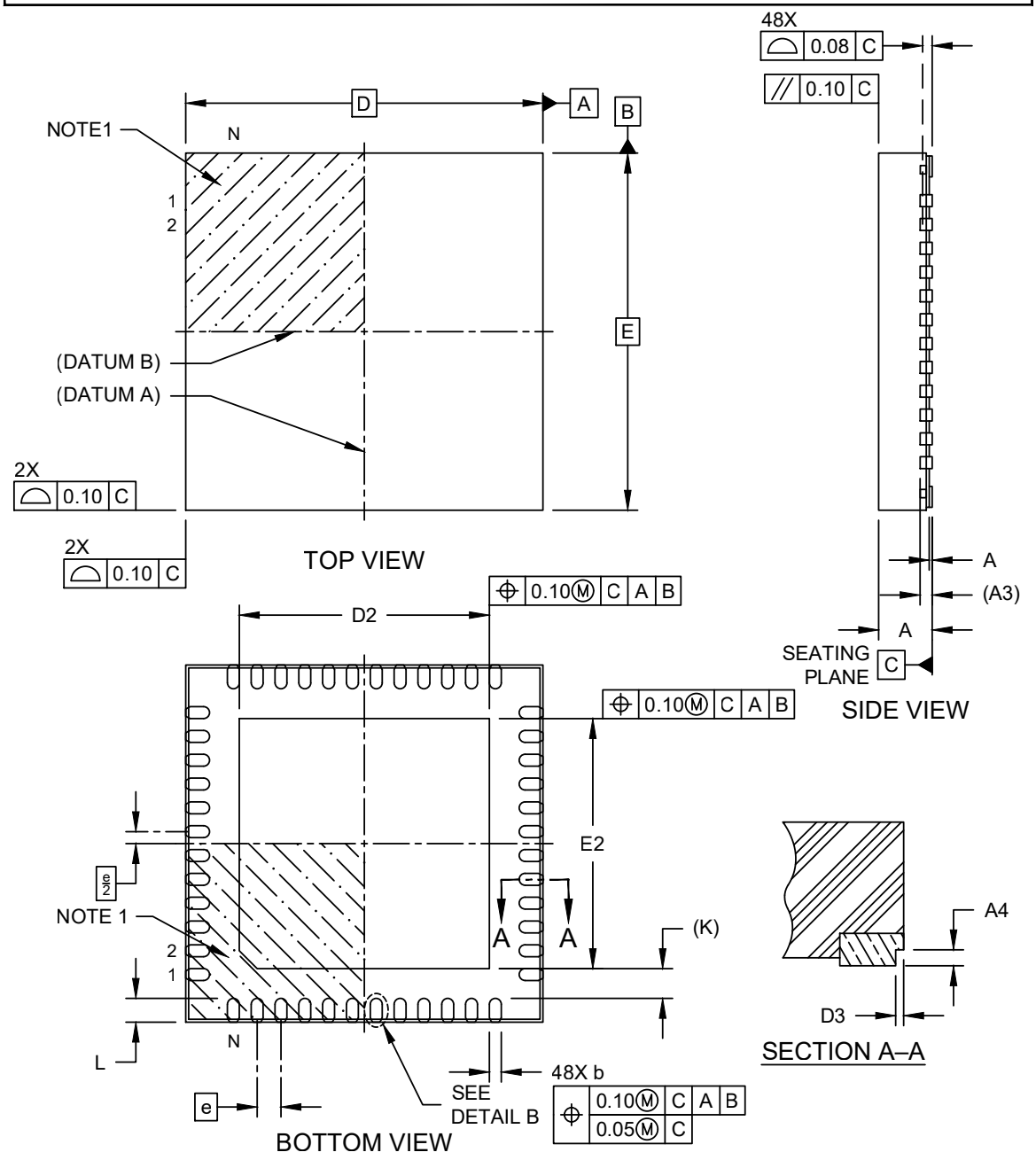
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-02425 Rev E

48-Lead Very Thin Plastic Quad Flat, No Lead Package (ZWX) - 6x6x1 mm Body [VQFN]
With 4.20 mm Exposed Pad and Stepped Wettable Flanks

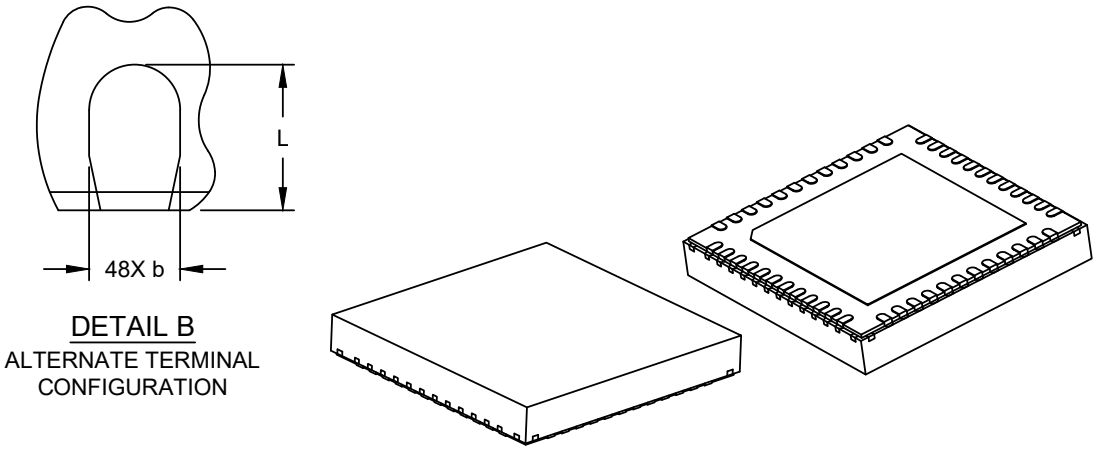
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-00531 Rev C Sheet 1 of 2

48-Lead Very Thin Plastic Quad Flat, No Lead Package (ZWX) - 6x6x1 mm Body [VQFN] With 4.20 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		48	
Pitch	e		0.40 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	4.10	4.20	4.30
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	4.10	4.20	4.30
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.50 REF	
Wettable Flank Step Cut Length	D3	-	-	0.085
Wettable Flank Step Cut Height	A4	0.10	-	0.19

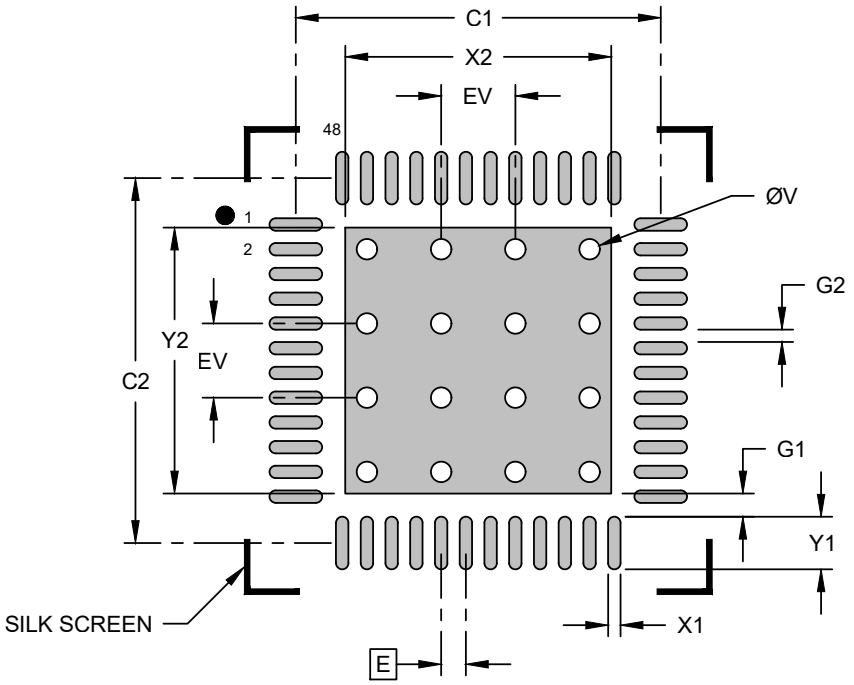
Notes:

1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. The package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-00531 Rev C Sheet 2 of 2

48-Lead Very Thin Plastic Quad Flat, No Lead Package (ZWX) - 6x6x1 mm Body [VQFN] With 4.20 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Center Pad Width	X2			4.30
Center Pad Length	Y2			4.30
Contact Pad Spacing	C1		5.90	
Contact Pad Spacing	C2		5.90	
Contact Pad Width (Xnn)	X1			0.20
Contact Pad Length (Xnn)	Y1			0.85
Contact Pad to Center Pad (Xnn)	G1	0.38		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-02531 Rev C

10. Revision History

Doc. Rev.	Date	Section	Comments
A	07/2026		Initial release of this document.

Product Identification System

To order or obtain information, for example, on pricing or delivery, contact Microchip: https://www.microchip.com/en-us/about/contact-us.

PART NO.	[X](1)	-XX	XX	X	/XXX	XXX
Device	Tape and Reel Option	VDD1	VIO	Temperature Range	Package	Qualification

Device:	MCP8048/MCP8049: 3-Phase Brushless DC (BLDC) Motor Gate Driver with Power Module and Sleep Mode	
Tape and Reel option(1):	T	Tape and Reel (3300/Reel – VQFN package)
VDD1:	50	VDD1=5.0V, VDD2=3.3V
	33	VDD1=3.3V, INH instead of VDD2 for MCP8048-3333/MCP8049-3333
VIO:	50	VIO = 5.0V
	33	VIO = 3.3V
Temperature:	H	-40°C to +150°C, AEC Q100 Grade 0
Package:	NHX	5x5 mm VQFN 40L, Very Thin Quad Flatpack No-Leads, Wettable Flanks, with Exposed Pad (**OpAmp2 and LIN not available in this version**)
	ZWX	6x6 mm VQFN 48L, Very Thin Quad Flatpack No-Leads, Wettable Flanks, with Exposed Pad
Qualification:	VAO	AEC-Q100 Automotive Qualified

Examples:

- MCP8049T-3333H/NHXVAO: Tape and Reel, VDD1 = VIO = 3.3V, High Temp., 5x5 mm VQFN 40L package, AEC-Q100 Automotive Qualified
- MCP8048T-5033H/ZWXVAO: Tape and Reel, VDD1 = 5V, VIO = 3.3V, LIN transceiver with selectable TXD dominant timeout timer disable, High Temp., 6x6 mm VQFN 48L package, AEC-Q100 Automotive Qualified
- MCP8048T-5050H/ZWXVAO: Tape and Reel, VDD1 = VIO = 5V, LIN transceiver with selectable TXD dominant timeout timer disable, High Temp., 6x6 mm VQFN 48L package, AEC-Q100 Automotive Qualified
- MCP8048T-3333H/ZWXVAO: Tape and Reel, VDD1 = VIO = 3.3V, with INH & LIN transceiver with selectable TXD dominant timeout timer disable, High Temp., 6x6 mm VQFN 48L package, AEC-Q100 Automotive Qualified

Notes:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. RoHS compliant, maximum concentration value of 0.09% (900 ppm) for Bromine (Br) and Chlorine (CI) and less than 0.15% (1500) total Bromine (Br) and Chlorine (CI) in any homogeneous material. Maximum concentration value of 0.09% (900 ppm) for Antimony (Sb) in any homogeneous material.
3. Contact your local Microchip sales office to request automotive qualified variants for other package types.

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