



SC1894 FW4.1.03.08 Release Notes

User Guide

UG6342; Rev 2; 10/16

Abstract

This document provides information to evaluate the operation and performance of the SC1894 with different power amplifiers.

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1. Introduction

1.1. *Overview*

Firmware 4.1.03.08 is a production release firmware based on 4.1.01.01. The major modification is that the FW does not access the one-time programmable (OTP) memory. This FW modification does not affect the linearization performance since none of the linearization algorithms have been changed. The OTP memory was previously used to select different bundles and store ATE calibration parameters. The feature selection function is no longer needed since all features are available for a given FW (See section 4.5.3 for Firmware Boot Procedure Change Diagram).

The SC1894 RF PA Linearizer (RFPAL) is designed to fully address the linearization requirements for cellular infrastructure (LTE, TD-LTE, WCDMA, WiMax®, EVDO), VHF and UHF terrestrial broadcast television (CMMB, DVB-T, ISDBT, ATSC), and other systems. The SC1894 is pin-to-pin compatible with prior generations of RFPAL, provides improved linearization performance and a wider operating frequency range of 225MHz to 3800MHz. FW 4.1 does support operation from 3.8GHz to 4.2GHz for evaluation and prototyping only.

Note: only the 225MHz to 3800MHz frequency range has been qualified for production in this FW release.

SC1894 includes the following three levels of features:

- Linearizer
 - Power indicator sliders based on RFIN AGC (PDET) and RFFB AGC values. A new scratch variable was added to always reflect the current value of the RFFB AGC index being used by the firmware.
 - Added EEPROM parameters for GaN performance improvement. See SC1894 SPI programming guide [4] for details.
 - Lower Freeze Threshold was changed from 21dB to 15dB. See [4] for details.
 - Wideband performance for fully and non-fully occupied signals
 - Support the following external clock system clock rates (MHz): 10, 13, 15.36, 19.2, 20, 26, and 30.72.
- RFIN and RFFB Power Measurement Unit (PMU)
 - Independent RFIN and RFFB Power Measurement. See section 5 for detail.
- Features for debug purposes only (no performance guaranteed)
 - Spectrum monitoring and alarm
 - CCDF. See section 5 for detail.
- AdvGUI2.5.10 advanced GUI to allow access to EEPROM Customer configuration parameters in ACCP tab. These parameters are described in the SC1894 SPI programming guide [4]. GUI 2.5.8 or Advanced GUI 2.5.10 are required to operate this Firmware 4.1.03.08 and Evaluation kits (EV kits). Read “Scintera¹ GUI Installation Guide” [2].

 *It is required to un-install all previous GUI versions and all previously installed firmware before installing GUI 2.5.8 or AdvGUI2.5.10.*

 *After upgrading from previous firmware to 4.1.03.08, it is required to redo Smooth Calibration from the GUI or to send special SPI command to copy ATE calibration parameters from OTP to EEPROM. See SC1894 SPI programming guide [4] for details.*

¹ *Scintera is part of Maxim Integrated.*

- **SC1894 Frequency Bands (MHz):**

Frequency Bands	Range (MHz)
09	3300-3800
08	2700-3500
07	1800-2700
06	698-2700 ¹
05	1040-2080
04	520-1040
03	225-960 ¹
02	260-520
01	225-260

¹ Stitched ranges. To limit spurious, it is recommended to limit min and max frequency-scanning range to the frequency range needed for the application.

Evaluation Kits (Contact Maxim Integrated Sales for availability):

Frequency (MHz)	EV Kits
3300-3800	(P/N SC1894-EVK3400)
2300-2700	(P/N SC1894-EVK2400)
1800-2200	(P/N SC1894-EVK1900)
1350-1800	(P/N SC1894-EVK1500)
698-960	(P/N SC1894-EVK900)
470-928	(P/N SC1894-EVK500)
225-470	(P/N SC1894-EVK200)

1.2. *Scope*

This document is meant to provide a comprehensive user guide for the SC1894 with FW 4.1 in order to evaluate the operation and performance with a given power amplifier. The documents referenced in section 1.5 are companion documents for use when implementing the SC1894 in a design.

1.3. Limitations

- RFIN and RFFB power levels reported by GUI need to be calibrated since the offset varies with the EV kit frequency band.
- The RFFB AGC index parameter used by the GUI switches to “0” during PMU cycle.
- SC1894 supports instantaneous signal bandwidths from 1.2MHz to 75MHz.
- The SC1894 is guaranteed to operate across power supply and temperature variations as specified in the data sheet. Operation above 3.8GHz is limited to 25°C, for evaluation purposes only and not guaranteed. If operation across full operating conditions is required for operating frequencies above 3.8GHz, contact Maxim sales.
- The following features are no longer supported:
 - Internal temperature monitoring and alarm.
 - Four general-purpose DAC outputs that may be configured analog functions including reference voltage or current sourcing, or as additional digital outputs.
 - Four ADC for monitoring and alarm functions:
 - External temperature.
 - Voltage monitoring or reverse power detector measurement.

1.4. Reference Documents

Document	
[1]	SC1894 FW4.1.03.08 Quick Start Guide
[2]	Scintera GUI Installation Guide
[3]	SC1894 Hardware Design Guide
[4]	SC1894 SPI Programming Guide
[5]	SC1894 Data Sheet
[6]	SC1894 and PA system design power budget calculator
[7]	Designing Linearizable RF PA using RFPAL

1.5. Revision History

Revision	Date	Description
1.0	May 2013	Initial Release
1.1	May 2013	FW 4.1.01.01 fixes an issue in firmware 4.1.01.00 with narrow-band signal less than 3MHz. Added Guard Band parameter for Wideband optimization. It is strongly recommended to upgrade to FW 4.1.01.01
1.2	July 2014	FW 4.1.03.08 enables all features for all bundles and no longer accesses the OTP memory.
1.3	February 2015	Added AdvGUI2.5.10 for customers to be able to access EEPROM Customer configuration parameters. Updated 4.1.03.08.sci to include the different customer configuration parameters. No change to the firmware.
2	October 2016	Initial Release to web page. General edits to remove requirement for NDA to access SC1894 collateral. Updated Error/Warning section. Added sections on quick start guide and Scintera Advanced GUI. Removed features no longer supported. General edits. 4.1.03.08.sci updated to expose more parameters. No change to the firmware.

2. Quick Start Guide

To get started with the evaluation, the following steps are recommended:

- Install the GUI as described in Scintera GUI Installation Guide [2].
- Check SC1894 evaluation kit hardware configuration in section 2.
- Set-up SC1894 evaluation kit with PA line-up as described in section 3.
- First, focus on testing a static waveform at the PA maximum output power targeted in Optimized mode. Make sure to reset SC1894 after changing the PA or signal conditions.
- For performance optimization, refer to section 2.4.
- For tuning your power amplifier, refer to the application note “Designing_Linearizable_RF_PA_using_RFPAL application” [7].
- For dynamic performance, make sure to first calibrate in smooth mode. Refer to section 4.6.2.1.
- Refer to detailed operation of SC1894 available in section 4.
- Description of the Power Monitoring Input features available in section 5.
- Description of the debug features in section 6.
- Example of performance data in section 7 and in SC1894_PA_Results folder.

3. SC1894 Evaluation Kit Setup

3.1. SC1894 Evaluation Board with integrated delay line

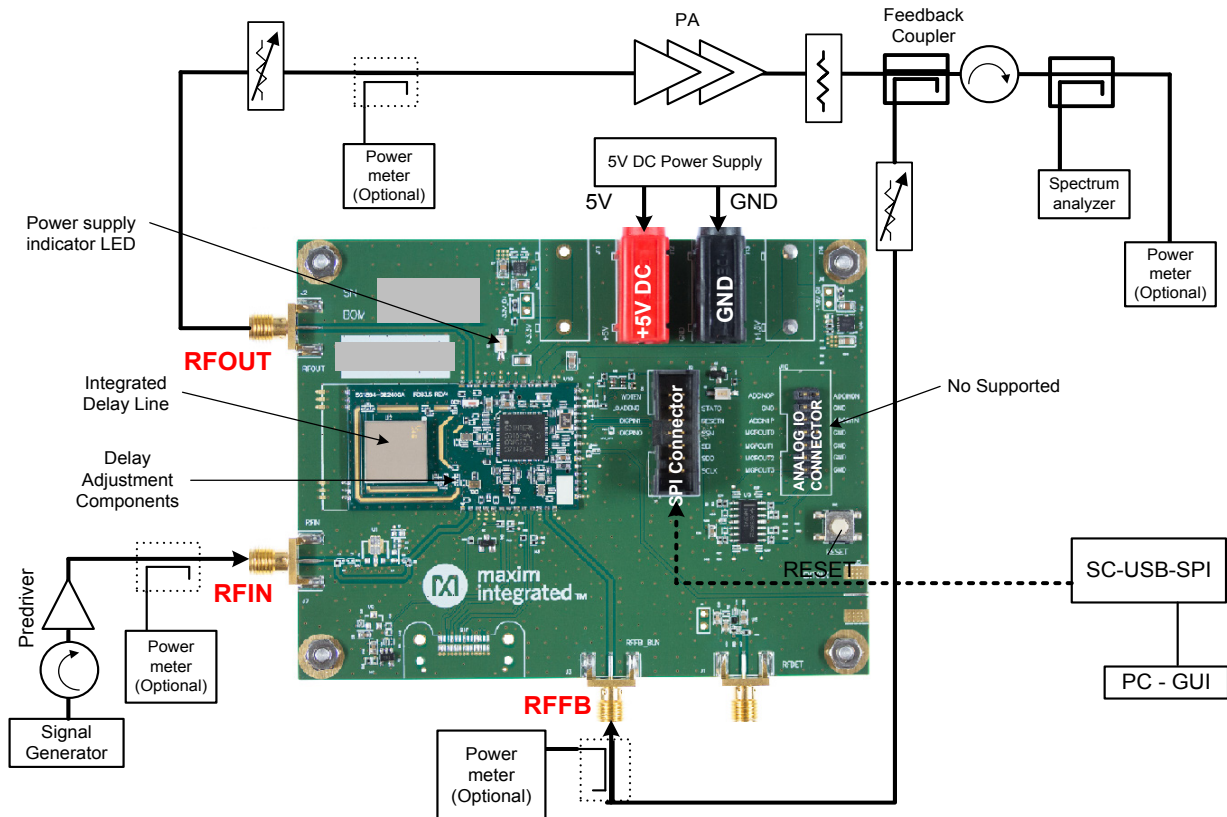


Figure 1. SC1894 evaluation board connection diagram.

1. The SC1894 Evaluation Board must be powered from a +5V, DC power supply capable of providing 0.6A (although the actual average power consumption of SC1894 is lower). Connect the power supply to the banana jacks on the SC1894 Evaluation Board labeled +5V (red) and GND (black).
2. RFOUT is connected to the power amplifier input. The attenuator between the RFOUT and the PA is useful for setting the RFIN level of the Linearizer (assuming that the PA is adjusted to a fixed output power) and should be set using the RFIN AGC slider on the GUI. While not absolutely required, it is helpful that an adjustable attenuator is used for setting the power level of the RF power amplifier.
3. RFFB is connected to the power amplifier feedback coupler. While not absolutely required, it is helpful during the optimization of the linearization performance, to adjust the attenuator to set the RFFB level into the evaluation board by using the RFFB AGC slider.

IMPORTANT — RFIN and RFFB level should follow the recommendations from section 4.4.

4. Connect the USB cable from NI-8451 or SC-SPI-USB to the PC. Maxim recommends using a USB cable less than 4ft-long.
5. Reset SC1894 using either the GUI or the board reset button.

Multiple PCB configurations were required in order to cover all the frequency bands as specified in the data sheet. The different board configurations were required to accommodate the different coupling ratios for RFIN and RFOUT couplers as described in **Table 1**. It is important as well in the gain lineup to take into account the RFIN to RFOUT loss described in that same table.

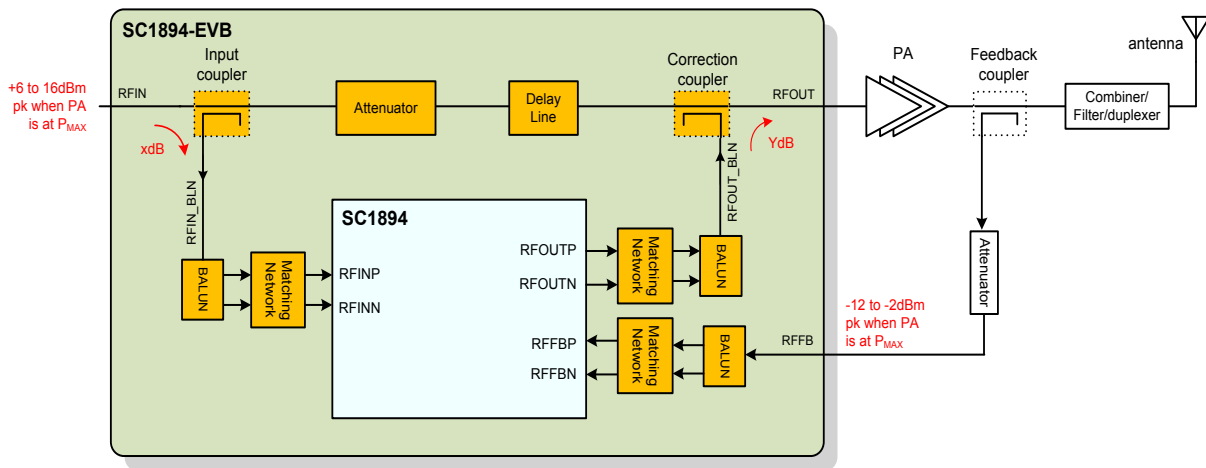


Figure 2. SC1894 system block diagram.

Table 1. RFIN and RFOUT couplers for SC1894 Evaluation Boards

EV Kit #	Frequency Range (MHz)	RFIN Coupler	RFOUT Coupler	RFIN-RFOUT loss (dB)
SC1894-EVK3400	3300-3800	5	7	9.5
SC1894-EVK2400	2300-2700	10	6	6.5
SC1894-EVK1900	1800-2200	10	7	6
SC1894-EVK1500	1350-1800	10	10	4.4
SC1894-EVK900	698-960	10	10	3.5
SC1894-EVK500	470-928	10	10	4
SC1894-EVK200	225-470	10	10	3.5

3.2. Programmable Through-Path Delay Line and Attenuator

The SC1894 EV kit printed circuit board integrates a ceramic delay line (Richardson DL246) whose delay is programmable through external jumper settings. In original configuration from Maxim, the delay value is set to 4ns (Figure 3). By modifying the location of the 0 Ω jumpers, the delay can be set to 2ns and 6ns or to 0ns bypassing the delay line (Figure 3 to Figure 6).

Provisions are also available for a through-path pi-attenuator.

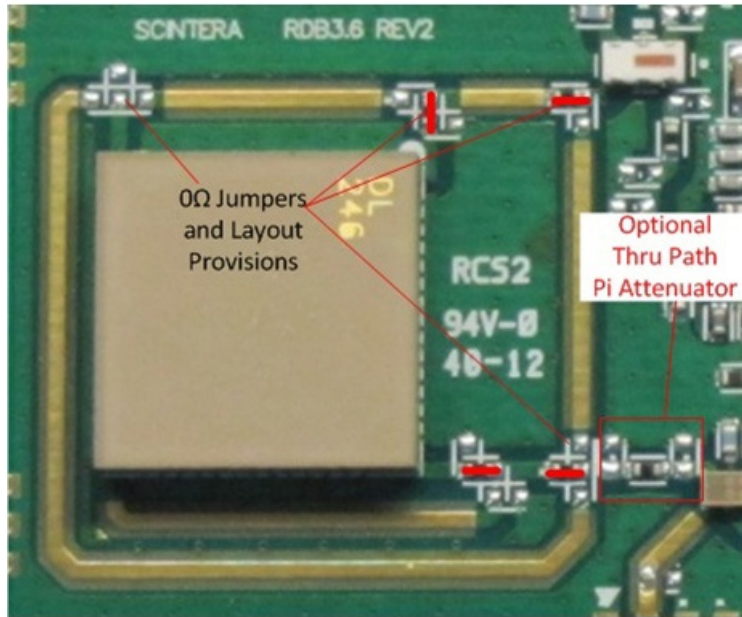


Figure 3. Delay Line DL-246 default configuration for 4ns.

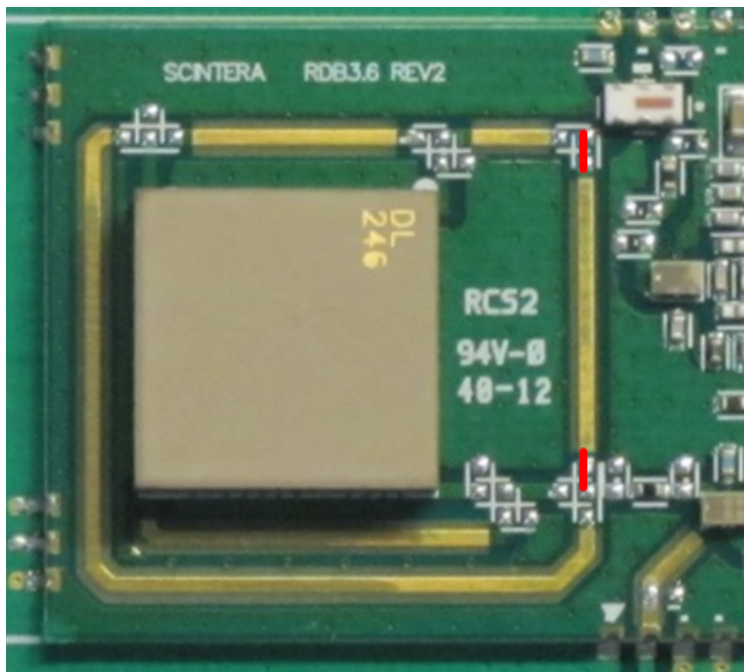


Figure 4. Location of 0 Ω jumpers for 0ns delay.

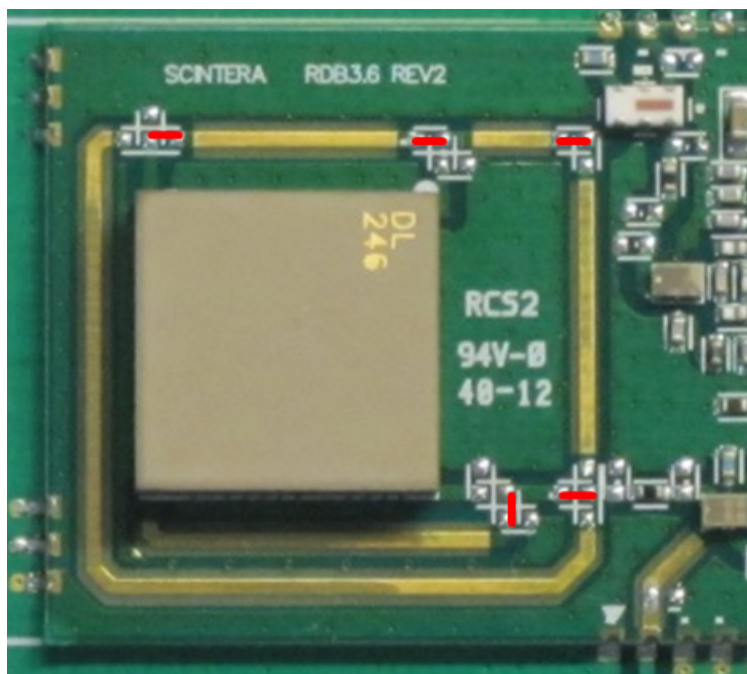


Figure 5. Location of 0Ω jumpers for 2ns delay.

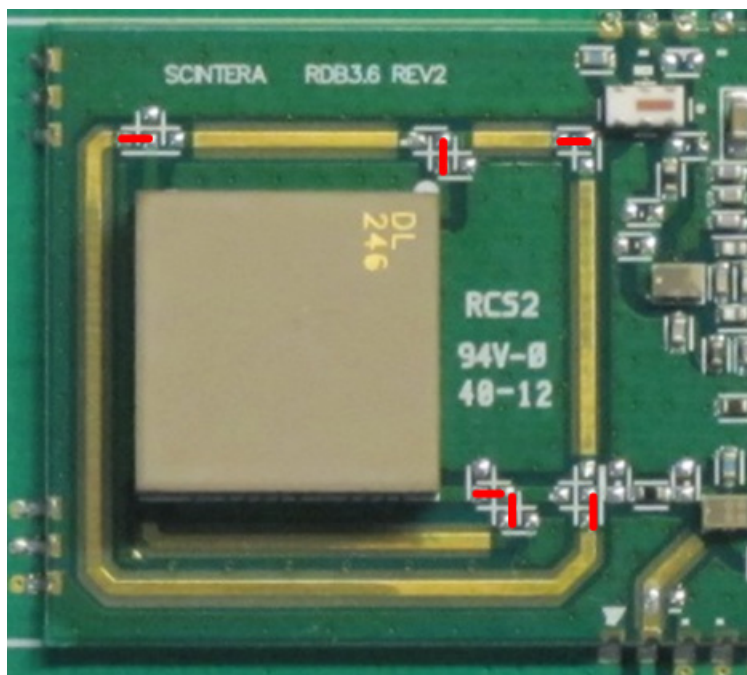


Figure 6. Location of 0Ω jumpers for 6ns delay.

3.3. Power Supply Connections and Regulators

In default configuration, Evaluation Boards require only 5V power supply connections (**Figure 7**). Onboard regulators are used to generate supply voltages (1.8V and 3.3V) for RFPAL IC.

In case it is required to bias RFPAL directly using external 3.3V and 1.8V supplies, provisions for connectors are available on the EV kit board as shown in Figure 7. Regulator outputs must be disconnected by removing 3.3V and 1.8V jumpers shown.

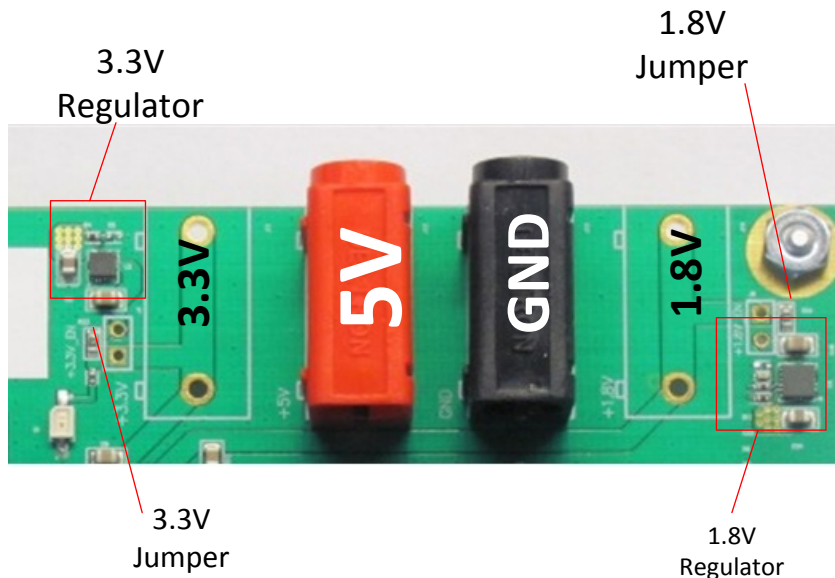


Figure 7. SC1894 - EV kit power supply connections.

3.4. What to look for if performance is lower than expected?

- Make sure that the Status Indicator indicates “TRACK.” If not, then SC1894 has not fully converged to the optimal solution.
- Check the linearity of the signal source provided to the linearizer. A predriver between the signal generator and RFIN might be required to ensure that the signal source has enough linearity. It is recommended that the input linearity be at least 5dB to 10dB better than the desired linearity at the PA output.
- Check that RFIN and RFFB are at the recommended levels at the PA maximum output power (see section 3.1).
- Make sure the spectrum analyzer internal attenuation is not too high, increasing the noise floor and limiting performance. Reduce the spectrum analyzer’s attenuation as much as possible while not overdriving the analyzer.
- Make sure the PA is not running into compression (see section 6.2).
- Try different delay line values, especially in case of signal bandwidth greater than 20MHz (see section 3.2). Make sure the firmware is configured to the correct frequency range and the input signal is within the frequency scanning boundaries (see section 4.3.3).
- For non-fully-occupied signals, it is recommended to configure some parameters as defined in the SPI programming guide [4].

3.5. Signal Generator Considerations for Power Level Change Performance Tests

To prevent the signal generator from transmitting undesirable peaks during power level changes, it is required to take the following precautions.

- With some signal generators, it is important to turn ALC OFF and to configure “Power Search” properly.
 - Select “Manual” option if available.
 - With some signal generators, “Power Search” doesn’t have a “Manual” option. In this case, select “Span.” Then select “Configure Span Power Search” and select “User” for “Span Type” and configure “Start Frequency” and “Stop Frequency” to the center frequency of the signal test.

4. SC1894 Hardware Setup

4.1. RFIN and RFFB Levels

For optimal performance, it is required to set the correct RFIN and RFFB levels into SC1894 as described in the SC1894 data sheet [5]. As shown in Table 2, the different SC1894 EV kits have different offsets over frequency and it is important to calibrate the RFIN and RFFB offsets in the GUI.

If the system is set up as described in the following tables, the linearization provided by SC1894 should be sufficient over the entire output-power operating range of a typical power amplifier. The amount of correction required by the amplifier generally decreases as the PA-output power is backed off (constant SEM specifications).

For example, for SC1894-EVK1900 with 10dB RFIN coupler and 8dB PAR, it is recommended to set RFIN and RFFB power levels when the PA is at maximum output power:

- RFIN = +6dBm RMS, which is +14dBm peak into the coupler
- RFIN_BLN = -4dBm RMS, which is +4dBm peak into the Balun
- RFFB = -12dBm RMS, which is -4dBm peak.

4.2. RFIN and RFFB Evaluation Board Offsets

The RFIN and RFFB power measurement values reported by the GUI reflect the power level into SC1894. To reflect the power level into the SC1894 EV kit SMA connectors or any other reference points, calibration is required as explained in section 5.1 to adjust the RFIN and RFFB offsets. These offsets depend on the board design due to the RFIN coupler ratio and board loss as shown in Table 2.

Table 2. SC1894 EV Kit RFIN and RFFB Offsets over Frequencies

EV Kit	Frequency (MHz)	RFIN Offset ¹ (dB)	RFFB Offset ² (dB)
EVK3400 ³	3550	7.7	-3.5
EVK2400	2550	11.9	0
EVK1900	2000	11.9	1.7
EVK900	900	10.6	0.4
EVK500	500	9.6	0.4
EVK200	250	9.8	0

1. RFIN Offset = RFIN Measured at SMA Connector on SC1894 EV kit RFIN PMU value (Default in GUI = 0dB).
2. RFFB Offset = RFFB Measured at SMA Connector on SC1894 EV kit RFFB PMU value (Default in GUI = 0dB).
3. For SC1894-EVK3400, more fluctuation expected for reported PMU value due to board-to-board variation and PMU accuracy only up to 2.7GHz.

IMPORTANT: RFIN and RFFB offsets are provided as examples and are expected to vary over ICs and EV kits. See GUI figures in 4.1 for an example.

4.3. Through-Path Delay and Loss

The evaluation kit board utilizes a Kyocera DL246 for the delay line. This integrated delay line provides a 2ns delay line and a 4ns delay line that can be connected to form a 6ns delay. The evaluation kit board can be configured with 0Ω jumpers to either ~0ns, 2ns, 4ns or 6ns through path delay using the onboard DL246, or it can be configured to use an external delay line.

Table 3. DL246 4 ns Delay Insertion Loss

Parameter	Typical	Units	Frequency (MHz)
Delay	4	ns	225-3800
Insertion Loss	1	dB	225
Insertion Loss	1.3	dB	450
Insertion Loss	1.6	dB	700
Insertion Loss	1.8	dB	900
Insertion Loss	3.2	dB	2140
Insertion Loss	3.7	dB	2800
Insertion Loss	4.8	dB	3600
Insertion Loss	5	dB	3800

A through-path delay line between the input and output couplers (see Figure 3 for coupler locations) that approximates the internal delay of SC1894 can be required for optimal performance, especially for bandwidths wider than 20MHz.

For most PA applications, the optimal delay is approximately 3ns to 4ns; this is the length of the delay circuit integrated with the evaluation kit. Some designs may require more or less delay in the through path to optimize performance. Maxim suggests making system measurements with the following delay-line options:

1. 4ns (integrated)
2. 2ns
3. 6ns
4. Minimal delay

For most PA's, the optimum delay value is 3ns to 4ns for best performance. For amplifiers that exhibit more than usual memory effects, 6ns can provide better performance. Similarly, for a PA with little memory effect, a 2ns delay line may be sufficient. The optimum delay line should be determined during product development.

NOTE

- The absolute phase of the delay line is not critical.
- The delay-line delay accuracy is not critical.
- The performance difference between 2ns, 4ns, and 6ns is usually less than 3dB of correction at maximum output power.

4.4. Average Coefficient Indicator

The SC1894 provides an average coefficient indicator. The average coefficient indicator gives an indication if the SC1894 is operating within the optimal range for linearizing the amplifier under test. The average coefficient indicator, if checked, should be done once TRACK is reached at maximum output power. At the same time, the final linearity (ACLR or IMD level) of the system under test should be measured. This is intended to be used as an indicator during manufacturing as part of a factory alignment and verification. It is not intended to be used to monitor the system in field operation.

The SC1894 correction-signal processor is capable of operating over a wide-dynamic range. For this reason, the valid operating range can span a wide range of values. The optimal location for the indicator also heavily depends on the PA's IMx roll-off performance. As a general rule, the average indicator should be lower if the PA's IMs roll off very fast (i.e., IM3 >> IM5, etc.) or higher if the IMs are more 'flat' (i.e., IM3 ~ IM5, etc.). It is not recommended to "over optimize" using this parameter; any value within the range and possibly even beyond is a valid condition if the resulting corrected performance meets expectation.

If the Avg Coeff Val > 100 when operating at the typical power amplifier maximum output power and the system linearity is not as expected, then this is an indication that the correction power at RFOUT is not at a sufficient level to correct the amplifier. The path loss from RFOUT_BLN to RFOUT should be verified and a lower coupling factor used for the RFOUT coupler, or in case an attenuator is used in this path, it should be reduced.

If Avg Coeff Val < 10 at the typical power amplifier maximum output power, the ratio of correction power to signal power might be too high. A typical measure would be to increase the coupler value or insert an attenuator in the RFOUT path.

4.5. External Clock Configuration

The SC1894 provides support for the following standard system clock rates (MHz): 10, 13, 15.36, 19.2, 20, 26, and 30.72. When the external clock rate is selected, then the GUI automatically configures the required EEPROM parameters. Refer to the SPI programming guide [4] for details on selecting these clock rates from the host.

To test external clock, it is required to modify SC1894 EV kits.

4.6. Evaluation Kit Board Typical Power Consumption at 25°C

4.6.1. SC1894 Evaluation Kit Board Typical 5V Power Consumption at 25°C

Table 4 shows the SC1894 evaluation kit board typical 5V power consumption at room temperature (25°C).

Table 4. Typical 5V Average Power and Current Consumption for SC1894 EV Kit (25°C)

Conditions ¹	5V Current (mA)	Total Power (mW)
No Firmware Running	34	170
Average Current/PWR During INIT/CAL Modes	208	1025
FSA/TRACK Duty-Cycled Feedback OFF	241	1205
TRACK Duty-Cycled Feedback ON ²	117	585

NOTE:

1. Measurements made at the +5V supply of the SC1894 EV kit.
2. Average for Duty-Cycled Feedback ON: 10% ON and 90% OFF. ON Time is 100ms and OFF time is 1s. Total period is 1.1s.

4.6.2. SC1894 Evaluation Board Typical 1.8/3.3V Power Consumption at 25°C

Table 5 shows SC1894 evaluation board typical 1.8V and 3.3V power consumption at room temperature (25°C).

Table 5. Typical 1.8V and 3.3V Power Consumption for SC1894 (25°C)

Conditions ¹	1.8V Current (mA)	3.3V Current (mA)	Total Power (mW)
No Firmware Running	10	19	243
Average Current/PWR During INIT/CAL Modes	366	63	867
FSA/TRACK Duty-Cycled Feedback OFF	427	56	1006
TRACK Duty-Cycled Feedback ON ²	211	29	476

NOTE:

1. Measurements made at the +1.8V and 3.3V supply connections of SC1894.
2. Average for Duty-Cycled Feedback ON: 10% ON and 90% OFF. ON Time is 100ms and OFF time is 1s. Total period is 1.1s.

5. SC1894 Linerization Operation

This section describes how to change certain parameters within the SC1894 as well as how to access status information over the SC1894 SPI. The supplied Scintera GUI enables the user to access the SC1894 SPI using the SPI to USB converter.

5.1. SC1894 GUI

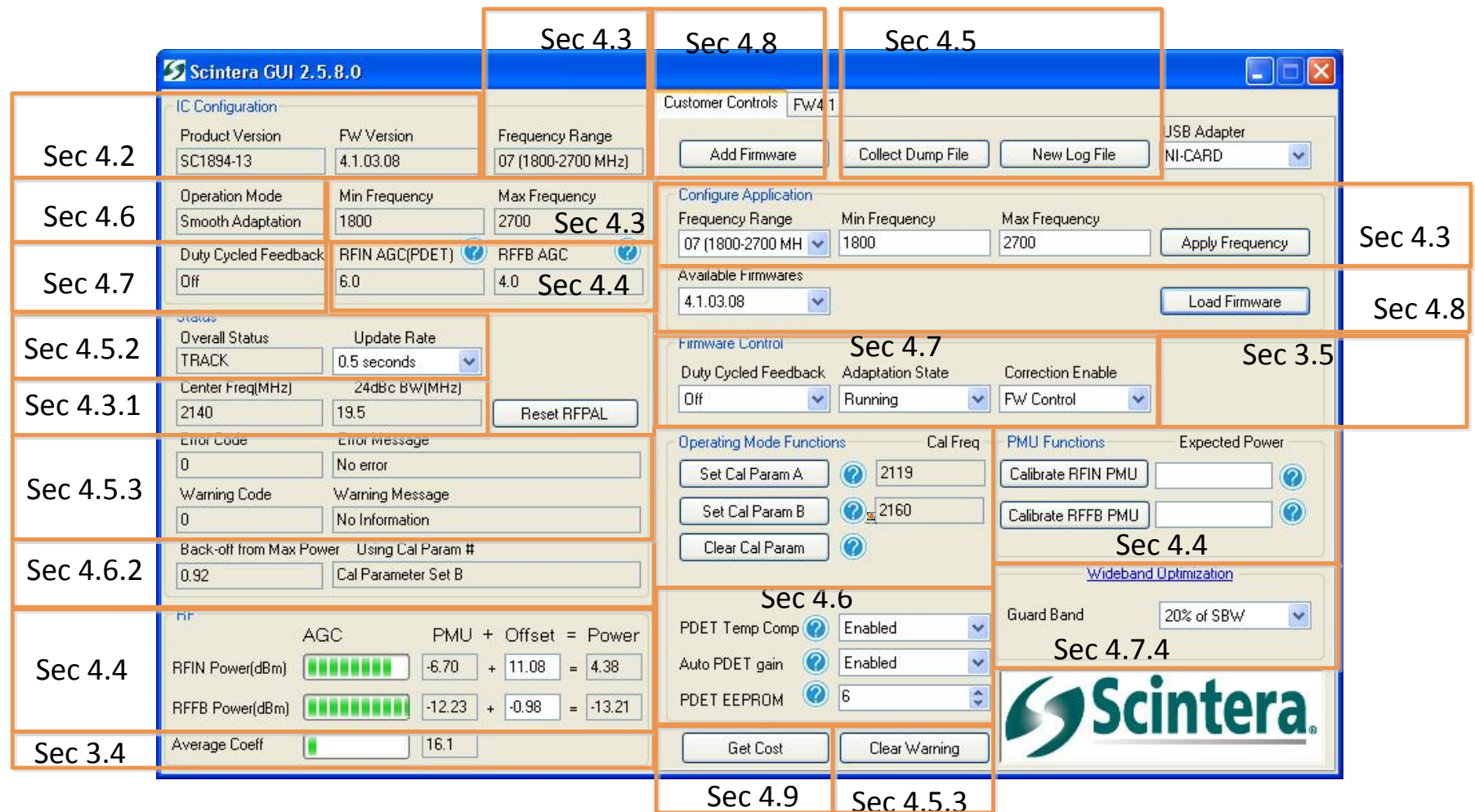


Figure 8. SC1894 Main GUI window annotated with reference sections.

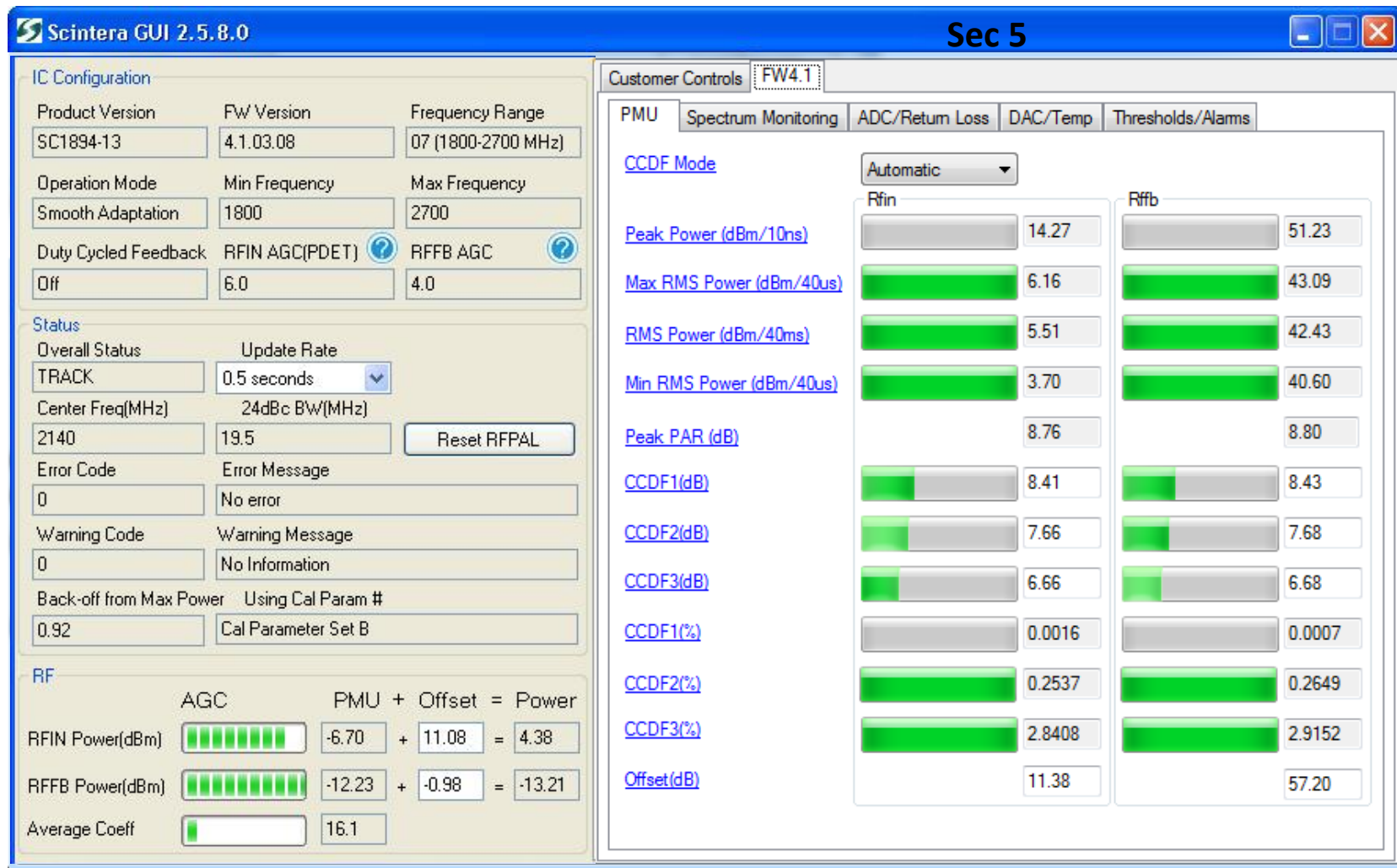


Figure 9. SC1894 PMU window.

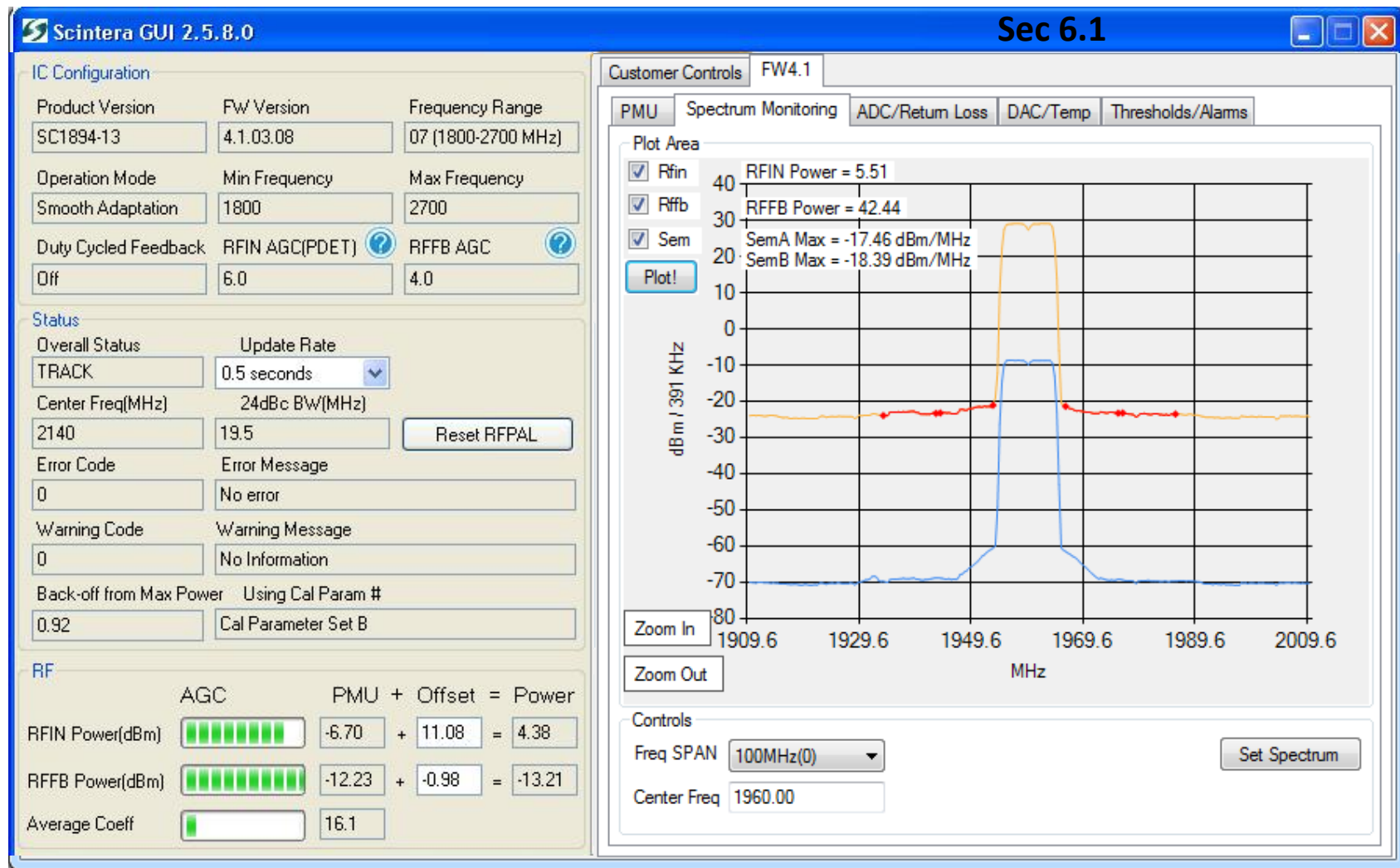


Figure 10. SC1894 Spectrum Monitoring tab.

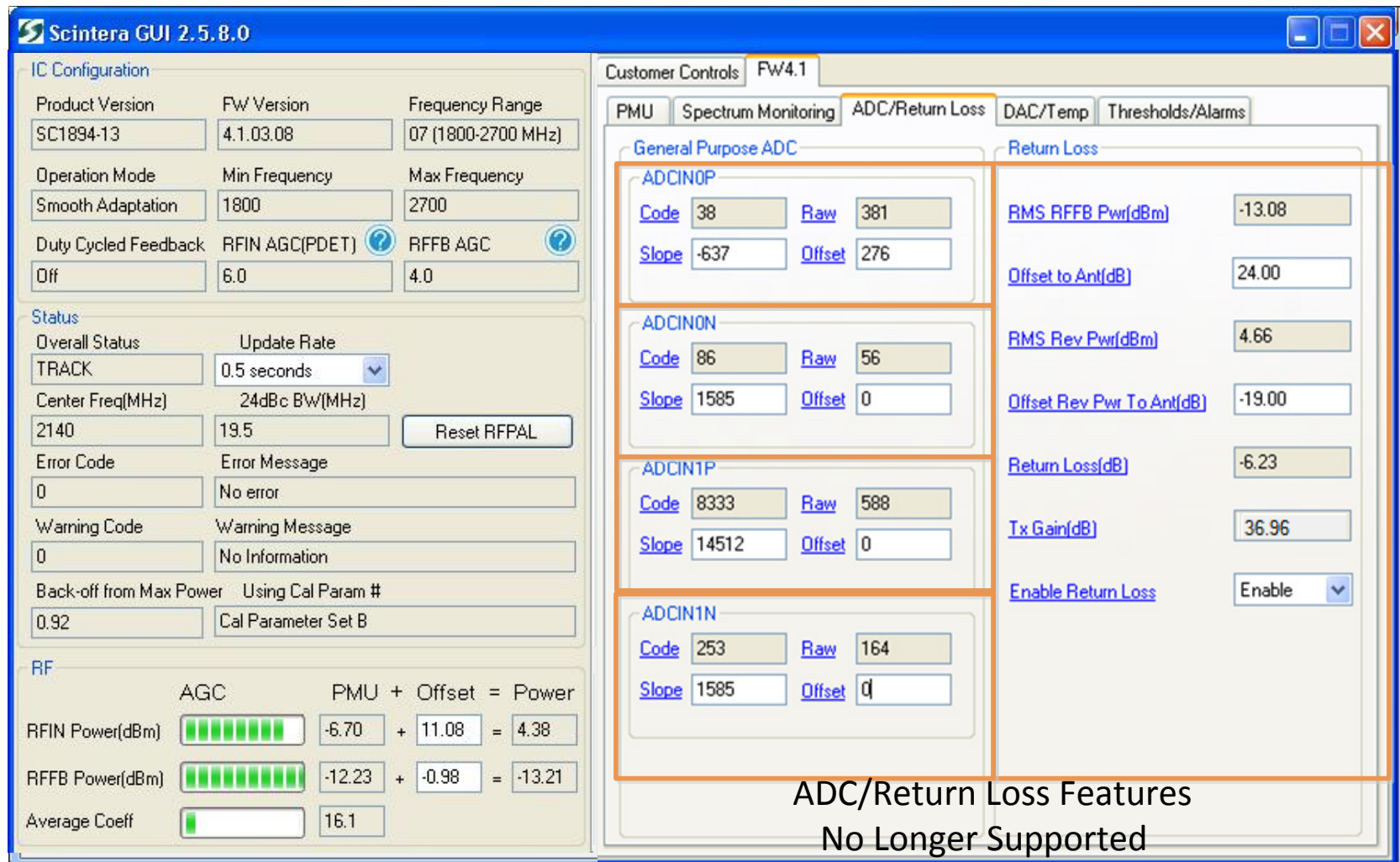


Figure 11. SC1894 ADC/Return Loss window annotated with reference sections.

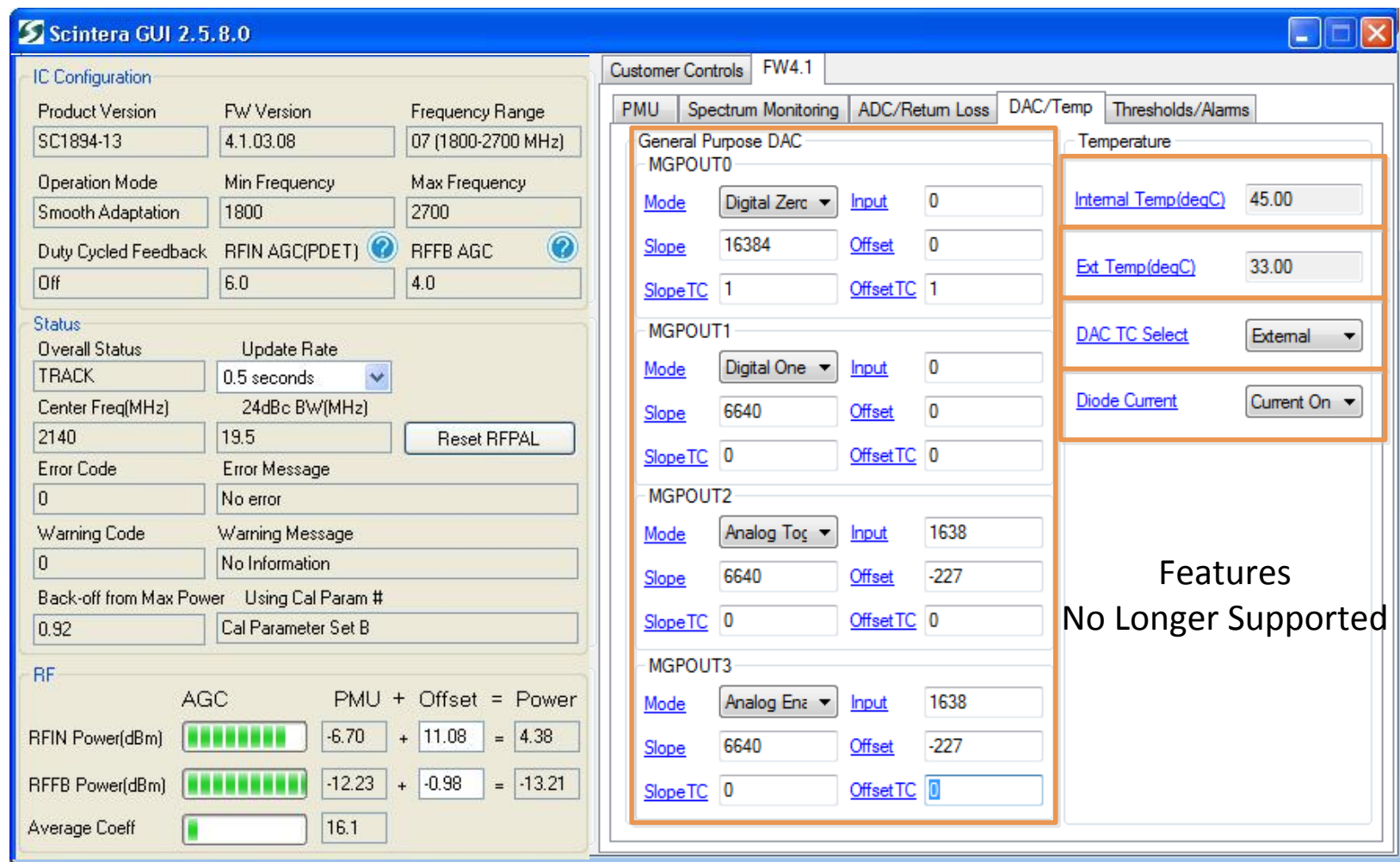


Figure 12. SC1894 DAC/Temp window annotated with reference sections.

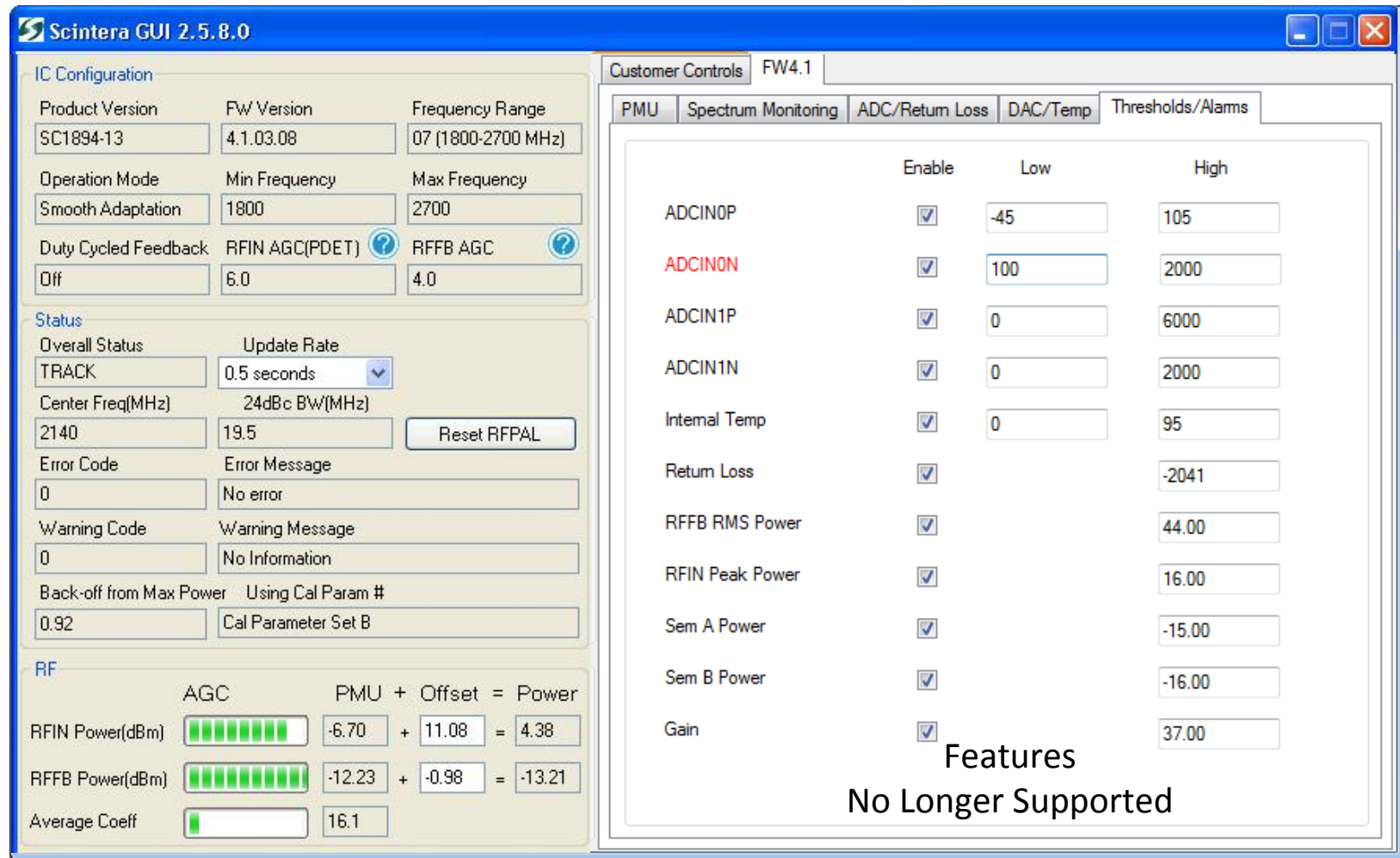


Figure 13. SC1894 Thresholds/Alarms window annotated with reference sections.

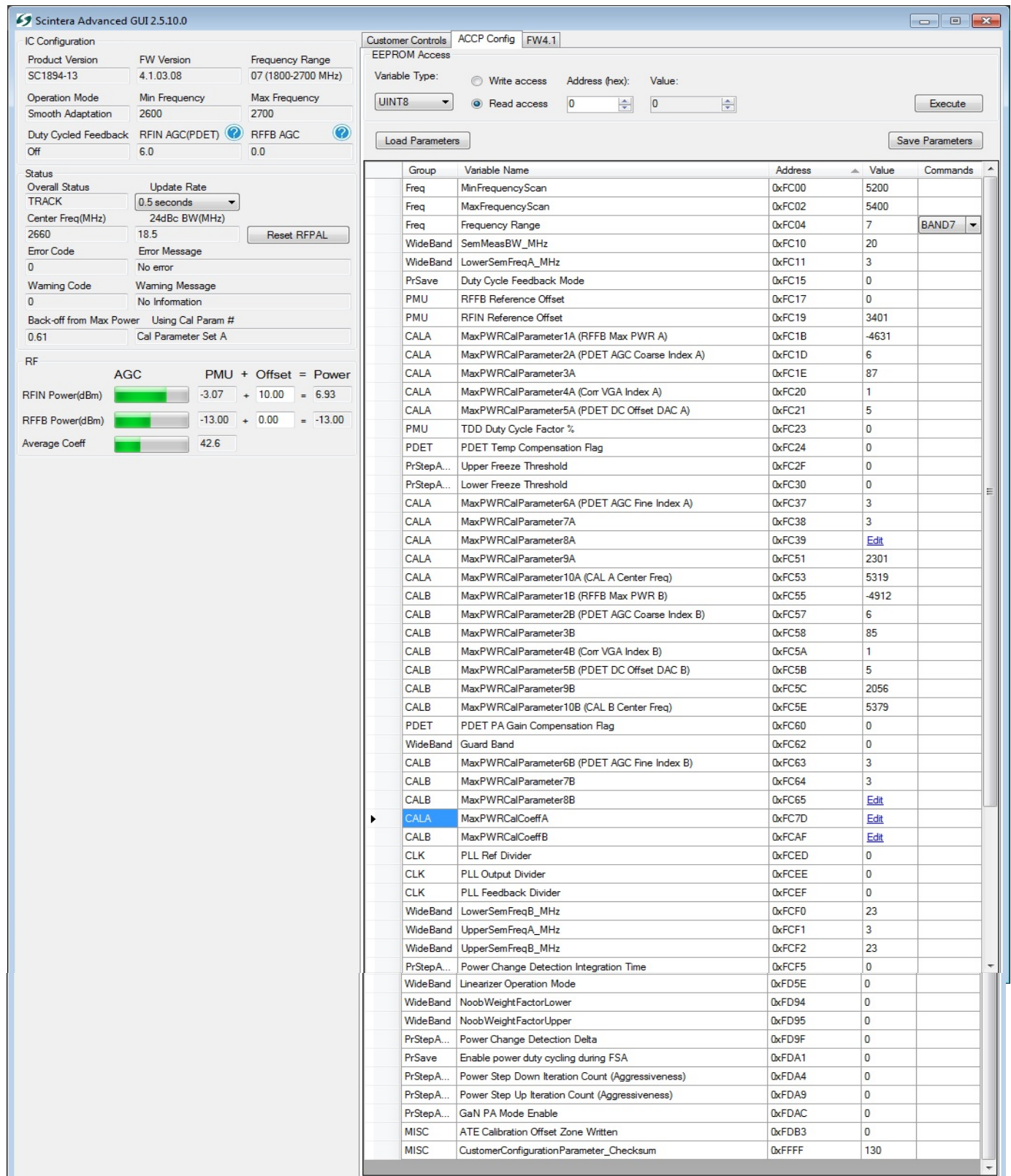


Figure 14. SC1894 advanced GUI.

5.2. IC Configuration

The IC Information indicates the hardware status as well as the setting of user parameters available in the EEPROM.

The firmware version loaded on the SC1894 can be read using the Scintera GUI. See section 4.8 to change the firmware.

5.3. Frequency Range, Min Frequency, Max Frequency, Center Frequency, and Bandwidth

5.3.1. Frequency Range

The SC1894 supports operation from 225MHz to 3800MHz divided in multiple ranges. The SC1894 only scans for the input frequency within the band that is selected. The range is an EEPROM parameter and can be read from the GUI over the SPI interface. The following ranges are supported:

Table 6. SC1894 Frequency Ranges

Frequency Range	Guaranteed Frequency Ranges GUI Frequency Pulldown Options ¹		Available Frequency Ranges for Testing	
Range	Min Freq	Max Freq	Min Freq	Max
01	225	260	130	260
02	260	520	260	520
03 ²	225	960	130	1040
04	520	1040	520	1040
05	1040	2080	1040	2080
06 ²	698	2700	520	3049
07	1800	2700	1616	3049
08	2700	3500	2666	4500
09	3300	3800	3191	4500

1. Operation outside the Guaranteed Frequency Ranges is not guaranteed.
2. For stitched range 03 and 06, it is recommended to limit the frequency range needed for the application due to spurious considerations.

5.3.2. Changing Frequency Range

The frequency range of the SC1894 can be changed using the SPI. This change is written to the internal EEPROM, so that it only needs to be done once to reconfigure the SC1894 to operate in a new band. There is no limit to the number of times the SC1894 can be configured to a new frequency range.

You should be sure that your scanning range matches the design frequency of your board or evaluation kit.

5.3.3. Min Frequency and Max Frequency

The Frequency Scanning Bounds define the frequency range over which the SC1894 scans for the RF signal on RFIN and RFFB. Min frequency (MHz) and max frequency (MHz) are the EEPROM parameters that define the scanning bounds. The current settings for these values can be read over the SPI. The GUI displays these values in the Status box.

5.3.4. Changing Min Frequency and Max Frequency

The min frequency is the lowest frequency that the SC1894 scans when searching for the signal center frequency and max frequency is the highest frequency that the SC1894 scans when searching for the signal center frequency. It is good practice to set the min frequency and the max frequency to the actual values required for the operating range of the application. Setting an unnecessary wide range can lead to intermittent spurs in the band of interest.

Setting the min frequency and max frequency writes the values to the internal EEPROM and it is only required to set them once. There is no limit to the number of times these parameters can be configured.

The default frequency scanning bounds for each range are the guaranteed frequency ranges as defined in **Table 6**. This table also shows the available frequency ranges that can be used to extend these ranges for test purpose.

5.3.5. Center Frequency and Bandwidth

Once the SC1894 exits the CAL state, the detected signal center frequency ($\pm 0.5\text{MHz}$) and -24dBc signal bandwidth ($\pm 0.75\text{MHz}$ for $\text{BW} < 5\text{MHz}$, $\pm 1.5\text{MHz}$ for $\text{BW} \geq 5\text{MHz}$) may be obtained from the GUI. The SC1894 considers signals within this displayed bandwidth as “in band” and does not include this signal power as distortion to be corrected.

If the distortion products of your amplifier are above -24dBc , the SC1894 may consider them as signal and not operate properly.

The SC1894 does not attempt to correct signals that are less than 1MHz of modulated signal bandwidth.

The maximum signal bandwidth is 75MHz .

If the detected signal bandwidth does not reflect system or test equipment settings, it may indicate that the SC1894 is not operating under the correct conditions.

5.4. *RFIN and RFFB AGC Sliders*

The RFIN AGC (PDET) parameter is an attenuator in an AGC loop within the SC1894 analog circuitry. This RFIN AGC loop ensures that the peak voltage into the correction block stays within the desired range across RFIN level and temperature. In Optimized Correction mode, the RFIN AGC (PDET) index is determined during the PDET state between CAL and FSA. The RFIN AGC (PDET) index is an integer value between 0 and 15. At room temperature, when the PA operates at maximum output power, the RFIN AGC (PDET) index must be within 8 and 1. This needs to be taken into account as well for smooth adaptation calibration. The calibrated RFIN AGC (PDET) value must be within 8 and 1, and ideally around to 6-7.

- At maximum PA output power, if RFIN AGC (PDET) > 8, then RFIN is too high and needs to be lowered.
- At maximum PA output power, if RFIN AGC (PDET) < 1, then RFIN is too low and needs to be increased.

Over temperature, the PA gain and SC1894 internal gain varies. To compensate for the PA gain variations, the PA AGC loop external to SC1894 adjusts the RFIN level to maintain a constant PA output power. If the RFIN level increases, the optimal PDET index needs to increase as well. Similarly, as temperature changes affect the SC1894 internal gain, the PDET index adjusts to maintain optimal signal levels within the SC1894. These PDET index adjustments create a short ACLR degradation. For some applications, these temporary degradations in ACLR correction might not be acceptable and it is possible to disable the PDET index compensation over temperature variations by setting both the “PDET Temperature Compensation Flag” and PA Gain Compensation Flag to ‘1.’ This holds the calibrated PDET value constant over all conditions. The tradeoff is that the correction performance may degrade slightly at extreme temperatures. This potential degradation is a function of the PA’s gain and P1dB overtemperature within the temperature range required (see [4] for configuration details).

The RFFB AGC is an AGC loop within the SC1894 used to hold the RFFB signal to the optimum level. The higher the RFFB power level, the lower the RFFB AGC value. The RFFB AGC value should be between 4 and 12 at room temperature, when the PA operates at maximum power.

- At maximum PA output power, if RFFB AGC > 12, then RFFB is too low and needs to be increased
- At maximum PA output power, if RFFB AGC < 4, then RFFB is too high and needs to be lowered

However, the RFIN/RFFB power level limits stipulated in the [SC1894 data sheet](#) must be met.

5.5. *Firmware Status*

The SC1894 supports various status commands from the GUI to aid during development and monitor the SC1894 status during operation. It is recommended that the GUI be used to monitor the SC1894 status during development.

The GUI displays the SC1894 status. The rate at which the GUI is updated is shown in Status - Update Rate. It is configurable and is set to be 0.5 seconds by default. It is possible to disable the GUI refresh and to only update the GUI with the “Force Update” button.

5.5.1. Overall Status

The state of the correction processor can be read using the SPI and is displayed on the GUI. These are important indicators to determine if the SC1894 is operating as intended. The GUI displays these states.

5.5.2. Firmware States

INIT

- Initialize microprocessor
- Initialize all internal data memories
- Load configuration parameters from EEPROM

CAL

- Calibrate internal VCO/PLL and internal gain levels
- Adaptation engine is scanning to find the carrier center frequency and bandwidth. If the average RFIN and RFFB levels are within the specified dynamic range (see section 3.1) then the SC1894 completes CAL and begins optimizing gain settings (PDET).
- Perform initial adaptation

PDET

- Optimize gain settings

FSA

- Full speed adaptation to converge quickly to initial pre-distortion solution.
- SC1894 rapidly adapts the coefficients with a large step size to converge to an ACLR close to the final one as fast as possible. RFFB is used to measure and minimize the system's out-of-band distortion.
- Large changes in the ACLR may occur as the optimum values are found.
- PMU measurement values are available.

TRACK

- Firmware has converged to the best possible predistortion solution
- Slow-rate adaptation to account for small changes over power, temperature and voltage.
- Monitor feedback signal for average power changes and adjust adaptation parameters appropriately.
- Monitor feedback signal for center frequency, bandwidth or carrier configuration changes and adjust predistortion parameters appropriately. SC1894 reliably detects center frequency changes $\leq 40\text{MHz}$.
- PMU measurement values are available.

5.5.3. Firmware Boot Procedure Change Diagram

Figure 15 illustrates the difference in firmware boot procedures between 4.1.01.01 and 4.1.03.08

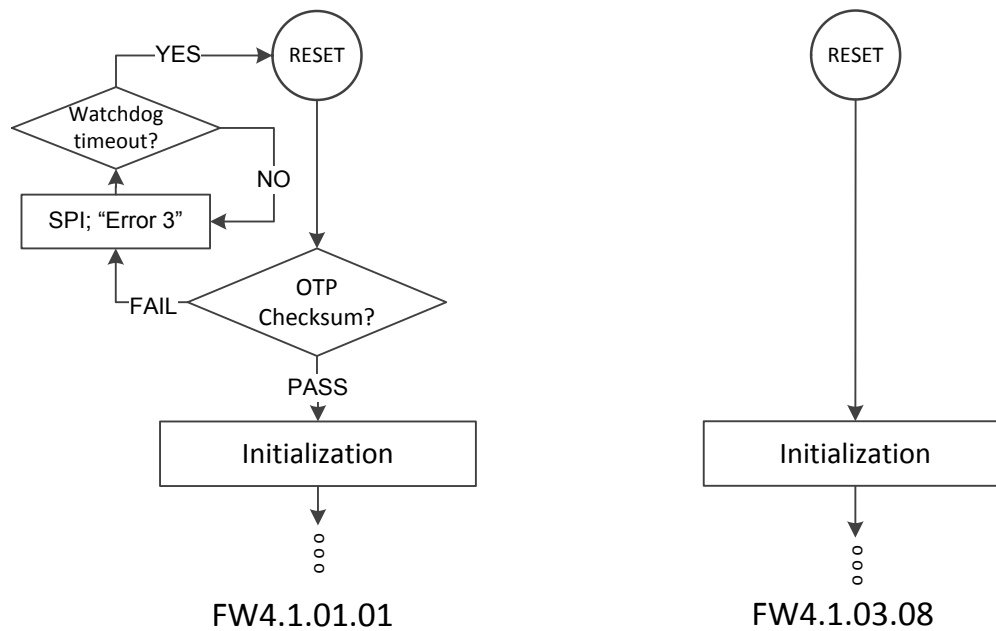


Figure 15. Comparison of firmware OTP check behaviors.

5.5.4. Error/Warning Codes

The SC1894 provides warning or error codes if these registers are polled over the SPI. Warnings do not interrupt the operation of the IC although a warning typically indicates that optimal performance is not being obtained. Errors indicate that the SC1894 resets itself to clear an error condition.

Different Error and Warning Codes are described in **Table 7** and **Table 8**.

Table 7. Error Codes

Error Code	Meaning
0	No Error
3	“EEPROM corrupted” Improper use of the part resulted in EEPROM corruption. Downloading the firmware again using the Scintera GUI might fix this error. If not, contact the Maxim Technical support team.
5	“Center Frequency outside the Defined Frequency Range” Center Frequency is outside the min and max frequency range. Modify the min and max frequency range to fix this error.
13	“Wrong CLK Setting” Clock rate doesn’t correspond to the external clock configuration EEPROM parameters. Refer to SPI Programming Guide [4] for more details.
Others	“Internal Chip Error” Contact the Maxim Technical support team if you get any other error that doesn’t get fixed after reset or downloading the firmware again using the Scintera GUI.

Table 8. Warning Codes

Warning Code	Meaning
0	No Warning
44/48	“Center Frequency Too Low” This warning should not happen for customers using the GUI but could happen for a customer using a host to control SC1894. This indicates that the device is operating outside the recommended frequency ranges defined in Table 6.
50	“DAC Code Value Out of Range” Slope and Offset need to be adjusted.
62	“IC Temperature Outside Allowed Range” Check ATE Calibration Offset Zone Written flag (0xFDB3) and set to “0.” Refer to SPI Programming Guide [4] for details.
Others	“Internal Warning” Contact the Maxim Technical support team for further information.

When the firmware issues a warning, the GUI won’t clear that warning until the “Clear Warning” button is pressed, even if the warning is no longer applicable. So after a warning is reported, it is recommended to clear it.

5.5.5. GUI Log Files

The GUI allows the Error and Warning codes to be logged; each time the GUI is started an "Error/Warning" log file is created.

For Windows XP®, it is created with a unique name based on its originating name:

C:\Documents and Settings\All Users\Application Data\Scintera\ScinteraGUI\Log

For Windows 7, the log file is created under:

C:\ProgramData\Scintera\ScinteraGUI\Log

Note that with Windows 7, ProgramData directory is hidden by default. To make it visible, open Windows Explorer and select the C: drive. Press "Alt," select tools, and then "Folder Options" to select "Show hidden files, folders, and drivers to display it." Hit "Apply" or "OK."

The format is: etrace20110517_182622.csv indicating date and time of the log file start.

The first eight characters are date in yyyymmdd format (May 17 2011 in this case) and the last six digits are time of day in 24-hour hhmmss format (6PM 26minutes and 22s in this case).

All errors and warning are captured in this log file. The New Log File button allows starting a new log file without having to close the GUI.

5.5.6. GUI Collect Dump

This opens a file explorer window to designate the path to where the Dump Files are created and saved.

By default, for Windows XP, it is saved under:

C:\Documents and Settings\All Users\Application Data\Scintera\ScinteraGUI

By default, for Windows 7, the log file is created under:

C:\ProgramData\Scintera\ScinteraGUI

The Dump File .scidmp contains important variables and state information used for factory troubleshooting/debugging. This is only available using the GUI.

5.5.7. Reset

The SC1894 supports a hardware reset pin as outlined in the hardware design guide. The HW reset is implemented on the evaluation kit as a push button as show in Figure 1. There is a GUI command button which is equivalent to the HW reset. When using the GUI, it is not recommended to use the pushbutton reset on the PCB.

5.6. Operation Modes

The firmware supports two user-selectable operating modes: Optimized Correction Mode and Smooth Adaptation Mode. While it is strongly recommended to use smooth adaptation, the user should determine which mode to use based upon the system performance and evaluation criteria.

The SPI interface is used to read the calibration parameters to determine what operating mode the SC1894 is in. The GUI does this periodically and displays the operating mode in the Status box.

5.6.1. Optimized Correction Mode

This is the default mode of operation and mostly used during initial evaluation of a system. It can be useful to determine the best possible performance achievable under a given set of conditions, but the dynamic performance is very poor. Only Smooth Adaptation Mode should be used for systems deployed in the field. Optimized Correction Mode is mostly used just for experimental purposes or performing the factory calibration in order to enable Smooth Adaptation Mode. This mode sets the adaptation parameters to achieve the best ACLR cancellation at all power levels once reconvergence is achieved. Readaptation is triggered whenever the average power level or signal bandwidth is changed over a 50ms period. The readaptation appears noisy and exhibits rapid changes in ACLR until the device completes reconvergences.

5.6.2. Smooth Adaptation Mode

Smooth Adaptation Mode fixes certain adaptation parameters to speed up the reconvergence resulting in less ACLR degradation under dynamic signal conditions. Operation in this mode requires an initial factory calibration of the SC1894 with the Power Amplifier system. Smooth adaptation mode may result in slightly degraded performance in backoff when compared with Optimized Correction Mode. At maximum power, there is no difference in correction performance between Smooth Adaptation Mode and Optimized Correction Mode. See section 4.6.2.1 for detailed calibration procedure.

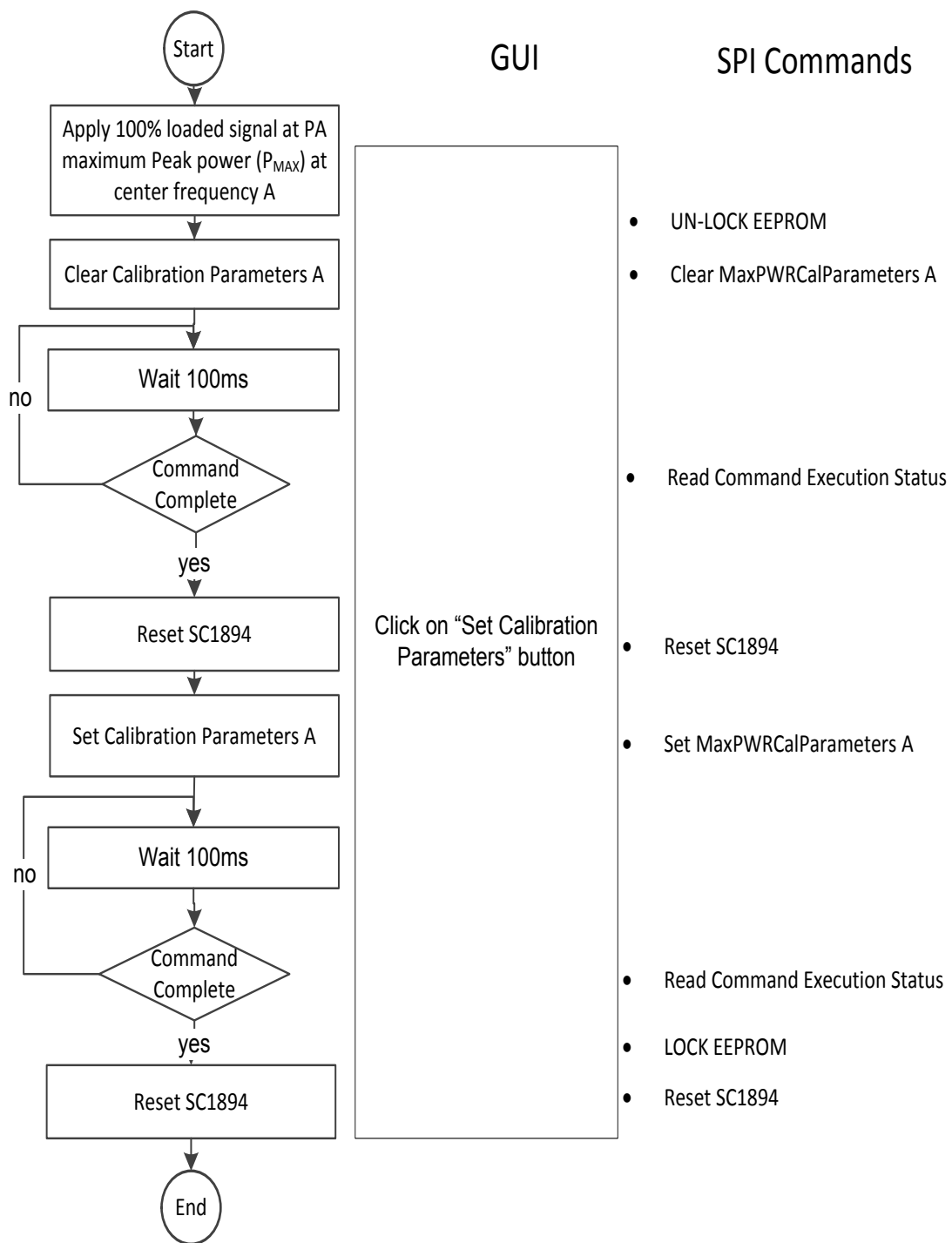


Figure 16. Smooth Adaptation Calibration procedure at center frequency A.

IMPORTANT: Smooth Adaptation Calibration has to be done with the system at maximum peak PA output power with minimum PAR (for Maximum RMS power) and maximum expected signal bandwidth.

5.6.2.1. Calibration – Selecting Smooth Adaptation Mode

Smooth adaptation calibration is required during manufacturing. It is possible to calibrate at either one or two center frequencies. With the system at least at constant, maximum peak output power in operation (or even 0.5dB higher) and the maximum signal bandwidth, the SC1894 adapts and the calibration parameters are stored in the EEPROM. A signal with 100% resource block (RB) utilization should be used; the PAR being around 7dB. For TDD systems; it is recommended to use 100% RB utilization during the TX ON period.

The GUI enables the user to perform this calibration with a single push of the “Set Calibration Parameters” button. When pressing the button “Set Calibration Parameters”, the GUI automatically executes all the SPI commands described in **Figure 16**.

To enable this Smooth Adaptation Mode from a host, the host firmware needs to follow the same steps. See the SPI Programming Guide [4]

When pressing the button “Set Calibration Parameters”, the GUI first Un-Lock the EEPROM and then sends a “Clear MaxPWRCalParameters A” message communication command to SC1894. Then the GUI reads the execution status of the command to confirm that the firmware has executed this command and cleared all the Maximum Power Calibration Parameters. After getting confirmation that the command has been completed, then the GUI resets the SC1894.

After Reset, the GUI waits one second and issues a “Set MaxPWRCalParameters A” message communication command to SC1894. Then the firmware automatically stores all the Maximum Power Calibration Parameters, coefficients and checksum to the customer configuration parameter zone in the EEPROM.

Once the firmware has completed this command, it sends back a message to confirm that the command has been completed. As a last step, the GUI resets the SC1894 to boot up in Smooth adaptation mode.

Once this procedure is done, the SC1894 at power up or reset always operates in Smooth Adaptation Mode unless the calibration parameters are cleared. The calibration is specific to the system so if the PA or other components in the system change, the SC1894 should be re-calibrated. If the maximum operating power is changed, the procedure should also be re-done.

When this mode is enabled, the GUI displays the difference between the calibrated power and the current power: Backoff from Calibrated Max Power.

With two frequency calibrations, the smooth adaptation calibration parameters corresponding to the closer calibration frequency is chosen at a given frequency. The threshold for deciding which frequency to use is the midpoint of the two calibration frequencies. For example, with calibration at 3800MHz and 3700MHz and a center frequency of 3760MHz, the parameters from the calibration at 3800MHz is selected. See the SPI Programming Guide [4] for details.

5.6.2.2. Clearing Calibration Parameters

Clearing the calibration parameters puts the SC1894 into the default Optimized Correction Mode. It is important to clear all of the calibration parameters. The GUI enables the user to clear these parameters with a single push of the “Clear Calibration Parameters” button. The host needs to first unlock the EEPROM and then send a simple “Clear MaxPWRCalParameters A” message to SC1894 to clear all the Maximum Power Calibration Parameters.

5.7. Adaptation and Correction Options

5.7.1. Duty-Cycled Feedback

This is an EEPROM parameter. Duty cycling of the feedback receiver and adaptation circuitry offers the benefit of reduced average power consumption. The feedback receiver and adaptation are duty cycled as soon as adaptation starts after calibration completes. This can significantly slow down convergence; alternatively, the firmware can be configured to only duty cycle once it reaches TRACK state. Refer to [4] for the details. By default, Duty-Cycled Feedback is disabled.

When Duty Cycle Feedback is “Off”:

- This is the default mode.
- SC1894 continuously adapts coefficients and monitors RFFB.
- In this mode, the coefficients also continuously adapt with 100% duty cycle.

When Duty Cycle Feedback is “On”:

- Once it is “On” the device comes up in this mode on power-up or reset.
- Duty-Cycle period = ON_TIME + OFF_TIME = 100 + 1000 = 1100ms
- During ON_TIME (100ms), SC1894 adapts coefficients and monitors power-level change on RFFB
- During OFF_TIME (1s), the coefficients do not adapt and correction still applies. SC1894 does not monitor RFFB power-level change, center-frequency change or signal-bandwidth change.

5.7.2. Adaptation States

The adaptation engine can be stopped to freeze the current coefficients. This is typically used for debug and lab evaluation purposes only. The last calculated coefficients are applied to the correction signal processor and are not updated.

- Running: Default state. Adaptation mode running as described above.
- Frozen: Freeze coefficient adaptation. All other circuits are left in the state they were in when the freeze command is applied.

5.7.3. Enabling and Disabling Correction

Once in TRACK, it is possible to turn off the predistortion signal. This is set to “FW Control” by default and can be used to toggle between corrected and uncorrected performance of the PA. It is typically used during evaluation and development. It is not recommended to disable SC1894 at low-output powers since the firmware handles this automatically.

Disabled: The predistortion signal is disabled and coefficients are not adapted. All other circuits are left in the state they were in when the disable command was applied.

FW Control: The predistortion signal is enabled.

During other states, this option is disabled since the RFOUT must be under firmware control.

5.7.4. Wideband Performance Optimization

Guard Band is an EEPROM parameter defined as the frequency band between the carrier edge (defined by the -24dBc signal bandwidth) and the IMD measurement region used for adaptation.

By default (value is "0"), the Guard Band is set to 20% of the signal bandwidth. This configuration is for IMD5 performance optimization of contiguous carriers with signal bandwidth greater than 40MHz.

For noncontiguous carriers or for close-in IMD optimization, it is recommended to try different options.

The Guard Band parameter can be configured to 1MHz, 1.5MHz, 2MHz or 2.5MHz.

Note that 1MHz was used in firmware 4.0. From the host, the Guard Band can be configured as any positive multiple of 0.5MHz. See SC1894 SPI programming guide for detail [4].

5.8. Upgrading SC1894 Firmware

The internal EEPROM in the SC1894 supports field upgrades of the firmware. The firmware is upgradeable using the GUI.

5.8.1. GUI function Adding New Firmware to "Available Firmware" list

"Add Firmware" allows adding future firmware to the "Available Firmware" list. A New Firmware version is included in the CD provided with the EV kit board and can easily be added to the "Installed Firmware" list. New firmware versions are provided in encrypted format ".sci."

Click on "Add Firmware" and navigate to the file to be added.

Select the .sci file and click Open. The firmware is added to the available firmware drop down and downloaded to the SC1894 chip.

5.8.2. Change Firmware

To download firmware to SC1894, select one of the "Available Firmware" and click "Change Firmware."

5.9. Cost Function

The cost function is measured at the RFFB input and is a scalar value proportional to ACLR measurement. The magnitude of this scalar depends on the modulation type. Monitoring the relative change of this scalar provides an indication of a given PA's ACLR.

The values reported by the GUI are averaged over 30 measurements.

5.10. Scintera Advanced GUI 2.5.10

As shown in **Figure 14**, the Scintera Advanced GUI 2.5.10 allows one to view and configure the different EEPROM configuration parameters. Refer to the SPI programming guide [4] for detailed descriptions of these different parameters.

6. Power Measurement Unit (PMU) Features

The SC1894 integrates two sets of analog power detectors, analog-to-digital converters and sampling integration. As soon as the SC1894 has detected the signal-center frequency and signal bandwidth, it provides the following precise RFIN and RFFB power measurements using the SPI interface every 300ms:

- RFIN and RFFB Peak Power (dBm/10ns): Highest 10ns average values for both RFIN and RFFB over the 40ms average window.
- RFIN and RFFB RMS Power (dBm/40ms) over a 40ms measurement window.
- RFIN and RFFB Max RMS Power (dBm/40μs). Highest 40μs average values for both RFIN and RFFB over the 40ms average window. This value allows reporting power either during Preamble or during those portions of the waveform where the most user resource blocks are occupied without needing synchronization signals, knowledge of frame boundaries, nor support from the baseband.
- RFIN and RFFB Min RMS Power (dBm/40μs). Lowest 40μs average values for both RFIN and RFFB over the 40ms average window
- Peak PAR(dB) is defined as Peak Power (dBm/10ns) minus RMS Power (dBm/40ms)
- RFIN and RFFB CCDF (%) are the percentage of samples with a power level higher than the three different threshold levels defined by the corresponding CCDF fields (dB). These thresholds are defined as the Peak Par (dB) minus 0.25dB, 1dB and 2db in the automatic mode or could be configured manually by the customer in the manual mode. See section 6.2 for detail.

In order to provide enough integration samples to allow precise measurements of signals with high-peak to average values, the default measurement time for the power detector is set to 40ms.

IMPORTANT: Once SC1894 has detected the signal center frequency and signal bandwidth, then the RFIN values are measured even if the RFFB is off (PA disabled or failed) for more than 40ms.

- a. SC1894 is not adapting the predistortion coefficients during measurement time.*
- b. If the frame length of the waveform is not a multiple of 40ms, or a value that is evenly divisible by 40ms, then the power measurement is done over an incomplete frame length.*

6.1. PMU Calibration

The reference points for the RFIN and RFFB PMU are the inputs of the chip. For precise power measurements, the PMU requires a single-point calibration in manufacturing. The PMU calibration typically consists of setting the PA at maximum output power. An external calibrated power meter is used to read the PA power. The SC1894 is allowed to converge and reach TRACK. The PMU value is then read over the SPI for RFFB and used as the reference point. A similar procedure can be used to calibrate the RFIN value as well. These reference values are then stored in the host and used as an offset to calculate absolute power from the PMU values read from SC1894. See the SPI programming guide for examples and usage. This calibration can be done at the same time as the calibration for Smooth Adaptation Mode if desired.

The GUI enables the customer to display absolute power at outside reference points (typically, the absolute PA output power) by providing a window to enter the value read from the external power meter. This value is then used to calculate the offset, which is applied to the power as measured by the SC1894 and displayed as Ref power. *If the calibration is not done, then the offset in the GUI is preset for the approximate coupler loss and matching circuit loss for both RFIN and RFFB, so the approximate power at the*

board connectors is displayed in Ref as shown above. The GUI calculates the offset when the Expected Power is entered and “Calibrate RFFB PMU” or “Calibrate RFIN PMU” is pushed. Expected power should be the value read from external reference such as calibrated power meter or spectrum analyzer. Alternatively, the offset can be manually entered in the offset window.

$$P [Ref] = P [Chip] + Offset$$

IMPORTANT: RFIN and RFFB power indicators must be calibrated. See Table 2 for SC1894 EV kit RFIN and RFFB offset over frequencies

6.2. TDD Considerations - Operation with <100% duty cycle

The SC1894 PMU operates continuously over the measurement window; it does not discard samples, which may have been taken when the PA is off. This affects the reading for waveforms with less than 100% duty cycle as would be seen in TDD applications. For example, the PMU value read for a 50% PA on time (duty cycle) is 3dB lower than the value with 100% duty cycle. It is straightforward to calculate the PA on time power from the PMU value:

1. For systems with a fixed duty cycle, it is recommended to calibrate the PMU with the procedure above using a waveform with proper Rx/Tx duty cycle. This is the preferred method.
2. For systems with variable Rx/Tx duty cycle, the host controller can be used to scale the measurement value by the duty cycle (D_{CYCLE}) and calibrate the PMU values with a 100% duty cycle. Then the conversion of read PMU values into dBm values are as follow:

$$P_{RFIN} = \frac{RFIN_PMU * 3.01}{1024} + OFFSET_{RFIN} - 10 * \log_{10}(D_{CYCLE})$$

$$P_{RFFB} = \frac{RFFB_PMU * 3.01}{1024} + OFFSET_{RFFB} - 10 * \log_{10}(D_{CYCLE})$$

The duty cycle (D_{CYCLE}) factor doesn't need to be applied to RFIN and RFFB Peak Power (dBm/10ns), RFIN and RFFB Max RMS Power (dBm/40μs), RFIN and RFFB Min RMS Power (dBm/40μs) and Peak PAR(dB).

7. Debug Features

The debug features include the following:

- Spectral Monitoring. See section 6.1 for details.
- Complementary cumulative distribution function (CCDF). See section 6.2 for details.

7.1. Spectrum Monitoring (SEM and PSD)

The spectrum emission mask (SEM) is measured for RFFB signal at the same time as the RFFB PMU values described in section 5. So it is averaged over the same 40ms integration window and updated every 300ms.

The power spectrum density (PSD) plots are only generated when pressing the “Plot!” button on the GUI.

7.1.1. Power Spectrum Density Plot (PSD)

It is possible to select RFIN or RFFB or both and configure the frequency span to plot the (PSD).

IMPORTANT: After selecting the frequency span (MHz), it is required to press “Set Spectrum” for the change to take effect.

Then every time the “Plot!” button is pressed, the selected power-spectrum density plots are captured and displayed.

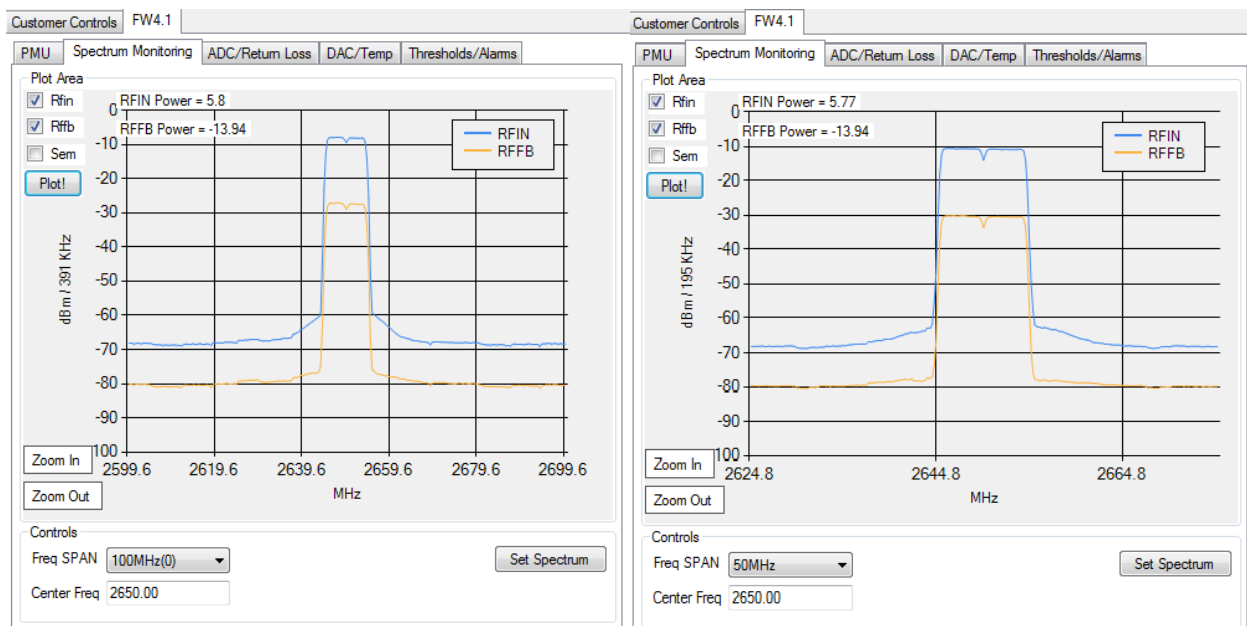


Figure 17. PSD with different frequency span (MHz).

7.1.2. Spectrum Emission Mask (SEM)

IMPORTANT: SEM graph in red is only valid if:

- a. RFFB is selected since SEM is always based on RFFB.*
- b. Center Frequency is not changed.*
- c. Frequency Span set = 100MHz.*

The reported SEM value is always valid and based on a 100MHz sampling rate with detected center frequency independent of the frequency span and center frequency selection.

When selecting RFFB and then SEM, a window opens with the following parameters:

- AccMaxSemRangeA: maximum Spectrum Emission Mask of Lower and Upper SEM bands defined by LowerSemFreqA and UpperSemFreqA over SemMeasBw. Average Lower and Upper SEM values are measured with 1MHz windows averaged over SemMeasBw/2MHz average window. This maximum SEMA value of the Lower and Upper SEM bands A is updated every 300ms.
- AccMaxSemRangeB: maximum spectrum emission mask of lower and upper SEM bands defined by LowerSemFreqB and UpperSemFreqB over SemMeasBw updated every 300ms. Average lower and upper SEM values are measured with 1MHz windows averaged over SemMeasBw/2MHz average window. The maximum value of the lower and upper SEM bands is updated every 300ms. This maximum SEMB value of the lower and upper SEM bands B is updated every 300ms.
- AccSemMaxSemPsdMeas: highest 40μs PSD value in dBm/MHz over 40ms window. Updated every 300ms.
- LowerSemFreqA: 2*LowerOffsetA in MHz from the lower edge of the signal
- UpperSemFreqA: 2*UpperOffsetA in MHz from the upper edge of the signal
- LowerSemFreqB: 2*LowerOffsetB in MHz from the lower edge of the signal
- UpperSemFreqB: 2*UpperOffsetB in MHz from the upper edge of the signal
- SemMeasBw: 2*SEM Measurement Bandwidth in MHz

IMPORTANT: It is recommended to set LowerSemFreqA = UpperSemFreqA and LowerSemFreqB = UpperSemFreqB

Figure 18 and **Figure 19** show two example of SEM setting and the corresponding results with an LTE 10MHz 7.5dB PAR waveform.

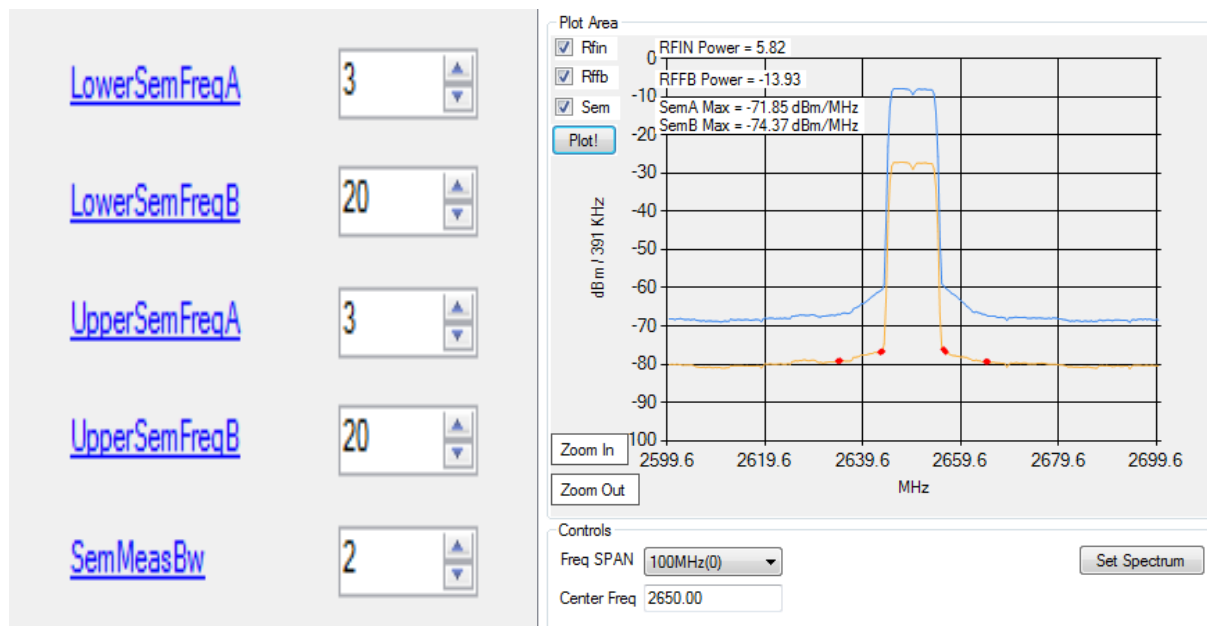


Figure 18. Narrow integration SEM setting.

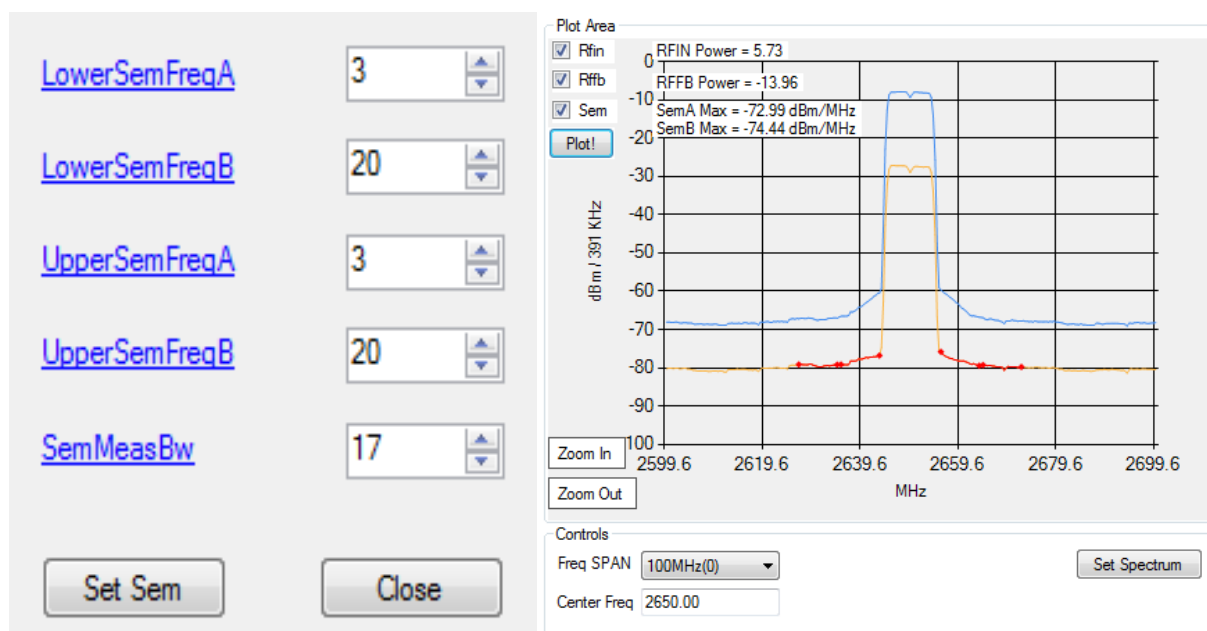


Figure 19. Wide integration SEM setting.

7.2. Complementary Cumulative Distribution Function (CCDF)

SC1894 reports the percentage of points that are over a user-specified threshold. The thresholds are defined as CCDF1 (dB), CCDF2 (dB), and CCDF3 (dB). Three sets of data-pairs are collected for RFIN and RFFB based on the thresholds: CCDF1 (%), CCDF2 (%), and CCDF3 (%). These represent three different points on the CCDF curve. These CCDF (%) are the percentage of samples with power level going above the three different threshold levels defined by CCDF1 (dB), CCDF2 (dB), and CCDF3 (dB).

In automatic mode, these thresholds are respectively defined as CCDF1 (dB) = Peak PAR (dB) - 0.25dB, CCDF2 (dB) = Peak PAR (dB) - 1dB and CCDF3 (dB) = Peak PAR (dB) - 2dB.

In Manual mode, it is required to configure these thresholds as needed after each Reset as these parameters are not saved into the EEPROM.

IMPORTANT: On GUI PMU tab, the Peak PAR (dB) values of RFIN and RFFB should be within 1dB of each other to make sure that the PA is not running too much into compression.

8. SC1894 Performance Data

In the following sections, the plots should be read as follows:

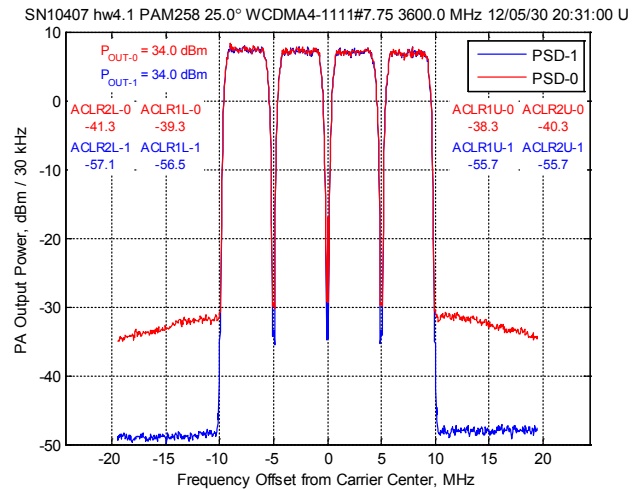
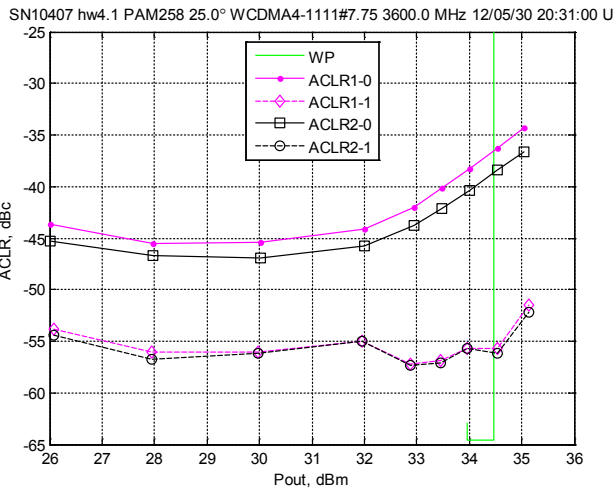
- The green vertical line is $P_{SAT} - PAR$ for the waveform. $P_{SAT} = P_{3dB}$ or 3dB PAR compression point. To be measured with SC1894 with a high PAR waveform (~10dB).
- ACLR/ACPR ending in "-0" (red traces on spectrum plots) are without correction.
- ACLR/ACPR ending in "-1" (blue traces on spectrum plots) are with correction using SC1894.
- FOR WCDMA
 - ACLR1 is the power in a 3.84MHz IBW at a 5MHz offset, relative to the power in the 3.84MHz carrier (for multicarrier signals it is offset from the center of the end carrier).
 - ACLR2 is the power in a 3.84MHz IBW at a 10MHz offset, relative to the power in the 3.84MHz carrier (for multicarrier signals it is offset from the center of the end carrier).
- For CDMA
 - ACPR1 is the power in a 30kHz bandwidth at an 885kHz offset relative to the power in the 1.2288MHz carrier bandwidth.
 - ACPR2 is the power in a 30kHz bandwidth at a 1980kHz offset relative to the power in the 1.2288MHz carrier bandwidth.
- For multicarrier signals, ACLR1L (ACPR1L) is offset from the center of the first carrier, and ACLR1U (ACPR1U) is offset from the center of the last carrier.
- For multicarrier signals, ACLR2L (ACPR2L) is offset from the center of the first carrier, and ACLR2U (ACPR2U) is offset from the center of the last carrier.

8.1. Ampleon Class AB Performance Data at 3.6GHz

- Ampleon BLF6G38-10 class AB, LDMOS
- Frequency range: 3400MHz to 3600MHz
- Frequency of operation: 3600MHz
- Gain: 16dB. P_{SAT} : 42dBm

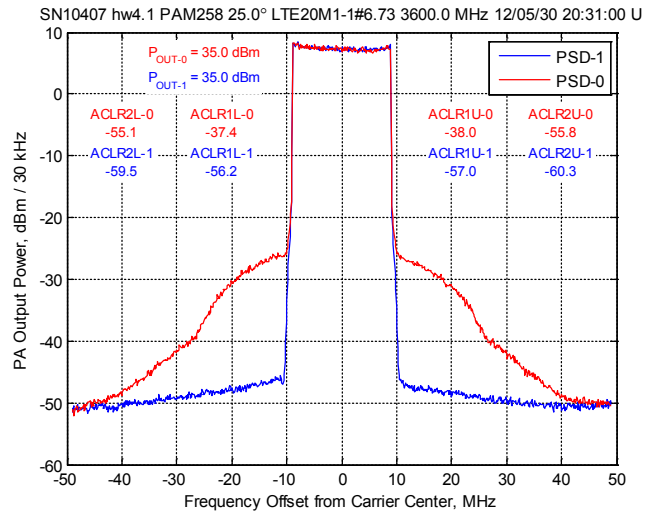
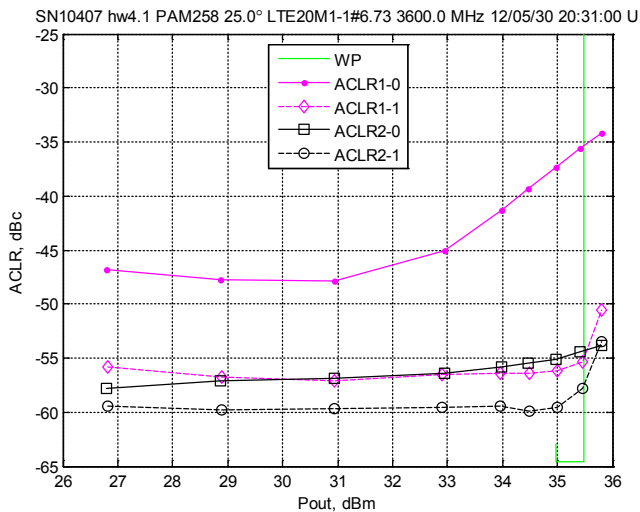
8.1.1. WCDMA 4 Carrier 7.75dB PAR

PA output-power level sweep with NXP BLF6G38-10.



8.1.2. LTE 20MHz E-TM3.1

PA output power level sweep with NXP BLF6G38-10.



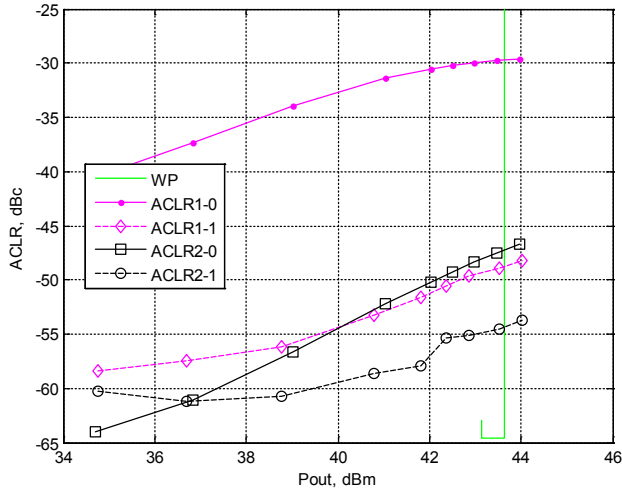
8.2. 2100MHz NXP Doherty, Average Power 20-50W

- NXP 2x MRF8S21100, Doherty PAM, LDMOS
- Optimized for Efficiency.
- Frequency: 2140MHz
- Gain 16dB, Psat ~53.1dBm

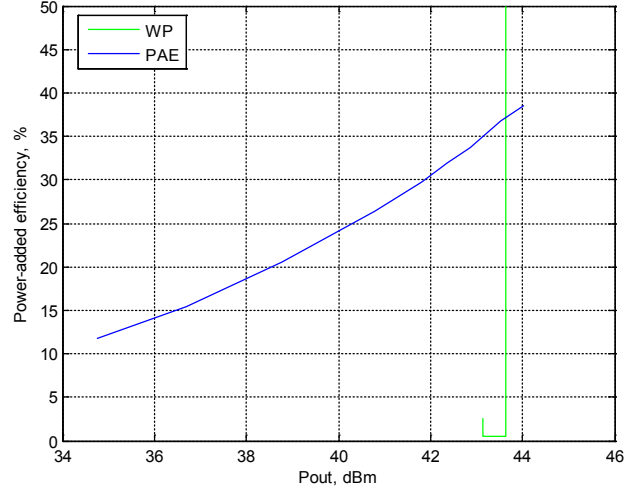
8.2.1. LTE 20MHz E-TM3.1 (9.51dB PAR)

PA output power level sweep with NXP 2xMRF8S21100.

SN10606 hw4.1 PAM114 25.0° 1.80V 3.30V LTE20M1-1#9.51 2140.0 MHz 12/08/22 17:17:22 U

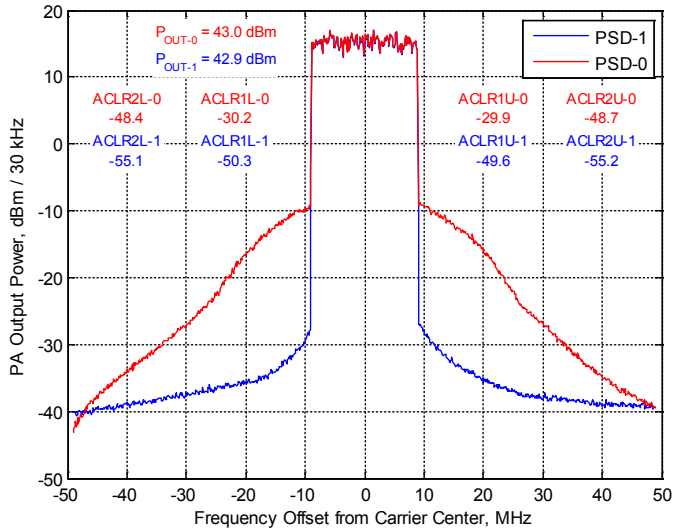


SN10606 hw4.1 PAM114 25.0° 1.80V 3.30V LTE20M1-1#9.51 2140.0 MHz 12/08/22 17:17:22 U



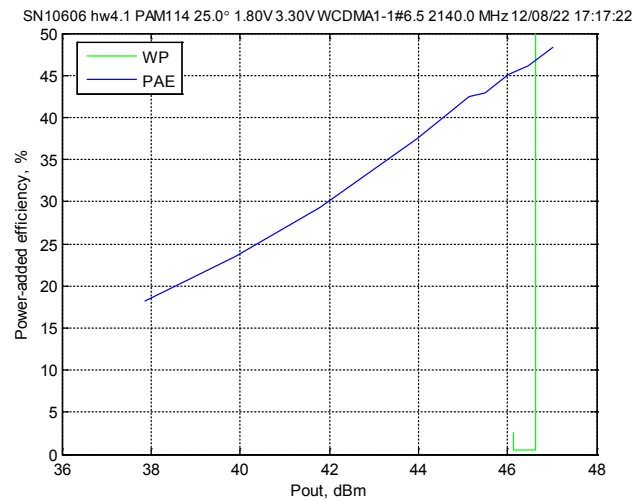
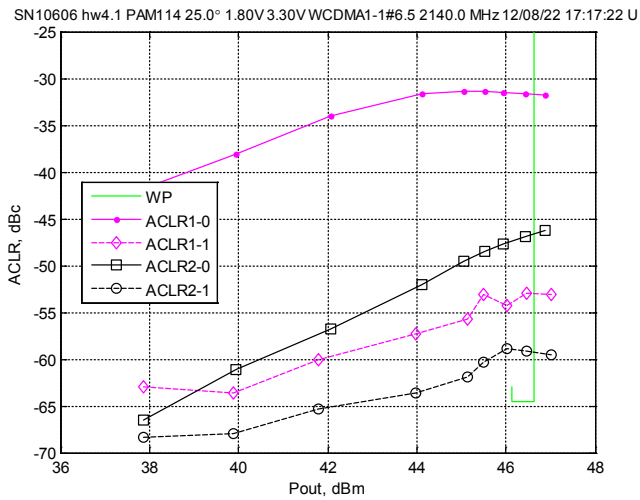
PA Output = 42.9dBm

SN10606 hw4.1 PAM114 25.0° 1.80V 3.30V LTE20M1-1#9.51 2140.0 MHz 12/08/22 17:17:22 U



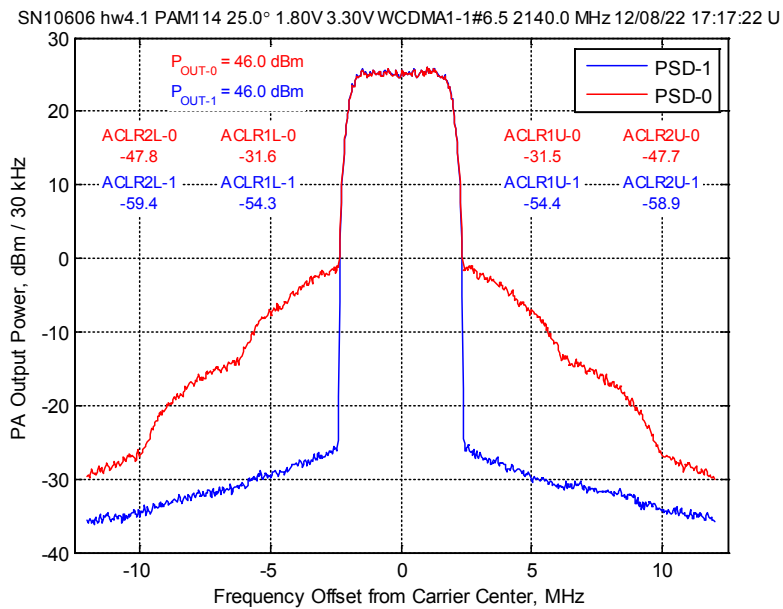
8.2.2. Single Carrier WCDMA PAR = 6.5dB

PA output-power level sweep with NXP 2xMRF8S21100.



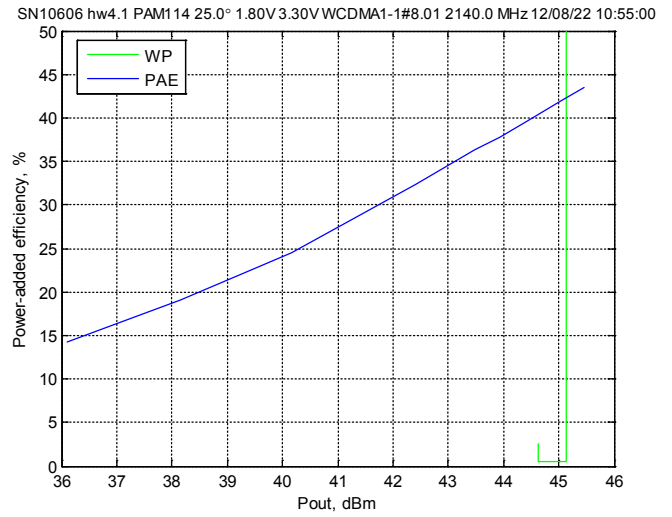
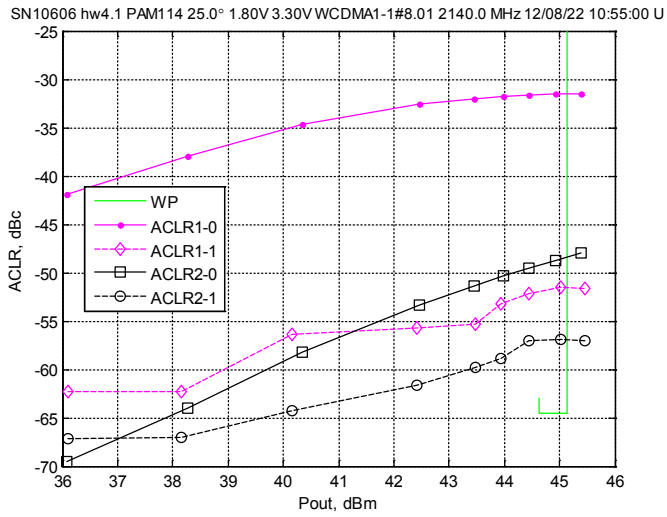
PA Output = 46dBm.

Power Added Efficiency: 45%



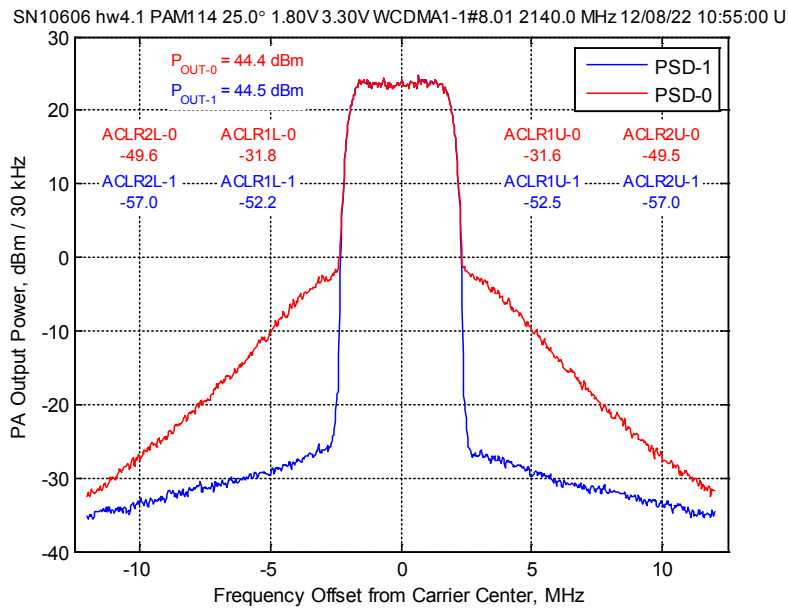
8.2.3. Single Carrier WCDMA PAR = 8dB

PA output-power level sweep with NXP 2xMRF8S21100.



PA Output = 44.5dBm.

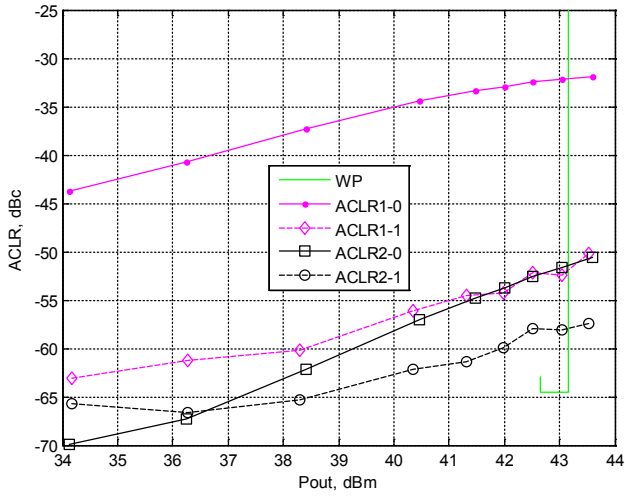
Power Added Efficiency: 40%



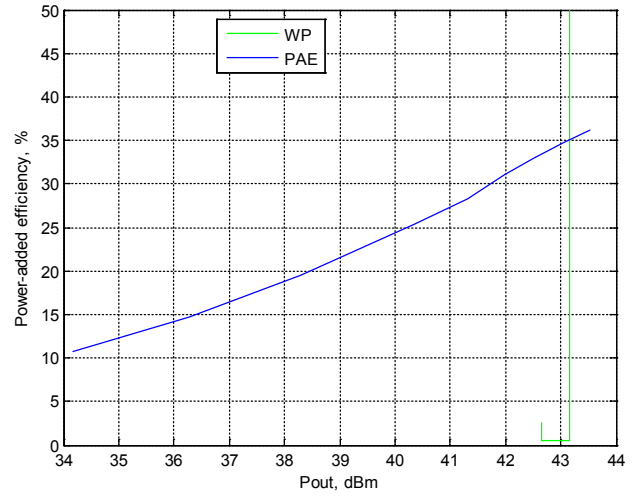
8.2.4. Single Carrier WCDMA TM1 PAR = 9.99dB

PA output-power level sweep with NXP 2xMRF8S21100.

SN10606 hw4.1 PAM114 25.0° 1.80V 3.30V WCDMA1-1#9.99 2140.0 MHz 12/08/22 17:17:22 U



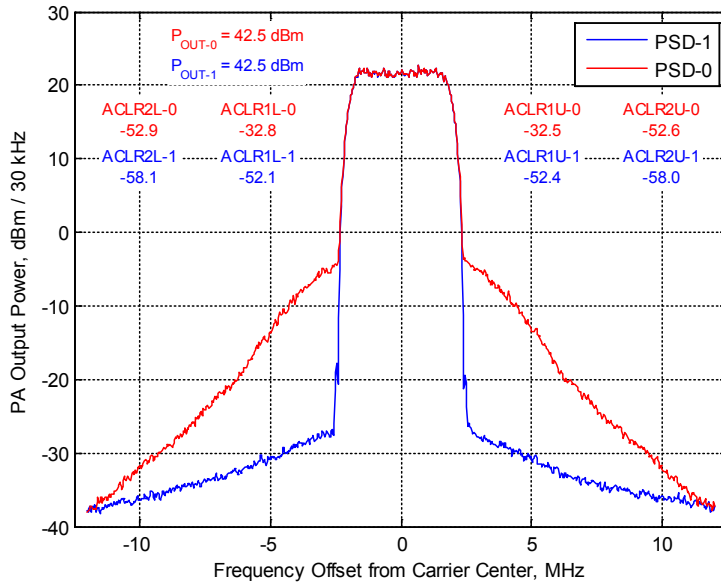
SN10606 hw4.1 PAM114 25.0° 1.80V 3.30V WCDMA1-1#9.99 2140.0 MHz 12/08/22 17:17:22



PA Output = 42.55dBm.

Power Added Efficiency: 33%

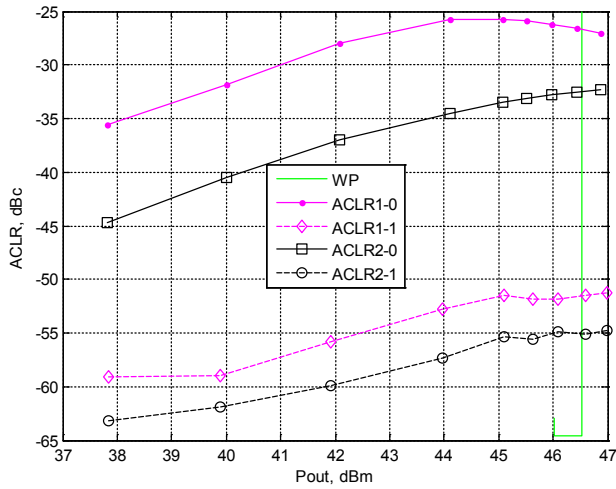
SN10606 hw4.1 PAM114 25.0° 1.80V 3.30V WCDMA1-1#9.99 2140.0 MHz 12/08/22 17:17:22 U



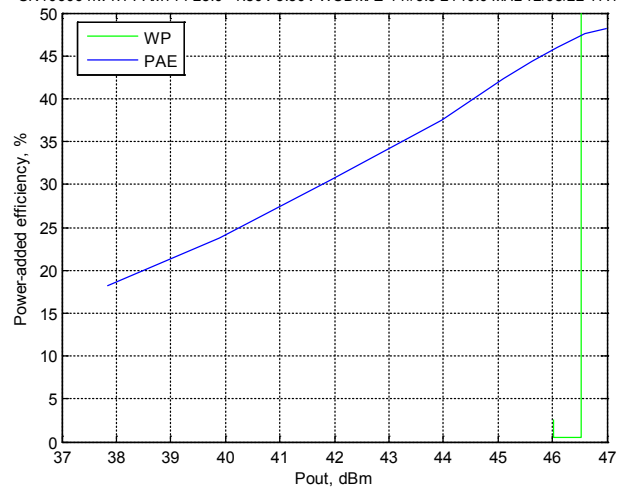
8.2.5. Dual Carrier WCDMA2 PAR = 6.50dB

PA output-power level sweep with NXP 2xMRF8S21100.

SN10606 hw4.1 PAM114 25.0° 1.80V 3.30V WCDMA2-11#6.5 2140.0 MHz 12/08/22 17:17:22 U



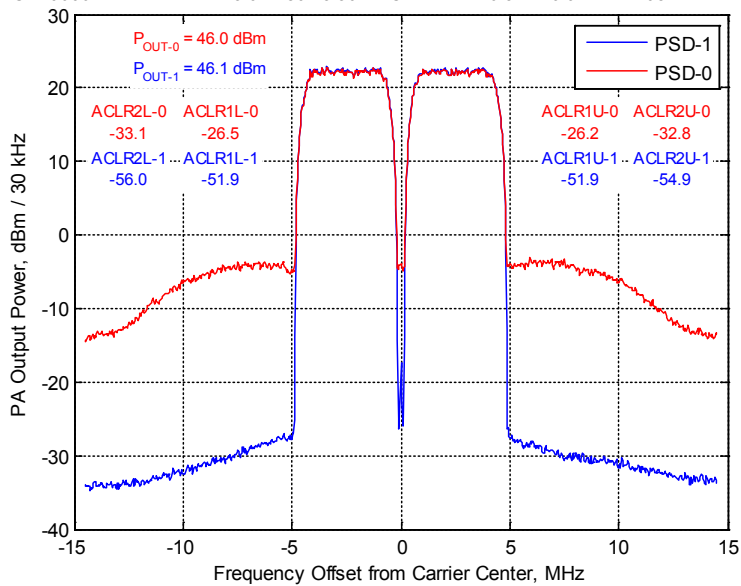
SN10606 hw4.1 PAM114 25.0° 1.80V 3.30V WCDMA2-11#6.5 2140.0 MHz 12/08/22 17:17:22 U



PA Output = 46.1dBm

Power Added Efficiency: 45%

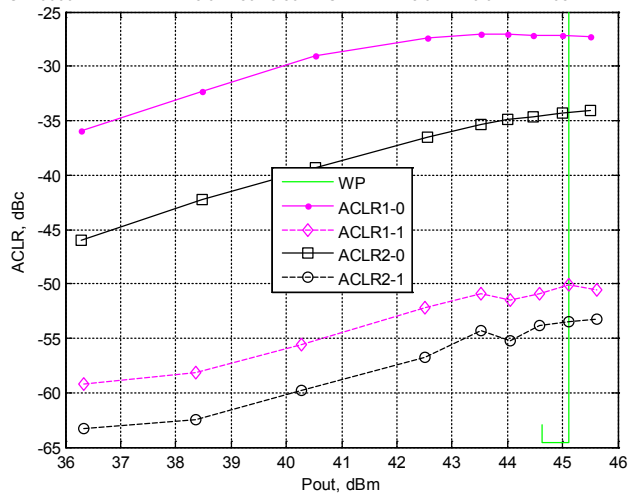
SN10606 hw4.1 PAM114 25.0° 1.80V 3.30V WCDMA2-11#6.5 2140.0 MHz 12/08/22 17:17:22 U



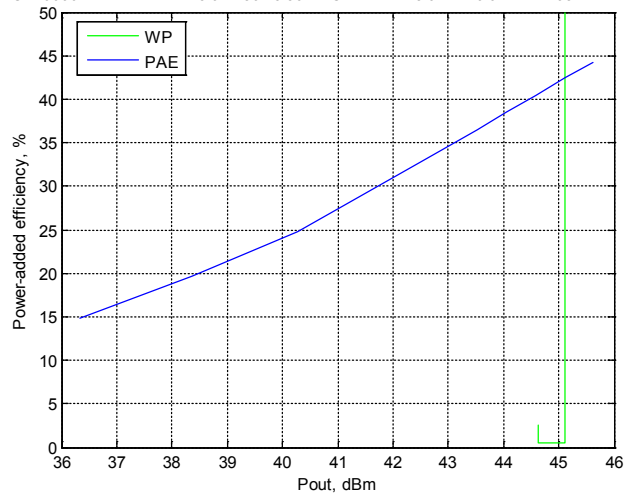
8.2.6. Dual Carriers WCDMA PAR = 8dB

PA output-power level sweep with NXP 2xMRF8S21100.

SN10606 hw4.1 PAM114 25.0° 1.80V 3.30V WCDMA2-11#8.02 2140.0 MHz 12/08/22 17:17:22 U



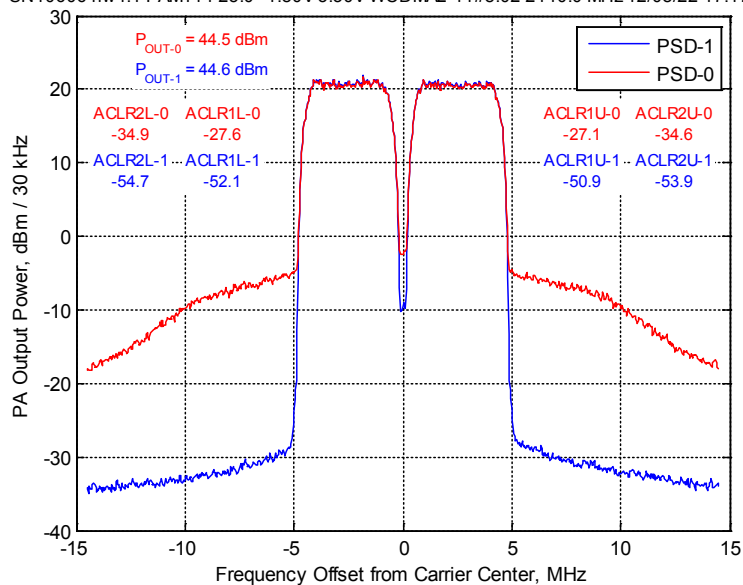
SN10606 hw4.1 PAM114 25.0° 1.80V 3.30V WCDMA2-11#8.02 2140.0 MHz 12/08/22 17:17:22



PA Output = 44.6dBm.

Power Added Efficiency: 40%

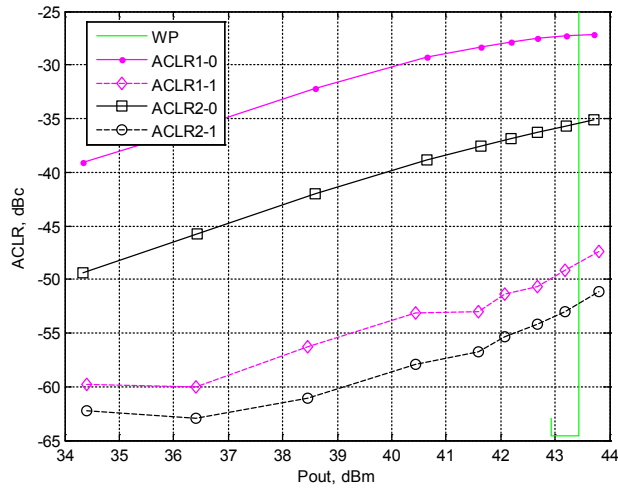
SN10606 hw4.1 PAM114 25.0° 1.80V 3.30V WCDMA2-11#8.02 2140.0 MHz 12/08/22 17:17:22 U



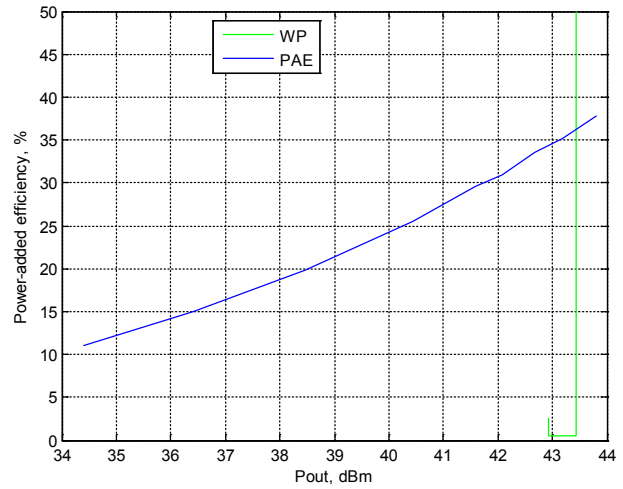
8.2.7. Dual Carriers WCDMA TM1 PAR = 9.70dB

PA output-power level sweep with NXP 2xMRF8S21100.

SN10606 hw4.1 PAM114 25.0° 1.80V 3.30V WCDMA2-11#9.70 2140.0 MHz 12/08/21 11:46:48 U



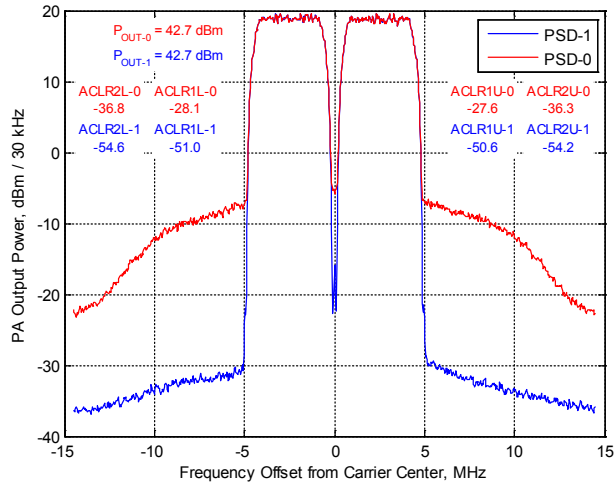
SN10606 hw4.1 PAM114 25.0° 1.80V 3.30V WCDMA2-11#9.70 2140.0 MHz 12/08/21 11:46:48



PA Output = 42.55dBm.

Power Added Efficiency: 34%

SN10606 hw4.1 PAM114 25.0° 1.80V 3.30V WCDMA2-11#9.70 2140.0 MHz 12/08/21 11:46:48 U

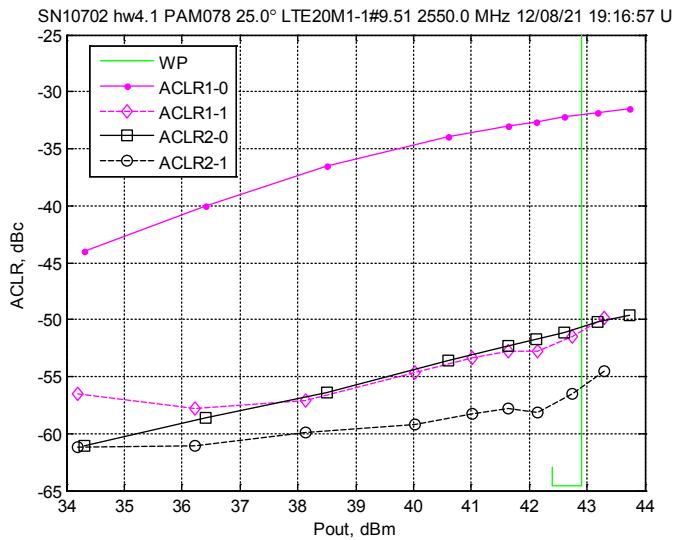


8.3. 2600-2700MHz Ampleon Doherty, Average Power 15-20W

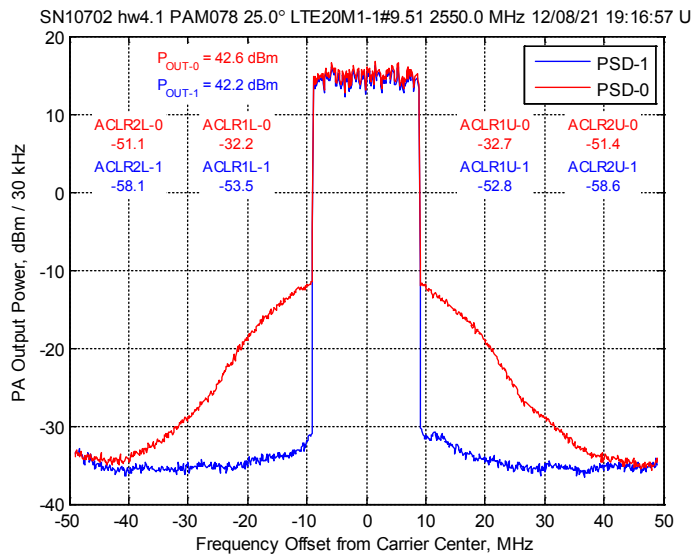
- Ampleon BLF6G27-150P
- Operating Frequency: 2655MHz
- Frequency Range: 2500MHz to 2700MHz
- Doherty, LDMOS Technology
- Gain ~15dB,
- Psat ~52.6dBm

8.3.1. LTE 20MHz ETM 3.3 (PAR = 9.51dB)

PA output-power level sweep with NXP BLF6G27-150P.

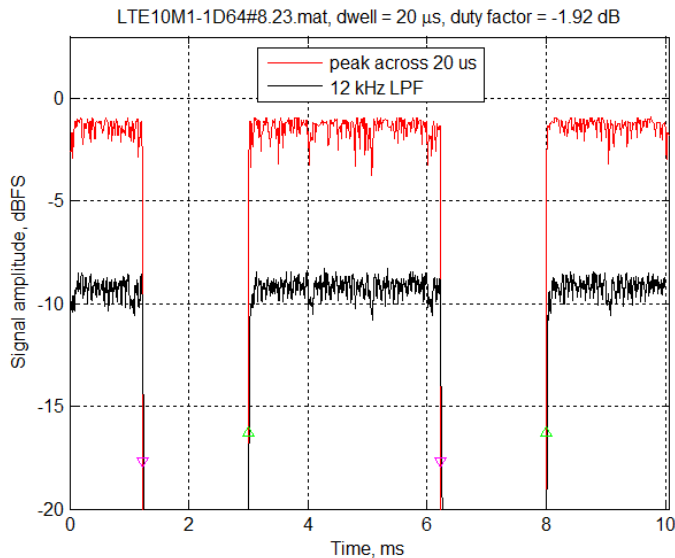


PA Output = 42.2dBm

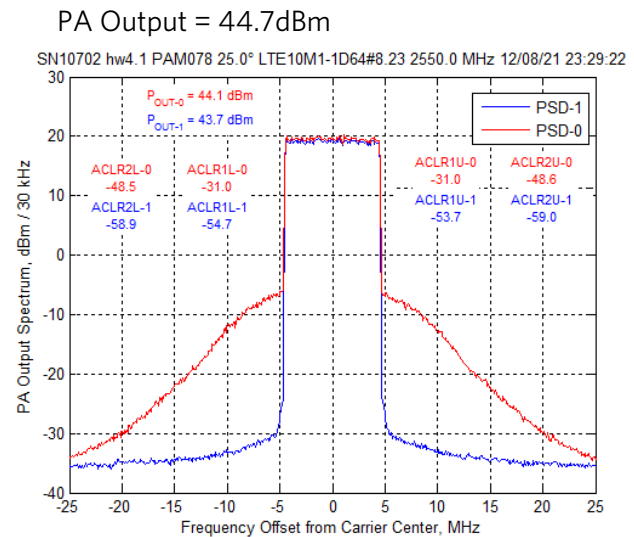
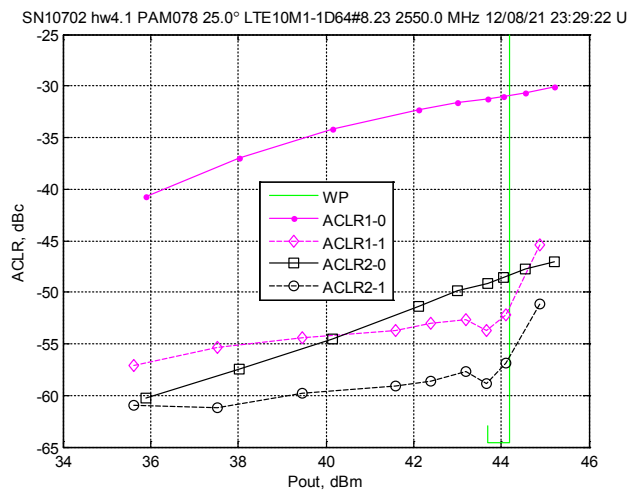


8.3.2. TD-LTE 10MHz (64% duty cycle ; 8dB PAR)

The TD-LTE spectral amplitude over time is shown in the following figure:

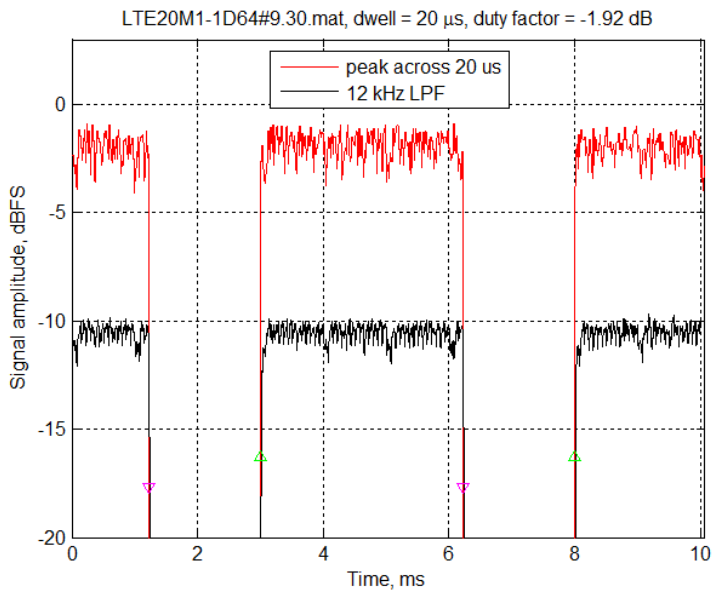


PA output power level sweep with NXP BLF6G27-150P and spectrum plot are shown in the following figures:

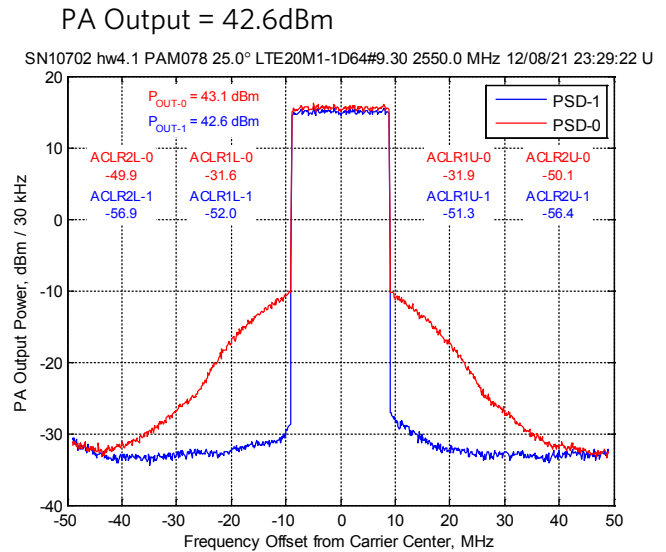
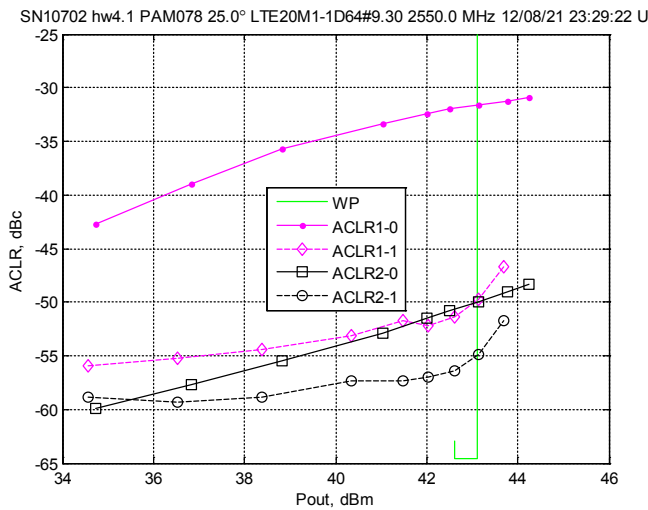


8.3.1. TD-LTE 20MHz (64% duty cycle; 9.3dB PAR)

The TD-LTE 20MHz spectral amplitude over time is shown in the following figure:



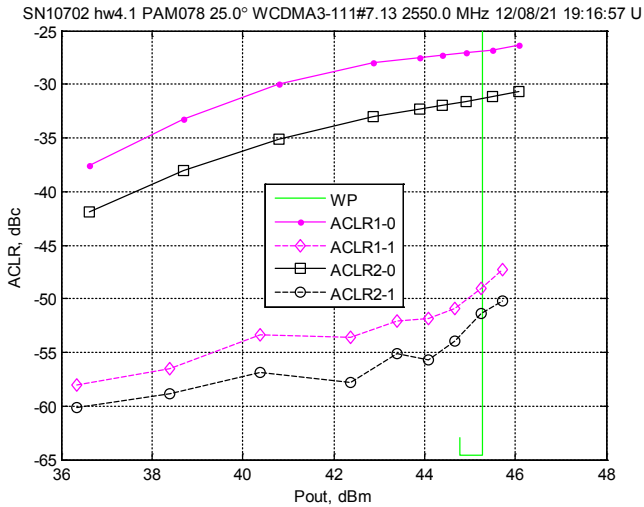
PA output-power level sweep with NXP BLF6G27-150P and spectrum plot are shown in the following figures:



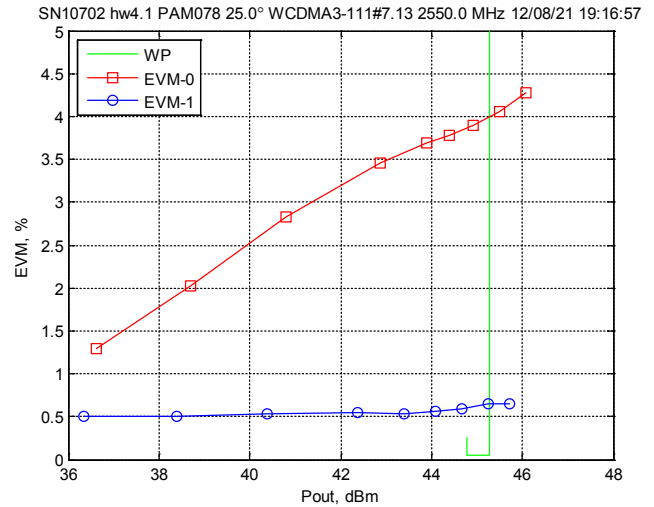
8.3.2. Three Carriers WCDMA PAR = 7.13dB

PA output-power level sweep with NXP BLF6G27-150P.

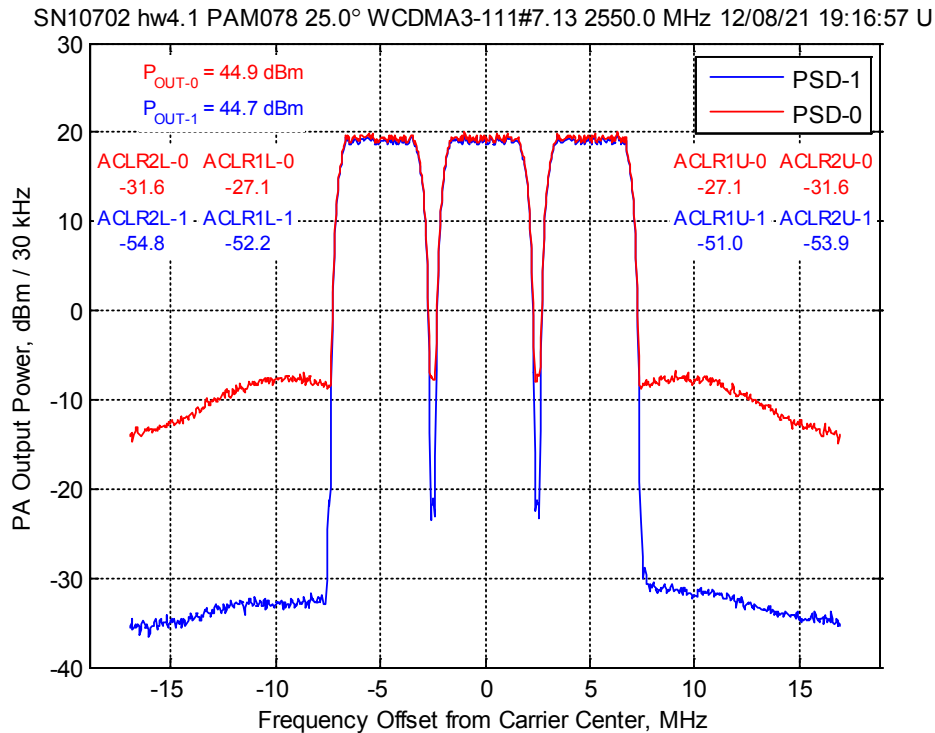
ACLR vs PA output



EVM vs PA output



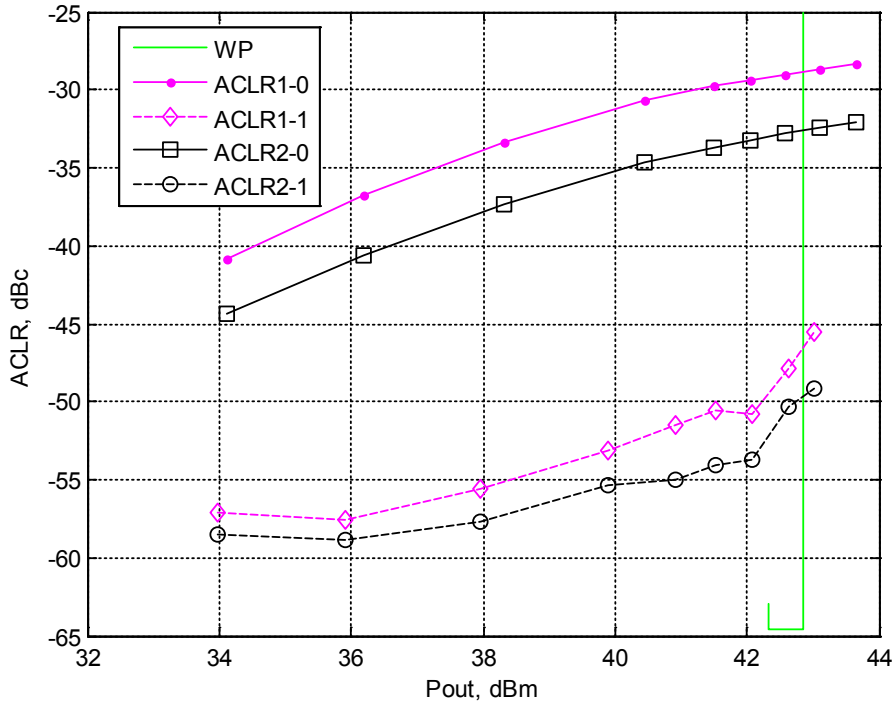
PA Output = 44.7dBm



8.3.3. Three Carriers WCDMA PAR = 9.58dB

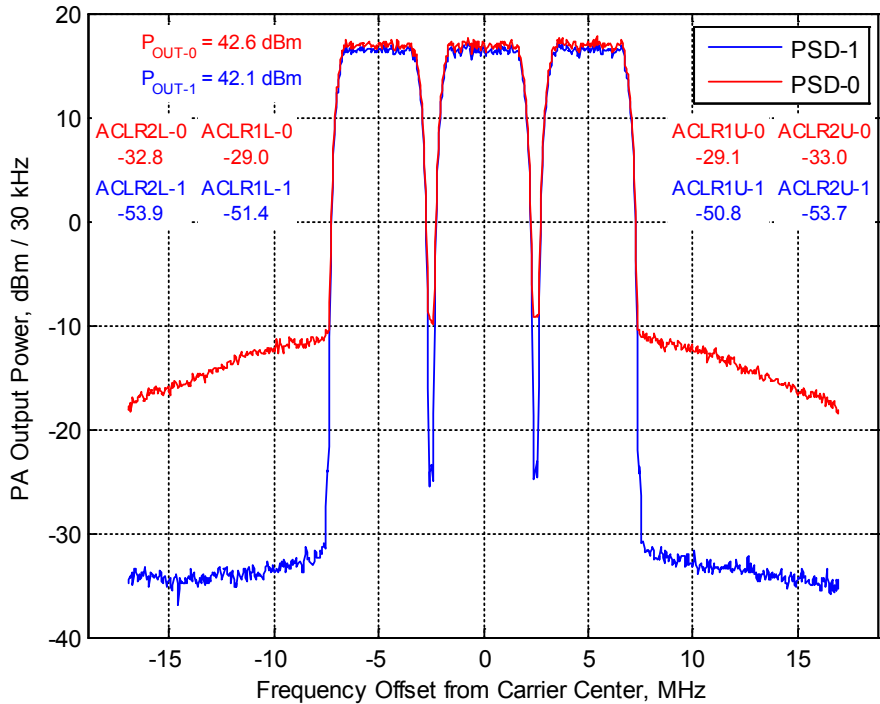
PA output-power level sweep with NXP BLF6G27-150P.

SN10702 hw4.1 PAM078 25.0° WCDMA3-111#9.58 2550.0 MHz 12/08/21 19:16:57 U



PA Output = 42.1dBm

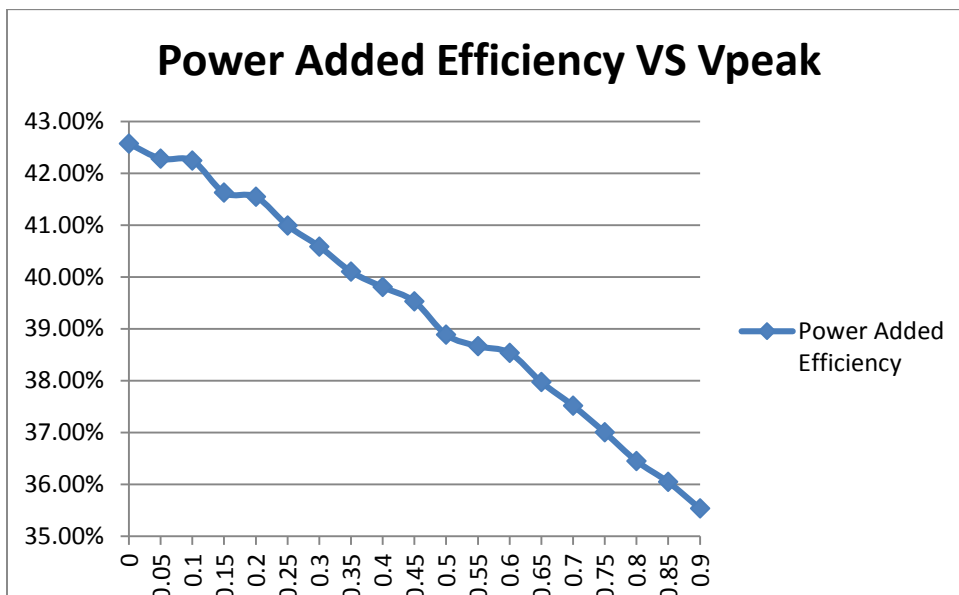
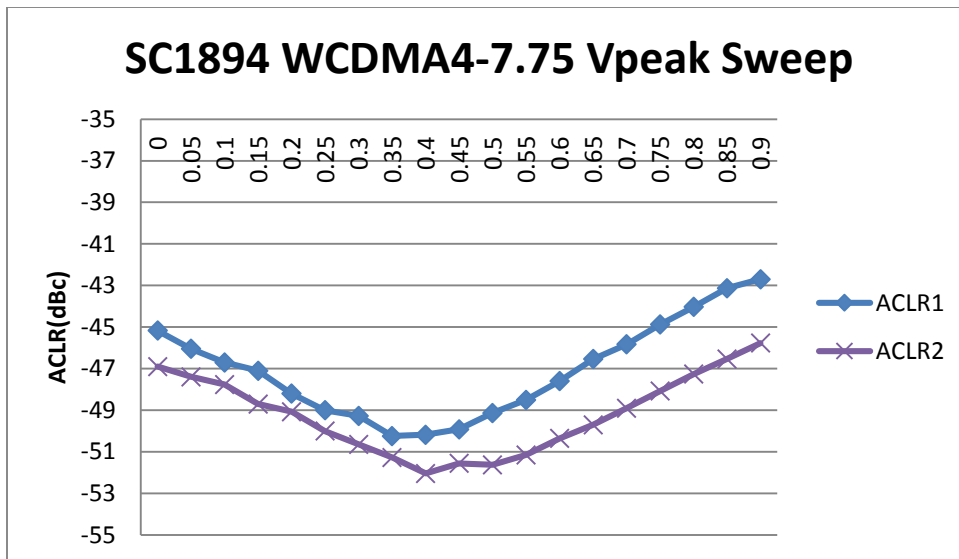
SN10702 hw4.1 PAM078 25.0° WCDMA3-111#9.58 2550.0 MHz 12/08/21 19:16:57 U



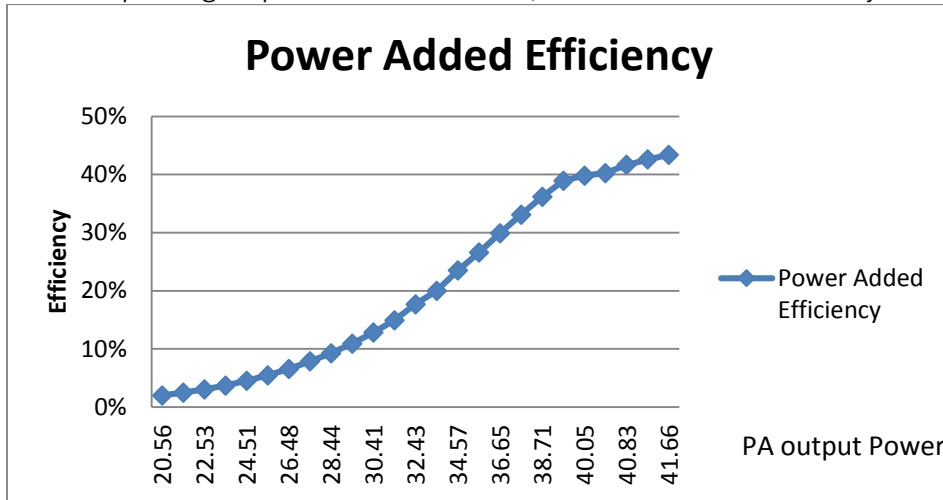
8.4. Peaking Amplifier Bias Adjustment with Ampleon BLD6G22-50 and WCDMA4 (PAR=7.75dB)

- Ampleon BLD6G22-50 Compact Design
- Operating Frequency: 2140MHz
- Frequency Range: 2110MHz to 2170MHz
- Doherty, LDMOS Technology
- Gain ~15dB,
- Psat ~48.2dBm

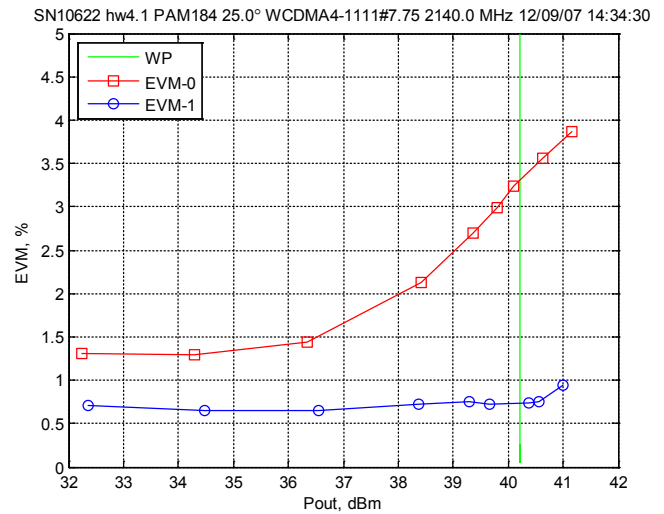
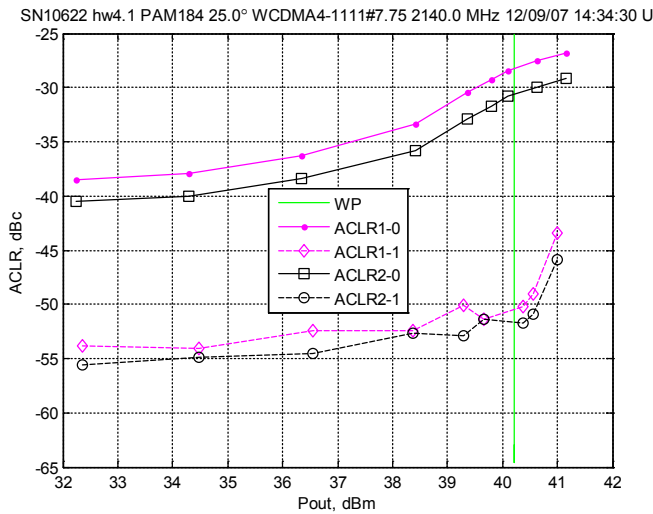
With NXP BLF6G22-50 PA output-power level at 40.4dBm ($P_{SAT} - PAR$), the peaking amplifier bias was adjusted from 0V to 0.9V. It was determined that 0.4V was the best value for final linearity with SC1894. The following plots shows the WCDMA4 (7.75dB PAR) final linearity and the power added efficiency with SC1894 versus different peaking amplifier bias (V_{PEAK}).



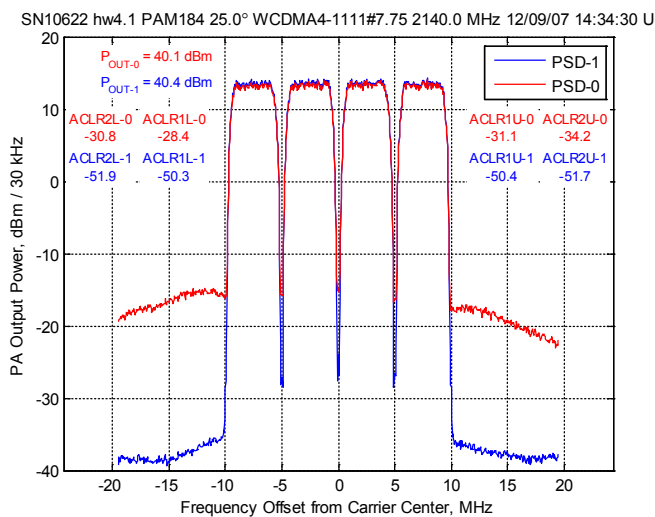
With the peaking amplifier bias set to 0.4V, the Power Added Efficiency versus PA output-power level was collected:



ACLR and EVM sweep versus PA output power level:



At 40.4dBm output power with PAE = 40%, the Spectrum plot is:



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