PF9453

Power management IC for i.MX 91 and I.MX 93

Rev. 2.0 — 26 November 2025 Product data sheet

1 General description

The PF9453 is a single chip Power Management IC (PMIC) designed for i.MX 91 or i.MX 93 processors. It provides power supply solutions for Industrial, IoT, smart appliance, and portable applications where size and efficiency are critical.

The device provides four high efficiency step-down regulators, up to three LDOs, one 400mA load switch and a 32.768 kHz crystal oscillator driver. One buck regulator supports dynamic voltage scaling (DVS) along with programmable ramping up and down time. This device is characterized across -40 °C to 105 °C ambient temperature range for HVQFN40 package and across -40 °C to 85 °C for WLCSP36 package, making it a good option for the industrial, extended industrial, and consumer markets. The four step-down regulators are designed to provide power for the i.MX 91/93 processor and the associated DRAM memory. One always-on LDO is for secure nonvolatile storage (SNVS) core power supply, remainder LDOs are used to supply power to processor and peripheral devices. One 400 mA load switch supplies 3.3 V power to the SD card, the load switch has an internal discharge resistor used to discharge the electric charge stored in the output when the equipment is turned off, for safety reasons.

The PF9453 is offered in two packages:

- 40-pin HVQFN package, 5 mm x 5 mm, 0.4 mm pitch.
- 36-bump wafer-level CSP package, 2.46 mm x 2.46 mm, 0.4 mm pitch.

Table 1 shows the differences between QFN and WLCSP package.

Table 1. Differences between PF9453 QFN and WLCSP

Characteristic	PF9453 QFN	PF9453 WLCSP	Details
Package type	HVQFN40	WLCSP36	6 Pinning information
Number of regulators	4 BUCKs, 3 LDOs	4 BUCKs, 2 LDOs (LDO2 not available)	7 Functional description
OTPs and current limit for BUCKs	A1, B1, and A2 OTPs available	A1 and B1 OTPs available	4 Ordering information
Temperature range	-40 ºC to 105 ºC for industrial and consumer applications	-40 ºC to 85 ºC for consumer applications	12 Thermal characteristics
Reset input pins	PMIC_RST_B and WDOG_B pins available	Only WDOG_B pin available	7.5 PMIC_RST_B configuration
LDO SNVS output voltage	Configurable from 1.2 V to 3.4 V	Configurable from 0.8 V to 3.0 V	8.2.28 LDOSNVS_CFG1
LDO1 input voltage	Dedicated input voltage	Connected to VSYS	5 Block diagram
Load switch protection	Overcurrent/short-circuit protection available	No overcurrent/short-circuit protection	7.6.4 Load switch
Register map	All registers in the register map table are available for QFN package	Some registers in the register map table are not available for WLCSP package	8.2 Register details

2 Features and benefits

- Four buck regulators
  - BUCK1: 0.6 V to 3.775 V, 25 mV step, 2000 mA[1]
  - BUCK2: 0.6 V to 2.1875 V, 12.5 mV step, 2700 mA[1]
  - BUCK3: 0.6 V to 3.775 V, 25 mV step, 2000 mA[1]
  - BUCK4: 0.6 V to 3.775 V, 25 mV step, 2500 mA[1]
  - Dynamic voltage scaling on BUCK2
  - Monitor fault condition
- Three linear regulators
  - LDO_SNVS, always-on, 1.2 V to 3.4 V (QFN package) or 0.8 V to 3.0 V (WLCSP package), with 25 mV step, 10 mA
  - LDO1, 0.8 V to 3.3 V with 25 mV step, 250 mA, voltage selection through SD_VSEL pin
  - LDO2, 0.5 V to 1.95 V with 25 mV step, 200 mA (only available in QFN package)
- One 400 mA load switch with a built-in active discharge resistor and GPIO/I^2C control
- 32.768 kHz crystal oscillator driver and buffer output
- Power control I/O
  - Power ON/OFF control
  - Standby/Run mode control
  - Watchdog reset input
- Flexible power ON/OFF sequence, one time programmable (OTP) device configuration
- Built-in active discharge resistor
- Fm+ 1 MHz I^2C Interface
- ESD protection
  - Human body model (HBM) ±2000 V
  - Charged device model (CDM) ±500 V
- 40-pin QFN,5 mm x 5 mm, 0.4 mm pitch
- 6 x 6 bump array, WLCSP, 2.46 mm x 2.46 mm, 0.4 mm pitch

3 Applications

- IoT devices
- White goods appliances
- Industrial applications
- Portable devices

1 Output current of PF9453 regulators changes depending on the part number; refer to Table 2

4 Ordering information

Table 2. Ordering information

Part number	Topside marking	Ambient temperature	Package			OTP configuration	Processor	Notes
			Name	Description	Version			
MPF9453AVMA1HN	-	-40 °C to +105 °C (for use in industrial applications)	HVQFN40	40-pin QFN, 5.0 mm x 5.0 mm with exposed pad, 0.4 mm pitch	SOT2231-1	A1	i.MX 9131, 9111	[1]
MPF9453AVMA2HN	-					A2	i.MX 93	[2]
MPF9453AVMB1HN	-					B1	i.MX9121, 9101	[3]
MPF9453ACMA1HN	-	-40 °C to +85 °C (for use in consumer applications)				A1	i.MX 9131, 9111	[1]
MPF9453ACMB1HN	-					B1	i.MX9121, 9101	[3]
MPF9453ACMA1UKR2	-	-40 °C to +85 °C (for use in consumer applications)	WLCSP36	Wafer Level Chip Scale Package; 36 bumps; 2.46 mm x 2.46 mm x 0.525 mm body (backside coating included), 0.4 mm pitch	SOT1780-14	A1	i.MX91	[1]
MPF9453ACMB1UKR2	-					B1	i.MX9121, 9101	[3]

[1] For A1 OTP configuration, BUCK1 and BUCK3 are 1000 mA, BUCK2 is 1500 mA and BUCK4 is 2500 mA
[2] For A2 OTP configuration, BUCK1 and BUCK3 are 2000 mA, BUCK2 is 2700 mA and BUCK4 is 2500 mA
[3] For B1 OTP configuration, BUCK1, BUCK2 and BUCK3 are 1000 mA, and BUCK4 is 1500 mA

Details of the OTP programming for each device can be found in Section 14.

5 Block diagram

5.1 Block diagram QFN package

Output current of PF9453 regulators changes depending on the part number. See Table 2

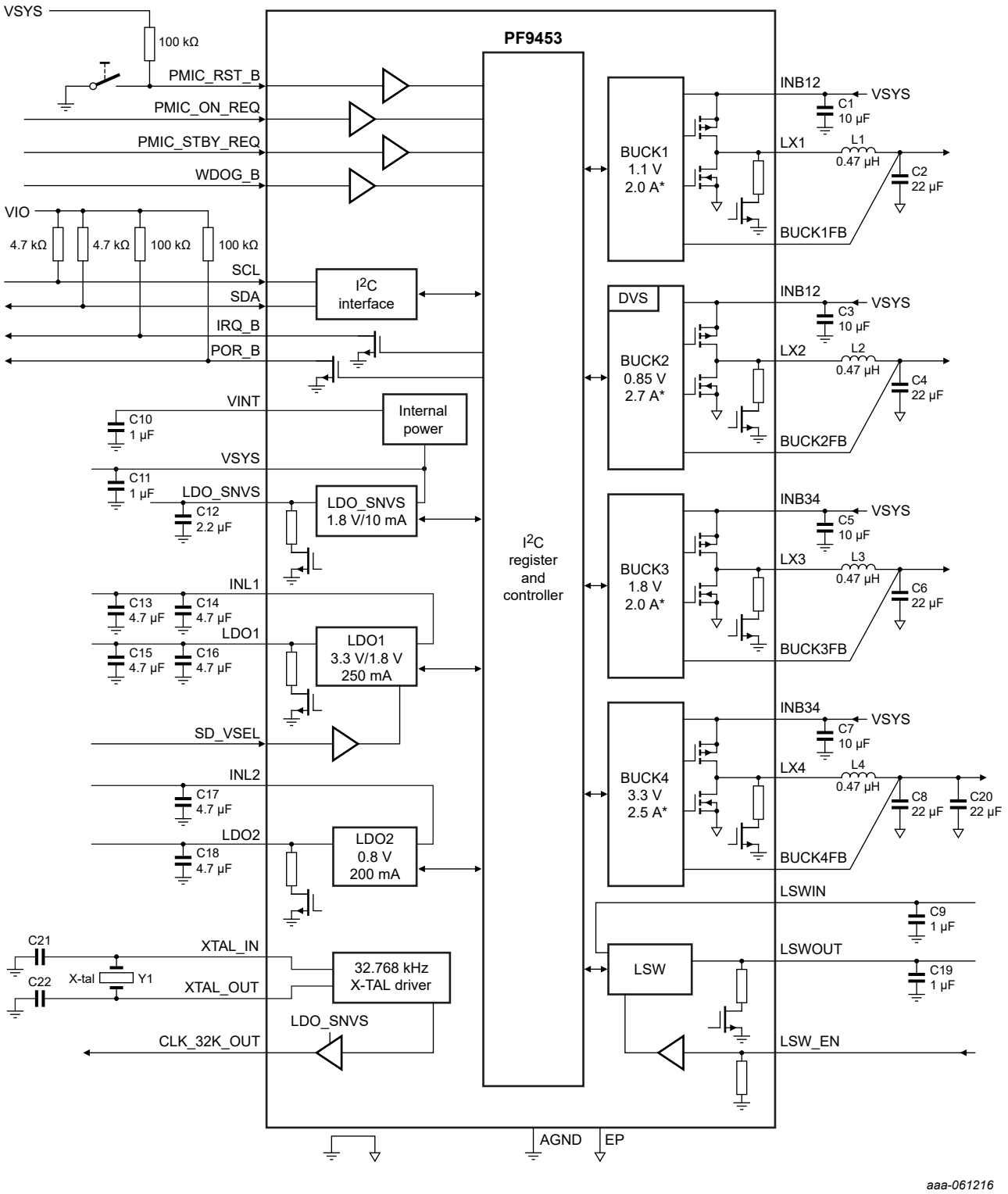


Figure 1. PF9453 block diagram - HVQFN40 package

5.2 Block diagram WLCSP package

Output current of PF9453 regulators changes depending on the part number. See Table 2

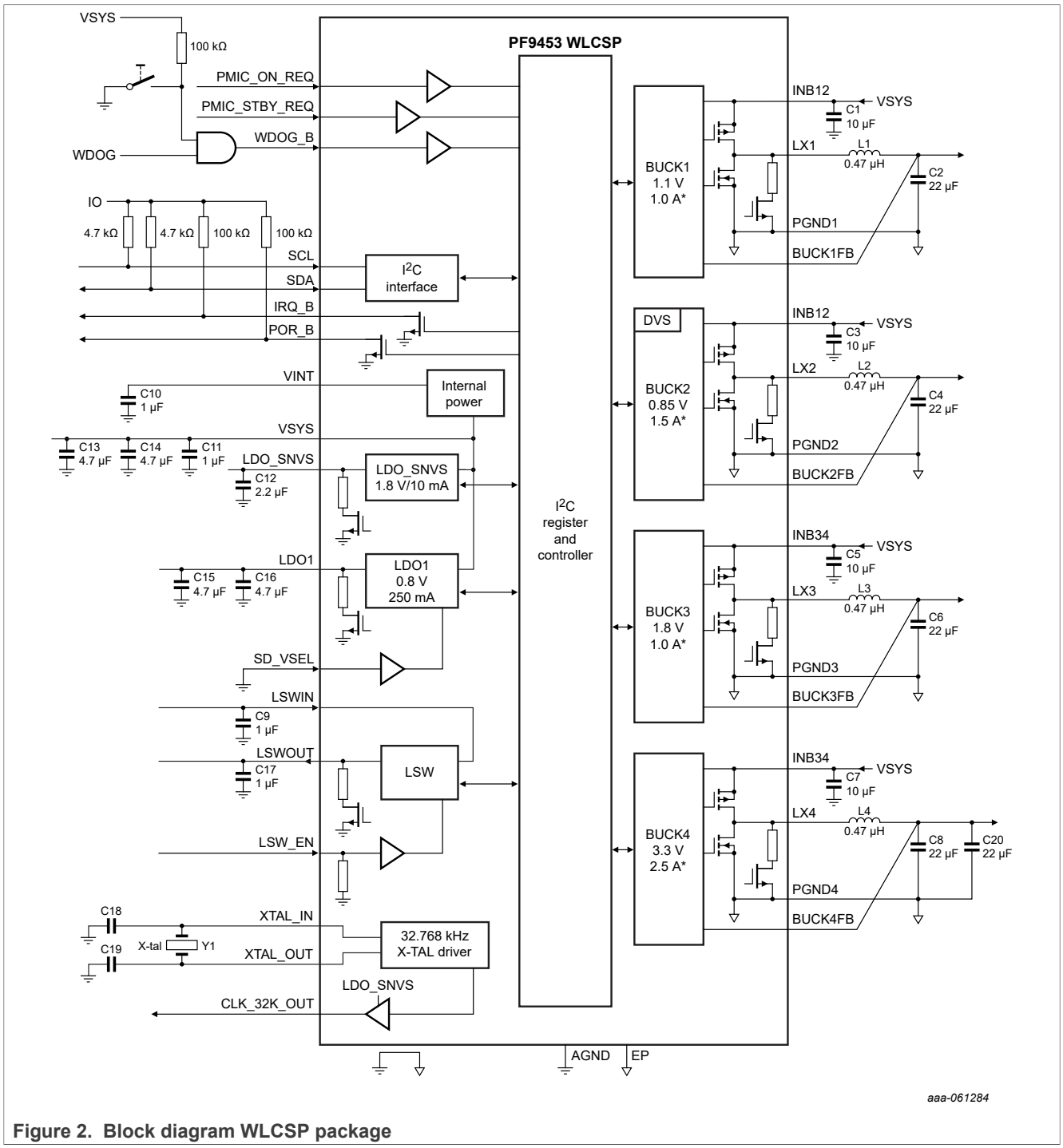


Figure 2. Block diagram WLCSP package

6 Pinning information

6.1 Pinning QFN package

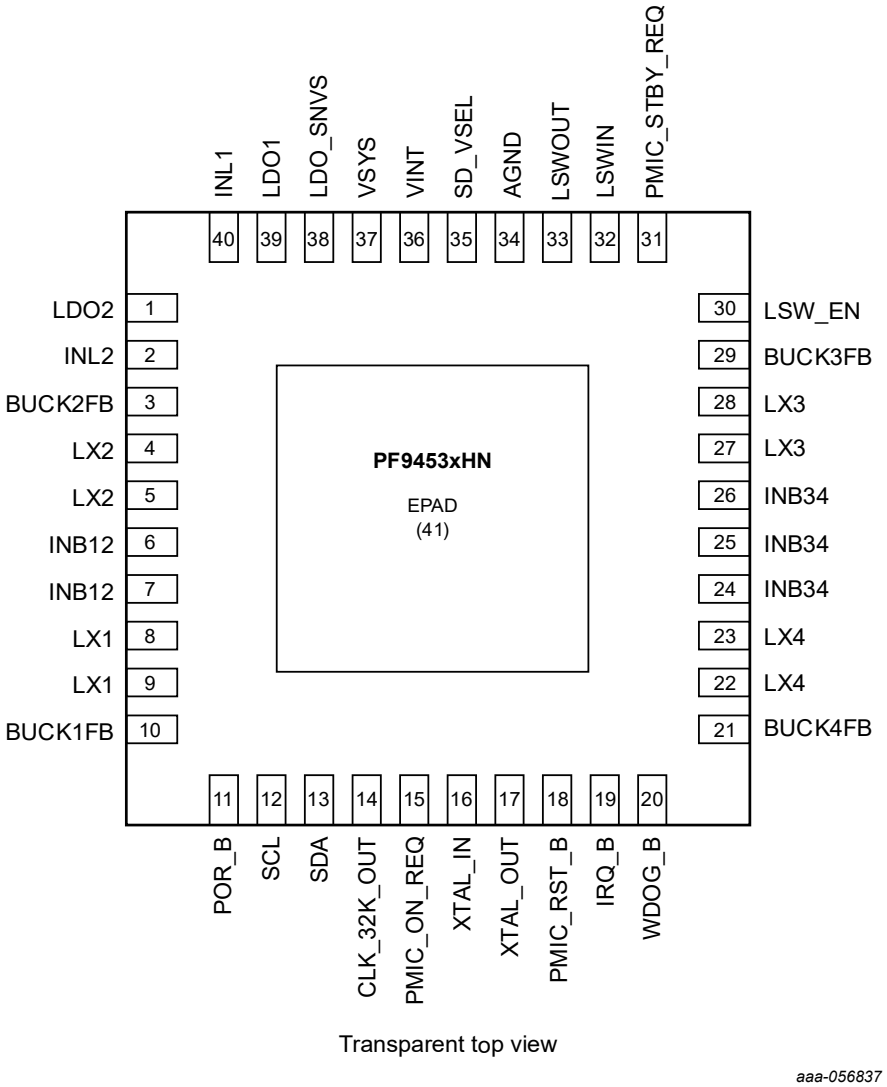


Figure 3. PF9453 pin map – HVQFN40 Transparent top view

6.2 Pinning WLCSP package

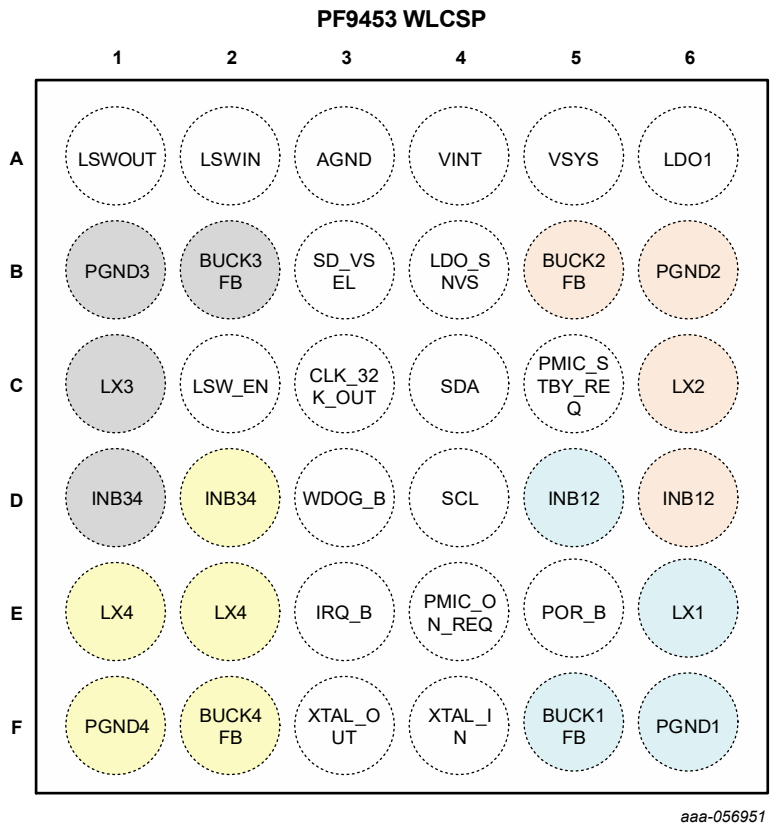


Figure 4. PF9453 pin map WLCSP36 – Top view (bump-side down)

6.3 Pin description QFN package

Table 3. Pin description – PF9453 QFN

Symbol	Pin	Type	Description
LDO2	1	P	LDO2 output, bypass with a 4.7 µF to GND
INL2	2	P	LDO2 input pin, bypass with a 4.7 µF to GND
BUCK2FB	3	AI	Buck 2 feedback pin
LX2	4, 5	P	Buck 2 switching node
INB12	6, 7	P	Buck 1 and Buck 2 input pins, bypass with 2 µF x 10 µF
LX1	8, 9	P	Buck 1 switching node
BUCK1FB	10	AI	Buck 1 feedback pin
POR_B	11	DO	Power-on reset (POR) output pin. Open-drain output requiring external pullup resistor
SCL	12	DI	I^2C serial clock pin
SDA	13	DIO	I^2C serial data pin
CLK_32K_OUT	14	DO	32.768 kHz clock CMOS output with LDO_SNVS power rail
PMIC_ON_REQ	15	DI	PMIC input from an application processor. When it is asserted high, the device starts power on sequence
XTAL_IN	16	AI	32.768 kHz crystal oscillator input, tie to GND if X-tal is not used
XTAL_OUT	17	AO	32.768 kHz crystal oscillator output, leave floating if X-tal is not used
PMIC_RST_B	18	DI	PMIC reset input pin. Once it is asserted low, PMIC performs a Cold Reset

Table 3. Pin description – PF9453 QFN*...continued*

Symbol	Pin	Type	Description
IRQ_B	19	DO	PMIC interrupt pin, open-drain output requiring external pullup resistor.
WDOG_B	20	DI	Watchdog reset input from application processor
BUCK4FB	21	AI	Buck 4 feedback pin
LX4	22, 23	P	Buck 4 switching node
INB34	24, 25, 26	P	Buck 3 and Buck 4 input pins, bypass with 2 µF x 10 µF
LX3	27, 28	P	Buck 3 switching node
BUCK3FB	29	AI	Buck 3 feedback pin
LSW_EN	30	DI	Load switch enable input pin. It has an internal 1.5 MΩ pulldown resistor
PMIC_STBY_REQ	31	DI	Standby mode input from application processor. When it is asserted high, the device enters standby mode
LSWIN	32	P	Load switch input pin. Bypass with a 1 µF to GND
LSWOUT	33	P	Load switch output pin, bypass with a 1 µF to GND
AGND	34	GND	Analog GND pin. It should be connected to the GND plane through via. Do not short to EPAD directly on the top layer
SD_VSEL	35	DI	LDO1 voltage selection input pin. LDO1 output is 3.3 V when it is driven low and 1.8 V when driven high
VINT	36	P	Internal power supply output, bypass with a 1 µF to GND
VSYS	37	P	Internal power input. Bypass with a 1 µF to GND
LDO_SNVS	38	P	LDO_SNVS output pin, bypass with a 2.2 µF to GND
LDO1	39	P	LDO1 output. Bypass with 2 µF x 4.7 µF to GND
INL1	40	P	LDO1 input pin, bypass with 2 µF x 4.7 µF to GND
EPAD	41	GND	Exposed pad, connect to GND

6.4 Pin description WLCSP package

Table 4. Pin description – PF9453 WLCSP package

Symbol	Pin	Type	Description
LSWOUT	A1	P	Load switch output pin, bypass with a 1 µF to Ground.
LSWIN	A2	P	Load switch input pin. Bypass with a 1 µF to Ground
AGND	A3	GND	Analog ground pin. It should be connected to ground plane through Via
VINT	A4	P	Internal power supply output, bypass with a 1 µF to GND
VSYS	A5	P	Internal power input. Bypass with a 1 µF to Ground
LDO1	A6	P	LDO1 output. Bypass with 2 x 4.7 µF to Ground
PGND3	B1	GND	Buck 3 power ground
BUCK3FB	B2	AI	Buck 3 feedback pin
SD_VSEL	B3	DI	LDO1 voltage selection input pin. LDO1 outputs voltage set by L1_OUT_L[6:0] when it is driven low and L1_OUT_H[6:0] when driven high
LDO_SNVS	B4	P	LDO_SNVS output pin, bypass with a 2.2 µF to Ground
BUCK2FB	B5	AI	Buck 2 feedback pin
PGND2	B6	GND	Buck 2 Power ground
LX3	C1	P	Buck 3 switching node
LSW_EN	C2	DI	Load switch enable input pin. It has internal 1.5 Mohm pull down resistor
CLK_32K_OUT	C3	DO	32.768 kHz clock CMOS output with LDO_SNVS power rail
SDA	C4	DIO	I2C serial data pin
PMIC_STBY_REQ	C5	DI	Standby mode input from application processor. When it is asserted high, device enters STANDBY mode
LX2	C6	P	Buck 2 switching node

Table 4. Pin description – PF9453 WLCSP package*...continued*

Symbol	Pin	Type	Description
INB34	D1, D2	P	Buck 3 and Buck 4 input pins, bypass with 2 x 10 µF
WDOG_B	D3	DI	Watchdog reset input from application processor
SCL	D4	DI	I2C serial clock pin
INB12	D5, D6	P	Buck 1 and Buck 2 input pins, bypass with 2 x 10 µF
LX4	E1, E2	P	Buck 4 switching node
IRQ_B	E3	DO	PMIC interrupt pin, open drain output requiring external pull up resistor
PMIC_ON_REQ	E4	DI	PMIC ON input from application processor. When it is asserted high, the device starts power on sequence
POR_B	E5	DO	Power On reset output pin. Open drain output requiring external pull up resistor
LX1	E6	P	Buck 1 switching node
PGND4	F1	GND	Buck 4 power ground
BUCK4FB	F2	AI	Buck 4 feedback pin
XTAL_OUT	F3	AO	32.768 kHz crystal oscillator output, leave float if X-tal is not used
XTAL_IN	F4	AI	32.768 kHz crystal oscillator input, tie to GND if X-tal is not used
BUCK1FB	F5	AI	Buck 1 feedback pin
PGND1	F6	GND	Buck 1 power ground

7 Functional description

7.1 Functional diagram

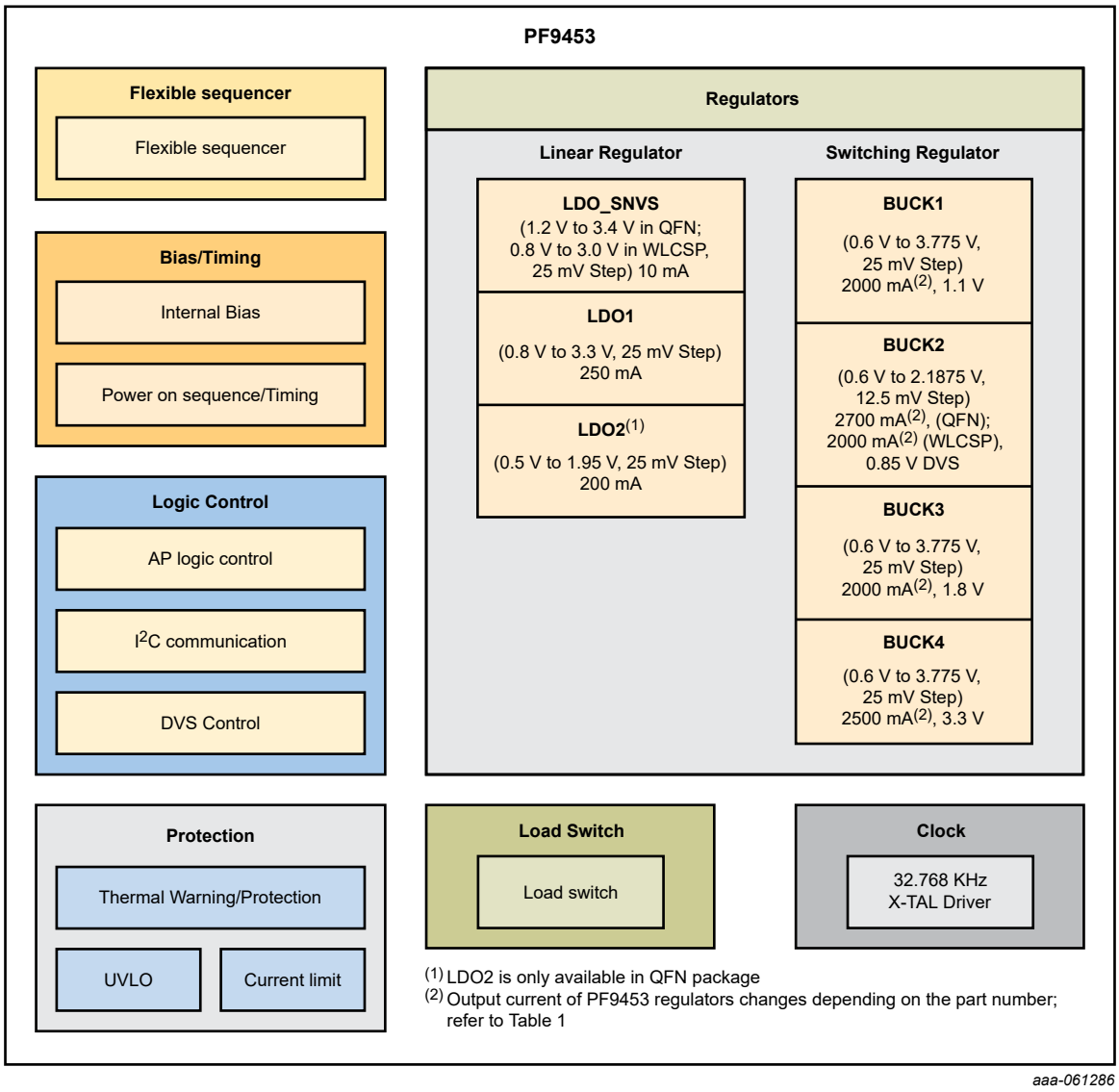


Figure 5. PF9453 functional block diagram

7.2 PF9453 OTP version

The PF9453 can be configured to each regulator default voltage and startup sequence from the internal OTP configuration. Table 5 shows the power-up sequence for existing OTPs.

Table 5. Power up sequence

Regulator	MPF9453AxMA1HN, MPF9453AxMA2HN, MPF9453AxMB1HN	MPF9453ACMA1UKR2, MPF9453ACMB1UKR2
LDO_SNVS	1.8 V, always on	1.8 V, always on
BUCK1	T4, 1.1 V	T4, 1.1 V
BUCK2	T1, 0.85 V	T1, 0.85 V
BUCK3	T3, 1.8 V	T3, 1.8 V
BUCK4	T5, 3.3 V	T5, 3.3 V

Table 5. Power up sequence*...continued*

Regulator	MPF9453AxMA1HN, MPF9453AxMA2HN, MPF9453AxMB1HN	MPF9453ACMA1UKR2, MPF9453ACMB1UKR2
LDO1	T6, 3.3 V / 1.8 V	T2, 0.8 V
LDO2*	T2, 0.8 V	NA
Load Switch	T5	T5

Details of the OTP programming for each device can be found in Section 14.

7.3 Power states

PF9453 has six power states: OFF, SNVS, RUN, PWRDN, PWRUP, and FAULT_SD. Figure 6 shows the state transition diagram with the conditions to enter and exit each state.

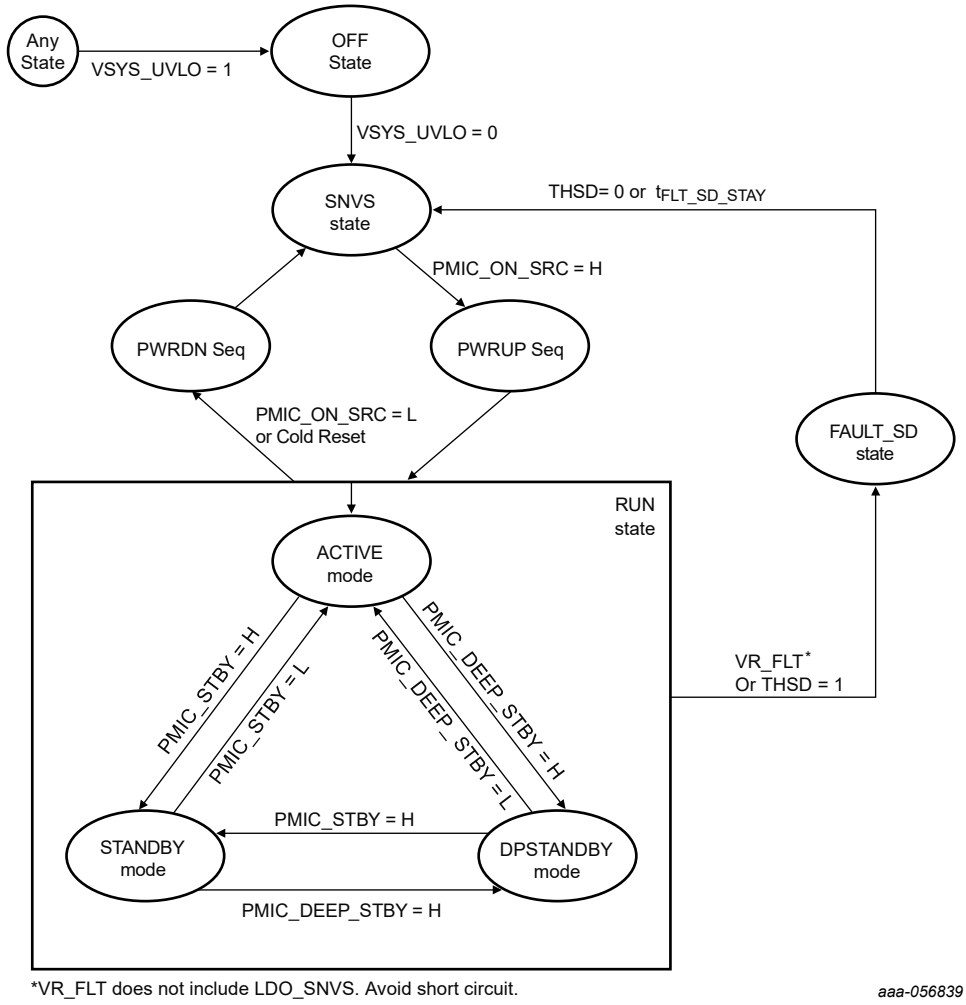


Figure 6. Power states diagram

7.3.1 Off state

PF9453 enters the OFF state from any state when VSYS falls below the V_{SYS_UVLO} threshold. All regulators, including LDO_SNVS are off, and all registers get reset in the state.

7.3.2 SNVS state

PF9453 enters the secure non-volatile storage (SNVS) mode when VSYS exceeds the V_{SYS_UVLO} rising threshold. LDO_SNVS is turned on within t_{SNVS}. After turning LDO_SNVS on, the power on source signals to move to PWRUP state are monitored.

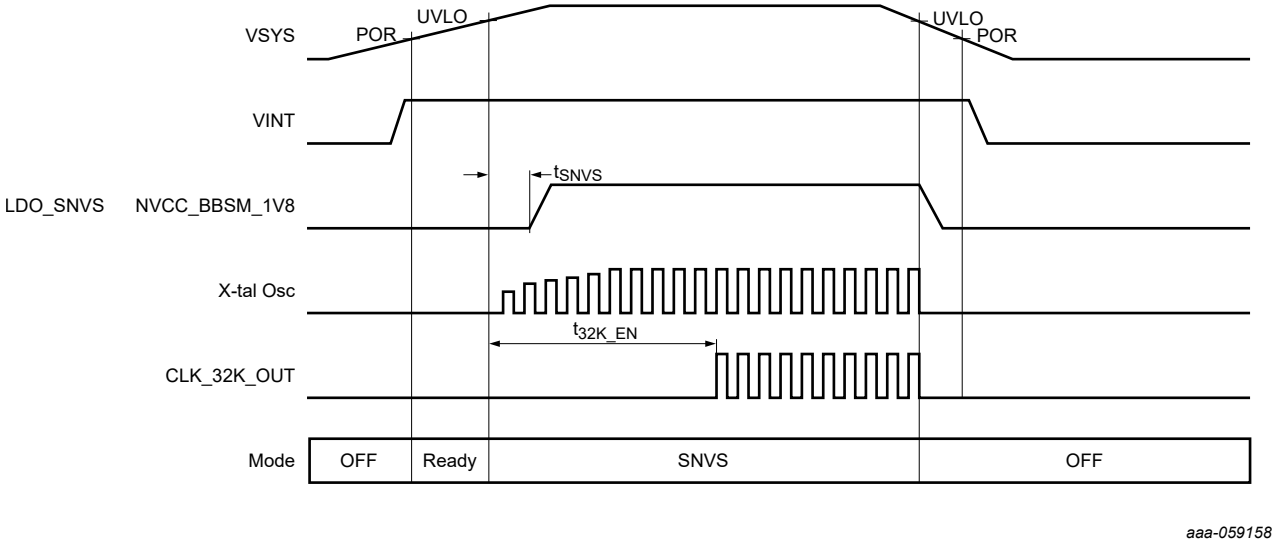


Figure 7. SNVS state ON/OFF sequence

Table 6. SNVS state

Time	Description	Value
t_{SNVS}	Maximum time to enable LDO_SNVS from VSYS UVLO detected	10 ms
t_{32K_EN}	Time to stable 32 kHz clock buffer output from VSYS UVLO detected	1 s

7.3.3 PWRUP state

7.3.3.1 Power ON sources

When the internal signal PMIC_ON_SRC is asserted high in the SNVS state, it starts powering up regulators with the pre-defined power ON sequence. The PMIC_ON_SRC signal is generated by these two signals:

- PMIC_ON_REQ after its debounce time (t_{ON_DEB})
- PMIC_RST_B after its debounce time ($t_{DEB\_PMIC\_RST\_B}$) and ONKEY timer (t_{ONKEY}) expires.[2]
  For more details about PMIC_RST_B behavior and configuration see Section 7.5.

Figure 8 shows how PMIC_ON_SRC is generated.

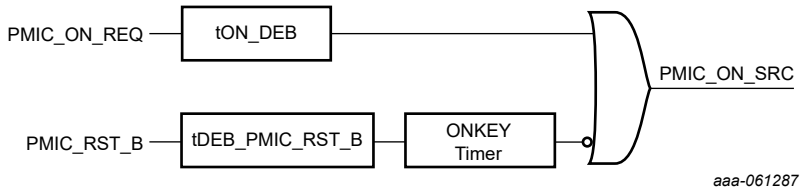


Figure 8. PF9453 power on source

2 PMIC_RST_B pin is available only in QFN

7.3.3.2 Power-on sequence

PF9453 supports a flexible power sequencer allowing the power-on sequence to be preprogrammed in OTP.

When PMIC_ON_SRC is asserted high, the PUD_T1 group is turned on at first in the t_{ON_STEP} after PMIC_ON_SRC is high. The next group, PUD_T2 is turned on in the t_{ON_STEP} after POK of the PUD_T1 group regulator(s) is high. If the POK does not come up within t_{POK_EXP}, then the POK is ignored and the next group is turned ON in t_{ON_STEP}. This power-on sequence ends up releasing the POR_B pin high impedance in t_{RSTB} after the last group, PUD_T16 regulator, is turned ON. For PUD group which any regulator is not assigned, the next PUD group is turned on in t_{ON_STEP}.

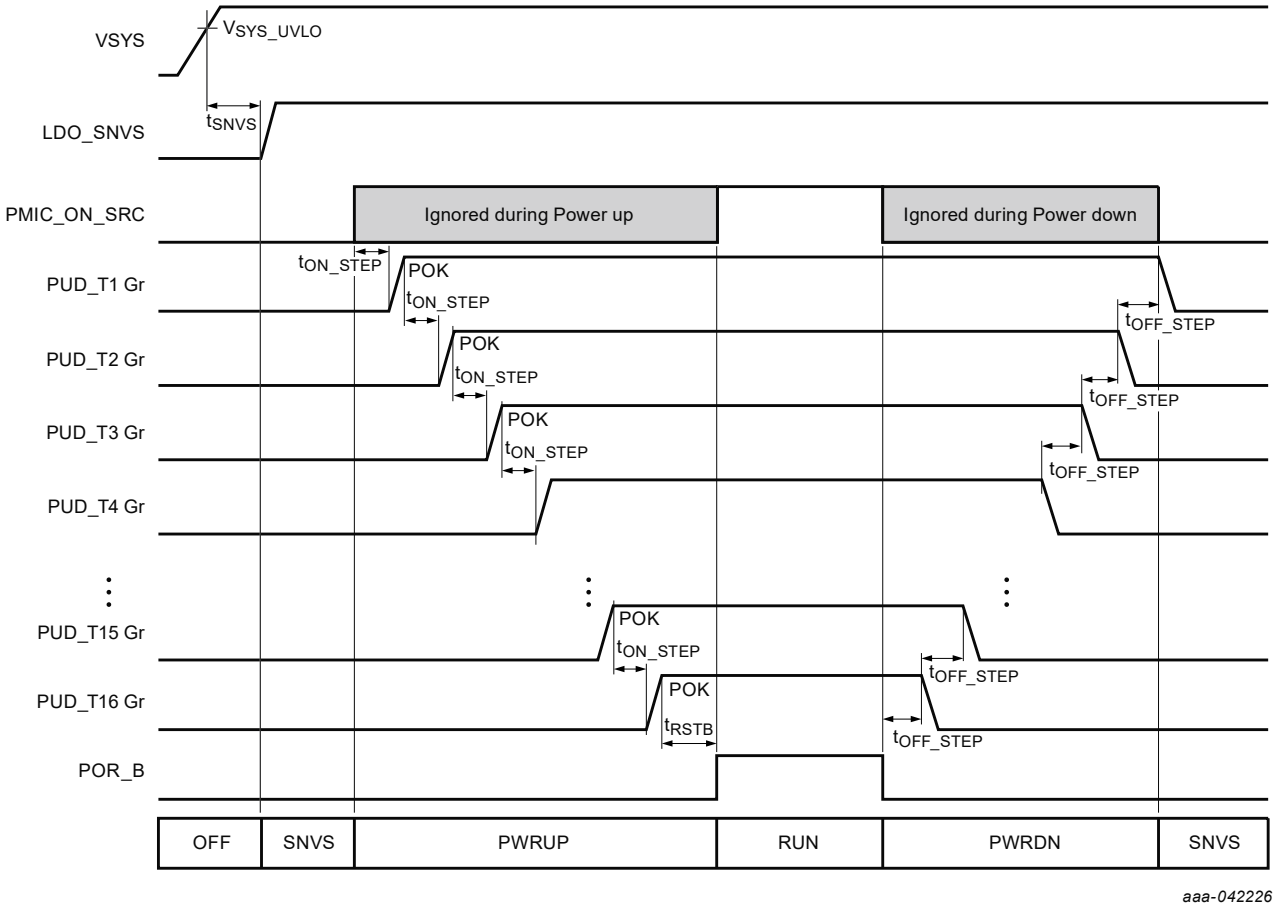


Figure 9. PF9453 ON/OFF sequence

Table 7. Power ON/OFF sequence timing table

Time	Description	Value	Comment
t_{ON_STEP}	Time step to turn on each regulator	2 ms	Programmable, PSQ_TON_STEP. OTP programmable
t_{OFF_STEP}	Time step to turn off each regulator	8 ms	Programmable, PSQ_TOFF_STEP. OTP programmable
t_{RSTB}	Time from PUD_T16 GrPOK to POR_B release during Power On sequence	20 ms	—
t_{POK_EXP}	POK wait timer out during Power On sequence	10 ms	—

7.3.4 PWRDN state

When PMIC_ON_SRC is asserted low in the RUN state, the PF9453 enters the PWRDN state, where it starts with pulling down POR_B, and then turning off each PUD group in t_{OFF_STEP}. The state machine then enters the SNVS state. See Figure 9.

7.3.5 RUN state

The PF9453 enters the RUN state after the PWRUP state. If PMIC_ON_SRC is asserted low, the PF9453 transitions to the PWRDN state. When a cold reset event is triggered in the RUN state, it transitions to the PWRDN state. If a Regulator fault or Thermal shutdown happens in this state, it transitions to FAULT_SD state.

As shown in Table 8, there are three modes in the RUN state, ACTIVE, STANDBY and DPSTANDBY modes, depending on the PMIC_STBY_REQ pin and the STANDBY_CFG bit in the SYS_CFG1 register.

Table 8. States summary

State	Mode	VSYS	PMIC_ON_SRC	STANDBY_CFG bit	PMIC_STBY_REQ
OFF	—	VSYS < VSYS_UVLO	X	X	X
SNVS	—	VSYS > VSYS_UVLO	Low	X	X
RUN	ACTIVE	VSYS > VSYS_UVLO	High	X	Low
RUN	STANDBY	VSYS > VSYS_UVLO	High	0b	High
RUN	DPSTANDBY	VSYS > VSYS_UVLO	High	1b	High

Note: *Signals with letter "X" are meant to be ignored.*

Internal signals to change modes are generated as below.

1. PMIC_STBY = PMIC_STBY_REQ pin when STANDBY_CFG = 0b. PMIC_STBY is set high only when the PMIC_STBY_REQ pin is high and the STANDBY_CFG bit is 0b.
2. PMIC_DEEP_STBY = PMIC_STBY_REQ pin when STANDBY_CFG = 1b. PMIC_DEEP_STBY is set high only when the PMIC_STBY_REQ pin is high and the STANDBY_CFG bit is 1b.

Each regulator and load switch has enable configuration bits to turn on each mode.

00b = OFF

01b = ON at RUN State

10b = ON at ACTIVE mode or STANDBY mode, OFF at DPSTANDBY

11b = ON at ACTIVE mode, OFF at STANDBY or DPSTANDBY

7.3.5.1 ACTIVE mode

When PF9453 enters the RUN state from the PWRUP state, the state machine enters the ACTIVE mode at first. Then it transitions to STANDBY mode or DPSTANDBY mode, depending on the PMIC_STBY or PMIC_DEEP_STBY signal.

7.3.5.2 STANDBY mode

PF9453 transitions to STANDBY mode when PMIC_STBY is high. PMIC_STBY is determined by the PMIC_STBY_REQ pin when the STANDBY_CFG bit in the SYS_CFG1 register is set to 0b. The PF9453 moves to ACTIVE mode when the PMIC_STBY_REQ pin is low. It transitions to DPSTANDBY mode when the STANDBY_CFG bit changes to 1b.

7.3.5.3 DPSTANDBY mode

The PF9453 transitions to DPSTANDBY (Deep Standby) mode when PMIC_DEEP_STBY is high. PMIC_DEEP_STBY is determined by the PMIC_STBY_REQ pin when the STANDBY_CFG bit in the SYS_CFG2 register is set to 1b. The PF9453 moves to ACTIVE mode when the PMIC_STBY_REQ pin is low. It transitions to STANDBY mode when STANDBY_CFG bit changes to 0b.

7.3.6 FAULT_SD state

PF9453 has two fault shutdown sources.

1. **Thermal shutdown**: Transition to SNVS state after FAULT_SD state
   When junction temperature reaches T_{JSHDN}, the PF9453 enters the FAULT_SD state after t_{FLT_THSD}, where all regulators are turned off immediately after pulling down POR_B. The PF5493 stays at FAULT_SD until the junction temperature falls below T_{JSHDN}. When the temperature drops below T_{JSHDN}, the PF5493 transitions to the SNVS state.

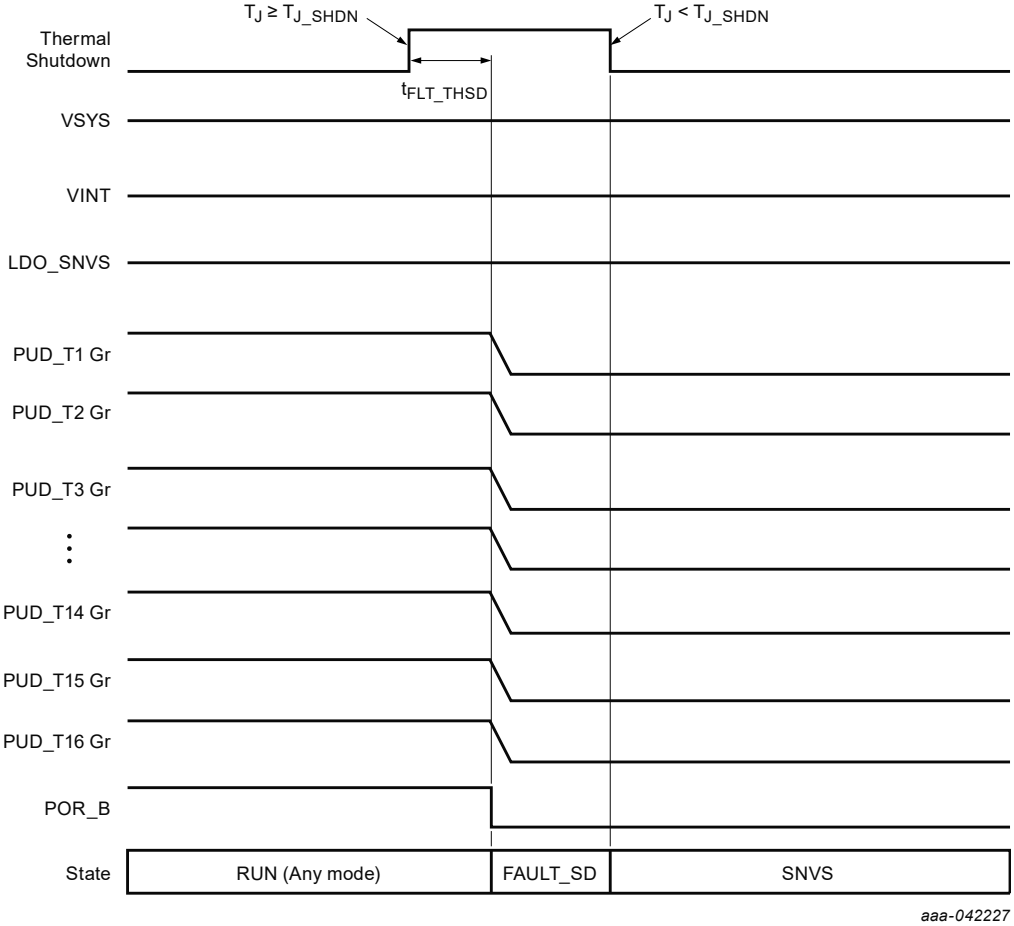


Figure 10. PF9453 FAULT_SD from thermal shutdown

Table 9. FAULT_SD thermal shutdown timing

Time	Description	Value	Comment
t_{FLT_THSD}	Time to reset released from fault event	20 µs	—

2. **Voltage regulator fault in RUN state:** Transition to FAULT_SD state in $t_{FLT\_SD\_WAIT}$ after a Fault is detected and then transitions to the SNVS state in $t_{FLT\_SD\_STAY}$.

The VR Fault status bit VR_FLT1_S in the INT1_STATUS register is latched to "1" when the corresponding regulator (except LDO_SNVS) voltage falls below the POK threshold for t_{DEB_POKB}.
If the Fault status bit is masked in the VRFLT1_MASK register, the PF9453 does not enter the FAULT_SD state, instead, the PF9453 stays in the RUN state. If the Fault register bit is unmasked, it starts the $t_{FLT\_SD\_WAIT}$ timer. The application processor can determine to enter the FAULT_SD state by masking the VR Fault status bit in the VRFLT1_MASK registers before the timer expires. The PF9453 enters the FAULT_SD state when the timer expired. The PF9453 stays in the FAULT_SD state for $t_{FLT\_SD\_STAY}$ and moves to the SNVS state from the FAULT_SD state after $t_{FLT\_SD\_STAY}$.

Note:

PF9453 does not enter the FAULT_SD mode from the load switch overcurrent fault.

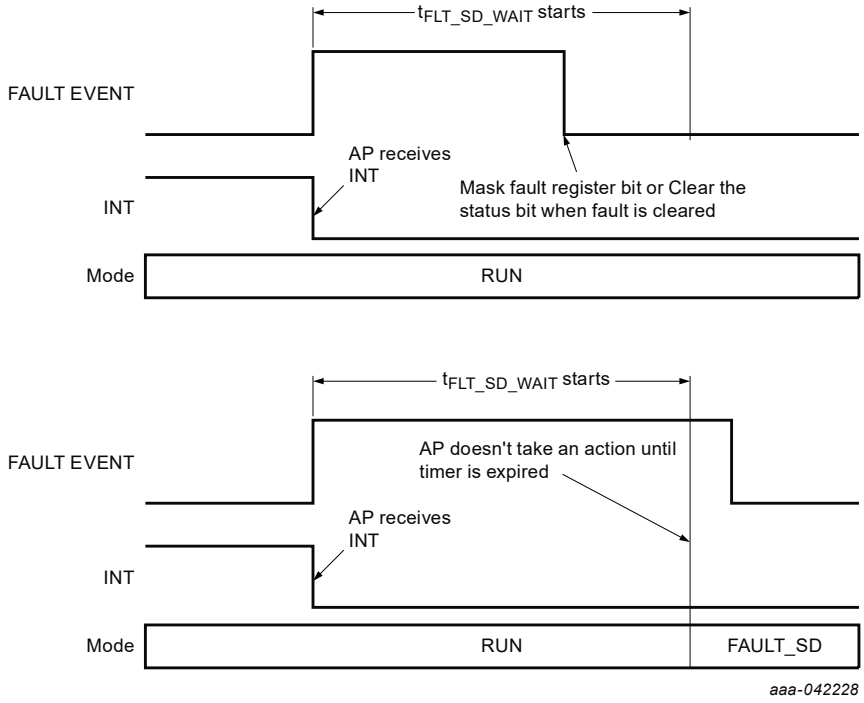


Figure 11. FAULT_SD from VR fault in RUN state

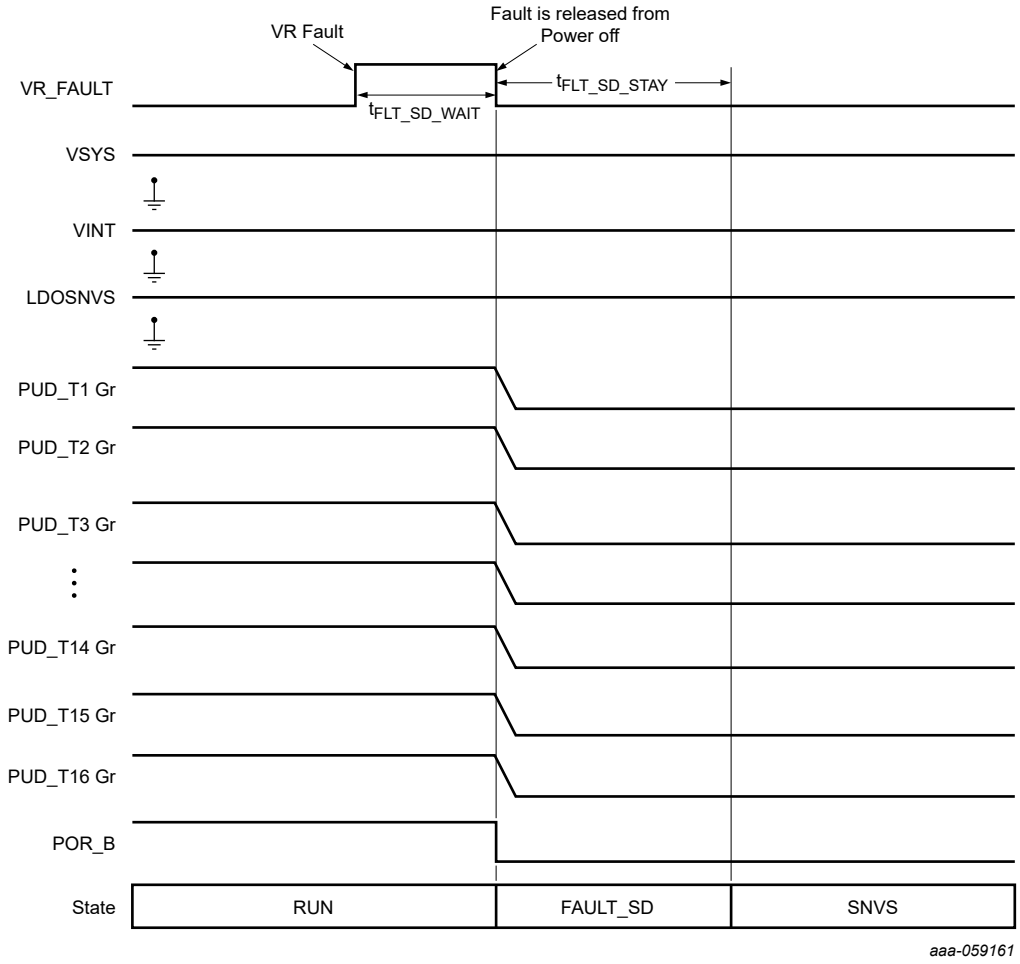


Figure 12. FAULT_SD from VR fault in RUN/STANDBY

Table 10. FAULT_SD description

Time	Description	Value	Comment
$t_{FLT\_SD\_WAIT}$	VR fault wait time to enter fault shutdown	100 ms	20 µs, 100 ms option
$t_{FLT\_SD\_STAY}$	Time to stay at Fault_SD state	100 ms	—

7.4 PMIC reset

The PF9453 PMIC has three reset inputs: the WDOG_B pin, the PMIC_RST_B pin and the I^2C reset bit. The reset is executed only at the RUN state.

Note: *The PMIC_RST_B pin is only available in the QFN package. If using the WLCSP package, omit PMIC_RST_B and use the WDOG_B pin as the default reset option*

The reset behavior is configured in the 0x08 RESET_CTRL register for the WDOG_B pin and the PMIC_RST_B pin. The I^2C reset behavior is configured in the 0x09 SW_RST register.

Table 11. PMIC reset description

0x08 – RESET_CTRL				Reset type S
Bit	**Name**	**Type**	**Reset**	**Description**
7:6	WDOG_B_CFG	R/W	00	When WDOG_B is asserted to L, PMIC behavior **00b = WDOG_B reset is disabled** 01b = Warm Reset, POR_B pin is asserted low for t_{RESET} 10b,11b = Cold Reset, all voltage regulators (except LDO_SNVS) are recycled
5:4	PMIC_RST_CFG	R/W	10	When PMIC_RST_B is asserted to L, PMIC behavior 00b = PMIC_RST_B reset is disabled 01b = Warm Reset, POR_B pin is asserted low for t_{RESET} **10b**, 11b **= Cold reset, all voltage regulators (except LDO_SNVS) are recycled**
0x09 – SW_RST				**Reset type O**
7:0	SW_RST_KEY	R/W	0x00	Software reset register. This register is read back to "0x00" right after writing the value. **0x00 = No action** 0x05 = Reset O-type registers to default value 0x09 = Reset O-type registers and S-type registers 0x14 = Cold reset (Power recycle all regulators except LDO_SNVS) 0x35 = Warm reset (Toggle POR_B for t_{RESET}) 0xEE = PMIC digital reset (debug purpose only) Others = Forbidden

When the WDOG_B pin is asserted low, the PF9453 gets reset depending on the WDOG_B_CFG bit configuration. When the bits are set to 2b00, the reset by the WDOG_B pin is disabled. If the bits are set to 2b01, Warm reset is performed, pulling POR_B low for t_{RESET} and reset I^2C O type registers to default values, keeping power rails remaining ON. After reset, the WDOG_B pin must be released high to get another reset from the WDOG_B falling edge.

When PMIC_RST_B is asserted low and stays low for RESETKEY timer configured in the SYS_CFG1 register, PF9453 waits for t_{RESET_WAIT} after issuing the RESETKEY interrupt. If the application processor does not disable reset by writing 00b in PMIC_RST_CFG bits, then the PF9453 gets reset depending on the PMIC_RST_CFG bits configuration. When the bits are set to 2b00, any reset by PMIC_RST_B pin is disabled. If the bits are set to 2b01, Warm Reset is performed, in which POR_B is pulled low for t_{RESET} and reset I^2C O type registers to default value, with power rails remaining ON. After reset, the PMIC_RST_B pin must be released high to get another reset from the PMIC_RST_B falling edge.

A Cold Reset event is generated by either I^2C reset, WDOG_B falling edge or PMIC_RST_B falling edge after debounce time. Once it is detected, POR_B is pulled low and takes the Power-down sequence. PF9453 stays at RESET for $t_{RESTART}$ and then starts the Power-on sequence even though the WDOG_B pin is still low.

Figure 13 shows Cold Reset behavior. From any Cold Reset signal from either PMIC_RST_B, WDOG_B or I^2C, it starts with the Power-down sequence and stays off for $t_{RESTART}$. It automatically proceeds to the Power-on sequence and then enters the RUN state. PMIC_ON_SRC is ignored for $t_{PWR\_HOLD\_RST}$ after entering the RUN state. If PMIC_ON_SRC does not come up until $t_{PWR\_HOLD\_RST}$ is expired, then PF9453 is turned off.

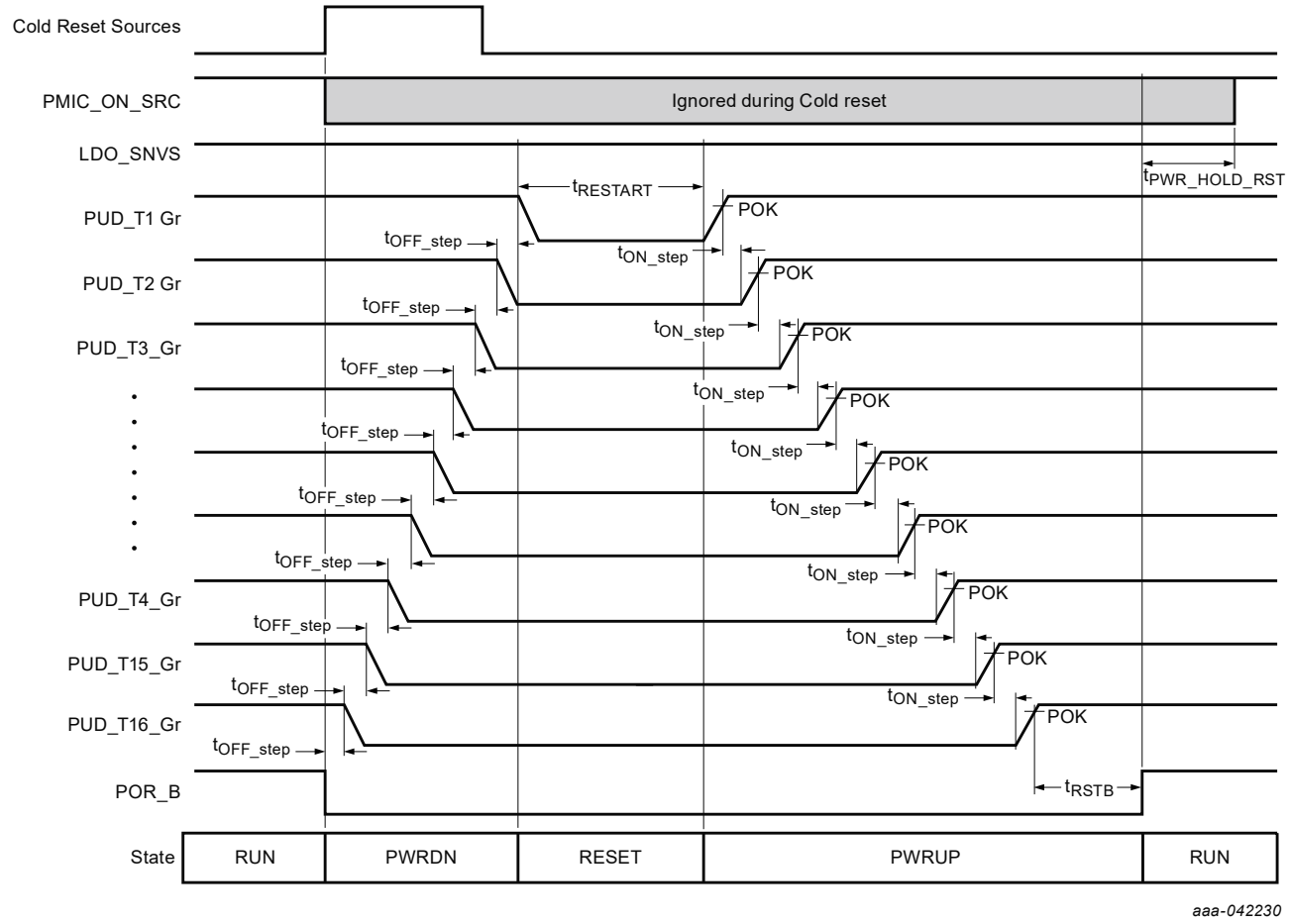


Figure 13. PF9453 cold reset

Table 12. PF9453 cold reset description

Time	Description	Value	Comment
$t_{RESTART}$	Time to Power-on sequence from end of Power-off sequence during Cold Reset	250 ms	–
$t_{PWR\_HOLD\_RST}$	Time to hold power-on after reset	100 ms	–

Figure 14 shows Warm Reset behavior. From any Warm Reset signal from either of PMIC_RST_B, WDOG_B or I^2C, POR_B toggles for t_{RESET} and all O type registers get reset. PMIC_ON_SRC is ignored for $t_{PWR\_HOLD\_RST}$ after entering the RUN state as in Cold Reset behavior.

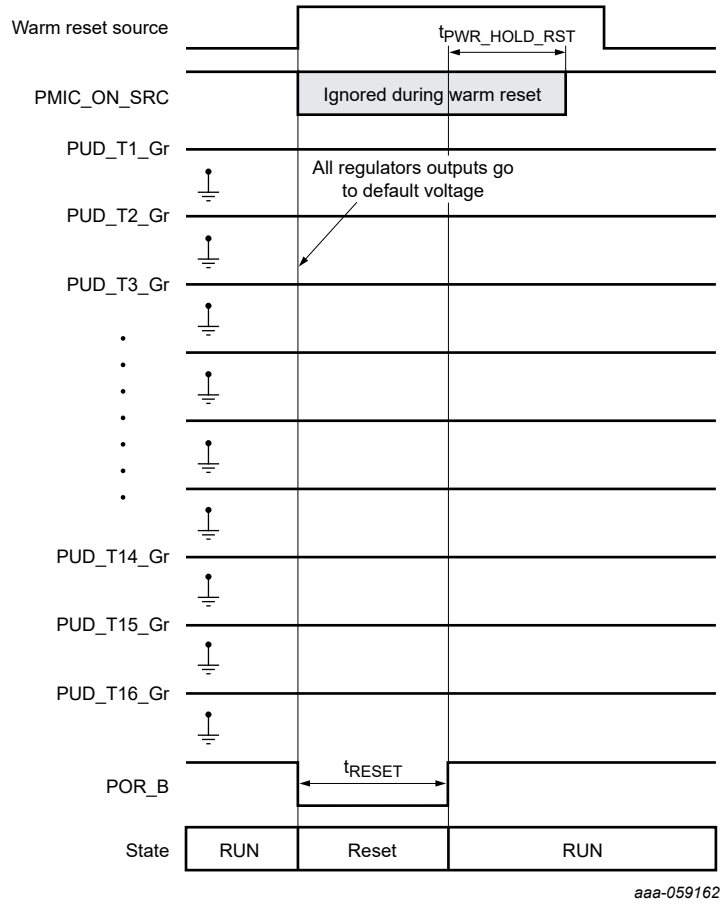


Figure 14. Warm reset

Table 13. Warm reset description

Time	Description	Value	Comment
t_{RESET}	POR_B low time at Warm Reset	20 ms	–

7.5 PMIC_RST_B configuration

The PMIC_RST_B pin is available only in the QFN package.

It is used either to power on the PF9453 from the SNVS state or to trigger a reset during the RUN state. When a falling edge is detected on this pin, the PMIC_RSTB_S status bit in the INT1_STATUS register is updated after a debounce period defined by the PMIC_RST_B_DEB bits (tDEB_PMIC_RST_B).

In the SNVS state, a falling edge on PMIC_RST_B—after the debounce time—starts the ONKEY timer (t_{ONKEY}), configured via the ONKEY_TIMER bits. Once the timer expires, the ONKEY_S status bit is set. If the pin is configured as a power-on source in the PWR_SEQ_CTRL register (PMIC_RST_B_ON bit), the PMIC_ON_SRC signal is generated, allowing the device to power up. This power-up behavior is applicable only in the SNVS state.

In the RUN state, a falling edge on PMIC_RST_B—after the debounce time—triggers the RESETKEY timer (tRESETKEY), configured via the RESETKEY_TIMER bits. Once the timer expires, the RESETKEY_S status bit is updated. After a delay (tRESET_WAIT), which allows the application processor (AP) to decide whether to proceed with the reset, and if the reset is enabled via the PMIC_RST_CFG bit, the reset is executed according to the configuration in the RESET_CTRL register.

The figure below illustrates the behavior of the PMIC_RST_B pin and the related configurable registers.

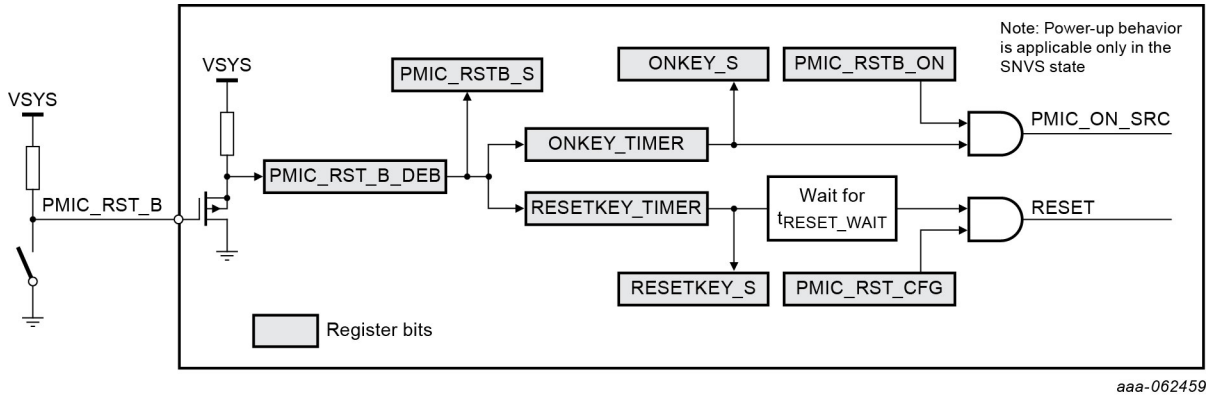


Figure 15. Regulator summary.

7.6 Regulator summary

The PF9453 PMIC features four high-efficiency low quiescent current buck regulators, two LDO regulators, for QFN package or one for WLCSP package, and a low Iq SNVS LDO to supply voltages for the application processor and peripheral devices.

7.6.1 Buck regulators

The PF9453 has four high-efficiency buck regulators. Each buck regulator features soft start and over-current protection. Buck regulators operate in two modes: pulse frequency modulation (PFM) and pulse width modulation (PWM) mode. Each buck regulator operates in PFM mode at a light load that generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shut down to achieve the lowest operating quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current.

In PFM, the switching frequency varies linearly with the load current. At medium and high load conditions, the device automatically enters PWM mode and operates in continuous conduction mode with a nominal switch frequency fsw of typically 2 MHz. The boundary between PWM and PFM mode is when the inductor current becomes discontinuous.

When the FPWM bit is set to "1", the buck regulator operates only in PWM mode regardless of load current.

An internal active discharge resistor is installed in each buck regulator output to discharge voltage on output capacitors when the regulator is off. It is configurable through an I^2C register.

Table 14 contains a summary of buck regulator information.

Table 14. PF9453 buck summary

Buck#	Input pin	Default VOUT [V]	VOUT range [V]	Step size [mV]	Default ON/ OFF	Current rating [mA]
BUCK1	INB12	1.1	0.6 - 3.775	25	ON	2000[1]
BUCK2	INB12	0.85	0.6 - 2.1875	12.5	ON	2700[1]
BUCK3	INB34	1.8	0.6 - 3.775	25	ON	2000[1]
BUCK4	INB34	3.3	0.6 - 3.775	25	ON	2500[1]

[1] Output current of PF9453 regulators changes depending on the part number; see Table 2.

7.6.1.1 ON/OFF control

Each buck regulator can be turned ON/OFF through the I^2C or PMIC_STBY_REQ pin, which can be configured in each of the Bx_ENMODE bits in the BUCKxCTRL register.

- BxENMODE = 00b: the buck regulator is forced OFF
- BxENMODE = 01b: the buck regulator is ON in RUN state (ACTIVE / STANDBY / DPSTANDBY mode)
- BxENMODE = 10b: the buck regulator is ON in ACTIVE or STANDBY mode and it is OFF in DPSTANDBY mode
- BxENMODE = 11b: the buck regulator is ON in ACTIVE mode and it is OFF in STANDBY or DPSTANDBY mode

7.6.1.2 Dynamic voltage scaling

BUCK2 supports dynamic voltage scaling (DVS) through the PMIC_STBY_REQ pin.

The BUCK2 regulator output voltage is determined by the BUCK2OUT and BUCK2OUT_STBY registers through the PMIC_STBY_REQ pin.

Figure 16 contains a DVS functional block diagram.

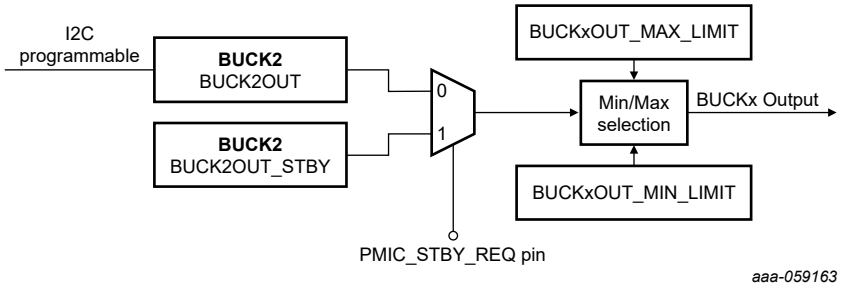


Figure 16. DVS functional diagram

The programmable voltage ramp-up and ramp-down are applied during the DVS voltage transition. The ramp rate is configured by the B2_RAMP bits in the BUCK2CTRL register.

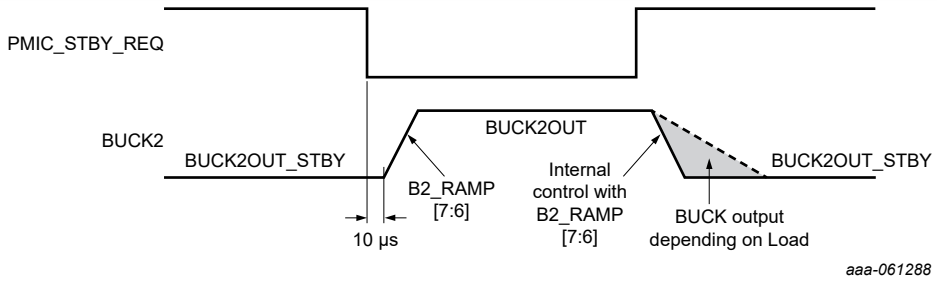


Figure 17. DVS timing

7.6.1.3 Overshoot improvement from PWM to PFM mode transient

The load transient response in PWM mode is improved compared to PFM mode, because the converter reacts faster on the load step and actively sinks energy on the load release. The PF9453 buck regulator automatically enters PWM mode for 16 cycles after a heavy load release to bring the output voltage back to the regulation level faster. After 16 cycles of PWM mode, the regulator automatically returns to PFM mode. Figure 18 shows this behavior.

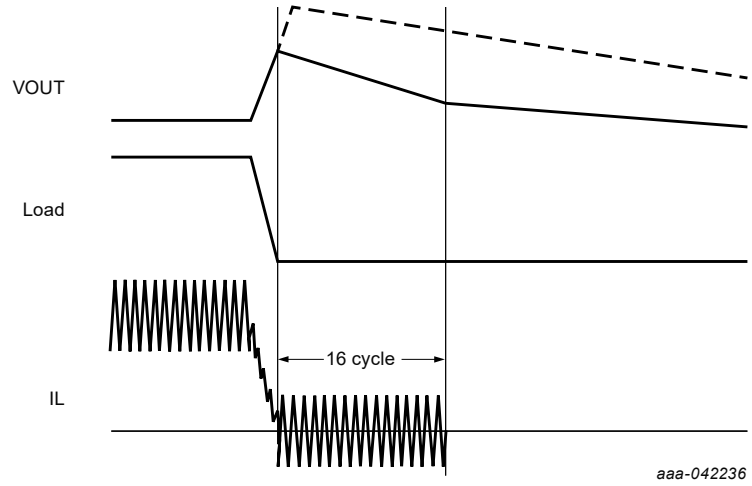


Figure 18. Overshoot improvement from PWM to PFM mode transient

7.6.1.4 Buck output limiting

An application processor may accidentally write a higher or lower voltage than the absolute maximum or minimum voltage rating of its power input. This may cause significant damage to the application processor. The PF9453 has registers to limit the maximum and minimum voltage to prevent such an incident (only available for the BUCK2).

The BUCK2 maximum / minimum outputs are limited by the BUCK2OUT_MAX_LIMIT and BUCK2OUT_MIN_LIMIT registers, respectively. Even if a buck output is configured to higher than the limit voltage configured in BUCK2OUT_MAX_LIMIT registers or lower than the limit voltage configured in BUCK2OUT_MIN_LIMIT registers, the actual buck output is clamped to the limiting voltage set by the BUCK2OUT_MAX_LIMIT or BUCK2OUT_MIN_LIMIT registers.

7.6.2 LDO

The PF9453 has up to three low quiescent LDOs, depending on the package. LDO_SVNS supplies the SNVS core in the application processor. This LDO features an ultralow quiescent current (0.4 µA typical), since it is always ON when VSYS is valid.

A designated active discharge resistor for each LDO is configurable through I^2C.

Table 15. LDO summary

LDO#	Input pin	Default VOUT (V)	VOUT range (V)	Step size (mV)	Default ON/ OFF	Current rating (mA)
LDO_SNVS	VSYS	1.8 V	1.2 to 3.4A	25	ON	10
LDO1	INL1	3.3 V / 1.8 V	0.8 to 3.3	25	ON	250
LDO2[1]	INL2	0.8 V	0.5 to 1.95	25	ON	200

[1] LDO2 is only available in QFN package.

7.6.3 32 kHz crystal oscillator driver

The PF9453 contains a crystal oscillator driver with an external load capacitor buffer referenced to the LDO_SNVS voltage. When VSYS exceeds the POR threshold and internal power VINT is good, the 32.768 kHz crystal oscillator starts oscillating. The crystal oscillator typically takes a few seconds to be stabilized.

The PF9453 CLK_32K_OUT buffer outputs a stable 32 kHz clock after t_{32K_EN} from VSYS_UVLO. The output buffer is disabled when the CLK_32K_DIS bit = 1b.

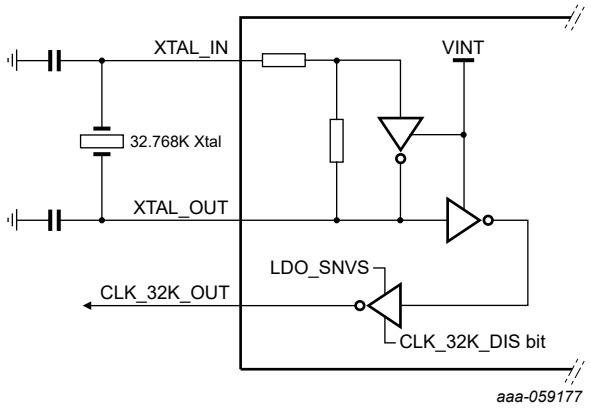


Figure 19. 32 kHz crystal oscillator driver block diagram

7.6.4 Load switch

The PF9453 integrates a 400 mA load switch which can supply the SD card VDD. LSWIN pin is typically connected to the BUCK4 output. The load switch is enabled by the LSW_EN pin or the LSW_EN[1:0] bits in the LSW_CTRL1 register. It has a soft-start feature to reduce inrush current during turn-on.

In the QFN package, the load switch includes overcurrent and short-circuit protection. These protections are not available in the WLCSP package, so additional external protection is recommended to prevent exceeding the maximum output current of the load switch.

In case of QFN package, this load switch has overcurrent protection and short-circuit protection implemented by monitoring the voltage difference between the LSWIN and LSWOUT pins. When the switch current exceeds the overcurrent threshold (I_{OC}) for overcurrent debounce time (t_{OC_DEB}), the LSW_OCP bit in the VRFLT1_INT register is set to 1 and the fault behavior is determined by the LSW_OC[1:0] bits configuration in the LSW_CTRL2 register. When the switch current exceeds the short-circuit current threshold (I_{SC}), the LSW_OCP bit in the VRFLT1_INT register is set to 1 and the switch is turned off immediately.

Note: *The OCP function was designed to support short-to-ground for a typical use case of an SD card. This circuit is sensitive to parasitic inductance. NXP recommends not connecting wires or any other components that may generate such inductance, as this could cause damage.*

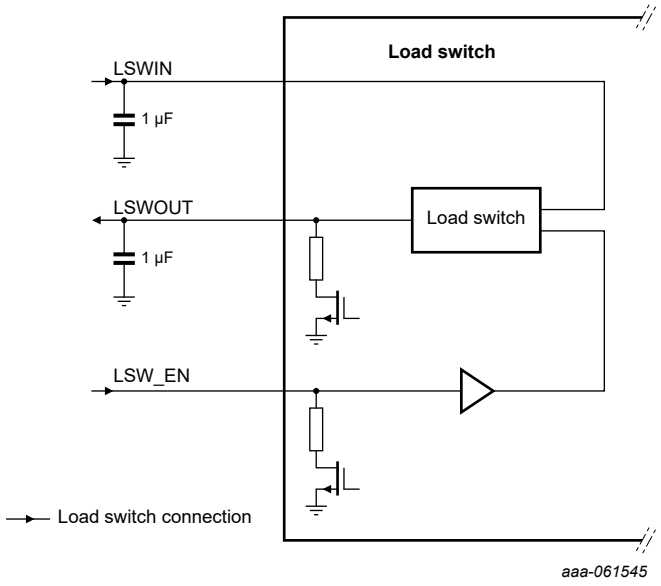


Figure 20. Load switch block diagram

7.6.5 Regulator protection register

Each regulator output voltage configuration register is protected by a lock key in the REG_LOCK register

An unlock key must be written in the 0x4E register before updating the registers, and registers can be read without an unlock key. Below is a list of the protected registers.

1. BUCK output configuration registers: BUCK1OUT, BUCK2OUT, BUCK3OUT, and BUCK4OUT.
2. BUCK2 min/max output configuration registers: BUCK2OUT_MAX_LIMIT, BUCK2OUT_MIN_LIMIT.
3. LDO output configuration registers: LDOSNVS_CFG1, LDO1_OUT_L, LDO1_OUT_H, and for QFN package the LDO2_OUT.

7.7 Interrupt management

The IRQ_B pin is an interface to the software-controlled system that indicates any interrupt bit status change in the INT1 register. The IRQ_B pin is pulled low when any unmasked interrupt bit status is changed, and it is released high once the application processor reads the INT1 register.

The INT1 bits are latched to 1 whenever a corresponding INT1_STATUS bit is changed and the latch is cleared when the INT1 register is read. The INT1_MASK bits are used to enable or disable individual interrupt bits of the INT1 register. The INT1_STATUS register indicates the status and is not latched.

Note: *Figure 21 shows the interrupt diagram for QFN package and Figure 22 shows the one for WLCSP package.*

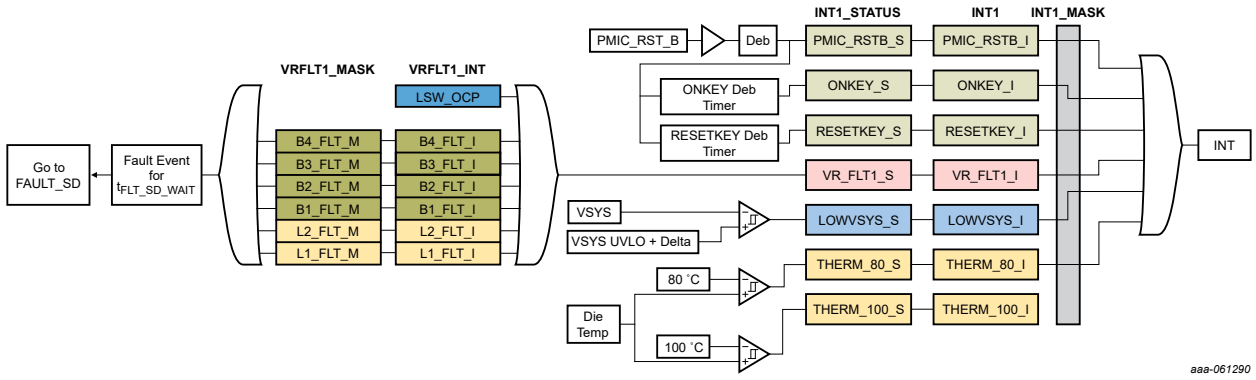


Figure 21. Interrupt diagram for QFN package

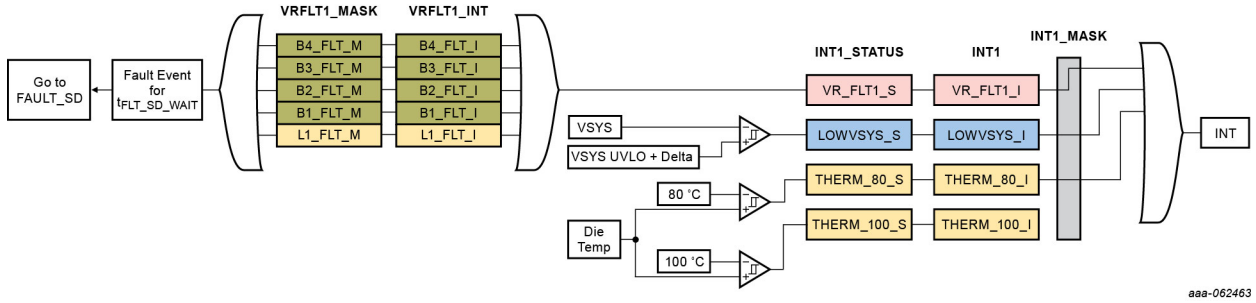


Figure 22. Interrupt diagram for WLCSP package

8 Software interface

The PF9453 implements an I^{2}C-bus target interface and it interfaces with the host system. The host processor can issue commands, monitor status and receive response through this bus. A detailed description of the I^{2}C-bus specification, with applications, is given in UM10204, C-bus specification and user manual [Ref. 4]. PF9453 supports I^{2}C-bus data transfers in standard-mode (100 kbit/s), fast-mode (400 kbit/s) and fast-mode plus (1 Mbit/s). See Table 16.

Table 16. I^{2}C address at Power-on Reset

OTP version	7-bit slave address	8-bit write address	8-bit read address
Default	0x32, 0b 011 0010	0x64, 0b 0110 0100	0x65, 0b 0110 0101
OTP1	0x33, 0b 011 0011	0x66, 0b 0110 0110	0x67, 0b 0110 0111
OTP2	0x36, 0b 011 0110	0x6C, 0b 0110 1100	0x6D, 0b 0110 1101
OTP3	0x37, 0b 011 0111	0x6E, 0b 0110 1110	0x6F, 0b 0110 1111

I^{2}C register reset type

Type S : (VSYS < V_{SYS_UVLO}) || (VINT_POK) || (SW_RST_KEY = 0x09)

Type O : (VSYS < V_{SYS_UVLO}) || (VINT_POK) || (Cold Reset) || (Warm Reset) || (falling edge of PMIC_ON_SRC) || (SW_RST_KEY=0X05) || (SW_RST_KEY=0x09) || (FAULT_SD) || (thermal SD)

8.1 Register map

Note: *Reserved registers are not shown in Table 17.*

Table 17. Register map

Add	Name	Description								R/W	Reset Type	QFN package reset value	WLCSP package reset value
		B7	B6	B5	B4	B3	B2	B1	B0				
01h	Device_ ID	CHIP_ID				REV_ID				R	S	0xB2	0x32
02h	INT1	RSVD	PMIC_ RSTB_I	ONKEY_I	RESETKEY_ I	VR_FLT1_I	LOWVSYS_ I	THERM_ 80_I	THERM_ 100_I	R/C	S	0x00	
03h	INT1_ MASK	RSVD	PMIC_ RSTB_M	ONKEY_M	RESETKEY_ M	VR_FLT1_M	LOWVSYS_ M	THERM_ 80_M	THERM_ 100_M	R/W	S	0xFF	
04h	INT1_ STATUS	RSVD	PMIC_ RSTB_S	ONKEY_S	RESETKEY_ S	VR_FLT1_S	LOWVSYS_ S	THERM_ 80_S	THERM_ 100_S	R	S	0x00	
05h	VRFLT1_ INT	LSW_OCP	RSVD	L2_FLT_I	L1_FLT_I	B4_FLT_I	B3_FLT_I	B2_FLT_I	B1_FLT_I	R/W/C	S	0x00	
06h	VRFLT1_ MASK	RSVD	RSVD	L2_FLT_M	L1_FLT_M	B4_FLT_M	B3_FLT_M	B2_FLT_M	B1_FLT_M	R/W	S	0xFF	
07h	PWR_ STATE	PWR_STAT				PWR_MODE				R	S	0x00	
08h	**RESET_ CTRL[1]**	**WDOG_B_CFG**		**PMIC_RST_CFG**		**TRESTART**	**RSVD**			**R/W**	**S**	**0x20**	
09h	SW_RST	SW_RST_KEY								R/W	O	0x00	
0Ah	**PWR_ SEQ_ CTRL[1]**	**PMIC_RST_ B_ON**	**RSVD**	**PMIC_RST_ B_DEB**	**RSVD**	**PSQ_TON_STEP**		**PSQ_TOFF_STEP**		**R/W**	**S**	**0x06**	
0Bh	SYS_ CFG1	LOW_VSYS		STANDBY_ CFG	RESETKEY_TIMER			TFLT_SD_ WAIT	THERM_ SD_DIS	R/W	O	0x54	
0Ch	**SYS_ CFG2[1]**	**ONKEY_TIMER**		**RSVD**			**POK_PU**	**VSYS_UVLO**		**R/W**	**S**	**0x71**	
0Dh	CLK_32 K_CFG	RSVD							CLK_32K_ DIS	R/W	O	0x00	
10h	**BUCK1 CTRL[1]**	**RSVD**				**B1_AD**	**B1_FPWM**	**B1_ENMODE**		**R/W**	**O**	**0x39**	
11h	**BUCK1 OUT[1]**	**RSVD**	**B1_OUT**							**R/W**	**O**	**0x14**	
14h	**BUCK2 CTRL[1]**	**B2_RAMP**		**RSVD**		**B2_AD**	**B2_FPWM**	**B2_ENMODE**		**R/W**	**O**	**0x79**	
15h	**BUCK2 OUT[1]**	**RSVD**	**B2_OUT**							**R/W**	**O**	**0x14**	
1Dh	BUCK2 OUT_ STBY	RSVD	B2_DVS_STBY							R/W	O	0x14	
1Fh	**BUCK2 OUT_ MAX_ LIMIT[1]**	**RSVD**	**B2_MAX_LIMIT**							**R/W**	**O**	**0x18**	
20h	**BUCK2 OUT_ MIN_ LIMIT[1]**	**RSVD**	**B2_MIN_LIMIT**							**R/W**	**O**	**0x01**	
21h	**BUCK3 CTRL[1]**	**RSVD**				**B3_AD**	**B3_FPWM**	**B3_ENMODE**		**R/W**	**O**	**0x39**	
22h	**BUCK3 OUT[1]**	**RSVD**	**B3_OUT**							**R/W**	**O**	**0x30**	
2Eh	**BUCK4 CTRL[1]**	**RSVD**				**B4_AD**	**B4_FPWM**	**B4_ENMODE**		**R/W**	**O**	**0x39**	
2Fh	**BUCK4 OUT[1]**	**RSVD**	**B4_OUT**							**R/W**	**O**	**0x6C**	
36h	**LDO1_ OUT_ L[1]**	**RSVD**	**L1_OUT_L**							**R/W**	**O**	**0x64**	**0x00**
37h	**LDO1_ CFG[1]**	**RSVD**		**L1_AD_SD_ VSEL**	**L1_AD**	**RSVD**		**L1_ENMODE**		**R/W**	**O**	**0x31**	
38h	**LDO1_ OUT_ H[1]**	**RSVD**	**L1_OUT_H**							**R/W**	**O**	**0x28**	**0x00**
39h	**LDOSNVS_ CFG1[1]**	**LSNVS_AD**	**L_SNVS_OUT**							**R/W**	**O**	**0x98**	**0xA8**

Table 17. Register map...*continued*

Add	Name	Description								R/W	Reset Type	QFN package reset value	WLCSP package reset value
		B7	B6	B5	B4	B3	B2	B1	B0				
3Ah	LDOSNVS_CFG2	RSVD							LS_ENMODE	R/W	O	0x01	
3Bh	**LDO2_CFG[1]**	**RSVD**	**L2_AD**	**L2_LLSEL**		**L2_CSEL**		**L2_ENMODE**		**R/W**	**O**	**0x59**	**0x11**
3Ch	**LDO2_OUT[1]**	**L2_INL2_MDET**	**L2_INL2_VSEL**	**L2_OUT**						**R/W**	**O**	**0x0C**	**0x11**
3Dh	**BUCK_POK_F_CFG[1]**	**BUCK4_POK_F**		**BUCK3_POK_F**		**BUCK2_POK_F**		**BUCK1_POK_F**		**R/W**	**O**	**0x00**	
40h	**LSW_CTRL1[1]**	**RSVD**			**LSW_AD**	**RSVD**		**LSW_EN**		**R/W**	**O**	**0x11**	
41h	LSW_CTRL2	RSVD						LSW_SC	LSW_OC	R/W	O	0x01	0x00
4Eh	REG_LOCK	UNLOCK_KEY								R/W	O	0x00	

- **Green:** Bits available in QFN and WLCSP
- **Yellow:** Bits not available in WLCSP
- ***Bold:*** OTP configurable registers

8.2 Register details

8.2.1 Device_ID

The device identification code stores a unique identifier for each version and/or revision of a PF9453, so that the connected processor recognizes it automatically.

Table 18. Device_ID register (address 01h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CHIP_ID				CHIP_REV			
QFN reset	1	0	1	1	0	0	1	0
WLCSP reset	0	0	1	1	0	0	1	0
Access	R	R	R	R	R	R	R	R

Table 19. Device_ID register (address 01h) bit descriptions

Bit	Symbol	Description
7 to 4	CHIP_ID	Chip ID **1011 —** PF9453 QFN (default) **0011 —** PF9463 WLCSP (default)
3 to 0	CHIP_REV	Chip Revision **0000 —** revision 0 **0010 —** revision 2 (default)

8.2.2 INT1

The interrupt source register (INT1) bits are latched to 1 whenever corresponding INT1_STATUS bit is changed and the latch is cleared when the INT1 register is read. This register is **Read** and **Clear**. PMIC_RSTB_I, ONKEY_I and RESETKEY_I bits are not available in WLCSP package.

Table 20. INT1 register (address 02h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD	PMIC_RSTB_I	ONKEY_I	RESETKEY_I	VR_FLT1_I	LOWVSYS_I	THERM_80_I	THERM_100_I
Reset	0	0	0	0	0	0	0	0
Access	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C

Table 21. INT1 register (address 02h) bit descriptions

Bit	Symbol	Description
7	RSVD	Reserved
6	PMIC_RSTB_I	PMIC_RSTB_I interrupt **0 —** PMIC_RSTB_S bit has not been changed (default) **1 —** PMIC_RSTB_S bit has been changed
5	ONKEY_I	ON Key timer interrupt **0 —** ONKEY_S bit has not been changed (default) **1 —** ONKEY_S bit has been changed
4	RESETKEY_I	RESET Key timer interrupt **0 —** RESETKEY_S bit has not been changed (default) **1 —** RESETKEY_S bit has been changed
3	VR_FLT1_I	Voltage regulator Group1 Fault **0 —** VR_FLT1_S bit has not been changed (default) **1 —** VR_FLT1_S bit has been changed
2	LOWVSYS_I	Low VSYS Voltage interrupt **0 —** LOWVSYS_S bit has not been changed (default) **1 —** LOWVSYS_S bit has been changed
1	THERM_80_I	Die temperature 80 °C interrupt **0 —** THERM_80_S bit has not been changed (default) **1 —** THERM_80_S bit has been changed
0	THERM_100_I	Die temperature 100 °C interrupt **0 —** THERM_100_S bit has not been changed (default) **1 —** THERM_100_S bit has been changed

8.2.3 INT1_MASK

The INT1_MASK bits are used to enable or disable individual interrupt bits of INT1 register. If any bit in INT1 register is set to 1 and the corresponding bit is enable in INT1_MASK then the IRQ_B pin is pulled to low. PMIC_RSTB_M, ONKEY_M and RESETKEY_M bits are not available in WLCSP package.

Table 22. INT1_MASK register (address 03h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD	PMIC_RSTB_M	ONKEY_M	RESETKEY_M	VR_FLT1_M	LOWVSYS_M	THERM_80_M	THERM_100_M
Reset	1	1	1	1	1	1	1	1

Table 22. INT1_MASK register (address 03h) bit allocation*...continued*

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 23. INT1_MASK register (address 03h) bit descriptions

Bit	Symbol	Description
7	RSVD	Reserved
6	PMIC_RSTB_M	PMIC_RSTB_I interrupt mask bit **—** Enable PMIC_RSTB_I interrupt **—** Mask PMIC_RSTB_I interrupt (default)
5	ONKEY_M	ONKEY_I interrupt mask bit **0 —** Enable ONKEY_I interrupt **1 —** Mask ONKEY_I interrupt (default)
4	RESETKEY_M	RESETKEY_I interrupt mask bit **0 —** Enable RESETKEY_I interrupt **1 —** Mask RESETKEY_I interrupt (default)
3	VR_FLT1_M	VR_FLT1_I interrupt mask bit **0 —** Enable VR_FLT1_I interrupt **1 —** Mask VR_FLT1_I interrupt (default)
2	LOWVSYS_M	LOWVSYS_I interrupt mask bit **0 —** Enable LOWVSYS_I interrupt **1 —** Mask LOWVSYS_I interrupt (default)
1	THERM_80_M	THERM_80_I interrupt mask bit **0 —** Enable THERM_80_I interrupt **1 —** Mask THERM_80_I interrupt (default)
0	THERM_100_M	THERM_100_I interrupt mask bit **0 —** Enable THERM_100_I interrupt **1 —** Mask THERM_100_I interrupt (default)

8.2.4 INT1_STATUS

The STATUS register shows current status. Any status bit change sets the corresponding interrupt bit to 1 in INT1 register. PMIC_RSTB_S, ONKEY_S and RESETKEY_S bits are not available in WLCSP package.

Table 24. INT1_STATUS register (address 04h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD	PMIC_RSTB_S	ONKEY_S	RESETKEY_S	VR_FLT1_S	LOWVSYS_S	THERM_80_S	THERM_100_S
Reset	—	—	—	—	—	—	—	—
Access	R	R	R	R	R	R	R	R

Table 25. INT1_STATUS register (address 04h) bit descriptions

Bit	Symbol	Description
7	RSVD	Reserved
6	PMIC_RSTB_S	PMIC_RST_B pin status **0 —** PMIC_RST_B pin is low

Table 25. INT1_STATUS register (address 04h) bit descriptions*...continued*

Bit	Symbol	Description
		1 — PMIC_RST_B pin is high
5	ONKEY_S	ONKEY status bit **0 —** PMIC_RST_B pin is not low for ONKEY timer **1 —** PMIC_RST_B pin is low for ONKEY timer
4	RESETKEY_S	RESETKEY status bit **0 —** PMIC_RST_B pin is not low for RESETKEY timer **1 —** PMIC_RST_B pin is low for RESETKEY timer
3	VR_FLT1_S	Voltage Regulator Fault status **0 —** All voltage regulators are OK **1 —** Either of voltage regulators is in Fault state
2	LOWVSYS_S	VSYS low voltage status **0 —** VSYS is above Low VSYS threshold (V_{LOW_VSYS}) + V_{SYS_UVLO} **1 —** VSYS is below Low VSYS threshold (V_{LOW_VSYS}) + V_{SYS_UVLO}
1	THERM_80_S	Die temperature 80 °C statue **0 —** Die temperature is below 80 °C **1 —** Die temperature is above 80 °C
0	THERM_100_S	Die temperature 100 °C statue **0 —** Die temperature is below 100 °C **1 —** Die temperature is above 100 °C

8.2.5 VRFLT1_INT

Voltage regulator fault interrupt register. The bits corresponding to each regulator in this register are set to 1 when it is detected that the regulators (except LDO_SNVS) experienced a fault. If "1" is overwritten, the corresponding bit is newly updated by the current status. LSW_OCP and L2_FLT_I bits are not available in WLCSP package.

Table 26. VRFLT1_INT register (address 05h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	LSW_OCP	RSVD	L2_FLT_I	L1_FLT_I	B4_FLT_I	B3_FLT_I	B2_FLT_I	B1_FLT_I
Reset	0	0	0	0	0	0	0	0
Access	R/W/C	R/W/C	R/W/C	R/W/C	R/W/C	R/W/C	R/W/C	R/W/C

Table 27. VRFLT1_INT register (address 05h) bit descriptions

Bit	Symbol	Description
7	LSW_OCP	Load SW OCP interrupt, deglitched with t_{OC_DEB} **0 —** Load SW doesn't exceed current limit or is OFF (default) **1 —** Load SW exceeded current limit
6	RSVD	Reserved
5	L2_FLT_I	LDO2 Fault interrupt, deglitched with t_{DEB_POKB} **0 —** LDO2 output is good or LDO2 is OFF (default) **1 —** LDO2 output falls below 90 % of target
4	L1_FLT_I	LDO1 Fault interrupt, deglitched with t_{DEB_POKB}

Table 27. VRFLT1_INT register (address 05h) bit descriptions*...continued*

Bit	Symbol	Description
		0 — LDO1 output is good or LDO1 is OFF (default) **1 —** LDO1 output falls below 90 % of target
3	B4_FLT_I	BUCK4 Fault interrupt, deglitched with t_{DEB_POKB} **0 —** BUCK4 output is good or BUCK4 is OFF (default) **1 —** BUCK4 output falls below POK threshold set by BUCK4_POK_F[1:0]
2	B3_FLT_I	BUCK3 Fault interrupt, deglitched with t_{DEB_POKB} **0 —** BUCK3 output is good or BUCK3 is OFF (default) **1 —** BUCK3 output falls below POK threshold set by BUCK3_POK_F[1:0]
1	B2_FLT_I	BUCK2 Fault interrupt, deglitched with t_{DEB_POKB} **0 —** BUCK2 output is good or BUCK2 is OFF (default) **1 —** BUCK2 output falls below POK threshold set by BUCK2_POK_F[1:0]
0	B1_FLT_I	BUCK1 Fault interrupt, deglitched with t_{DEB_POKB} **0 —** BUCK1 output is good or BUCK1 is OFF (default) **1 —** BUCK1 output falls below POK threshold set by BUCK1_POK_F[1:0]

8.2.6 VRFLT1_MASK

VR fault mask bit. Once the bit is masked, the PF9453 does not enter Fault shutdown even if a fault condition of the corresponding regulator happens. L2_FLT_M bit is not available in WLCSP package.

Table 28. VRFLT1_MASK register (address 06h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD	RSVD	L2_FLT_M	L1_FLT_M	B4_FLT_M	B3_FLT_M	B2_FLT_M	B1_FLT_M
Reset	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 29. VRFLT1_MASK register (address 06h) bit descriptions

Bit	Symbol	Description
7	RSVD	Reserved
6	RSVD	Reserved
5	L2_FLT_M	LDO2 FLT mask **0 —** Unmasked **1 —** Masked (default)
4	L1_FLT_M	LDO1 FLT mask **0 —** Unmasked **1 —** Masked (default)
3	B4_FLT_M	BUCK4 FLT mask **0 —** Unmasked **1 —** Masked (default)
2	B3_FLT_M	BUCK3 FLT mask **0 —** Unmasked **1 —** Masked (default)

Table 29. VRFLT1_MASK register (address 06h) bit descriptions*...continued*

Bit	Symbol	Description
1	B2_FLT_M	BUCK2 FLT mask **0 —** Unmasked **1 —** Masked (default)
0	B1_FLT_M	BUCK1 FLT mask **0 —** Unmasked **1 —** Masked (default)

8.2.7 PWR_STATE

The power state register shows current PF9453 power states and modes.

Table 30. PWR_STATE register (address 07h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	PWR_STAT				PWR_MODE			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 31. PWR_STATE register (address 07h) bit descriptions

Bit	Symbol	Description
7 to 4	PWR_STAT	Current PF9453 STATES **0000 —** OFF (default) **0100 —** SNVS **0101 —** PWRUP **1000 —** RUN **1100 —** PWRDN **1110 —** FAULT_SD **others —** Reserved
3 to 0	PWR_MODE	Current PF9453 MODE, only effective at RUN state **0000 —** Active mode – DVS0 (default) **1000 —** STANDBY MODE **1010 —** DP_STANDBYMODE **others —** Reserved

8.2.8 RESET_CTRL

Reset behavior configuration register. OTP programmable register. PMIC_RST_CFG bits are not available in WLCSP package.

Table 32. RESET_CTRL register (address 08h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WDOG_B_CFG		PMIC_RST_CFG		TRESTART	RSVD		
Reset	0	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 33. RESET_CTRL register (address 08h) bit descriptions

Bit	Symbol	Description
7 to 6	WDOG_B_CFG	When WDOG_B is asserted to low, PMIC reset behavior **0 —** WDOG_B reset is disabled (default) **1 —** Warm reset, POR_B pin is asserted low for tRSTB **10 and 11 —** Cold Reset, all voltage regulators are recycled, except LDO_SNVS.
5 to 4	PMIC_RST_CFG	When PMIC_RST_B is asserted to low, PMIC reset behavior **0 —** PMIC_RST_B reset is disabled **1 —** Warm Reset, POR_B pin is asserted low for tRSTB **10 and 11 —** Cold Reset, all voltage regulators are recycled (default), except LDO_SNVS.
3	TRESTART	Time to stay regulators off during Cold Reset **0 —** 250 ms (default) **1 —** 500 ms
2 to 0	RSVD	Reserved

8.2.9 SW_RST

Software reset register.

Table 34. SW_RST register (address 09h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SW_RST_KEY							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 35. SW_RST register (address 09h) bit descriptions

Bit	Symbol	Description
7 to 0	SW_RST_KEY	Software reset register. This register is read back to “0x00” right after writing the value. **0000 0000 —** No action (default) **0000 0101 —** Reset O-type registers to default value **0000 1001 —** Reset O-type registers and S-type registers **0001 0100 —** Cold Reset (power recycle all regulators) **0011 0101 —** Warm Reset (toggle POR_B for 20 ms) **1110 1110 —** PMIC digital reset (debug purposes only) **others —** Forbidden

8.2.10 PWR_SEQ_CTRL

Debounce timer configuration register. OTP programmable register. PMIC_RST_B_ON and PMIC_RST_B_DEB bits are not available in WLCSP package.

Table 36. PWR_SEQ_CTRL register (address 0Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	PMIC_RST_B_ON	RSVD	PMIC_RST_B_DEB	RSVD	PSQ_TON_STEP		PSQ_TOFF_STEP	
Reset	0	0	0	0	0	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 37. PWR_SEQ_CTRL register (address 0Ah) bit descriptions

Bit	Symbol	Description
7	PMIC_RST_B_ON	Configure PMIC_RST_B pin as Power ON source **0 —** Mask (default) **1 —** Power ON Source
6	RSVD	Reserved
5	PMIC_RST_B_DEB	Debounce time for PMIC_RST_B pin for falling edge. (rising edge doesn't have debounce time) **0 —** 20 ms (default) **1 —** 100 ms
4	RSVD	Reserved
3 to 2	PSQ_TON_STEP	Time step configuration during power on sequence **00 —** 1 ms **01 —** 2 ms (default) **10 —** 4 ms **11 —** 8 ms
1 to 0	PSQ_TOFF_STEP	Time step configuration during power down sequence **00 —** 2 ms **01 —** 4 ms **10 —** 8 ms (default) **11 —** 16 ms

8.2.11 SYS_CFG1

Systems 1 configuration register. RESETKEY_TIMER bits are not available in WLCSP package.

Table 38. SYS_CFG1 register (address 0Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	LOW_VSYS		STANDBY_CFG	RESETKEY_TIMER			TFLT_SD_WAIT	THERM_SD_DIS
Reset	0	1	0	1	0	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 39. SYS_CFG1 register (address 0Bh) bit descriptions

Bit	Symbol	Description
7 to 6	LOW_VSYS	Low VSYS threshold above V_{SYS_UVLO} **00 —** 100 mV **01 —** 200 mV (default) **10 —** 300 mV **11 —** 400 mV
5	STANDBY_CFG	Mode configuration bit when PMIC_STBY_REQ pin is High **0 —** STANDBY mode (default) **1 —** DPSTANDBY mode
4 to 2	RESETKEY_TIMER	RESETKEY timer configuration after PMIC_RST_B pin falls low **000 —** 100 ms **001 —** 1 sec **10 —** 2 sec **11 —** 4 sec **100 —** 6 sec **101 —** 8 sec (default) **110 —** 10 sec **111 —** 12 sec
1	TFLT_SD_WAIT	Wait time for AP action when regulator fault occurs **0 —** 100 ms (default) **1 —** 20 µs
0	THERM_SD_DIS	Thermal shutdown disable bit **0 —** Enable Thermal shutdown (default)

Table 39. SYS_CFG1 register (address 0Bh) bit descriptions*...continued*

Bit	Symbol	Description
		1 — Disable Thermal shutdown

8.2.12 SYS_CFG2

ONKEY timer and VSYS UVLO configuration register. OTP programmable register. ONKEY_TIMER bits are not available in WLCSP package.

Table 40. SYS_CFG2 register (address 0Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ONKEY_TIMER		RSVD		RSVD	POK_PU	VSYS_UVLO	
Reset	0	1	1	1	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 41. SYS_CFG2 register (address 0Ch) bit descriptions

Bit	Symbol	Description
7 to 6	ONKEY_TIMER	ONKEY timer configuration after PMIC_RST_B pin falls low **00 —** 1 sec **01 —** 2 sec (default) **10 —** 4 sec **11 —** 8 sec
5 to 4	RSVD	Reserved
3	RSVD	Reserved
2	POK_PU	POK reference during power up **0 —** POK is reference to turn on next power group (default) **1 —** POK is ignored during power up
1 to 0	VSYS_UVLO	VSYS UVLO threshold, rising threshold **00 —** 2.65 V **01 —** 2.85 V (default) **10 —** 3.0 V **11 —** 3.3 V

8.2.13 CLK_32K_CFG

Crystal driver configuration register.

Table 42. CLK_32K_CFG register (address 0Dh) bit allocation crystal driver configuration register

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD							CLK_32K_DIS
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 43. CLK_32K_CFG register (address 0Dh) bit descriptions

Bit	Symbol	Description
7 to 1	RSVD	Reserved
0	CLK_32K_DIS	**0 —** Enable 32.768 kHz crystal oscillator driver output buffer (default) **1 —** Disable 32.768 kHz crystal oscillator driver output buffer

8.2.14 BUCK1CTRL

BUCK1 control register for active discharge, FPWM and Enable. OTP programmable register.

Table 44. BUCK1CTRL register (address 10h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD		RSVD		B1_AD	B1_FPWM	B1_ENMODE	
Reset	0	0	1	1	1	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 45. BUCK1CTRL register (address 10h) bit descriptions

Bit	Symbol	Description
7 to 6	RSVD	Reserved
5 to 4	RSVD	Reserved
3	B1_AD	Buck1 Active discharge **0 —** Always disable Active discharge resistor **1 —** Enable Active discharge resistor when regulator is OFF (default)
2	B1_FPWM	Forced PWM mode **0 —** Automatic PFM and PWM mode transition (default) **1 —** Forced PWM mode
1 to 0	B1_ENMODE	Buck1 enable mode **00 —** OFF **01 —** ON at RUN State (default) **10 —** ON at ACTIVE mode or STANDBY mode, OFF at DPSTANDBY **11 —** ON at ACTIVE mode, OFF at STANDBY or DPSTANDBY

8.2.15 BUCK1OUT

BUCK1 output voltage configuration register. This register is protected by lock key; 0x4E register should be written with unlock key before updating this register. OTP programmable register.

Table 46. BUCK1OUT register (address 11h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD	B1_OUT						
Reset	0	0	0	1	0	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 47. BUCK1OUT register (address 11h) bit descriptions

Bit	Symbol	Description
7	RSVD	Reserved
6 to 0	B1_OUT	BUCK1 Output voltage Programmable from 0.60 V to 3.775 V in 25 mV steps **001 0100 —** 1.1 V (default, based on OTP configuration A1) See Table 67

8.2.16 BUCK2CTRL

BUCK2 control register for ramp, DVS control, active discharge, FPWM and enable. OTP programmable register.

Table 48. BUCK2CTRL register (address 14h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	B2_RAMP		RSVD		B2_AD	B2_FPWM	B2_ENMODE	
Reset	0	1	1	1	1	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 49. BUCK2CTRL register (address 14h) bit descriptions

Bit	Symbol	Description
7 to 6	B2_RAMP	BUCK2 DVS speed 00 — 25 mV / 1 µs 01 — 25 mV / 2 µs (default) 10 — 25 mV / 4 µs 11 — 25 mV / 8 µs
5 to 4	RSVD	Reserved
3	B2_AD	BUCK2 Active discharge **0 —** Always disable Active discharge resistor **1 —** Enable Active discharge resistor when regulator is OFF (default)
2	B2_FPWM	Forced PWM mode **0 —** Automatic PFM and PWM mode transition (default) **1 —** Forced PWM mode
1 to 0	B2_ENMODE	BUCK2 enable mode **00 —** OFF **01 —** ON at RUN State (default) **10 —** ON at ACTIVE mode or STANDBY mode, OFF at DPSTANDBY **11 —** ON at ACTIVE mode, OFF at STANDBY or DPSTANDBY

8.2.17 BUCK2OUT

BUCK2 DVS output voltage when PMIC_STBY_REQ = L. This register is protected by lock key; 0x4E register should be written with unlock key before updating this register. OTP programmable register.

Table 50. BUCK2OUT register (address 15h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD	B2_OUT						

Table 50. BUCK2OUT register (address 15h) bit allocation...*continued*

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	1	0	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 51. BUCK2OUT register (address 15h) bit descriptions

Bit	Symbol	Description
7	RSVD	Reserved
6 to 0	B2_OUT	BUCK2 Output voltage Programmable from 0.60 V to 2.1875 V in 12.5 mV steps **001 0100 —** 0.85 V (default, based on OTP configuration A1) See Table 66

8.2.18 BUCK2OUT_STBY

BUCK2 DVS output voltage, PMIC_STBY_REQ = H.

Table 52. BUCK2OUT_STBY register (address 1Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD	B2_DVS_STBY						
Reset	0	0	0	1	0	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 53. BUCK2OUT_STBY register (address 1Dh) bit descriptions

Bit	Symbol	Description
7	RSVD	Reserved
6 to 0	B2_DVS_STBY	BUCK2 Output voltage at Standby mode Programmable from 0.60 V to 2.1875 V in 12.5 mV steps **001 0100 —** 0.85 V (default) See Table 66

8.2.19 BUCK2OUT_MAX_LIMIT

BUCK2 output voltage max limit register. This register is protected by lock key; 0x4E register should be written with unlock key before updating this register. OTP programmable register.

Table 54. BUCK2OUT_MAX_LIMIT register (address 1Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD	B2_MAX_LIMIT						
Reset	0	0	0	1	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 55. BUCK2OUT_MAX_LIMIT register (address 1Fh) bit descriptions

Bit	Symbol	Description
7	RSVD	Reserved
6 to 0	B2_MAX_LIMIT	BUCK2 output voltage maximum limit Programmable from 0.60 V to 2.1875 V in 12.5 mV steps **001 1000 —** 0.90 V (default, based on OTP configuration A1) See Table 66

8.2.20 BUCK2OUT_MIN_LIMIT

BUCK2 output voltage lower limit register. This register is protected by lock key; 0x4E register should be written with unlock key before updating this register. OTP programmable register.

Table 56. BUCK2OUT_MIN_LIMIT register (address 20h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD	B2_MIN_LIMIT						
Reset	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 57. BUCK2OUT_MIN_LIMIT register (address 20h) bit descriptions

Bit	Symbol	Description
7	RSVD	Reserved
6 to 0	B2_MIN_LIMIT	BUCK2 output voltage minimum limit Programmable from 0.60 V to 2.1875 V in 12.5 mV steps **000 0001 —** 0.6125 V (default, based on OTP configuration A1) See Table 66

8.2.21 BUCK3CTRL

BUCK3 control register for active discharge, FPWM and enable. OTP programmable register.

Table 58. BUCK3CTRL register (address 21h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD		RSVD		B3_AD	B3_FPWM	B3_ENMODE	
Reset	0	0	1	1	1	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 59. BUCK3CTRL register (address 21h) bit descriptions

Bit	Symbol	Description
7 to 6	RSVD	Reserved
5 to 4	RSVD	Reserved
3	B3_AD	BUCK3 Active discharge **0 —** Always disable Active discharge resistor **1 —** Enable Active discharge resistor when regulator is OFF (default)

Table 59. BUCK3CTRL register (address 21h) bit descriptions...*continued*

Bit	Symbol	Description
2	B3_FPWM	Forced PWM mode **0 —** Automatic PFM and PWM mode transition (default) **1 —** Forced PWM mode
1 to 0	B3_ENMODE	BUCK3 enable mode **00 —** OFF **01 —** ON at RUN State (default) **10 —** ON at ACTIVE mode or STANDBY mode, OFF at DPSTANDBY **11 —** ON at ACTIVE mode, OFF at STANDBY or DPSTANDBY

8.2.22 BUCK3OUT

BUCK3 output voltage configuration register. This register is protected by lock key; 0x4E register should be written with unlock key before updating this register. OTP programmable register.

Table 60. BUCK3OUT register (address 22h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD	B3_OUT						
Reset	0	0	1	1	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 61. BUCK3OUT register (address 22h) bit descriptions

Bit	Symbol	Description
7	RSVD	Reserved
7 to 0	B3_OUT	BUCK3 Output voltage Programmable from 0.60 V to 3.775 V in 25 mV steps **011 0000 —** 1.8 V (default, based on OTP configuration A1) See Table 67

8.2.23 BUCK4CTRL

BUCK4 control register for Active discharge, FPWM and Enable. OTP programmable register.

Table 62. BUCK4CTRL register (address 2Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD		RSVD		B4_AD	B4_FPWM	B4_ENMODE	
Reset	0	0	1	1	1	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 63. BUCK4CTRL register (address 2Eh) bit descriptions

Bit	Symbol	Description
7 to 6	RSVD	Reserved
5 to 4	RSVD	Reserved

Table 63. BUCK4CTRL register (address 2Eh) bit descriptions*...continued*

Bit	Symbol	Description
3	B4_AD	Buck4 Active discharge **0 —** Always disable Active discharge resistor **1 —** Enable Active discharge resistor when regulator is OFF (default)
2	B4_FPWM	Forced PWM mode **0 —** Automatic PFM and PWM mode transition (default) **1 —** Forced PWM mode
1 to 0	B4_ENMODE	Buck4 enable mode **00 —** OFF **01 —** ON at RUN State (default) **10 —** ON at ACTIVE mode or STANDBY mode, OFF at DPSTANDBY **11 —** ON at ACTIVE mode, OFF at STANDBY or DPSTANDBY

8.2.24 BUCK4OUT

BUCK4 output voltage configuration register. This register is protected by Lock key; 0x4E register should be written with unlock key before updating this register. OTP programmable register.

Table 64. BUCK4OUT register (address 2Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD	B4_OUT						
Reset	0	1	1	0	1	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 65. BUCK4OUT register (address 2Fh) bit descriptions

Bit	Symbol	Description
7	RSVD	Reserved
6 to 0	B4_OUT	BUCK4 Output voltage Programmable from 0.60 V to 3.775 V in 25 mV steps **110 1100 —** 3.3 V (default, based on OTP configuration A1) See Table 67

Table 66. BUCK2 output voltage table

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
0x00	0.6000 V	0x20	1.0000 V	0x40	1.4000 V	0x60	1.8000 V
0x01	0.6125 V	0x21	1.0125 V	0x41	1.4125 V	0x61	1.8125 V
0x02	0.6250 V	0x22	1.0250 V	0x42	1.4250 V	0x62	1.8250 V
0x03	0.6375 V	0x23	1.0375 V	0x43	1.4375 V	0x63	1.8375 V
0x04	0.6500 V	0x24	1.0500 V	0x44	1.4500 V	0x64	1.8500 V
0x05	0.6625 V	0x25	1.0625 V	0x45	1.4625 V	0x65	1.8625 V
0x06	0.6750 V	0x26	1.0750 V	0x46	1.4750 V	0x66	1.8750 V

Table 66. BUCK2 output voltage table*...continued*

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
0x07	0.6875 V	0x27	1.0875 V	0x47	1.4875 V	0x67	1.8875 V
0x08	0.7000 V	0x28	1.1000 V	0x48	1.5000 V	0x68	1.9000 V
0x09	0.7125 V	0x29	1.1125 V	0x49	1.5125 V	0x69	1.9125 V
0x0A	0.7250 V	0x2A	1.1250 V	0x4A	1.5250 V	0x6A	1.9250 V
0x0B	0.7375 V	0x2B	1.1375 V	0x4B	1.5375 V	0x6B	1.9375 V
0x0C	0.7500 V	0x2C	1.1500 V	0x4C	1.5500 V	0x6C	1.9500 V
0x0D	0.7625 V	0x2D	1.1625 V	0x4D	1.5625 V	0x6D	1.9625 V
0x0E	0.7750 V	0x2E	1.1750 V	0x4E	1.5750 V	0x6E	1.9750 V
0x0F	0.7875 V	0x2F	1.1875 V	0x4F	1.5875 V	0x6F	1.9875 V
0x10	0.8000 V	0x30	1.2000 V	0x50	1.6000 V	0x70	2.0000 V
0x11	0.8125 V	0x31	1.2125 V	0x51	1.6125 V	0x71	2.0125 V
0x12	0.8250 V	0x32	1.2250 V	0x52	1.6250 V	0x72	2.0250 V
0x13	0.8375 V	0x33	1.2375 V	0x53	1.6375 V	0x73	2.0375 V
0x14	0.8500 V	0x34	1.2500 V	0x54	1.6500 V	0x74	2.0500 V
0x15	0.8625 V	0x35	1.2625 V	0x55	1.6625 V	0x75	2.0625 V
0x16	0.8750 V	0x36	1.2750 V	0x56	1.6750 V	0x76	2.0750 V
0x17	0.8875 V	0x37	1.2875 V	0x57	1.6875 V	0x77	2.0875 V
0x18	0.9000 V	0x38	1.3000 V	0x58	1.7000 V	0x78	2.1000 V
0x19	0.9125 V	0x39	1.3125 V	0x59	1.7125 V	0x79	2.1125 V
0x1A	0.9250 V	0x3A	1.3250 V	0x5A	1.7250 V	0x7A	2.1250 V
0x1B	0.9375 V	0x3B	1.3375 V	0x5B	1.7375 V	0x7B	2.1375 V
0x1C	0.9500 V	0x3C	1.3500 V	0x5C	1.7500 V	0x7C	2.1500 V
0x1D	0.9625 V	0x3D	1.3625 V	0x5D	1.7625 V	0x7D	2.1625 V
0x1E	0.9750 V	0x3E	1.3750 V	0x5E	1.7750 V	0x7E	2.1750 V
0x1F	0.9875 V	0x3F	1.3875 V	0x5F	1.7875 V	0x7F	2.1875 V

Table 67. BUCK1, BUCK3, BUCK4 output voltage table

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
0x00	0.600 V	0x20	1.400 V	0x40	2.200 V	0x60	3.000 V
0x01	0.625 V	0x21	1.425 V	0x41	2.225 V	0x61	3.025 V
0x02	0.650 V	0x22	1.450 V	0x42	2.250 V	0x62	3.050 V
0x03	0.675 V	0x23	1.475 V	0x43	2.275 V	0x63	3.075 V
0x04	0.700 V	0x24	1.500 V	0x44	2.300 V	0x64	3.100 V
0x05	0.725 V	0x25	1.525 V	0x45	2.325 V	0x65	3.125 V
0x06	0.750 V	0x26	1.550 V	0x46	2.350 V	0x66	3.150 V
0x07	0.775 V	0x27	1.575 V	0x47	2.375 V	0x67	3.175 V

Table 67. BUCK1, BUCK3, BUCK4 output voltage table*...continued*

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
0x08	0.800 V	0x28	1.600 V	0x48	2.400 V	0x68	3.200 V
0x09	0.825 V	0x29	1.625 V	0x49	2.425 V	0x69	3.225 V
0x0A	0.850 V	0x2A	1.650 V	0x4A	2.450 V	0x6A	3.250 V
0x0B	0.875 V	0x2B	1.675 V	0x4B	2.475 V	0x6B	3.275 V
0x0C	0.900 V	0x2C	1.700 V	0x4C	2.500 V	0x6C	3.300 V
0x0D	0.925 V	0x2D	1.725 V	0x4D	2.525 V	0x6D	3.325 V
0x0E	0.950 V	0x2E	1.750 V	0x4E	2.550 V	0x6E	3.350 V
0x0F	0.975 V	0x2F	1.775 V	0x4F	2.575 V	0x6F	3.375 V
0x10	1.000 V	0x30	1.800 V	0x50	2.600 V	0x70	3.400 V
0x11	1.025 V	0x31	1.825 V	0x51	2.625 V	0x71	3.425 V
0x12	1.050 V	0x32	1.850 V	0x52	2.650 V	0x72	3.450 V
0x13	1.075 V	0x33	1.875 V	0x53	2.675 V	0x73	3.475 V
0x14	1.100 V	0x34	1.900 V	0x54	2.700 V	0x74	3.500 V
0x15	1.125 V	0x35	1.925 V	0x55	2.725 V	0x75	3.525 V
0x16	1.150 V	0x36	1.950 V	0x56	2.750 V	0x76	3.550 V
0x17	1.175 V	0x37	1.975 V	0x57	2.775 V	0x77	3.570 V
0x18	1.200 V	0x38	2.000 V	0x58	2.800 V	0x78	3.600 V
0x19	1.225 V	0x39	2.025 V	0x59	2.825 V	0x79	3.625 V
0x1A	1.250 V	0x3A	2.050 V	0x5A	2.850 V	0x7A	3.650 V
0x1B	1.275 V	0x3B	2.075 V	0x5B	2.875 V	0x7B	3.675 V
0x1C	1.300 V	0x3C	2.100 V	0x5C	2.900 V	0x7C	3.700 V
0x1D	1.325 V	0x3D	2.125 V	0x5D	2.925 V	0x7D	3.725 V
0x1E	1.350 V	0x3E	2.150 V	0x5E	2.950 V	0x7E	3.750 V
0x1F	1.375 V	0x3F	2.175 V	0x5F	2.975 V	0x7F	3.775 V

8.2.25 LDO1_OUT_L

LDO1 output voltage register when SD_VSEL is low. This register is protected by Lock key; 0x4E register should be written with unlock key before updating this register. OTP programmable register.

Table 68. LDO1_OUT_L register (address 36h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD	L1_OUT_L						
QFN eset	0	1	1	0	0	1	0	0
WLCSP reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 69. LDO1_OUT_L register (address 36h) bit descriptions

Bit	Symbol	Description
7	RSVD	Reserved
6 to 0	L1_OUT_L	LDO1 output voltage when SD_VSEL pin = Low Programmable from 0.8 V to 3.3 V in 25 mV steps: • **0000 0000** — 0.8V (default, WLCSP package OTP A1) • **0110 0100** — 3.3V (default, QFN package OTP A1) See Table 70

Table 70. L1_OUT_L values

Voltage (V)	Code (Dec)	Code (Bin)	Voltage (V)	Code (Dec)	Code (Bin)	Voltage (V)	Code (Dec)	Code (Bin)
0.800	0	0000000	1.650	34	0100010	2.500	68	1000100
0.825	1	0000001	1.675	35	0100011	2.525	69	1000101
0.850	2	0000010	1.700	36	0100100	2.550	70	1000110
0.875	3	0000011	1.725	37	0100101	2.575	71	1000111
0.900	4	0000100	1.750	38	0100110	2.600	72	1001000
0.925	5	0000101	1.775	39	0100111	2.625	73	1001001
0.950	6	0000110	1.800	40	0101000	2.650	74	1001010
0.975	7	0000111	1.825	41	0101001	2.675	75	1001011
1.000	8	0001000	1.850	42	0101010	2.700	76	1001100
1.025	9	0001001	1.875	43	0101011	2.725	77	1001101
1.050	10	0001010	1.900	44	0101100	2.750	78	1001110
1.075	11	0001011	1.925	45	0101101	2.775	79	1001111
1.100	12	0001100	1.950	46	0101110	2.800	80	1010000
1.125	13	0001101	1.975	47	0101111	2.825	81	1010001
1.150	14	0001110	2.000	48	0110000	2.850	82	1010010
1.175	15	0001111	2.025	49	0110001	2.875	83	1010011
1.200	16	0010000	2.050	50	0110010	2.900	84	1010100
1.225	17	0010001	2.075	51	0110011	2.925	85	1010101
1.250	18	0010010	2.100	52	0110100	2.950	86	1010110
1.275	19	0010011	2.125	53	0110101	2.975	87	1010111
1.300	20	0010100	2.150	54	0110110	3.000	88	1011000
1.325	21	0010101	2.175	55	0110111	3.025	89	1011001
1.350	22	0010110	2.200	56	0111000	3.050	90	1011010
1.375	23	0010111	2.225	57	0111001	3.075	91	1011011
1.400	24	0011000	2.250	58	0111010	3.100	92	1011100
1.425	25	0011001	2.275	59	0111011	3.125	93	1011101
1.450	26	0011010	2.300	60	0111100	3.150	94	1011110

Table 70. L1_OUT_L values...*continued*

Voltage (V)	Code (Dec)	Code (Bin)	Voltage (V)	Code (Dec)	Code (Bin)	Voltage (V)	Code (Dec)	Code (Bin)
1.475	27	0011011	2.325	61	0111101	3.175	95	1011111
1.500	28	0011100	2.350	62	0111110	3.200	96	1100000
1.525	29	0011101	2.375	63	0111111	3.225	97	1100001
1.550	30	0011110	2.400	64	1000000	3.250	98	1100010
1.575	31	0011111	2.425	65	1000001	3.275	99	1100011
1.600	32	0100000	2.450	66	1000010	**3.300**	**100**	**1100100**
1.625	33	0100001	2.475	67	1000011	3.300	>100	>1100100

8.2.26 LDO1_CFG

LDO1 enable control and active discharge resistor configuration register. OTP programmable register.

Table 71. LDO1_CFG register (address 37h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD		L1_AD_SD_VSEL	L1_AD	RSVD		L1_ENMODE	
Reset	0	0	1	1	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 72. LDO1_CFG register (address 37h) bit descriptions

Bit	Symbol	Description
7 to 6	RSVD	Reserved
5	L1_AD_SD_VSEL	LDO1 Active discharge control during ON **0 —** Disable Active discharge resistor **1 —** Enable Active discharge resistor for 2 ms[1] during LDO1 transition only from 3.3 V to 1.8 V by toggling SD_VSEL pin (default)
4	L1_AD	LDO1 Active discharge control during OFF **0 —** Always disable Active discharge resistor **1 —** Enable Active discharge resistor when regulator is OFF (default)
3 to 2	RSVD	Reserved
1 to 0	L1_ENMODE	LDO1 Enable mode **00 —** OFF **01 —** ON at RUN State (default) **10 —** ON at ACTIVE mode or STANDBY mode, OFF at DPSTANDBY **11 —** ON at ACTIVE mode, OFF at STANDBY or DPSTANDBY

[1] During this 2 ms transition time, LDO1 maximum load current is limited.

8.2.27 LDO1_OUT_H

LDO1 output voltage register when SD_VSEL is High. This register is protected by Lock key; 0x4E register should be written with unlock key before updating this register. OTP programmable register.

Table 73. LDO1_OUT_H register (address 38h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD	L1_OUT_H						
QFN reset	0	0	1	0	1	0	0	0
WLCSP reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 74. LDO1_OUT_H register (address 38h) bit descriptions

Bit	Symbol	Description
7	RSVD	Reserved
6 to 0	L1_OUT_H	LDO1 output voltage when SD_VSEL pin = High Programmable from 0.8 V to 3.3 V in 25 mV steps • **0000 0000** — 0.8V (default, WLCSP package OTP A1) • **0010 1000** — 1.8V (default, QFN package OTP A1) See Table 75

Table 75. L1_OUT_H values

Voltage (V)	Code (Dec)	Code (Bin)	Voltage (V)	Code (Dec)	Code (Bin)	Voltage (V)	Code (Dec)	Code (Bin)
0.800	0	0000000	1.650	34	0100010	2.500	68	1000100
0.825	1	0000001	1.675	35	0100011	2.525	69	1000101
0.850	2	0000010	1.700	36	0100100	2.550	70	1000110
0.875	3	0000011	1.725	37	0100101	2.575	71	1000111
0.900	4	0000100	1.750	38	0100110	2.600	72	1001000
0.925	5	0000101	1.775	39	0100111	2.625	73	1001001
0.950	6	0000110	**1.800**	**40**	**0101000**	2.650	74	1001010
0.975	7	0000111	1.825	41	0101001	2.675	75	1001011
1.000	8	0001000	1.850	42	0101010	2.700	76	1001100
1.025	9	0001001	1.875	43	0101011	2.725	77	1001101
1.050	10	0001010	1.900	44	0101100	2.750	78	1001110
1.075	11	0001011	1.925	45	0101101	2.775	79	1001111
1.100	12	0001100	1.950	46	0101110	2.800	80	1010000
1.125	13	0001101	1.975	47	0101111	2.825	81	1010001
1.150	14	0001110	2.000	48	0110000	2.850	82	1010010
1.175	15	0001111	2.025	49	0110001	2.875	83	1010011
1.200	16	0010000	2.050	50	0110010	2.900	84	1010100
1.225	17	0010001	2.075	51	0110011	2.925	85	1010101
1.250	18	0010010	2.100	52	0110100	2.950	86	1010110

Table 75. L1_OUT_H values...*continued*

Voltage (V)	Code (Dec)	Code (Bin)	Voltage (V)	Code (Dec)	Code (Bin)	Voltage (V)	Code (Dec)	Code (Bin)
1.275	19	0010011	2.125	53	0110101	2.975	87	1010111
1.300	20	0010100	2.150	54	0110110	3.000	88	1011000
1.325	21	0010101	2.175	55	0110111	3.025	89	1011001
1.350	22	0010110	2.200	56	0111000	3.050	90	1011010
1.375	23	0010111	2.225	57	0111001	3.075	91	1011011
1.400	24	0011000	2.250	58	0111010	3.100	92	1011100
1.425	25	0011001	2.275	59	0111011	3.125	93	1011101
1.450	26	0011010	2.300	60	0111100	3.150	94	1011110
1.475	27	0011011	2.325	61	0111101	3.175	95	1011111
1.500	28	0011100	2.350	62	0111110	3.200	96	1100000
1.525	29	0011101	2.375	63	0111111	3.225	97	1100001
1.550	30	0011110	2.400	64	1000000	3.250	98	1100010
1.575	31	0011111	2.425	65	1000001	3.275	99	1100011
1.600	32	0100000	2.450	66	1000010	3.300	100	1100100
1.625	33	0100001	2.475	67	1000011	3.300	>100	>1100100

8.2.28 LDOSNVS_CFG1

LDO_SNVS control register for enable and voltage. This register is protected by Lock key; 0x4E register should be written with unlock key before updating this register. OTP programmable register.

Table 76. LDOSNVS_CFG1 register (address 39h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	LSNVS_AD	L_SNVS_OUT						
QFN reset	1	0	0	1	1	0	0	0
WLCSP reset	1	0	1	0	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 77. LDOSNVS_CFG1 register (address 39h) bit descriptions

Bit	Symbol	Description
7	LSNVS_AD	SNVS LDO Active discharge enable **0 —** Always disable Active discharge resistor **1 —** Enable Active discharge resistor when regulator is OFF (default)
6 to 0	L_SNVS_OUT	LDO_SNVS output voltage Programmable from 1.2 V to 3.4 V for QFN package or 0.8 V to 3.0 V for WLCSP package in 25 mV steps • **010 1000** — 1.8V (default, WLCSP package OTP A1) See Table 78 • **001 1000** — 1.8V (default, QFN package OTP A1) See Table 79

Table 78. L_SNVS_OUT values for WLCSP package

Voltage(V)	Code (Dec)	Code (Bin)	Voltage (V)	Code (Dec)	Code (Bin)	Voltage (V)	Code (Dec)	Code (Bin)
0.800	0	0000000	1.650	34	0100010	2.500	68	1000100
0.825	1	0000001	1.675	35	0100011	2.525	69	1000101
0.850	2	0000010	1.700	36	0100100	2.550	70	1000110
0.875	3	0000011	1.725	37	0100101	2.575	71	1000111
0.900	4	0000100	1.750	38	0100110	2.600	72	1001000
0.925	5	0000101	1.775	39	0100111	2.625	73	1001001
0.950	6	0000110	**1.800**	**40**	**0101000**	2.650	74	1001010
0.975	7	0000111	1.825	41	0101001	2.675	75	1001011
1.000	8	0001000	1.850	42	0101010	2.700	76	1001100
1.025	9	0001001	1.875	43	0101011	2.725	77	1001101
1.050	10	0001010	1.900	44	0101100	2.750	78	1001110
1.075	11	0001011	1.925	45	0101101	2.775	79	1001111
1.100	12	0001100	1.950	46	0101110	2.800	80	1010000
1.125	13	0001101	1.975	47	0101111	2.825	81	1010001
1.150	14	0001110	2.000	48	0110000	2.850	82	1010010
1.175	15	0001111	2.025	49	0110001	2.875	83	1010011
1.200	16	0010000	2.050	50	0110010	2.900	84	1010100
1.225	17	0010001	2.075	51	0110011	2.925	85	1010101
1.250	18	0010010	2.100	52	0110100	2.950	86	1010110
1.275	19	0010011	2.125	53	0110101	2.975	87	1010111
1.300	20	0010100	2.150	54	0110110	3.000	88	1011000
1.325	21	0010101	2.175	55	0110110	3.000	>88	>1011000
1.350	22	0010110	2.200	56	–	–	–	–
1.375	23	0010111	2.225	57	–	–	–	–
1.400	24	0011000	2.250	58	–	–	–	–
1.425	25	0011001	2.275	59	–	–	–	–
1.450	26	0011010	2.300	60	–	–	–	–
1.475	27	0011011	2.325	61	–	–	–	–
1.500	28	0011100	2.350	62	–	–	–	–
1.535	29	0011101	2.375	63	–	–	–	–
1.550	30	0011110	2.400	64	–	–	–	–
1.575	31	0011111	2.425	65	–	–	–	–
1.600	32	0100000	2.450	66	–	–	–	–
1.625	33	0100001	2.475	67	–	–	–	–

Table 79. L_SNVS_OUT values for QFN package

Voltage (V)	Code (Dec)	Code (Bin)	Voltage (V)	Code (Dec)	Code (Bin)	Voltage (V)	Code (Dec)	Code (Bin)
1.200	0	0000000	2.050	34	0100010	2.900	68	1000100
1.225	1	0000001	2.075	35	0100011	2.925	69	1000101
1.250	2	0000010	2.100	36	0100100	2.950	70	1000110
1.275	3	0000011	2.125	37	0100101	2.975	71	1000111
1.300	4	0000100	2.150	38	0100110	3.000	72	1001000
1.325	5	0000101	2.175	39	0100111	3.025	73	1001001
1.350	6	0000110	2.200	40	0101000	3.050	74	1001010
1.375	7	0000111	2.225	41	0101001	3.075	75	1001011
1.400	8	0001000	2.250	42	0101010	3.100	76	1001100
1.425	9	0001001	2.275	43	0101011	3.125	77	1001101
1.450	10	0001010	2.300	44	0101100	3.150	78	1001110
1.475	11	0001011	2.325	45	0101101	3.175	79	1001111
1.500	12	0001100	2.350	46	0101110	3.200	80	1010000
1.525	13	0001101	2.375	47	0101111	3.225	81	1010001
1.550	14	0001110	2.400	48	0110000	3.250	82	1010010
1.575	15	0001111	2.425	49	0110001	3.275	83	1010011
1.600	16	0010000	2.450	50	0110010	3.300	84	1010100
1.625	17	0010001	2.475	51	0110011	3.325	85	1010101
1.650	18	0010010	2.500	52	0110100	3.350	86	1010110
1.675	19	0010011	2.525	53	0110101	3.375	87	1010111
1.700	20	0010100	2.550	54	0110110	3.400	88	1011000
1.725	21	0010101	2.575	55	0110111	3.400	>88	>1011000
1.750	22	0010110	2.600	56	0111000	–	–	–
1.775	23	0010111	2.625	57	0111001	–	–	–
1.800	**24**	**0011000**	2.650	58	0111010	–	–	–
1.825	25	0011001	2.675	59	0111011	–	–	–
1.850	26	0011010	2.700	60	0111100	–	–	–
1.875	27	0011011	2.725	61	0111101	–	–	–
1.900	28	0011100	2.750	62	0111110	–	–	–
1.925	29	0011101	2.775	63	0111111	–	–	–
1.950	30	0011110	2.800	64	1000000	–	–	–
1.975	31	0011111	2.825	65	1000001	–	–	–
2.000	32	0100000	2.850	66	1000010	–	–	–
2.025	33	0100001	2.875	67	1000011	–	–	–

8.2.29 LDOSNVS_CFG2

LDO_SNVS control register.

Table 80. LDOSNVS_CFG2 register (address 3Ah) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD							LS_ENMODE
Reset	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 81. LDOSNVS_CFG2 register (address 3Ah) bit descriptions

Bit	Symbol	Description
7:1	RSVD	Reserved
0	LS_ENMODE	LDO_SNVS Enable mode **0 —** OFF **1 —** Always ON (default)

8.2.30 LDO2_CFG

LDO2 control register. OTP programmable register. This register is not available for WLCSP package (reset value WLCSP 0x00).

Table 82. LDO2_CFG register (address 3Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD	L2_AD	L2_LLSEL		L2_CSEL		L2_ENMODE	
Reset	0	1	0	1	1	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 83. LDO2_CFG register (address 3Bh) bit descriptions

Bit	Symbol	Description
7	RSVD	Reserved
6	L2_AD	LDO2 Active discharge enable **0** — Always disable Active discharge resistor **1** — Enable Active discharge resistor when regulator is OFF (default)
5 to 4	L2_LLSEL	Output trace resistance compensation **00** = No Compensation **01** = 15 mΩ (default) **10** = 30 mΩ **11** = 45 mΩ
3 to 2	L2_CSEL	Total Output capacitor selection **00** = Setting for Cout < 5 µF **01** = Setting for Cout > 5 µF **10,11** = Auto Cout detection (default)
1 to 0	L2_ENMODE	LDO2 Enable mode **00** = OFF

Table 83. LDO2_CFG register (address 3Bh) bit descriptions*...continued*

Bit	Symbol	Description
		01 = ON at RUN State (default) **10** = ON at ACTIVE mode or STANDBY mode, OFF at DPSTANDBY **11** = ON at ACTIVE mode, OFF at STANDBY or DPSTANDBY

8.2.31 LDO2_OUT

LDO2 output voltage register. This register is protected by Lock key; 0x4E register should be written with unlock key before updating this register. OTP programmable register. This register is not available for WLCSP package (reset value WLCSP 0x00).

Table 84. LDO2_OUT register (address 3Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	L2_INL2_MDET	L2_INL2_VSEL	L2_OUT					
Reset	0	0	0	0	1	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 85. LDO2_OUT register (address 3Ch) bit descriptions

Bit	Symbol	Description
7	L2_INL2_MDET	Manual detection for INL2 supply **0** = Auto detection (default) **1** = Manual configuration
6	L2_INL2_VSEL	INL2 voltage selection, effective only when L2_INL2_MDET = 1b **0b** = (V_{SYS} – V_{INL2}) > 0.7 V (default) **1b** = (V_{SYS} – V_{INL2}) ≤ 0.7 V
5 to 0	L2_OUT	LDO2 output voltage Programmable from 0.5 V to 1.95 V in 25 mV step **00 1100 —** 0.8 V (default, based on OTP configuration A1); See Table 86

Table 86. L2_OUT values

Voltage (V)	Code (Dec)	Code (Bin)	Voltage (V)	Code (Dec)	Code (Bin)	Voltage (V)	Code (Dec)	Code (Bin)
0.500	0	000000	1.000	20	010100	1.500	40	101000
0.525	1	000001	1.025	21	010101	1.525	41	101001
0.550	2	000010	1.050	22	010110	1.550	42	101010
0.575	3	000011	1.075	23	010111	1.575	43	101011
0.600	4	000100	1.100	24	011000	1.600	44	101100
0.625	5	000101	1.125	25	011001	1.625	45	101101
0.650	6	000110	1.150	26	011010	1.650	46	101110
0.675	7	000111	1.175	27	011011	1.675	47	101111
0.700	8	001000	1.200	28	011100	1.700	48	110000
0.725	9	001001	1.225	29	011101	1.725	49	110001

Table 86. L2_OUT values*...continued*

Voltage (V)	Code (Dec)	Code (Bin)	Voltage (V)	Code (Dec)	Code (Bin)	Voltage (V)	Code (Dec)	Code (Bin)
0.750	10	001010	1.250	30	011110	1.750	50	110010
0.775	11	001011	1.275	31	011111	1.775	51	110011
0.800	**12**	**001100**	1.300	32	100000	1.800	52	110100
0.825	13	001101	1.325	33	100001	1.825	53	110101
0.850	14	001110	1.350	34	100010	1.850	54	110110
0.875	15	001111	1.375	35	100011	1.875	55	110111
0.900	16	010000	1.400	36	100100	1.900	56	111000
0.925	17	010001	1.425	37	100101	1.925	57	111001
0.950	18	010010	1.450	38	100110	1.950	58	111010
0.975	19	010011	1.475	39	100111	1.950	>58	>111010

8.2.32 BUCK_POK_F_CFG

BUCKx POK falling thresholds setting register. OTP programable register. This register is not available for WLCSP package, POK for all BUCKs is fixed to 75% for all BUCKs in WLCSP package. Reset value WLCSP 0x00.

Table 87. BUCK_POK_F_CFG register (address 3Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	BUCK4_POK_F		BUCK3_POK_F		BUCK2_POK_F		BUCK1_POK_F	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 88. BUCK_POK_F_CFG register (address 3Dh) bit descriptions

Bit	Symbol	Description
7 to 6	BUCK4_POK_F	BUCK4 POK falling threshold **00** = 75% of output voltage (default) **01** = 80% of output voltage **10** = 85% of output voltage **11** = 85% of output voltage
5 to 4	BUCK3_POK_F	BUCK3 POK falling threshold **00** = 75% of output voltage (default) **01** = 80% of output voltage **10** = 85% of output voltage **11** = 85% of output voltage
3 to 2	BUCK2_POK_F	BUCK2 POK falling threshold **00** = 75% of output voltage (default) **01** = 80% of output voltage **10** = 85% of output voltage **11** = 85% of output voltage

Table 88. BUCK_POK_F_CFG register (address 3Dh) bit descriptions*...continued*

Bit	Symbol	Description
1 to 0	BUCK1_POK_F	BUCK1 POK falling threshold **00** = 75% of output voltage (default) **01** = 80% of output voltage **10** = 85% of output voltage **11** = 85% of output voltage

8.2.33 LSW_CTRL1

Load switch configuration register. OTP programmable register.

Table 89. LSW_CTRL1 register (address 40h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD	RSVD		LSW_AD	RSVD		LSW_EN	
Reset	0	0	0	1	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 90. LSW_CTRL1 register (address 40h) bit descriptions

Bit	Symbol	Description
7	RSVD	Reserved
6 to 5	RSVD	Reserved
4	LSW_AD	Load SW active discharge **0** — Disabled **1** — Enabled when Load SW1 is off (default)
3 to 2	RSVD	Reserved
1 to 0	LSW_EN	Load SW Enable mode **00** — Forcedly OFF **01** — Enabled by LSW_EN pin (default) **10** — Forcedly ON **11** — Forcedly ON

8.2.34 LSW_CTRL2

Load switch configuration register.

Table 91. LSW_CTRL2 register (address 41h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RSVD	RSVD	RSVD	RSVD	RSVD	LSW_SC	LSW_OC	
Reset	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 92. LSW_CTRL2 register (address 41h) bit descriptions

Bit	Symbol	Description
7:3	RSVD	Reserved
2	LSW_SC	When switch detects short circuit current **0** = Turned OFF and LSW_EN[1:0] are set to 00b automatically (default) **1** = Turned OFF and restart in 100ms
1 to 0	LSW_OC	When load switch detects over current **00** = Turned OFF and LSW_EN[1:0] are set to 00b automatically **01** = Turned OFF and restart in 100ms (default) **10, 11** = stay ON

8.2.35 REG_LOCK

Output voltage configuration unlock key.

Table 93. REG_LOCK register (address 4Eh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	UNLOCK_KEY							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 94. REG_LOCK register (address 4Eh) bit descriptions

Bit	Symbol	Description
7 to 0	UNLOCK_KEY	Unlock key is written to change regulator output configuration. **1011100 —** Unlock regulator output configuration registers (0x5C) **Others —** Lock regulator output configuration registers

9 Application design-in information

9.1 Reference schematic

9.1.1 PF9453 reference schematic

Figure 23 illustrates PF9453 (HVQFN40 package) reference schematic with i.MX 91 processor.

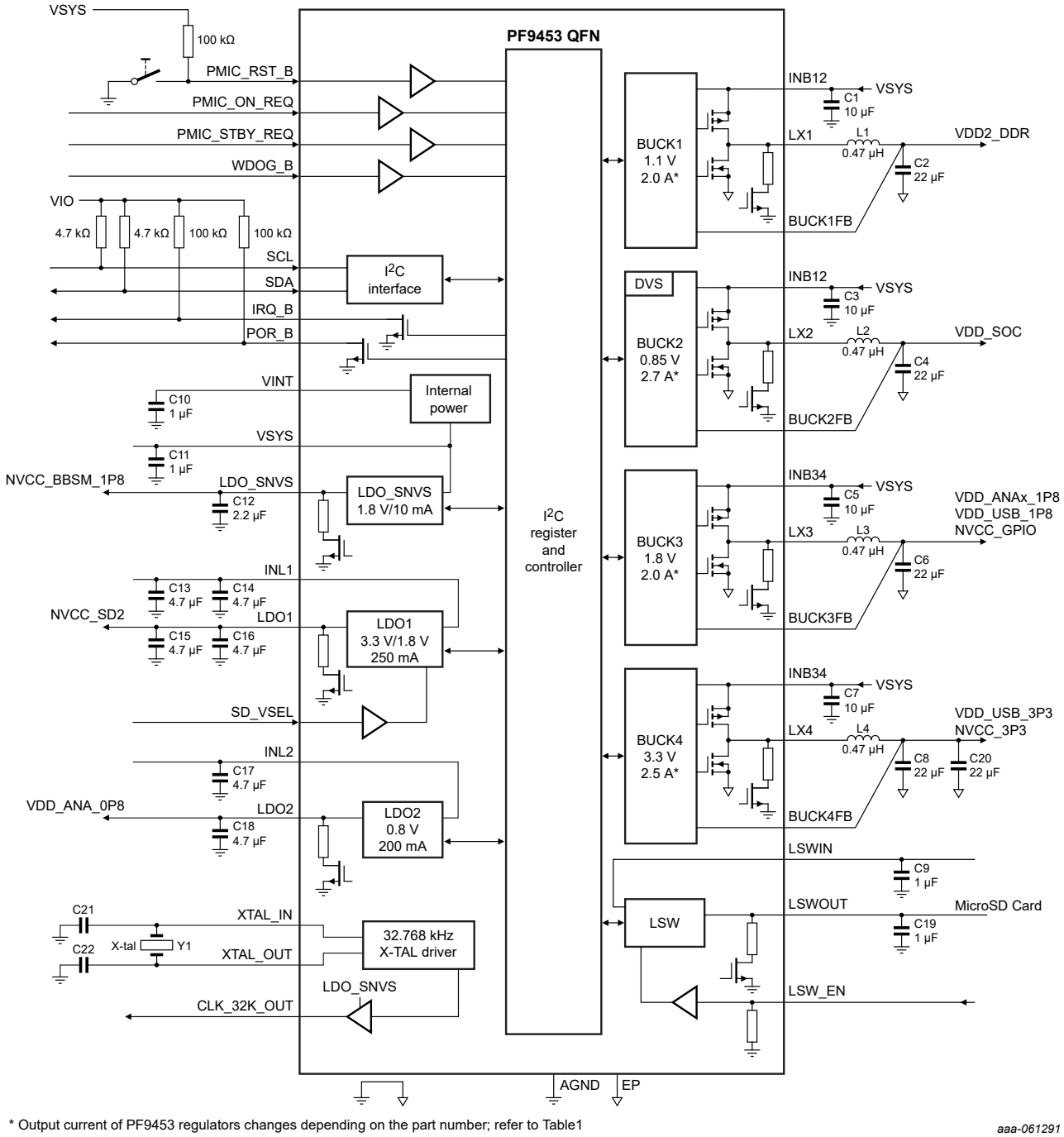


Figure 23. PF9453 QFN application schematic

Figure 24 illustrates PF9453 (WLCSP package) reference schematic with i.MX 91 processor.

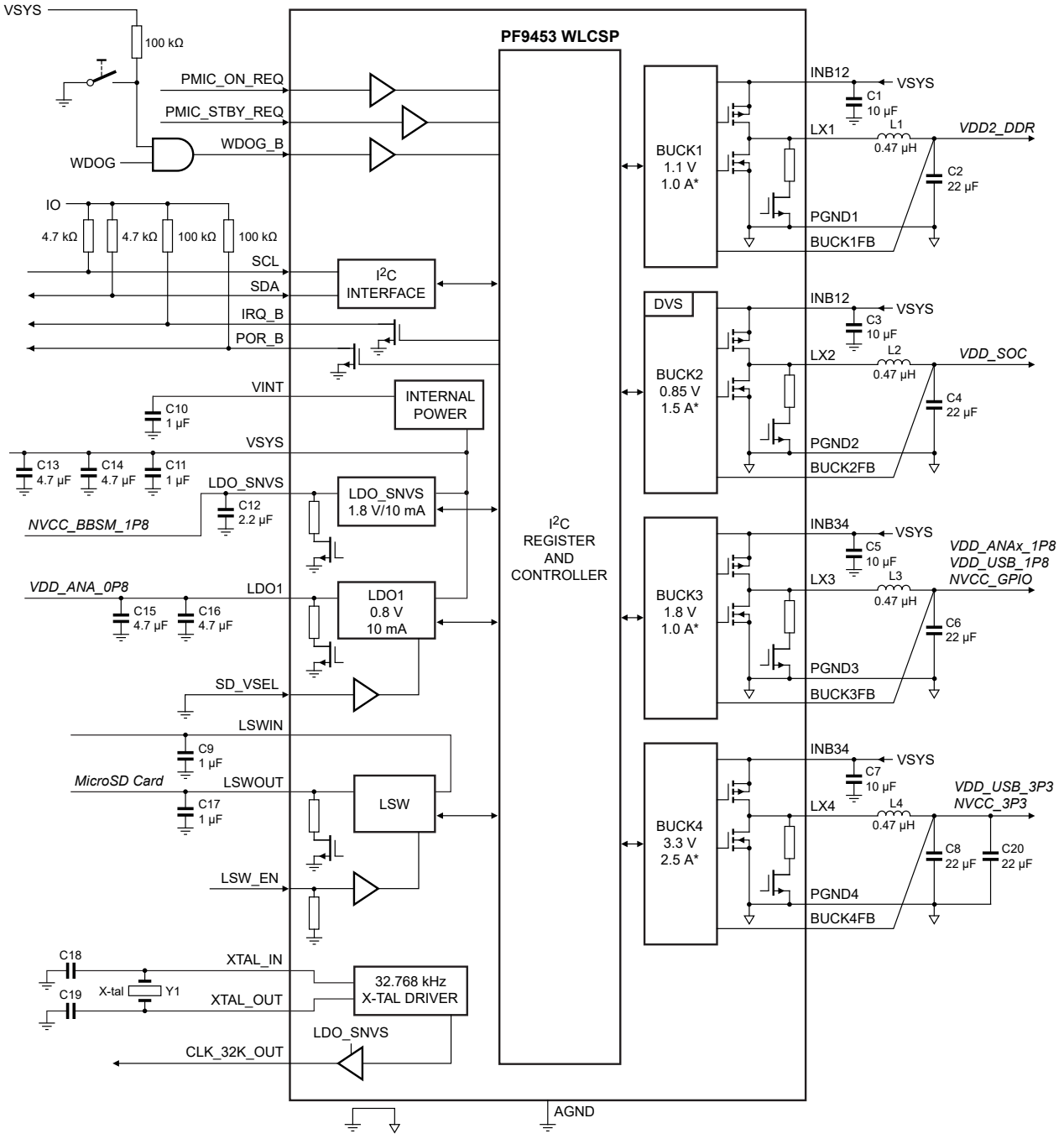


Figure 24. PF9453 (WLCSP package) reference schematic

9.1.2 External BOM in reference schematic

Table 95 shows external BOM in reference schematic for QFN package.

Table 95. External BOM for QFN package

Ref	Block	Pin	Part number	Size [mm]	Value
L1	BUCK	LX1	DFE21CCNR47MELL	2012	0.47 µH
L2	BUCK	LX2	DFE21CCNR47MELL	2012	0.47 µH
L3	BUCK	LX3	DFE21CCNR47MELL	2012	0.47 µH
L4	BUCK	LX4	DFE21CCNR47MELL	2012	0.47 µH
C1, C3	BUCK	INB12	GRM188R60J106ME	1608	10 µF x 2
C2	BUCK	BUCK1 Output	GRM158C80G226ME	1005	22 µF
C5, C7	BUCK	INB34	GRM188R60J106ME	1608	10 µF x 2
C4	BUCK	BUCK2 Output	GRM158C80G226ME	1005	22 µF
C6	BUCK	BUCK3 Output	GRM158C80G226ME	1005	22 µF
C8, C20	BUCK	BUCK4 Output	GRM158C80G226ME	1005	22 µF x 2
C13, C14	LDO	INL1	GRM155R60J475ME	1005	4.7 µF x 2
C17	LDO	INL2	GRM155R60J475ME	1005	4.7 µF
C15, C16	LDO	LDO1	GRM155R60J475ME	1005	4.7 µF x 2
C18	LDO	LDO2	GRM155R60J475ME	1005	4.7 µF
C10	VINT	VINT	GRM155R61C105KA	1005	1 µF
C11	VSYS	VSYS	GRM155R61C105KA	1005	1 µF
C12	LDO	LDO_SNVS	GRM155R61C225KE	1005	2.2 µF
C9	LSW	LSWIN	GRM155R61C105KA	1005	1 µF
C19	LSW	LSWOUT	GRM155R61C105KA	1005	1 µF
C21	XTAL	XTAL_IN	GCM1555C1H180JA16	1005	18 pF
C22	XTAL	XTAL_OUT	GCM1555C1H180JA16	1005	18 pF
Y1	XTAL	XTAL_IN and XTAL_OUT	ABS07-32.768KHZ-T	3.2 mm x 1.5 mm	32.768 kHz

Table 96 shows external BOM in reference schematic for WLCSP package.

Table 96. External BOM for WLCSP package

Ref	Block	Pin	Part number	Size [mm]	Value
L1	BUCK	LX1	DFE201210S-R47M	2012	0.47 µH
L2	BUCK	LX2	DFE201210S-R47M	2012	0.47 µH
L3	BUCK	LX3	DFE201210S-R47M	2012	0.47 µH
L4	BUCK	LX4	DFE201210S-R47M	2012	0.47 µH
C1, C3	BUCK	INB12	GRM188R60J106ME	1608	10 µF x 2
C2	BUCK	BUCK1 Output	GRM158C80G226ME	1005	22 µF

Table 96. External BOM for WLCSP package*...continued*

Ref	Block	Pin	Part number	Size [mm]	Value
C5, C7	BUCK	INB34	GRM188R60J106ME	1608	10 µF x 2
C4	BUCK	BUCK2 Output	GRM158C80G226ME	1005	22 µF
C6	BUCK	BUCK3 Output	GRM158C80G226ME	1005	22 µF
C8, C20	BUCK	BUCK4 Output	GRM158C80G226ME	1005	22 µF x 2
C13, C14	LDO	VSYS	GRM155R60J475ME	1005	4.7 µF x 2
C15, C16	LDO	LDO1	GRM155R60J475ME	1005	4.7 µF x 2
C10	VINT	VINT	GRM155R61C105KA	1005	1 µF
C11	VSYS	VSYS	GRM155R61C105KA	1005	1 µF
C12	LDO	LDO_SNVS	GRM155R61C225KE	1005	2.2 µF
C9	LSW	LSWIN	GRM155R61C105KA	1005	1 µF
C17	LSW	LSWOUT	GRM155R61C105KA	1005	1 µF
C18	XTAL	XTAL_IN	GCM1555C1H180JA16	1005	18 pF
C19	XTAL	XTAL_OUT	GCM1555C1H180JA16	1005	18 pF
Y1	XTAL	XTAL_IN and XTAL_OUT	ABS07-32.768KHZ-T	3.2 mm x 1.5 mm	32.768 kHz

9.2 Typical application

The PF9453 devices have only a few design requirements. For more details on how to create schematics with the PF9453 PMIC and best practices for layout, refer to the PF9453 QFN or WLCSP application note.

10 Limiting values

Table 97. Limiting values

Absolute maximum ratings

Explanation	Pin	Conditions	Min	Max	Unit
Voltage range (with respect to GND)	VSYS	–	-0.5	+6.0	V
	INB12, INB34, INL1, INL2	QFN	-0.5	VSYS + 0.5	V
	INB12, INB34	WLCSP	-0.5	VSYS + 0.5	V
	LX1, LX2	–	-0.5	INB12 + 0.5[1]	V
	LX3, LX4	–	-0.5	INB34 + 0.5[1]	V
	BUCK1FB, BUCK2FB, BUCK3FB, BUCK4FB	–	-0.5	VSYS + 0.5	V
	LDO1	QFN	-0.5	V_{INL1}+0.5	V
		WLSCP	-0.5	VSYS + 0.5	V
	LDO2	QFN	-0.5	V_{INL2}+0.5	V
	XTAL_IN, XTAL_OUT	–	-0.5	VSYS + 0.5	V
	VINT	–	-0.5	+1.8	V

Table 97. Limiting values...*continued*

Absolute maximum ratings

Explanation	Pin	Conditions	Min	Max	Unit
	LSWIN	–	-0.5	VSYS + 0.5	V
	LSWOUT	–	-0.5	LSWIN	V
	LDO_SNVS	–	-0.5	VSYS + 0.5	V
	CLK_32K_OUT	–	-0.5	LDO_SNVS + 0.5	V
	PMIC_ON_REQ, POR_B PMIC_ STBY_REQ, WDOG_B, IRQ_B, SCL, SDA, LSW_EN, SD_VSEL, PMIC_RST_B, (PMIC_RST_B only available in QFN)	–	-0.5	VSYS + 0.5	V
Output current	LSWOUT	–	–	0.45	A
Junction temperature	–	–	-40	+150	°C
VESD	All pins	HBM (JESD22-001)	-2	+2	kV
		CDM (JESD22-C101E)	-500	500	V

[1] LX voltage overshoot and undershoot above or below the absolute maximum rating during power transistor switching period is normal and guaranteed by design as it is already checked in design phase in the point of device safe operating area (SOA) and lifetime.

11 Recommended operating conditions

Table 98. Recommended operating conditions

Explanation	Pin	Conditions	Min	Max	Unit
Voltage range (with respect to GND)	VSYS, INL1, INL2	–	2.7	5.5	V
	INB12, INB34	–	2.7	5.5	V
	LSWIN	–	1.8	5.5	V
Junction temperature	–	–	-40	+125	°C
Ambient temperature	–	QFN	-40	+105	°C
	–	WLCSP	-40	+85	°C
Storage temperature	–	QFN	-65	+150	°C
	–	WLCSP	-55	+150	°C

12 Thermal characteristics

Table 99. Thermal characteristics

Symbol	Parameter	Board type	Package	Typ	Unit
$R_{\theta JA}$	Thermal resistance from junction to ambient[1]	JESD51-9, 2s2p	QFN	33	°C/W
		JESD51-9, 2s2p	WLCSP	53.5	°C/W
Ψ_{JT}	Junction to top of package thermal characterization parameter[1]	JESD51-9, 2s2p	QFN	2.1	°C/W
		JESD51-9, 2s2p	WLCSP	1.1	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

13 Electrical characteristics

13.1 Top level parameter

Table 100. Top level parameter

Unless otherwise specified:

- ***WLCSP*** → *VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, TA= –40 °C ~ +85 °C*
- ***QFN*** →*VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VINL1 = VINL2 = 3.8 V, TA= –40 °C ~ +105 °C*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Quiescent current							
$I_{Q\_Shutdown}$	Shutdown current	LDO_SNVS is ON and no load.	QFN, 25 °C	–	11	22	µA
			WLCSP, 25 °C	–	10	16	
			QFN, -40 °C ~105 °C	–	11	30	
			WLCSP, -40 °C ~85 °C	–	10	23	
I_{Q1}	System current	LDO_SNVS and BUCK1 are ON and no load.	QFN, 25 °C	–	23	49	µA
			WLCSP, 25 °C	–	22	35	
			QFN, -40 °C ~105 °C	–	23	57	
			WLCSP, -40 °C ~85 °C	–	22	45	
I_{Q2}	System current	All Regulators are ON and no load.	QFN, 25 °C	–	59	107	µA
			WLCSP, 25 °C	–	52	100	
			QFN, -40 °C ~105 °C	–	59	148	
			WLCSP, -40 °C ~85 °C	–	52	112	
VSYS							
V_{SYS_UVLO}	VSYS UVLO	Rising – OTP Programmable 00b = 2.65 V **01b = 2.85 V** 10b = 3.0 V 11b = 3.3 V	–	2.7	2.85	3.0	V
$V_{SYS\_UVLO\_H}$	VSYS UVLO hysteresis	Falling	–	–	200		mV
VINT							
VINT	Internal power supply	VSYS = 3.8 V	–	1.4	1.5	1.6	V
Low VSYS							
V_{LOW_VSYS}	Low VSYS	Falling, Low VSYS threshold above V_{SYS_UVLO}, L_{OW_VSYS} [7:6] = 01b	QFN	110	200	300	mV
			WLCSP	140	200	300	mV
$V_{LOW\_VSYS\_HYS}$	Low VSYS hysteresis	Rising	–	–	100	–	mV
Thermal shutdown							
T_{JSHDN}	Thermal shutdown	Tj Rising, 15°C hysteresis	–	–	150	–	°C
T_{J80}	Thermal interrupt1	Tj Rising, 15°C hysteresis	–	–	80	–	°C
T_{J100}	Thermal interrupt2	Tj Rising, 15°C hysteresis	–	–	100	–	°C
T_{JHYS}	Thermal hysteresis	–	–	–	15	–	°C
Logic and control signals							
V_{IL}	Input LOW level	PMIC_ON_REQ, PMIC_STBY_REQ, WDOG_B, PMIC_RST_B, (PMIC_RST_B only available in QFN)	–	–	–	0.4	V
V_{IH}	Input HIGH level	PMIC_ON_REQ, PMIC_STBY_REQ, WDOG_B, PMIC_RST_B,	–	1.4	–	–	V

Table 100. Top level parameter*...continued*

Unless otherwise specified:

- ***WLCSP*** *→ VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, TA= –40 °C ~ +85 °C*
- ***QFN*** *→VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VINL1 = VINL2 = 3.8 V, TA= –40 °C ~ +105 °C*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		(PMIC_RST_B only available in QFN)					
I_{LEAK}	Logic Input leakage current	PMIC_ON_REQ, PMIC_STBY_ REQ, WDOG_B, PMIC_RST_B, (PMIC_RST_B only available in QFN) V_{Logic} = 5.5 V, VSYS = 5.5 V	–	-1	–	+1	µA
V_{OL}	Output LOW level	IRQ_B, POR_B, I_{OL} = 6 mA	–		–	0.4	V
I_{LEAK}	Output high leakage current	IRQ_B, POR_B, V_{Logic} = 5.5 V, VSYS = 5.5 V	–	-1	–	+1	µA
Timing spec							
t_{SNVS}	Maximum time to enable LDO_SNVS from VSYS UVLO detected	–	–	–	10	–	ms
t_{32K_EN}	Time to stable 32 kHz clock buffer output from VSYS UVLO detected	–	–	–	1	–	sec
t_{ON_DEB}	PMIC_ON_REQ debounce time	–	–	40	50	60	µs
$t_{DEB\_PMIC\_RST\_B}$[1]	Debounce time of PMIC_RST_B	Programmable, PMIC_RST_B_ DEB = 0b	–	16	20	24	ms
t_{ONKEY}[1]	ONKEY timer of PMIC_ RST_B	Programmable, ONKEY_ TIMER = 01b	–	1.6	2	2.4	sec
$t_{RESETKEY}$[1]	RESETKEY timer of PMIC_RST_B	Programmable, RESETKEY_ TIMER = 101b	–	7.2	8	9.6	sec
t_{RESET_WAIT}[1]	Wait time from RES ETKEY detection to perform reset	–	–	80	100	120	ms
t_{ON_STEP}	Time step to turn on each regulator	Programmable, PSQ_TON_ STEP = 01b	–	1.6	2	2.4	ms
t_{POK_EXP}	POK wait timer out during power ON sequence	–	–	8	10	12	ms
t_{OFF_STEP}	Time step to turn off each regulator	Programmable, PSQ_TOFF_ STEP = 10b	–	6	8	10	ms
t_{RSTB}	Time from PUD_T16 Gr POK to POR_B release during Power on seq	–	–	16	20	24	ms
t_{FLT_THSD}	Debounce time for thermal fault	–	–	16	20	24	µs
t_{DEB_POKB}	Debounce time of regulator POKB	–	–	240	300	360	µs
t_{OC_DEB}[1]	Debounce time of Load Switch overcurrent	–	–	240	300	360	µs
$t_{FLT\_SD\_WAIT}$	Wait time to enter FAULT_SD after fault interrupt	At STANDBY and Run mode, programmable, $t_{FLT\_SD\_WAIT}$ = 0b	–	80	100	120	ms
$t_{FLT\_SD\_STAY}$	Time to stay at FAULT_ SD to move other mode		–	80	100	120	ms
$t_{RESTART}$	Wait time to start power up after power down at Cold Reset	Programmable, $t_{RESTART}$ = 0b	–	200	250	300	ms
$t_{PWR\_HOLD\_RST}$	Power Hold time after reset is performed	–	–	80	100	120	ms

Table 100. Top level parameter...*continued*

Unless otherwise specified:

- ***WLCSP*** → *VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, TA= –40 °C ~ +85 °C*
- ***QFN*** →*VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VINL1 = VINL2 = 3.8 V, TA= –40 °C ~ +105 °C*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{RESET}	POR_B low time at Warm Reset	–	–	16	20	24	ms
t_{DEB_WDOGB}	Debounce time of WDOG_B	–	–	40	50	60	µs
$t_{FLT\_POK\_MSK}$	POK mask time when regulator is enabled at RUN/Standby mode	–	–	2.4	3	3.6	ms

[1] Only applicable for QFN package.

13.2 BUCK1

Table 101. BUCK1

Unless otherwise specified:

- ***WLCSP*** → *VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, TA= –40 °C ~ +85 °C*
- ***QFN*** → *VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VINL1 = VINL2 = 3.8 V, TA= –40 °C ~ +105 °C*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{INB12}	Input voltage range	INB12 pin		2.7	–	5.5	V
I_Q	Quiescent current	IOUT = 0 A		–	10	–	µA
I_{OUT_MAX}	Max output current	–		2000[1]	–	–	mA
V_{BUCK1_RANGE}	Programmable output voltage range	I^2C programmable, 25 mV/step		0.6	–	3.775	V
V_{BUCK1}	DC output voltage accuracy	V_{INB12} = 3.8 V, V_{BUCK1} = 1.1 V, I_{OUT} = 0 A, forced PWM (FPWM) mode		-2	–	2	%
$\Delta V_{OUT(\Delta VINB)}$	DC line regulation	VINB12 = 3 V to 5 V, I_{OUT} = I_{OUT_MAX}		–	2	–	mV/V
$\Delta V_{OUT(\Delta IOUT)}$	DC load regulation	0 mA < I_{OUT} < I_{OUT_MAX}, VBUCK1 = 1.1 V		–	3	–	mV/A
$\Delta V_{OUT(\Delta IOUT)}$	Transient load response	I_{OUT} changes 0 to I_{OUT_MAX} (1 A/us slope), V_{BUCK1} = 1.1 V	QFN	–	50	–	mV
			WLCSP	–	75		
ΔV_{OUT}	Output voltage ripple	FPWM mode	–	–	10	–	mV
f_{SW}	Switching frequency	Continuous conduction mode (CCM)	–	–	2	–	MHz
R_{DSON}	High side P-FET R_{DSON}	V_{INB12} = 3.8 V	QFN	–	130	–	mΩ
			WLCSP	–	100	–	
	Low Side N-FET R_{DSON}	V_{INB12} = 3.8 V	QFN	–	72	–	mΩ
			WLCSP	–	50	–	
I_{LIM}	Peak inductor current limit	V_{INB12} = 3.8 V	–	3.0	3.6	4.2	A
t_{START}	Startup time	EN rising to 90 % of output voltage	–	–	510	710	µs
V_{soft_strup}	Soft-start slew rate	–	–	–	12.5	–	mV/us
R_{DIS}	Output active discharge resistance	–	–	–	100	150	Ω
BUCK_POK_R	Output power good rising	–	QFN	85	90	95	%
			WLCSP	74	85	96	
BUCK_POK_F	Output power good falling	Programmed by BUCK1_POK_F[1:0] bits	QFN	71	75	79	%
				76	80	84	
				81	85	89	
		Fixed values	WLCSP	65	75	85	%

Table 101. BUCK1*...continued*

Unless otherwise specified:

- ***WLCSP*** *→ VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, TA= –40 °C ~ +85 °C*
- ***QFN*** *→ VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VINL1 = VINL2 = 3.8 V, TA= –40 °C ~ +105 °C*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{POK_Deb}	POK debounce time	POK falling	–	–	300	–	µs
L	Inductor value	–	–	–	0.47	–	µH
C_{OUT}	Output capacitance	Minimum nominal capacitance	–	22	–	–	µF

[1] Output current of PF9453 regulators changes depending on the part number; refer to Table 2

13.3 BUCK2

Table 102. BUCK2

Unless otherwise specified:

- ***WLCSP*** *→VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, TA= –40 °C ~ +85 °C*
- ***QFN*** *→VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VINL1 = VINL2 = 3.8 V, TA= –40 °C ~ +105 °C*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{INB12}	Input voltage range	INB12 pin		2.7		5.5	V
I_Q	Quiescent current	IOUT = 0A		-	10		µA
I_{OUT_MAX}	Max output current	-		2700[1]			mA
V_{BUCK2_RANGE}	Programmable output voltage range	I^2C programmable, 12.5 mV/step		0.6		2.1875	V
V_{BUCK2}	DC output voltage accuracy	V_{INB12} = 3.8 V, V_{BUCK2} = 0.85 V, I_{OUT} = 0A, FPWM mode		-2		2	%
$\Delta V_{OUT(\Delta VINB)}$	DC Line regulation	VINB12 = 3 V to 5 V, I_{OUT}= I_{OUT_MAX}		-	2		mV/V
$\Delta V_{OUT(\Delta IOUT)}$	DC Load regulation	0 mA < $_{IOUT}$ < I_{OUT_MAX}, V_{BUCK2} = 0.85 V		-	3		mV/A
$\Delta V_{OUT(\Delta IOUT)}$	Transient load response	I_{OUT} changes 0 to I_{OUT_MAX} (1A/us slope), V_{BUCK2} = 0.85 V		-	50		mV
ΔV_{OUT}	Output voltage ripple	FPWM mode		-	10		mV
f_{SW}	Switching frequency	CCM		-	2		MHz
R_{DSON}	High Side P-FET R_{DSON}	V_{INB12} = 3.8 V	QFN	-	130		mΩ
			WLCSP	-	100		
	Low Side N-FET R_{DSON}	V_{INB12} = 3.8 V	QFN	-	72		mΩ
			WLCSP	-	50		
I_{LIM}	Peak inductor current limit	V_{INB12} = 3.8 V	QFN	3.5	4.0	4.65	A
			WLCSP	3	3.6	4.2	
t_{START}	Startup time	EN rising to 90 % of output voltage		-	480	680	µs
V_{RAMP}	Output voltage slew rate	Programmable, RAMP[1:0] = 01b		-	12.5		mV/us
V_{soft_strup}	Soft-start slew rate	-		-	12.5		mV/us
BUCK_POK_R	Output power good rising	-	QFN	85	90	95	%
			WLCSP	74	85	96	
BUCK_POK_F	Output power good falling	Programmed by BUCK2_POK_F[1:0] bits	QFN	71	75	79	%
				76	80	84	
				81	85	89	
		Fixed values	WLCSP	65	75	85	%
t_{POK_Deb}	POK debounce time	POK falling		-	300		µs
RDIS	Output active discharge resistance	-		-	100	150	Ω

Table 102. BUCK2*...continued*

Unless otherwise specified:

- ***WLCSP*** *→VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, TA= –40 °C ~ +85 °C*
- ***QFN*** *→VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VINL1 = VINL2 = 3.8 V, TA= –40 °C ~ +105 °C*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
L	Inductor value	-	-	0.47		µH
C_{OUT}	Output capacitance	Minimum nominal capacitance	22			µF

[1] Output current of PF9453 regulators changes depending on the part number; refer to Table 2.

13.4 BUCK3

Table 103. BUCK3

Unless otherwise specified:

- ***WLCSP*** *→VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, TA= –40 °C ~ +85 °C*
- ***QFN*** *→ VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VINL1 = VINL2 = 3.8 V, TA= –40 °C ~ +105 °C*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{INB34}	Input voltage range	INB34 pin		2.7		5.5	V
I_Q	Quiescent current	I_{OUT} = 0A		-	10		µA
I_{OUT_MAX}	Max output current	-		2000[1]			mA
V_{BUCK3_RANGE}	Programmable output voltage range	I^2C programmable, 25 mV/step		0.6		3.775	V
V_{BUCK3}	DC output voltage accuracy	V_{INB34} = 3.8 V, V_{BUCK3} = 1.8 V, I_{OUT} = 0A, FPWM mode		-2		2	%
$\Delta V_{OUT(\Delta VINB)}$	DC line regulation	V_{INB34} = 3 V to 5 V, I_{OUT}= I_{OUT_MAX}		-	2		mV/V
$\Delta V_{OUT(\Delta IOUT)}$	DC load regulation	0 mA < I_{OUT} < I_{OUT_MAX}, VBUCK3 = 1.8 V		-	3		mV/A
$\Delta V_{OUT(\Delta IOUT)}$	Transient load response	I_{OUT} changes 0 to I_{OUT_MAX} (1A/us slope), V_{BUCK3} = 1.8 V	QFN	-	75		mV
			WLCSP	-	135		
ΔV_{OUT}	Output voltage ripple	FPWM mode		-	10		mV
f_{SW}	Switching frequency	CCM		-	2		MHz
R_{DSON}	High side P-FET R_{DSON}	V_{INB34} = 3.8 V	QFN	-	130		mΩ
			WLCSP	-	100		
	Low Side N-FET R_{DSON}	V_{INB34} = 3.8 V	QFN	-	72		mΩ
			WLCSP	-	50		
I_{LIM}	Peak inductor current limit	V_{INB34} = 3.8 V		3.0	3.6	4.2	A
t_{START}	Startup time	EN rising to 90 % of output voltage		-	570	770	µs
V_{soft_strup}	Soft-start slew rate	-		-	12.5		mV/us
R_{DIS}	Output active discharge resistance	-		-	100	150	Ω
BUCK_POK_R	Output power good rising	-	QFN	85	90	95	%
			WLCSP	78	85	93	
BUCK_POK_F	Output power good falling	Programmed by BUCK3_POK_F[1:0] bits	QFN	71	75	79	%
				76	80	84	
				81	85	89	
		Fixed values	WLCSP	68	75	82	%
t_{POK_Deb}	POK debounce time	POK falling		-	300		µs
L	Inductor value	-		-	0.47		µH
C_{OUT}	Output capacitance	Minimum nominal capacitance		22			µF

[1] Output current of PF9453 regulators changes depending on the part number; refer to Table 2.

13.5 BUCK4

Table 104. BUCK4

Unless otherwise specified:

- ***WLCSP*** → *VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, TA= –40 °C ~ +85 °C*
- ***QFN*** → *VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VINL1 = VINL2 = 3.8 V, TA= –40 °C ~ +105 °C*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{INB12}	Input voltage range	INB34 pin		2.7		5.5	V
I_Q	Quiescent current	I_{OUT} = 0A		-	10		µA
I_{OUT_MAX}	Max output current	V_{INB34} = 4.2 V		2500[1]			mA
V_{BUCK4_RANGE}	Programmable output voltage range	I^2C programmable, 25 mV/step		0.6		3.775	V
V_{BUCK4}	DC Output Voltage Accuracy	V_{INB34} = 3.8 V, V_{BUCK4} = 3.3 V, I_{OUT} = 0A, FPWM mode		-2		2	%
$\Delta V_{OUT(\Delta VINB)}$	DC line regulation	V_{INB34} = 4.0 V to 5.0 V, I_{OUT}= I_{OUT_MAX}	QFN	-	2		mV/V
			WLCSP	-	9		
$\Delta V_{OUT(\Delta IOUT)}$	DC load regulation	0 mA < I_{OUT} < I_{OUT_MAX}, V_{INB34} = 4.2 V, V_{BUCK4} = 3.3 V		-	6		mV/A
$\Delta V_{OUT(\Delta IOUT)}$	Transient load response	I_{OUT} changes 0 to I_{OUT_MAX} (1A/us slope), V_{INB34} = 4.2 V, V_{BUCK4} = 3.3 V	QFN	-	160		mV
			WLCSP	-	175		
ΔV_{OUT}	Output voltage ripple	FPWM mode		-	10		mV
f_{SW}	Switching frequency in CCM	CCM		-	2		MHz
R_{DSON}	High side P-FET R_{DSON}	V_{INB34} = 3.8 V	QFN	-	95		mΩ
			WLCSP	-	75		
	Low side N-FET R_{DSON}	V_{INB34} = 3.8 V	QFN	-	54		mΩ
			WLCSP	-	40		
I_{LIM}	Peak inductor current limit	V_{INB34} = 3.8 V		3.5	4.1	4.7	A
t_{START}	Startup time	EN rising to 90 % of output voltage		-	700	900	µs
V_{soft_strup}	Soft-start slew rate	-		-	12.5		mV/us
R_{DIS}	Output active discharge resistance	-		-	100	150	Ω
BUCK_POK_Z	Output power good rising	-	QFN	85	90	95	%
			WLCSP	80	85	90	
BUCK_POK_F	Output power good falling	Programmed by BUCK4_POK_F[1:0] bits	QFN	71	75	79	%
				76	80	84	
				81	85	89	
		Fixed values	WLCSP	71	75	79	%
t_{POK_Deb}	POK debounce time	POK falling	-	-	300		µs
L	Inductor value	-	-	-	0.47		µH
C_{OUT}	Output capacitance	Minimum nominal capacitance	-	44			µF

[1] Output current of PF9453 regulators changes depending on the part number; refer to Table 2.

13.6 LDO_SNVS (Always-On LDO)

Table 105. LDO_SNVS (Always-On LDO)

Unless otherwise specified:

- ***WLCSP*** → *VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VLDO_SNVS = 1.8 V, Tamb = – 40 °C ~ +85 °C*
- ***QFN*** → *VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VINL1 = VINL2 = 3.8 V, VLDO_SNVS = 1.8 V, Tamb = – 40 °C to +105 °C*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Input voltage range	VSYS pin		2.5	-	5.5	V
I_Q	Quiescent current	Regulator enabled, No load			0.4	0.7	µA
I_{OUT_MAX}	Maximum output DC current	$V_{LDOSNVS}$ = 1.8 V		10	-	-	mA
I_{LIMIT}	Short current limit	Output shorted to GND		20		-	mA
V_{DO}	Dropout voltage	$I_{OUT} = I_{OUT\_MAX}$, V_{SYS} = 3.2 V, $V_{LDOSNVS}$ =3.3 V		-	25	50	mV
$V_{LDOSNVS}$	Nominal output voltage	I^2C Programmable, 25 mV step	QFN	1.2	-	3.4	V
			WLCSP	0.8	-	3	
	Default voltage	-		-	1.8	-	V
	DC accuracy	$V_{LDOSNVS}$ = 1.8 V, I_{Load} = 5mA		-3	-	3	%
V_{NOISE}	Output noise	f = 10 Hz to 10 kHz, I_{OUT} = 10 % of IMAX, VLDOSNVS = 1.8 V		-	450	-	µV
$\Delta V_{OUT(\Delta VINL\_DC)}$	DC Line regulation	$V_{LDOSNVS}$ +0.3 V < V_{SYS} < 5.5 V, IOUT = 10 % of IOUT_MAX		-	0.2	-	%/V
$\Delta V_{OUT(\Delta IOUT\_DC)}$	DC Load regulation	V_{SYS} = $V_{LDOSNVS}$ +0.3 V to 5.5 V, 0 mA < IOUT < IOUT_MAX		-	0.25	-	%
$\Delta V_{OUT(\Delta VINL\_AC)}$	Transient Line Response	$V_{LDOSNVS}$ +0.3 V < V_{SYS} < 5.5 V, I_{OUT} = 10 % of I_{OUT_MAX}		-	0.5	-	%/V
$\Delta V_{OUT(\Delta IOUT\_AC)}$	Transient Load Response	V_{SYS} = $V_{LDOSNVS}$ +0.3 V to 5.5 V, 1 mA < I_{OUT} < I_{OUT_MAX} , tr = 10 µs, $V_{LDOSNVS}$ = 1.8 V, T_{amb}= 25 °C		-1	-	1	%
PSRR	Power Supply Rejection ratio	f = 10 Hz to 10 kHz, I_{OUT} = 10 % of I_{OUT_MAX}		-	50	-	dB
V_{soft_strup}	Soft-start slew rate	I_{OUT} = 0 mA, 10 % to 90 % of $V_{LDOSNVS}$		-	6.0	-	mV/µs
V_{ov_srtup}	Overshoot at startup	I_{OUT} = 0 mA		-	-	10	mV
t_{EN}	Enable time	EN rising to 90 % of output voltage		-	700	1500	µs
LDO_POK	Output power good	Percentage of $V_{LDOSNVS}$ configuration		86	90	94	%
t_{POK_Deb}	POK debounce time	POK falling		-	300	-	µs
R_{DIS}	Active discharge resistance	-		50	100	150	Ω
C_{OUT}	Output capacitance	Minimum nominal capacitance		2.2	-	-	µF

13.7 LDO1

Table 106. LDO1

Unless otherwise specified:

- ***WLCSP*** →*VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, Tamb = – 40 °C ~ +85 °C*
- ***QFN*** → *VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VINL1 = VINL2 = 3.8 V, Tamb = – 40 °C to +105 °C*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Input voltage range	INL1 pin		2.5	-	5.5	V
I_Q	Quiescent current	Regulator enabled, No load	QFN	-	0.4	0.9	µA
			WLCSP	-	0.4	0.7	
I_{OUT_MAX}	Maximum output DC current	V_{LDO1} = 3.3 V		250	-	-	mA
I_{LIMIT}	Short current limit	Output shorted to GND		260	-	-	mA

Table 106. LDO1*...continued*

Unless otherwise specified:

- ***WLCSP*** *→VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, Tamb = – 40 °C ~ +85 °C*
- ***QFN*** *→ VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VINL1 = VINL2 = 3.8 V, Tamb = – 40 °C to +105 °C*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DO}	Dropout voltage	IOUT = IOUT_MAX, VINL1 = 3.2 V, L1_OUT = 3.3 V	QFN	-	80	120	mV
			WCSP	-	60	100	
V_{LDO1}	Nominal output voltage	I^2C Programmable, 25 mV/step		0.8		3.3	V
	Default voltage	SD_VSEL = Low	QFN	-	3.3	-	V
			WLCSP	-	0.8	-	
		SD_VSEL = High	QFN	-	1.8	-	
			WLCSP	-	0.8	-	
	DC accuracy	V_{LDO1} = 3.3 V, I_{Load} = 5 mA		-2		2	%
V_{NOISE}	Output noise	f = 10 Hz to 10 kHz, I_{OUT} = 10 % of IMAX, VLDO1 = 3.3 V			150		µV
$\Delta V_{OUT(\Delta VINL\_DC)}$	DC Line regulation	V_{LDO1} +0.3 V < V_{INL1} < 5.5 V, I_{OUT} = 10 % of IOUT_MAX			0.15		%/V
$\Delta V_{OUT(\Delta IOUT\_DC)}$	DC Load regulation	V_{INL1} = V_{LDO1} +0.3 V to 5.5 V, 0.1 mA < IOUT < IOUT_MAX, V_{LDO1} = 3.3 V	QFN		0.4		%
			WLSCP		0.15		
$\Delta V_{OUT(\Delta VINL\_AC)}$	Transient Line Response	V_{LDO1} +0.3 V < V_{INL1} < 5.5 V, I_{OUT} = 10 % of I_{OUT_MAX}, tr = 10 µs			0.5		%/V
$\Delta V_{OUT(\Delta IOUT\_AC)}$	Transient Load Response	V_{INL} = V_{LDO1} +0.3 V to 5.5 V, 1 mA < IOUT < IOUT_MAX , tr = 10 µs, VLDO1 = 3.3 V		-3		3	%
PSRR	Power Supply Rejection ratio	f = 10 Hz to 10 kHz, I_{OUT} = 10 % of IOUT_MAX			50		dB
V_{soft_strup}	Soft-start slew rate	I_{OUT} = 0 mA, 10 % to 90 % of V_{LDO1}			6.0		mV/µs
V_{ov_srtup}	Overshoot at startup	I_{OUT} = 0 mA				20	mV
t_{EN}	Enable time	EN rising to 90 % of output voltage, V_{LDO1} = 3.3 V			500	1800	µs
LDO_POK	Output power good	Percentage of V_{LDO1} configuration		86	90	94	%
t_{POK_Deb}	POK debounce time	POK falling			300		µs
R_{DIS}	Active discharge resistance				100	200	Ω
C_{OUT}	Output capacitance	Minimum nominal capacitance		4.7			µF

13.8 LDO2

Table 107. LDO2 (only for QFN package)

Unless otherwise specified, VSYS = 3.8 V, V_{INB12} = V_{INB34} = 3.8 V, V_{INL1} = V_{INL2} = 3.8 V, T_{amb}= –40 °C to +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage range	INL2 pin, VSYS > V_{LDO2} + 1.5 V	V_{LDO2} + V_{DO}	-	5.5	V
I_Q	Quiescent current	Regulator enabled, No load	-	0.5	1.0	µA
I_{OUT_MAX}	Maximum output DC current	V_{INL2} > V_{LDO2} + 0.2 V, V_{LDO2} = 0.8 V	200	-	-	mA
I_{LIMIT}	Short current limit	Output shorted to GND	260	-	-	mA
V_{DO}	Dropout voltage	I_{OUT} = I_{OUT_MAX}, V_{INL2} = 1.8 V, L2_OUT = 1.95 V, VSYS > V_{LDO2} + 1.5 V	-	120	195	mV
V_{LDO2}	Nominal output voltage	I^2C Programmable, 25 mV/step	0.5	-	1.95	V
	Default voltage	-	-	0.8	-	V

Table 107. LDO2 (only for QFN package)*...continued*

Unless otherwise specified, VSYS = 3.8 V, V_{INB12} = V_{INB34} = 3.8 V, V_{INL1} = V_{INL2} = 3.8 V, T_{amb}= –40 °C to +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	DC accuracy	V_{LDO2} = 0.8 V, I_{Load} = 5mA	-2	-	2	%
V_{NOISE}	Output noise	f = 10Hz to 10kHz, I_{OUT} = 10% of I_{MAX}, V_{LDO2} = 0.8 V	-	66	-	µV
$\Delta V_{OUT(\Delta VINL\_DC)}$	DC line regulation	V_{LDO2} + 0.3 V < V_{INL2} < 5.5 V, I_{OUT} = 10% of I_{OUT_MAX}	-	0.01	-	%/V
$\Delta V_{OUT(\Delta IOUT\_DC)}$	DC load regulation	V_{INL2} = V_{LDO2} + 0.3 V to 5.5 V, 0.1 mA < I_{OUT} < I_{OUT_MAX}, V_{LDO2} = 0.8 V	-	1.2	-	%
$\Delta V_{OUT(\Delta VINL\_AC)}$	Transient line response	V_{LDO2} + 0.3 V < V_{INL2} < 5.5 V, I_{OUT} = 10% of I_{OUT_MAX}, tr = 10us	-	3	-	%/V
$\Delta V_{OUT(\Delta IOUT\_AC)}$	Transient load response	V_{INL2} = V_{LDO2} + 0.3 V to 5.5 V, 1 mA < I_{OUT} < I_{OUT_MAX} , tr = 10us, V_{LDO2} = 0.8 V	-3.5	-	5	%
PSRR	Power supply rejection ratio	f = 10Hz to 10kHz, I_{OUT} = 10% of I_{OUT_MAX}	-	55	-	dB
V_{soft_strup}	Soft-start slew rate	I_{OUT} = 0mA, 10% to 90% of V_{LDO2}	-	4	-	mV/µs
V_{ov_srtup}	Overshoot at startup	I_{OUT} = 0mA	-	-	20	mV
t_{EN}	Enable time	EN rising to 90% of output voltage at V_{LDO2} = 0.8 V	-	200	250	µs
LDO2_POK	Output power good	Delta from V_{LDO2} Target	87	90	93	%
t_{POK_Deb}	POK debounce time	POK falling	-	300	-	µs
R_{DIS}	Active discharge resistance	-	-	100	180	Ω
C_{OUT}	Output capacitance	Minimum nominal capacitance	2.2	-	10	µF

13.9 LSW (load switch)

Table 108. LSW (load switch)

Unless otherwise specified:

- ***WLCSP*** *→VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VLSWIN = 3.3 V, Tamb = – 40 °C ~ +85 °C*
- ***QFN*** *→ VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VINL1 = VINL2 = 3.8 V, VLSWIN = 3.3 V, Tamb = – 40 °C to +105 °C*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{LSWIN}	Input voltage range	LSWIN pin	QFN	1.8	-	VSYS	V
			WLCSP	1.2	-	5.5	
I_Q	Quiescent current	Switch enabled, No load, V_{LSWIN} = 3.3 V	QFN	-	5	8	µA
		Enabled, No load, VLSWIN=1.8V	WLCSP	-	0.5	50	nA
I_{SHDN}	Shutdown current	V_{LSWIN} = 3.3 V	QFN	-	50	5000	nA
			WLCSP	-	5	700	nA
I_{OC}	Overcurrent threshold	-	QFN	-	700	-	mA
I_{SC}	Short circuit current threshold	-	QFN	-	1.3	-	A
R_{DSON}	Switch ON resistance	V_{LSWIN} = 1.8 V, I_{LOAD} = 150 mA	QFN	-	210	280	mΩ
			WLCSP	-	150	220	mΩ
t_{EN}	Enable time	Time to LSWOUT 10 % from EN, V_{LSWIN} = 3.3 V, C_{LSW} = 10µF	QFN	-	30	50	µs
		Time to LSWOUT 10 % from EN, VLSWIN = 1.8 V	WLSCP	-	70	110	µs
t_{ON}	Output rise time	C_{LSW} = 10 µF, V_{LSWIN} = 3.3 V, LSWOUT 10 % to 90 %, no load	QFN	-	50	100	µs
		CLSW = 10 µF, VLSWIN = 3.3 V, LSWOUT 10 % to 90 %, no load	WLSCP	-	150	300	µs

Table 108. LSW (load switch)...*continued*

Unless otherwise specified:

- ***WLCSP*** →*VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VLSWIN = 3.3 V, Tamb = – 40 °C ~ +85 °C*
- ***QFN*** → *VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VINL1 = VINL2 = 3.8 V, VLSWIN = 3.3 V, Tamb = – 40 °C to +105 °C*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{DIS}	Active discharge resistance	Load switch is off	-	-	95	150	Ω

13.10 I^2C interface and logic I/O

Table 109. I^2C interface and logic I/O

Unless otherwise specified:

- ***WLCSP*** → *VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VLSWIN = 3.3 V, Tamb = – 40 °C ~ +85 °C*
- ***QFN*** → *VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VINL1 = VINL2 = 3.8 V, VLSWIN = 3.3 V, Tamb = – 40 °C to +105 °C*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SCL, SDA						
f_{I2C}	I^2C Clock frequency	-	-	-	1	MHz
V_{IH}	High-level Input voltage	SCL, SDA; V_{SYS} = 3.0 V to 5.5 V	1.2	-	-	V
V_{IL}	Low-level Input voltage	SCL, SDA; V_{SYS} = 3.0 V to 5.5 V	-	-	0.4	V
V_{hys}	Hysteresis of Schmitt trigger inputs	-	0.01	-	-	V
V_{OL}	Low-level output voltage	SDA, I_{load} = 20 mA, VSYS = 3.0 V to 5.5 V	0	-	0.4	V
$t_{HD,STA}$	Hold time (repeated) START condition	Fast mode plus; After this period, the first clock pulse is generated	0.26	-	-	µs
t_{LOW}	LOW period of I^2C clock	Fast mode plus	0.5	-	-	µs
t_{HIGH}	HIGH period of I^2C clock	Fast mode plus	0.26	-	-	µs
$t_{SU,STA}$	Setup time (repeated) START condition	Fast mode plus	0.26	-	-	µs
$t_{HD,DAT}$	Data hold time	Fast mode plus	0	-	-	µs
$t_{SU,DAT}$	Data setup time	Fast mode plus	50	-	-	ns
t_r	Rise time of I2C_SCL and I2C_SDA signals	Fast mode plus	-	-	120	ns
t_f	Fall time of I2C_SCL and I2C_SDA signals	Fast mode plus	-	-	120	ns
$t_{SU,STO}$	Setup time for STOP condition	Fast mode plus	0.26	-	-	µs
t_{BUF}	Bus free time between STOP and START condition	Fast mode plus	0.5	-	-	µs
$t_{VD,DAT}$	Data valid time	Fast mode plus	-	-	0.45	µs
$t_{VD,ACK}$	Data valid acknowledge time	Fast mode plus	-	-	0.45	µs
t_{SP}	Pulse width of spikes that must be suppressed by input filter	-	0	-	50	ns

13.11 32.768 kHz crystal driver

Table 110. 32.768 kHz crystal driver

Unless otherwise specified:

- ***WLCSP*** → *VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VLSWIN = 3.3 V, Tamb = – 40 °C ~ +85 °C*
- ***QFN*** →*VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VINL1 = VINL2 = 3.8 V, VLSWIN = 3.3 V, Tamb = – 40 °C to +105 °C*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CLK}	Clock frequency	External 32.768 kHz crystal oscillator	-	32.768	-	kHz
t_{32K_STABLE}	Oscillator stabilization time	-	-	1000	-	ms

Table 110. 32.768 kHz crystal driver...*continued*

Unless otherwise specified:

- ***WLCSP*** *→ VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VLSWIN = 3.3 V, Tamb = – 40 °C ~ +85 °C*
- ***QFN*** *→VSYS = 3.8 V, VINB12 = VINB34 = 3.8 V, VINL1 = VINL2 = 3.8 V, VLSWIN = 3.3 V, Tamb = – 40 °C to +105 °C*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Duty	Output duty cycle	-	30	50	70	%
V_{OL}	Output low level	V_{LDO_SNVS} = 1.8 V, I_{OL} = 1 mA	-	-	0.4	V
V_{OH}	Output high level	V_{LDO_SNVS} = 1.8 V, I_{OH} = 1 mA	1.6	-	-	V

14 PF9453 OTP version

The PF9453 can be configured to each regulator default voltage and start-up sequence from the internal OTP configuration. Table 111 shows each OTP configuration for all devices.

Table 111. PF9453 OTP configuration

Functional Block	Register	Feature	MPF9453AVMXXHN	MPF9453ACMXXUKR2
BUCK1	0x10 (BUCK1CTRL)	Buck1 enable mode	ON at RUN State (default)	ON at RUN State (default)
	0x10 (BUCK1CTRL)	Forced PWM mode	Automatic PFM and PWM mode transition (default)	Automatic PFM and PWM mode transition (default)
	0x10 (BUCK1CTRL)	Buck1 Active discharge	Enable Active discharge resistor when regulator is OFF(default)	Enable Active discharge resistor when regulator is OFF(default)
	0x11 (BUCK1OUT)	BUCK1 Output voltage	1.1	1.1
	0x3D (BUCK_POK_F_ CFG)	BUCK1 POK falling threshold	75% of output voltage (default)	**NA**
	Internal OTP register bits	BUCK1 Sequence	T4 (Default)	T4 (Default)
BUCK2	0x14 (BUCK2CTRL)	Buck2 enable mode	ON at RUN State (default)	ON at RUN State (default)
	0x14 (BUCK2CTRL)	Forced PWM mode	Automatic PFM and PWM mode transition (default)	Automatic PFM and PWM mode transition (default)
	0x14 (BUCK2CTRL)	Buck2 Active discharge	Enable Active discharge resistor when regulator is OFF(default)	Enable Active discharge resistor when regulator is OFF(default)
	0x14 (BUCK2CTRL)	BUCK2 DVS speed	25 mV / 2 µs (default)	25 mV / 2 µs (default)
	0x15 (BUCK2OUT)	BUCK2 Output voltage	0.85	0.85
	0x1F (BUCK2OUT_MAX_ LIMIT)	BUCK2 output voltage maximum limit	0.9 **(0.95 for PPF9453AVMA2HN)**	0.9
	0x20 (BUCK2OUT_MIN_ LIMIT)	BUCK2 output voltage minimum limit	0.6125	0.6125
	0x3D (BUCK_POK_F_ CFG)	BUCK2 POK falling threshold	75% of output voltage (default)	**NA**
	Internal OTP register bits	BUCK2 Sequence	T1 (Default)	T1 (Default)
BUCK3	0x21 (BUCK3CTRL)	BUCK3 enable mode	ON at RUN State (default)	ON at RUN State (default)
	0x21 (BUCK3CTRL)	Forced PWM mode	Automatic PFM and PWM mode transition (default)	Automatic PFM and PWM mode transition (default)
	0x21 (BUCK3CTRL)	BUCK3 Active discharge	Enable Active discharge resistor when regulator is OFF(default)	Enable Active discharge resistor when regulator is OFF(default)
	0x22 (BUCK3OUT)	BUCK3 Output voltage	1.8	1.8
	0x3D (BUCK_POK_F_ CFG)	BUCK3 POK falling threshold	75% of output voltage (default)	**NA**
	Internal OTP register bits	BUCK3 Sequence	T3 (Default)	T3 (Default)
BUCK4	0x2E (BUCK4CTRL)	BUCK4 enable mode	ON at RUN State (default)	ON at RUN State (default)
	0x2E (BUCK4CTRL)	Forced PWM mode	Automatic PFM and PWM mode transition (default)	Automatic PFM and PWM mode transition (default)
	0x2E (BUCK4CTRL)	Buck4 Active discharge	Enable Active discharge resistor when regulator is OFF(default)	Enable Active discharge resistor when regulator is OFF(default)

Table 111. PF9453 OTP configuration*...continued*

Functional Block	Register	Feature	MPF9453AVMXXHN	MPF9453ACMXXUKR2
	0x2F (BUCK4OUT)	BUCK4 Output voltage	3.3	3.3
	0x3D (BUCK_POK_F_CFG)	BUCK4 POK falling threshold	75% of output voltage (default)	**NA**
	Internal OTP register bits	BUCK4 Sequence	T5 (Default)	T5 (Default)
LDO1	0x36 (LDO1_OUT_L)	LDO1 output voltage when SD_VSEL pin = Low	3.3	0.8
	0x37 (LDO1_CFG)	LDO1 Enable mode	ON at RUN State (default)	ON at RUN State (default)
	0x37 (LDO1_CFG)	LDO1 Active discharge control during OFF	Enable Active discharge resistor when regulator is OFF(default)	Enable Active discharge resistor when regulator is OFF(default)
	0x37 (LDO1_CFG)	LDO1 Active discharge control during ON	Enable Active discharge resistor for 2ms during LDO1 transition only from 3.3V to 1.8V by toggling SD_VSEL pin (default)	Enable Active discharge resistor for 2ms during LDO1 transition only from 3.3V to 1.8V by toggling SD_VSEL pin (default)
	0x38 (LDO1_OUT_H)	LDO1 Output voltage when SD_VSEL pin = High	1.8	0.8
	Internal OTP register bits	LDO1 sequence	T6 (Default)	T2 (Default)
LDO_SNVS	0x39 (LDOSNVS_CFG1)	LDO_SNVS output voltage	1.8	1.8
	0x39 (LDOSNVS_CFG1)	SNVS LDO Active discharge enable	Enable Active discharge resistor when regulator is OFF (default)	Enable Active discharge resistor when regulator is OFF (default)
LDO2	0x3B (LDO2_CFG)	LDO2 Enable mode	ON at RUN State (default)	**NA**
	0x3B (LDO2_CFG)	Total Output capacitor selection	Auto Cout detection (default)	**NA**
	0x3B (LDO2_CFG)	Output trace resistance compensation	15 mohm (default)	**NA**
	0x3B (LDO2_CFG)	LDO2 Active discharge enable	Enable Active discharge resistor when regulator is OFF (default)	**NA**
	0x3C (LDO2_OUT)	LDO2 output voltage	0.8	**NA**
	0x3C (LDO2_OUT)	INL2 voltage selection, effective only when L2_INL2_MDET = 1b	(VSYS – VINL2) > 0.7V (default)	**NA**
	0x3C (LDO2_OUT)	Manual detection for INL2 supply	Auto detection (default)	**NA**
	Internal OTP register bits	LDO2 Sequence	T2 (Default)	**NA**
Load Switch	0x40 (LSW_CTRL1)	Load SW Enable mode	Enabled by LSW_EN pin (default)	Enabled by LSW_EN pin (default)
	0x40 (LSW_CTRL1)	Load SW active discharge	Enabled when Load SW1 is off (default)	Enabled when Load SW1 is off (default)
	Internal OTP register bits	LoadSwitch Sequence	T5 (Default)	T5 (Default)
PWR_SEQ_CTRL	0x0A (PWR_SEQ_CTRL)	Time step configuration during power down sequence	8 ms (default)	8 ms (default)
	0x0A (PWR_SEQ_CTRL)	Time step configuration during power on sequence	2 ms (default)	2 ms (default)
	0x0A (PWR_SEQ_CTRL)	Debounce time for PMIC_RST_B pin for falling edge.	20 ms (default)	**NA**
	0x0A (PWR_SEQ_CTRL)	Configure PMIC_RST_B pin as Power ON source	Mask (default)	**NA**
SYS_CFG2	0x0C (SYS_CFG2)	VSYS UVLO threshold, rising threshold	2.85 V (default)	2.85 V (default)
	0x0C (SYS_CFG2)	POK reference during power up	POK is reference to turn on next power group (default)	POK is reference to turn on next power group (default)
	0x0C (SYS_CFG2)	ONKEY timer configuration after PMIC_RST_B pin falls low	2 sec (default)	**NA**
RESET_CTRL	0x08 (RESET_CTRL)	Time to stay regulators off during Cold reset	250 ms (default)	250 ms (default)

Table 111. PF9453 OTP configuration*...continued*

Functional Block	Register	Feature	MPF9453AVMXXHN	MPF9453ACMXXUKR2
	0x08 (RESET_CTRL)	When PMIC_RST_B is asserted to low, PMIC reset behavior	Cold Reset, all voltage regulators are recycled (default)	**NA**
	0x08 (RESET_CTRL)	When WDOG_B is asserted to low, PMIC reset behavior	WDOG_B reset is disabled (default)	WDOG_B reset is disabled (default)

15 Package outline

15.1 Package outline for QFN

The PF9453 QFN uses a 40-pin QFN 5.0 mm x 5.0 mm with exposed pad, case number 98ASA02134D.

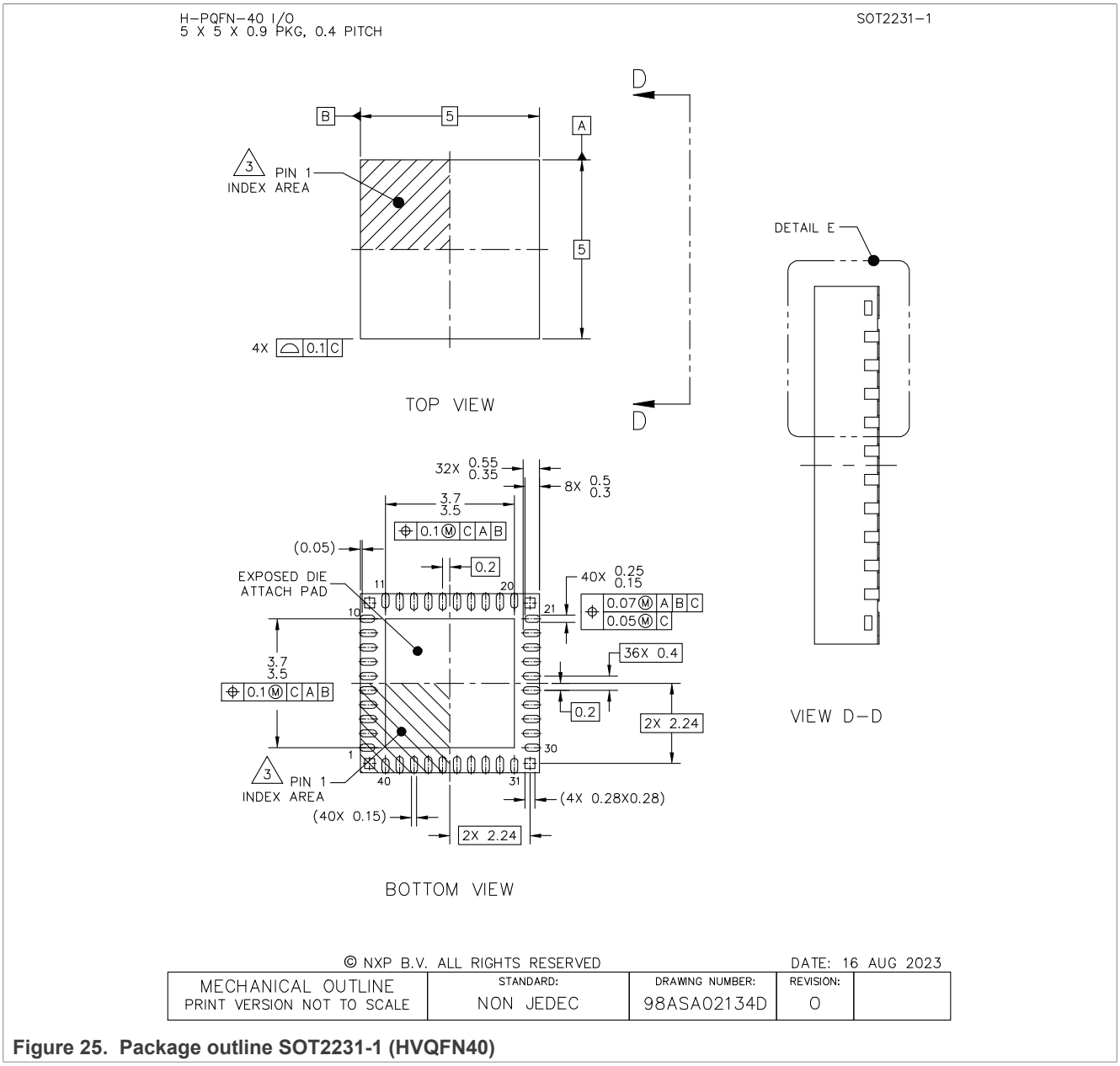
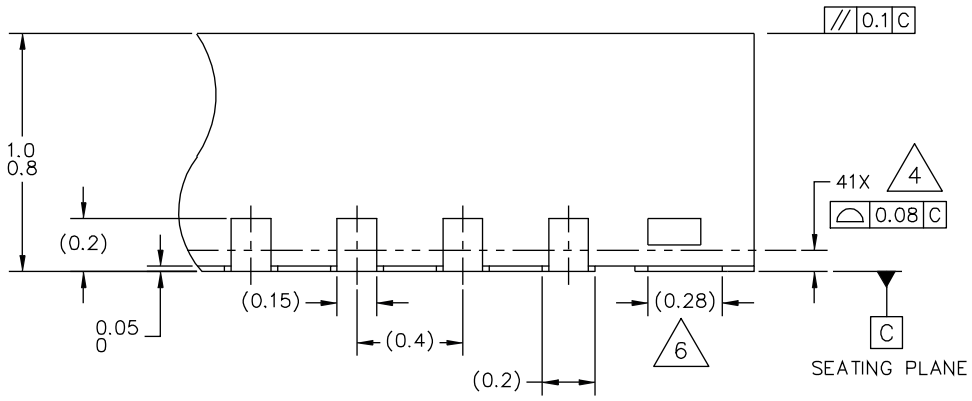


Figure 25. Package outline SOT2231-1 (HVQFN40)

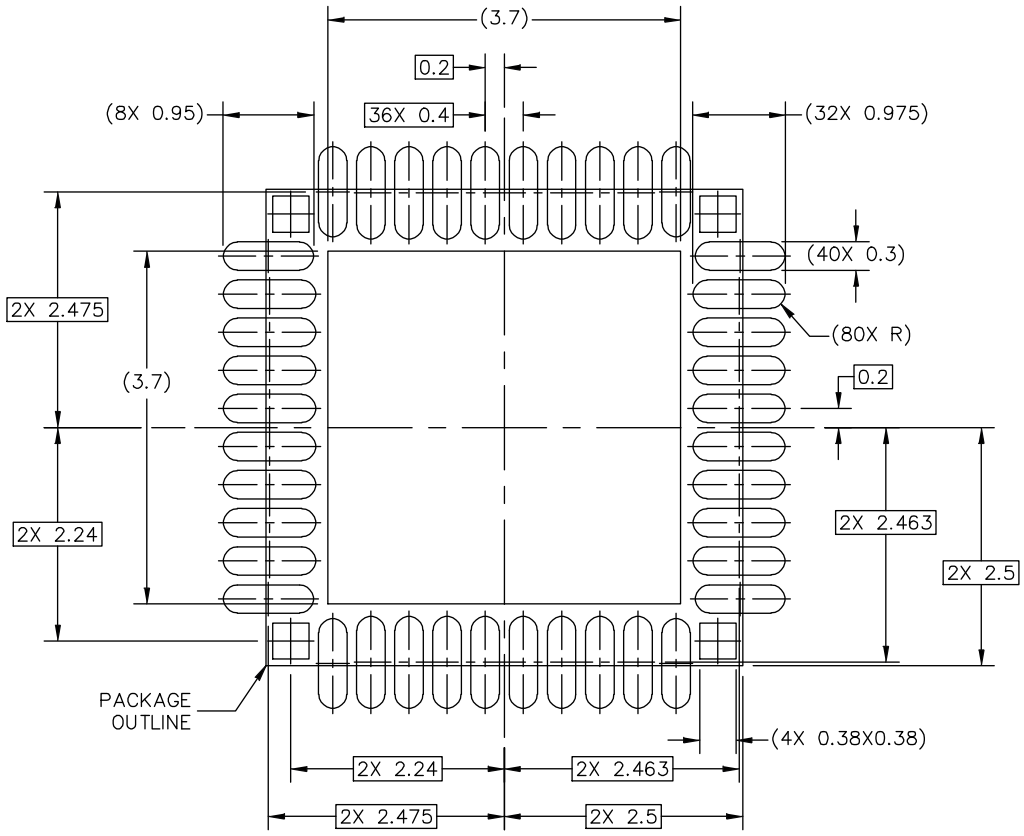


DETAIL E
VIEW ROTATED 90° CW

DATE: 16 AUG 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02134D	REVISION: O	

Figure 26. Package outline SOT2231-1 (HVQFN40) detail E



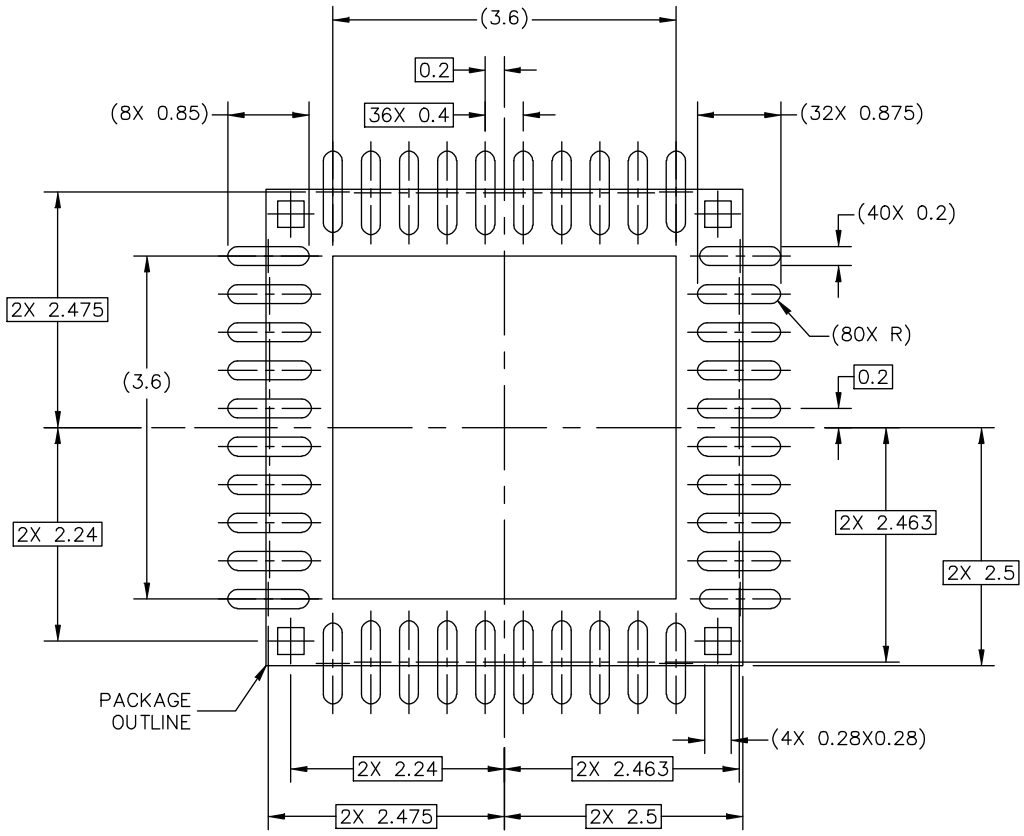
PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 16 AUG 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02134D	REVISION: O	

Figure 27. SOT2231-1 solder mask opening pattern



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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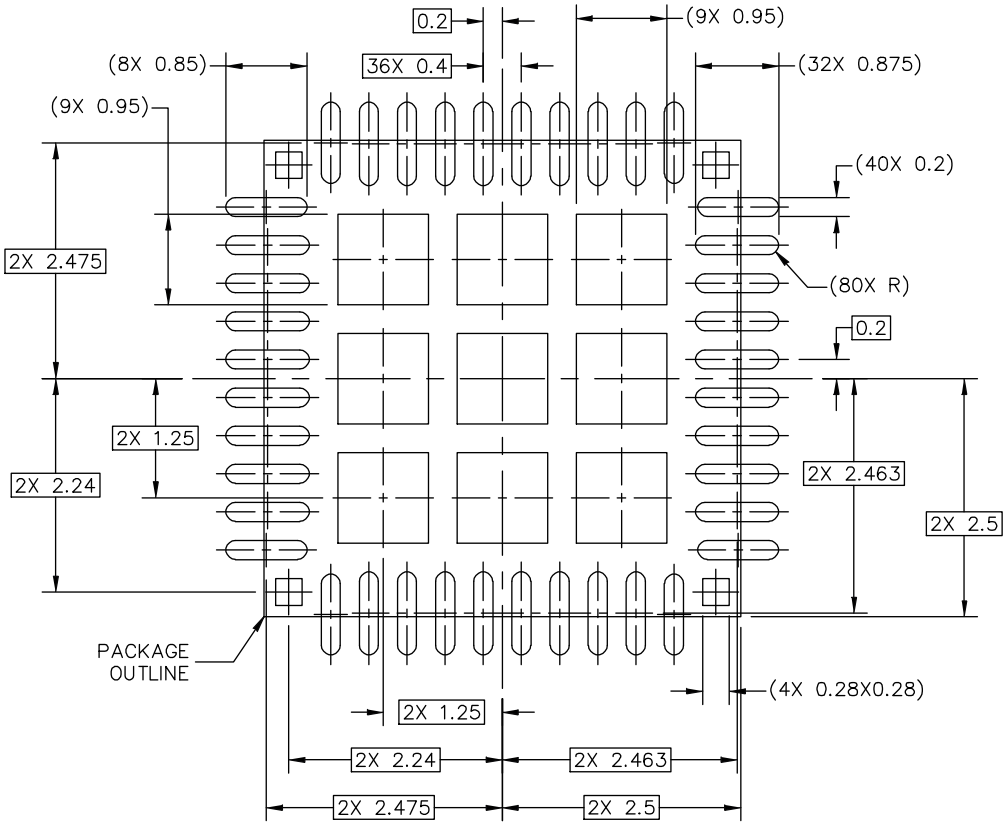
DATE: 16 AUG 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02134D	REVISION: O	

Figure 28. SOT2231-1 I/O pads and solderable area



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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DATE: 16 AUG 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02134D	REVISION: O	

Figure 29. SOT2231-1 solder paste stencil

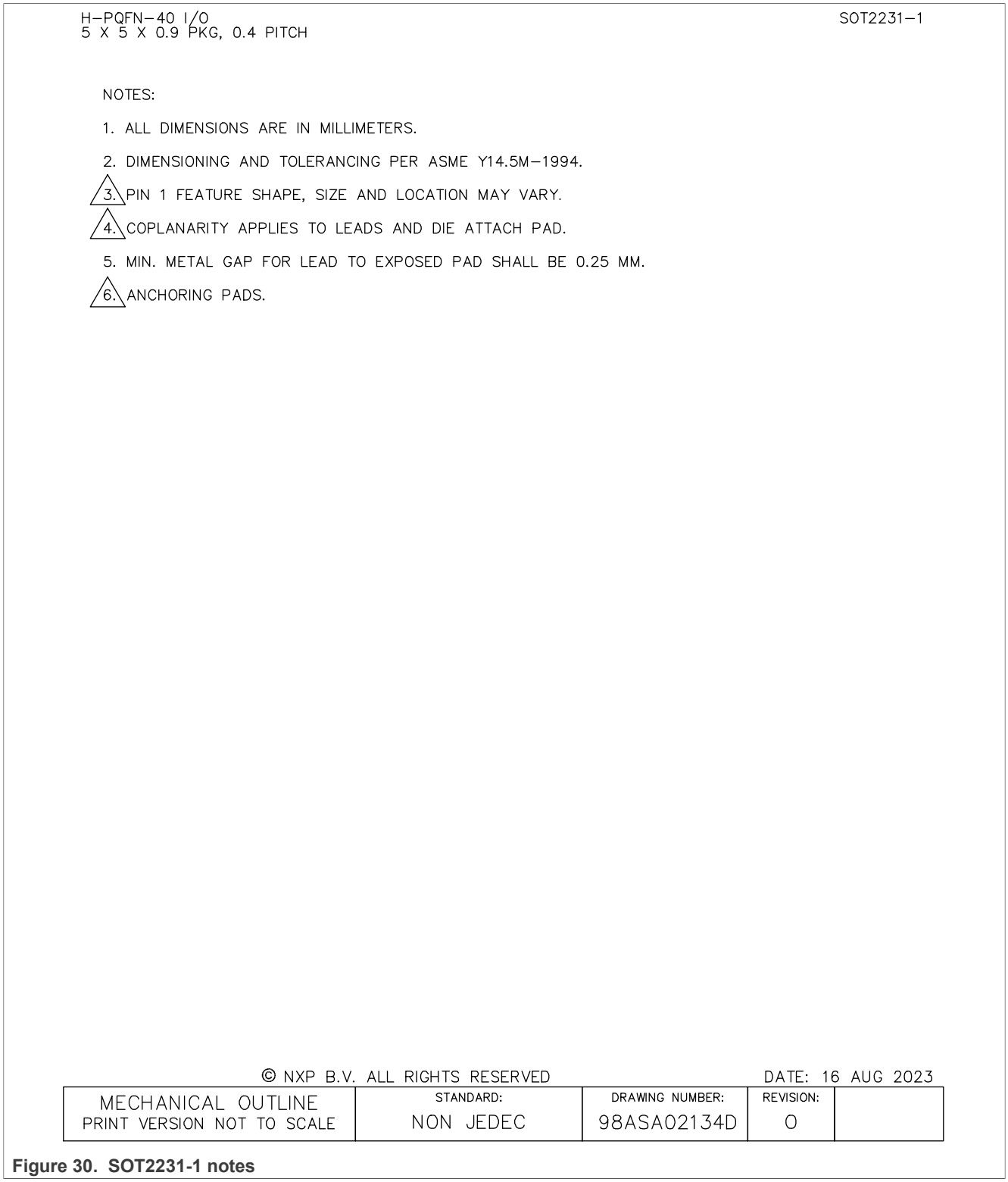


Figure 30. SOT2231-1 notes

15.2 Package outline for WLCSP

The PF9453 WLCSP uses a 36 bumps Wafer level chip scale 2.46 mm x 2.46 mm with 0.4 mm pitch, case number 98ASA02052D.

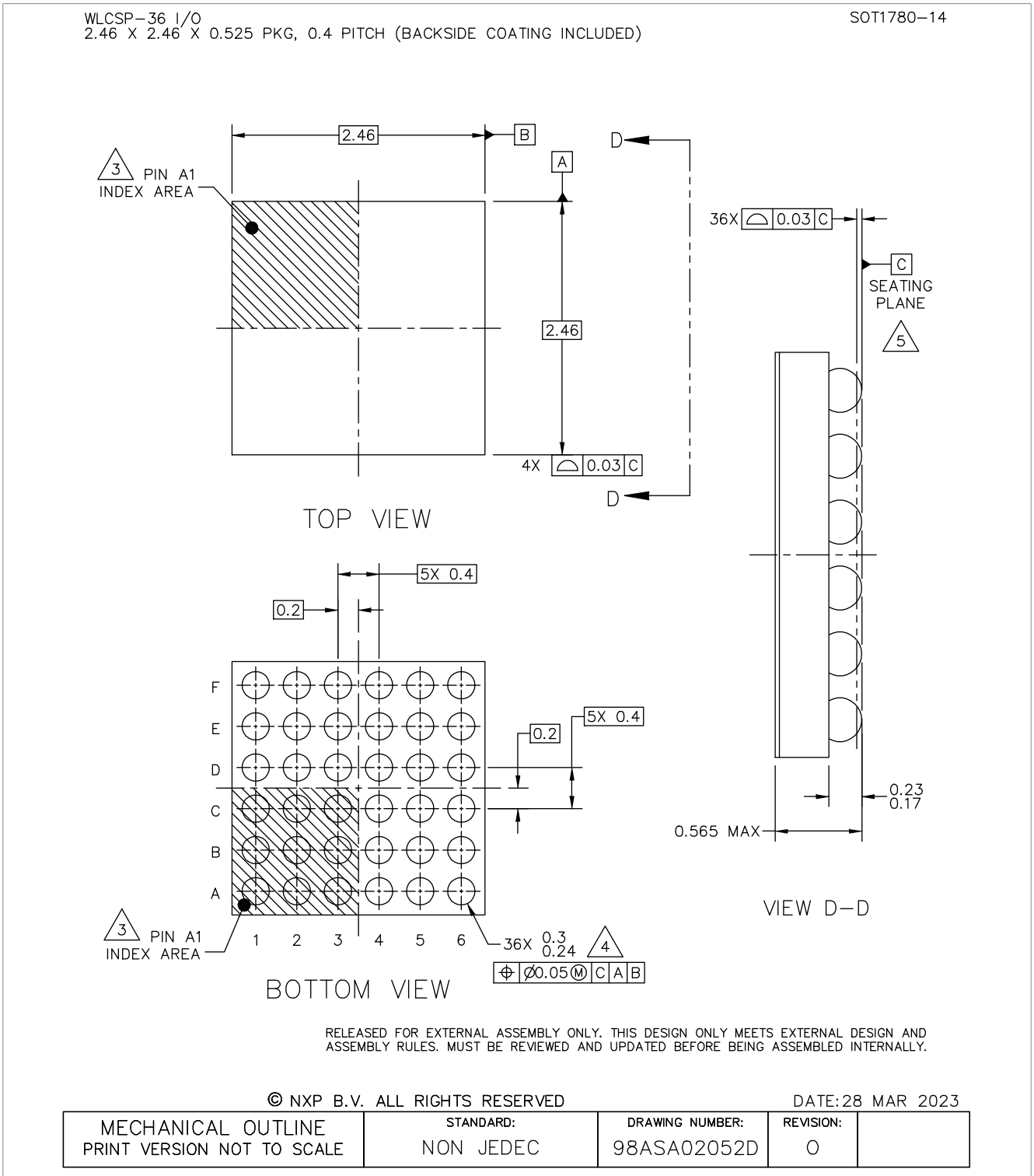


Figure 31. Package outline WLCSP36

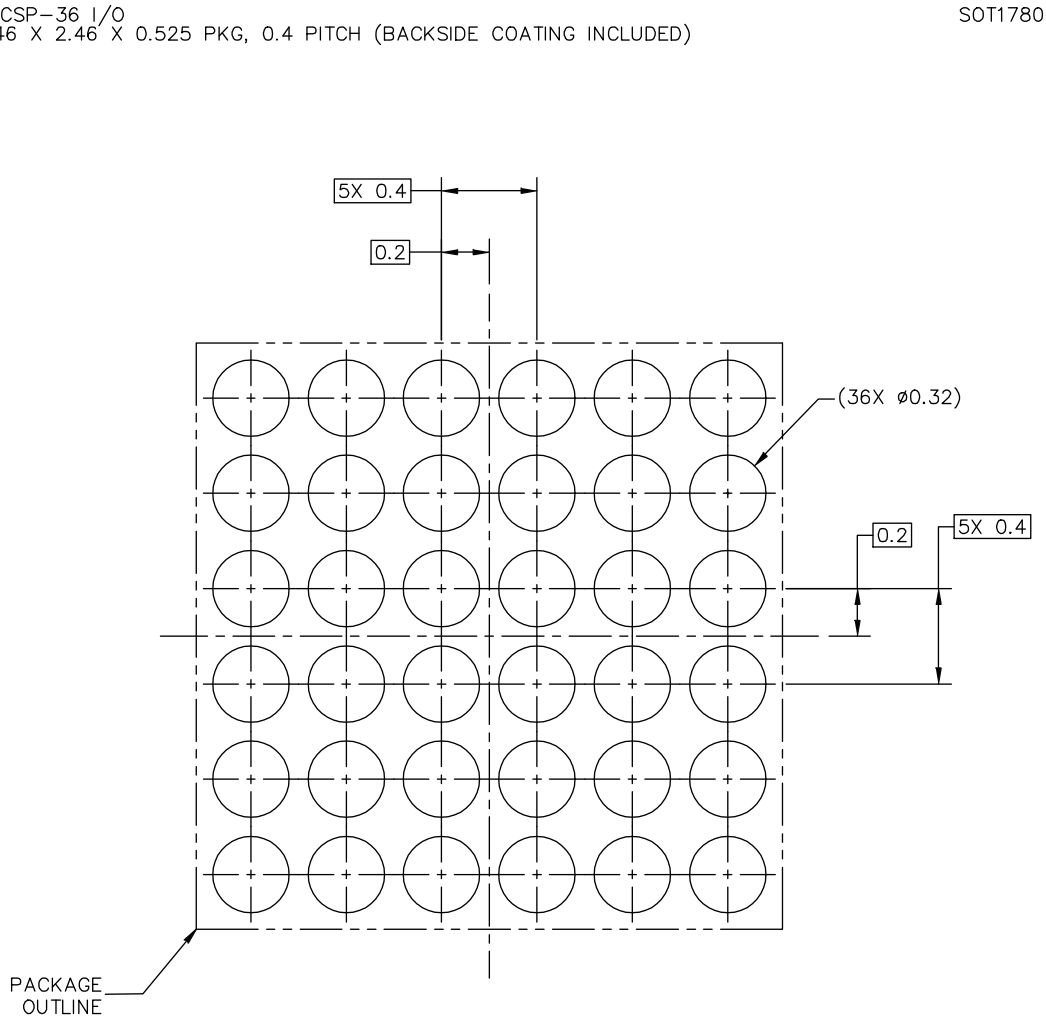
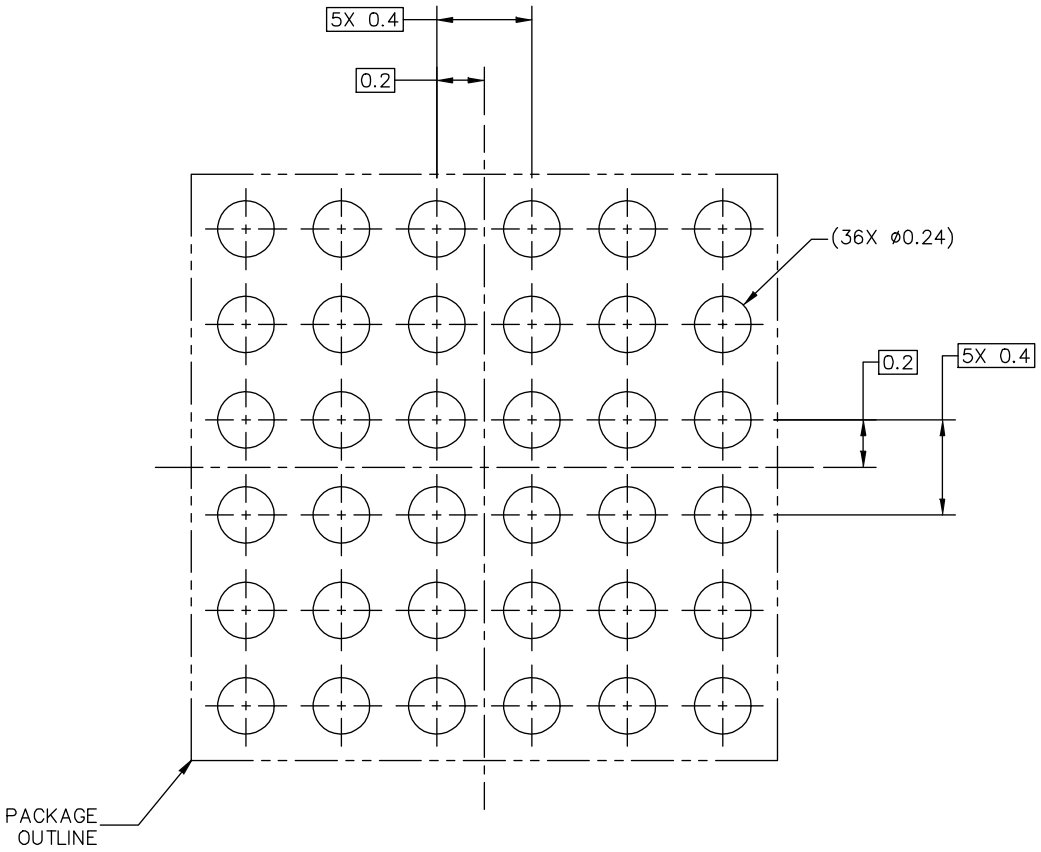


Figure 32. SOT1780-14 solder mask opening pattern

WLCSP−36 I/O
2.46 X 2.46 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1780−14



PCB DESIGN GUIDELINES − I/O PADS AND SOLDERABLE AREA

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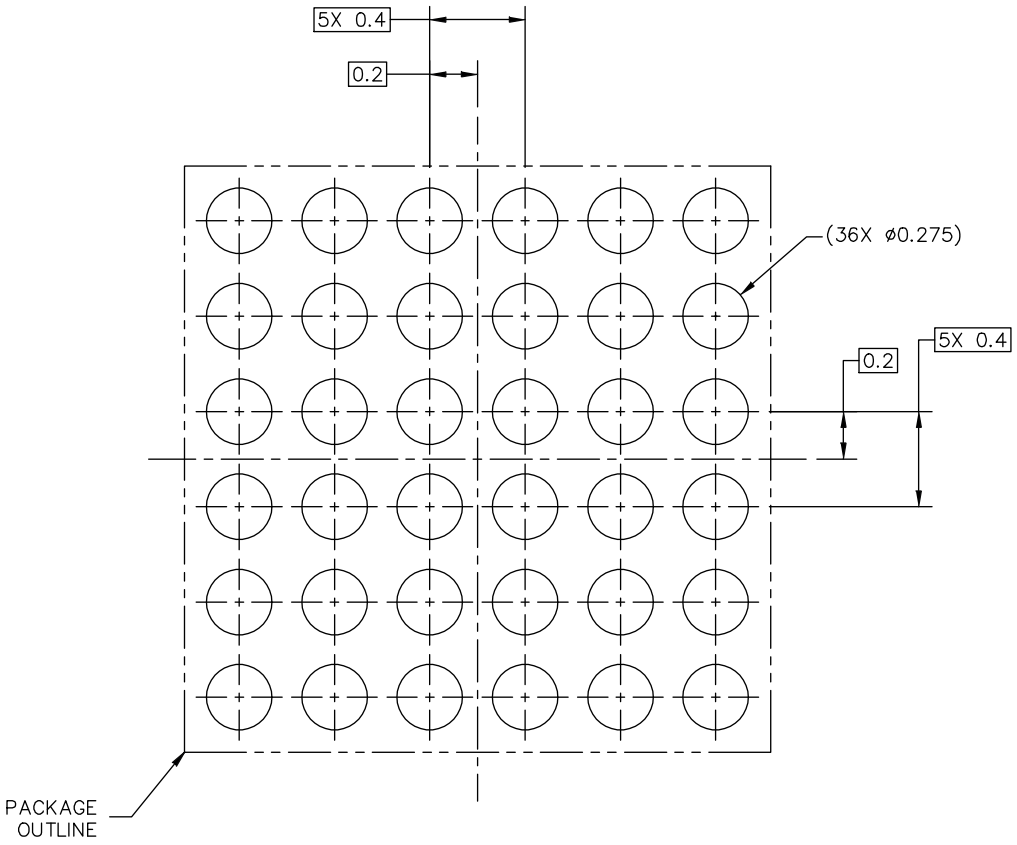
DATE: 28 MAR 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02052D	REVISION: O	

Figure 33. Package outline WLCSP36

WLCSP−36 I/O
2.46 X 2.46 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1780−14



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES − SOLDER PASTE STENCIL

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DATE: 28 MAR 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02052D	REVISION: O	

Figure 34. Package outline WLCSP36

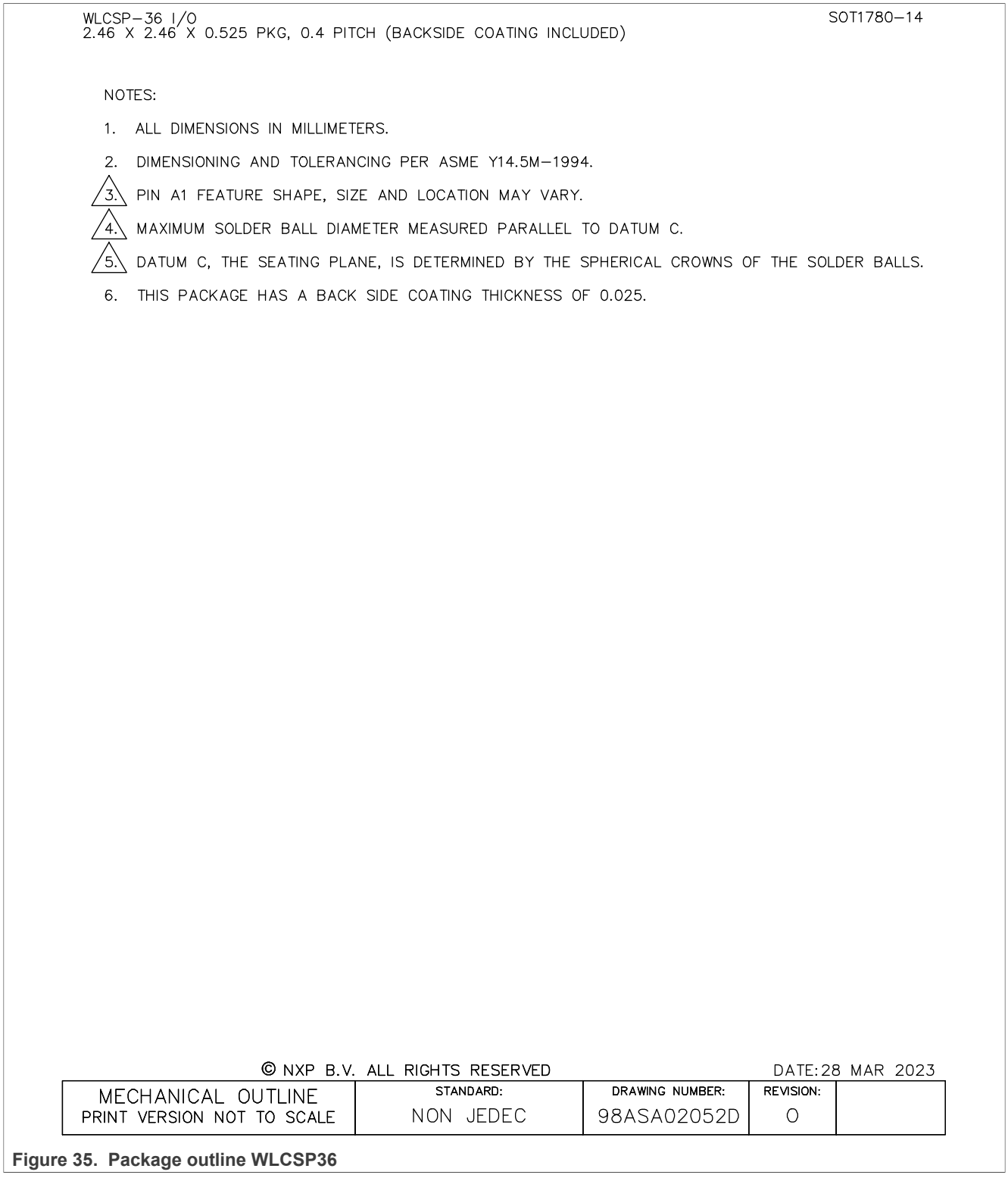

Figure 35. Package outline WLCSP36

16 Revision history

Table 112. Revision history

Document ID	Release date	Description
PF9453 v.2.0	26 November 2025	Updates: • Table 19: Updated "0011 — PF9453 WLCSP (default)". • Table 78: Table added • Table 97: Updated QFN and WLSCP conditions • Table 98: Updated QFN and WLSCP conditions • Table 99: Updated QFN and WLSCP conditions • Table 100: Updated QFN and WLSCP conditions • Table 101: Updated QFN and WLSCP conditions • Table 102: Updated QFN and WLSCP conditions • Table 103: Updated QFN and WLSCP conditions • Table 104: Updated QFN and WLSCP conditions • Table 106: Updated QFN and WLSCP conditions • Table 108: Updated QFN and WLSCP conditions • Section 15: Updated package outline of WLSCP
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Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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