



2605271814 New Assembly, Test and Ship Site and MOQ Change for BGM11S

PCN Issue Date: May 27, 2026

Effective Date: Sep 02, 2026

PCN Type: Assembly; Test

Description of Change

Silicon Labs is pleased to announce the successful qualification of ASE Chung-Li as a new assembly, test, and ship site for BGM11S. There are no changes to the test program, data sheet parameters, test platform, or test hardware for the new test site qualification. The tray capacity will be updated from 260 to 377 units, and the Minimum Order Quantity (MOQ) for tray orders will be adjusted from 1300 to 1885 units accordingly.

Package reliability stresses, including Preconditioning, Temperature Cycling, High Temperature Storage Life (HTSL), and Unbiased Highly Accelerated Stress Test (uHAST), have been successfully completed and passed. Temperature Humidity Bias (THB) qualification is currently in progress, with partial lots completed due to socket board limitations. Based on existing reliability stress results, THB qualification is expected to pass. Final results will be published prior to the PCN effective date and will be available upon request.

ASE Chung-Li is an existing assembly, test and ship site for Silicon Labs, and is certified to ISO9001, ISO14001 and IATF 16949.

ASE Chung-Li Ship Address:
ASE Chung-Li
No. 550, Chung-Hwa Road, Section 1,
Chung-Li, Taoyuan, 320, Taiwan

As of the effective date of the PCN, Silicon Labs will supply BGM11S modules from new qualified site.

Software Impact Description

Not Applicable

Reason for Change

Ensure supply continuity

Impact on Form, Fit, Function, Quality, Reliability

There is no change on form, function, quality or reliability

Product Identification

Existing Part #
BGM11S12F256GA-V2
BGM11S12F256GA-V2R
BGM11S22F256GA-V2
BGM11S22F256GA-V2R
BM11S12P1263GA
BM11S12P1263GAR
BM11S12P1452GA
BM11S12P1452GAR
BM11S22P1419GA
BM11S22P1419GAR
BM11S22P1680GA

BM11S22P1680GAR

Last Date of Unchanged Product: Sep 02, 2026

Qualification Samples

Available upon request

Customer Response

Lack of acknowledgment of the PCN within 30 days constitutes acceptance of the change, Ref. JEDEC-J-STD-046.

To request further data or inquire about this notification, please contact your Silicon Labs sales representative. A list of Silicon Labs sales representatives is available at <https://www.silabs.com>.

Customers may approve early PCN acceptance by emailing approval, along with PCN # to PCN@silabs.com

User Registration

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Qualification Data

Qualification report is attached in the Appendix

BGM11S Qualification report



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Part Rev A, TSMC Fabrication, Assembly except as noted

Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
Test Group A – Accelerated Environment Stress Tests (ASEKr)							
THB	JA101	3 lots, N=>25	Q044388	0/26	1	3 lots 0/78	Pass
	85°C, 85%RH		Q044229	0/26	1, 4		
	Vcc=3.8V, 1000 hours		Q044230	0/26	1, 4		
Temp Cycle	JA104	3 lots, N=>25	Q044381	0/25	1	3 lots 0/75	Pass
	Cond B: -55°C to 125°C		Q044382	0/25	1		
	500 cycles		Q044225	0/25	1, 4		
HTSL	JA103	3 lots, N=>25	Q044399	0/25	1	3 lots 0/75	Pass
	150°C, 1000hr		Q044400	0/25	1		
			Q044227	0/25	1, 4		
UHASt	JA110	3 lots, N=>25	Q052712	0/25	1, 5	3 lots 0/75	Pass
	130°C, 85%RH		Q052713	0/25	1, 5		
	96 hours		Q052714	0/25	1, 5		
Test Group A – Accelerated Environment Stress Tests (ASECL)							
THB	JA101	3 lots, N=>25	Q052874	0/21	1	3 lots 0/55	In-progress
	85°C, 85%RH		Q052875	0/17	1		
	Vcc=3.8V, 1000 hours		Q052876	0/17	1		
Temp Cycle	JA104	3 lots, N=>25	Q052868	0/25	1	3 lots 0/75	Pass
	Cond C: -65°C to 150°C		Q052869	0/25	1		
	500 cycles		Q052870	0/25	1		
HTSL	JA103	3 lots, N=>25	Q052871	0/25	1	3 lots 0/75	Pass
	150°C, 1000hr		Q052872	0/25	1		
			Q052873	0/25	1		
UHASt	JA110	3 lots, N=>25	Q053078	0/25	1	3 lots 0/75	Pass
	130°C, 85%RH		Q053079	0/25	1		
	96 hours		Q053080	0/25	1		
Test Group B – Accelerated Lifetime Simulation Tests							
HTOL	JA108	3 lots, N=>77	Q038136	0/80	2	4 lots 0/290	Pass
	T _j ≥ 125°C, Dynamic		Q038102	0/53	2		
	Vcc=3.8V, 1000 hours		Q037998	0/78	2		
			Q037622	0/79	2		
LTOL	JA108	1 lot, N=>32	Q037624	0/40	2	1 lot 0/40	Pass
ELFR	JA108	3 lots, N=>500	Q038755	0/501	2	4 lots 0/2021	Pass
	T _j ≥ 125°C, Dynamic		Q037570	0/508	2		
	Vcc=3.8V, 48 hours		Q037999	0/507	2		
			Q038137	0/505	2		
NVM Endurance, Retention and Operating Life	JA117	3 lots, N=>39	Q038147	0/40	2	3 lots 0/120	Pass
	25°C						
	500 hours						

Approved by: Kelvin Lee

Prepared on : 11-May-26

BGM11S Qual report_1

BGM11S Qualification report



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Part Rev A, TSMC Fabrication, Assembly except as noted

Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
NVM Endurance, Retention and Operating Life	JA117	3 lots, N=>39	Q038066	0/40	2	4 lots 1/159	Pass
	125°C		Q038028	0/40	2		
	1000 hours		Q038024	1/39	2, 3		
			Q037652	0/40	2		
Test Group E – Electrical Verification							
ESD-HBM	JS-001	1 lot, N=>3	Q040933		2	2 kV	Class 2
ESD-CDM	JESD22-C101	1 lot, N=>3	Q040932		2	500 V	Class II
			Q052941			500 V	
Latch Up	JESD78 ±200mA Overvoltage = 2.85V	1 lot, N=>3	Q040936	125 °C	2		Pass

Notes:

1. Parts are Pre-conditioned at MSL3/260°C
2. Leveraged die family qualification data
3. Failure analysis on the failure was inconclusive. An additional 40 units were stressed from the same wafer lot (Q038028) to reduce the LTPD% below the requirement. LTPD% = 5.76 at 90% confidence with 0 fails and a sample size =40.
4. Leveraged package family qualification data
5. ASEKR/ASECL joint partial shield assembly

This report applies to the following part numbers:

BGM11S12F256GA-V2 (BM11S12GGA-V2)	BGM11S12F256GA-V2R (BM11S12GGA-V2R)
BGM11S22F256GA-V2 (BM11S22GGA-V2)	BGM11S22F256GA-V2R (BM11S22GGA-V2R)

Approved by: Kelvin Lee

Prepared on : 11-May-26

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