PXIe-8520 Specifications

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Contents

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These specifications apply to the PXIe-8520 and all interface devices that may be installed within the PXIe-8520.

Revision History

Version	Date changed	Description
379025C-01	July 2026	Added timing and synchronization specifications. Added tap latency specifications and the IEEE 802.1AS protocol.
379025B-01	August 2025	Added the Ethernet PHY chipset model.
379025A-01	March 2025	Initial release.

Looking For Something Else?

For information not found in the specifications for your product, such as operating instructions, browse *Related Information*.

Related information:

- PXIe-8520 User Manual
- Software and Driver Downloads
- Dimensional Drawings
- Product Certifications
- Letter of Volatility
- Discussion Forums
- NI Learning Center

Definitions

Warranted Specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical**—describes the performance met by a majority of models.
- **Nominal**—describes an attribute that is based on design, conformance testing, or supplemental testing.

Values are *Typical* unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- 0 °C to 55 °C

PXIe-8520 Pinout

The I/O of the interface devices installed within the PXIe-8520 interface carrier determine the available I/O.

IVN-8532 Pinout

Use the pinout to connect to the H-MTD Z (f) ports on the IVN-8532 when it is installed within the PXIe-8520.

Each IVN-8532 has two H-MTD Z (f) ports.

Note The PXIe-8520 supports polarity correction at 1 Gb/s link speeds. The PXIe-8520 does not support polarity correction at 100 Mb/s link speeds. Ensure that the cable polarity matches the IVN-8532 polarity in the IVN-8532 pinout.

Figure 1. IVN-8532 H-MTD Z (f) Connector Pinout

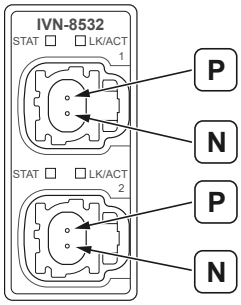

Table 1. IVN-8532 Signal Descriptions

Signal Name	Description
P	Transceiver positive
N	Transceiver negative

Physical Characteristics

Table 2. PXIe-8520 Physical Characteristics

Dimensions	3U, one-slot, PXI Express/Compact PCI Express module 2.0 cm × 13.0 cm × 21.6 cm (0.8 in. × 5.1 in. × 8.5 in.) For more information, visit *ni.com/dimensions* and search by module number.
Weight	452.6 g (1.00 lb)

Table 3. IVN-8532 Physical Characteristics

Dimensions	1.7 cm × 4.7 cm × 9.8 cm (0.7 in. × 1.8 in. × 3.9 in.)
Weight	38.5 g (0.08 lb)

Table 4. Ethernet PHY Chipset Model

Chipset	BCM89885M

Network Interface

Table 5. PXIe-8520 with IVN-8532

Port configuration	2 Taps or 4 endpoints
Tap latency	• 100 Mb/s: 5.8 µs, typical • 1 Gb/s: 6.8 µs, typical
Protocols	• IEEE 802.3 Raw Ethernet • TCP/IP • UDP/IP • IEEE 802.1AE (MACsec) • IEEE 802.1AS

Note For information about using endpoints, refer to the *PXIe-8520 User Manual*.

Bus Interface

Table 6. Bus Interface

Form factor	Gen 3 x8 PXI Express, specification revision 1.0 compliant
Slot compatibility	x1, x4, x8 and x16 PXI Express or PXI Express hybrid slots

Power Requirements

Table 7. PXIe-8520 Power Requirements

Voltage rating	+3.3 V DC, +12 V DC
Current and power ratings	• +3.3 V DC: 3 A • +12 V DC: 4 A Total power: 58 W

Table 8. IVN-8532 Power Requirements (J1)

Voltage rating	+12 V DC, +4.35 V DC, +1.8 V DC
Current and power ratings	• +12 V DC: 50 mA • +4.35 V DC: 250 mA • +1.8 V DC: 150 mA

Timing and Synchronization

Table 9. Network Timekeeping

Timing and synchronization protocol	802.1AS
Network synchronization accuracy	<1 µs

Table 10. Timebases

Local	100 MHz, shared by all ports, disciplined by PXI_Clk10 if available
Network	x4 (1 clock per port), independently disciplined by an external grand master (port is configured as a slave)[1] or the local timebase (port is configured as a master)

Table 11. Trigger I/O source

Trigger I/O source	PXI_Trig <0:7>

Table 12. Input Trigger Capability

Timestamps[2]	x4 timestamps, one per port; each captures both local time and network time[3]

Table 13. Output Trigger Capability

Time triggers	x4 time triggers, one per port; generated from local time or network time

1. If the port is not connected to an 802.1AS network, the network timebase falls back to local time.
2. You can trigger each timestamp by any PXI_Trig <0:7>.
3. If no external network is available, use local time instead.

Note You can export clock outputs and time triggers on any PXI_Trig<0:7>.

Environmental Guidelines

Notice Failure to follow the mounting instructions in the product documentation can cause temperature derating.

Notice This product is intended for use in indoor applications only.

Notice All cabling should be strain-relieved near input connectors. Take care not to directionally bias cable connectors within input connectors when applying strain relief.

Notice Cover all empty slots using filler panels.

Environmental Characteristics

Table 14. Temperature

Operating	0 °C to 55 °C[4]
Storage	-40 °C to 71 °C

Table 15. Humidity

Operating	10% RH to 90 % RH, noncondensing
Storage	5% RH to 95 % RH, noncondensing

Table 16. Pollution Degree

Pollution degree	2

Table 17. Maximum Altitude

Maximum altitude	2,000 m

4. Not all chassis with slot cooling capacity ≥58 W can achieve this ambient temperature range. Refer to PXI chassis specifications to determine the ambient temperature ranges your chassis can achieve.

Table 18. Shock and Vibration

Operating vibration	5 Hz to 500 Hz, 0.3 g RMS
Non-operating vibration	5 Hz to 500 Hz, 2.4 g RMS
Operating shock	30 g, half-sine, 11 ms pulse