

MOSFET – N-Channel, POWERTRENCH®

30 V, 6.9 mΩ

FDMS7680, FDMS7680-NC

General Description

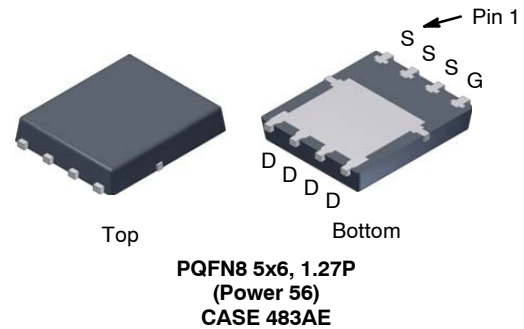
This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

Features

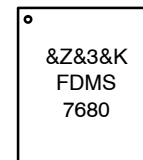
- Max $R_{DS(on)}$ = 6.9 mΩ at V_{GS} = 10 V, I_D = 14 A
- Max $R_{DS(on)}$ = 11 mΩ at V_{GS} = 4.5 V, I_D = 11 A
- Advanced Package and Silicon Combination for Low $R_{DS(on)}$ and High Efficiency
- Next Generation Enhanced Body Diode Technology, Engineered for Soft Recovery
- MSL1 Robust Package Design
- 100% UIL Tested
- This Device is Halide Free and RoHS Compliant with Exemption 7a, Pb-Free 2LI (on second level interconnection)

Applications

- IMVP Vcore Switching for Notebook
- VRM Vcore Switching for Desktop and Server
- OringFET / Load Switch
- DC-DC Conversion

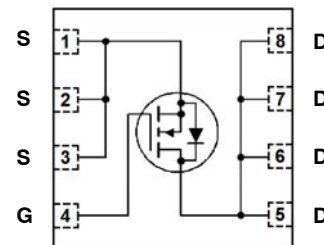


MARKING DIAGRAM



&Z = Assembly Plant Code
&3 = 3-Digit Date Code Format
&K = 2-Digits Lot Run Traceability Code
FDMS7680 = Specific Device Code

PIN ASSIGNMENT



MOSFET MAXIMUM RATINGS (T_C = 25 °C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage (Note 4)	±20	V
I_D	Drain Current: – Continuous (Package Limited) T_C = 25 °C – Continuous (Silicon Limited) T_C = 25 °C – Continuous T_A = 25 °C (Note 1a) – Pulsed (Note 4)	28 53 14 80	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	29	mJ
P_D	Power Dissipation T_C = 25 °C T_A = 25 °C (Note 1a)	33 2.5	W
T_J , T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.7	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^{\circ}\text{C}$		13		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	1.25	1.9	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^{\circ}\text{C}$		-6		mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 14\text{ A}$		5.6	6.9	m Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 11\text{ A}$		8.0	11	
		$V_{GS} = 10\text{ V}$, $I_D = 14\text{ A}$, $T_J = 125\text{ }^{\circ}\text{C}$		7.3	10.1	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}$, $I_D = 14\text{ A}$		86		S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		1390	1850	pF
C_{oss}	Output Capacitance			430	575	pF
C_{rss}	Reverse Transfer Capacitance			60	85	pF
R_g	Gate Resistance		0.1	0.9	2.0	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 14\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		10	20	ns
t_r	Rise Time			4	10	ns
$t_{d(off)}$	Turn-Off Delay Time			21	34	ns
t_f	Fall Time			3	10	ns
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V}$ to 10 V , $V_{DD} = 15\text{ V}$, $I_D = 14\text{ A}$		20	28	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V}$ to 4.5 V , $V_{DD} = 15\text{ V}$, $I_D = 14\text{ A}$		9	13	nC
Q_{gs}	Gate to Source Charge	$V_{DD} = 15\text{ V}$, $I_D = 14\text{ A}$		4.6		nC
Q_{gd}	Gate to Drain "Miller" Charge			2.3		nC

DRAIN-SOURCE DIODE CHARACTERISTICS

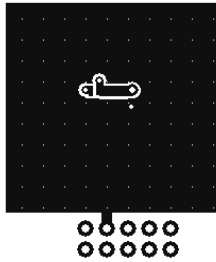
V_{SD}	Source-Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2.1\text{ A}$ (Note 2)		0.74	1.2	V
		$V_{GS} = 0\text{ V}$, $I_S = 14\text{ A}$ (Note 2)		0.83	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 14\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		24	39	ns
Q_{rr}	Reverse Recovery Charge			8	15	nC
t_{rr}	Reverse Recovery Time	$I_F = 14\text{ A}$, $di/dt = 300\text{ A}/\mu\text{s}$		20	36	ns
Q_{rr}	Reverse Recovery Charge			15	27	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

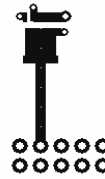
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NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50 °C/W when mounted on
a 1 in² pad of 2 oz copper.



b) 125 °C/W when mounted on
a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%.
3. Starting $T_J = 25$ °C, $L = 0.3$ mH, $I_{AS} = 14$ A, $V_{DD} = 27$ V, $V_{GS} = 10$ V.
4. Pulse I_d refers to Figure.11 Forward Bias Safe Operation Area.



TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

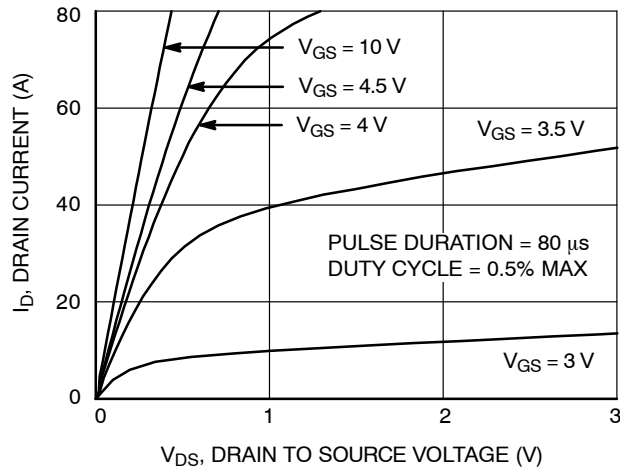


Figure 1. On-Region Characteristics

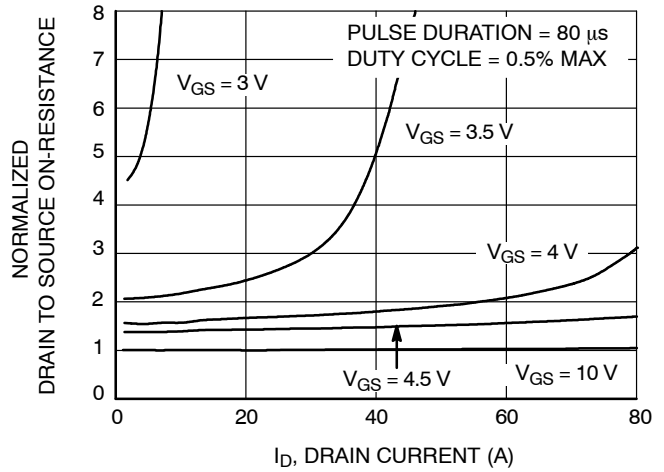


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

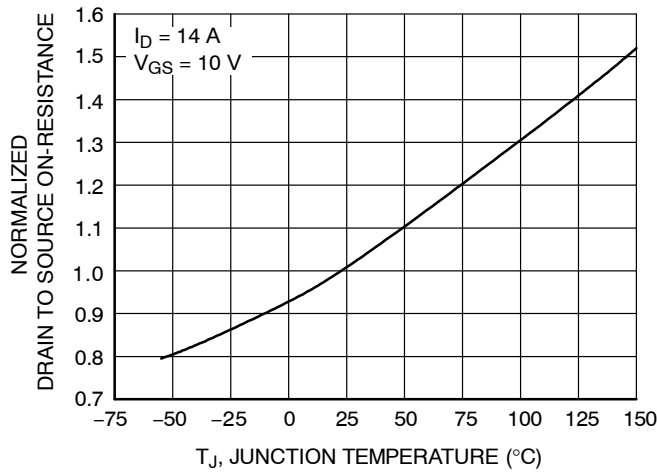


Figure 3. Normalized On-Resistance vs. Junction Temperature

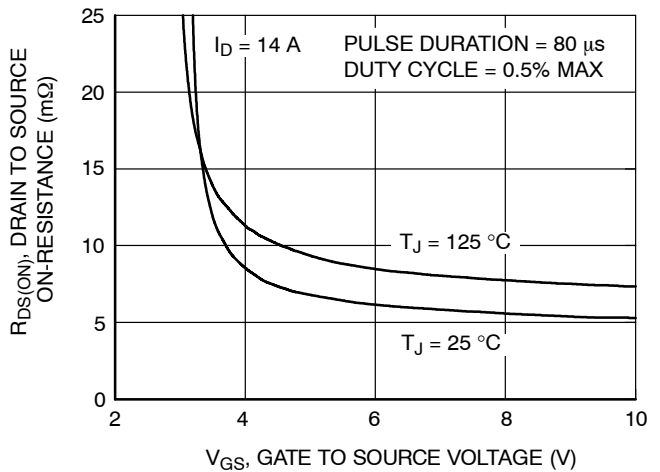


Figure 4. On-Resistance vs. Gate to Source Voltage

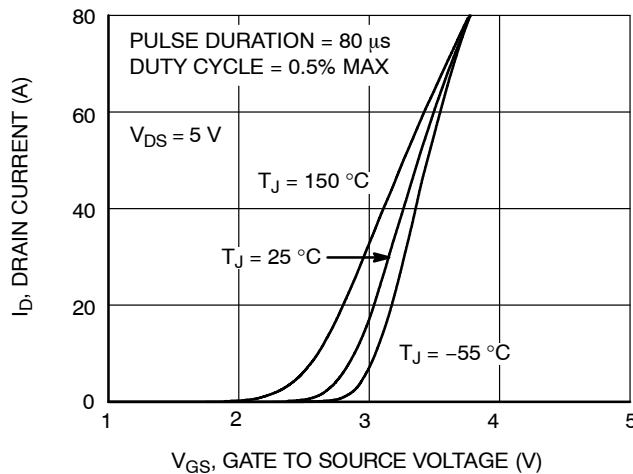


Figure 5. Transfer Characteristics

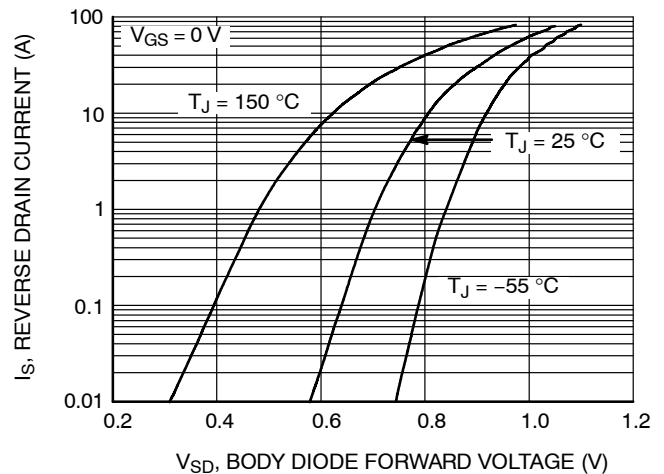


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

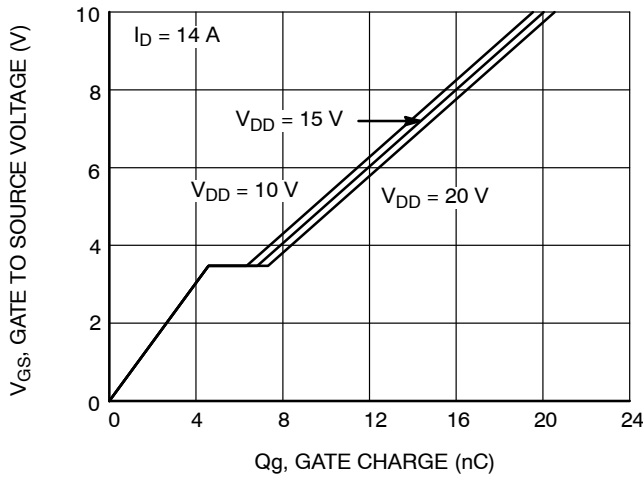


Figure 7. Gate Charge Characteristics

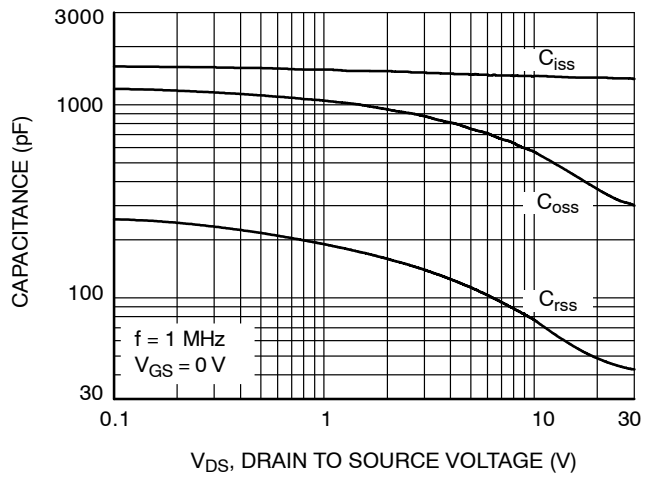


Figure 8. Capacitance vs. Drain to Source Voltage

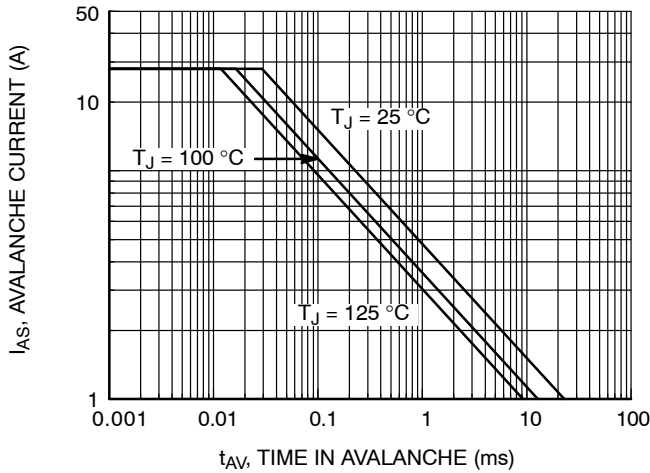


Figure 9. Unclamped Inductive Switching Capability

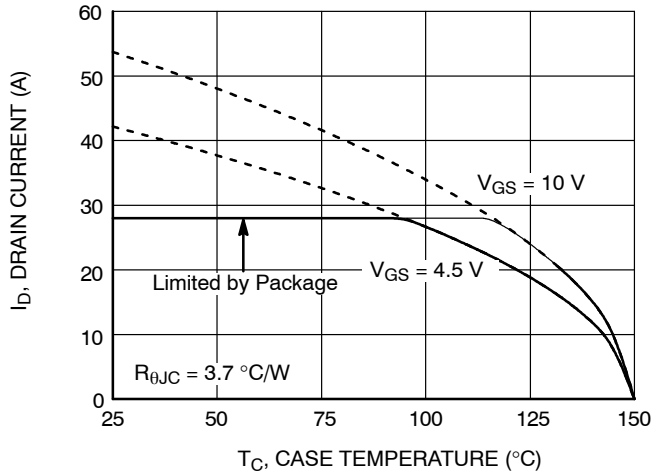


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

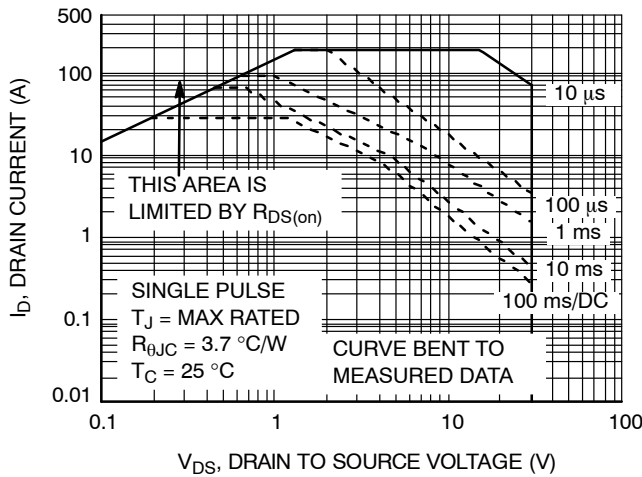


Figure 11. Forward Bias Safe Operating Area

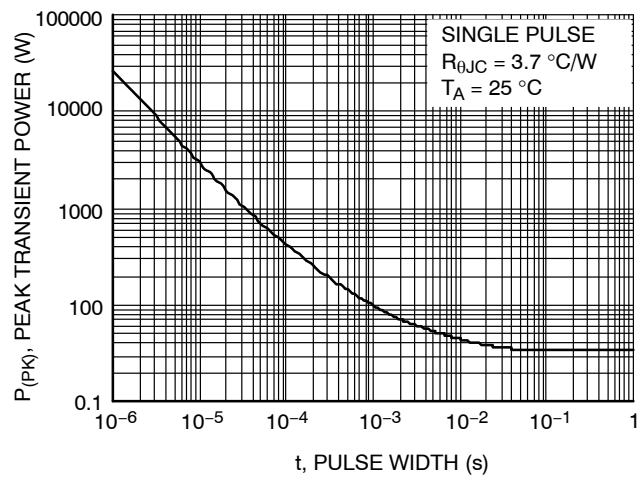


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

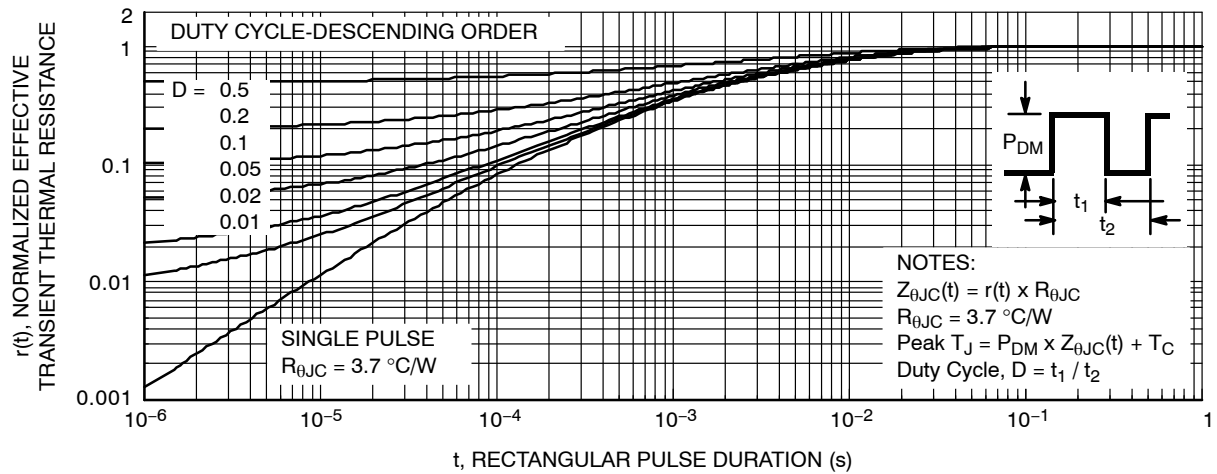


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

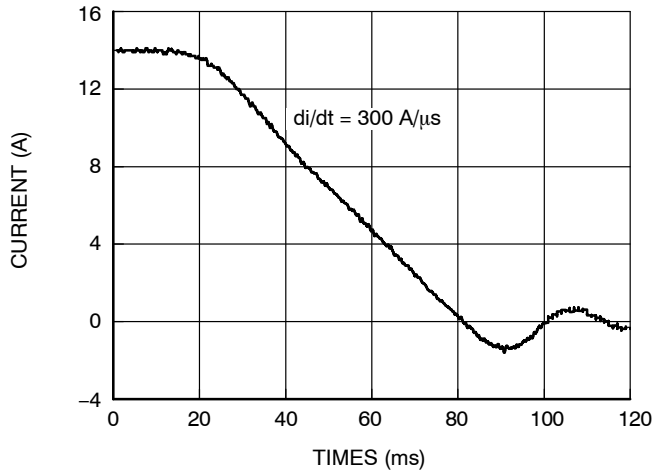


Figure 14. Body Diode Reverse Recovery Characteristics

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping [†]
FDMS7680	FDMS7680	PQFN8 5x6, 1.27P (Power 56)	13"	12 mm	3000 / Tape & Reel
FDMS7680-NC					

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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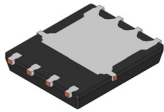
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REVISION HISTORY

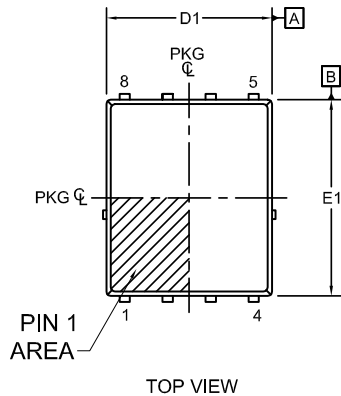
Revision	Description of Changes	Date
3	Document converted to onsemi format. Added FDMS7680-NC device.	8/9/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

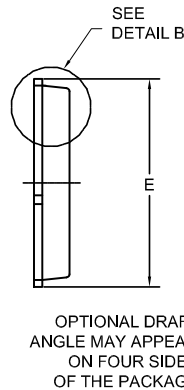



PQFN8 5X6, 1.27P
CASE 483AE
ISSUE C

DATE 21 JAN 2022

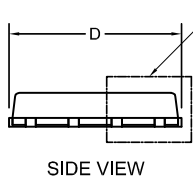


TOP VIEW

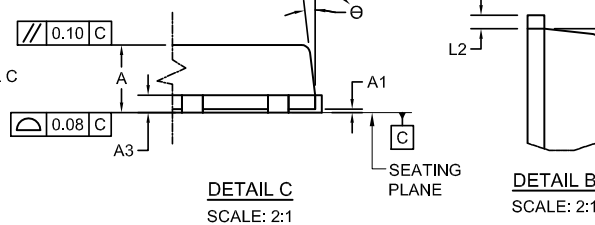
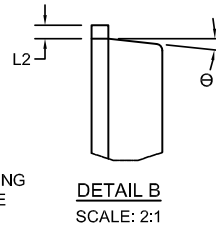
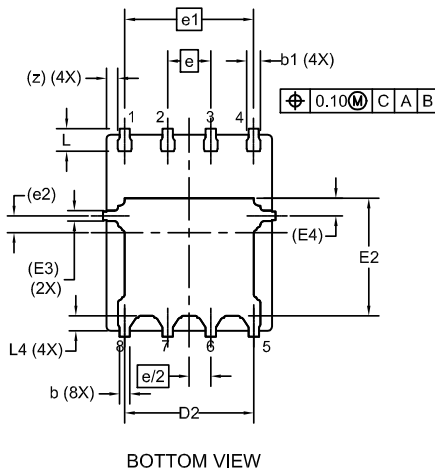

OPTIONAL DRAFT
ANGLE MAY APPEAR
ON FOUR SIDES
OF THE PACKAGE

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



SIDE VIEW


DETAIL C
SCALE: 2:1

DETAIL B
SCALE: 2:1


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