

1200V, 80 mΩ N-Channel mSiC[®] MOSFET
MSC080SMB120Q



Product Overview

1200V, 80 mΩ typical at $V_{GS} = 18V$, 98 mΩ typical at $V_{GS} = 15V$, Silicon Carbide (SiC) N-Channel MOSFET, Quadruple Decawatt Package (QDPAK) 22-lead with a source sense.

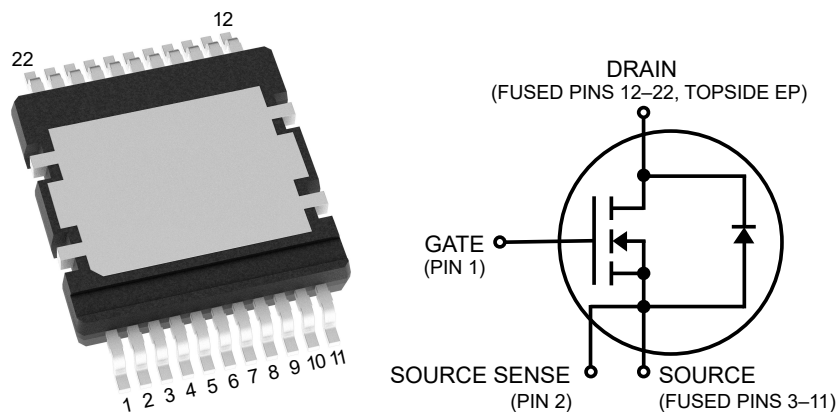


Table 1. Ordering Information

Catalog Part Number (CPN)	Package	Packing Media (Qty.)	Qualification
MSC080SMB120Q	QDPAK 22-lead	Tube (32)	Industrial
MSC080SMB120QT/R		Tape and Reel (800)	
MSC080SMB120QVAO	QDPAK 22-lead	Tube (32)	AEC-Q101
MSC080SMB120QT/RVAO		Tape and Reel (800)	

Features

- Low capacitances and low gate charge
- Fast switching speed due to low internal gate resistance (ESR)
- Stable operation at high junction temperature, $T_{J(max)} = 175\text{ }^{\circ}\text{C}$
- Fast and reliable body diode
- Innovative top-side cooled package
- Superior avalanche ruggedness (100% UIS production tested)
- RoHS compliant

Applications

- Photovoltaic (PV) inverter, converter, and industrial motor drives
- Smart grid transmission and distribution
- Induction heating and welding
- Hybrid Electric Vehicle (HEV) powertrain and Electric Vehicle (EV) charger
- Power supply and distribution

Benefits

- High efficiency to enable lighter and more compact system
- Simple to drive and easy to parallel
- Superior thermal performance and lower switching losses
- Eliminates the need for external freewheeling diode
- Lower system cost of ownership

1. Device Specifications

This section shows the specifications of this device.

1.1. Absolute Maximum Ratings

The following table shows the absolute maximum ratings of this device.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain source voltage	1200	V
I_D	Continuous drain current at $T_C = 25\text{ }^{\circ}\text{C}$	30	A
	Continuous drain current at $T_C = 100\text{ }^{\circ}\text{C}$	21	
I_{DM}	Pulsed drain current ¹	63	
V_{GS}	Gate-source voltage	21/-10	V
	Transient gate-source voltage	23/-12	
	Recommended turn-on gate-source voltage	15 to 18	
	Recommended turn-off gate-source voltage	-5	
P_D	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	168	W
	Linear derating factor	1.1	W/ $^{\circ}\text{C}$

Note:

1. Repetitive rating: Pulse width and case temperature are limited by the maximum junction temperature.

1.2. Thermal and Mechanical Characteristics

The following table shows the thermal and mechanical characteristics of this device.

Table 1-2. Thermal and Mechanical Characteristics

Symbol	Characteristic/Test Conditions	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-case thermal resistance	—	0.69	0.89	$^{\circ}\text{C}/\text{W}$
T_J	Operating junction temperature	-55	—	175	$^{\circ}\text{C}$
T_{STG}	Storage temperature	-55	—	175	
—	Reflow temperature	—	—	260	$^{\circ}\text{C}$
Wt	Package weight	—	2.15	—	g

ESD practices should comply with JESD-625.

1.3. Electrical Performance

The following table shows the static characteristics of this device at $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 1-3. Static Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{V}, I_D = 100\text{ }\mu\text{A}$	1200	—	—	V
$R_{DS(on)}$	Drain-source on resistance ¹	$V_{GS} = 18\text{V}, I_D = 6\text{A}$	—	80	112	m Ω
		$V_{GS} = 15\text{V}, I_D = 6\text{A}$	—	98	—	
		$V_{GS} = 18\text{V}, I_D = 6\text{A}, T_J = 175\text{ }^{\circ}\text{C}$	—	132	—	
$V_{GS(th)}$	Gate-source threshold voltage	$V_{GS} = V_{DS}, I_D = 0.75\text{ mA}$	1.9	3.0	5.0	V
		$V_{DS} = 960\text{V}, I_D = 0.75\text{ mA}$	1.5	—	—	

Table 1-3. Static Characteristics (continued)

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 1200V, V_{GS} = 0V$	—	0.02	3.75	μA
		$V_{DS} = 1200V, V_{GS} = 0V, T_J = 175\text{ }^{\circ}C$	—	0.30	—	
I_{GSS}	Gate-source leakage current	$V_{GS} = 21V/-10V$	—	—	± 100	nA

Note:

1. Pulse test: pulse width < 380 μs , duty cycle < 2%.

The following table shows the dynamic characteristics of the device at $T_J = 25\text{ }^{\circ}C$ unless otherwise specified.

Table 1-4. Dynamic Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0V, V_{DD} = 1000V, V_{AC} = 25\text{ mV},$ $f = 100\text{ kHz}$	—	884	—	pF
C_{rss}	Reverse transfer capacitance		—	3.0	—	
C_{oss}	Output capacitance		—	41	—	
Q_G	Total gate charge	$V_{GS} = 18V/-5V, V_{DD} = 800V, I_D = 6A$	—	34	—	nC
Q_{GS}	Gate-source charge		—	8.0	—	
Q_{GD}	Gate-drain charge		—	6.0	—	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 850V, V_{GS} = 18V/-5V, I_D = 20A, R_G = 8\Omega,$ Freewheeling diode = MSC080SMB120Q ($V_{GS} = -5V$); reference Figure 1-20	—	11	—	ns
t_r	Rise time		—	8	—	
$t_{d(off)}$	Turn-off delay time		—	17	—	
t_f	Fall time		—	8	—	
E_{on}	Turn-on switching energy		—	167	—	μJ
E_{off}	Turn-off switching energy		—	62	—	
ESR	Gate equivalent series resistance	$f = 1\text{ MHz}, 25\text{ mV},$ drain-to-source short	—	2.7	—	Ω
SCWT	Short circuit withstand time	$V_{DS} = 960V, V_{GS} = 18V/0V, R_G = 20\Omega$	—	2	—	μs
E_{AS}	Avalanche energy, single pulse	$I_D = 1.9A, 100\%$ UIS production tested	280	—	—	mJ
$E_{AS\text{ CHAR}}$		$I_D = 8.0A,$ last typical pass	—	800	—	

The following table shows the body diode characteristics of the device at $T_J = 25\text{ }^{\circ}C$ unless otherwise specified.

Table 1-5. Body Diode Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
V_{SD}	Diode forward voltage	$I_{SD} = 6A, V_{GS} = 0V$	—	3.5	—	V
		$I_{SD} = 6A, V_{GS} = -5V$	—	3.9	5.0	
t_{rr}	Reverse recovery time	$I_{SD} = 20A, V_{GS} = -5V,$ Drive $R_G = 8\Omega, V_{DD} = 850V,$ $di/dt = -9000\text{ A}/\mu s$	—	22	—	ns
Q_{rr}	Reverse recovery charge		—	70	—	nC
I_{RRM}	Reverse recovery current		—	23	—	A

1.4. Typical Performance Curves

Figure 1-1. Drain Current vs. V_{DS} at T_J

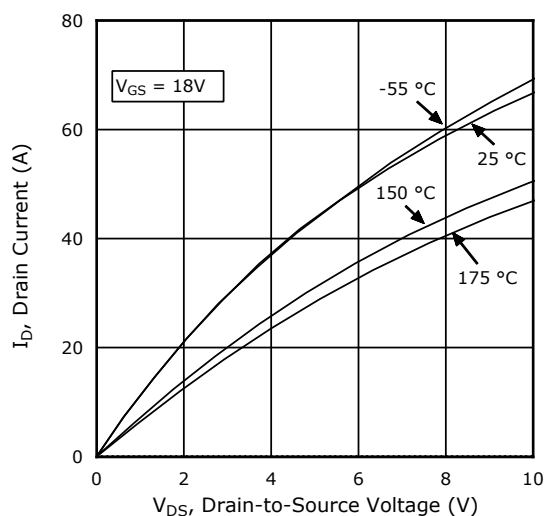


Figure 1-2. Drain Current vs. V_{DS} at V_{GS}

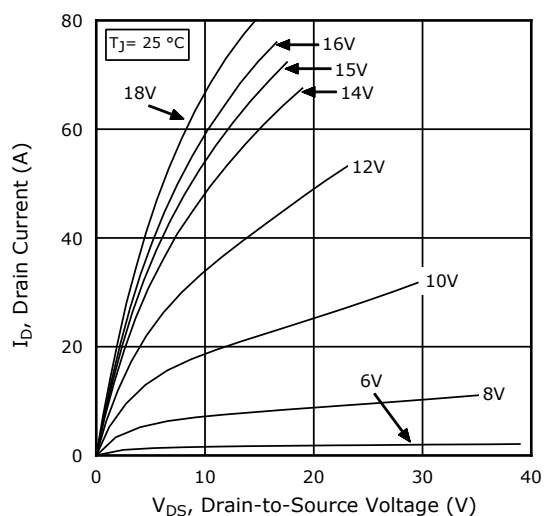


Figure 1-3. Drain Current vs. V_{DS} at V_{GS}

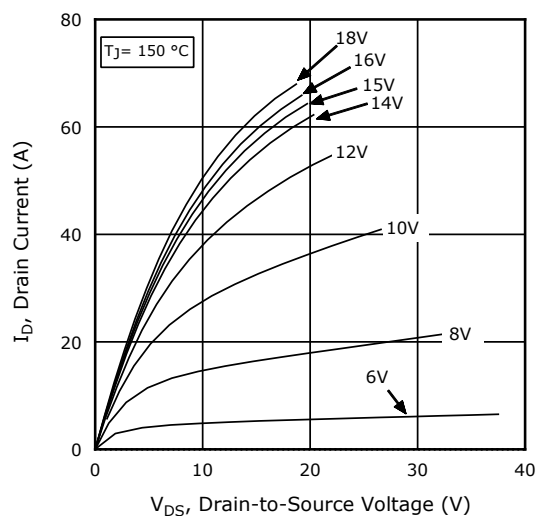


Figure 1-4. Drain Current vs. V_{DS} at V_{GS}

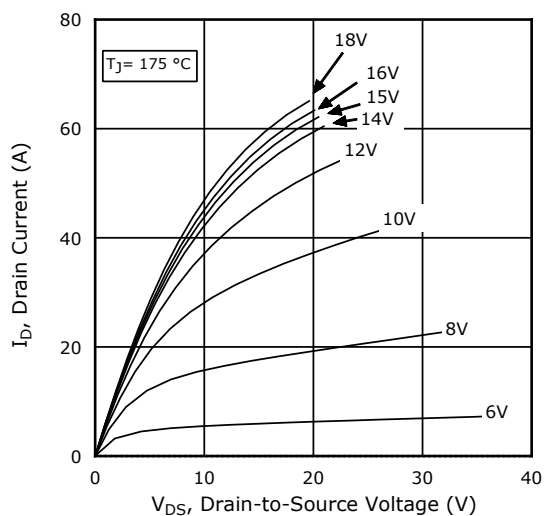


Figure 1-5. I_D vs. V_{DS} 3rd Quadrant Conduction

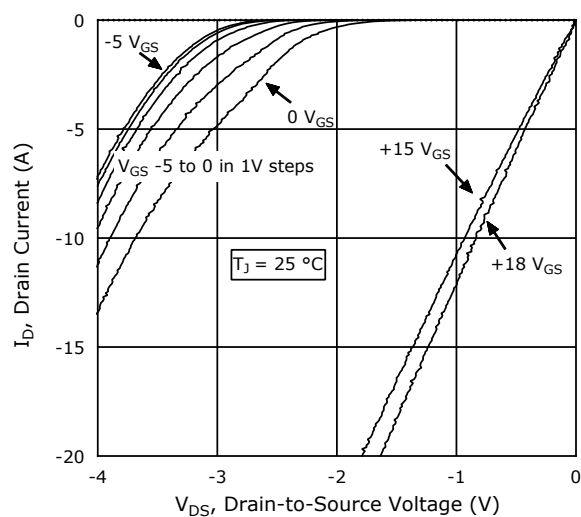


Figure 1-6. I_D vs. V_{DS} 3rd Quadrant Conduction

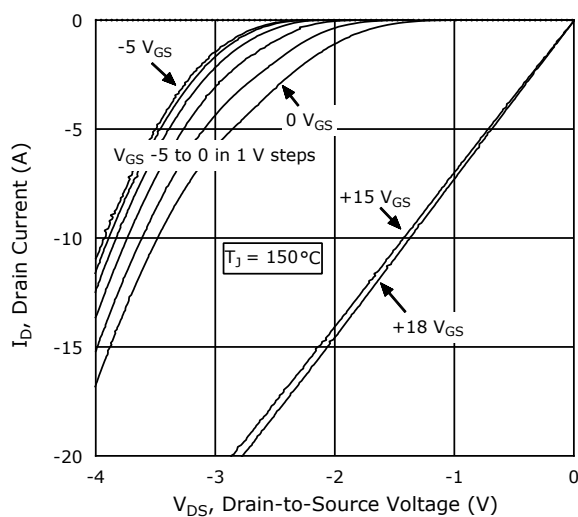


Figure 1-7. $R_{DS(on)}$ vs. Junction Temperature

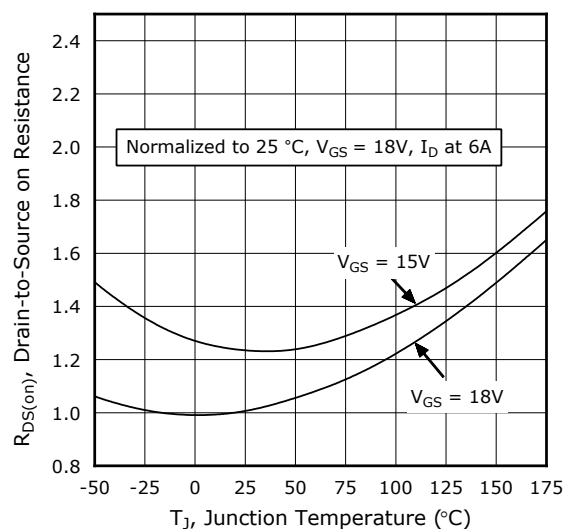


Figure 1-8. Threshold Voltage vs. Junction Temperature

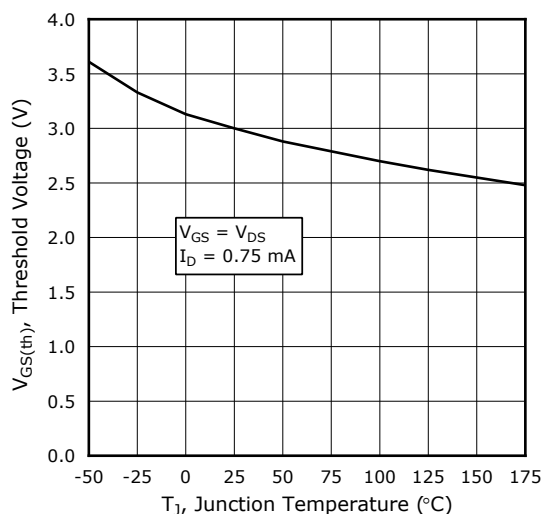


Figure 1-9. Threshold Voltage vs. V_{DS} at T_J

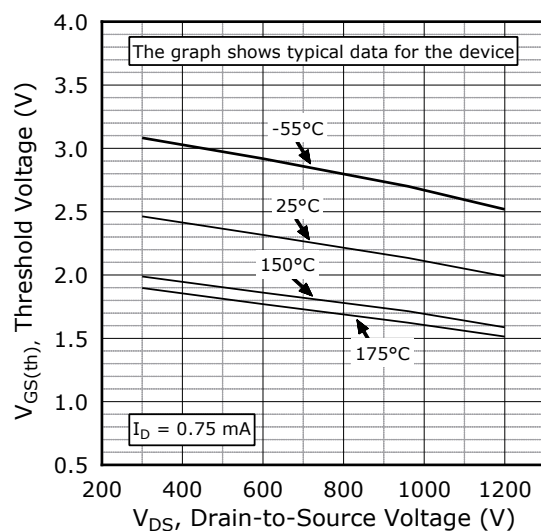


Figure 1-10. Gate Charge Characteristics

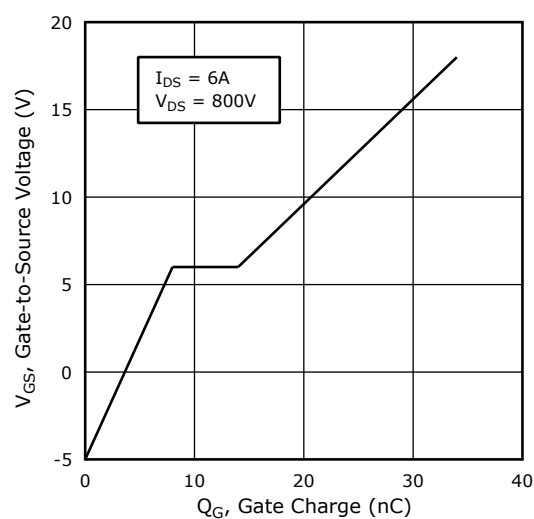


Figure 1-11. Capacitance vs. Drain-to-Source Voltage

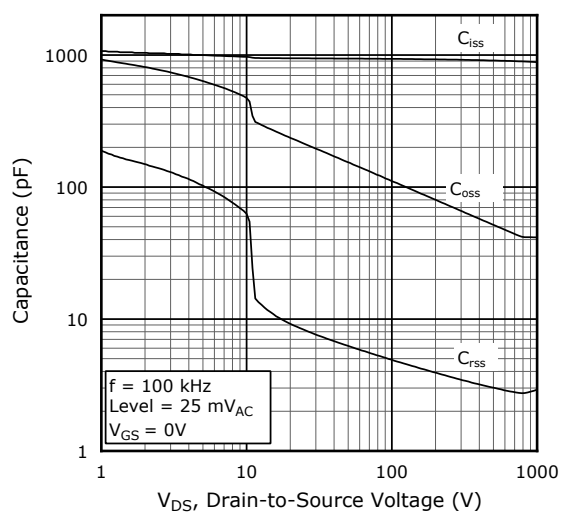


Figure 1-12. Q_{OSS} vs. Drain-to-Source Voltage

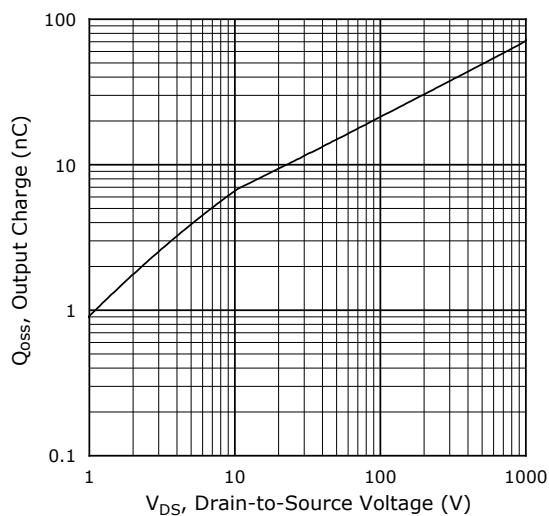


Figure 1-13. E_{oss} vs. Drain-to-Source Voltage

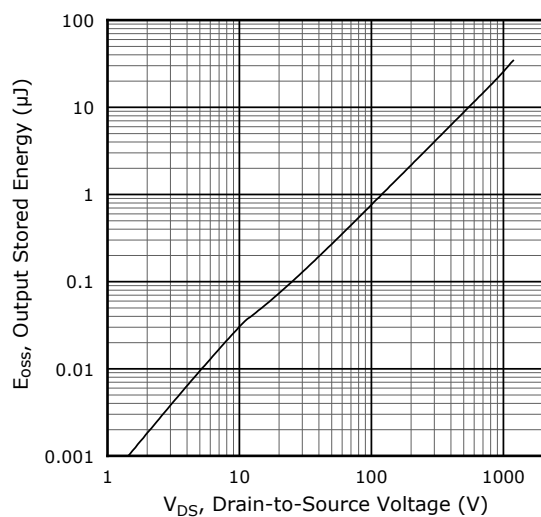


Figure 1-14. Switching Energy vs. V_{DS} & I_D

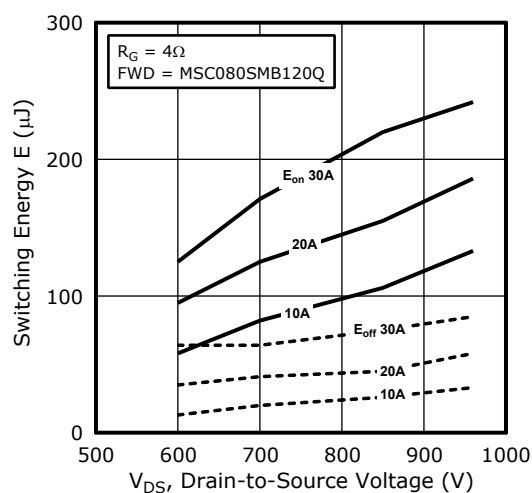


Figure 1-15. Switching Energy vs. V_{DS} & I_D

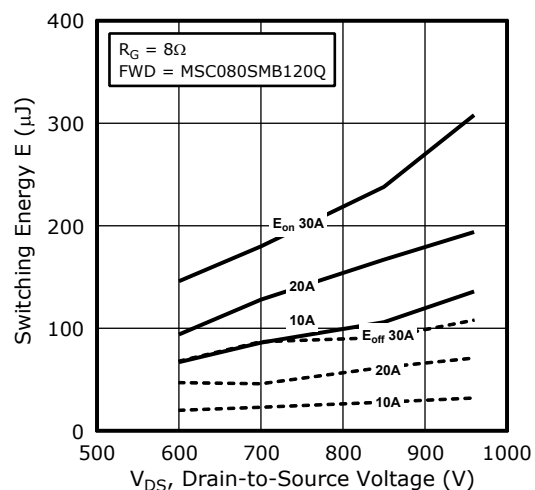


Figure 1-16. Switching Energy vs. V_{DS} & I_D

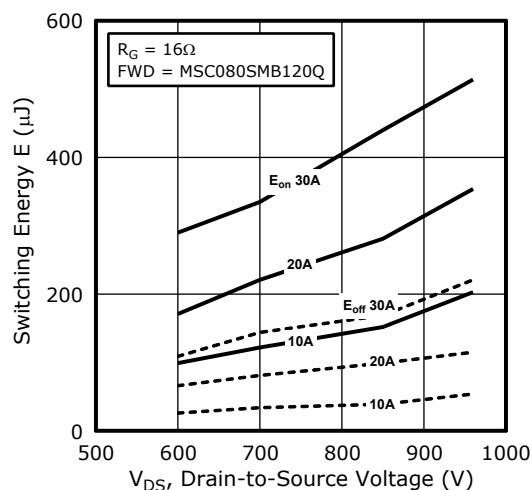


Figure 1-17. Switching Energy vs. Junction Temperature

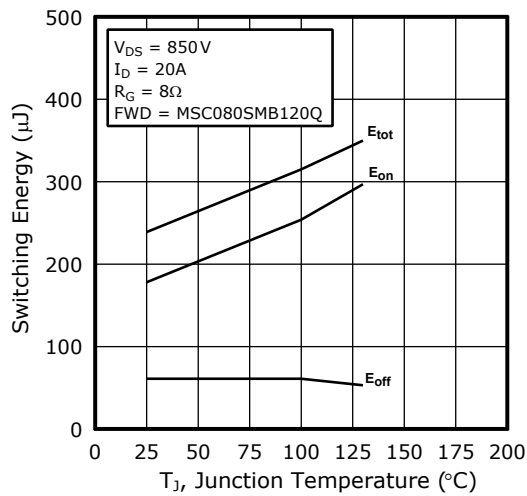


Figure 1-18. Forward Safe Operating Area

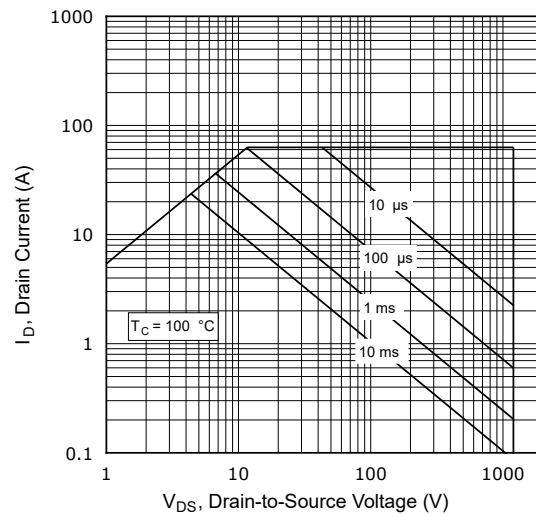
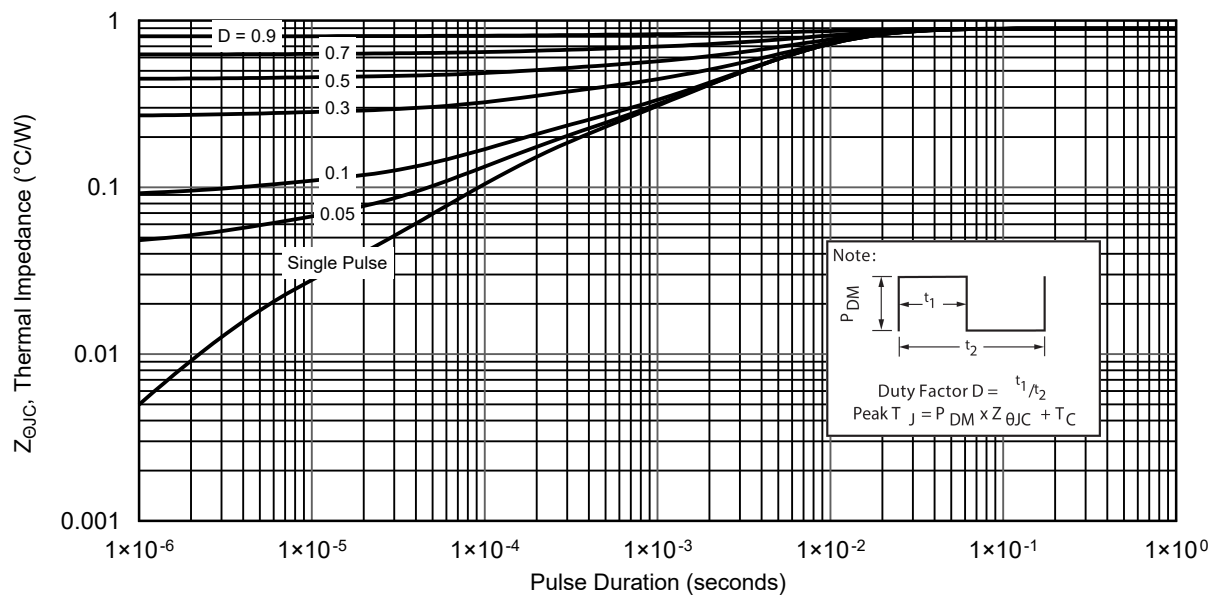
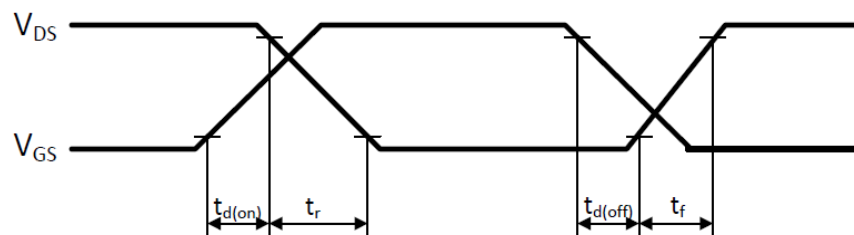


Figure 1-19. Maximum Transient Thermal Impedance



The following figure shows the switching waveform diagram of this device.

Figure 1-20. Switching Waveform



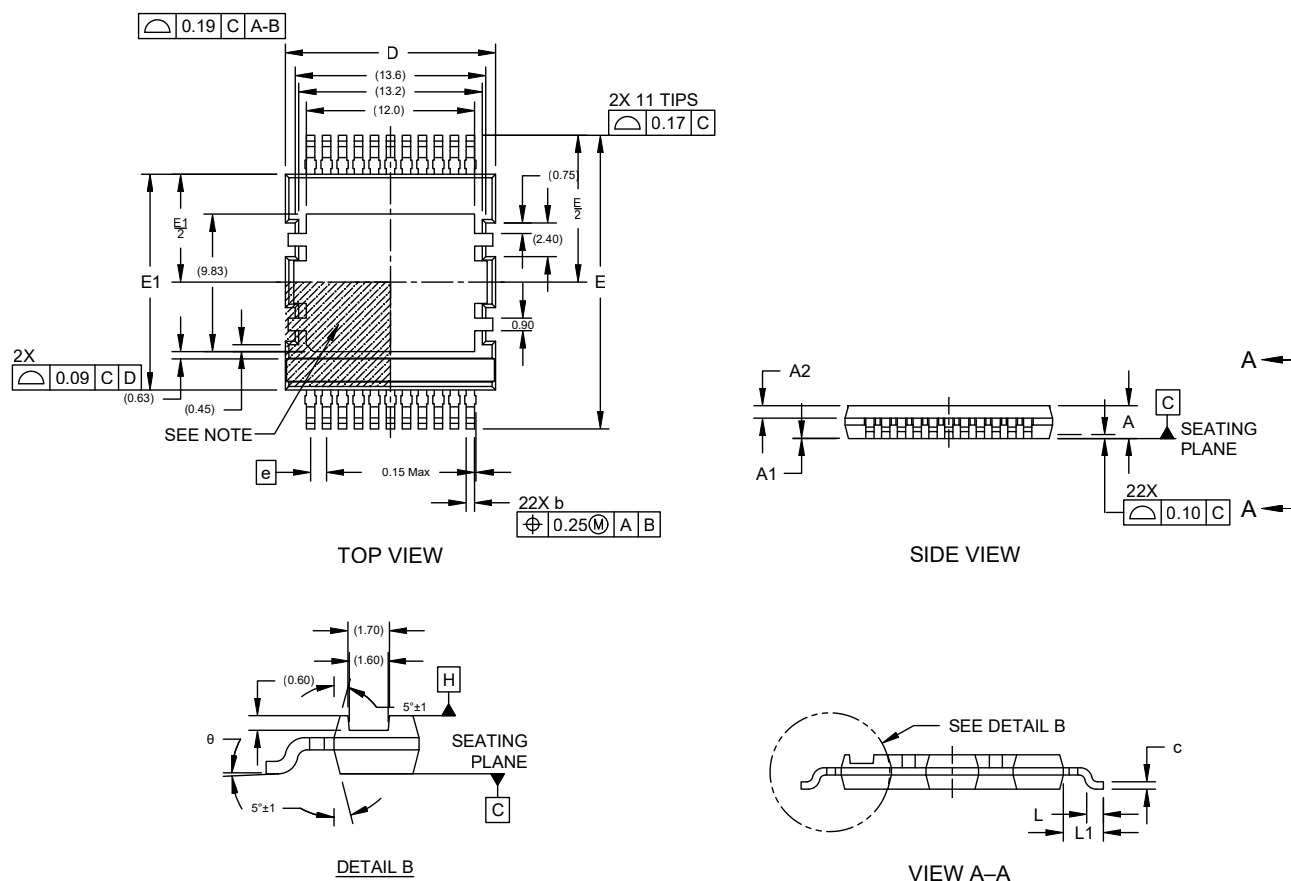
2. Package Specification

This section shows the package specification of this device.

2.1. Package Outline Drawing

The following figure illustrates the QDPAK-22L package outline of this device.

Figure 2-1. Package Outline Drawing



The following table shows the QDPAK-22L dimensions and should be used in conjunction with the package outline drawing.

Table 2-1. QDPAK-22L Dimensions

Symbol	Description	Min. (mm)	Nom. (mm)	Max. (mm)
N	Number of terminals	22		
e	Pitch	1.14 BSC		
A	Overall height	2.20	2.30	2.35
A1	Standoff	0.00	—	0.15
A2	Molded package edge to terminal	—	0.90	—
D	Overall length	14.90	15.00	15.10
E	Overall width	20.81	20.96	21.11
E1	Molded package width	15.30	15.40	15.50
b	Terminal width	0.59	0.60	0.61

Table 2-1. QDPAK-22L Dimensions (continued)

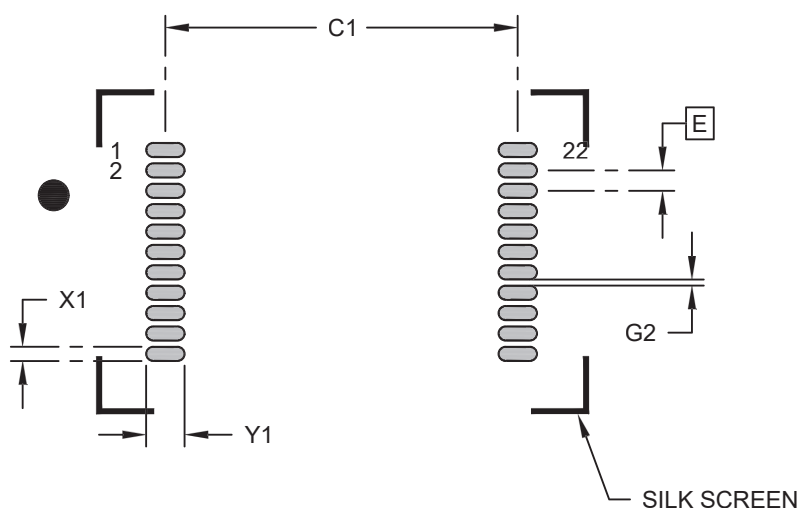
Symbol	Description	Min. (mm)	Nom. (mm)	Max. (mm)
c	Terminal thickness	0.50 REF		
L	Terminal length	—	1.30	—
L1	Footprint	2.78 REF		
θ	Foot angle	0°	—	8°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic dimension. Theoretically exact value shown without tolerances.
 - REF: Reference dimension, usually without tolerance, for information purposes only.

2.2. Recommended Land Pattern

The following figure illustrates the recommended land pattern of this device.

Figure 2-2. Recommended Land Pattern


The following table shows the recommended land pattern dimensions.

Table 2-2. Recommended Land Pattern Dimensions

Symbol	Description	Min. (mm)	Nom. (mm)	Max. (mm)
E	Contact pitch	1.14 BSC		
C1	Contact pad spacing	—	19.70	—
X1	Contact pad width (X22)	—	—	0.80
Y1	Contact pad length (X22)	—	13.40	2.15
G	Contact pad to contact pad (X20)	0.34	—	—

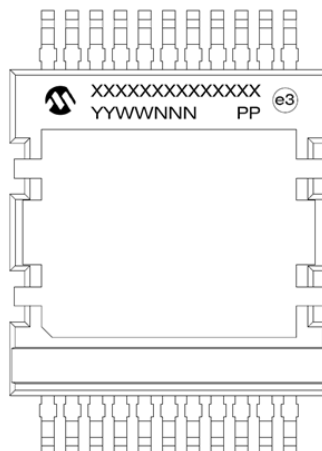
Notes:

- Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic dimension. Theoretically exact value shown without tolerances.
- For best soldering results, see current industry standard IPC-7093.
- The QDPAK package has positive standoff. Please see the *Quadruple Decawatt Package (QDPAK) Application Note* for more information.

2.3. Product Marking Information

The following figure shows the product marking information of this device.

Figure 2-3. Product Marking Information



Marking	Marking Identifier	Description
XXXXXXXXXX	Catalog Part Number (CPN)	This is the unique catalog number for the finished device. Note: For automotive-grade device, the VAO identifier is not shown.
YYWWNNN	Traceability code	A unique identifier assigned by Microchip to track and verify the manufacturing history of the device.
YYWW	Date code	A four-digit number which reflects the year and work week of manufacturing. It is the first four digits of the traceability code.
PP	Country of origin	Two-character code per ISO 3166-1-Alpha-2, indicating the manufacturing country.
e3	ROHS category (Lead finish code)	This code specifies the type of finish applied to the device's leads. Note: e3 indicates a 100% Matte Tin (Sn) finish.

3. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 3-1. Revision History

Revision	Date	Description
B	06/2026	The following changes are made in this revision of the document: • Updated data sheet type from advance information to final data sheet. • Updated the Features and Benefits sections in Product Overview. • Updated I_D and P_D values in Absolute Maximum Ratings. • Updated $R_{\theta JC}$ values in Thermal and Mechanical Characteristics. • Added Figure 1-9 in Typical Performance Curves. • Updated Figure 1-18 and Figure 1-19 in Typical Performance Curves.
A	12/2024	Initial revision (advance information)

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