KIT_PSC3M6_CC2 PSOC™ Control C3M6 Motor Drive Control Evaluation Kit guide

About this document

Scope and Purpose

Thank you for your interest in the KIT_PSC3M6_CC2 PSOC™ Control C3M6 Motor Drive Control Evaluation Kit. This document lists the kit contents, installation requirements, kit documentation, limitations, and known issues.

Intended audience

This document is intended for KIT_PSC3M6_CC2 PSOC™ Control C3M6 Motor Drive Control Evaluation Kit users. This board is intended to be used under laboratory conditions.

Reference board/kit

Product(s) embedded on a PCB with a focus on specific applications and defined use cases that may include software. PCB and auxiliary circuits are optimized for the requirements of the target application.

***Note**: Boards do not necessarily meet safety, EMI, quality standards (for example UL, CE) requirements.*

Safety precautions

Table 1 Safety precautions

	**Caution:** The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury
	**Caution:** Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.
	**Caution:** The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.
	**Caution:** A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.
	**Caution:** The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.

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1 Introduction

1.1 Kit contents

The KIT_PSC3M6_CC2 PSOC™ Control C3M6 Motor Drive Control Evaluation Kit box includes the following components:

- KIT_PSC3M6_CC2 motor control card
- USB Type-A to USB Type-C cable
- Quick start guide

1.2 Getting started

This guide is designed to familiarize you with the evaluation kit.

- The Kit operation section describes the major features and functionalities, such as programming, debugging, and USB-UART bridges of the PSOC™ Control C3M5 motor control card
- The Hardware section provides a detailed hardware description
- Application development using the PSOC™ Control C3M6 motor control card is supported in ModusToolbox™. ModusToolbox™ is a free development ecosystem that includes the Eclipse IDE for ModusToolbox™ and the PSOC™ Control C3M6 SDK along with PSOC™ Control C3M6 MCU. Using ModusToolbox™, you can enable and configure device resources, middleware libraries, write C/assembly source codes, and program or debug the device. For more information, see the ModusToolbox™ software installation guide
- Code examples are available for evaluating the PSOC™ Control C3M6 motor control card. These examples help you familiarize yourself with the PSOC™ Control C3M6 MCU and create your own designs. These examples can be accessed through the ModusToolbox™ Project Creator tool. Additionally, see Infineon code examples for ModusToolbox™ software to access these examples

1.3 Key features

The KIT_PSC3M6_CC2 PSOC™ Control C3M6 Motor Drive Control Evaluation Kit is equipped with the following features:

- Infineon PSOC™ Control C3M6 (Arm® Cortex® -M33 based) microcontroller **PSC3M6GES3AHQ1**, 180 MHz, up to 512 KB flash/128 KB SRAM, E-LQFP-100
- Multiple package footprints option for maximum evaluation flexibility
- Connection to MADK power boards:
  - HD100 MDAK board: on-board 100-pin HD connector
  - M1/M3/M5 MADK board: on-board M1/M3 and M5 connectors
- Unified encoder connectors:
  - 4 encoder connectors: ENC1, ENC2, ENC3, ENC4
  - Multi-motor sensor interface with support for Hall sensors and encoders
- Analog interface
  - On-board analog input buffers with optional filtering (Sallen-Key)
  - Selectable analog input range between 3.3 V and 5 V
  - On-board 2 buffered DAC outputs
  - External VAREF option
- User interface:
  - 2 Power LED: 5 V and 3V3

  - 2 Debug LEDs: DBG and COM, debugger-controlled LEDs
  - 2 User LEDs: LED1 and LED2, user-controlled LED
  - 2 User switches: SW1 and SW2
  - 2 User Potentiometers: POT1 and POT2
  - User USB (USB FS) interface
  - Reset switch
  - GPIO expansion headers
- Debugger and connectivity:
  - Isolated onboard debugger (SEGGER J-Link Lite) via USB-C connector
  - UART channel of on-board debugger (SEGGER J-Link Lite) via USB-C connector
  - Isolated CAN interface on a 3-pin CAN terminal block connector including termination jumper (TERM)
  - Non-isolated external debug option: SWD/JTAG 10-pin 1.27 mm header (PROG)
- Power supply options:
  - Debug USB-C connector (USB): 5 V isolated DC/DC converter
  - User USB-C connector (USB FS): 5 V provided by USB port
  - 2-pin terminal block connector (PWR): nominal voltage input 7 V to 24 V
  - 100-pin HD connector: 5 V or 24 V provided by MADK power board
  - M1/M3 connector: 3.3 V or 24 V provided by MADK power board
  - M5 connector: 5 V provided by MADK power board
  - 5 V (max. 2 A) is provided by on-board DC/DC converter or external source, for example MADK power board
  - 3.3 V (max. 800 mA) is provided by on-board LDO regulator

2 Kit operation

The KIT_PSC3M6_CC2 PSOC™ Control C3M6 Motor Drive Control Evaluation Kit is an evaluation board designed to assist engineers in developing PSOC™ Control C3-based motor control solutions in combination with suitable power stage evaluation boards featuring the MADK connectors (HD100/M1/M3/M5). The board features an isolated onboard debugger for programming and debugging over a USB interface. Additionally, it features USB VCOM functionality using the same USB connection as the debugger.

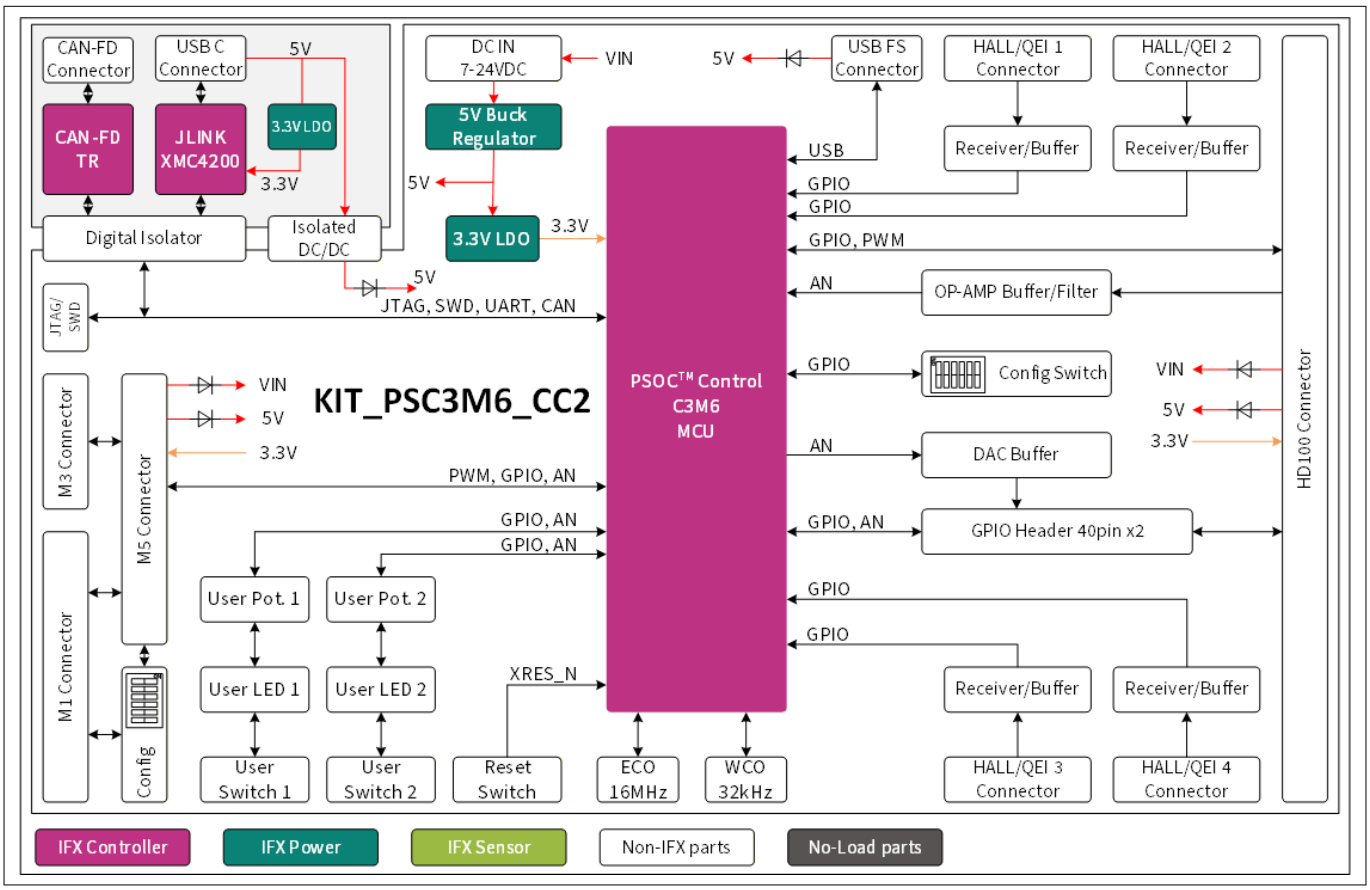


Figure 1 KIT_PSC3M6_CC2 motor control card block diagram

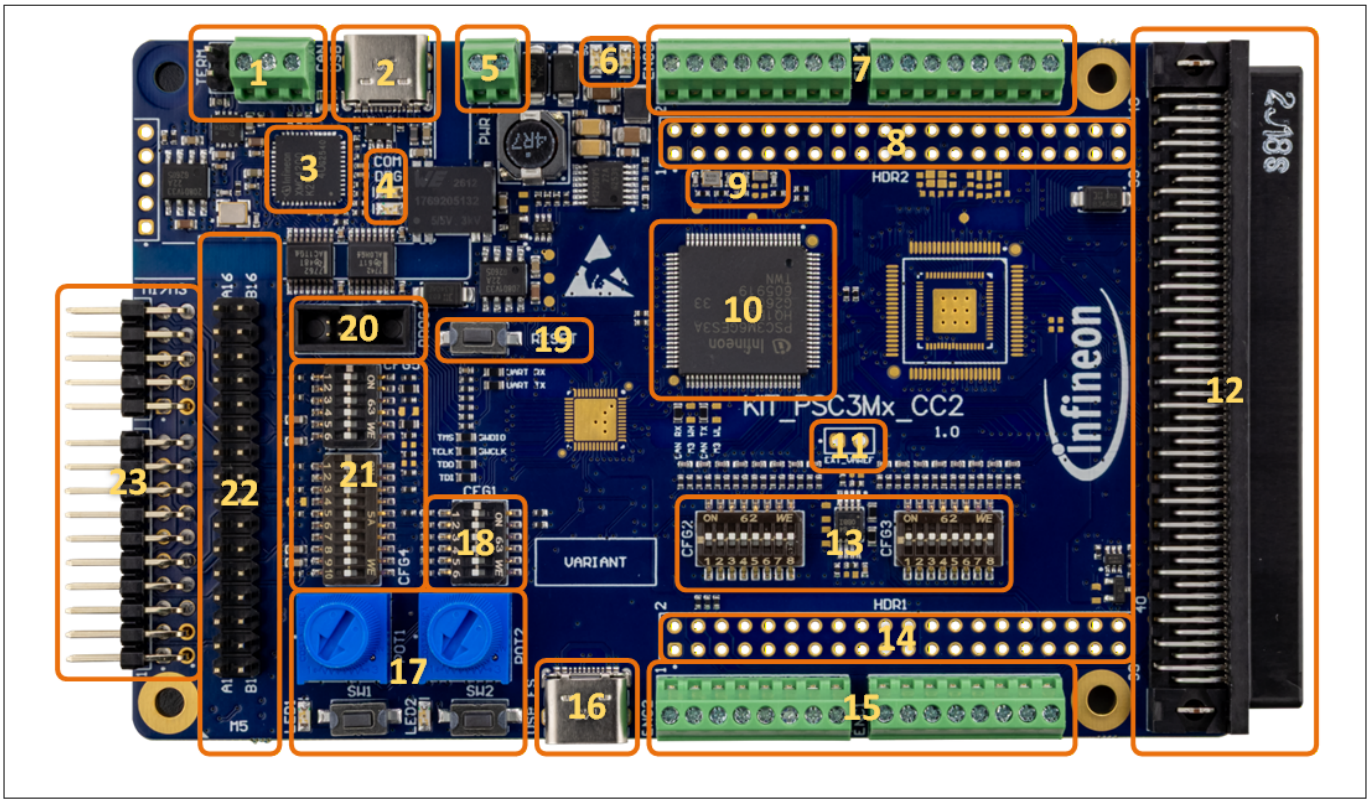


Figure 2 KIT_PSC3M6_CC2 motor control card details

1. Isolated CAN terminal block connector with termination jumper
2. Isolated onboard debugger USB-C socket
3. XMC4200 MCU (SEGGER J-Link Lite)
4. DBG and COM LEDs
5. External power input terminal block connector
6. Power status LEDs: 5V and 3V3
7. Encoder 3 & 4 terminal block connectors
8. Expansion header HDR2
9. ECO and WCO clock sources
10. Infineon PSOC™ Control C3M6 MCU **PSC3M6GES3AHQ1**
11. External VAREF header
12. 100-pin HD connector
13. Analog input attenuation switches CFG2 and CFG3
14. Expansion header HDR1
15. Encoder 1 & 2 terminal block connectors
16. USB-FS USB-C socket
17. User LEDs, switches and potentiometers
18. Bootloader and Encoder enable configuration switch CFG1
19. Reset switch
20. 10-pin Arm® Cortex® programming/debugging connector header PROG
21. M1/M3 & M5 configuration switches CFG4 and CFG5
22. M5 MADK power board connector
23. M1/M3 MADK power board connector

2.1 Using OOB example

The KIT_PSC3M6_CC2 PSOC™ Control C3M6 Motor Drive Control Evaluation Kit is, by default, programmed with the **Hello World** code example. For a detailed description of the project, see the example's `README.md` file in the GitHub repository. The `README.md` file is also available in the application directory once the application is created.

***Note**: At any point in time, if you overwrite the default application, you can restore it by programming the Hello World code example.*

1. Connect the kit to the PC using the provided USB cable
2. Verify that the debug LED on the board is glowing
3. Open a terminal program such as Tera Term or Minicom and select the J-Link VCOM port. Set the serial port parameters to 8N1 and 115200 baud
4. Press the **RESET** button on the board and confirm that the serial terminal application displays the bootup message as shown in
5. Confirm that the user **LED1** is blinking
6. Follow the instructions shown in the bootup message

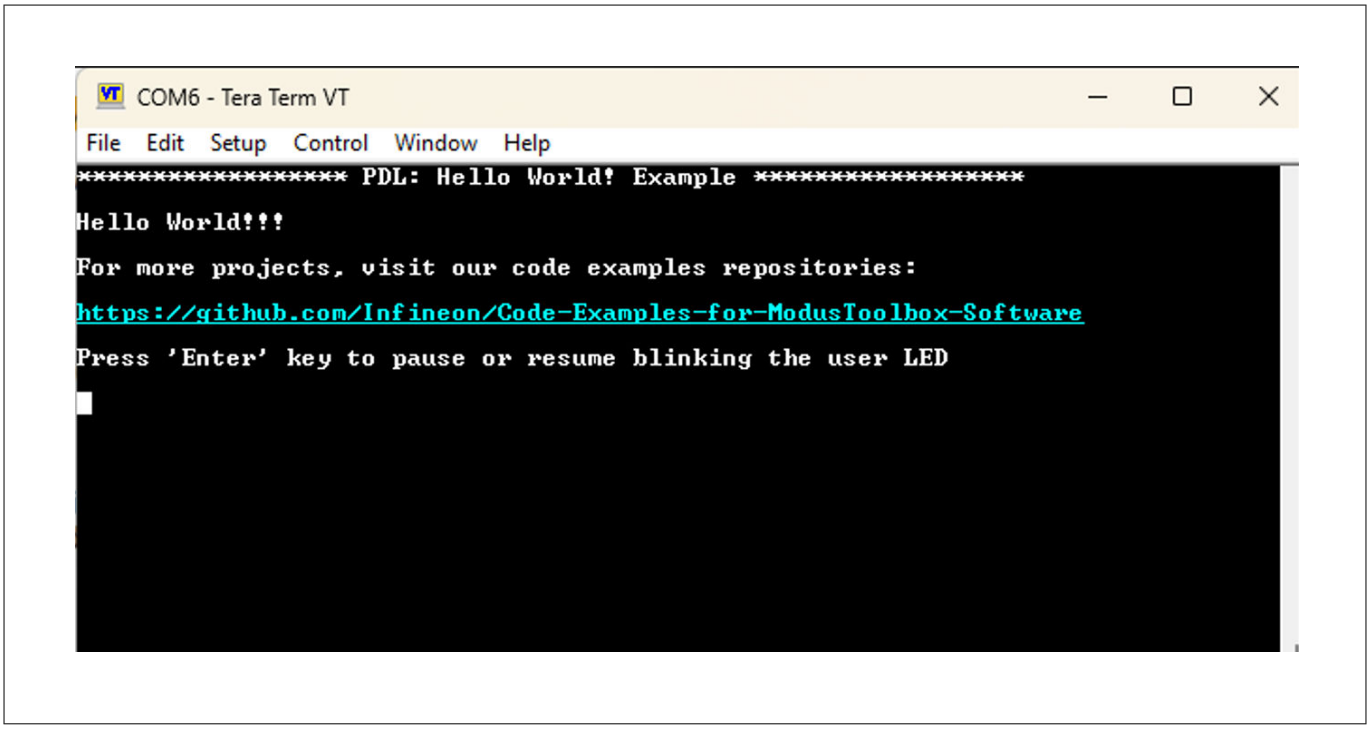


Figure 3 Serial terminal boot message

2.2 Creating a project and programming/debugging using ModusToolbox™

The KIT_PSC3M6_CC2 PSOC™ Control C3M6 Motor Drive Control Evaluation Kit can be programmed and debugged using the onboard J-Link debugger. This onboard programmer/debugger supports a USB-UART bridge. An XMC4200 device is used to implement the J-Link functionality. See the J-Link user guide for more details.

The following steps briefly introduce project creation, programming, and debugging using ModusToolbox™. For detailed instructions, see **Help** > **ModusToolbox™ general documentation** > **ModusToolbox™ user guide.**

1. Connect the board to the PC using the provided USB cable through the J-Link USB connector (**USB**), as shown in Figure 4. It enumerates as a USB composite device if you are connecting it to your PC for the first time

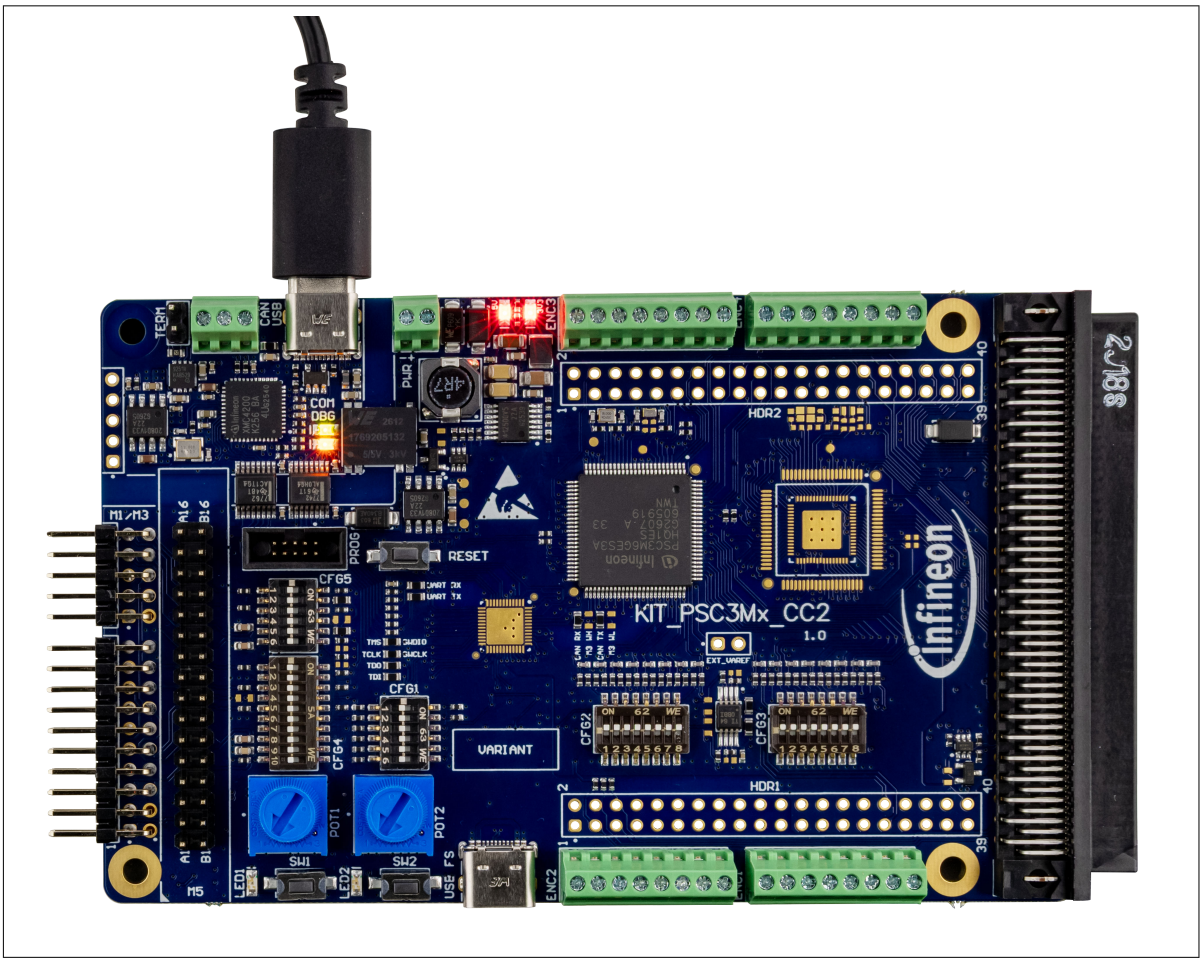


Figure 4 Connect USB cable to the USB connector on board

2. The debugger on this kit features the J-Link Lite with UART and the **DBG** orange LED is always ON if the USB is connected

   ***Note**: The programming can be done either with the onboard J-Link debugger (isolated) or by attaching an external debugger to the **PROG** connector (non-isolated) on the board. It is recommended to use the onboard J-Link debugger*

3. In the Eclipse IDE for ModusToolbox™, import the desired code example (application) into a new workspace

   a. Click on **New Application** from the Quick Panel tab

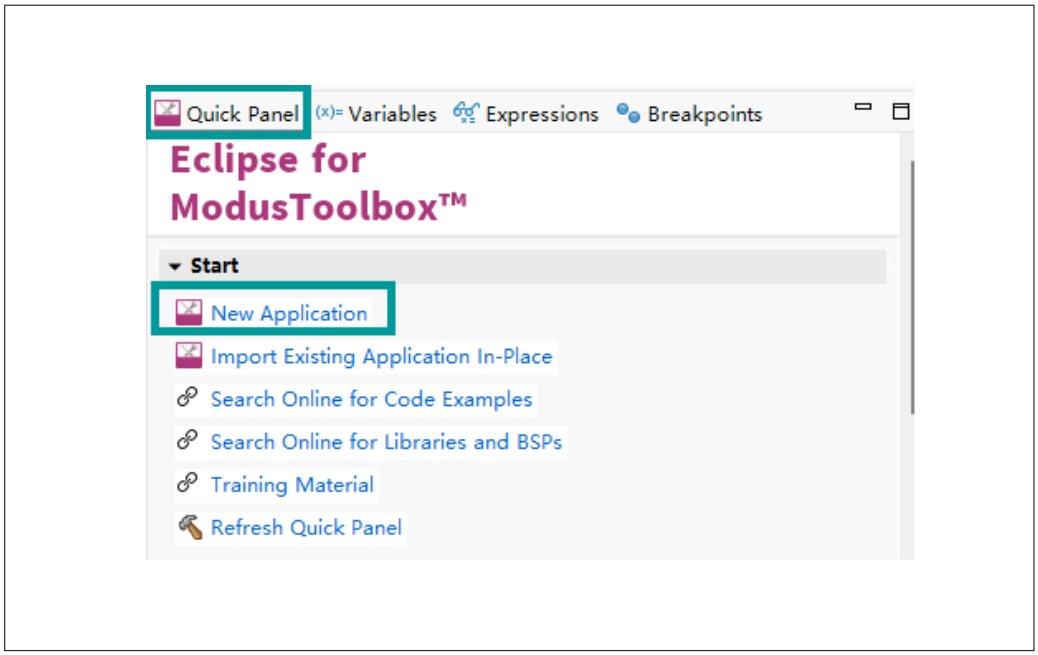


Figure 5 Create new application

b. In the Choose Board support package (BSP) window, expand the PSOC™ Control BSPs, select the **KIT_PSC3M6_CC2** BSP, and click **Next**

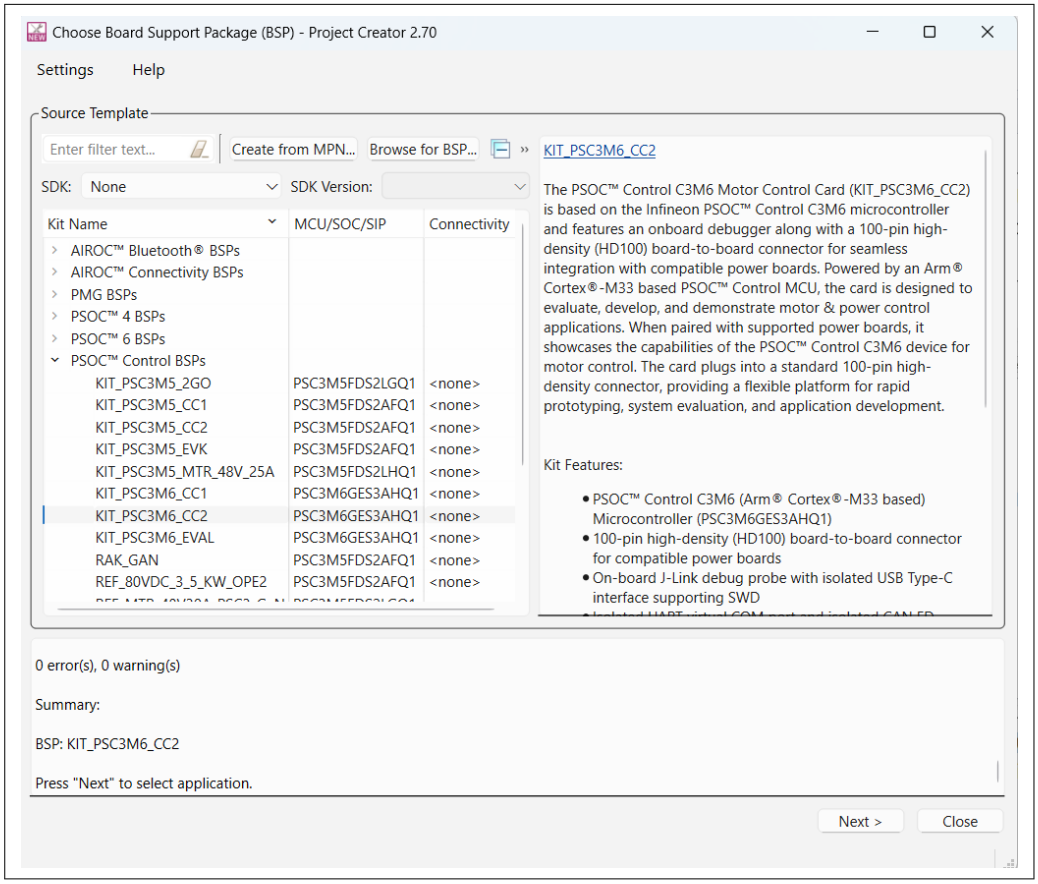


Figure 6 Choose board support package

c. In the Select Application window, expand the Getting Started section, select the **Hello World** application, and click **Create**

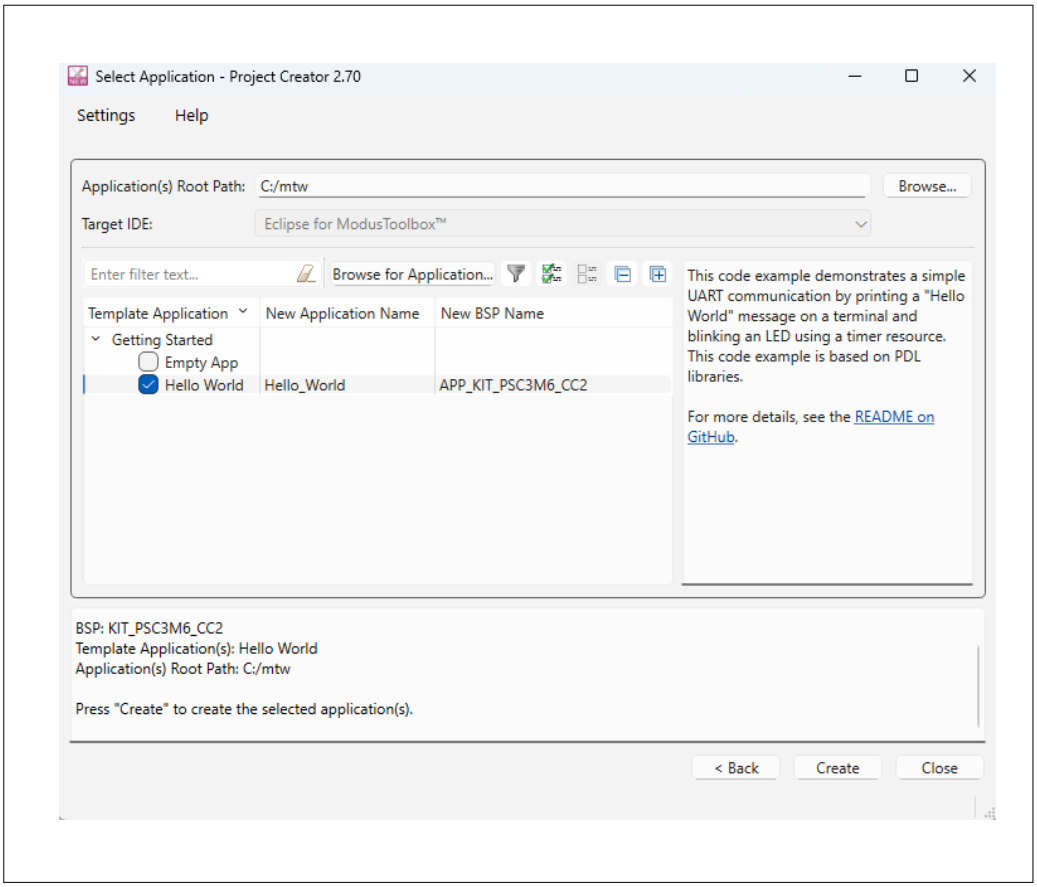


Figure 7 Select application

4. To build and program the PSOC™ Control C3M6 MCU application, do the following:

a. In the Project Explorer, select the **<App_Name>** project

b. In the Quick Panel tab, scroll to the **Launches**

c. Click the **<App_Name> Program (J-Link)** configuration

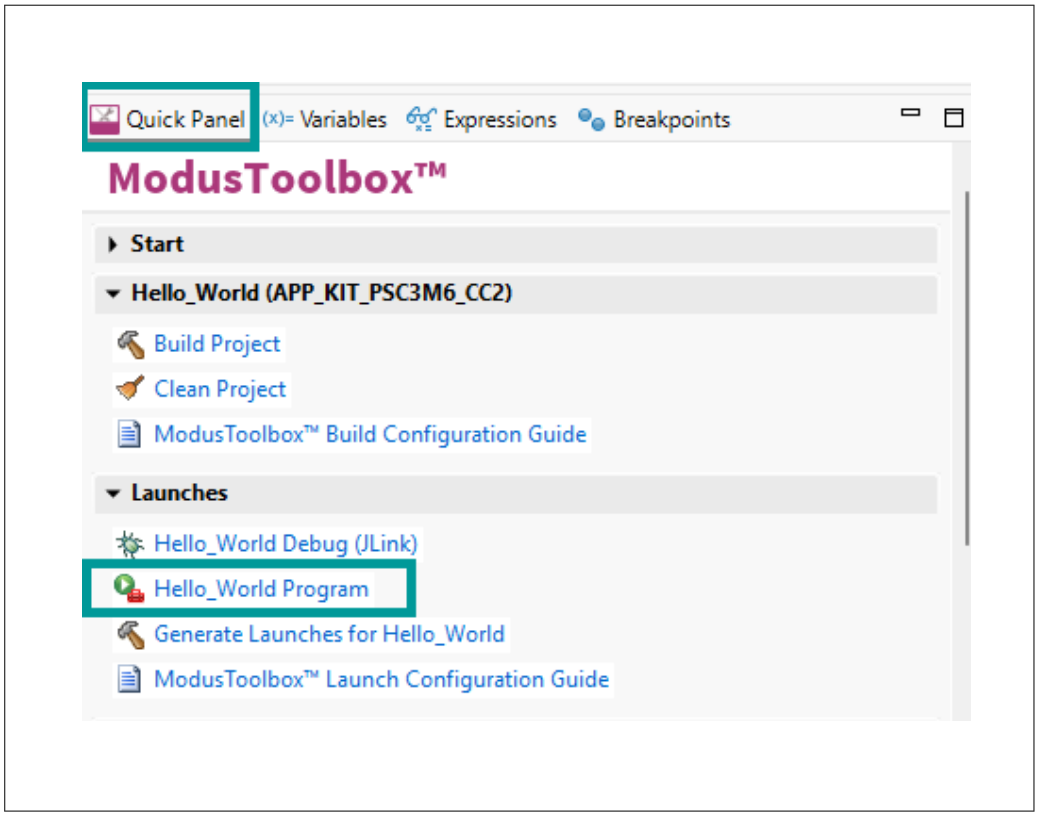


Figure 8 Programming in ModusToolbox™

5. ModusToolbox™ software has an integrated debugger. To debug a PSOC™ Control C3M6 MCU application:
   a. In the Project Explorer, select the **<App_Name>** project
   b. In the Quick Panel, scroll to the Launches section and click the **<App_Name> Debug (J-Link)** configuration. For more information, see the Program and debug section in the Eclipse IDE for ModusToolbox™ user guide

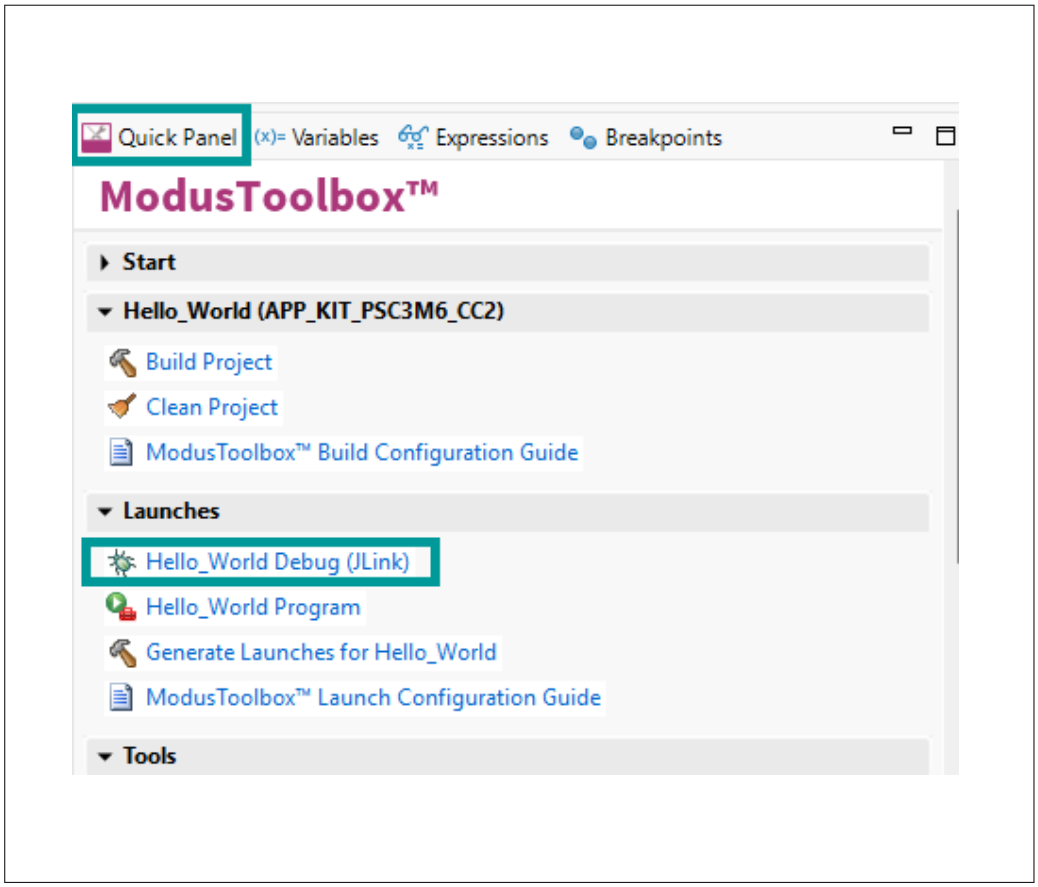


Figure 9 Debugging in ModusToolbox™

3 Hardware

3.1 Functional description

This section provides a detailed explanation of the individual hardware blocks used in this kit.

3.2 KIT_PSC3M6_CC2 PSOC™ Control C3M6 Motor Control Card

The control card is designed for the PSOC™ Control C3M6 microcontroller in an E-LQFP-100 package. The onboard isolated J-Link debugger is implemented using the XMC4200 microcontroller. Most of the I/Os from the PSOC™ Control C3M/P6 MCU are routed out to the 100-pin high-density (HD) connector, which provides connectivity to the motor control power boards using MADK HD100. Some I/Os from the PSOC™ Control C3M/P6 MCU are routed out to the on-board M1/M3 and M5 connectors which provide connectivity to the motor control power boards using MADK M1/M3, M5.

3.3 PSOC™ Control C3M/P6 MCU

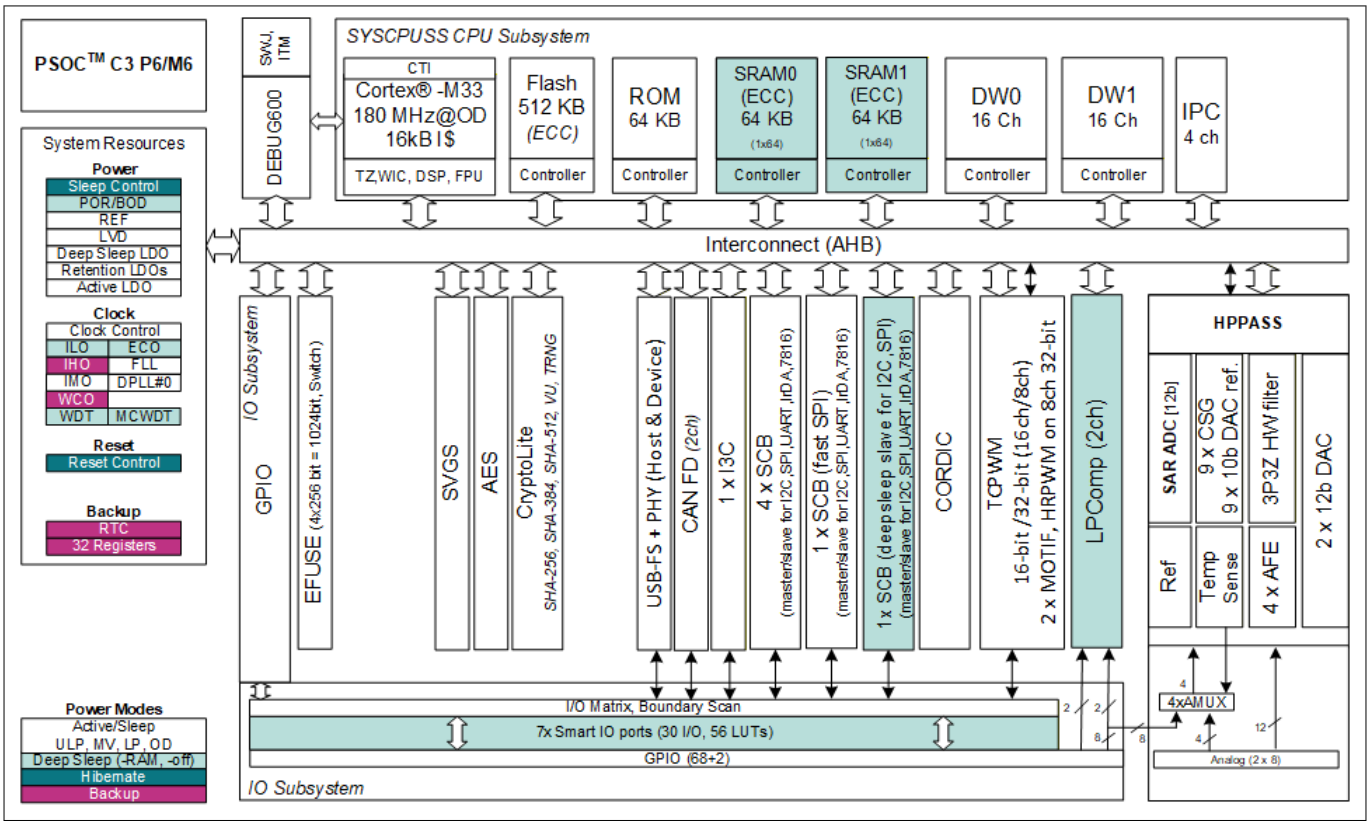


Figure 10 PSOC™ Control C3M/P6 MCU block diagram

The PSC3M6xD devices are based on the Arm® Cortex® -M33 microcontroller, running at up to 180 MHz with DSP and FPU capabilities. In addition to the CPU subsystem, the devices contain advanced real-time control peripherals, such as a high-performance programmable analog subsystem, comparators, advanced timers with high-resolution capability, up to six serial communication blocks (SCBs), and two CAN FDs for communication. The devices support one Active mode and five low-power modes for managing and reducing power consumption depending on application requirements.

3.4 PSOC™ Control C3M/P6 MCU power supply

The PSOC™ C3M/P6 MCU operates using a single regulated VDDD supply within the range of 1.71 V to 3.6 V. Additionally, there is an optional VBACKUP supply, which has a range of 1.4 V to 3.6 V. A linear regulator powers the core logic at four voltage levels: 0.9 V, 1.0 V, 1.1 V, and 1.2 V. Voltage level switching is implemented by writing to the power control registers. The voltage for the core logic can be set based on the application's performance and power requirements.

Typically, the backup domain requires an input voltage of 1.4 V to 3.6 V, which can be provided by connecting a backup battery or a super capacitor to the VBACKUP pin. The internal backup switch automatically selects between VDDD and VBACKUP (when VDDD is no longer available) for powering the backup domain peripherals like the RTC, WCO, ILO, and backup registers. Some I/O cells are powered from the VBACKUP supply before the internal backup switch. If the application does not require a dedicated backup source, VBACKUP can be connected to VDDD externally to ensure that the I/O cells powered by VBACKUP are functional.

The PSOC™ Control C3 MCU operates at 3.3 V, while the rest of the board requires both 3.3 V and 5 V supplies. The 3.3 V, used to power the MCU, is generated using the on-board low-dropout regulator. The 5V rail, which powers this regulator as well as the rest of the circuits running on 3 V or 5 V, can be sourced from any of the following options:

1. **Isolated USB supply:** The USB 5 V supply is used to power a 5 V isolated DC/DC converter, which in turn generates a 5V supply
2. **User USB supply:** The USB 5 V supply is used as 5 V supply
3. **Terminal block PWR connector:** External power supply with nominal voltage in a range of 7 V to 24 V is used to power on-board switching DC/DC regulator, which in turn generates 5 V supply
4. **5 V or 24 V supply from the power board:** The board can be powered by any of the following sources:
   a. 100-pin HD connector: 5 V or 24 V provided by MADK board
   b. M1/M3 connector: 3.3 V or 24 V provided by MADK board
   c. M5 connector: 24 V provided by MADK board

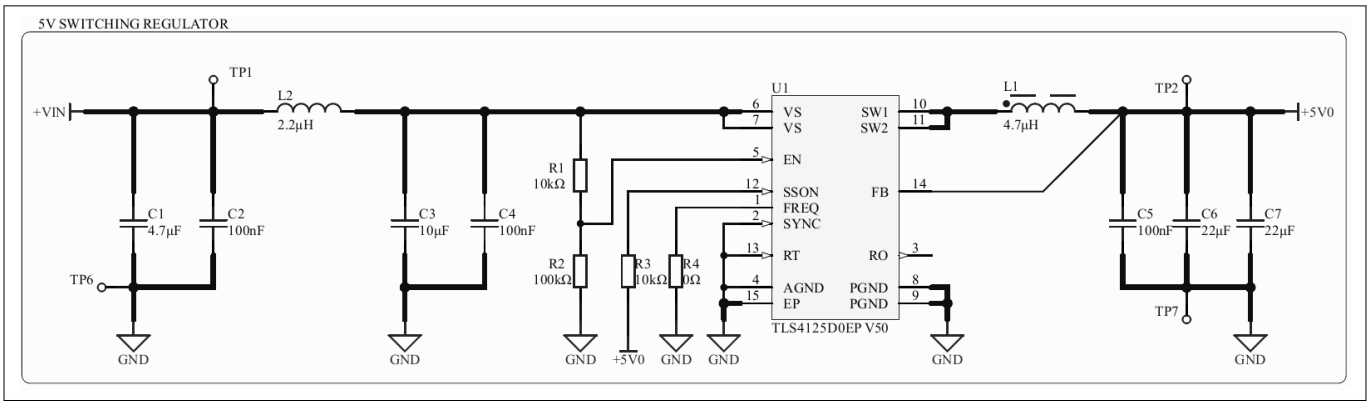


Figure 11 5 V switching regulator

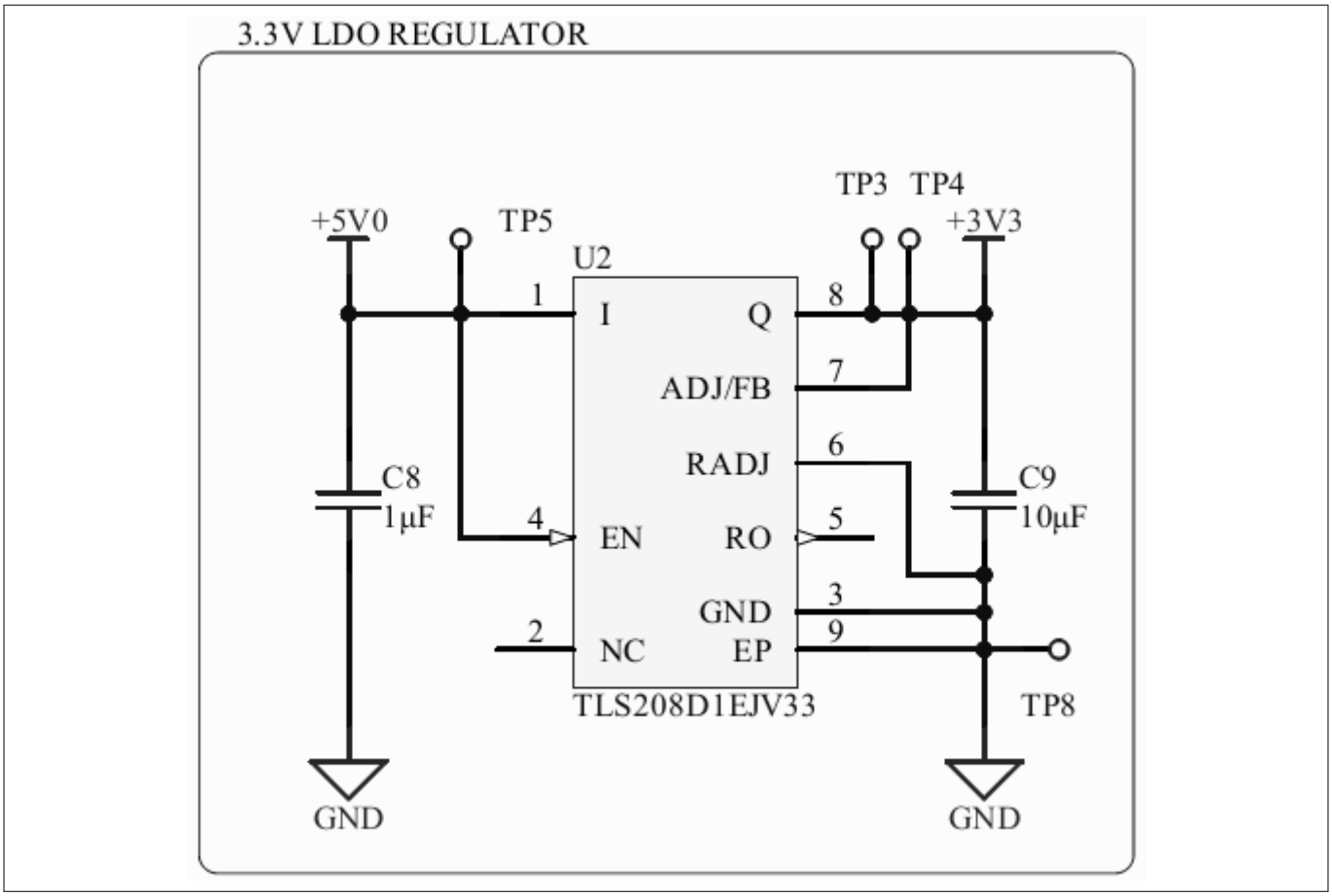


Figure 12 3.3V LDO regulator

3.5 PSOC™ Control C3M/P6 MCU clock sources

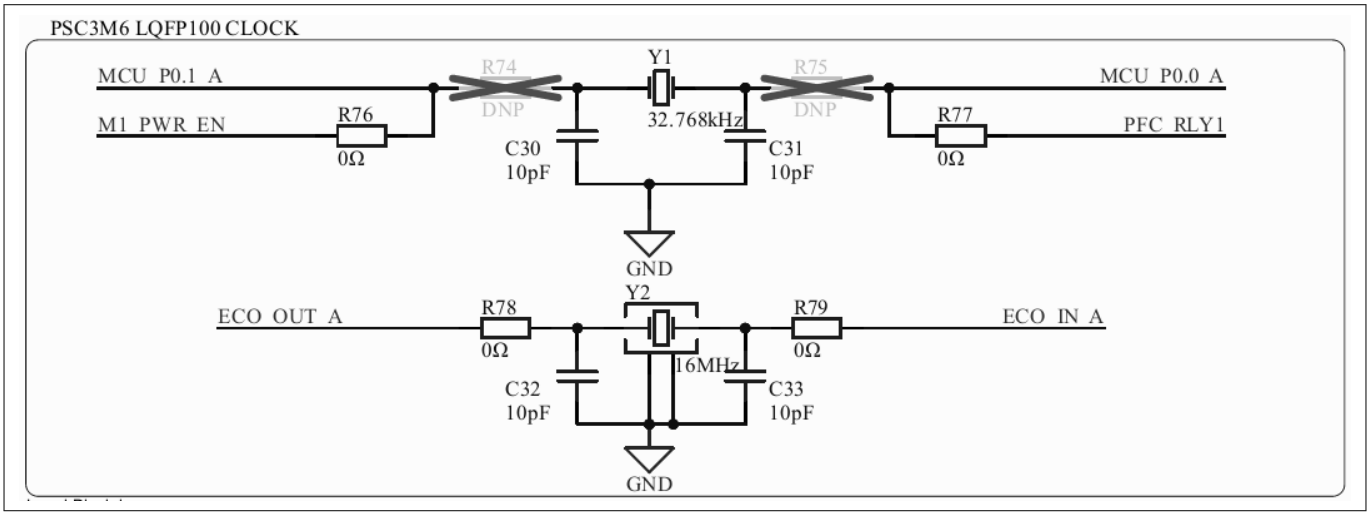


Figure 13 KIT_PSC3M6_CC2 ECO and WCO

The KIT_PSC3M6_CC2 provides the following two crystals as clock sources for PSC3M/P6 MCU:

- 16 MHz crystal is connected to P1.0 and P1.1 as external crystal oscillator (ECO)
- 32.768 kHz crystal, by default not connected to P0.0 and P0.1, as watch crystal oscillator (WCO). To connect WCO as a clock source, user is required to de-solder resistors R76 (0R) and R77(0R) and solder resistors R74(0R) and R75(0R)

3.6 PSOC™ Control C3M/P6 MCU programming and debugging

On-board programmer/debugger

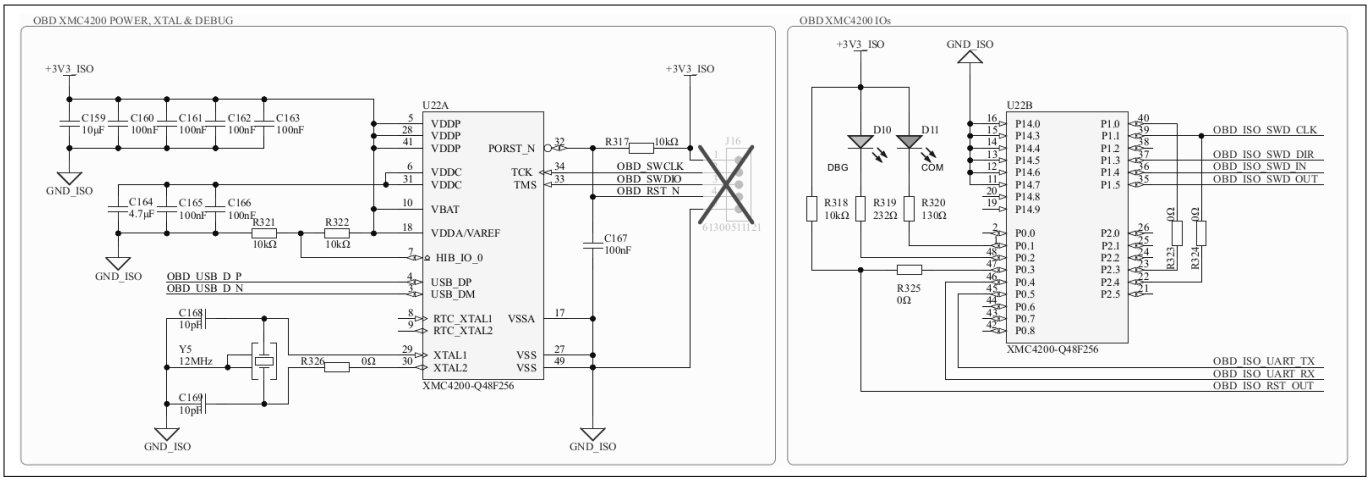


Figure 14 XMC4200 as an onboard programmer/debugger

The XMC4200-based onboard J-Link Lite programmer/debugger provides the SWD interface as well as the UART interface over USB for the target MCU. XMC4200 is powered using the 5 V USB supply, which is converted to 3.3 V using the LDO voltage regulator. The **DBG** Orange LED is ON when the USB interface is connected to the PC. The **COM** Green LED blinks during active communication between the debugger and the target MCU.

Non-isolated external debug option

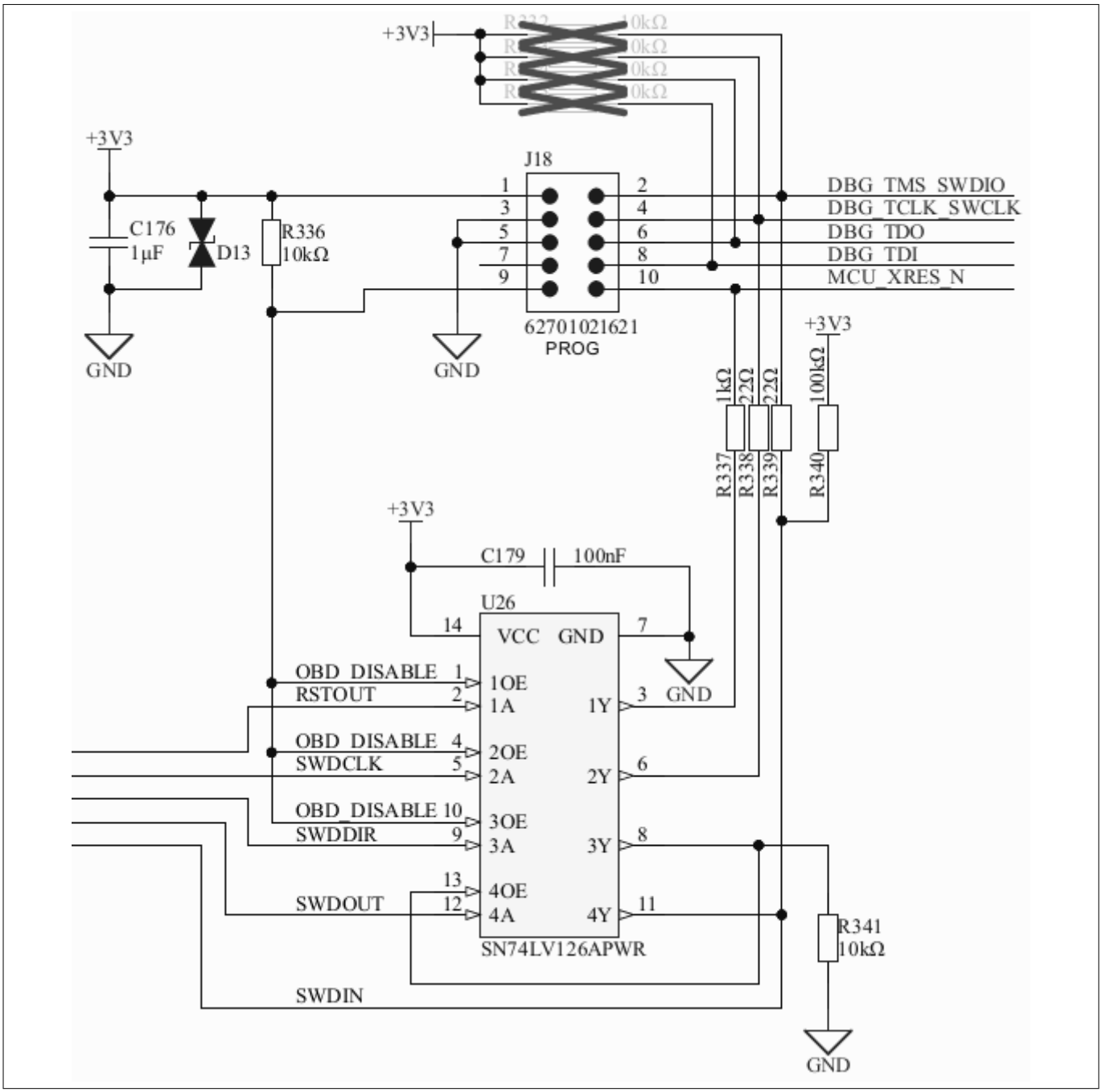


Figure 15 Programming/debugging connector header (PROG)

The board features a 10-pin 1.27 mm pitch Arm® Cortex® programming/debugging connector header (**PROG**). The selection between the isolated onboard debugger or the Cortex® 10-pin connector header (**PROG**) is automatically managed using on-board logic. When user connects external programmer/debugger to Cortex® 10-pin connector header (**PROG**), all programming/debugging I/Os between MCU and isolated on-board debugger are disconnected.

***Note**: The external programmer/debugger connections to MCU are not isolated.*

***Note**: In order to use automatic selection between debugging interfaces, user needs to make sure that pin 9 on Cortex® 10-pin connector header (**PROG**) is pulled to GND from external programmer/debugger device.*

DFU bootloader

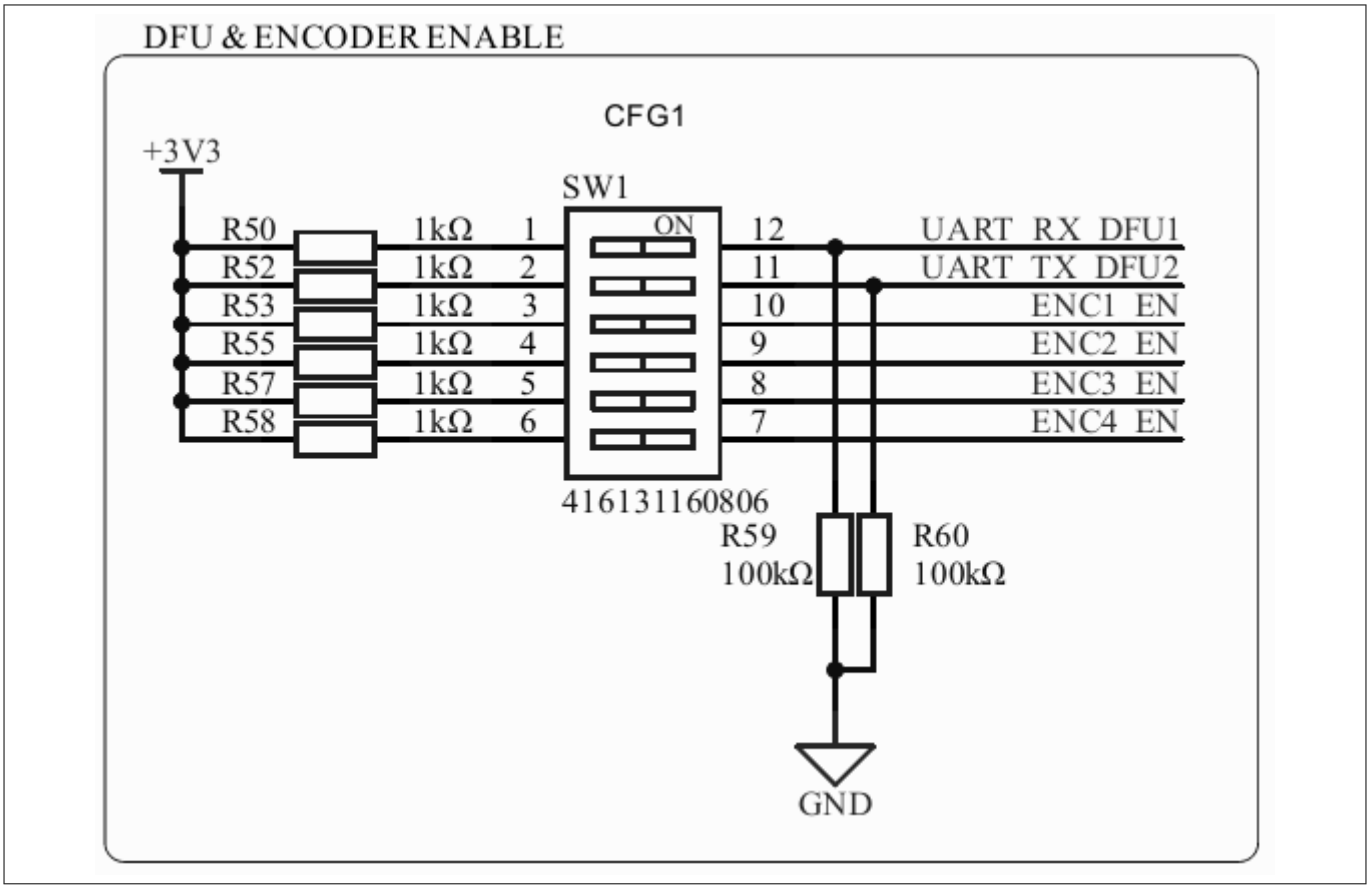


Figure 16 DFU & encoder config switch

The boot ROM supports firmware updates using a serial port. DFU functionality is disabled by default. It needs to be enabled in the OEM policy before use. For more details on how to enable and use DFU can be found in AN240106 - Getting started with PSOC™ Control C3 security.

When enabled, DFU mode selection is initiated during device boot-up depending on the **CFG1** config switch positions 1-12 and 2-11, as shown in Table 2.

Table 2 CFG1 switch positions for DFU mode selection

CFG1 position		DFU mode
1-12	**2-11**	
OFF	OFF	Disabled (Default)
ON	OFF	I2C
OFF	ON	UART
ON	ON	SPI

3.7 Analog subsystem

Analog input buffer and filter

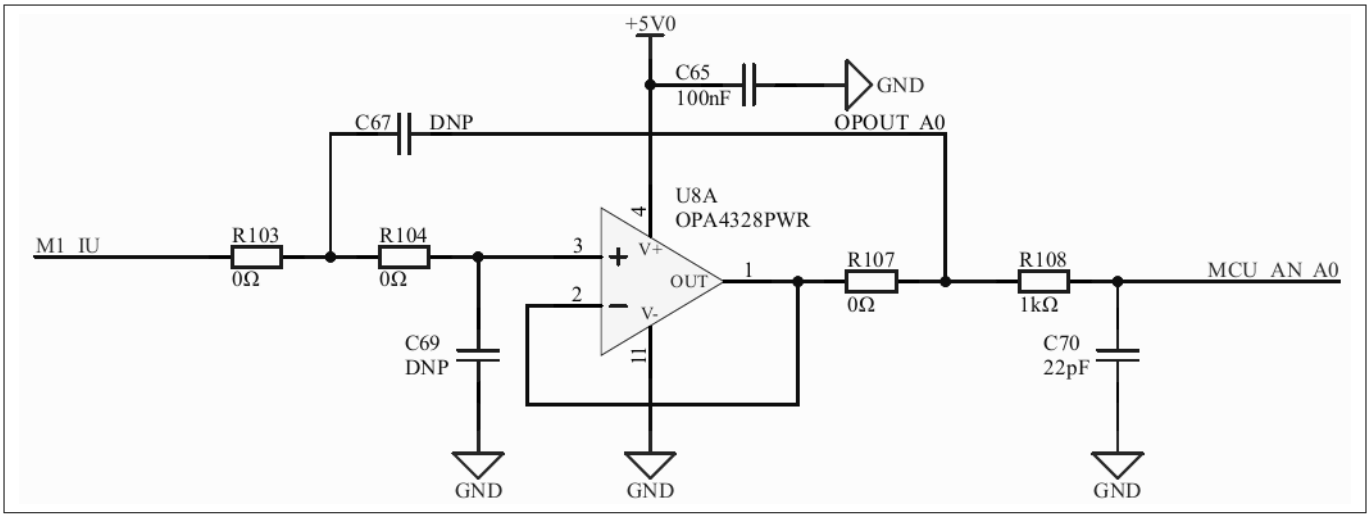


Figure 17 Analog input buffer & filter (single channel)

The analog signals coming from power stages, such as phase currents or back electromotive force (BEMF) voltages, DC link current, bus voltage, etc., are buffered using a unity gain amplifiers in the default configuration. All sixteen (AN_A0-AN_A7, AN_B0-AN_B7) analog input signal are buffered/filtered trough unity gain amplifier.

Unity gain amplifiers can be operated also as a second-order Sallen–Key filter by placing additional resistor and capacitor components on already predefined defined footprints.

Output from unity gain amplifier is connected to RC filter with cut-off frequency of 7.2 MHz. RC filter in combination with Analog Input Attenuation Switches **CFG2** and **CFG3** is used to make 5 V analog signals compatible with the 3.3V analog-to-digital converter (ADC) in the PSOC™ Control C3 MCU.

Unity gain amplifiers can be bypassed by removing 0R resistor from amplifier output (in our example R107) and placing 0R resistor on feedback capacitor footprint (in our example C67).

For additional information, schematics and footprint positions on the board, please see to the Production data section.

Analog input attenuation switches

As already mentioned in previous section, RC filter in combination with analog input attenuation switches **CFG2** and **CFG3** is used to make 5 V analog signals compatible with the 3.3 V analog-to-digital converter (ADC) in the PSOC™ Control C3 MCU.

By placing positions on switches into ON state, effectively we are placing resistor voltage divider between output of unity gain amplifier and analog input of MCU.

$$V_{OUT} = \frac{R_2}{R_1 + R_2} \times V_{IN}$$

where:

- V_{IN} - Analog input from a power board, for example DC link current
- V_{OUT} - Analog output from unity gain amplifier connected to MCU's AN_AN pin
- R_1 - In our case 1 kΩ resistor, part of RC filter network
- R_2 - In out case 2 kΩ resistor, part of attenuation switch circuit

With possibility to attenuate signals we are allowing powers boards with analog output range of 5 V to be attached to KIT_PSC3M6_CC2 board and operate with the 3.3 V analog-to-digital converter. In case that power board has analog output voltage in 3.3 V range, attenuation is not needed.

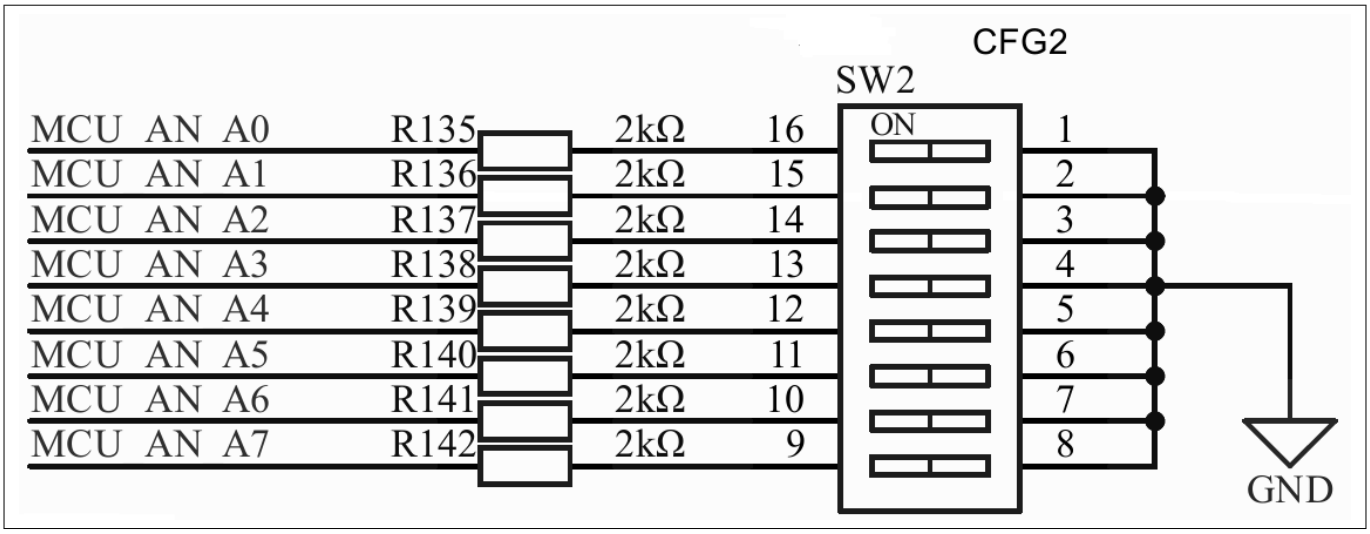


Figure 18 **Attenuation switch for A0-A7 inputs**

Table 3 **CFG2 switch positions**

Function (Net name)	Position	State	Description	PSC3 pin
M1_IU	1-16	ON	Signal attenuated by 1/3	AN_A0
M1_IV	2-15	ON	Signal attenuated by 1/3	AN_A1
M1_IW	3-14	ON	Signal attenuated by 1/3	AN_A2
M1_IDC	4-13	ON	Signal attenuated by 1/3	AN_A3
M1_VDC	5-12	ON	Signal attenuated by 1/3	AN_A4
M2_IU	6-11	ON	Signal attenuated by 1/3	AN_A5
M2_IV	7-10	ON	Signal attenuated by 1/3	AN_A6
M2_IW	8-9	ON	Signal attenuated by 1/3	AN_A7

Default state for **CFG2** switch positions is ON.

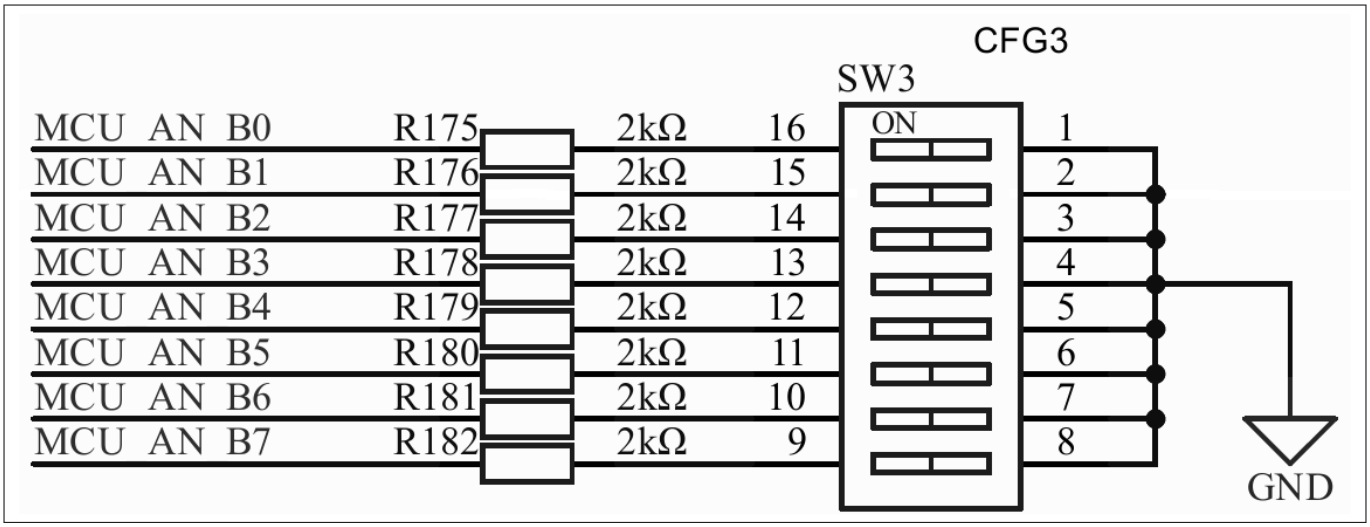


Figure 19 **Attenuation switch for B0-B7 inputs**

Table 4 CFG3 switch positions

Function (Net name)	Position	State	Description	PSC3 pin
M3_IU_M1_VU	1-16	ON	Signal attenuated by 1/3	AN_B0
M3_IV_M1_VV	2-15	ON	Signal attenuated by 1/3	AN_B1
M3_IW_M1_VW	3-14	ON	Signal attenuated by 1/3	AN_B2
M2_IDC	4-13	ON	Signal attenuated by 1/3	AN_B3
M4_IU_M4_IDC	5-12	ON	Signal attenuated by 1/3	AN_B4
M4_IV	6-11	ON	Signal attenuated by 1/3	AN_B5
M1_TMP_PFC_NTC	7-10	ON	Signal attenuated by 1/3	AN_B6
M3_IDC_PFC_VDC	8-9	ON	Signal attenuated by 1/3	AN_B7

Default state for **CFG3** switch positions is ON.

Analog output buffer

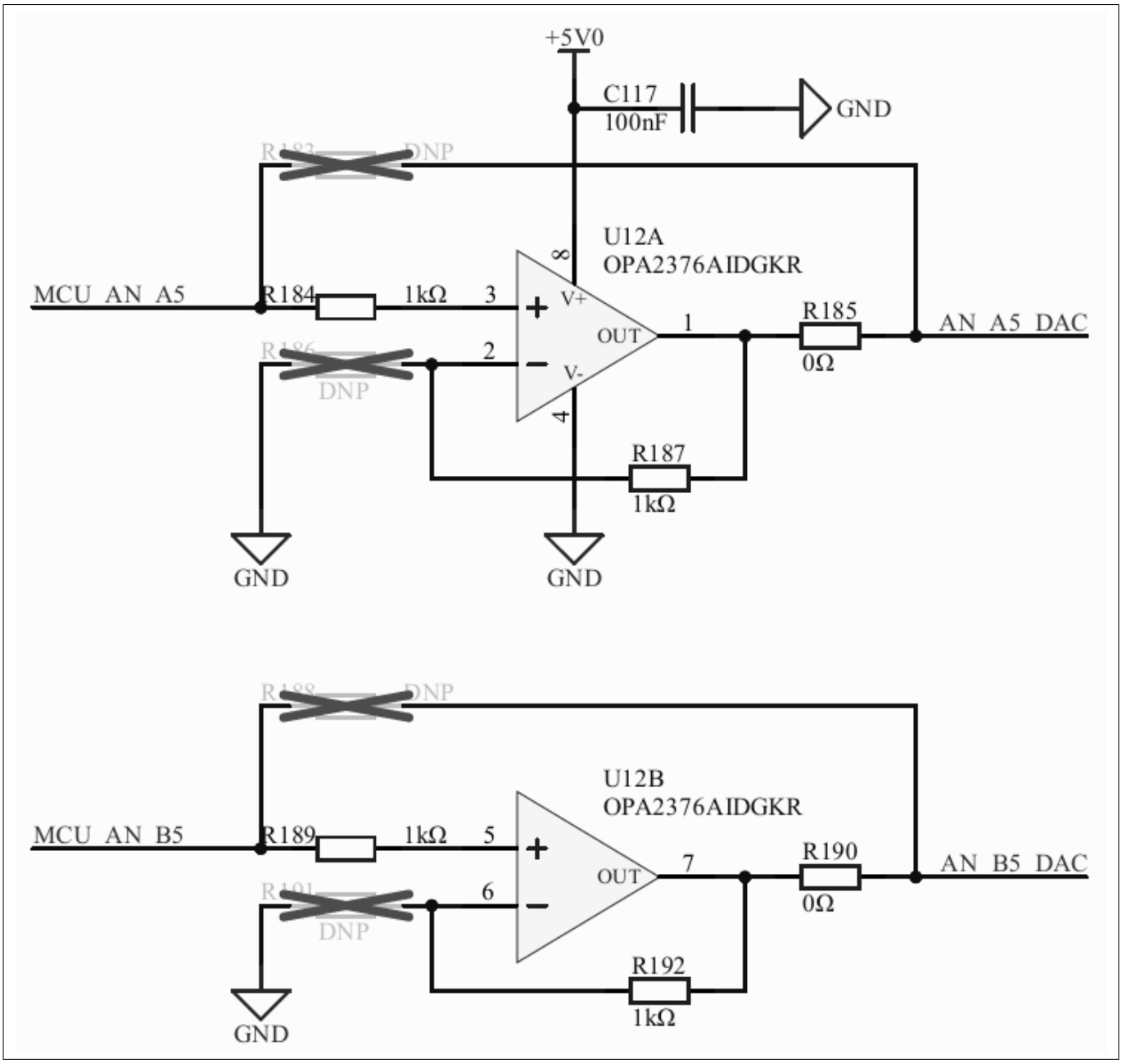


Figure 20 Analog output (DAC) buffer

The PSOC™ Control C3 MCU analog pins AN_A5 and AN_B5 are also DAC outputs and they are buffered troughs unity gain amplifier.

External VAREF connection

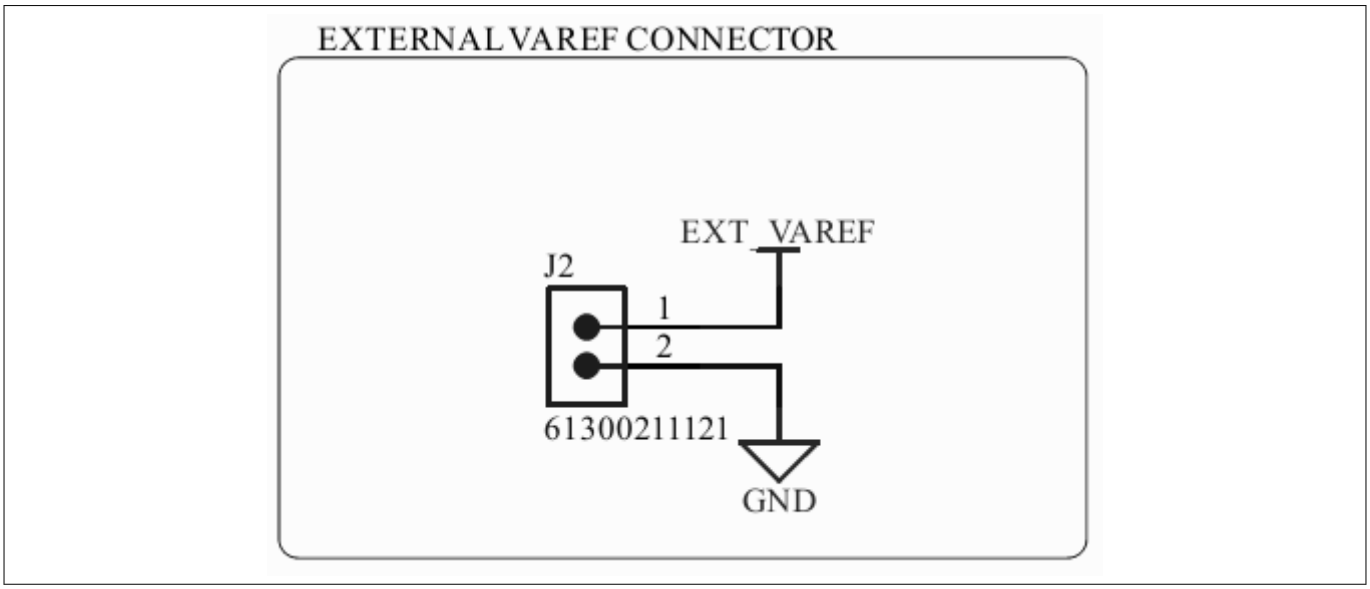


Figure 21 VAREF connector

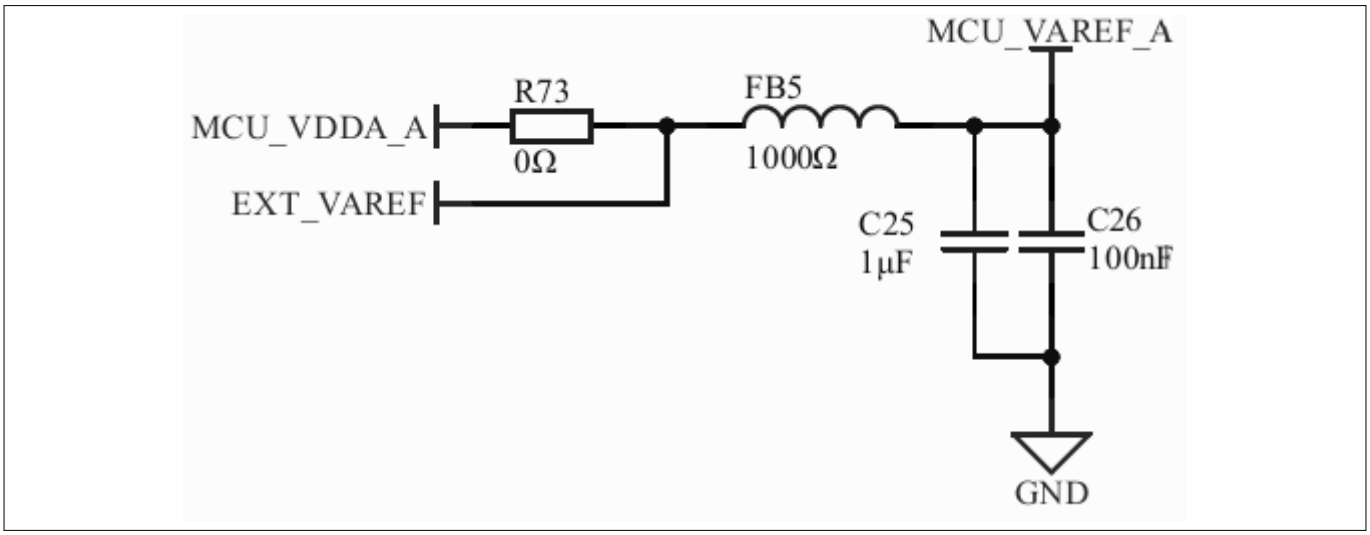


Figure 22 MCU VAREF power supply circuit

KIT_PSC3M6_CC2 provides connector (not placed by default) and additional circuitry to enable connection of more precise analog reference voltage for the 3.3 V analog-to-digital converter (ADC) in the PSOC™ Control C3 MCU. Before analog reference voltage is provided on the connector, resistor R73(0R) needs to be de-soldered.

3.8 100-pin HD connector interface

PSC3M6 QFP100	HD100	NET NAME		J3		NET NAME	HD100	PSC3M6 QFP100
P5.1	IIC_SCL	SCB_MISO_SCL	A1		B1	SCB_MOSI_SDA	IIC_SDA	P5.0
P5.2	SPI_CLK	SCB_CLK	A2		B2	SCB_MOSI_SDA	SPI_MOSI	P5.0
P5.1	SPI_MISO	SCB_MISO_SCL	A3		B3	SCB_SEL0_USR_SW2	SPI_CS0	P5.3
	SPI_CS1	NC	A4		B4	NC	SPI_CS2	
	GND	GND	A5		B5	+5V0_HD100	PWR_IN_5V	
	AGND	GND	A6		B6	M1_IU	AIN_IU_VU	AN_A0
	AGND	GND	A7		B7	M1_IV	AIN_IV_VV	AN_A1
	AGND	GND	A8		B8	M1_IW	AIN_IW_VW	AN_A2
	AGND	GND	A9		B9	M1_IDC	AIN_IDC	AN_A3
	GND	GND	A10		B10	+5V0_HD100	PWR_IN_5V	
P4.1	PWM_UL	M1_PWM_UL	A11		B11	M1_PWM_UH	PWM_UH	P4.0
P4.3	PWM_VL	M1_PWM_VL	A12		B12	M1_PWM_VH	PWM_VH	P4.2
P4.5	PWM_WL	M1_PWM_WL	A13		B13	M1_PWM_WH	PWM_WH	P4.4
P8.0	ESTOP	M1_ESTOP	A14		B14	M1_PWR_EN	GD_EN	P0.1
P8.1	PWM_BRAKE	M1_BRK_PFC_RLY2	A15		B15	M1_TMP_PFC_NTC	AIN_TEMP1	AN_B6
	AGND	GND	A16		B16	M1_VDC	AIN_VDC	AN_A4
	AGND	GND	A17		B17	M3_IU_M1_VU	AIN_IU_VU	AN_B0
	AGND	GND	A18		B18	M3_IV_M1_VV	AIN_IV_VV	AN_B1
	AGND	GND	A19		B19	M3_IW_M1_VW	AIN_IW_VW	AN_B2
	AGND	GND	A20		B20	M2_IDC	AIN_IDC	AN_B3
	GND	GND	A21		B21	+3V3	PWR_OUT_VSYS	
P8.3	PWM_UL	M2_PWM_UL	A22		B22	M2_PWM_UH	PWM_UH	P8.2
P9.1	PWM_VL	M2_PWM_VL	A23		B23	M2_PWM_VH	PWM_VH	P9.0
P9.3	PWM_WL	M2_PWM_WL	A24		B24	M2_PWM_WH	PWM_WH	P9.2
P7.7	ESTOP	M2_ESTOP	A25		B25	M2_PWR_EN	GD_EN	P9.7
P9.4	GPIO_RES1	MCU_P9.4	A26		B26	MCU_P9.5	GPIO_RES2	P9.5
	GPIO_RES3	NC	A27		B27	NC	GPIO_RES4	
	AGND	GND	A28		B28	M2_IU	AIN_IU_VU	AN_A5
	AGND	GND	A29		B29	M2_IV	AIN_IV_VV	AN_A6
	AGND	GND	A30		B30	M2_IW	AIN_IW_VW	AN_A7
	AGND	GND	A31		B31	M3_IDC_PFC_VDC	AIN_IDC	AN_B7
DAC0	AIN_RES1	AN_A5_DAC	A32		B32	AN_B5_DAC	AIN_RES2	DAC1
P3.3	ESTOP	M3_ESTOP_PFC_OCP	A33		B33	M3_PWR_EN	GD_EN	P9.6
P7.1	PWM_UL	M3_PWM_UL	A34		B34	M3_PWM_UH	PWM_UH	P7.0
P7.3	PWM_VL	M3_PWM_VL	A35		B35	M3_PWM_VH	PWM_VH	P7.2
P12.1	PWM_WL	M3_PWM_WL	A36		B36	M3_PWM_WH	PWM_WH	P12.0
P8.7	ESTOP	M4_ESTOP	A37		B37	M4_PWR_EN	GD_EN	P8.6
P12.3	PWM_UL	M4_PWM_UL	A38		B38	M4_PWM_UH	PWM_UH	P12.2
P12.5	PWM_VL	M4_PWM_VL	A39		B39	M4_PWM_VH	PWM_VH	P12.4
P12.7	PWM_WL	M4_PWM_WL	A40		B40	M4_PWM_WH	PWM_WH	P12.6
	GND	GND	A41		B41	+24V_HD100	PWR_IN_24V	
AN_B4	AIN_IU_VU	M4_IU_M4_IDC	A42		B42	M4_IV	AIN_IV_VV	AN_B5
AN_B7	AIN_IW_VW	M3_IDC_PFC_VDC	A43		B43	M4_IU_M4_IDC	AIN_IDC	AN_B4
	AIN_RES4	NC	A44		B44	M2_IW	AIN_RES3	AN_A7
	AGND	GND	A45		B45	M2_IU	AIN_PFC_I1	AN_A5
AN_B7	AIN_PFC_VDC	M3_IDC_PFC_VDC	A46		B46	M2_IV	AIN_PFC_I2	AN_A6
P3.3	GPIO_RES5	M3_ESTOP_PFC_OCP	A47		B47	NC	AIN_RES5	
	AIN_RES6	NC	A48		B48	M1_TMP_PFC_NTC	AIN_TEMP2	AN_B6
P0.0	PFC_RELAY1	PFC_RLY1	A49		B49	M1_BRK_PFC_RLY2	PFC_RELAY2	P8.1
P6.0	PWM_PFC_H	PFC_PWM_H	A50		B50	PFC_PWM_L	PWM_PFC_L	P6.1

MH1 MH2
FX2-100S-1.27DSL(71)
GND GND

Figure 23 100-pin HD connector interface

The 100-pin HD connector interfaces with the drive adapter card, providing connectivity for MADK motor power stages. It supports connection of up to four motors, as well as optional power factor correction (PFC) control.

Table 5 HD connector pin-out details

Function (Net name)	PSC3 pin	HD pin	HD pin	PSC3 pin	Function (Net name)
SCB_MISO_SCL	P5.1	**A1**	**B1**	P5.0	SCB_MOSI_SDA
SCB_CLK	P5.2	**A2**	**B2**	P5.0	SCB_MOSI_SDA
SCB_MISO_SCL	P5.1	**A3**	**B3**	P5.3	SCB CS0
-	-	**A4**	**B4**	-	-
Ground	GND	**A5**	**B5**	+5V0	PWR_IN_5V
Analog ground	AGND	**A6**	**B6**	AN_A0	AIN_IU_VU
Analog ground	AGND	**A7**	**B7**	AN_A1	AIN_IV_VV
Analog ground	AGND	**A8**	**B8**	AN_A2	AIN_IW_VW
Analog ground	AGND	**A9**	**B9**	AN_A3	AIN_IDC
Ground	GND	**A10**	**B10**	+5V0	PWR_IN_5V
M1_PWM_UL	P4.1	**A11**	**B11**	P4.0	M1_PWM_UH
M1_PWM_VL	P4.3	**A12**	**B12**	P4.2	M1_PWM_VH
M1_PWM_WL	P4.5	**A13**	**B13**	P4.4	M1_PWM_WH
M1_ESTOP	P8.0	**A14**	**B14**	P0.1	M1_PWR_EN
M1_BRK_PFC_RLY2	P8.1	**A15**	**B15**	AN_B6	M1_TEMP_PFC_NTC
Analog ground	AGND	**A16**	**B16**	AN_A4	M1_VDC
Analog ground	AGND	**A17**	**B17**	AN_B0	M3_IU_M1_VU
Analog ground	AGND	**A18**	**B18**	AN_B1	M3_IV_M1_VV
Analog ground	AGND	**A19**	**B19**	AN_B2	M3_IW_M1_VW
Analog ground	AGND	**A20**	**B20**	AN_B3	M2_IDC
Ground	GND	**A21**	**B21**	+3V3	PWR_OUT_VSYS
M2_PWM_UL	P8.3	**A22**	**B22**	P8.2	M2_PWM_UH
M2_PWM_VL	P9.1	**A23**	**B23**	P9.0	M2_PWM_VH
M2_PWM_WL	P9.3	**A24**	**B24**	P9.2	M2_PWM_WH
M2_ESTOP	P7.7	**A25**	**B25**	P9.7	M2_PWR_EN
MCU_P9.4	P9.4	**A26**	**B26**	P9.5	MCU_P9.5
-	-	**A27**	**B27**	-	-
Analog ground	AGND	**A28**	**B28**	AN_A5	M2_IU
Analog ground	AGND	**A29**	**B29**	AN_A6	M2_IV
Analog ground	AGND	**A30**	**B30**	AN_A7	M2_IW
Analog ground	AGND	**A31**	**B31**	AN_B7	M3_IDC_PFC_VDC
An_A5_DAC	AN_A5	**A32**	**B32**	AN_B5	AN_B5_DAC
M3_ESTOP_PFC_OCP	P3.3	**A33**	**B33**	P9.6	M3_PWR_EN

(table continues...)

Table 5 (continued) HD connector pin-out details

Function (Net name)	PSC3 pin	HD pin	HD pin	PSC3 pin	Function (Net name)
M3_PWM_UL	P7.1	**A34**	**B34**	P7.0	M3_PWM_UH
M3_PWM_VL	P7.3	**A35**	**B35**	P7.2	M3_PWM_VH
M3_PWM_WL	P12.1	**A36**	**B36**	P12.0	M3_PWM_WH
M4_ESTOP	P8.7	**A37**	**B37**	P8.6	M4_PWR_EN
M4_PWM_UL	P12.3	**A38**	**B38**	P12.2	M4_PWM_UH
M4_PWM_VL	P12.5	**A39**	**B39**	P12.4	M4_PWM_VH
M4_PWM_WL	P12.7	**A40**	**B40**	P12.6	M4_PWM_WH
Ground	GND	**A41**	**B41**	+24V	PWR_IN_24V
M4_IU_M4_IDC	AN_B4	**A42**	**B42**	AN_B5	M4_IV
M3_IDC_PFC_VDC	AN_B7	**A43**	**B43**	AN_B4	M4_IU_M4_IDC
-	-	**A44**	**B44**	AN_A7	M2_IW
Analog ground	AGND	**A45**	**B45**	AN_A5	M2_IU
AIN_PFC_VDC	AN_B7	**A46**	**B46**	AN_A6	M2_IV
GPIO_RES5	P3.3	**A47**	**B47**	-	-
-	-	**A48**	**B48**	AN_B6	M1_TMP_PFC_NTC
PFC_RLY1	P0.0	**A49**	**B49**	P8.1	M1_BRK_PFC_RLY2
PFC_PWM_H	P6.0	**A50**	**B50**	P6.1	PFC_PWM_L

3.9 M1/M3 and M5 connector interface

M1/M3 connector interface

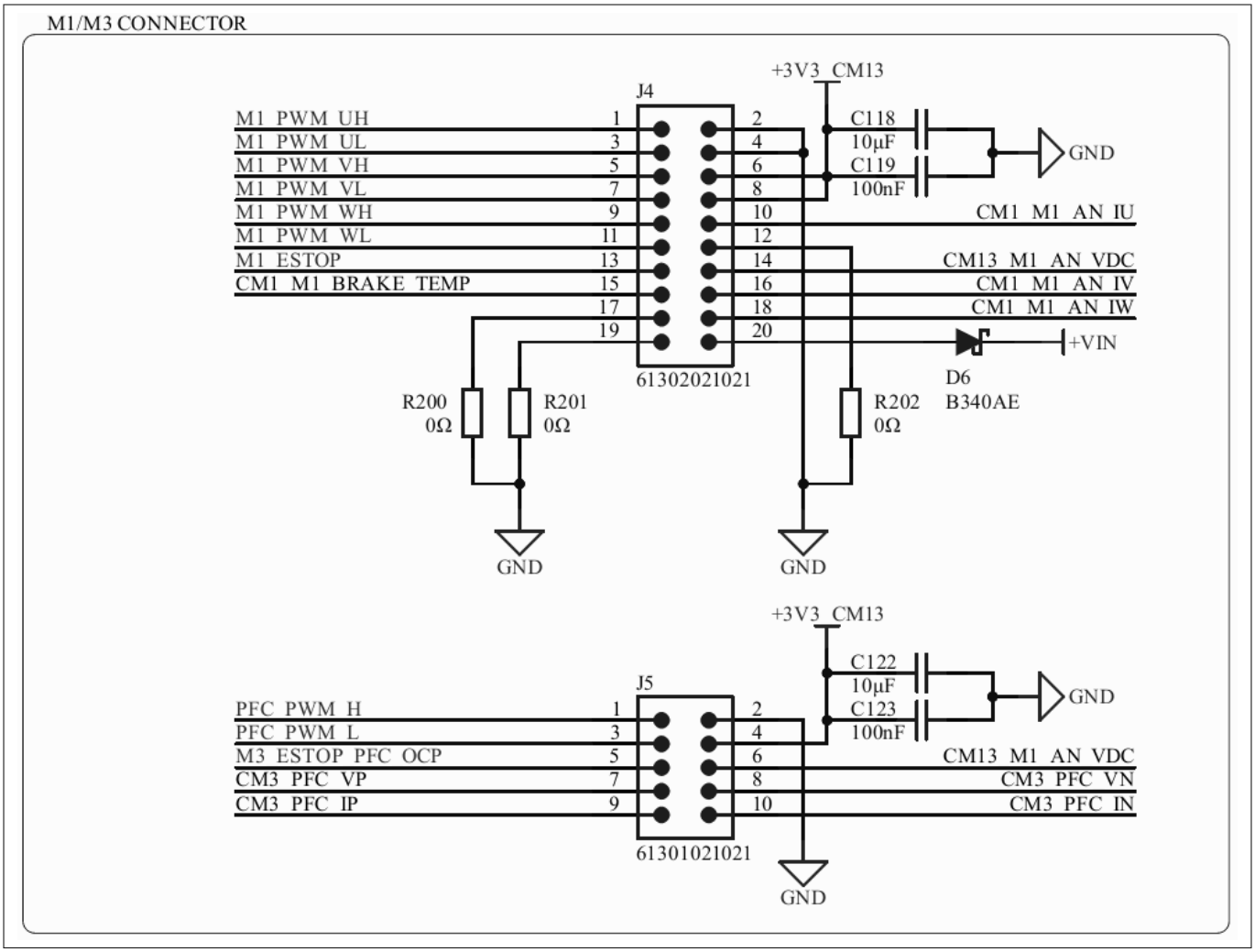


Figure 24 M1/M3 connector interface

Table 6 M1 connector pin-out details

Function (Net name)	PSC3 pin	M1 pin	M1 pin	PSC3 pin	Function (Net name)
M1_PWM_UH	P4.0	**1**	**2**	GND	Ground
M1_PWM_UL	P4.1	**3**	**4**	GND	Ground
M1_PWM_VH	P4.2	**5**	**6**	+3V3	PWR_OUT_VSYS
M1_PWM_VL	P4.3	**7**	**8**	+3V3	PWR_OUT_VSYS
M1_PWM_WH	P4.4	**9**	**10**	*	CM1_M1_AN_IU
M1_PWM_WL	P4.5	**11**	**12**	GND	Ground via 0R resistor
M1_ESTOP	P8.0	**13**	**14**	*	CM13_M1_AN_VDC
CM1_M1_BRAKE_TEMP	*	**15**	**16**	*	CM1_M1_AN_IV
Ground via 0R resistor	GND	**17**	**18**	*	CM1_M1_AN_IW
Ground via 0R resistor	GND	**19**	**20**	+24V	PWR_IN_24V

Table 7 M3 connector pin-out details

Function (Net name)	PSC3 pin	M3 pin	M3 pin	PSC3 pin	Function (Net name)
PFC_PWM_H	P6.0	**1**	**2**	GND	Ground
PFC_PWM_L	P6.1	**3**	**4**	+3V3	PWR_OUT_VSYS
M3_ESTOP_PFC_OCP	P3.3	**5**	**6**	*	CM13_M1_AN_VDC
CM3_PFC_VP	*	**7**	**8**	*	CM3_PFC_VN
CM3_PFC_IP	*	**9**	**10**	*	CM3_PFC_IN

***Note**: Signals marked with asterisk (*) have connections and functionality described in section M1/M3 & M5 configuration switches.*

M5 connector interface

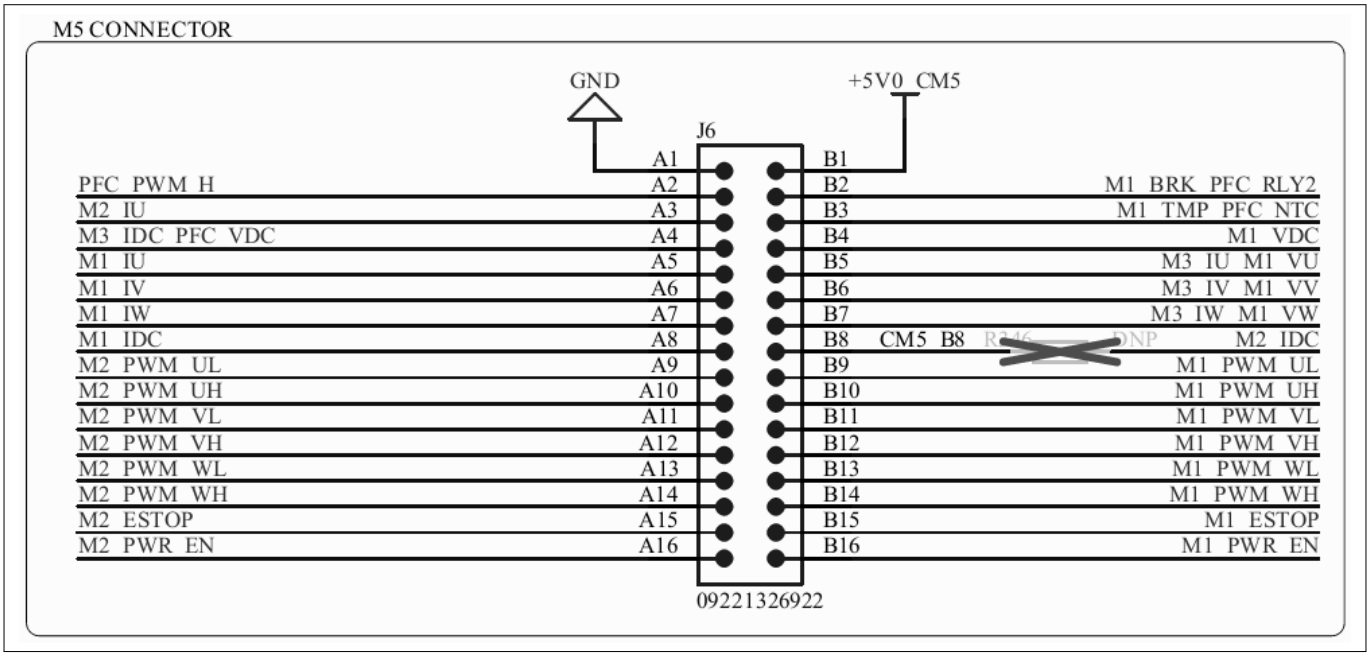


Figure 25 M5 connector interface

Table 8 M5 connector pin-out details

Function (Net name)	PSC3 pin	M5 pin	M5 pin	PSC3 pin	Function (Net name)
Ground	GND	**A1**	**B1**	+5V	PWR_IN_5V
PFC_PWM_H	P6.0	**A2**	**B2**	P8.1	M1_BRK_PFC_RLY2
M2_IU	AN_A5	**A3**	**B3**	AN_B6	M1_TMP_PFC_NTC
M3_IDC_PFC_VDC	AN_B7	**A4**	**B4**	AN_A4	M1_VDC
M1_IU	AN_A0	**A5**	**B5**	AN_B0	M3_IU_M1_VU
M1_IV	AN_A1	**A6**	**B6**	AN_B1	M3_IV_M1_VV
M1_IW	AN_A2	**A7**	**B7**	AN_B2	M3_IW_M1_VW
M1_IDC	AN_A3	**A8**	**B8**	*	CM5_B8* / M2_IDC (AN_B3)
M2_PWM_UL	P8.3	**A9**	**B9**	P4.1	M1_PWM_UL

(table continues...)

Table 8 (continued) M5 connector pin-out details

Function (Net name)	PSC3 pin	M5 pin	M5 pin	PSC3 pin	Function (Net name)
M2_PWM_UH	P8.2	**A10**	**B10**	P4.0	M1_PWM_UH
M2_PWM_VL	P9.1	**A11**	**B11**	P4.3	M1_PWM_VL
M2_PWM_VH	P9.0	**A12**	**B12**	P4.2	M1_PWM_VH
M2_PWM_WL	P9.3	**A13**	**B13**	P4.5	M1_PWM_WL
M2_PWM_WH	P9.2	**A14**	**B14**	P4.4	M1_PWM_WH
M2_ESTOP	P7.7	**A15**	**B15**	P8.0	M1_ESTOP
M2_PWR_EN	P9.7	**A16**	**B16**	P0.1	M1_PWR_EN

***Note**: Signals marked with asterisk (*) have connections and functionality described in section M1/M3 & M5 configuration switches.*

M1/M3 & M5 configuration switches

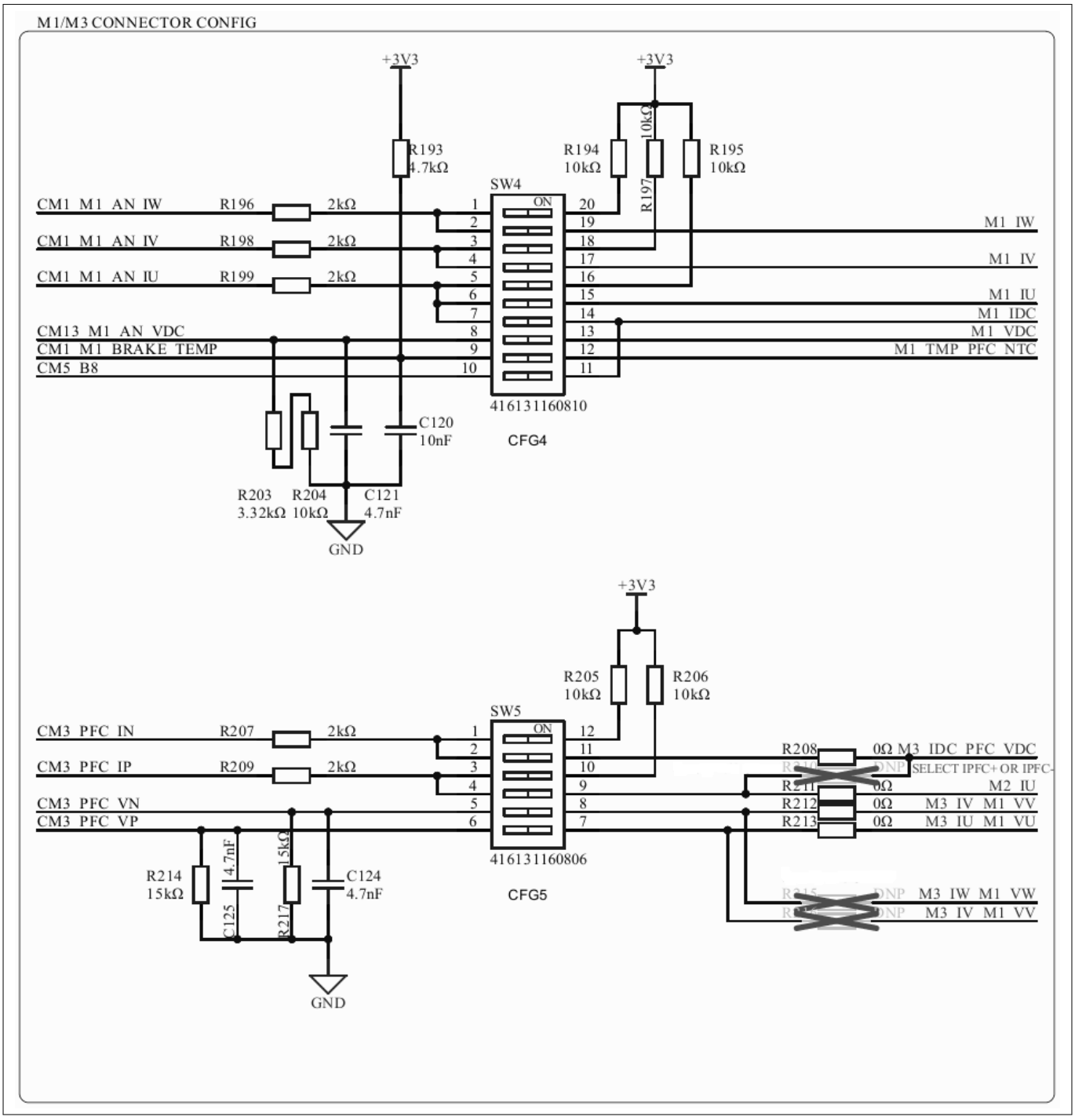


Figure 26 M1/M3 config switches

Table 9 CFG4 switch positions

Function (Net name)	Position	State	Description	Function	PSC3 pin
CM1_M1_AN_IW	1-20	ON	10 kΩ pull-up enabled	-	-
CM1_M1_AN_IW	2-19	ON	Connected to	M1_IW	AN_A2
CM1_M1_AN_IV	3-18	ON	10 kΩ pull-up enabled	-	-

(table continues...)

Table 9 (continued) CFG4 switch positions

Function (Net name)	Position	State	Description	Function	PSC3 pin
CM1_M1_AN_IV	4-17	ON	Connected to	M1_IV	AN_A1
CM1_M1_AN_IU	5-16	ON	10 kΩ pull-up enabled	-	-
CM1_M1_AN_IU	6-15	ON	Connected to	M1_IU	AN_A0
CM1_M1_AN_IU	7-14	ON	Connected to	M1_IDC	AN_A3
CM13_M1_AN_VDC	8-13	ON	Connected to	M1_VDC	AN_A4
CM1_M1_BRAKE_TEMP	9-12	ON	Connected to	M1_TMP_PFC_NTC	AN_B6
CM5_B8	10-11	ON	Connected to	M1_IDC	AN_A3

Table 10 CFG5 switch positions

Function (Net name)	Position	State	Description	Function	PSC3 pin
CM3_PFC_IN	1-12	ON	10 kΩ pull-up enabled	-	-
CM3_PFC_IN	2-11	ON	Connected to	M3_IDC_PFC_VDC	AN_B7
CM3_PFC_IP	3-10	ON	10 kΩ pull-up enabled	-	-
CM3_PFC_IP	4-9	ON	Connected to	M2_IU	AN_A5
CM3_PFC_VN	5-8	ON	Connected to	M3_IV_M1_VV	AN_B1
CM3_PFC_VP	6-7	ON	Connected to	M3_IU_M1_VU	AN_B0

3.10 Multi-motor sensor interface

Connector

Multi-motor sensor interface provides unified connector for both HALL and differential encoder inputs.

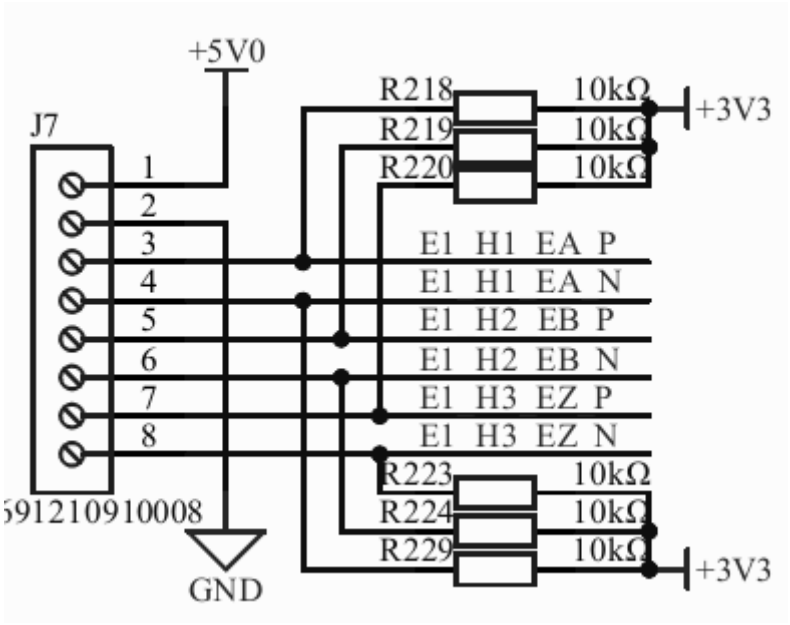


Figure 27 Encoder connector

Table 11 Encoder connector pin-out

Connector pin	Function	HALL	DIFF.
1	+5 V	-	-
2	GND	-	-
3	Input	H1	A+
4	Input	-	A-
5	Input	H2	B+
6	Input	-	B-
7	Input	H3	Z+
8	Input	-	Z-

HALL input buffer interface

When HALL is enabled (by default), inputs are buffered trough logic buffer accepting voltage levels up to 15 V. When HALL is disabled, outputs from the buffer are in High-Z state.

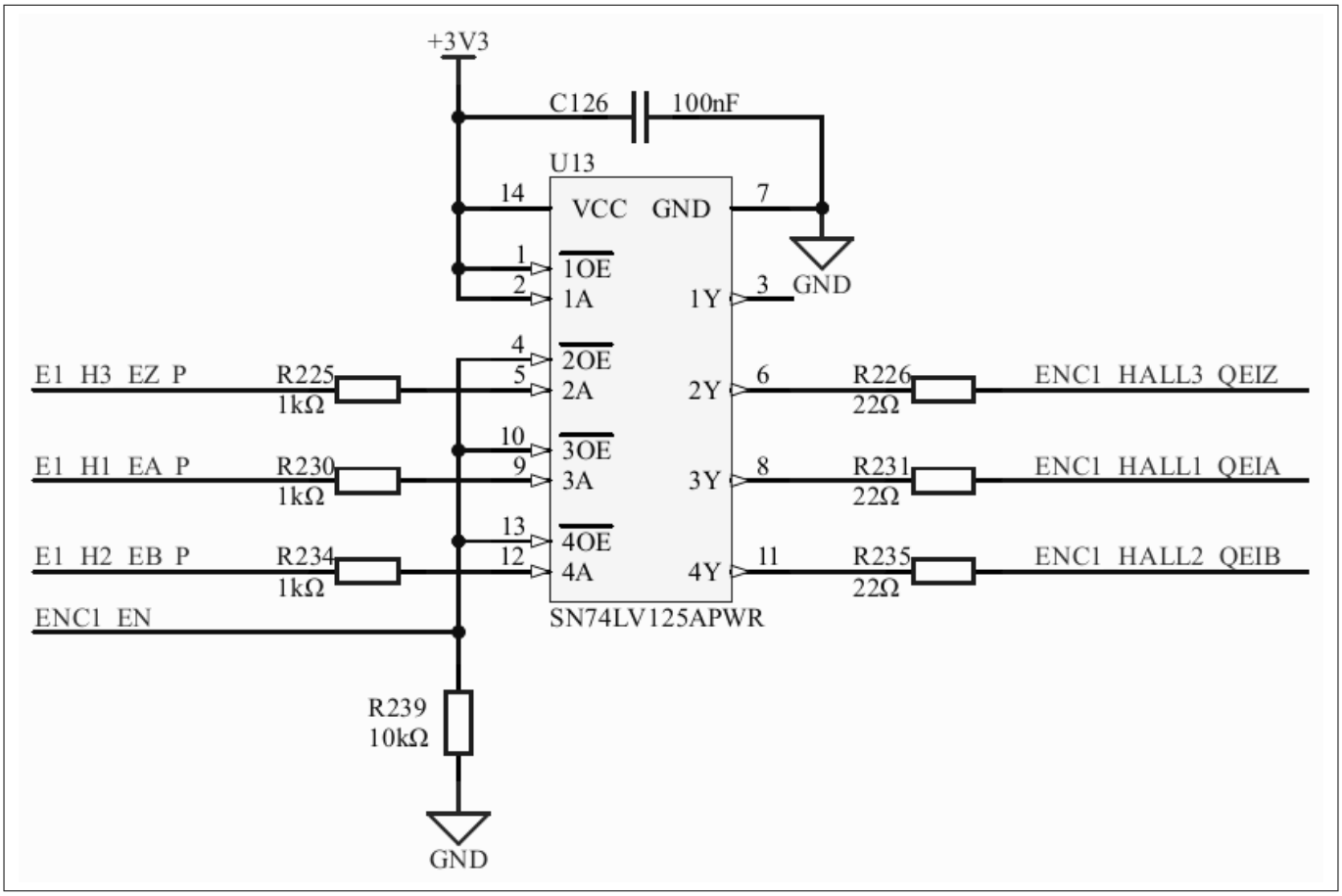


Figure 28 HALL input buffer

Differential encoders interface

When differential encoder is enabled, inputs are passed to differential line receiver with 3-state outputs. When differential encoder is disabled, outputs from differential line receiver are in High-Z state.

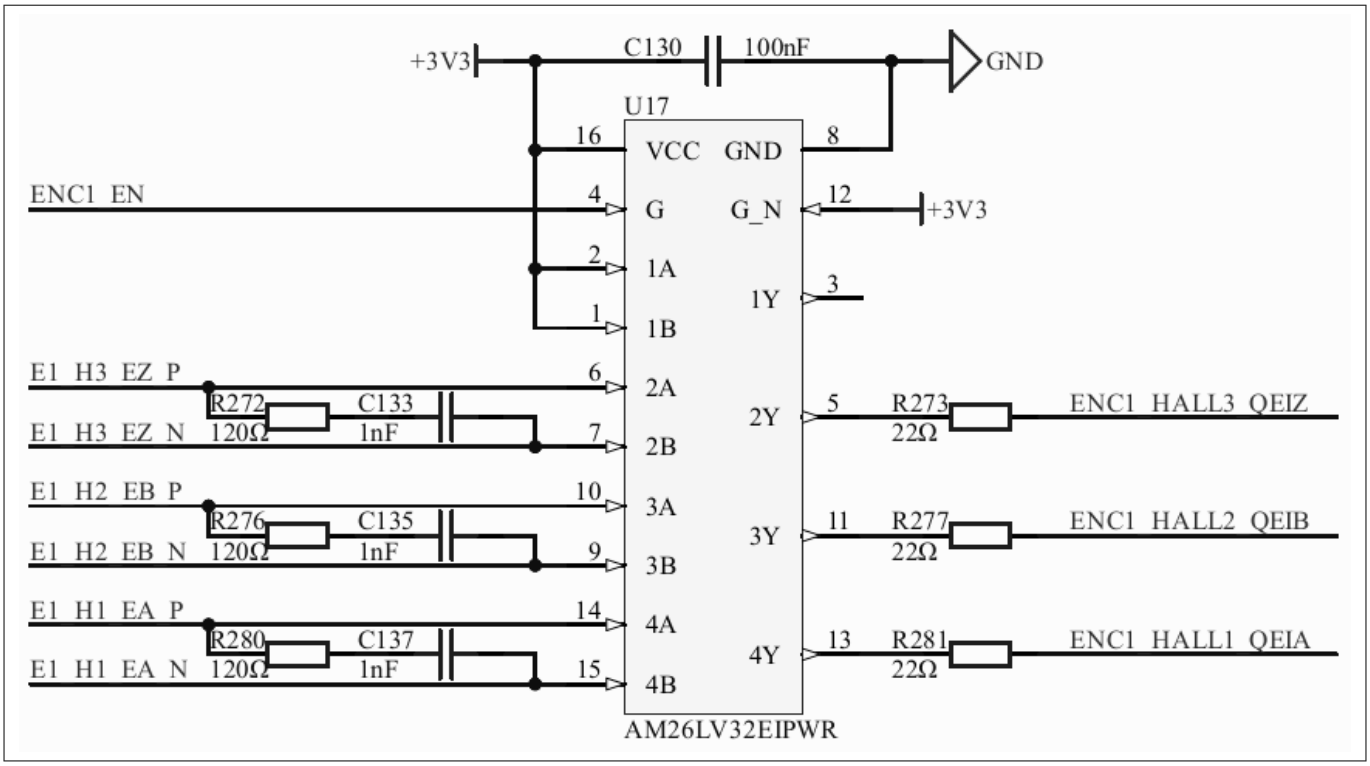


Figure 29 Differential input

Encoder enable config switch

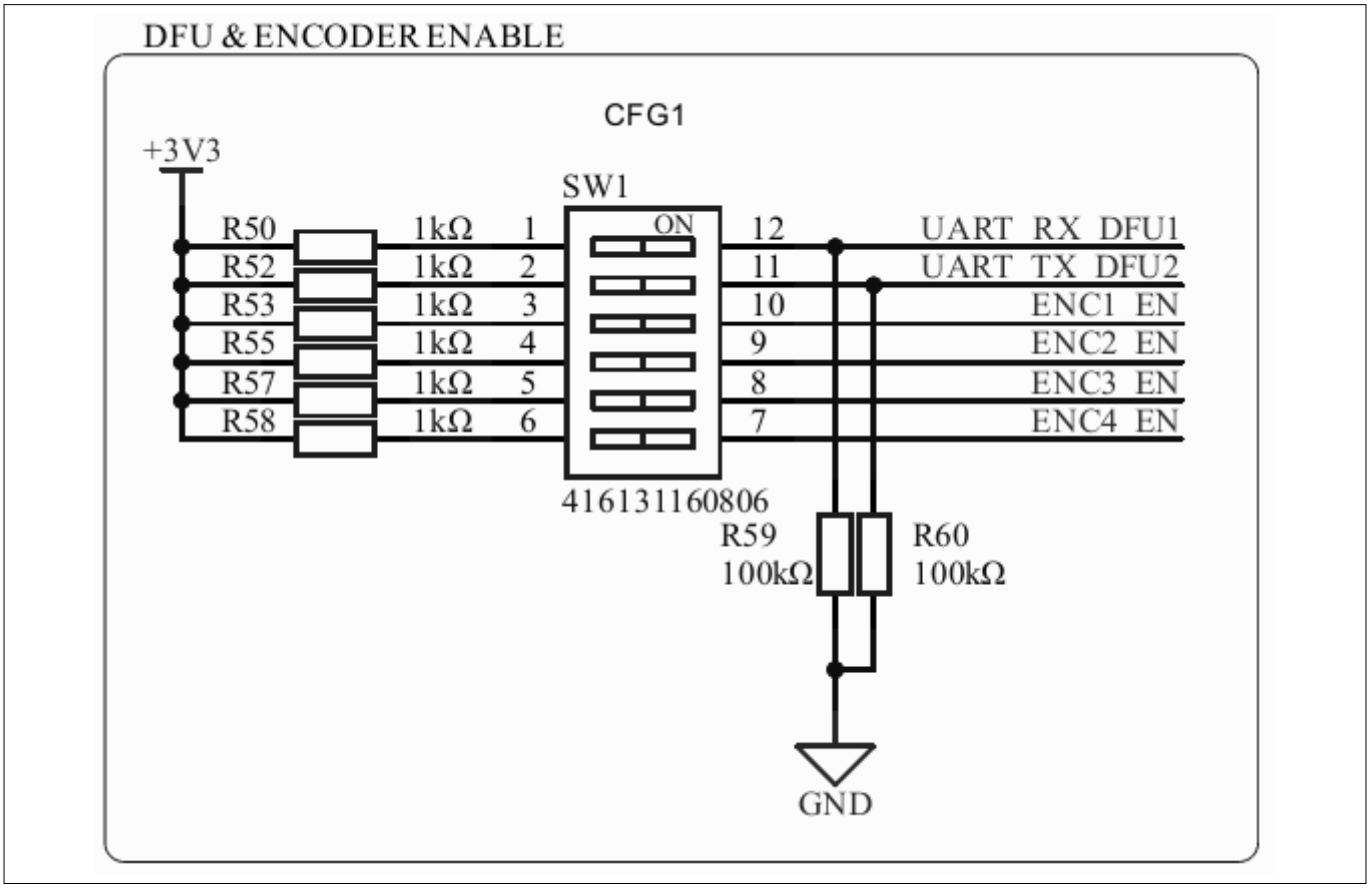


Figure 30 DFU & encoder config switch

Table 12 CFG1 switch positions

Function (Net name)	Position	State	Description	PSC3 pin
ENC1_EN	3-10	ON	Encoder 1 enabled, HALL1 disabled	P4.7
ENC2_EN	4-9	ON	Encoder 2 enabled, HALL2 disabled	-
ENC3_EN	5-8	ON	Encoder 3 enabled, HALL3 disabled	-
ENC4_EN	6-7	ON	Encoder 4 enabled, HALL4 disabled	-

Default state for encoder enable **CFG1** switch positions is OFF.

3.11 User interface

Reset switch

Reset switch (**RESET**) is connected to the *XRES* pin of **PSC3M/P6** device and used to reset the device.

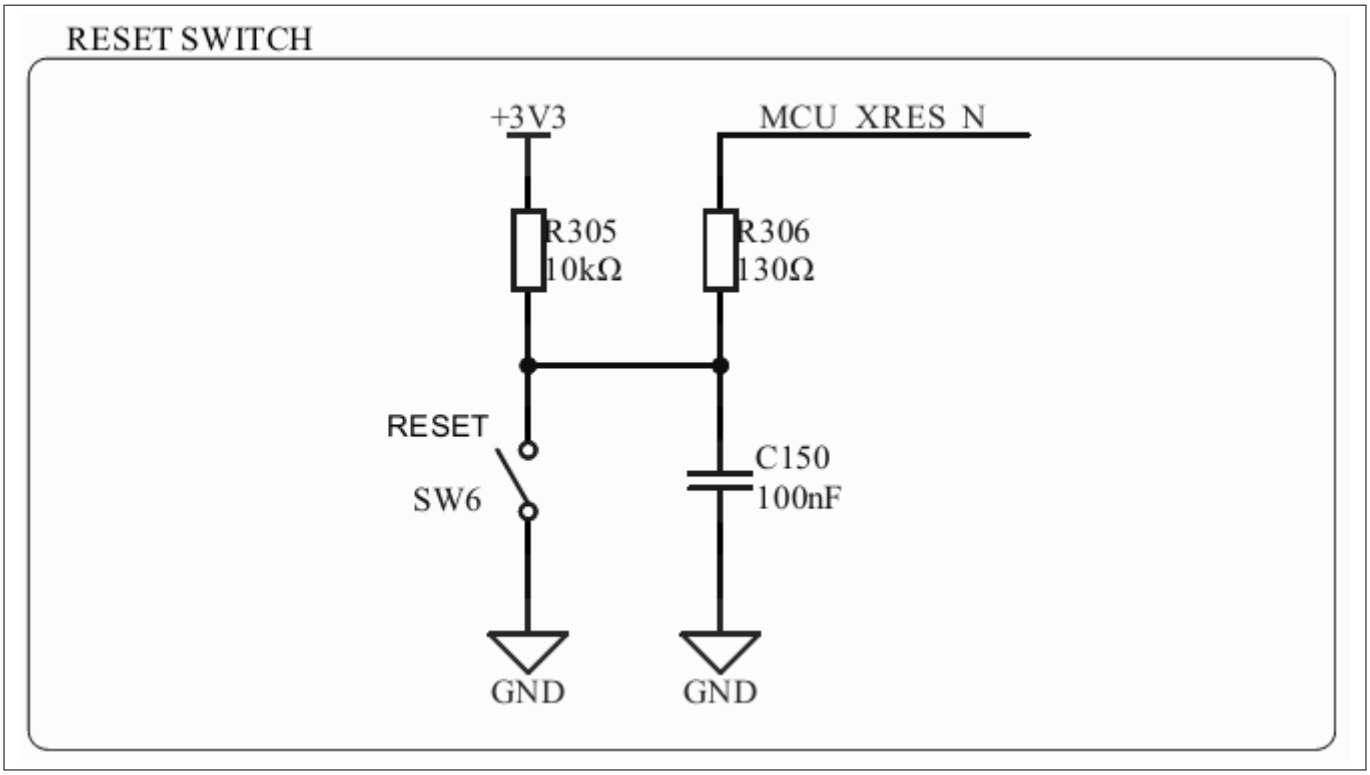


Figure 31 Reset switch

Switches

The board includes the following user switches:

- User switch **SW1** connected to pin *P4.6*
- User switch **SW2** connected to pin *P5.3*

All switches are in the ACTIVE LOW configuration and short to GND when pressed.

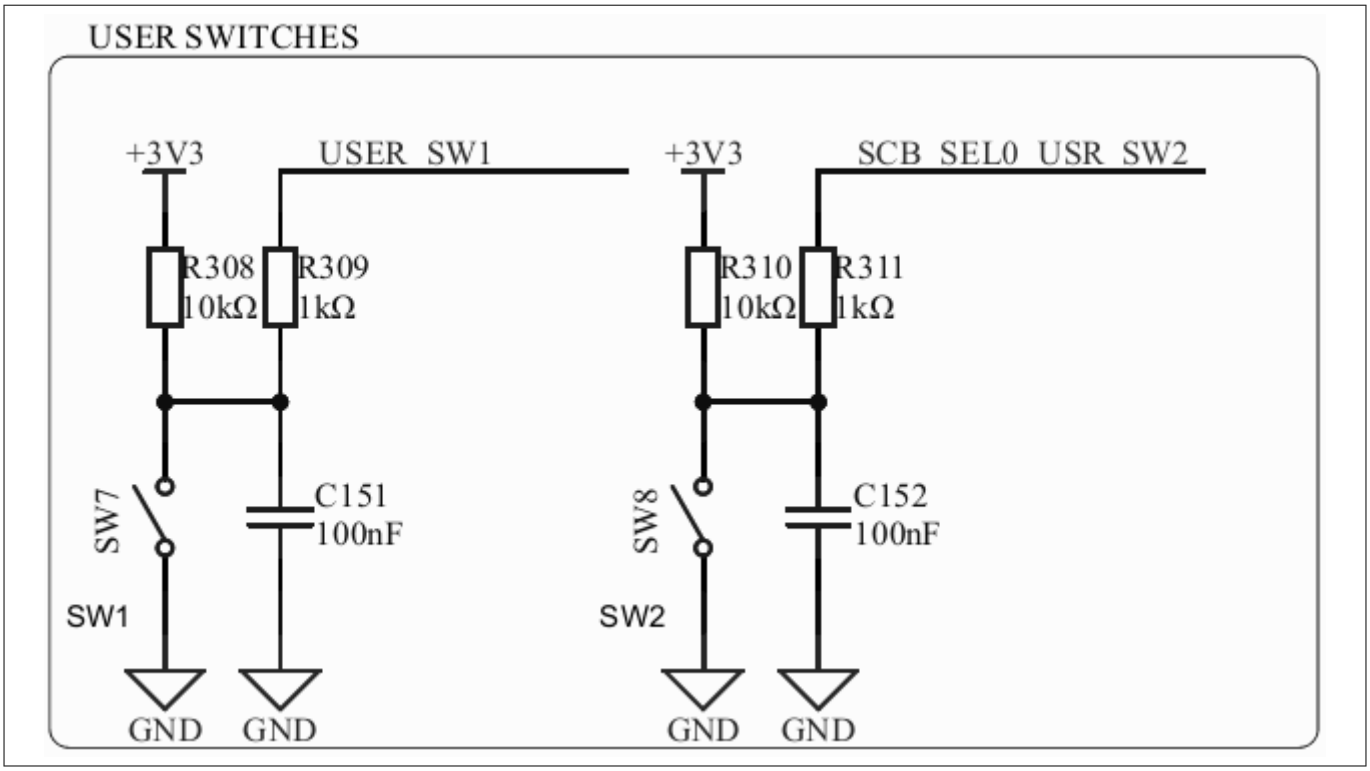


Figure 32 User switches

LEDs

The board includes two user controllable LEDs:

- User **LED1** (GREEN) connected to pin *P2.0*
- User **LED2** (YELLOW) connected to pin *P2.1*

All LEDs are in the ACTIVE LOW configuration.

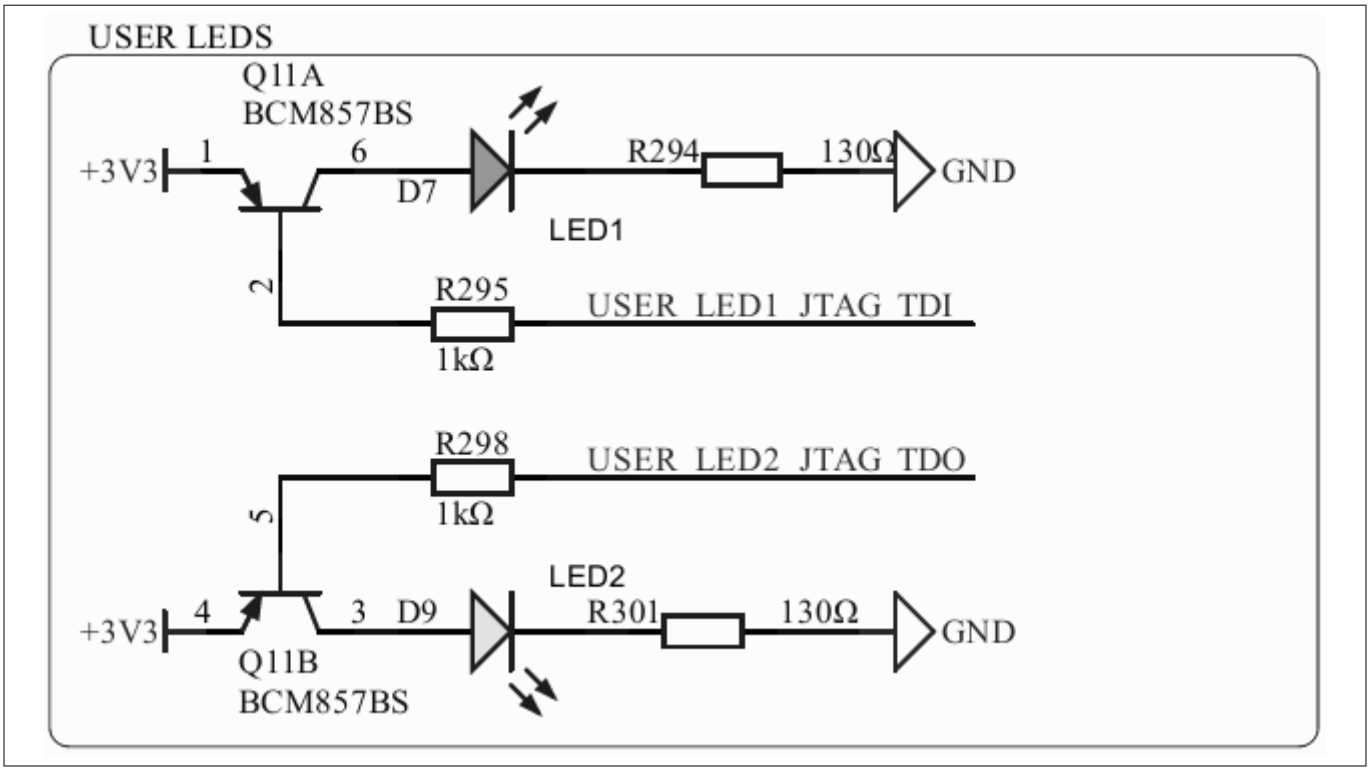


Figure 33 User LEDs

Potentiometers

The board includes two user potentiometers:

- User potentiometer **POT1** connected to pin *P8.4*
- User potentiometer **POT2** connected to pin *P8.5*

ADC output readings will increase when the potentiometer is rotated in a clockwise direction and conversely.

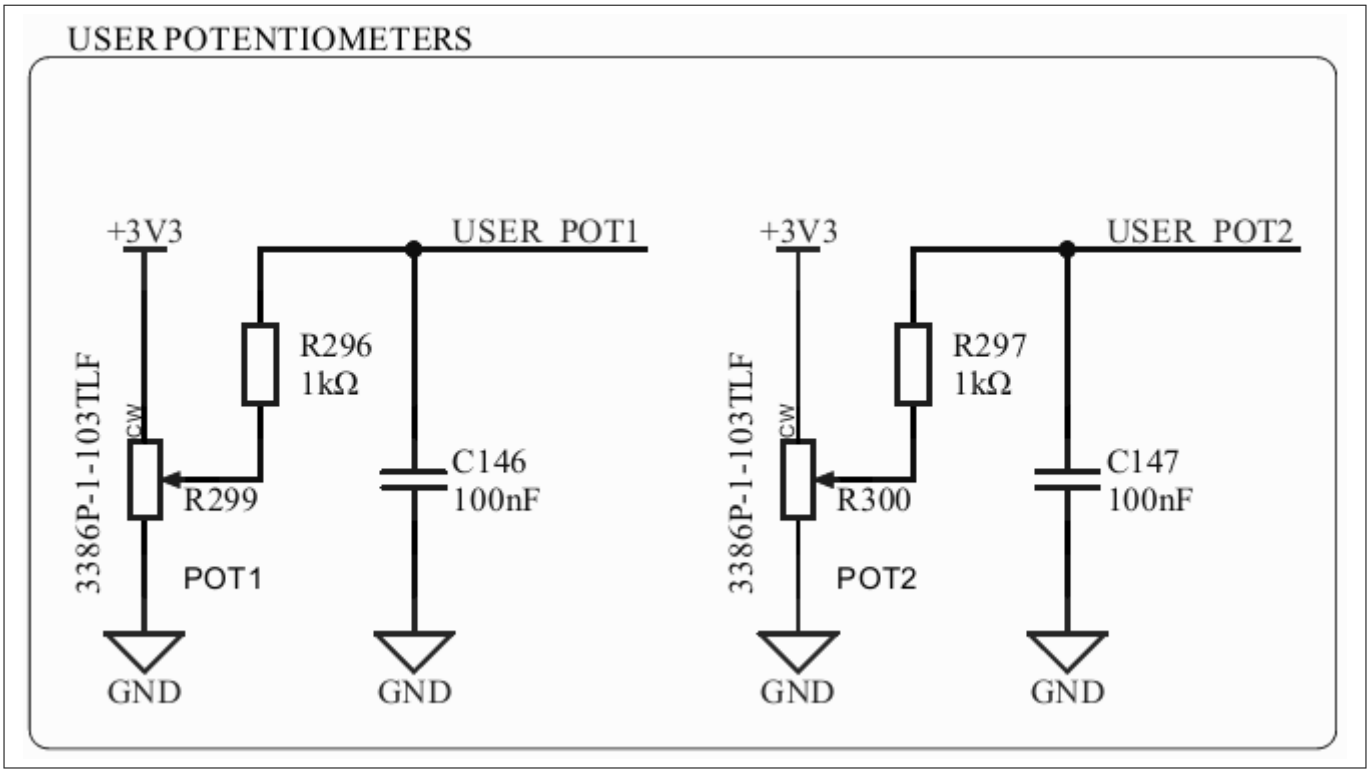


Figure 34 User potentiometers

USB-FS interface

The board features a dedicated USB 2.0 Full-Speed (12 Mbps) interface via a USB Type-C connector, which is connected directly to the internal USB PHY of PSC3M/P6 MCU. This direct hardware connection allows the MCU to operate in USB device mode, enabling the development of diverse applications.

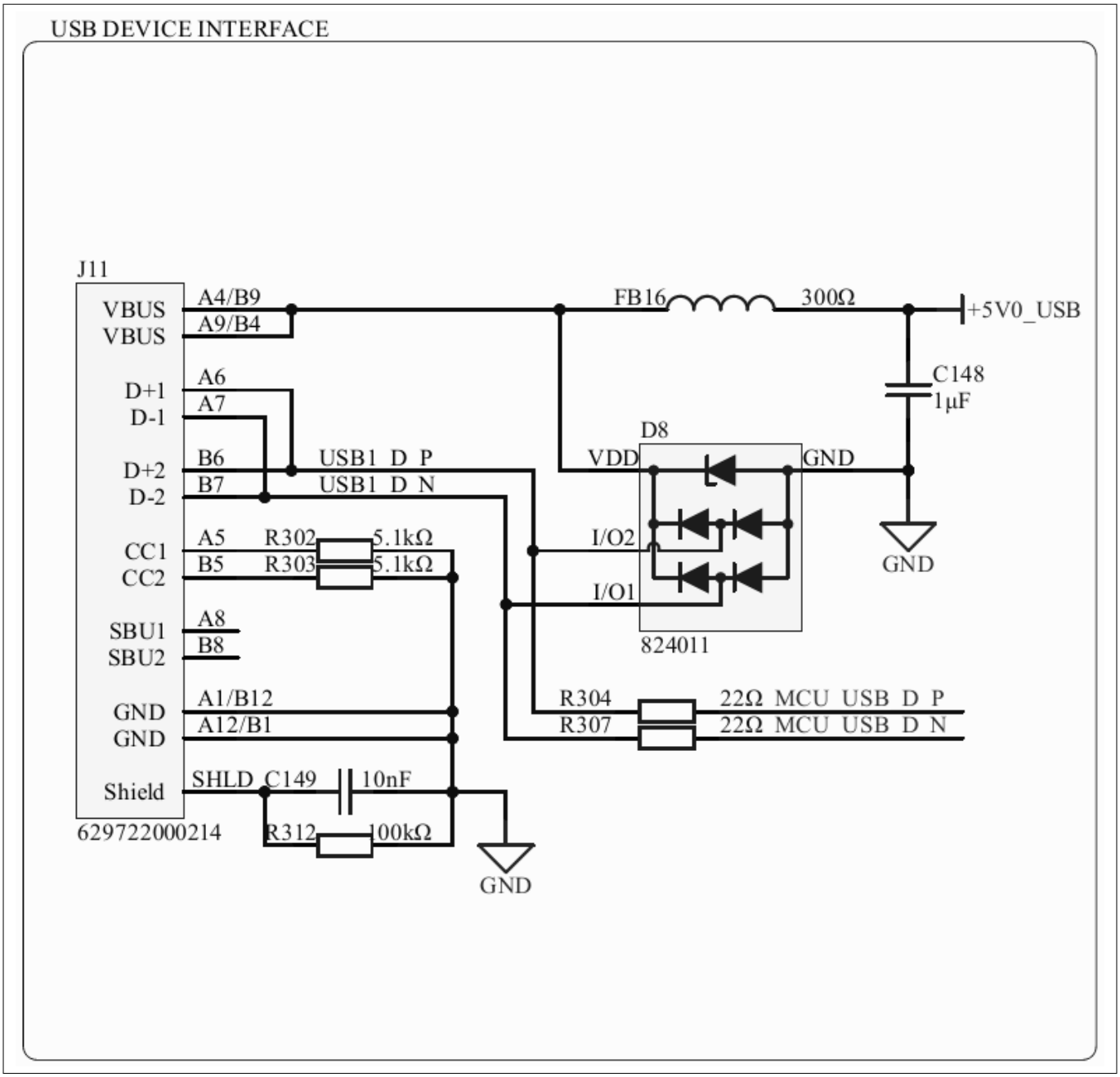


Figure 35 User USB-FS interface

Isolated CAN interface

The board features an isolated high-speed CAN transceiver, TLE9251V, operating as an interface between the CAN controller and the physical bus medium. A high-speed CAN network is a two-wire, differential network that allows data transmission rates up to 5 Mbps.

The CANH and CANL pins are the interfaces to the CAN bus; both pins operate as an input and an output

The RxD and TxD pins are the interfaces to the MCU:

- RxD pin is connected to pin *P6.2*
- TxD pin is connected to pin *P6.3*

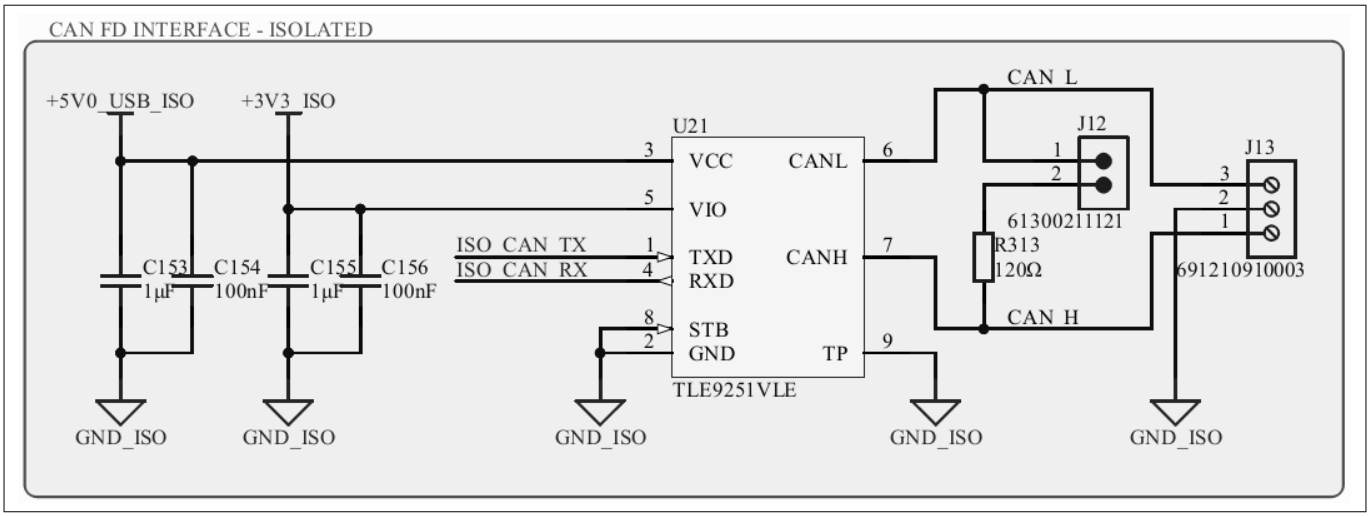


Figure 36 Isolated CAN interface

3.12 Expansion headers

The KIT_PSC3M6_CC2 is provided with header interfaces to enable direct access to PSOC™ Control C3 MCU pins.

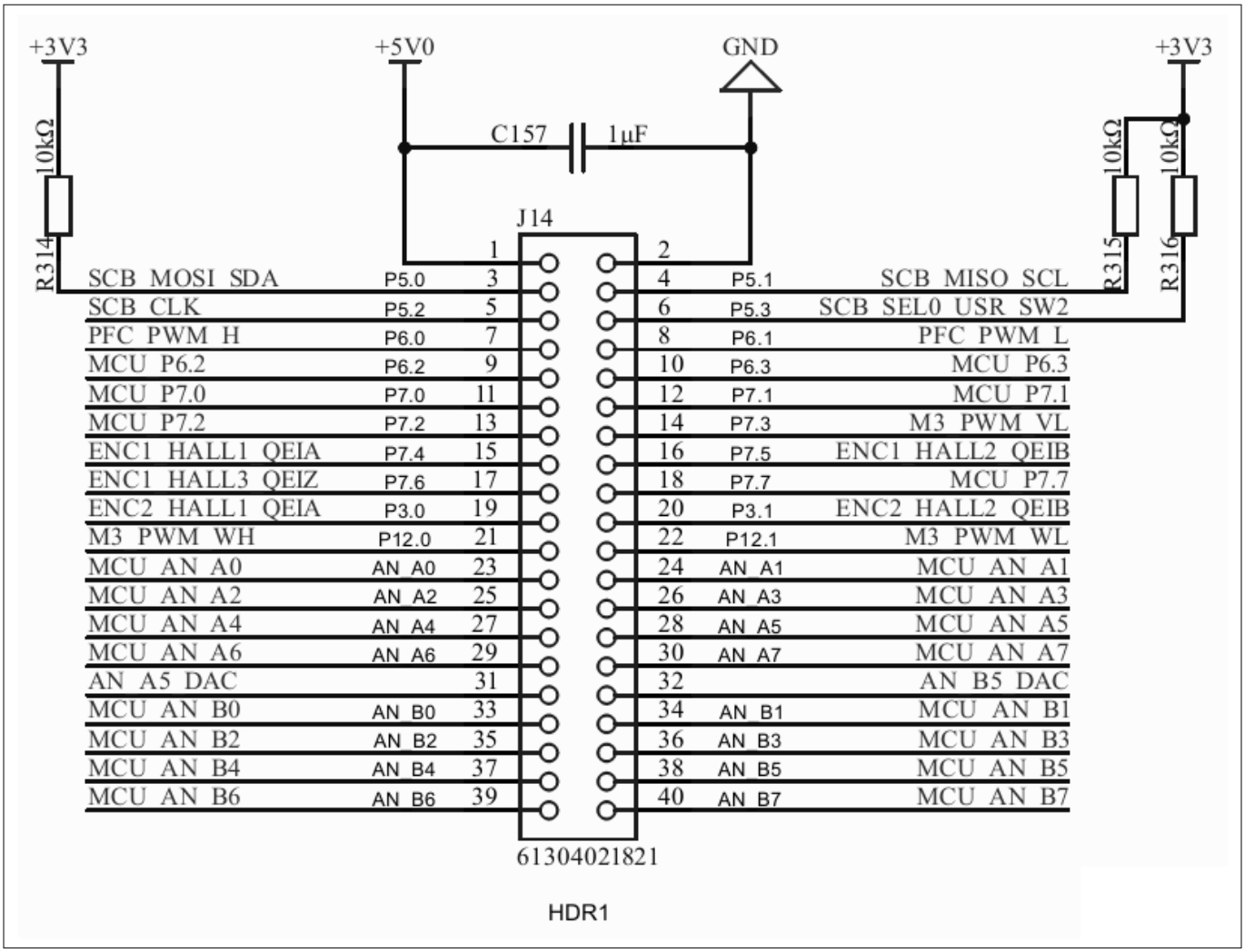


Figure 37 Expansion header 1 pin-out

Table 13 HDR1 header pin-out details

Function (Net name)	PSC3 pin	HDR1 pin	HDR1 pin	PSC3 pin	Function (Net name)
+5V0	+5V	**1**	**2**	GND	Ground
SCB_MOSI_SDA	P5.0	**3**	**4**	P5.1	SCB_MISO_SCL
SCB_CLK	P5.2	**5**	**6**	P5.3	SCB_SEL0_USR_SW2
PFC_PWM_H	P6.0	**7**	**8**	P6.1	PFC_PWM_L
MCU_P6.2	P6.2	**9**	**10**	P6.3	MCU_P6.3
MCU_P7.0	P7.0	**11**	**12**	P7.1	MCU_P7.1
MCU_P7.2	P7.2	**13**	**14**	P7.3	M3_PWM_VL
ENC1_HALL1_QEIA	P7.4	**15**	**16**	P7.5	ENC1_HALL2_QEIB
ENC1_HALL3_QEIZ	P7.6	**17**	**18**	P7.7	MCU_P7.7
ENC2_HALL1_QEIA	P3.0	**19**	**20**	P3.1	ENC2_HALL2_QEIB
M3_PWM_WH	P12.0	**21**	**22**	P12.1	M3_PWM_WL
MCU_AN_A0	AN_A0	**23**	**24**	AN_A1	MCU_AN_A1
MCU_AN_A2	AN_A2	**25**	**26**	AN_A3	MCU_AN_A3
MCU_AN_A4	AN_A4	**27**	**28**	AN_A5	MCU_AN_A5
MCU_AN_A6	AN_A6	**29**	**30**	AN_A7	MCU_AN_A7
AN_A5_DAC	AN_A5 (DAC)	**31**	**32**	AN_B5 (DAC)	AN_B5_DAC
MCU_AN_B0	AN_B0	**33**	**34**	AN_B1	MCU_AN_B1
MCU_AN_B2	AN_B2	**35**	**36**	AN_B3	MCU_AN_B3
MCU_AN_B4	AN_B4	**27**	**38**	AN_B5	MCU_AN_B5
MCU_AN_B6	AN_B6	**39**	**40**	AN_B7	MCU_AN_B7

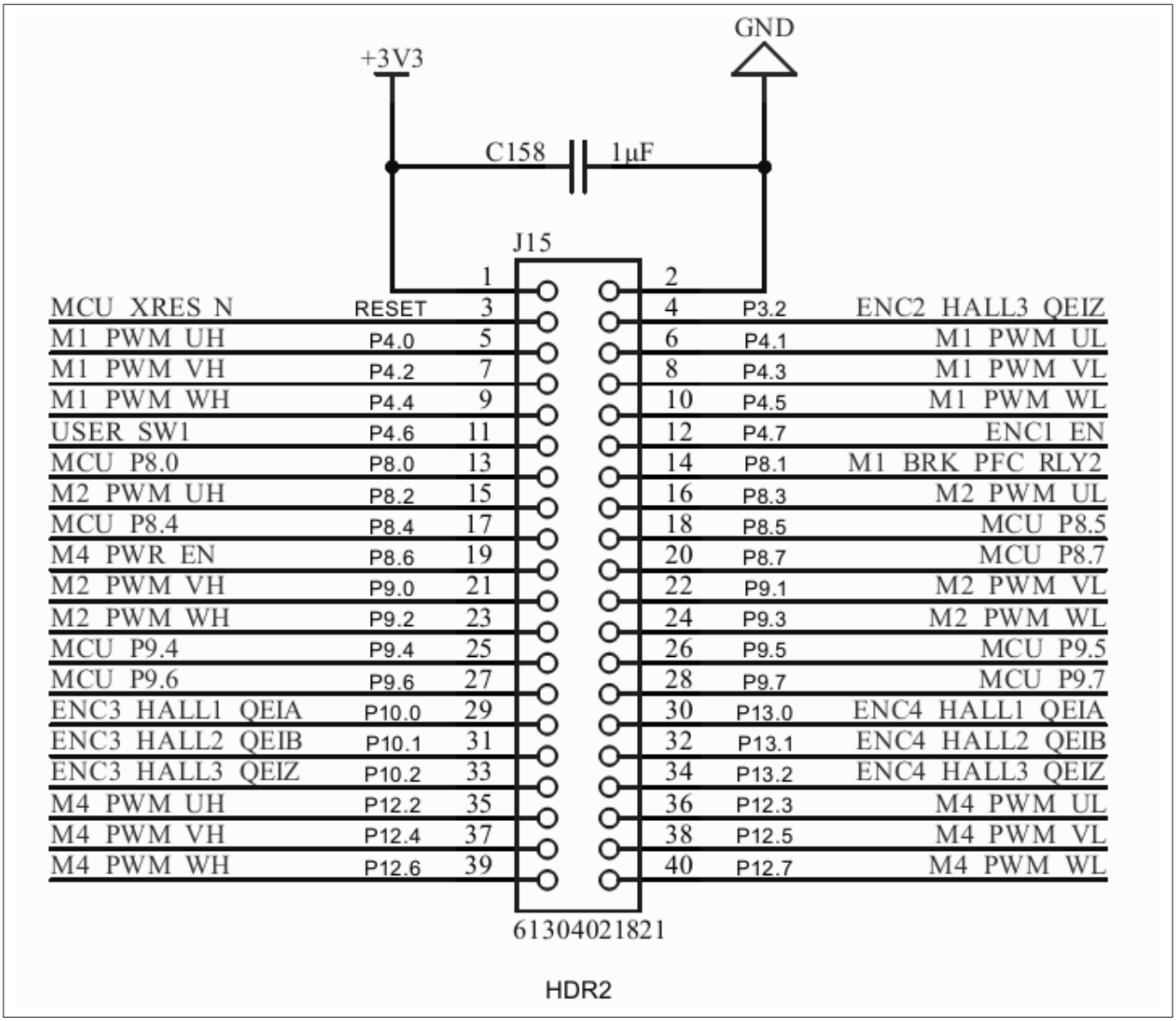


Figure 38 Expansion header 2 pin-out

Table 14 HDR2 header pin-out details

Function (Net name)	PSC3 pin	HDR1 pin	HDR1 pin	PSC3 pin	Function (Net name)
+3V3	+3.3V	**1**	**2**	GND	Ground
MCU_XRES_N	RESET	**3**	**4**	P3.2	ENC2_HALL1_QEIA
M1_PWM_UH	P4.0	**5**	**6**	P4.1	M1_PWM_UL
M1_PWM_VH	P4.2	**7**	**8**	P4.3	M1_PWM_VL
M1_PWM_WH	P4.4	**9**	**10**	P4.5	M1_PWM_WL
USER_SW1	P4.6	**11**	**12**	P4.7	ENC1_EN
MCU_P8.0	P8.0	**13**	**14**	P8.1	M1_BRK_PFC_RLY2
M2_PWM_UH	P8.2	**15**	**16**	P8.3	M2_PWM_UL

(table continues...)

Table 14 (continued) HDR2 header pin-out details

Function (Net name)	PSC3 pin	HDR1 pin	HDR1 pin	PSC3 pin	Function (Net name)
MCU_P8.4	P8.4	**17**	**18**	P8.5	MCU_P8.5
M4_PWR_EN	P8.6	**19**	**20**	P8.7	MCU_P8.7
M2_PWM_VH	P9.0	**21**	**22**	P9.1	M2_PWM_VL
M2_PWM_WH	P9.2	**23**	**24**	P9.3	M2_PWM_WL
MCU_P9.4	P9.4	**25**	**26**	P9.5	MCU_P9.5
MCU_P9.6	P9.6	**27**	**28**	P9.7	MCU_P9.7
ENC3_HALL1_QEIA	P10.0	**29**	**30**	P13.0	ENC4_HALL1_QEIA
ENC3_HALL2_QEIB	P10.1	**31**	**32**	P13.1	ENC4_HALL2_QEIB
ENC3_HALL3_QEIZ	P10.2	**33**	**34**	P13.2	ENC4_HALL3_QEIZ
M4_PWM_UH	P12.2	**35**	**36**	P12.3	M1_PWM_UL
M4_PWM_VH	P12.4	**27**	**38**	P12.5	M1_PWM_VL
M4_PWM_WH	P12.6	**39**	**40**	P12.7	M1_PWM_WL

4 Production data

The KIT_PSC3M6_CC2 PSOC™ Control C3M6 Motor Drive Control Evaluation Kit is designed with Altium Designer™. The complete PCB design data, schematics, layout, and BOM for this board can be downloaded from the kit webpage, Design resources tab..

Revision history

Document revision	Date	Description of changes
**	2026-08-21	Initial release.

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