

am^u AS7160

Datasheet

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Table of contents

1	General description	4
1.1	Key benefits & features.....	5
1.2	Applications	5
1.3	Block diagram	6
2	Ordering information	7
3	Pin assignment	7
3.1	Pin diagram.....	7
3.2	Pin description	8
4	Absolute maximum ratings	10
5	Electrical characteristics.....	12
5.1	Power consumption	14
6	Typical operating characteristics	16
7	Functional description.....	18
7.1	LED driver	18
7.2	Photodiode inputs	21
7.3	ADC1 and ADC2.....	22
7.4	Sequencer	26
7.5	Measurement sample structure	26
7.6	FIFO description	42
7.7	Communication interfaces	45
7.8	Startup information	52
7.9	Standby mode.....	53
8	Register description	55
8.1	Register overview	55
8.2	OTP	60
8.3	Power.....	61
8.4	Control	68
8.5	ADC modulator	71

8.6	LED driver	76
8.7	Photodiodes	92
8.8	SINC filter	106
8.9	Photodiode offset.....	108
8.10	Advanced automatic offset control.....	113
8.11	Post processing	115
8.12	Sequencer	119
8.13	FIFO.....	130
8.14	Miscellaneous	131
9	Application information.....	139
9.1	Schematic	139
9.2	External components	140
10	Package drawings & markings	141
11	Tape & reel information	143
12	Revision information	144
13	Legal information	145

AS7160 Precision analog frontent IC for optical force sensing, proximity detection and customizable spectral analytics

1 General description

The AS7160 is a low noise, high dynamic range proximity detection analog front end that has been optimized for optical force sensing for consumer market applications.

The data acquisition system provides up to eight LEDs and eight photodiode inputs. The LEDs are controlled with two high current 8-bit programmable LED drivers current sinks. Each current sink support up to four different operating current ranges for best tunability of the LED light intensity. Additionally, a special laser safety support system can be enabled, which offers the possibility to use VCSEL die as a light source.

The photodiodes can be read out synchronously with two 20-bit ADCs each equipped with a 12-bit current DAC for ambient light suppression. The on chip advanced automatic offset control (AAOC) enables the system to adjust the DAC current towards the ambient light situation before the actual measurement starts and minimizes data loss due to analog saturation caused by ambient light influences.

The device is available in a 42-ball wafer-level chip scale package (WLCSP) with dimensions 2.82 mm x 2.55 mm and operates over the temperature range -40 °C to 85 °C.

1.1 Key benefits & features

The benefits and features of AS7160 are listed below:

Table 1: Added value of using AS7160

Benefits	Features
Highest measurement resolution OFS (5µm)	• 20-bit true current input analog to digital converter • High Signal to Noise ratio (90dB) • On chip averaging support
Simultaneous proximity and force measurement	State machine controlled automatic measurement range reconfiguration
Highly flexible LED/photodiode configuration	Up to 8 LED output pins and 8 photodiode input pins.
Allows the smallest application size	Small Wafer-Level-Chip-Scale-Package (WLCSP)
Long operating time	A hardware sequencer to offload the processor with an adjustable LED driver with current control.
Low power operating mode	Automatically controlled standby mode function
No influence on ambient light influences	Integrated Advanced Automatic Offset Compensation function

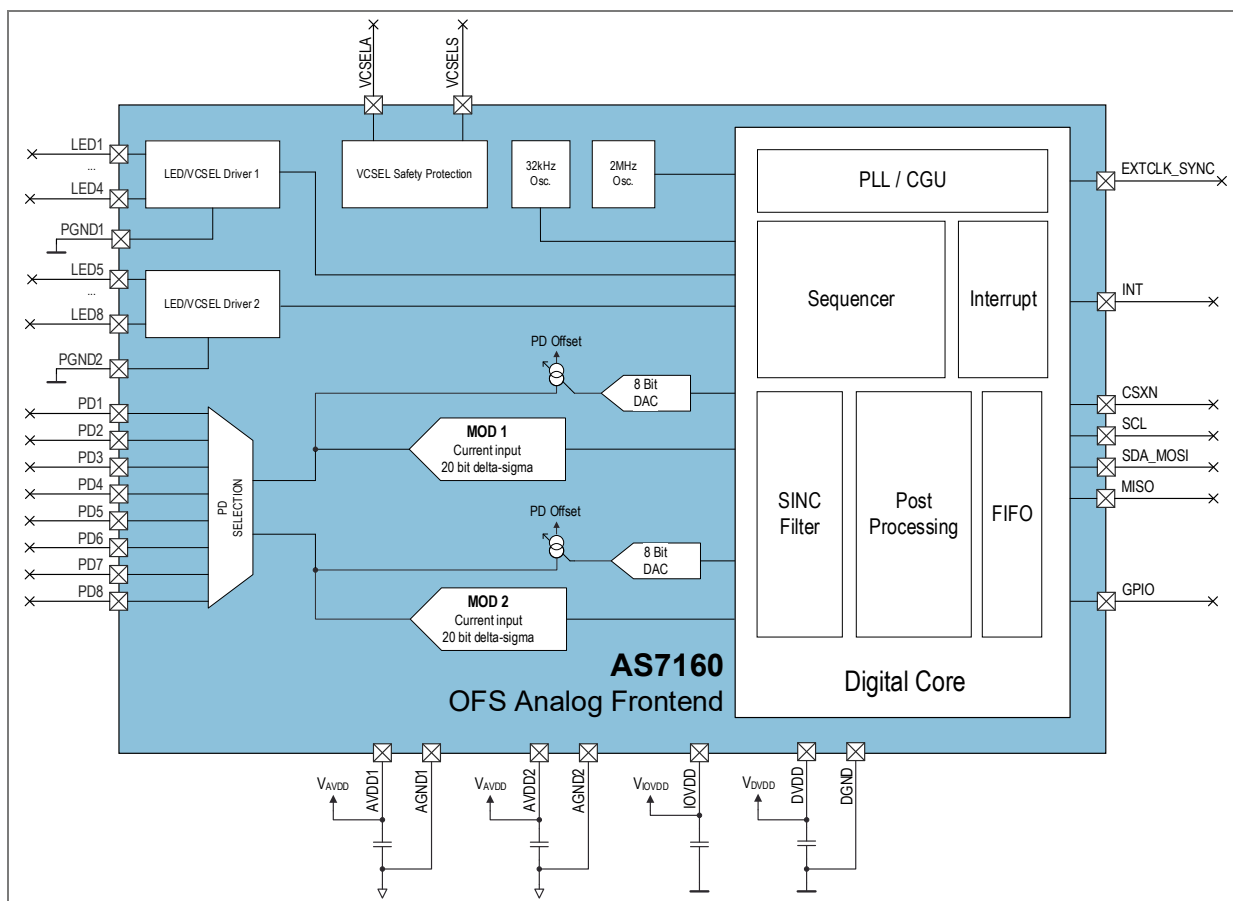
1.2 Applications

- Mobile phones
- Tablets
- Smart watch
- Industrial Automation
- Home & Building Automation
- Medical & Digital Diagnostics Devices
- Appliances & Power Tools
- Robotics

1.3 Block diagram

The functional blocks of this device are shown below:

Figure 1: Functional blocks of AS7160



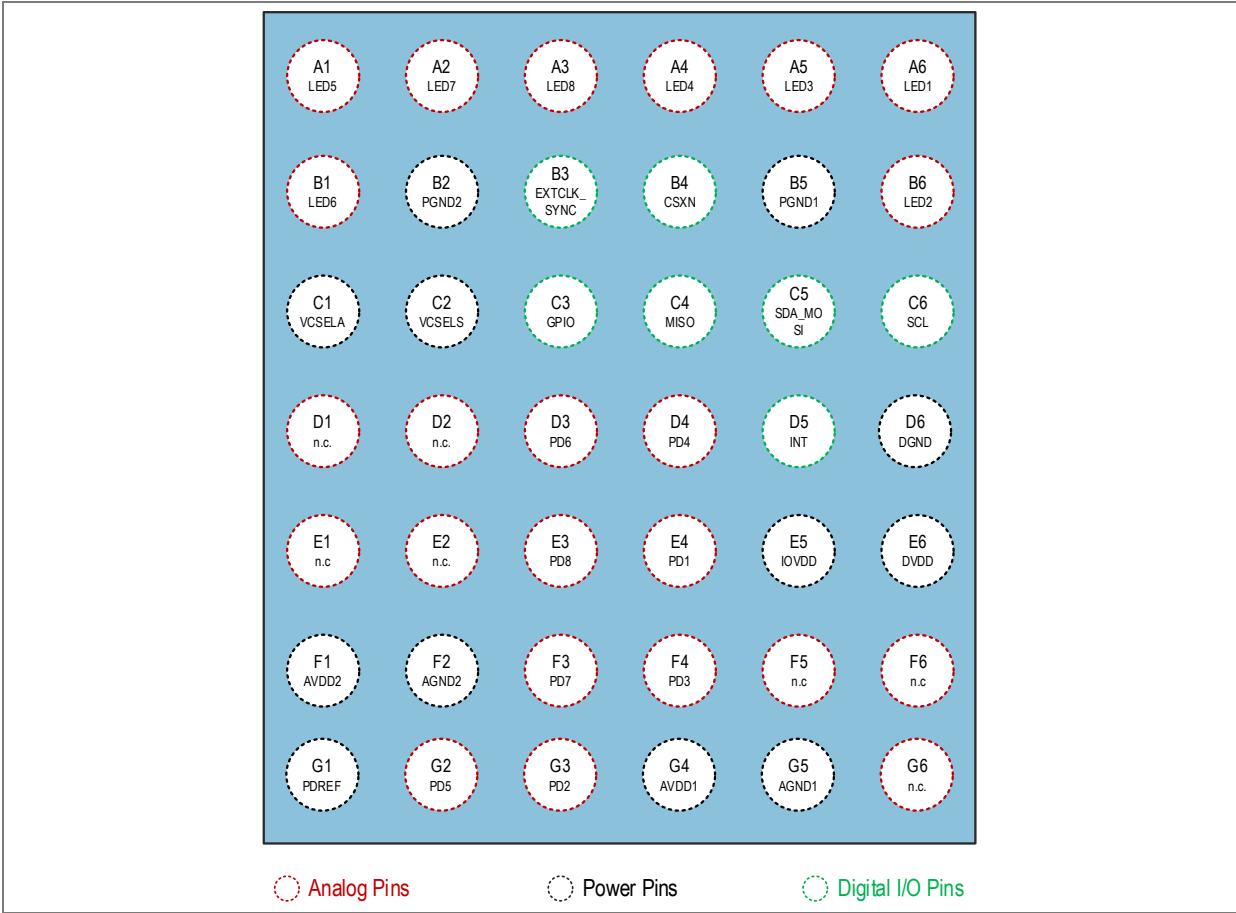
2 Ordering information

Ordering code	Package	Marking	Delivery form	Delivery quantity
Q65115A0138	WLCSP	AS7160	Tape & reel	10000 pcs / reel

3 Pin assignment

3.1 Pin diagram

Figure 2: Pin diagram of AS7160 (Top View)



3.2 Pin description

Table 2: Pin description of AS7160

Pin number	Pin name	Pin type ⁽¹⁾	Description
A1	LED5	AI	LED input number 5 which is connected internally to LED driver 2. In case input is not used in application pin can be left unconnected.
A2	LED7	AI	LED input number 7 which is connected internally to LED driver 2. In case input is not used in application pin can be left unconnected.
A3	LED8	AI	LED input number 8 which is connected internally to LED driver 2. In case input is not used in application pin can be left unconnected.
A4	LED4	AI	LED input number 4 which is connected internally to LED driver 1. In case input is not used in application pin can be left unconnected.
A5	LED3	AI	LED input number 3 which is connected internally to LED driver 1. In case input is not used in application pin can be left unconnected.
A6	LED1	AI	LED input number 1 which is connected internally to LED driver 1. In case input is not used in application pin can be left unconnected.
B1	LED6	AI	LED input number 6 which is connected internally to LED driver 2. In case input is not used in application pin can be left unconnected.
B2	PGND2	G	LED driver 2 power ground pin for LED inputs LED5, LED6, LED7 and LED8.
B3	EXTCLK_SYNC	DI	External clock and synchronization input. This digital input can be used to feed in an external 2 MHz clock. Furthermore, pin can also be used for external host synchronization to trigger a measurement start based on signal level of the EXTCLK_SYNC pin.
B4	CSXN	DI	SPI chip select input pin. In case I²C interface is used as device host communication interface, this pin requires an external pull up resistor.
B5	PGND1	G	LED driver 1 power ground pin for LED inputs LED1, LED2, LED3 and LED4.
B6	LED2	AO	LED input number 2 which is connected internally to LED driver 1. In case input is not used in application pin can be left unconnected.
C1	VCSELA	AO	VCSEL diode anodes
C2	VCSELS	P	This is the power supply input pin for the LED driver and VCSEL circuit. Pin must always be connected to LED supply voltage and must not be left unconnected.
C3	GPIO	DO/DI	Digital general purpose I/O which allows to assign various functions.
C4	MISO	DO	SPI data output pin
C5	SDA_MOSI	DO/DI	Data for I ² C interface/SPI data in
C6	SCL	DI	Clock input for I ² C/SPI interface
D1	n.c.	-	Not connected. Leave this pin unconnected
D2	n.c.	-	Not connected. Leave this pin unconnected
D3	PD6	AI	Photodiode input number 6

Pin number	Pin name	Pin type ⁽¹⁾	Description
D4	PD4	AI	Photodiode input number 4
D5	INT	DO	Digital interrupt push/pull output pin. The polarity of the interrupt pin acting as active high or active low can be programmed via control register.
D6	DGND	G	Digital ground
E1	n.c.	-	Not connected. Leave this pin unconnected
E2	n.c.	-	Not connected. Leave this pin unconnected
E3	PD8	AI	Photodiode input number 8
E4	PD1	AI	Photodiode input number 1
E5	IOVDD	P	This is the digital I/O supply pin. This supply is separated from the digital core supply of AS7160 and can for example be connected to a 1.2 V supply voltage to enable lower I ² C or SPI interface voltages to eliminate the need of external level shifters.
E6	DVDD	P	Positive digital supply terminal of AS7160 which needs to be connected to a 1.8 V power supply.
F1	AVDD2	P	Positive analog supply terminal 2 which supplies all analog blocks of the device. Needs to be connected to a low noise 1.8V power supply.
F2	AGND2	G	Analog ground
F3	PD7	AI	Photodiode input number 7
F4	PD3	AI	Photodiode input number 3
F5	n.c.	-	Not connected. Leave this pin unconnected
F6	n.c.	-	Not connected. Leave this pin unconnected
G1	PDREF	AO	Reference potential for photodiodes
G2	PD5	AI	Photodiode input number 5
G3	PD2	AI	Photodiode input number 2
G4	AVDD1	P	Positive analog supply terminal 1 which supplies all analog blocks of the device. Needs to be connected to a low noise 1.8V power supply.
G5	AGND1	P	Analog ground
G6	n.c.	-	Not connected. Leave this pin unconnected

(1) Explanation of abbreviations:

DI Digital Input
DO Digital Output
AI Analog Input
AO Analog Output
P Power Supply
G Ground

4 Absolute maximum ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3: Absolute maximum ratings of AS7160

Symbol	Parameter	Min	Max	Unit	Comments
Electrical parameters					
V_{DVDD}	Digital supply voltage	-0.3	1.98	V	DVDD to DGND
V_{AVDD}	Analog supply voltage	-0.3	1.98	V	AVDD to AGND
V_{IOVDD}	IO supply voltage	-0.3	1.98	V	IOVDD to AGND
V_{VCSELS}	VCSELS supply voltage	-0.3	5.5	V	VCSELS to AGND
V_{VCSELA}	VCSELA pin voltage	-0.3	5.5	V	VCSELA to AGND
$V_{VCSELA-VCSELS}$	Voltage difference between pins VCSELA and VCSELS	-0.3	0.3	V	
V_{LED}	LED pin voltage	-0.3	5.5	V	LED1-LED8 to PGND1 or PGND2
$V_{IN-DIGITAL}$	Digital input pin voltage to ground	-0.3	$V_{IOVDD}+0.3\text{ V}$ max. 1.98 V	V	Applicable to pins SCL, SDA_MOSI, CSXN, GPIO and EXTCLK_SYNC
$V_{IN-ANALOG}$	Analog input pin voltage to ground	-0.3	$V_{AVDD}+0.3\text{ V}$ max. 1.98 V	V	Applicable to pins PD1, PD2, PD3, PD4, PD5, PD6, PD7 and PD8
$V_{PGND-AGND}$	Power to analog ground voltage difference	-0.3	0.3	V	
$V_{DGND-AGND}$	Digital to analog ground voltage difference	-0.3	0.3	V	
I_{LEDON}	Average LED ON current		35	mA	
I_{SCR}	Input current (latch-up immunity)		± 100	mA	JEDEC JESD78E
Electrostatic discharge					
ESD_{HBM}	Electrostatic discharge HBM		± 2	kV	JS-001-2017
ESD_{CDM}	Electrostatic discharge CDM		± 500	V	JS-002-2018

Symbol	Parameter	Min	Max	Unit	Comments
Temperature ranges and storage conditions					
T _A	Operating ambient temperature	-40	85	°C	
T _{STRG}	Storage temperature range	-40	125	°C	
T _{BODY}	Package body temperature		260	°C	IPC/JEDEC J-STD-020 ⁽¹⁾
RH _{NC}	Relative humidity (non-condensing)	5	85	%	
MSL	Moisture sensitivity level		1		According to JEDEC J-STD-020E Represents a max. floor life time of unlimited

- (1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices." The lead finish for Pb-free leaded packages is "Matte Tin" (100 % Sn).

5 Electrical characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Conditions: $T_A = 25\text{ °C}$, $V_{DVDD} = 1.8\text{ V}$, $V_{AVDD} = 1.8\text{ V}$, $V_{IOVDD} = 1.8\text{ V}$

Table 4: Electrical characteristics of AS7160

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DVDD}	Digital supply voltage		1.70	1.80	1.98	V
V_{AVDD}	Analog supply voltage		1.70	1.80	1.98	V
V_{IOVDD}	IO supply voltage		1.08	1.80	1.98	V
V_{VCSELS}	VCSELS supply voltage	Voltage must not be below V_{AVDD}	1.75		5.50	V
Photodiode inputs						
C_{PD}	Total photodiode capacitance connected to MOD1 or MOD2	0 V reverse voltage			300	pF
I_{PD}	Photocurrent input				64	μA
MOD1 & MOD2						
MOD_{DAC_OFF}	DAC offset current full-scale range for MOD1 or MOD2 (X = 1 or 2)	$MODX_IOS_FS = 0$		1		μA
		$MODX_IOS_FS = 1$		2		
		$MODX_IOS_FS = 2$		4		
		$MODX_IOS_FS = 3$		8		
		$MODX_IOS_FS = 4$		16		
		$MODX_IOS_FS = 5$		32		
		$MODX_IOS_FS = 6$		64		
		$MODX_IOS_FS = 7$		128		
MOD_{RES}	ADC resolutions of MOD1 and MOD2			20		bit

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LED driver						
LED _{RES}	LED driver resolution			8		bit
I _{RANGE1}	Allowed operating input current for LED pin 1 to 4 (X = 1 to 4)	LEDX_IRNG = 0		25		mA
		LEDX_IRNG = 1		150		
		LEDX_IRNG = 2		225		
		LEDX_IRNG = 3		300		
I _{RANGE2}	Allowed operating input current for LED pin 5 to 8 (X = 5 to 8)	LEDX_IRNG = 0		25		mA
		LEDX_IRNG = 1		150		
		LEDX_IRNG = 2		225		
		LEDX_IRNG = 3		300		
V _{Compl1}	Compliance voltage for LED pin 1 to 4 (X = 1 to 4)	LEDX_IRNG = 0		0.3		V
		LEDX_IRNG = 1		0.4		V
		LEDX_IRNG = 2		0.55		V
		LEDX_IRNG = 3		0.75		V
V _{Compl2}	Compliance voltage for LED pin 5 to 8 (X = 5 to 8)	LEDX_IRNG = 0		0.3		V
		LEDX_IRNG = 1		0.4		V
		LEDX_IRNG = 2		0.55		V
		LEDX_IRNG = 3		0.75		V
Digital inputs (SDA_MOSI, SCL, EXTCLK_SYNC, CSXN, GPIO)						
V _{IH}	Input high		V _{IOVDD} × 0.7			V
V _{IL}	Input low				V _{IOVDD} × 0.3	V
f _{EXTCLK_SYNC}	External clock frequency	Input frequency at pin EXTCLK_SYNC; Only 2 MHz or 4 MHz is supported	2		4	MHz
Digital outputs (SDA_MOSI, MISO, INT, GPIO)						
V _{OH}	Output high towards GND	Current load ≤ 6 mA	V _{IOVDD} - 0.4			V
V _{OL}	Output low towards IOVDD	Current load ≤ 6 mA			0.4	V

5.1 Power consumption

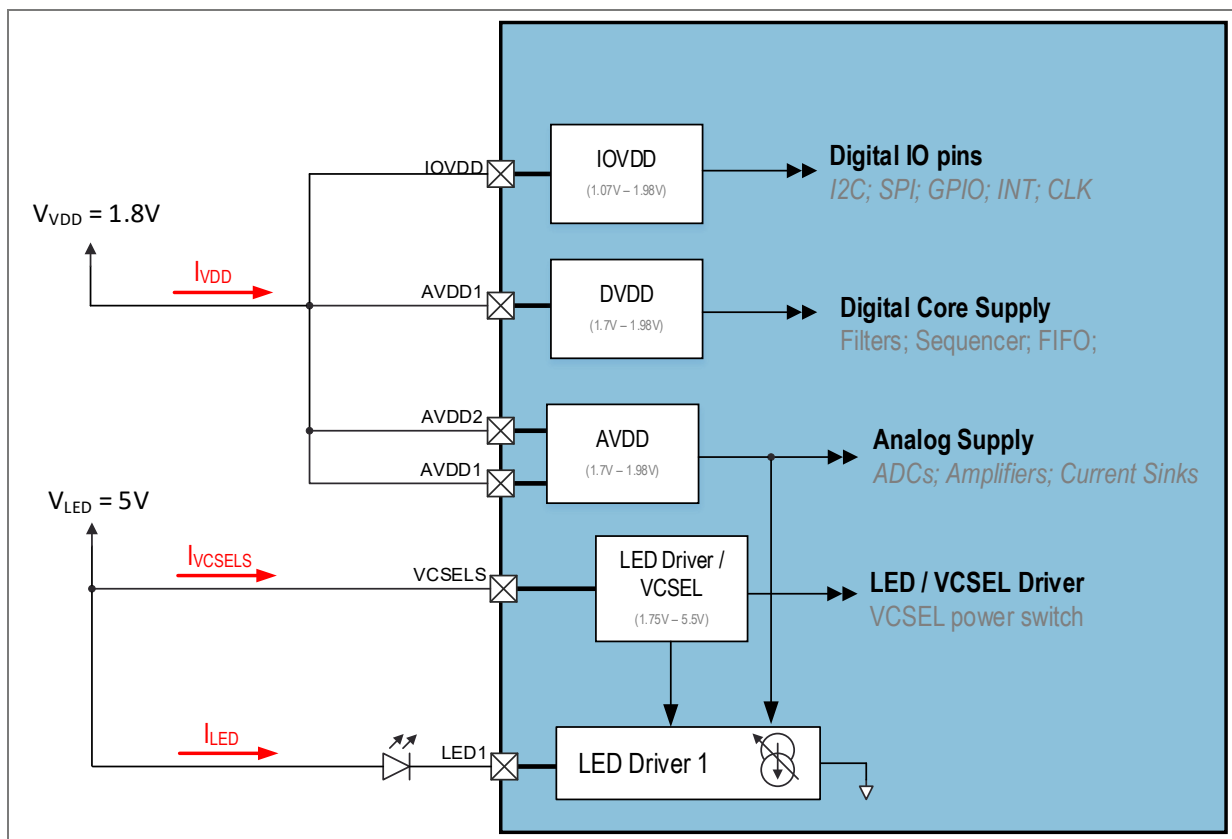
This chapter contains typical power consumption values for different device configurations and sample rates. The measurement setup is shown in Figure 3.

Conditions: $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DVDD} = 1.8\text{ V}$, $V_{AVDD} = 1.8\text{ V}$, $V_{IOVDD} = 1.8\text{ V}$; $V_{VCSELS} = 5\text{ V}$

Table 5: Typical power consumption

Symbol	Operation mode	Measurement conditions	Typ. I_{VDD}	Typ. I_{VCSELS}	Typ. I_{LED}	Unit
I_{DVDD}	Supply current in power down mode			1.80		μA
I_{AVDD}	Supply current in power down mode			0.15		μA
I_{IOVDD}	Supply current in power down mode			0.02		μA
I_{VCSELS}	Supply current in power down mode			0.01		μA
$I_{25\text{Hz}}$	Current consumption 25 Hz sample rate	Standby Mode enabled; 1 LED driver active @ 150 mA current range; 10 mA LED active current; 1 ADC active; Single Normal Measurement; no postprocessing enabled; $f_s = 25\text{ Hz}$; $f_{MOD_CLK} = 10\text{ MHz}$; $t_{INTEGRATION} = 58\text{ }\mu\text{s}$;	17	0.01	15	μA
		Standby Mode enabled; 1 LED driver active @ 150 mA current range; 10 mA LED active current; 1 ADC active; Single Normal Measurement; no postprocessing enabled; $f_s = 25\text{ Hz}$; $f_{MOD_CLK} = 10\text{ MHz}$; $t_{INTEGRATION} = 117\text{ }\mu\text{s}$;	28	0.01	29	μA

Figure 3: Block diagram of power consumption measurement setup



6 Typical operating characteristics

Figure 4: SNR vs. PD current ADC range = 64 μA ; $f_s = 200\text{ Hz}$

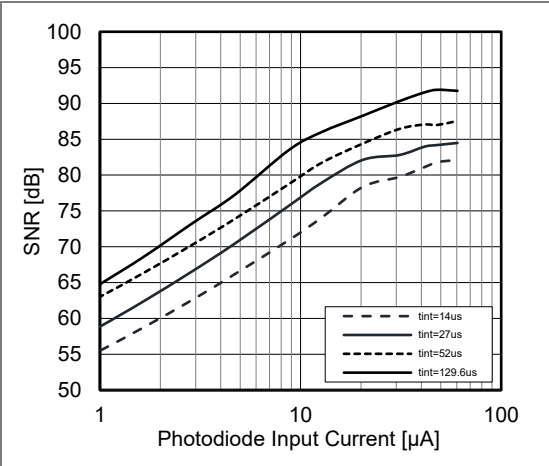


Figure 5: SNR vs. PD current; ADC range = 32 μA ; $f_s = 200\text{ Hz}$

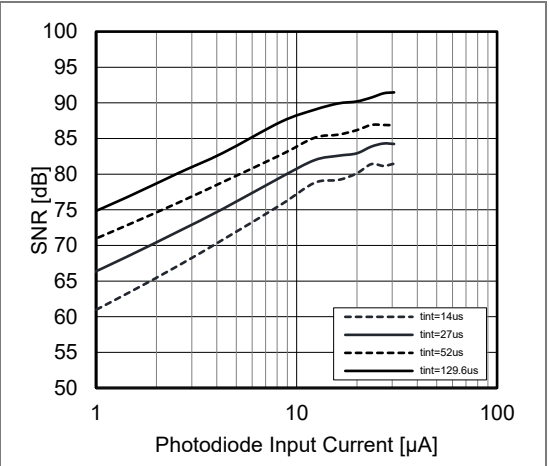


Figure 6: SNR vs. PD current 64 μA multi measurement = 16x, ADC range = 64 μA , $t_{\text{INT}}=129.1\text{ }\mu\text{s}$; $f_s = 200\text{ Hz}$

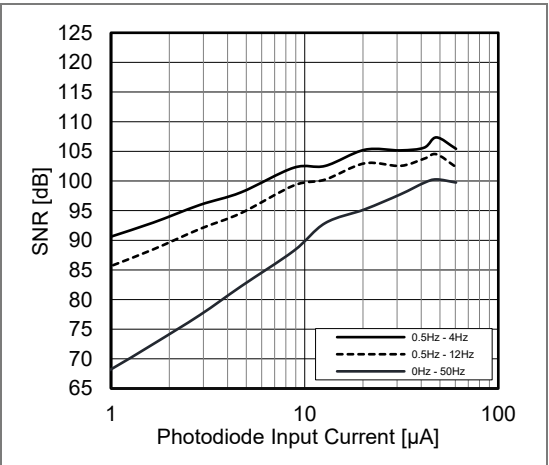


Figure 7: SNR vs. PD current 32 μA multi measurement = 16x, ADC range = 32 μA , $t_{\text{INT}}=129.1\text{ }\mu\text{s}$; $f_s = 200\text{ Hz}$

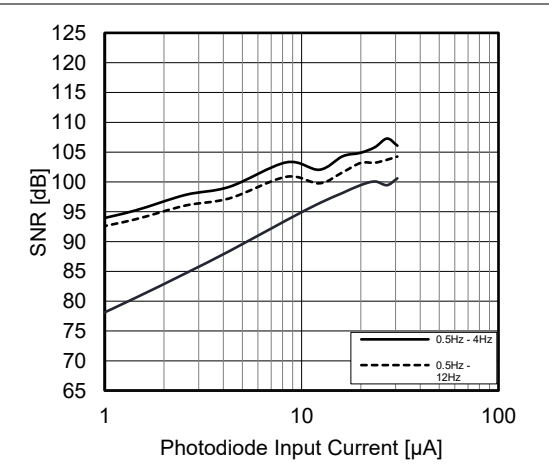


Figure 8: SNR vs. PD current ADC range = 64 μA , $t_{\text{INT}} = 129.1 \mu\text{s}$

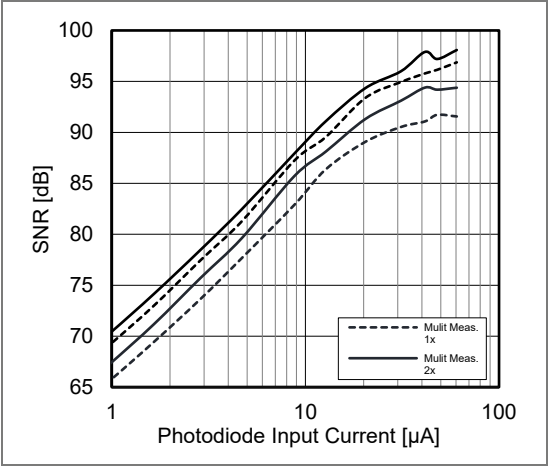
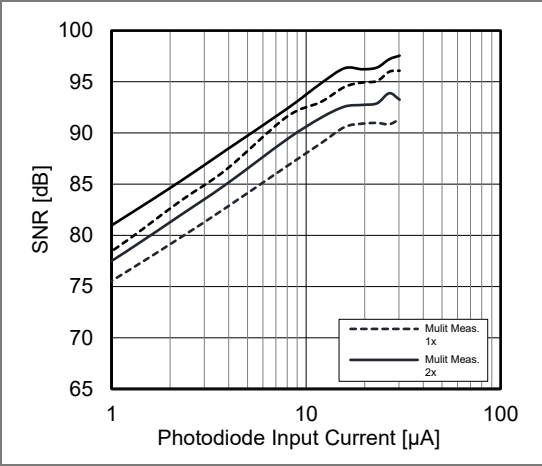


Figure 9: SNR vs. PD current ADC range = 32 μA , $t_{\text{INT}} = 129.1 \mu\text{s}$



7 Functional description

The AS7160 data acquisition system supports up to eight LEDs and eight photodiode inputs and includes two high-resolution optical readout channels with a new ambient light cancelation feature and two high-current LED drivers to complete the system.

The AS7160 is fully programmable by the registers, and the digital output data is stored in a 512-word FIFO. The FIFO allows the device to be connected to a microcontroller or processor on a shared I²C or SPI bus. They both operate in fully autonomous mode for low-power battery applications.

The device works on a 1.8 V main supply voltage and up to 5.5 V at the LED pins. They both have flexible timing and shutdown configurations, as well as control of individual blocks to minimize the total power consumption during downtime to optimize the measurement with securing a high accuracy.

7.1 LED driver

The data acquisition block in the AS7160 features two independent LED current drivers connected to eight LED input pins via two multiplexers. The two LED current sinks have 8-bit resolution with four programmable full-scale range settings of 25 mA, 150 mA, 225 mA, and 300 mA (typ.). The lowest range with 25 mA is supposed to be used in combination with the VCSEL emitter technology. Both drivers include their protection block to supervise the power supply and interrupt when a malfunction is detected, which would violate laser safety regulations. The configuration of the LED drivers can be uniquely set for each measurement. The **SUBY_DRVX_SEL** defines which LED is selected for each sub sample measurement.

Table 6: LED driver and MUX configuration

Register value	SUBy_DRV1_SEL	SUBy_DRV2_SEL
0	LED1	LED5
1	LED2	LED6
2	LED3	LED7
3	LED4	LED8

Figure 10 shows how the two LED drivers are connected to the eight LED pins and how the VCSEL protection block is integrated. The minimum LED supply voltage V_{LED} depends on the forward voltage of the selected LEDs and the minimum driver headroom voltage which is shown in Table 7.

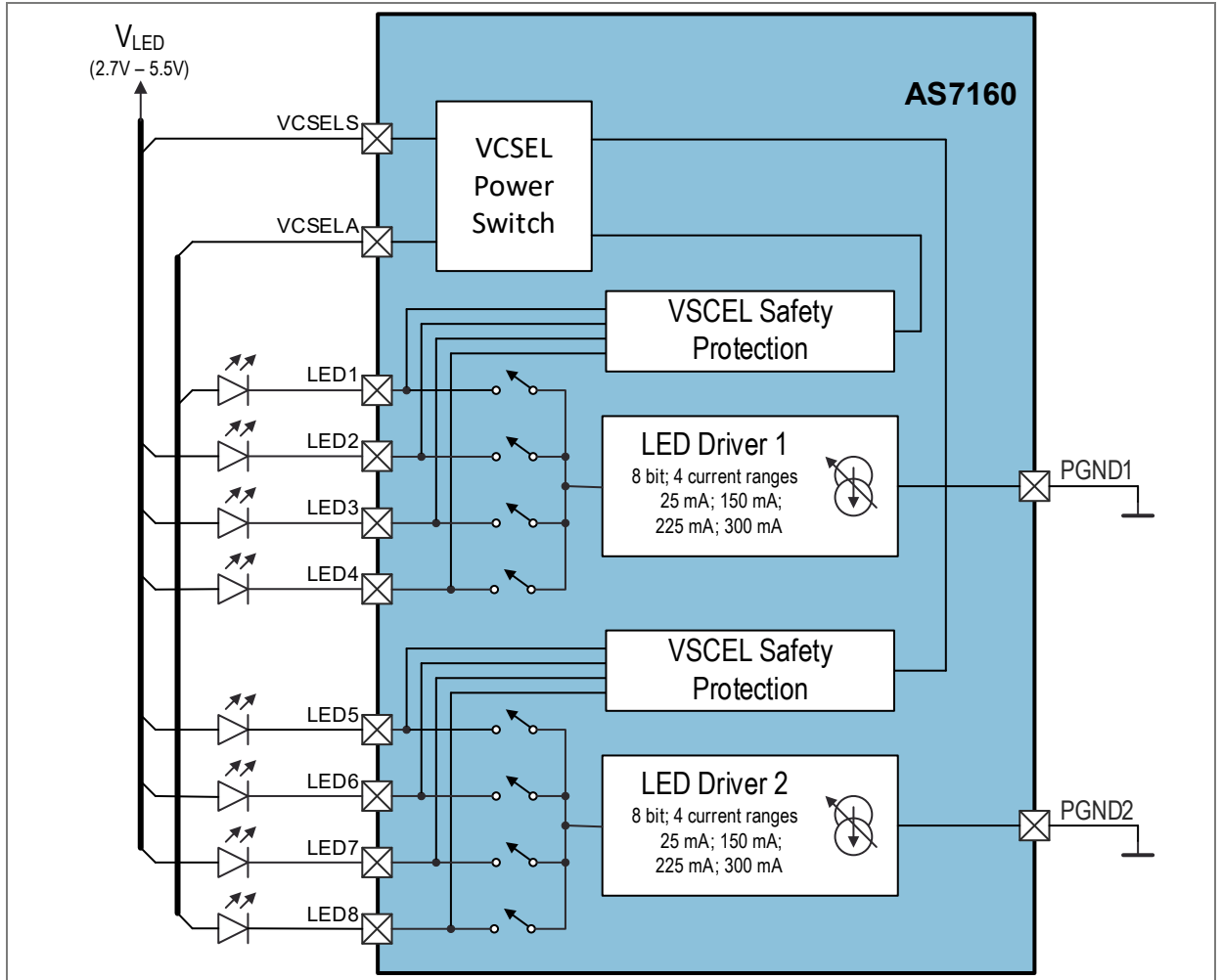
Since AS7160 current sinks support up to four different current operation ranges the minimum driver headroom voltage is also dependent on the selected LED driver full-scale range. Therefore, the minimum voltage that needs to be applied is the sum of the forward voltage of the LED and the LED driver headroom voltage depending on the selected LED driver full scale range.

Table 7: LED driver full-scale range headroom voltage

LED driver full-scale range (mA)	LED driver headroom voltage (mV)
25	300
150	400
225	550
300	750

The V_{LED} supply voltage must be above the sum of both voltages to enable proper regulation of the LED driver and to guarantee the configured LED current for each driver. A lower supply voltage can result in increased noise behavior and not reaching target LED currents.

Figure 10: LED driver block diagram



The LED driver includes a VCSEL safety protection. This block consists of a PMOS VCSEL supply switch, a watchdog, and two comparators for short circuit detection. The block is activated if the current range for the LED driver is set to 25 mA (**LED_IRNGX** = 0). The **VCSEL_MODE** register provides the selection of the monitored LED pad.

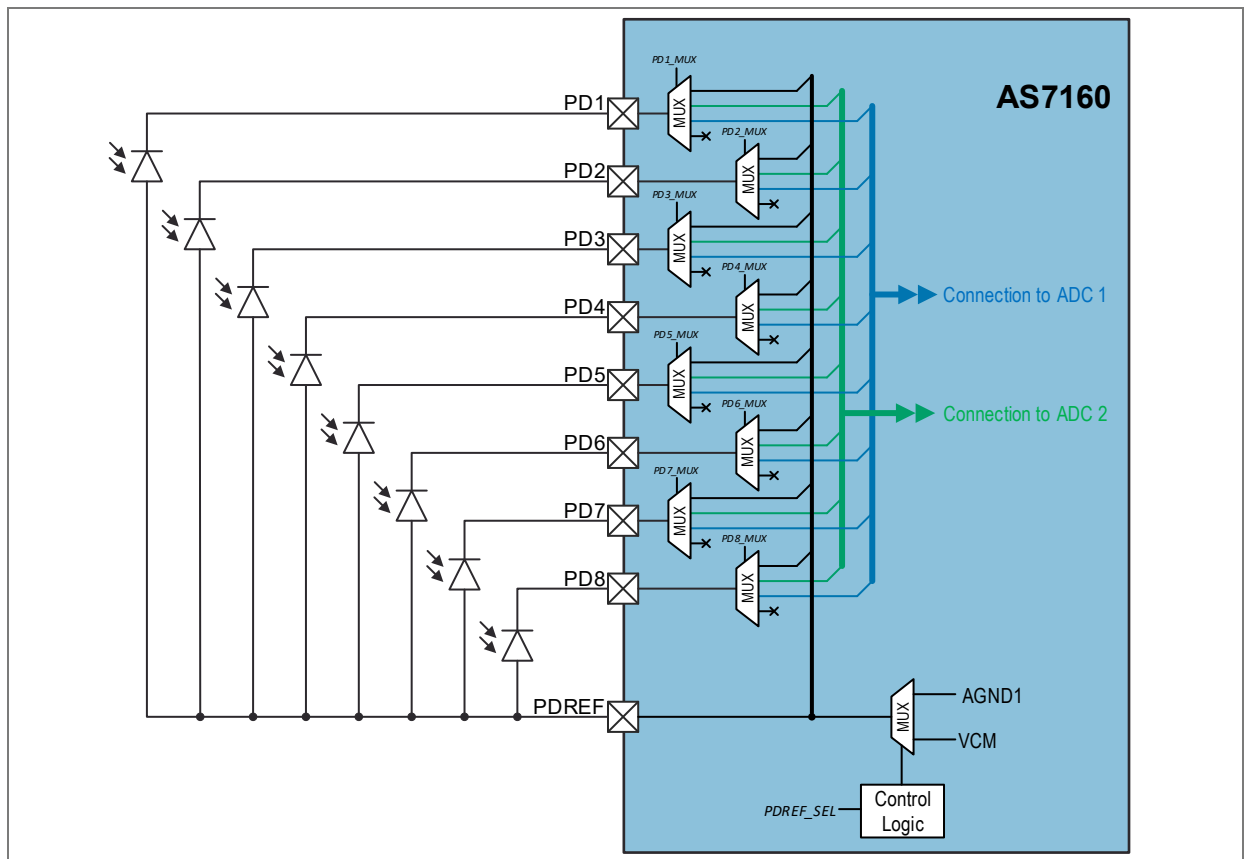
The major events monitored by the protection block are short circuits to VSS and VCSELS pins as well as monitoring the on-time. If the LED on-time is larger than the watchdog time, an interrupt is generated, and the VCSEL power switch is switched off automatically.

In case the block detects any error, the measurement is immediately stopped (e.g. watchdog event) and an interrupt is released. The **STATUS_VCSEL** status register shows the source of the error (a short to VSS, a short to VCSELS, or a watchdog event). If no VCSEL is used, the protection feature can be switched off with the **VCSEL_CFG** register.

7.2 Photodiode inputs

The AS7160 supports up to eight photodiode inputs which can be routed to both ADCs for highest design flexibility. A simplified block diagram which shows the input structures of the photodiode inputs is shown in Figure 11. Each photodiode input features a dedicated multiplexer that allows each photodiode to be connected to ADC 1, ADC 2 or PDREF pin which is the default connection to short circuit the photodiodes when not in use. This is also the reset state after power-up and when no measurement is ongoing. The input multiplexers are controlled automatically with the built in measurement sequencer and get connected and disconnected while a measurement is ongoing, according to the device configuration.

Figure 11: Photodiodes input selection



It is also possible to change the PDREF voltage level from typ. 0.8 V to 0 V via register **PDREF_SEL** register.

7.3 ADC1 and ADC2

The data acquisition signal path of AS7160 features two parallel synchronous current input analog to digital converters. Both ADC channels shown in Figure 12 and Figure 13 do provide same functionality and support true synchronous sampling of the assigned photodiode inputs. Therefore, it is possible to read out two photodiodes in a single subsample measurement.

Figure 12: ADC 1 signal path

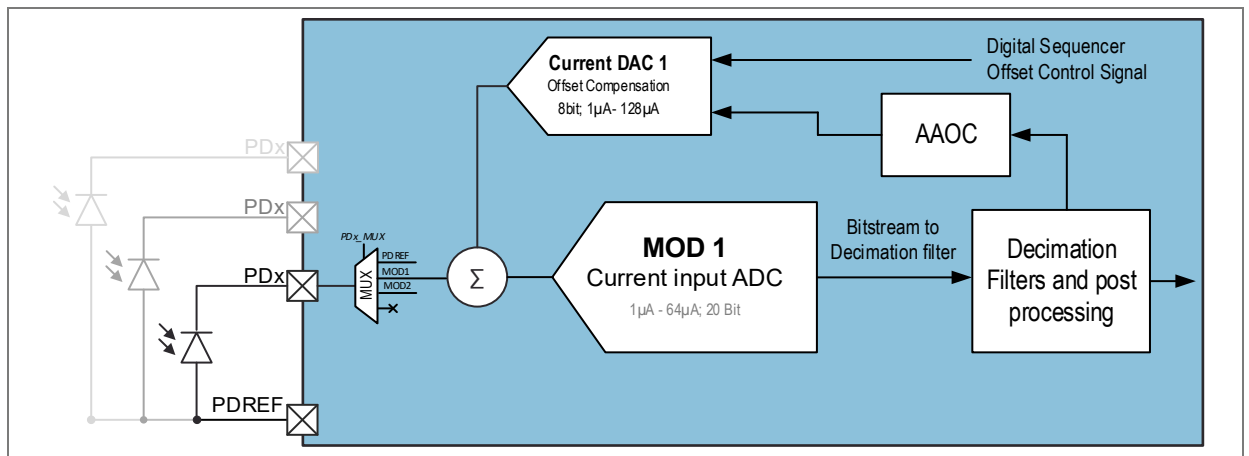
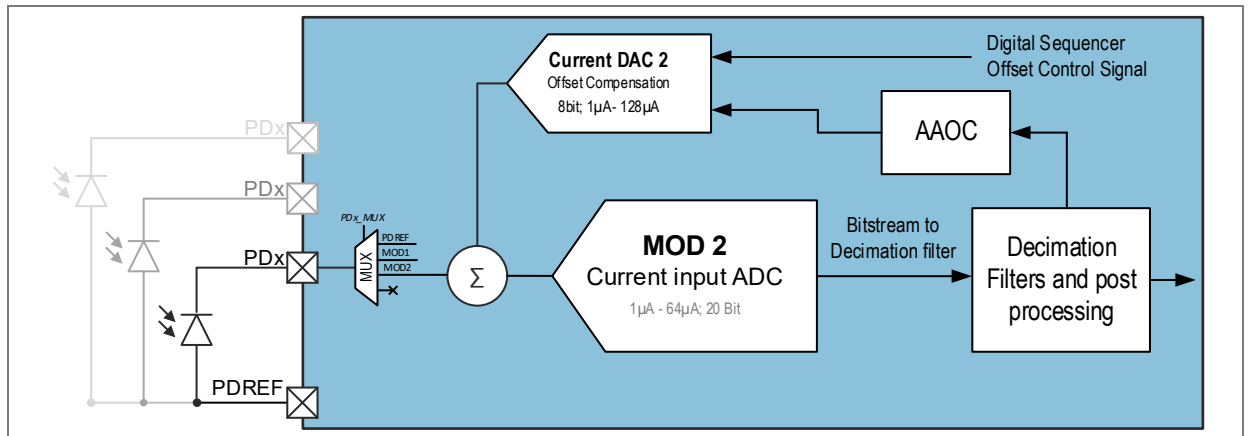


Figure 13: ADC 2 signal path



For applications requiring only one signal path to be active, one of the two channels can certainly be powered down via simple register control to reduce overall system power consumption. Each Modulator signal path supports seven full-scale range settings of 1 μ A, 2 μ A, 4 μ A, 8 μ A, 16 μ A, 32 μ A, and 64 μ A which is configured in **MOD1_CFG3** and **MOD2_CFG3** registers.

In order to achieve best ADC performance, it is necessary to reconfigure various complimentary device registers for different ADC full scale ranges dependent on the configured ADC full scale range. An overview with the necessary register configurations is shown in Table 8 and Table 9 for both ADC channels separately.

Table 8: ADC 1 register configuration depending on input full scale range

Register name	ADC _{FS} 1μA	ADC _{FS} 2μA	ADC _{FS} 4μA	ADC _{FS} 8μA	ADC _{FS} 16μA	ADC _{FS} 32μA	ADC _{FS} 64μA
MOD1_CFG1 [7:0] Address: 0x3a	0xA7	0xA7	0xA7	0xA7	0xAF	0x9F	0x9F
MOD1_CFG2 [3:0] Address: 0x3b	0x04	0x04	0x04	0x04	0x04	0x04	0x04
MOD1_CFG3 [7:0] Address: 0x3c	0x0 0	0x01	0x03	0x07	0x0F	0x1F	0x3F

Table 9: ADC 2 register configuration depending on input full scale range

Register name	ADC _{FS} 1μA	ADC _{FS} 2μA	ADC _{FS} 4μA	ADC _{FS} 8μA	ADC _{FS} 16μA	ADC _{FS} 32μA	ADC _{FS} 64μA
MOD2_CFG1 [7:0] Address: 0x3d	0xA7	0xA7	0xA7	0xA7	0xAF	0x9F	0x9F
MOD2_CFG2 [3:0] Address: 0x3e	0x04	0x04	0x04	0x04	0x04	0x04	0x04
MOD2_CFG3 [7:0] Address: 0x3f	0x0 0	0x01	0x03	0x07	0x0F	0x1F	0x3F

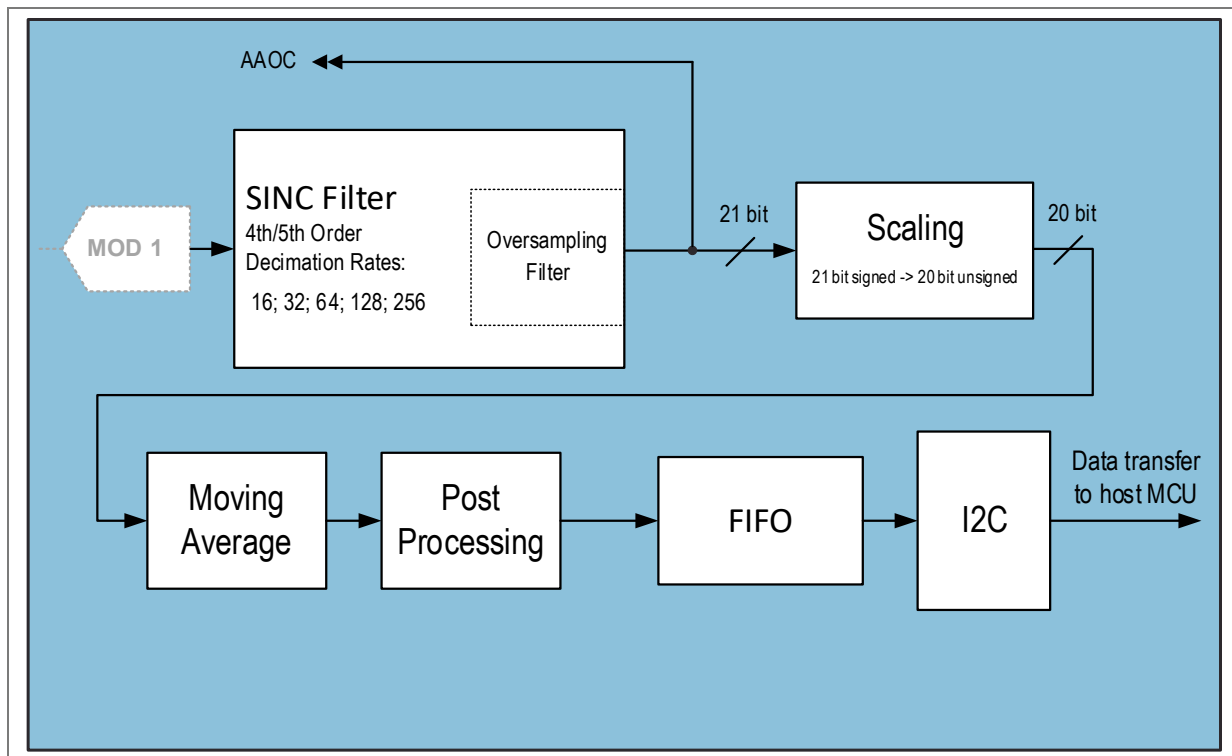
In addition to the full-scale settings both modulators have additional configuration registers **SINC_CFGA**, **SINC_CFGB** and **SINC_CFGC** which allow the configuration of the decimation filters and filter order to control the desired integrations times which are the determining factor for signal integrity as well as noise behavior for the target application.

Each signal path also includes an 8-bit offset current DAC for extending the optical dynamic range by sourcing some of the exposure current to the offset DAC. This feature helps to avoid the saturation of the ADC under high ambient light exposure. The current of the offset DAC can be directly controlled via registers **IOS_MOD1_SUBx** and **IOS_MOD2_SUBx** for each subsample and each modulator separately. This allows engineers to utilize their own offset compensations algorithms running on the host signal-processing unit. However, in case customers do not have an algorithm, AS7160 features also an Advanced Automatic Offset Cancellation (AAOC) function shown in Figure 12 and Figure 13 which automatically controls the DC offset compensation DAC eliminating the latency effect caused by I²C configuration via an external host MCU.

As indicated in the previous chapters and drawings, AS7160 supports various different post-processing options. An overview of all options and a device signal flow is shown in Figure 14. Please note that the processing options shown in Figure 14 are for ADC 1 and ADC 2 the same.

The output of each modulator is connected to the SINC filter block, which acts as down sampling filter. It is possible to select between 4th and 5th filter order via register **SEL_ORDER** as well as decimation rates between 16, 32, 64, 128 and 256 via register **SINC_DEC**. In order to further improve SNR of the system there is an oversampling filter function, which is part of the down sampling filter, that can be enabled via register **SINC_OVS**. The three-bit register allows to enable 7 different oversampling filter ratios from factor 2 up to 128. The oversampling filter function is disabled in default configuration. Please mind that by enabling the oversampling function the active ADC modulator time is increased and therefore influencing power consumption with the benefit of better noise behavior. Once the signal passed the SINC decimation and optional oversampling filter the signal is feed into a scaling block which converts the signal into 20-bit unsigned signal. The next post-processing block, which can be enabled via register **MOVING_AVERAGE_ON** is an on-chip moving average filter. The number of samples used for the moving average filter varies from 2 samples up to 16 samples and can be configured with register **MOVING_AVERAGE_VAL**. The last processing block, before that data is written to the FIFO memory, is a simple post-processing block. It enables the detection of modulator saturation and manipulation of the saturated data with fixed values. This function can be enabled via register **ASAT_ON**.

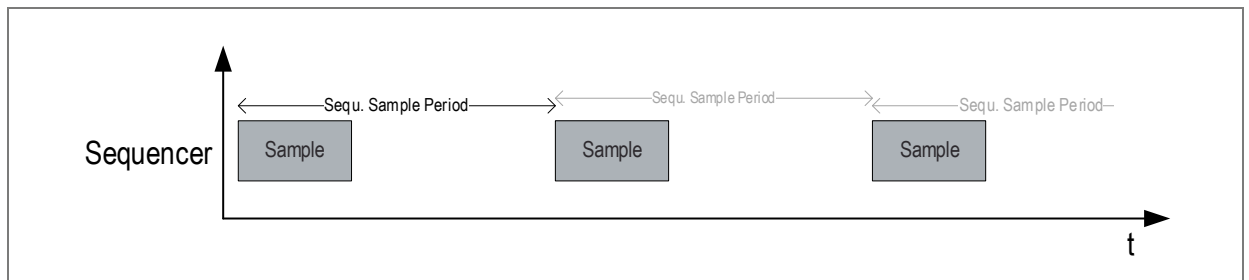
Figure 14: ADC signal post processing overview



7.4 Sequencer

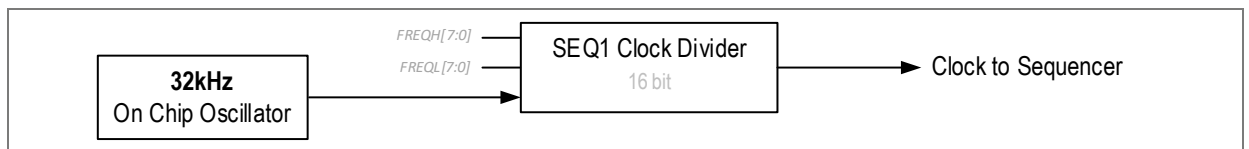
In order to unload MCU with re-occurring measurement tasks AS7160 has a built-in measurement sequencer which controls all hardware blocks with its corresponding timings. An overview of the sequencer timing diagram is shown in Figure 15.

Figure 15: Sequencer timing diagram



The timing for the sequencer is derived from the on-chip 32 kHz oscillator and is configured with the 16-bit clock divider registers **FREQH** and **FREQL**. A clock generation scheme for the sample rate generation is shown in Figure 16.

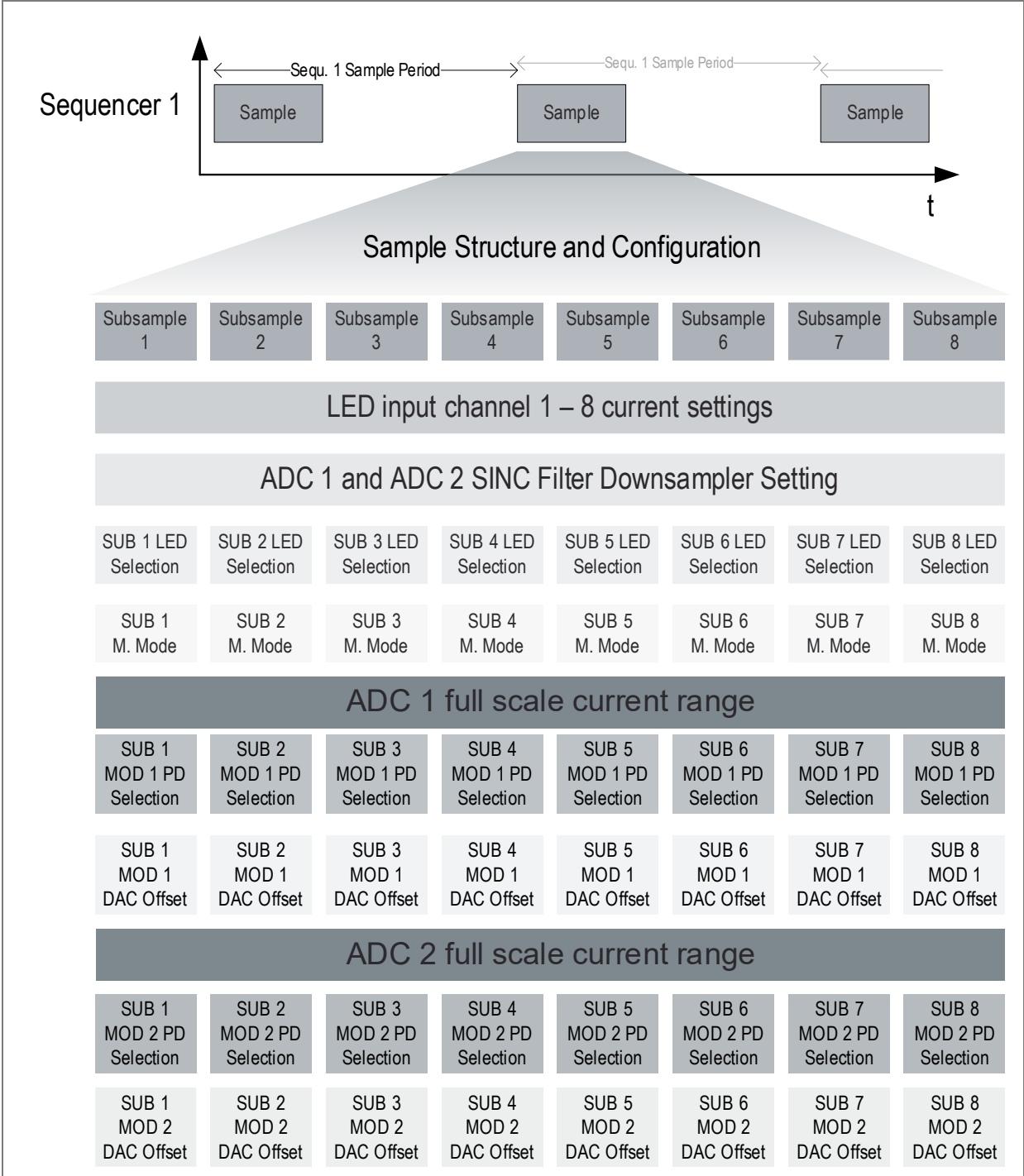
Figure 16: Sequencer clock generation



7.5 Measurement sample structure

The AS7160 offers high flexibility in programming all the different combinations of the photodiode and LED pins. The sequencer divides measurements into samples according to the programmed sample period times like it is shown in Figure 15. Each sample can be divided into a maximum of eight subsamples, which allow for individual configuration. An overview of the configuration options for a measurement sample is shown in Figure 17. There are general settings like which LED is assigned to which LED input channel which are the same for each subsample. The LED input channel current settings can be configured with **LEDx_ICTRL** along with the LED current range **LEDx_IRNG** for each LED.

Figure 17: Sample structure and configuration options



The second parameter which applies to all enabled subsamples are the settings for the SINC decimation filter and oversampling settings for ADC1 and ADC2 which can be configured in **SINC_DEC**, **SINC_OVS** and **SEL_ORDER**. In addition to the oversampling and LED current settings the LED assignment (**LED_SUBx**) as well as the measurement mode (**MODE_x**) for each subsample is a setting which is used for both ADC channels like it is shown in Figure 17. In order to maintain best dynamic range and noise behavior it is also important that the current range for ADC1 and ADC2 is configured accordingly. The current range configuration for each ADC applies also to all subsamples in a PGG measurement and can be configured with registers **MOD1_IOS_FS** and **MOD2_IOS_FS**. Individual configurations for each ADC are the photodiode assignments via register **MOD1_PDSELx** and **MOD2_PDSELx** as well as the offset DAC currents for ambient light rejection which can be configured via **IOS_MOD1_SUBx** and **IOS_MOD2_SUBx** registers.

7.5.1 Measurement modes

AS7160 does support three basic measurement modes which are:

- Single Measurement Mode
- Multi Measurement Mode
- Interleaved Measurement Mode

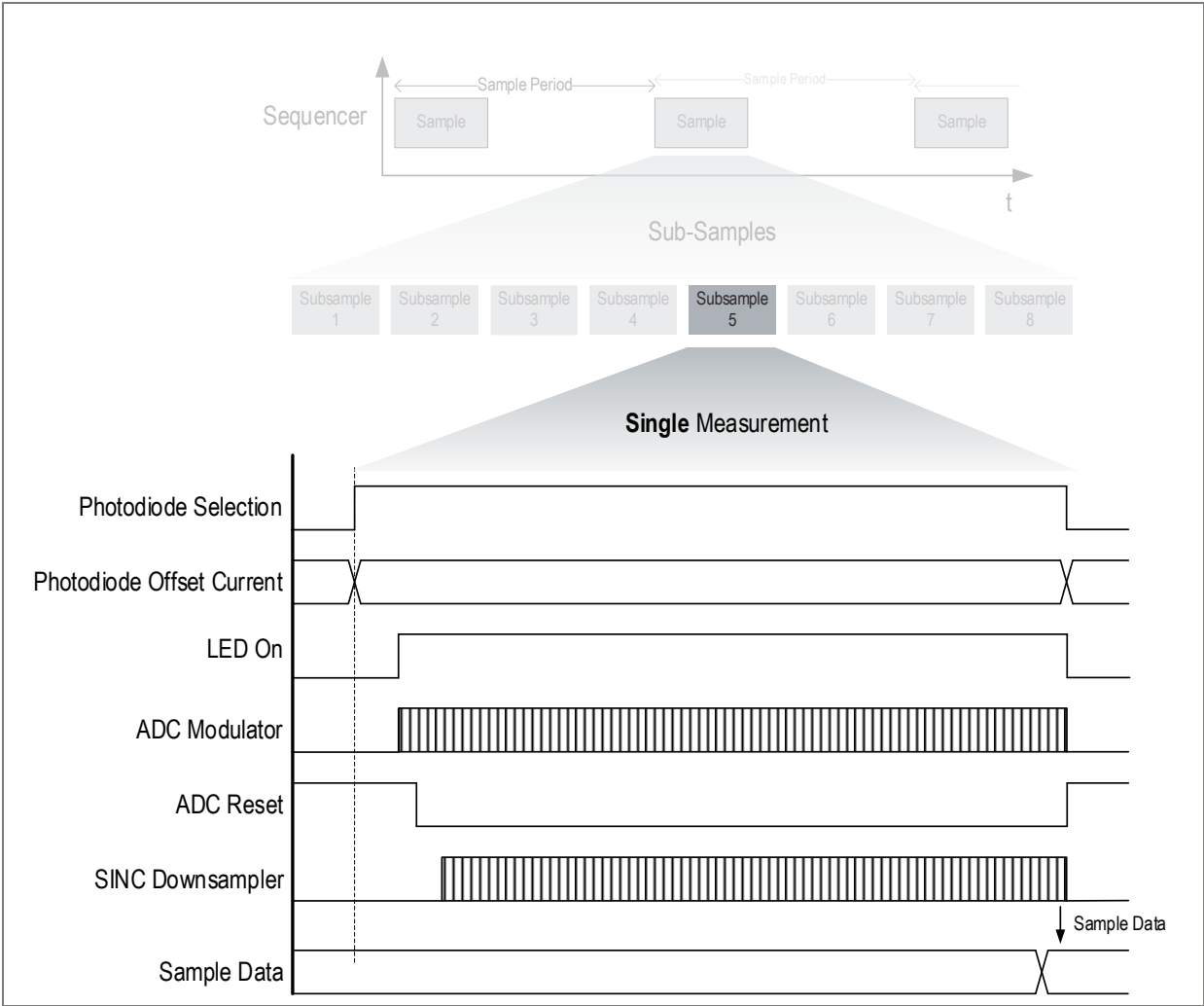
The three measurement modes covered in this chapter are basic measurement modes which do not support any kind of ambient light compensation. If ambient light compensation measurement modes are desired please refer to chapter 7.5.2 Ambient light compensation. However, it's worth mentioning that all measurement modes for ambient light compensation do rely on the basic principle and timing of the Single Measurement mode which is described in this chapter and illustrated in Figure 18.

7.5.1.1 Single measurement

The Single Measurement mode is the simplest measurement which can be selected and assigned to a subsample as a measurement. A simplified timing diagram to explain the operation mode and working principle of the Single Measurement is shown in Figure 18. Once a Single measurement is executed, the first step in the measurement procedure is that the assigned photodiode is connected via the internal multiplexers to the selected ADC channel. At the same time a DAC offset current, which is setup in the **IOS_MOD1_SUBx** for, is applied to the summing node of the selected ADC and the photodiode input. After a short delay, which can be configured as part of the chip configuration, the LEDs with the configured LED currents are enabled for the measurement and in parallel, the ADC modulator is started.

After a configurable modulator reset time, the SINC down-sampler filter is fed with data. The measurement time depends now very much on the configuration of the SINC filter, filter order and internal clock speed of AS7160. Once the measurement time has elapsed the sample data is written to the FIFO memory and ready for readout by a host MCU.

Figure 18: Single measurement mode – simplified timing diagram



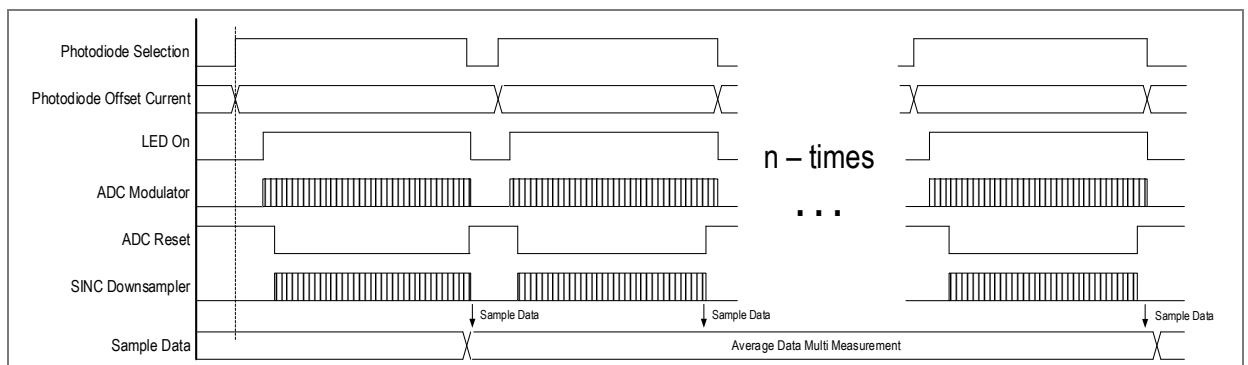
7.5.1.2 Multi measurement

The Multi Measurement operation mode is used to further enhance signal quality and allows for on-chip averaging over a predefined number of measurements. At the end of the measurement, one average value is stored to the FIFO memory.

The advantage compared to a standard moving average filter is the reduction of the time difference between the used sub-samples for averaging. The multi measurement uses multiple subsample timings with close to 0-time difference in comparison when a moving average filter is used. The used data is one sub-sample out of one sampling period. This is stacked over time to achieve the average. Therefore, the overall time until an averaged value is available is shortened with multi measurement in comparison to a standard moving average filter approach.

The total measurement time is then related to the number of multi measurements, which can be set in the **MODEx** register. This functionality can also be used with the Ambient Light Compensation Measurement modes described in chapter 7.5.2. A simplified timing diagram for a Single Measurement with activated Multi Measurement is shown in Figure 19.

Figure 19: Multi measurement mode – simplified timing diagram



7.5.2 Ambient light compensation

AS7160 offers up to three different options to compensate for ambient light influences while a measurement is ongoing. This chapter provides a detailed description of Double Measurement, Tripple Measurement and the Advanced Automatic Offset Compensation (AAOC).

7.5.2.1 Double measurement

The double sampling function measures two values within a subsample. The first measurement is the same like a single measurement with the LED enabled and the configured offset current is applied to the ADC input channel. The sample data is stored temporarily in the memory. The second part of the measurement is done with the LED disabled which represents an ambient light measurement. The difference between the first measurement and the ambient light measurement is stored in the FIFO memory.

Equation 1: Double measurement result calculation

$$C_{DOUBLE} = C_{LEDON} - C_{LEDOFF}$$

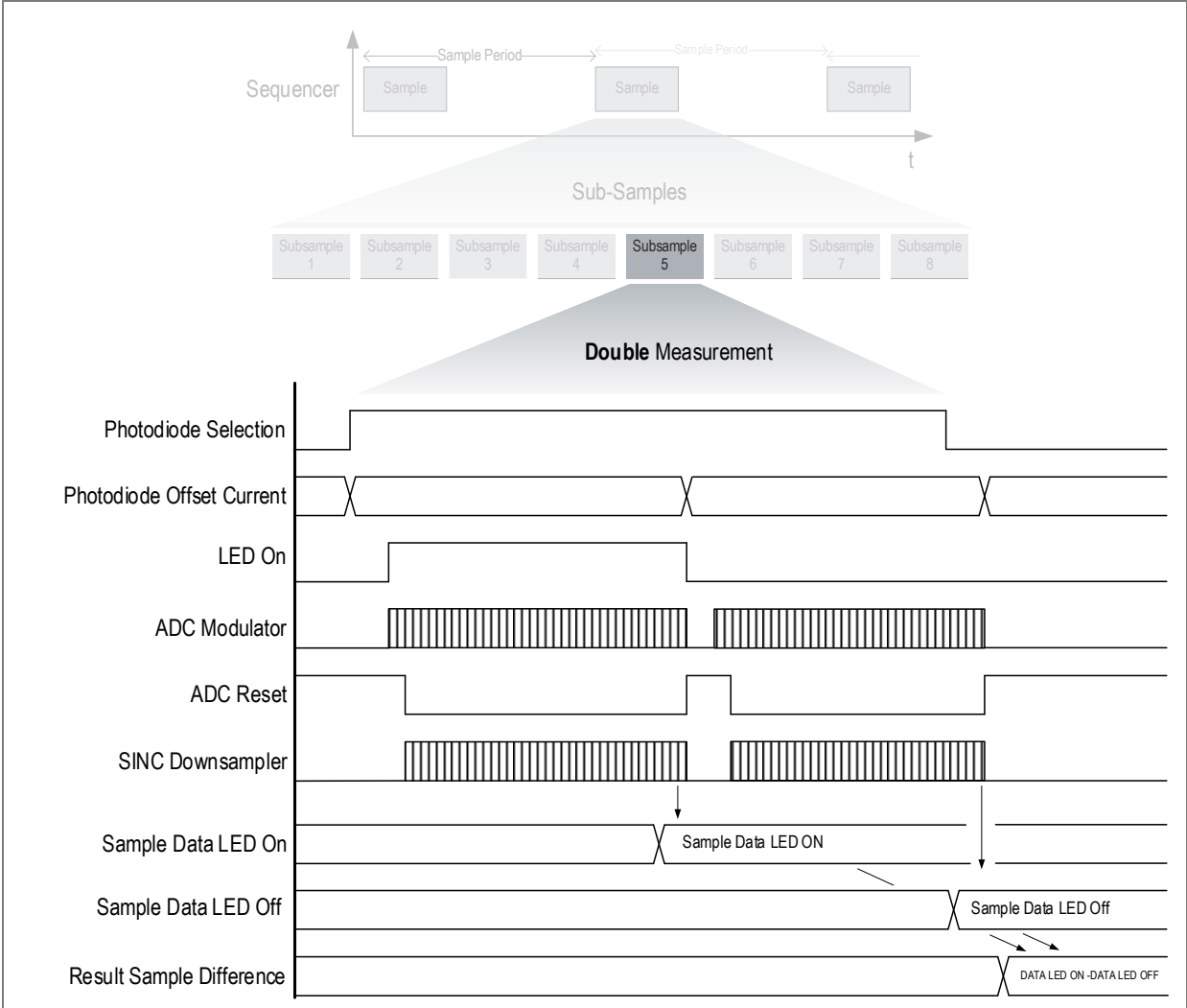
C_{DOUBLE} ... Double Measurement result stored to FIFO

C_{LEDON} ... ADC count value during LED on phase

C_{LEDOFF} ... ADC count values during LED off phase

The assignment of the photodiodes is for both measurements the same. The programmed DAC offset current is used for the first measurement and can also be used for the second measurement (**DIS_LEDOFF** = 1). Alternatively, it is possible to use also a different value, which is stored to **IOS_LEDOFF** register, for all subsamples if register **DIS_LEDOFF** bit is cleared.

Figure 20: Double measurement mode – simplified timing diagram



7.5.2.2 Tripple measurement

The Tripple Measurement function measures three different values within a subsample. The first measurement is an ambient light measurement with the LED disabled. The result of this sampling is stored temporarily to the device. The ambient light measurement is followed then by a measurement where the LED is enabled with the predefined LED current. Its measurement results is again stored temporarily to the device memory. The last part of a Tripple Measurement is again an ambient light measurement where the LEDs are disabled. Its result is also stored temporarily to the device memory and used for the calculation for the final measurement value which is stored to the FIFO memory. The calculation of the value stored to the FIFO memory is shown in Equation 2.

Equation 2: Tripple measurement result calculation

$$C_{TRIPPLE} = C_{LEDON} - \frac{C_{LEDOFF1}}{2} - \frac{C_{LEDOFF2}}{2}$$

$C_{TRIPPLE}$...FIFO Tripple Measurement result

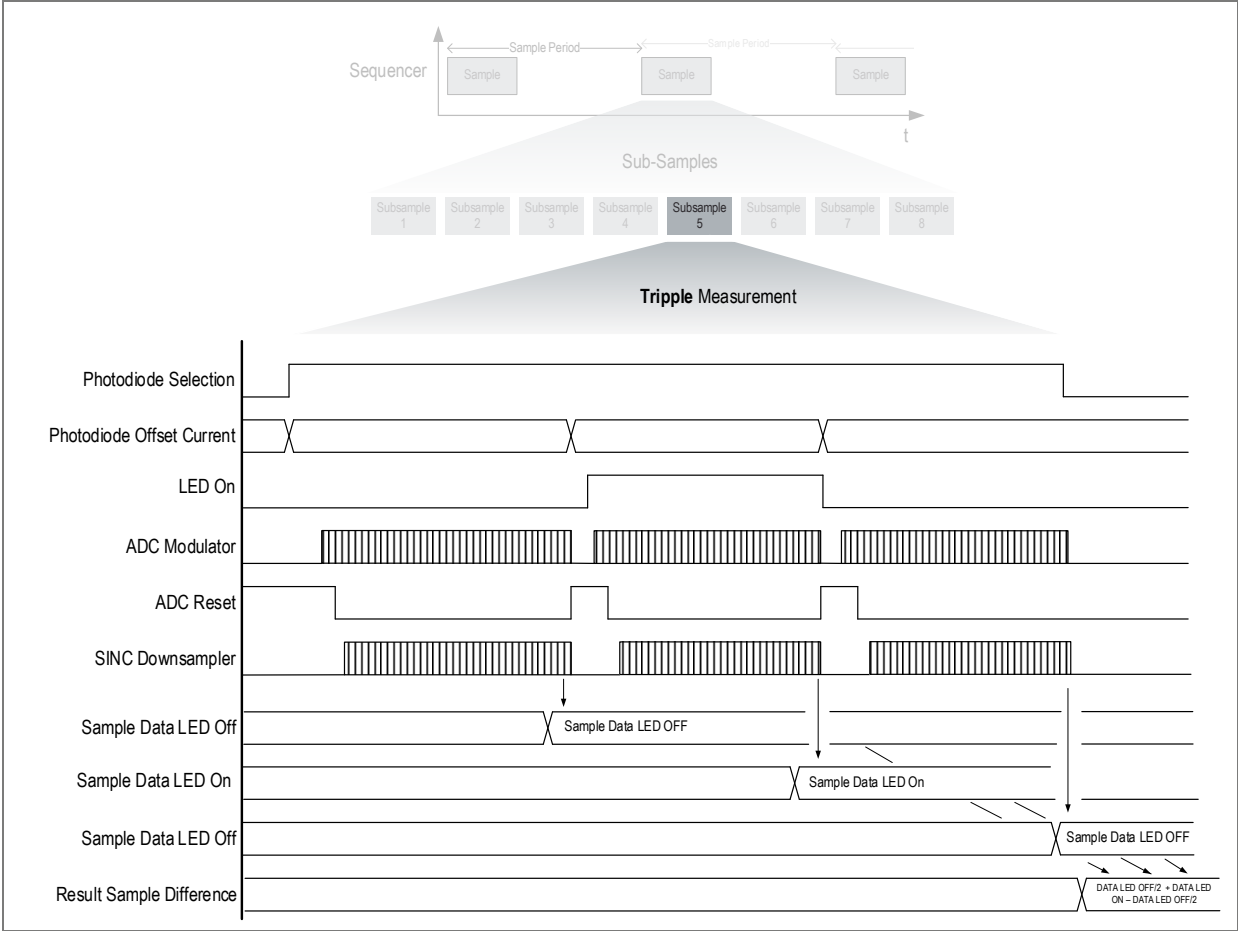
C_{LEDON} ...ADC count value during LED on phase

$C_{LEDOFF1}$...ADC count values during first LED off phase

$C_{LEDOFF2}$...ADC count values during second LED off phase

The assignment of the photodiodes is for all three measurements the same. The programmed DAC offset current is used for the second measurement but can also be used for the first and third measurement (**DIS_LEDOFF** = 1). Alternatively, it is possible to use also a different value during the LED off measurement phases which is stored to **IOS_LEDOFF** register if register **DIS_LEDOFF** bit is cleared.

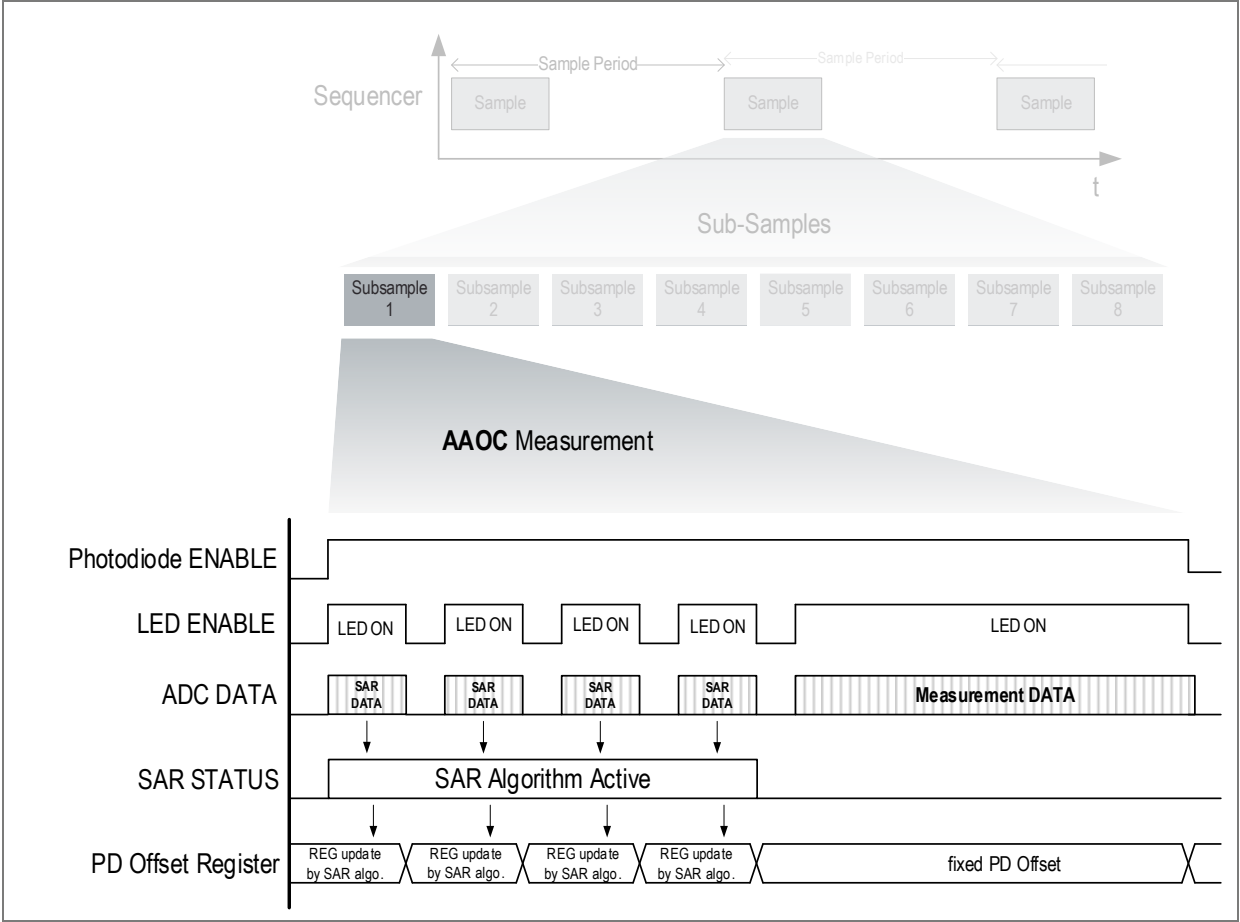
Figure 21: Tripple measurement mode – simplified timing diagram



7.5.2.3 Advanced automatic offset compensation (AAOC)

The built in AAOC is an advanced ambient light compensation solution which does not require an external host to adjust the DAC offset current. In conventional approach with Double Measurement and Tripple Measurement the DAC offset current registers need to be controlled and adjusted by a host MCU via I²C or SPI interface. This approach might require several measurement iterations until an appropriate offset value is found. The AAOC function eliminates the need of MCU interaction to find the correct photodiode offset current. It is based on a successive approximation approach to determine the upper 4 bits of the photodiode offset register. In order to achieve this and adjust the 4 bits accordingly. AS7160 does four short measurements prior to the actual measurement like it is shown in Figure 22. During each pre-measurement cycle the LED is also switched on and the ADC data read is feed into the SAR algorithm which adjusts the photodiode current. Once all four pre-measurements are done the offset current is adjusted correctly to avoid saturation of the ADC due to ambient light. The upper 4 bits of **IOS_MODx_SUBx** registers are determined automatically with the first four samplings, the lower 4 bits correspond to the programmable bits. The FIFO stores the AAOC data and the ADC results to simplify signal reconstruction for algorithm developers. The programmed current values for the LEDs are used for all five measurements. The assignment of the photodiodes is also fixed for all 5 measurements.

Figure 22: AAOC – simplified timing diagram



7.5.3 Parameter

This chapter contains detailed timing diagrams and parameters for the measurement samples.

Figure 23: Single measurement timing diagram

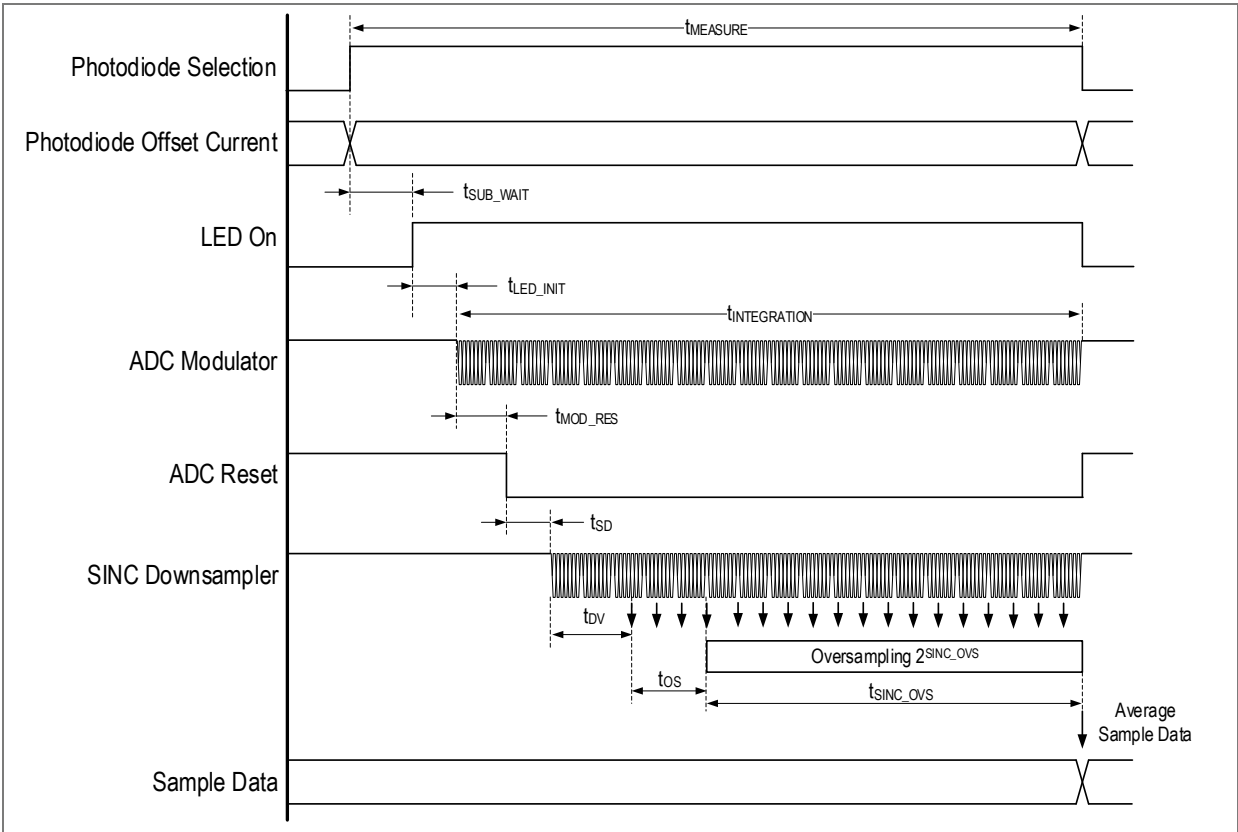


Figure 24: Double measurement timing diagram

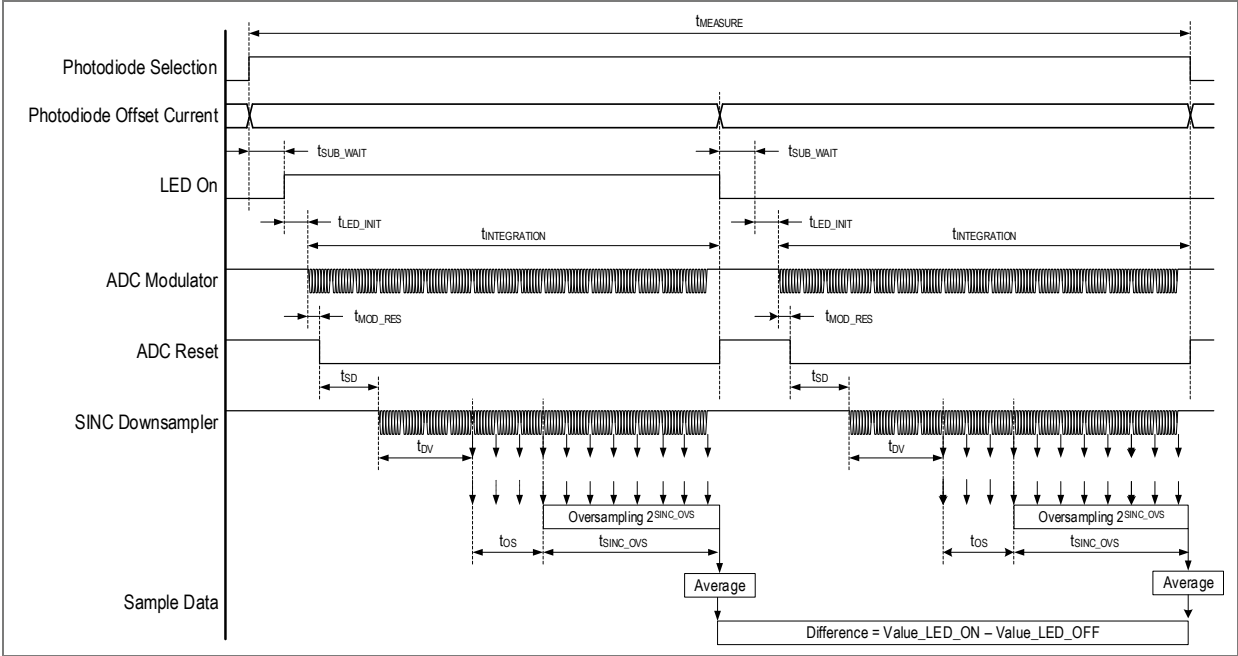


Figure 25: Tripple measurement timing diagram

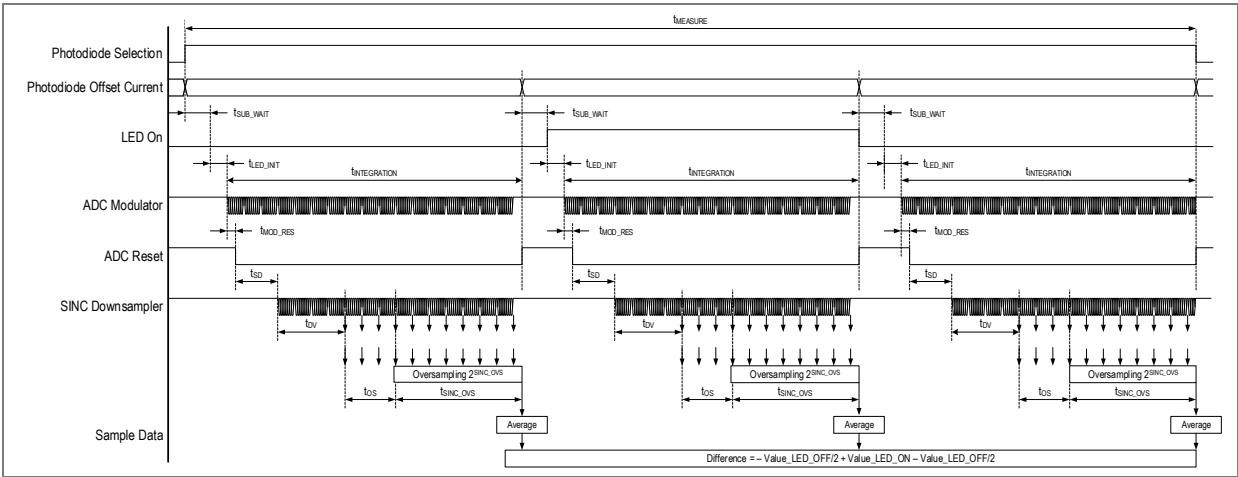


Figure 26: AAOC timing diagram

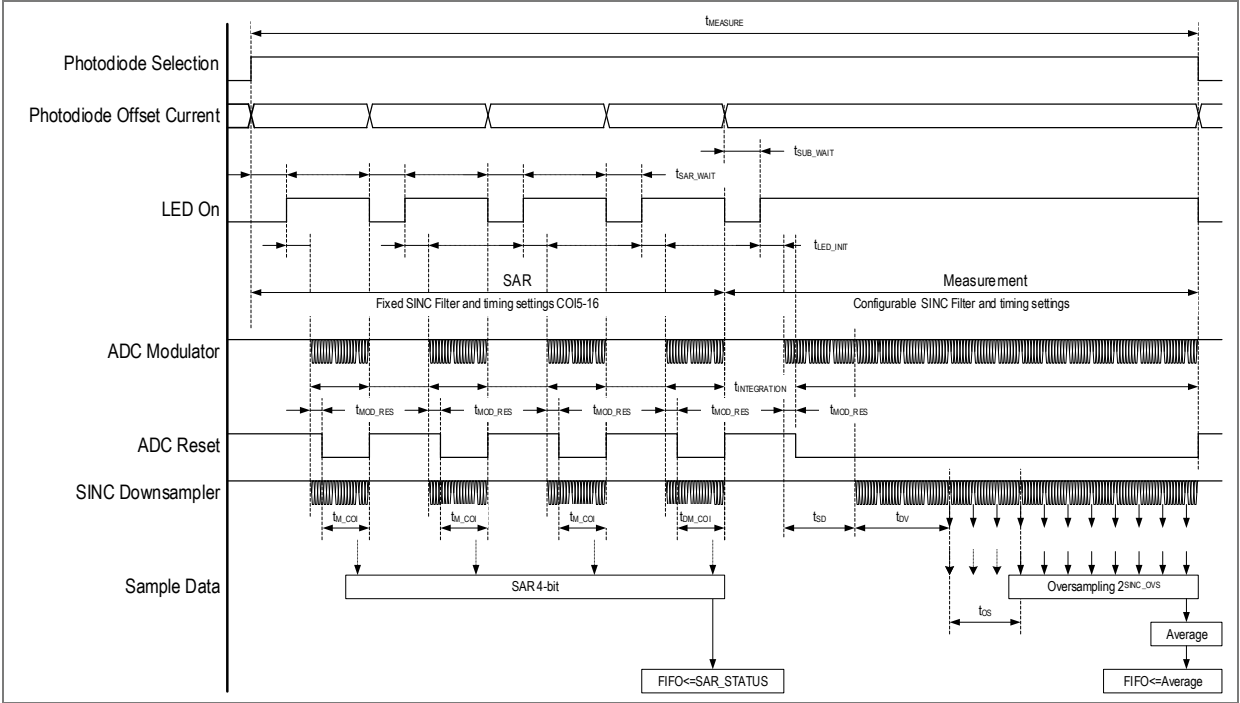


Table 10: Timing parameter measurement modes

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{\text{SUB_WAIT}}$	Subsample wait time	Parameter controlled via <i>sub_wait</i> register	0		255	μs
$t_{\text{LED_INIT}}$	LED initialization time	Parameter controlled via <i>led_init</i> register	0		255	μs
$t_{\text{MOD_RES}}$	ADC modulator reset time	Parameter controlled via <i>mod_reset_delay</i> register; <i>mod_clk</i> = 0	0.4		25.5	μs
t_{SD}	SINC downsampler start delay	Parameter controlled via <i>start_delay</i> register; <i>mod_clk</i> =0	0		25.5	μs
$t_{\text{SAR_WAIT}}$	AAOC SAR wait time	Parameter controlled via <i>sar_wait</i> register	0		255	μs
$t_{\text{M_COI}}$	SAR modulator on time	<i>mod_clk</i> =0		2.7		μs
		<i>mod_clk</i> =1		5.4		μs
		<i>mod_clk</i> =2		10.8		μs
		<i>mod_clk</i> =3		21.6		μs

The measurement time t_{MEASURE} is influenced by many parameters like modulator clock, filter order and decimation filter setting. Table 11 provides example register configurations with the resulting measurement times t_{MEASURE} depending on the modulator clock settings. In case additional information about different register settings are required please do consult your local ams OSRAM support team for assistance.

Table 11: t_{MEASURE} examples for different register settings

Register	Register example configurations								
<i>filter_mode</i>	1	1	1	1	1	1	1	1	1
<i>sel_order</i>	1	1	1	1	1	1	1	1	1
<i>seset_delay</i>	0	0	0	0	0	0	0	0	0
<i>start_delay</i>	0	0	0	0	0	0	0	0	0
<i>sinc_dec</i>	0	1	2	3	4	1	2	3	4
<i>os_delay</i>	0	0	0	0	0	0	0	0	0
<i>sinc_ovs</i>	0	0	0	0	0	1	2	4	7
ADC modulator clock ($f_{\text{MOD_CLK}}$)	t_{MEASURE} [μs]								
10 MHz	9.1	17.1	33.1	65.1	129.1	20.3	52.3	257.1	3380.3
5 MHz	18.2	34.2	66.2	130.2	258.2	40.6	104.6	514.2	6760.6
2.5 MHz	36.4	68.4	132.4	260.4	516.4	81.2	209.2	1028.4	13521
1.25 MHz	72.8	136.8	264.8	520.8	1032.8	162.4	418.4	2056.8	27042

7.6 FIFO description

The AS7160 contains a 1.5 kB FIFO register for buffering the measurement data output to an external microcontroller via the I²C or SPI interface. The FIFO buffering allows the external MCU to stay in idle mode during energy-saving measurements.

The measurement data of the three channels and possible status information from the AAOC will be collected in a common data stream and written to the FIFO. The coding of the data stream is described below in Figure 27.

Figure 27: FIFO data format

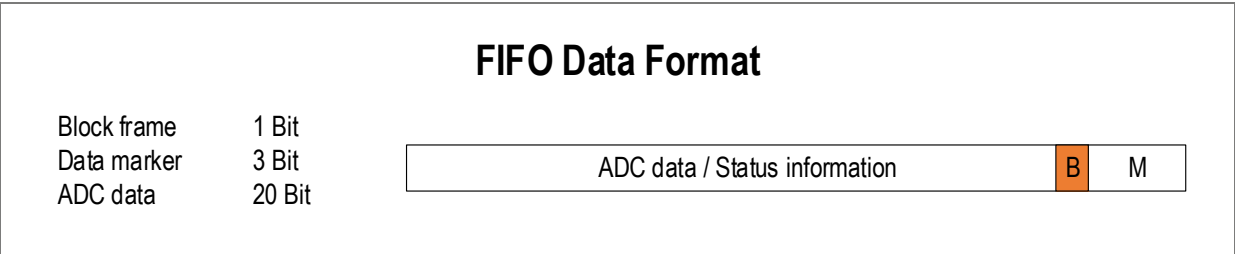


Table 12: FIFO data marker bit description

Data marker bits <2:0>	Description
'b'000	First ADC value of modulator 1
'b'001	Other ADC value of modulator 1
'b'010	First ADC value of modulator 2
'b'011	Other ADC value of modulator 2
'b'100	Reserved
'b'101	Reserved
'b'110	Reserved
'b'111	Status information

Figure 28: Status information

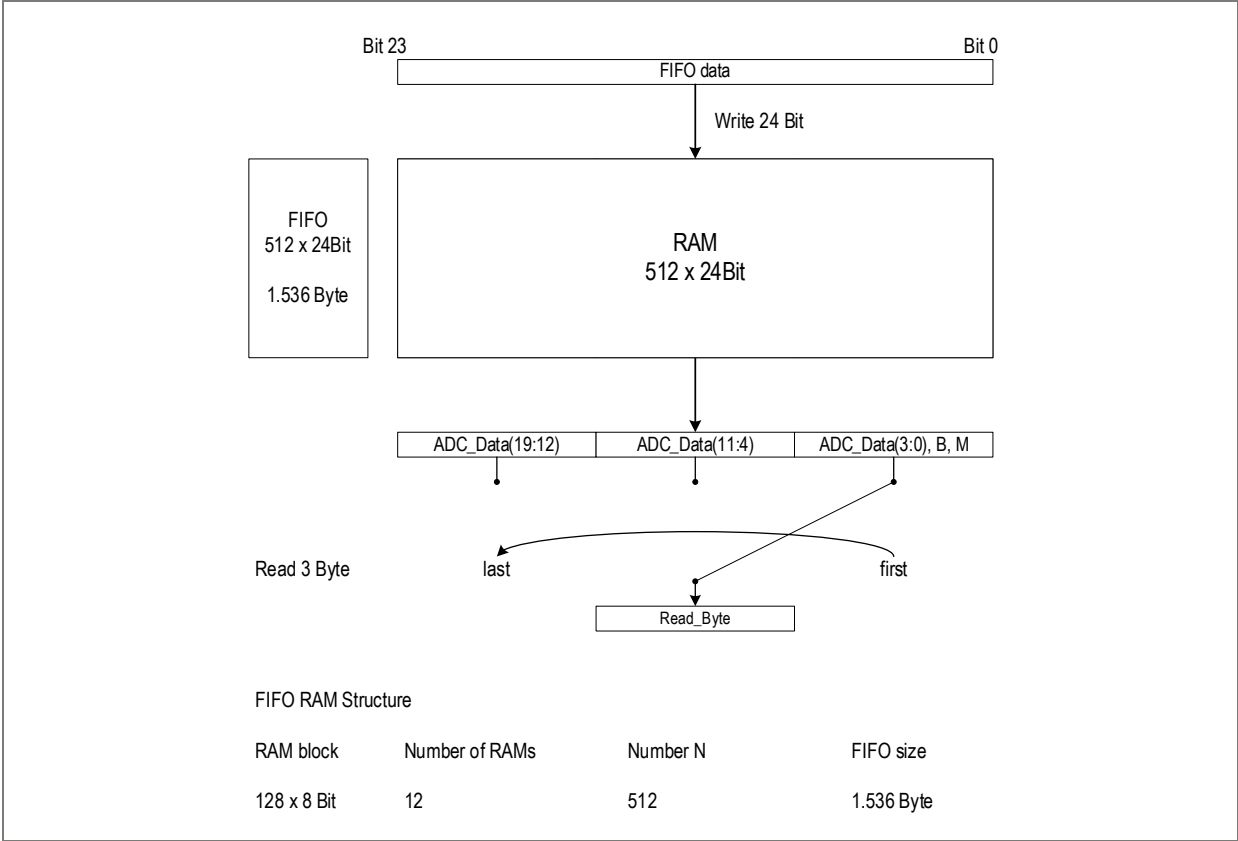
Status Informations

4Bit	4Bit	8Bit	4Bit		
Modulator	SubSample	PD Offset	3'h0	X	SAR Status (AAOC)
16'bx			3'h7	X	Synchronisation

Figure 29: AAOC status information

ADC data with SAR Status (AAOC)		
8Bit		5Bit
ADC Data(19:5)		PD Offset(7:4) X

Figure 30: FIFO data structure and organization



7.7 Communication interfaces

7.7.1 Interrupt

The interrupt manager processes interrupt events. These interrupt events must be released for processing via an interrupt enable register **IRQ_ENABLE**. The dedicated interrupt status bit is automatically reset when the corresponding sub-status register is read (auto-zero register). For the FIFO threshold reset, the FIFO must be read or cleared. In this way, no interrupt events may be lost.

7.7.2 GPIO

The GPIO pin can be used as an input or output. In default configuration the GPIO pin is configured as an input. Since the internal pull up/down resistors are disabled it is recommended to connect an external pull up or pull down resistor to define the logic input level of the pin. Alternatively, it is also possible to enable the internal pull up or pull down resistors via register **GPIO_PU** or **GPIO_PD** to avoid an external resistor as part of the initialization routine of AS7160. The logic input level can be read back via register **GPIO_IN** register. Once the GPIO pin is configured as an output via **GPIO_OEN** register there are various internal status signals which can be routed to the GPIO pin. The register **GPIO_PINMAP_SEL** in its default configuration configures the pin as normal output pin whose output signal level can be controlled via **GPIO_OUT** register. However, if the register is reconfigured it is also possible to indicate if the LEDs are enabled or if standby mode is active. Please mind that when the GPIO pin is configured as an output the **GPIO_IN** register is always set to one independent of the actual output signal level.

7.7.3 I²C/SPI interface

The AS7160 supports I²C and SPI as host communication and control interfaces. In both operation modes (I²C or SPI), AS7160 works as a slave device. The interface selection is handled via the CSXN pin during startup of the device. In case AS7160 is supposed to work in I²C operation mode it is mandatory to pull the CSXN pin high with an external pull up resistor. In case SPI operation mode should be used the CSXN pin has to be connected to the chip select pin of the SPI master device.

7.7.3.1 I²C interface

The AS7160 I²C slave uses an I²C address of 0x55 (7-bit format; R/W bit has to be added) - AAh (8-bit format for writing) and ABh (8-bit format for reading) respectively. It expects external pull-up resistors on the SDA_MOSI and SCL pins. Furthermore, it is mandatory to connect and external pull up resistors to CSXN pin for I²C interface selection. The interface supports the following features:

- Fast mode plus (1 MHz)
- Fast Mode (400 kHz)
- Standard Mode (100 kHz)
- 7+1-bit addressing mode
- Write formats
 - Single-Byte-Write
 - Burst-Write
- Read formats
 - Current-Address-Read
 - Random-Read
 - Sequential-Read
- IEEE standard requirements regarding filtering and timing are implemented.

7.7.3.2 I²C protocol

The Table 13: I²C symbol definition shows the symbols used in the coming mode descriptions.

Table 13: I²C symbol definition

Symbol	Definition	R/W	Note
S	Start condition after stop	R	1-bit
Sr	Repeated start	R	1-bit
DW	Device address for write	R	1010 1010b (AAh)
DR	Device address for read	R	1010 1011b (ABh)
WA	Word address	R	8-bit
A	Acknowledge	W	1-bit
N	No acknowledge	R	1-bit
reg_data	Register data/write	R	8-bit
data (n)	Register data/read	W	8-bit
P	Stop condition	R	1-bit
WA++	Increment word address internally	R	During acknowledge

7.7.3.3 I²C write access

Byte Write and Burst Write formats are used to write data to the slave.

Figure 31: I²C byte write format

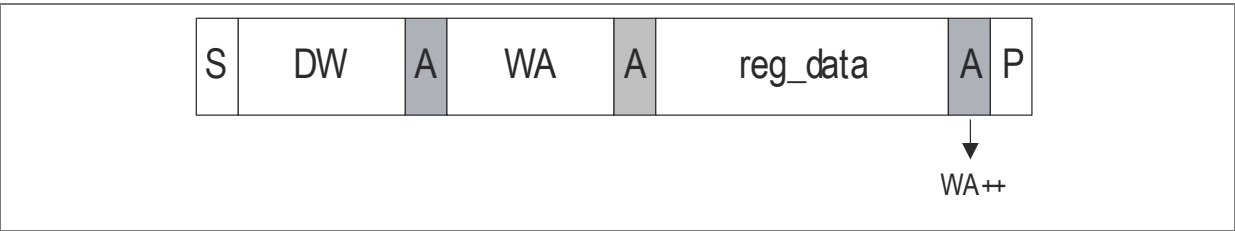
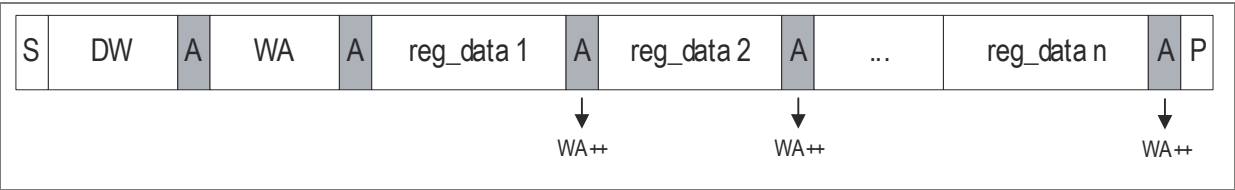


Figure 32: I²C burst write format

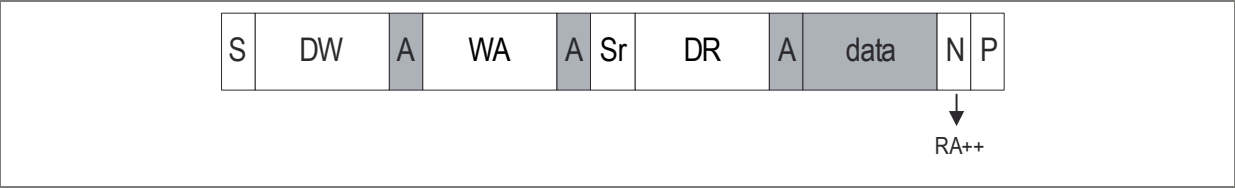


The transmission begins with the START condition, which is generated by the master when the bus is in an IDLE state (the bus is free). The device-write address is followed by the word address. After the word address, any number of data bytes can be sent to the slave. The word address is incremented internally to write subsequent data bytes on subsequent address locations.

7.7.3.4 I²C read

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address or with a new transmission START followed by the device-read address when the bus is in an IDLE state. The device-read address is always followed by the first register byte transmitted from the slave. In Read mode, any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

Figure 33: I²C random read format

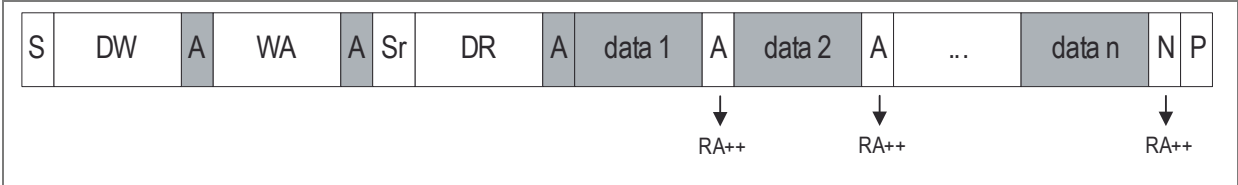


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

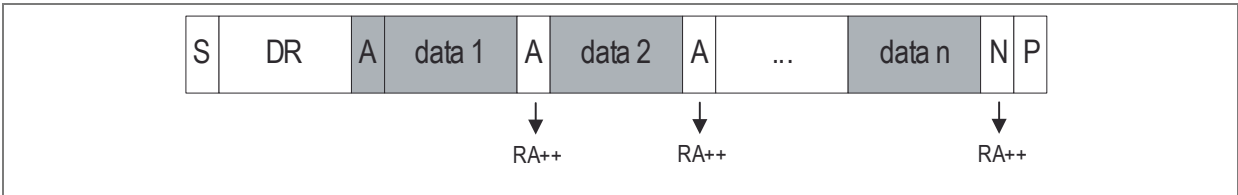
To change the data direction, a repeated START condition is issued on the first SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state, the slave transmits register data located by the previously received word address vector. The master responds to the data byte with a “not-acknowledge” and issues a STOP condition on the bus.

Figure 34: I²C sequential read format



Sequential Read is the extended form of Random Read, as more than one register-data byte is subsequently transferred. In contrast to the Random Read, an acknowledge from the master is the response for the transferred register-data bytes for a sequential read. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission, the master must send a “not-acknowledge” following the last data byte and subsequently generate the STOP condition.

Figure 35: I²C current address read format

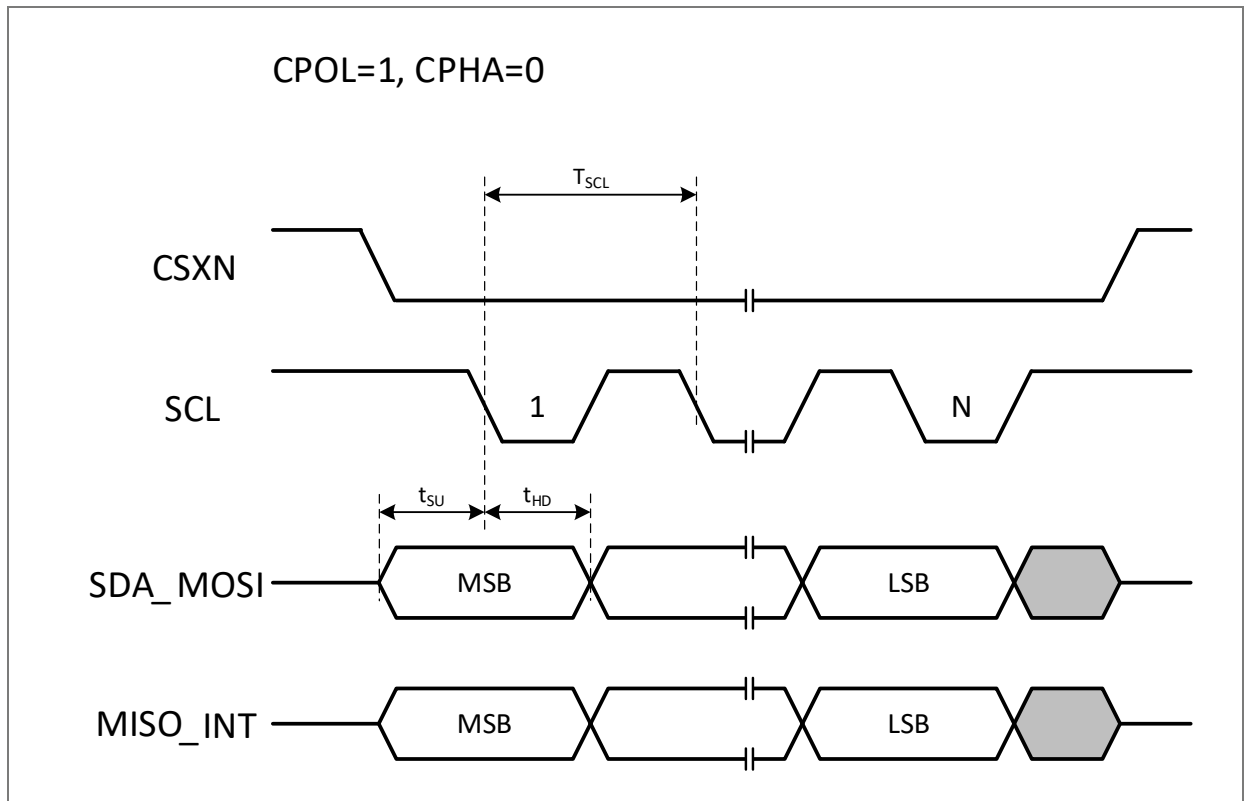


To keep the access time as small as possible, this format allows read access without the word address transfer in advance of the data transfer. The bus is idle, and the master issues a START condition, followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a “not-acknowledge” after the first register byte. Analogous to Sequential Read, an unlimited number of data bytes can be transferred – where an acknowledge from the master must be the response to the data bytes. For termination of the transmission, the master sends a “not-acknowledge” following the last data byte and a subsequent STOP condition.

7.7.3.5 SPI

SPI mode should be used: CPOL = 1, CPHA = 0 (see Figure 36).

Figure 36: SPI timing



SPI access protocols:

- Single Write RW=0, Address, Write Data Byte
- Single Read RW=1, Address, Read Data Byte
- Burst Read RW=1, Address, Read n Data Byte

Figure 37: SPI single access with address space of 256 Byte

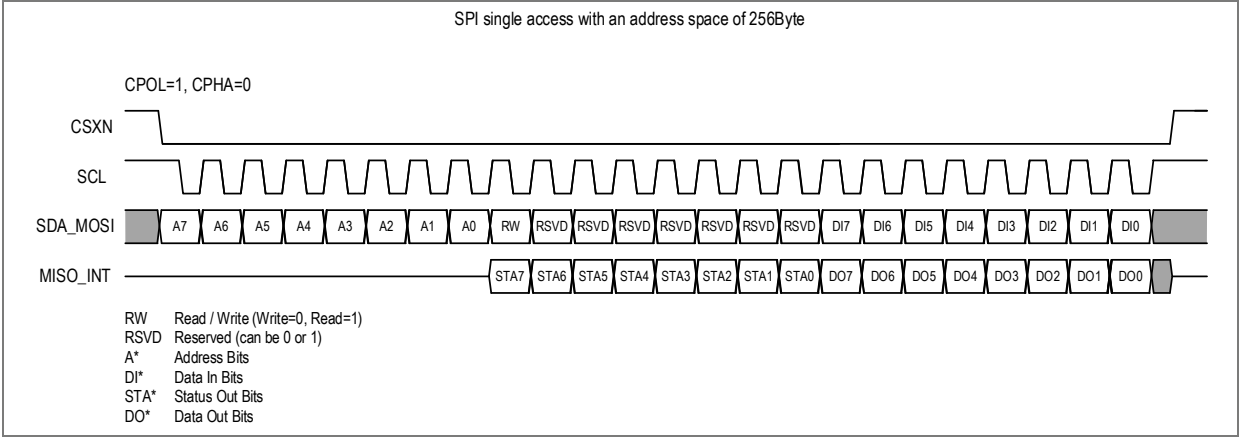
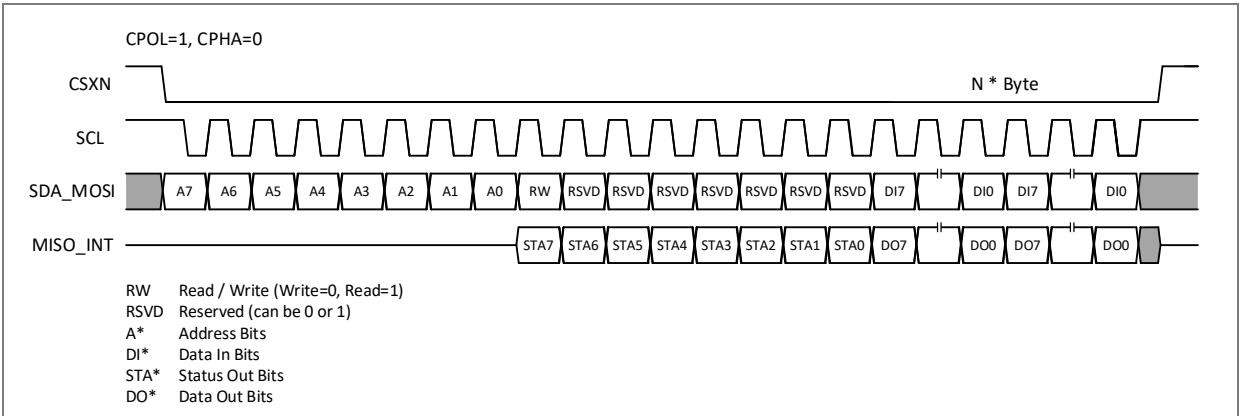


Figure 38: SPI burst access with address space of 256 Byte

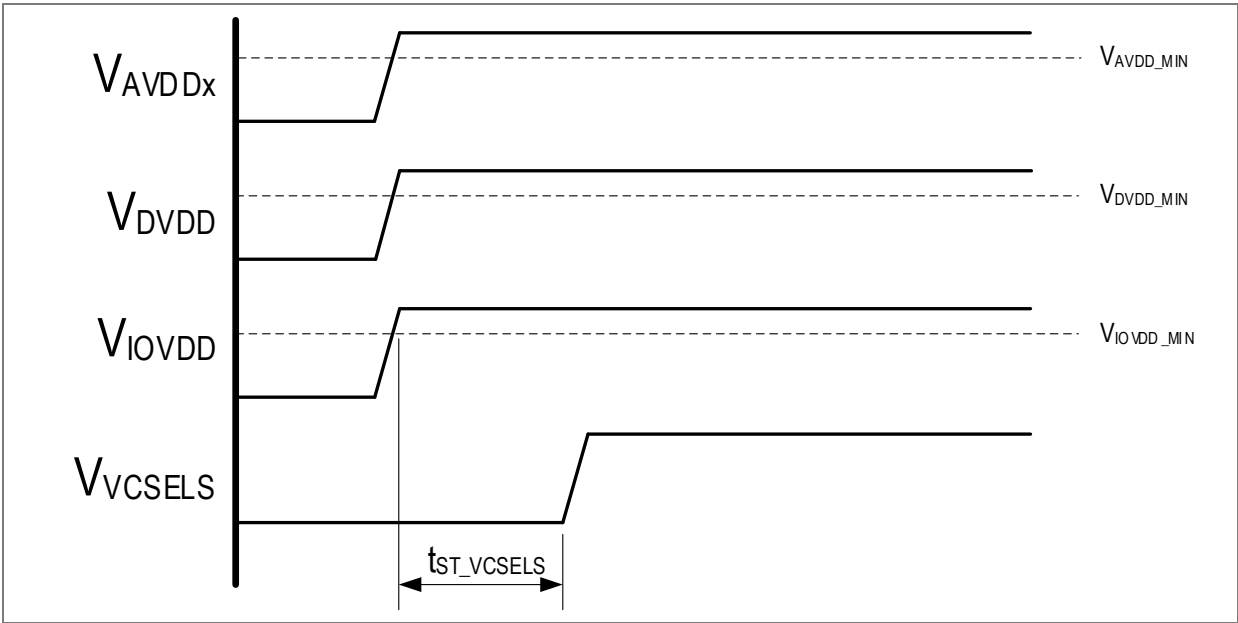


If a clock rate other than $n \cdot 8$ clocks is detected during data transmission in SPI mode, an error is displayed in the SPI status register.

7.8 Startup information

To guarantee proper startup of AS7160 it is recommended to follow a defined startup timing of the power supply reels. It is important that V_{VCSELS} supply voltage is delayed compared to V_{DVDD} , V_{AVDD} and V_{IOVDD} supply voltage like it is shown in Figure 39. However, if the suggested timing cannot be fulfilled and all supply voltages do start in parallel ($t_{ST_VCSELS}=0$ ms) this is supported with the drawback that the connected LEDs might light up for a short period of time during the very first startup of the device until all supplies are settled. If this behavior is acceptable, all supplies can start up in parallel.

Figure 39: AS7160 startup timing diagram



7.8.1 Parameter

Table 14: Startup timing parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ST_VCSELS}	Startup delay VLED supply voltage		0	1		ms

7.9 Standby mode

AS7160 supports standby operation mode to reduce overall power consumption during the pause times while no measurement is ongoing. Especially at very low sample rates standby mode helps to reduce system power consumption to extend the battery lifetime of a device. The standby mode function is controlled with up to 7 different standby mode enable control signals. Each of the seven standby enable signals control a dedicated hardware block of AS7160. An overview of the control signals is shown in Table 15 below. Furthermore, it contains information about the related blocks which are necessary for a certain application. The standby function and the block to be controlled in standby mode are enabled via **STANDBY_ON1** register. In addition to the enable registers each Standby Enable signal is also connected to a dedicated timing register to define the standby startup timing of the functional block. A simplified timing diagram of all Standby Enable signals is shown in Figure 40.

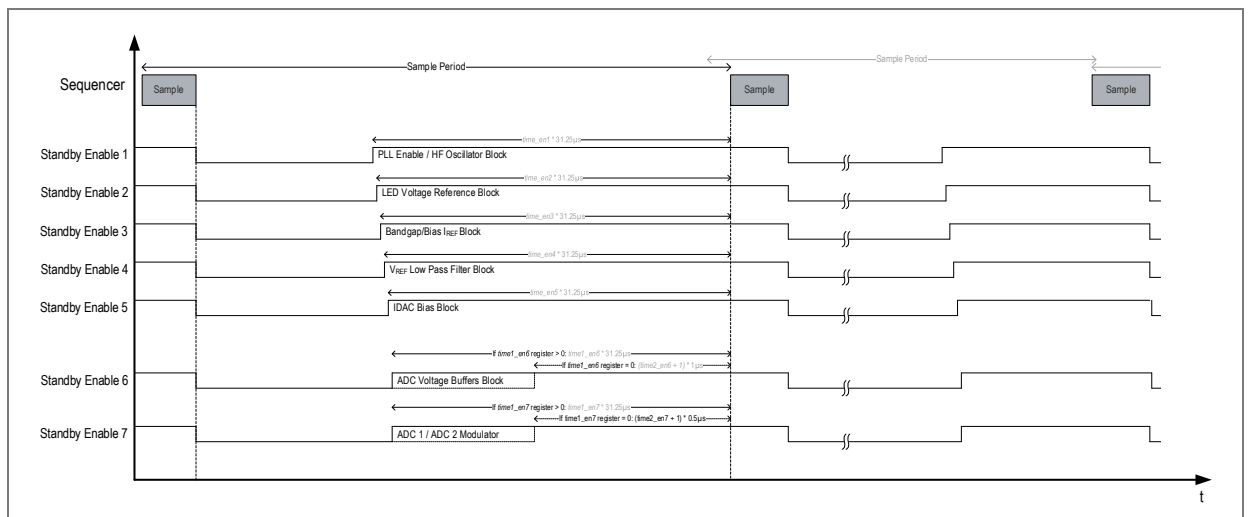
Table 15: Standby mode control signal overview

Standby control signal	Function	Timing control registers
Standby enable 1	Controls and enables the internal PLL and high frequency oscillator	<i>time_en1</i>
Standby enable 2	Controls and enables voltage reference for the LED drivers	<i>time_en2</i>
Standby enable 3	Controls and enables on chip bandgap and bias reference current	<i>time_en3</i>
Standby enable 4	Controls and enables the bypass functions of the low pass filter	<i>time_en4</i>
Standby enable 5	Controls and enables the bias voltage block of the current DAC	<i>time_en5</i>
Standby enable 6	Controls and enables the common mode voltage buffer	<i>time1_en6</i> <i>time2_en6</i>
Standby enable 7	Controls and enables the modulators	<i>time1_en7</i> <i>time2_en7</i>

The timings which are defined in the timing registers for each control signal define the start of a block prior to the actual measurement start. The timing registers allow for exact control of the startup timing behavior of all relevant blocks and it makes sure that all system blocks are active and properly settled when a measurement is started. Right after the measurement is finished and the measurement data is written to the FIFO memory of AS7160 all Standby Enable signals are disabled again and the connected blocks are powered down. Important to mention is that Standby Enable 1 – Standby Enable 5 signals do have only one timing control register (*time_enX*). Each register is linked to the 32 kHz clock domain of the device which results into a 31.25 μ s multiplication factor for these registers like it is also indicated in Figure 40. The Standby Enable 6 and Standby Enable 7 control signals have two timing control registers. The *time1_enX* timing registers are also linked to the 32 kHz clock domain of the device which results into a 31.25 μ s multiplication factor for these registers.

The second timing control register *time2_enX* which is also linked to each of the Standby Enable 6 and Standby Enable 7 registers is connected to the 2 MHz clock domain of AS7160 which results in a 1 μ s multiplication factor for these registers. Only one of the two-timing registers for a Standby Enable signal can be active at a time and the priority is controlled with the register content. In case a value greater than zero is written to *time1_enX* register the register content of *time2_enX* register is ignored and the timing is calculated and executed based on the register content of *time1_enX* register. In case the *time1_enX* register is set to zero, the content of register *time2_enX* is used for the Standby Enable signal timing based on the 1 μ s clock domain.

Figure 40: Standby enable signal timing diagram



8 Register description

8.1 Register overview

Table 16: Register overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>	
OTP										
0x15	P2RAM_OTP_21	temp_adc_ref[7:0]								
0x16	P2RAM_OTP_22	temp_adc_ref[15:8]								
POWER										
0x18	CLK_CFG			sel_extclk			pll_on	hf_osc_on	lf_osc_on	
0x19	REF_CFG1			sel_vcm	en_bg	en_vcm	en_vr_le d	en_bia s_iref	en_bias_i dac	
0x1a	REF_CFG2				en_vtem p				byp_ref_lp	
0x1b	REF_CFG3	sel_vcm_adc						sel_vcm_sw		
0x1c	STANDBY_ON1	stby_en_on[7:0]								
0x1d	STANDBY_ON2			stby_en_on[13:8]						
0x1e	STANDBY_EN1	stby_en1_time								
0x1f	STANDBY_EN2	stby_en2_time								
0x20	STANDBY_EN3	stby_en3_time								
0x21	STANDBY_EN4	stby_en4_time								
0x22	STANDBY_EN5	stby_en5_time								
0x23	STANDBY_EN6	stby_en6_time1				stby_en6_time2				
0x24	STANDBY_EN7	stby_en7_time1				stby_en7_time2				
0x2d	PWR_ON				pwr_on					
0x2e	PWR_ISO				pwr_iso					
0x2f	PWR_STAT				pwr_stat					
CONTROL										
0x31	I2C_MODE								i2c_fm_pl us	
0x32	INT_CFG			int_inv	int_e2	int_e4	reserved	int_pu	int_pd	
0x33	IF_CFG	sda_e2	sda_e4	reserved	miso_e2	miso_e4	reserved	csxn_p u	csxn_pd	
0x34	GPIO_CFG1	gpio_inv	gpio_oe n	reserved	gpio_e2	gpio_e4	reserved	gpio_p u	gpio_pd	
0x35	GPIO_CFG2						gpio_pinmap_sel			
0x36	IO_CFG							extclk_ pu	extclk_pd	

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
ADC MODULATOR									
0x37	MOD_CFG1							mod_opamp_ibias	
0x39	MOD_CFG3				mod_reset_delay			mod_clk	
0x3a	MOD1_CFG1	mod1_en	mod1_ios_mux	mod1_dsm_amp	mod1_cint				
0x3b	MOD1_CFG2	mod1_ios_dir	mod1_ios_fs		mod1_iref_scale				
0x3c	MOD1_CFG3	mod1_iref							
0x3d	MOD2_CFG1	mod2_en	mod2_ios_mux	mod2_dsm_amp	mod2_cint				
0x3e	MOD2_CFG2	mod2_ios_dir	mod2_ios_fs		mod2_iref_scale				
0x3f	MOD2_CFG3	mod2_iref							
LED DRIVER									
0x40	VCSEL_PASSWORD							vcsel_password	
0x41	VCSEL_CFG	vcsel_wd_disable	vcsel_safety_disable	vcsel_vrsel		vcsel_short_vdd_wait		vcsel_short_vss_wait	
0x42	VCSEL_MODE	vcsel_mode							
0x43	LED_CFG							led_wd_disable	
0x44	LED_DRV1				drv1_fas_t_tr	drv1_bias			
0x45	LED_DRV2				drv2_fas_t_tr	drv2_bias			
0x46	LED1_ICTRL	led1_ictrl							
0x47	LED2_ICTRL	led2_ictrl							
0x48	LED3_ICTRL	led3_ictrl							
0x49	LED4_ICTRL	led4_ictrl							
0x4a	LED5_ICTRL	led5_ictrl							
0x4b	LED6_ICTRL	led6_ictrl							
0x4c	LED7_ICTRL	led7_ictrl							
0x4d	LED8_ICTRL	led8_ictrl							
0x4e	LED_IRNG1	led4_irng		led3_irng		led2_irng		led1_irng	
0x4f	LED_IRNG2	led8_irng		led7_irng		led6_irng		led5_irng	
0x50	LED_SUB1		sub1_drv2_sel				sub1_drv1_sel		
0x51	LED_SUB2		sub2_drv2_sel				sub2_drv1_sel		
0x52	LED_SUB3		sub3_drv2_sel				sub3_drv1_sel		
0x53	LED_SUB4		sub4_drv2_sel				sub4_drv1_sel		
0x54	LED_SUB5		sub5_drv2_sel				sub5_drv1_sel		
0x55	LED_SUB6		sub6_drv2_sel				sub6_drv1_sel		
0x56	LED_SUB7		sub7_drv2_sel				sub7_drv1_sel		

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x57	LED_SUB8			sub8_drv2_sel				sub8_drv1_sel	
0x58	LOWVDS_WAIT				lowvds_wait				
PHOTODIODES									
0x59	PDSEL_CFG								pdref_sel
0x5a	MOD1_PDSEL1				mod1_pdsel_sub1				
0x5b	MOD1_PDSEL2				mod1_pdsel_sub2				
0x5c	MOD1_PDSEL3				mod1_pdsel_sub3				
0x5d	MOD1_PDSEL4				mod1_pdsel_sub4				
0x5e	MOD1_PDSEL5				mod1_pdsel_sub5				
0x5f	MOD1_PDSEL6				mod1_pdsel_sub6				
0x60	MOD1_PDSEL7				mod1_pdsel_sub7				
0x61	MOD1_PDSEL8				mod1_pdsel_sub8				
0x62	MOD2_PDSEL1				mod2_pdsel_sub1				
0x63	MOD2_PDSEL2				mod2_pdsel_sub2				
0x64	MOD2_PDSEL3				mod2_pdsel_sub3				
0x65	MOD2_PDSEL4				mod2_pdsel_sub4				
0x66	MOD2_PDSEL5				mod2_pdsel_sub5				
0x67	MOD2_PDSEL6				mod2_pdsel_sub6				
0x68	MOD2_PDSEL7				mod2_pdsel_sub7				
0x69	MOD2_PDSEL8				mod2_pdsel_sub8				
0x6a	MOD2_AFESEL1			mod2_afesel_sub2			mod2_afesel_sub1		
0x6b	MOD2_AFESEL2			mod2_afesel_sub4			mod2_afesel_sub3		
0x6c	MOD2_AFESEL3			mod2_afesel_sub6			mod2_afesel_sub5		
0x6d	MOD2_AFESEL4			mod2_afesel_sub8			mod2_afesel_sub7		
0x6e	MOD2_AFEEN				mod2_afe_en				
SINC FILTER									
0x6f	SINC_CFGA				sinc_ovs			sinc_dec	
0x70	SINC_CFGB				os_delay		comb_dly_en	sel_order	filter_mode
0x71	SINC_CFGC				start_delay				
0x72	SINC_CFGD			mod1_sinc_smd			mod2_sinc_smd		
PHOTODIODE OFFSET									
0x7a	IOS_MOD1_SUB1				ios_mod1_sub1				
0x7b	IOS_MOD1_SUB2				ios_mod1_sub2				
0x7c	IOS_MOD1_SUB3				ios_mod1_sub3				
0x7d	IOS_MOD1_SUB4				ios_mod1_sub4				
0x7e	IOS_MOD1_SUB5				ios_mod1_sub5				
0x7f	IOS_MOD1_SUB6				ios_mod1_sub6				
0x80	IOS_MOD1_SUB7				ios_mod1_sub7				

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x81	IOS_MOD1_SUB8				ios_mod1_sub8				
0x82	IOS_MOD2_SUB1				ios_mod2_sub1				
0x83	IOS_MOD2_SUB2				ios_mod2_sub2				
0x84	IOS_MOD2_SUB3				ios_mod2_sub3				
0x85	IOS_MOD2_SUB4				ios_mod2_sub4				
0x86	IOS_MOD2_SUB5				ios_mod2_sub5				
0x87	IOS_MOD2_SUB6				ios_mod2_sub6				
0x88	IOS_MOD2_SUB7				ios_mod2_sub7				
0x89	IOS_MOD2_SUB8				ios_mod2_sub8				
0x8a	IOS_LEDOFF				ios_ledoff				
0x8b	IOS_CFG								dis_ledoff
AAOC									
0x8c	AOC_SAR_THRES				sar_thres				
0x8d	AOC_SAR_RANGE				sar_range_en		sar_range		
0x8e	AOC_SAR_MOD1				sar_mod1_en				
0x8f	AOC_SAR_MOD2				sar_mod2_en				
POST PROCESSING									
0x90	PP_CFG				asat_on		asat_fil		
0x91	MOD1_PP1	mod1_pp_sub4		mod1_pp_sub3		mod1_pp_sub2		mod1_pp_sub1	
0x92	MOD1_PP2	mod1_pp_sub8		mod1_pp_sub7		mod1_pp_sub6		mod1_pp_sub5	
0x93	MOD2_PP1	mod2_pp_sub4		mod2_pp_sub3		mod2_pp_sub2		mod2_pp_sub1	
0x94	MOD2_PP2	mod2_pp_sub8		mod2_pp_sub7		mod2_pp_sub6		mod2_pp_sub5	
0x95	IRQ_ENABLE	irq_en_iir_overflow	irq_en_ledoff	irq_en_vcsel	irq_en_asat	irq_en_led_lowvds	irq_en_fifooverflow	irq_en_fifothreshold	irq_en_sequencer
SEQUENCER									
0x96	SUB_WAIT				sub_wait				
0x97	SAR_WAIT				sar_wait				
0x98	LED_INIT				led_init				
0x99	FREQ_L				freq[7:0]				
0x9a	FREQ_H				freq[15:8]				
0x9b	MOD1_SUB_EN				mod1_sub_en				
0x9c	MOD2_SUB_EN				mod2_sub_en				
0x9d	MODE1						mode_sub1		
0x9e	MODE2						mode_sub2		
0x9f	MODE3						mode_sub3		
0xa0	MODE4						mode_sub4		
0xa1	MODE5						mode_sub5		

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0xa2	MODE6						mode_sub6		
0xa3	MODE7						mode_sub7		
0xa4	MODE8						mode_sub8		
0xa5	CFG					ext_freq	moving_aver- age_on	moving_average_val	
0xb1	SAMPLE_NUM				sample_num				
FIFO									
0xca	FIFO_THRESHOLD				fifo_threshold[7:0]				
0xcb	FIFO_CTRL	fifo_clea- r				seq_syn- c_en	sinc_ran- dext_en	sar_da- ta_en	fifo_thresh- old[8]
MISCELLANEOUS									
0xeb	PRODUCT_ID				otp_part_id				
0xec	SILICON_ID				silicon_id				
0xee	GPIO_CTRL							gpio_in	gpio_out
0xef	CHIP_CTRL							wd_res- et	chip_reset
0xf0	SEQ_START								start_seq
0xf1	STATUS_CGB							pll_loc- k	clk_pll_ok
0xf2	STATUS_SEQ							seq_e- nd	seq_error
0xf3	STATUS_LED				led_lowvds				
0xf4	STATUS_ASATA		mod1_asat				mod2_asat		
0xf5	STATUS_ASATB						mod3_asat		
0xf6	STATUS_VCSEL				led_wd	vcsel_vs- s	vcsel_vd- d		vcsel_wd
0xf7	STATUS_VCSEL_VSS				vcsel_short_vss				
0xf8	STATUS_VCSEL_VDD				vcsel_short_vdd				
0xfa	STATUS	irq_iir_o- verflow	irq_lead- off	irq_vcsel	irq_asat	irq_led_l- owvds	irq_fifo- verflow	irq_fifo- thresh- old	irq_seque- ncer
0xfb	FIFO_LEVEL0				fifo_level[7:0]				
0xfc	FIFO_LEVEL1						fifo_over- flow	fifo_level[9:8]	
0xfd	FIFOL				fifol				
0xfe	FIFOM				fifom				
0xff	FIFOH				fifoh				

8.2 OTP

The register tables store the percentage error of the internal resistors with the following structure:

- 1-bit for the sign
- 5 bits for the integer number with 1% per code such that the range is $\pm 31\%$
- 4 bits for the decimal number with 0.06% per code

8.2.1 P2RAM_OTP_21 register (Address 0x15)

Table 17: P2RAM_OTP_21 register

Addr: 0x15		P2RAM_OTP_21		
Bit	Bit name	Default	Access	Bit description
7:0	<i>temp_adc_ref[7:0]</i>	0	R	Temperature reference ADC LSBs

8.2.2 P2RAM_OTP_22 register (Address 0x16)

Table 18: P2RAM_OTP_22 register

Addr: 0x16		P2RAM_OTP_22		
Bit	Bit name	Default	Access	Bit description
7:0	<i>temp_adc_ref[15:8]</i>	0	R	Temperature reference ADC MSBs

8.3 Power

8.3.1 CLK_CFG register (Address 0x18)

Table 19: CLK_CFG register

Addr: 0x18		CLK_CFG		
Bit	Bit name	Default	Access	Bit description
5:4	<i>sel_extclk</i>	0	RW	Selection of external clock 2 MHz or 4 MHz. 00: Internal HF_OSC (2 MHz) selected 10: External 2 MHz clock selected 11: External 4 MHz clock selected
2	<i>pll_on</i>	0	RW	Switching on the 20 MHz PLL. 0: Disable 1: Enable
1	<i>hf_osc_on</i>	0	RW	Switching on the 2 MHz Oscillator. The oscillator is the source for the 20 MHz PLL. 0: Disable 1: Enable
0	<i>lf_osc_on</i>	0	RW	Switching on the 32 kHz Oscillator. 0: Disable 1: Enable

8.3.2 REF_CFG1 register (Address 0x19)

Table 20: REF_CFG1 register

Addr: 0x19		REF_CFG1		
Bit	Bit name	Default	Access	Bit description
5	<i>sel_vcm</i>	0	RW	Selection of the common mode voltage. 0: VCM = 0.75 V 1: VCM = 0.8 V
4	<i>en_bg</i>	0	RW	Enable the bandgap. 0: Power down 1: Enabled
3	<i>en_vcm</i>	0	RW	Enable the common-mode voltage reference. 0: Power down 1: Enabled
2	<i>en_vr_led</i>	0	RW	Enable the LED driver voltage reference. 0: Power down 1: Enabled
1	<i>en_bias_iref</i>	0	RW	Enable the current reference source. 0: Power down 1: Enabled
0	<i>en_bias_idac</i>	0	RW	Enable IOS DAC and IREF DAC. 0: Disabled 1: Enabled

8.3.3 REF_CFG2 register (Address 0x1a)

Table 21: REF_CFG2 register

Addr: 0x1a		REF_CFG2		
Bit	Bit name	Default	Access	Bit description
4	<i>en_vtemp</i>	0	RW	Enable internal temperature sensor. 0: Power down 1: Enabled
0	<i>byp_ref_lp</i>	1	RW	The bypass of the low-pass filter for the Reference and VCM. 0: Not bypassed 1: Bypassed

8.3.4 REF_CFG3 register (Address 0x1b)

Table 22: REF_CFG3 register

Addr: 0x1b		REF_CFG3		
Bit	Bit name	Default	Access	Bit description
3:2	<i>sel_vcm_adc</i>	0	RW	Configuration bits for common mode voltage of ADC measurement signal path. Do not change register default register configuration.
1:0	<i>sel_vcm_sw</i>	0	RW	Configuration bits for common mode voltage of ADC measurement signal path. Do not change register default register configuration.

8.3.5 STANDBY_ON1 register (Address 0x1c)

Table 23: STANDBY_ON1 register

Addr: 0x1c		STANDBY_ON1		
Bit	Bit name	Default	Access	Bit description
7:0	<i>stby_en_on[7:0]</i>	0	RW	Set specific Standby registers Enable. 0...7 – Enable 1...8

8.3.6 STANDBY_ON2 register (Address 0x1d)

Table 24: STANDBY_ON2 register

Addr: 0x1d		STANDBY_ON2		
Bit	Bit name	Default	Access	Bit description
5:0	<i>stby_en_on[13:8]</i>	0	RW	Set specific Standby register Enable 9...14 0...5 - Enable 9...14

8.3.7 STANDBY_EN1 register (Address 0x1e)

Table 25: STANDBY_EN1 register

Addr: 0x1e		STANDBY_EN1		
Bit	Bit name	Default	Access	Bit description
7:0	<i>stby_en1_time</i>	4	RW	Time for Enable 1: $N * \text{TCLK_32KHZ}$, $N = 0 \dots 255$

8.3.8 STANDBY_EN2 register (Address 0x1f)

Table 26: STANDBY_EN2 register

Addr: 0x1f		STANDBY_EN2		
Bit	Bit name	Default	Access	Bit description
7:0	<i>stby_en2_time</i>	1	RW	Time for Enable2: $N * \text{TCLK_32KHZ}$, $N = 0 \dots 255$

8.3.9 STANDBY_EN3 register (Address 0x20)

Table 27: STANDBY_EN3 register

Addr: 0x20		STANDBY_EN3		
Bit	Bit name	Default	Access	Bit description
7:0	<i>stby_en3_time</i>	3	RW	Time for Enable3: $N * \text{TCLK_32KHZ}$, $N = 0 \dots 255$

8.3.10 STANDBY_EN4 register (Address 0x21)

Table 28: STANDBY_EN4 register

Addr: 0x21		STANDBY_EN4		
Bit	Bit name	Default	Access	Bit description
7:0	<i>stby_en4_time</i>	0	RW	Time for Enable4: $N * \text{TCLK_32KHZ}$, $N = 0 \dots 255$

8.3.11 STANDBY_EN5 register (Address 0x22)

Table 29: STANDBY_EN5 register

Addr: 0x22		STANDBY_EN5		
Bit	Bit name	Default	Access	Bit description
7:0	<i>stby_en5_time</i>	1	RW	Time for Enable5: $N * \text{TCLK_32KHZ}$, $N = 0 \dots 255$

8.3.12 STANDBY_EN6 register (Address 0x23)

Table 30: STANDBY_EN6 register

Addr: 0x23		STANDBY_EN6		
Bit	Bit name	Default	Access	Bit description
7:5	<i>stby_en6_time1</i>	0	RW	Time1 for Enable6 0: time2_en6 is active, Others: $(N+1) * \text{TCLK_32KHZ}$, $N = 0 \dots 7$
4:0	<i>stby_en6_time2</i>	16	RW	Time2 for Enable6: $N * \text{TCLK_2MHZ}$, $N = 0 \dots 31$

8.3.13 STANDBY_EN7 register (Address 0x24)

Table 31: STANDBY_EN7 register

Addr: 0x24		STANDBY_EN7		
Bit	Bit name	Default	Access	Bit description
7:5	<i>stby_en7_time1</i>	0	RW	Time1 for Enable7 0: time2_en7 is active, Others: (N+1) * TCLK_32KHZ, N = 0...7
4:0	<i>stby_en7_time2</i>	16	RW	Time2 for Enable7: N * TCLK_2MHZ, N = 0...31

8.3.14 PWR_ON register (Address 0x2d)

Table 32: PWR_ON register

Addr: 0x2d		PWR_ON		
Bit	Bit name	Default	Access	Bit description
3	<i>pwr_on</i>	0	RW	Switching of MOD2 power domain 0: Disable 1: Enable
2		0	RW	Switching of MOD1 power domain 0: Disable 1: Enable
1		0	RW	Switching of CTRL power domain 0: Disable 1: Enable
0		1	RW	Switching of CONF (Configuration) power domain 0: Disable 1: Enable

8.3.15 PWR_ISO register (Address 0x2e)

Table 33: PWR_ISO register

Addr: 0x2e		PWR_ISO		
Bit	Bit name	Default	Access	Bit description
4	<i>pwr_iso</i>	0	RW	Power isolation register bit. It is important that this bit is inverted to the <i>pwr_on</i> register. 0: Disable 1: Enable
3		0	RW	Power isolation register bit. It is important that this bit is inverted to the <i>pwr_on</i> register. 0: Disable 1: Enable
2		0	RW	Power isolation register bit. It is important that this bit is inverted to the <i>pwr_on</i> register. 0: Disable 1: Enable
1		0	RW	CTRL power isolation register bit. It is important that this bit is inverted to the <i>pwr_on</i> register. 0: Disable 1: Enable
0		1	RW	CONF power isolation register bit. It is important that this bit is inverted to the <i>pwr_on</i> register. 0: Disable 1: Enable

8.3.16 PWR_STAT register (Address 0x2f)

Table 34: PWR_STAT register

Addr: 0x2f		PWR_STAT		
Bit	Bit name	Default	Access	Bit description
3	<i>pwr_stat</i>	0	RO	ADC2
2		0	RO	ADC1
1		0	RO	CTRL
0		1	RO	CONF

8.4 Control

8.4.1 I2C_MODE register (Address 0x31)

Table 35: I2C_MODE register

Addr: 0x31		I2C_MODE		
Bit	Bit name	Default	Access	Bit description
0	<i>i2c_fm_plus</i>	0	RW	This register bit enables I ² C fast mode plus with 1 MHz I ² C clock speed. This register must not be written during burst mode. Only single write is possible. 0: I ² C Fast Mode Plus Disabled 1: I ² C Fast Mode Plus Enabled

8.4.2 INT_CFG register (Address 0x32)

Table 36: INT_CFG register

Addr: 0x32		INT_CFG		
Bit	Bit name	Default	Access	Bit description
5	<i>int_inv</i>	0	RW	Inverting interrupt.
4	<i>int_e2</i>	0	RW	Set the output driver strength high with 1.
3	<i>int_e4</i>	0	RW	Set the output driver strength high again with 1.
2	<i>reserved</i>	0	RW	Reserved system register. Do not change default register value.
1	<i>int_pu</i>	0	RW	PU = 1 -> pull-up at INT pin
0	<i>int_pd</i>	0	RW	PD = 1 -> pull-down at INT pin

8.4.3 IF_CFG register (Address 0x33)

Table 37: IF_CFG register

Addr: 0x33		IF_CFG		
Bit	Bit name	Default	Access	Bit description
7	<i>sda_e2</i>	0	RW	Set the output driver strength high with 1.
6	<i>sda_e4</i>	1	RW	Set the output driver strength high again with 1.
5	<i>reserved</i>	0	RW	Reserved system register. Do not change default register value.
4	<i>miso_e2</i>	0	RW	Set the output driver strength high with 1.
3	<i>miso_e4</i>	1	RW	Set the output driver strength high again with 1.
2	<i>reserved</i>	0	RW	Reserved system register. Do not change default register value.
1	<i>csxn_pu</i>	0	RW	PU = 1 -> pull-up at CSXN pin
0	<i>csxn_pd</i>	0	RW	PD = 1 -> pull-down at CSXN pin

8.4.4 GPIO_CFG1 (Address 0x34)

Table 38: GPIO_CFG1 register

Addr: 0x34		GPIO_CFG1		
Bit	Bit name	Default	Access	Bit description
7	<i>gpio_inv</i>	0	RW	Inverting the Output of the GPIO.
6	<i>gpio_oen</i>	0	RW	Output Enable of the GPIO.
5	<i>reserved</i>	0	RW	Reserved system register. Do not change default register value.
4	<i>gpio_e2</i>	0	RW	Set the output driver strength high with 1.
3	<i>gpio_e4</i>	0	RW	Set the output driver strength high again with 1.
2	<i>reserved</i>	0	RW	Reserved system register. Do not change default register value.
1	<i>gpio_pu</i>	0	RW	PU = 1 -> pull-up at GPIO pin
0	<i>gpio_pd</i>	0	RW	PD = 1 -> pull-down at GPIO pin

8.4.5 GPIO_CFG2 (Address 0x35)

Table 39: GPIO_CFG2 register

Addr: 0x35		GPIO_CFG2		
Bit	Bit name	Default	Access	Bit description
2:0	<i>gpio_pinmap_sel</i>	0	RW	Pinmap multiplexer for GPIO. If <i>gpio_oen</i> = 1, select the signal which is driven to the GPIO. 0: <i>gpio_out</i> 1: <i>led_on</i> 2: <i>standby_en5</i> 3: 0 Others: Reserved

8.4.6 IO_CFG (Address 0x36)

Table 40: IO_CFG register

Addr: 0x36		IO_CFG		
Bit	Bit name	Default	Access	Bit description
1	<i>extclk_pu</i>	0	RW	PU = 1 -> pull-up at EXTCLK_SYNC pin
0	<i>extclk_pd</i>	0	RW	PD = 1 -> pull-down at EXTCLK_SYNC pin

8.5 ADC modulator

8.5.1 MOD_CFG1 (Address 0x37)

Table 41: MOD_CFG1 register

Addr: 0x37		MOD_CFG1		
Bit	Bit name	Default	Access	Bit description
1:0	<i>mod_opamp_ibias</i>	0	RW	This register changes the ADC OPAMP bias current scaling. Please do not change this register. 0: x1 current scaling factor 1: x1.25 current scaling factor 2: x0.5 current scaling factor 3: x0.75 current scaling factor

8.5.2 MOD_CFG3 (Address 0x39)

Table 42: MOD_CFG3 register

Addr: 0x39		MOD_CFG3		
Bit	Bit name	Default	Access	Bit description
4:2	<i>mod_reset_delay</i>	0	RW	This register controls the ADC modulator reset delay for all modulators $t_{MOD_RES} = 2^{(N+2)} / f_{MOD_CLK}$ with $N = 0 \dots 7$. The modulator clock frequency f_{MOD_CLK} can be controlled with <i>mod_clk</i> register and is in default configuration 10 MHz.
1:0	<i>mod_clk</i>	0	RW	This register controls the modulator clock frequency f_{MOD_CLK}. Sequencer 1 and Sequencer 2 use the same modulator frequency. 0: 10 MHz 1: 5 MHz 2: 2.5 MHz 3: 1.25 MHz

8.5.3 MOD1_CFG1 (Address 0x3a)

Table 43: MOD1_CFG1 register

Addr: 0x3a		MOD1_CFG1		
Bit	Bit name	Default	Access	Bit description
7	<i>mod1_en</i>	0	RW	Enable Modulator1 0: Off 1: On
6	<i>mod1_ios_mux</i>	0	RW	Multiplex IOS DAC2 to modulator 1 for the calibration. 0: IOS DAC to MOD1 1: IOS DAC to MOD2 if mod1_ios_dir = 1
5	<i>mod1_dsm_ampl</i>	0	RW	This bit enables the DSM integrator scaling function. Please do not write this register and keep it at its default value.
4:0	<i>mod1_cint</i>	0	RW	This register controls the integrator capacitor value. Please do not change register unless instructed by ams OSRAM support team. The ams OSRAM support team provides different configuration values depending on the selected full scale range of the ADC modulator. 0: 1 pF 1: 2 pF 30: 31 pF 31: 32 pF

8.5.4 MOD1_CFG2 (Address 0x3b)

Table 44: MOD1_CFG2 register

Addr: 0x3b		MOD1_CFG2		
Bit	Bit name	Default	Access	Bit description
7	<i>mod1_ios_dir</i>	0	RW	Offset DAC current direction 0: PMOS (Ambient Light Cancellation) PD Current - PD Offset Current 1: NMOS (Special Mode) PD Current + PD Offset Current
6:4	<i>mod1_ios_fs</i>	0	RW	Offset DAC Full-Scale Current 0: 1 μ A 1: 2 μ A 2: 4 μ A 3: 8 μ A 4: 16 μ A 5: 32 μ A 6: 64 μ A 7: 128 μ A
3:0	<i>mod1_iref_scale</i>	0	RW	This is the current reference scale factor for modulator 1 photodiode offset DAC. Default reset value of the register is 0, however it is recommended to use 0.625 scale factor for measurements. 0: 0.125 1: 0.250 2: 0.375 3: 0.500 4: 0.625 5: 0.750 6: 0.875 7: 1.000 8-15: Do not use.

8.5.5 MOD1_CFG3 (Address 0x3c)

Table 45: MOD1_CFG3 register

Addr: 0x3c		MOD1_CFG3		
Bit	Bit name	Default	Access	Bit description
7:0	<i>mod1_iref</i>	0	RW	This register defines an internal current reference value. Please do not change register unless instructed by ams OSRAM support team. The ams OSRAM support team provides different configuration values depending on the selected full scale range of ADC modulator. 0: 1 μA 1: 2 μA 63: 64 μA 64-255: Do not use

8.5.6 MOD2_CFG1 (Address 0x3d)

Table 46: MOD2_CFG1 register

Addr: 0x3d		MOD2_CFG1		
Bit	Bit name	Default	Access	Bit description
7	<i>mod2_en</i>	0	RW	Enable Modulator1 0: Off 1: On
6	<i>mod2_ios_mux</i>	0	RW	Multiplex IOS DAC2 to modulator 1 for calibration. 0: IOS DAC to MOD1 1: IOS DAC to MOD2 if <i>mod1_ios_dir</i> = 1
5	<i>mod2_dsm_ampl</i>	0	RW	This bit enables the DSM integrator scaling function. Please do not write this register and keep it at its default value.
4:0	<i>mod2_cint</i>	0	RW	This register controls the integrator capacitor value. Please do not change register unless instructed by ams OSRAM support team. The ams OSRAM support team provides different configuration values depending on the selected full scale range of ADC modulator. 0: 1 pF 1: 2 pF 30: 31 pF 31: 32 pF

8.5.7 MOD2_CFG2 (Address 0x3e)

Table 47: MOD2_CFG2 register

Addr: 0x3e		MOD2_CFG2		
Bit	Bit name	Default	Access	Bit description
7	<i>mod2_ios_dir</i>	0	RW	Offset DAC current direction 0: PMOS (Ambient Light Cancellation) PD Current - PD Offset Current 1: NMOS (Special Mode) PD Current + PD Offset Current
6:4	<i>mod2_ios_fs</i>	0	RW	Offset DAC Full-Scale Current 0: 1 μ A 1: 2 μ A 2: 4 μ A 3: 8 μ A 4: 16 μ A 5: 32 μ A 6: 64 μ A 7: 128 μ A
3:0	<i>mod2_iref_scale</i>	0	RW	This is the current reference scale factor for modulator 2 photodiode offset DAC. Default reset value of the register is 0, however it is recommended to use 0.625 scale factor for measurements. 0: 0.125 1: 0.250 2: 0.375 3: 0.500 4: 0.625 5: 0.750 6: 0.875 7: 1.000 8-15: Do not use.

8.5.8 MOD2_CFG3 (Address 0x3f)

Table 48: MOD2_CFG3 register

Addr: 0x3f		MOD2_CFG3		
Bit	Bit name	Default	Access	Bit description
7:0	<i>mod2_iref</i>	0	RW	This register defines an internal current reference value. Please do not change register unless instructed by ams OSRAM support team. The ams OSRAM support team provides different configuration values depending on the selected full scale range of ADC modulator. 0: 1 μA 1: 2 μA 63: 64 μA 64-255: Do not use

8.6 LED driver

8.6.1 VCSEL_PASSWORD (Address 0x40)

Table 49: VCSEL_PASSWORD register

Addr: 0x40		VCSEL_PASSWORD		
Bit	Bit name	Default	Access	Bit description
0	<i>vcsel_password</i>	0	RO	Writing Value = 0x57 to this Register address sets the <i>vcsel_password</i> = 1'b1. Writing other Values to this Register address sets the <i>vcsel_password</i> = 1'b0. Only <i>vcsel_password</i> can be read.

8.6.2 VCSEL_CFG (Address 0x41)

Table 50: VCSEL_CFG register

Addr: 0x41		VCSEL_CFG		
Bit	Bit name	Default	Access	Bit description
7	<i>vcsel_wd_disable</i>	0	RW	Disable VCSEL Watchdog 0: Watchdog active 1: Watchdog inactive
6	<i>vcsel_safety_disable</i>	0	RW	Disable the safety control logic evaluation of the short to the VSS/VDD signals. 0: Safety logic active 1: Safety logic inactive
5:4	<i>vcsel_vrsel</i>	0	RW	Selection of the reference voltage for short to VDD comparators. 0: 50 mV 1: 100 mV 2: 150 mV 3: 200 mV
3:2	<i>vcsel_short_vdd_wait</i>	0	RW	The <i>vcsel_t_short_vdd_wait</i> defines the time between switching on Short detection and a valid result. All the VCSEL LEDs use the same time. 0: 2 μ s 1: 4 μ s 2: 8 μ s 3: 12 μ s
1:0	<i>vcsel_short_vss_wait</i>	0	RW	The <i>vcsel_t_short_vss_wait</i> defines the time between switching on Short detection and a valid result. All the VCSEL LEDs use the same time. 0: 2 μ s 1: 4 μ s 2: 7 μ s 3: 10 μ s

8.6.3 VCSEL_MODE (Address 0x42)

Table 51: VCSEL_MODE register

Addr: 0x42		VCSEL_MODE		
Bit	Bit name	Default	Access	Bit description
7	<i>vcsel_mode</i>	255	RW	Setting mode for LED pin 8. 0: LED mode 1: VCSEL mode
6			RW	Setting mode for LED pin 7, explanation at bit 7.
5			RW	Setting mode for LED pin 6, explanation at bit 7.
4			RW	Setting mode for LED pin 5, explanation at bit 7.
3			RW	Setting mode for LED pin 4, explanation at bit 7.
2			RW	Setting mode for LED pin 3, explanation at bit 7.
1			RW	Setting mode for LED pin 2, explanation at bit 7.
0			RW	Setting mode for LED pin 1, explanation at bit 7.

8.6.4 LED_CFG (Address 0x43)

Table 52: LED_CFG register

Addr: 0x43		LED_CFG		
Bit	Bit name	Default	Access	Bit description
0	<i>led_wd_disable</i>	0	RW	Disable the LED Watchdog 0: Watchdog active 1: Watchdog inactive

8.6.5 LED_DRV1 (Address 0x44)

Table 53: LED_DRV1 register

Addr: 0x44		LED_DRV1		
Bit	Bit name	Default	Access	Bit description
4	<i>drv1_fast_tr</i>	0	RW	Switching time of LED Driver 1 0: Normal switching 1: Fast switching
3:0	<i>drv1_bias</i>	0	RW	Bias current register for LED driver 1. Do not change default register setting.

8.6.6 LED_DRV2 (Address 0x45)

Table 54: LED_DRV2 register

Addr: 0x45		LED_DRV2		
Bit	Bit name	Default	Access	Bit description
4	<i>drv2_fast_tr</i>	0	RW	Switching time of LED Driver 2 0: Normal switching 1: Fast switching
3:0	<i>drv2_bias</i>	0	RW	Bias current register for LED driver 2. Do not change default register setting.

8.6.7 LED1_ICTRL (Address 0x46)

Table 55: LED1_ICTRL register

Addr: 0x46		LED1_ICTRL		
Bit	Bit name	Default	Access	Bit description
7:0	<i>led1_ictrl</i>	0	RW	LED output current control of driver 1 for pin LED1.

8.6.8 LED2_ICTRL (Address 0x47)

Table 56: LED2_ICTRL register

Addr: 0x47		LED2_ICTRL		
Bit	Bit name	Default	Access	Bit description
7:0	<i>led2_ictrl</i>	0	RW	LED output current control of driver 1 for pin LED2.

8.6.9 LED3_ICTRL (Address 0x48)

Table 57: LED3_ICTRL register

Addr: 0x48		LED3_ICTRL		
Bit	Bit name	Default	Access	Bit description
7:0	<i>led3_ictrl</i>	0	RW	LED output current control of driver 1 for pin LED3.

8.6.10 LED4_ICTRL (Address 0x49)

Table 58: LED4_ICTRL register

Addr: 0x49		LED4_ICTRL		
Bit	Bit name	Default	Access	Bit description
7:0	<i>led4_ictrl</i>	0	RW	LED output current control of driver 1 for pin LED4.

8.6.11 LED5_ICTRL (Address 0x4a)

Table 59: LED5_ICTRL register

Addr: 0x4a		LED5_ICTRL		
Bit	Bit name	Default	Access	Bit description
7:0	<i>led5_ictrl</i>	0	RW	LED output current control of driver 2 for pin LED5.

8.6.12 LED6_ICTRL (Address 0x4b)

Table 60: LED6_ICTRL register

Addr: 0x4b		LED6_ICTRL		
Bit	Bit name	Default	Access	Bit description
7:0	<i>led6_ictrl</i>	0	RW	LED output current control of driver 2 for pin LED6.

8.6.13 LED7_ICTRL (Address 0x4c)

Table 61: LED7_ICTRL register

Addr: 0x4c		LED7_ICTRL		
Bit	Bit name	Default	Access	Bit description
7:0	<i>led7_ictrl</i>	0	RW	LED output current control of driver 2 for pin LED7.

8.6.14 LED8_ICTRL (Address 0x4d)

Table 62: LED8_ICTRL register

Addr: 0x4d		LED8_ICTRL		
Bit	Bit name	Default	Access	Bit description
7:0	<i>led8_ictrl</i>	0	RW	LED output current control of driver 2 for pin LED8.

8.6.15 LED_IRNG1 (Address 0x4e)

Table 63: LED_IRNG1 register

Addr: 0x4e		LED_IRNG1		
Bit	Bit name	Default	Access	Bit description
7:6	<i>led4_irng</i>	0	RW	LED output current range for pin LED4. 0: 25 mA 1: 150 mA 2: 225 mA 3: 300 mA
5:4	<i>led3_irng</i>	0	RW	LED output current range for pin LED3. 0: 25 mA 1: 150 mA 2: 225 mA 3: 300 mA
3:2	<i>led2_irng</i>	0	RW	LED output current range for pin LED2. 0: 25 mA 1: 150 mA 2: 225 mA 3: 300 mA
1:0	<i>led1_irng</i>	0	RW	LED output current range for pin LED1. 0: 25 mA 1: 150 mA 2: 225 mA 3: 300 mA

8.6.16 LED_IRNG2 (Address 0x4f)

Table 64: LED_IRNG2 register

Addr: 0x4f		LED_IRNG2		
Bit	Bit name	Default	Access	Bit description
7:6	<i>led8_irng</i>	0	RW	LED output current range for pin LED8. 0: 25 mA 1: 150 mA 2: 225 mA 3: 300 mA
5:4	<i>led7_irng</i>	0	RW	LED output current range for pin LED7. 0: 25 mA 1: 150 mA 2: 225 mA 3: 300 mA
3:2	<i>led6_irng</i>	0	RW	LED output current range for pin LED6. 0: 25 mA 1: 150 mA 2: 225 mA 3: 300 mA
1:0	<i>led5_irng</i>	0	RW	LED output current range for pin LED5. 0: 25 mA 1: 150 mA 2: 225 mA 3: 300 mA

8.6.17 LED_SUB1 (Address 0x50)

Table 65: LED_SUB1 register

Addr: 0x50		LED_SUB1		
Bit	Bit name	Default	Access	Bit description
6:4	<i>sub1_drv2_sel</i>	0	RW	Select the LED used in subsample 1. Only one LED from LED5 to LED8 must be active. 0: No LED used 1: LED5 2: LED6 3: LED7 4-7: LED8
2:0	<i>sub1_drv1_sel</i>	0	RW	Select the LED used in subsample 1. Only one LED from LED1 to LED4 must be active. 0: No LED used 1: LED1 2: LED2 3: LED3 4-7: LED4

8.6.18 LED_SUB2 (Address 0x51)

Table 66: LED_SUB2 register

Addr: 0x51		LED_SUB2		
Bit	Bit name	Default	Access	Bit description
6:4	sub2_drv2_sel	0	RW	Select the LED used in subsample 2. Only one LED from LED5 to LED8 must be active. 0: No LED used 1: LED5 2: LED6 3: LED7 4-7: LED8
2:0	sub2_drv1_sel	0	RW	Select the LED used in subsample 2. Only one LED from LED1 to LED4 must be active. 0: No LED used 1: LED1 2: LED2 3: LED3 4-7: LED4

8.6.19 LED_SUB3 (Address 0x52)

Table 67: LED_SUB3 register

Addr: 0x52		LED_SUB3		
Bit	Bit name	Default	Access	Bit description
6:4	<i>sub3_drv2_sel</i>	0	RW	Select the LED used in subsample 3. Only one LED from LED5 to LED8 must be active. 0: No LED used 1: LED5 2: LED6 3: LED7 4-7: LED8
2:0	<i>sub3_drv1_sel</i>	0	RW	Select the LED used in subsample 3. Only one LED from LED1 to LED4 must be active. 0: No LED used 1: LED1 2: LED2 3: LED3 4-7: LED4

8.6.20 LED_SUB4 (Address 0x53)

Table 68: LED_SUB4 register

Addr: 0x53		LED_SUB4		
Bit	Bit name	Default	Access	Bit description
6:4	<i>sub4_drv2_sel</i>	0	RW	Select the LED used in subsample 4. Only one LED from LED5 to LED8 must be active. 0: No LED used 1: LED5 2: LED6 3: LED7 4-7: LED8
2:0	<i>sub4_drv1_sel</i>	0	RW	Select the LED used in subsample 4. Only one LED from LED1 to LED4 must be active. 0: No LED used 1: LED1 2: LED2 3: LED3 4-7: LED4

8.6.21 LED_SUB5 (Address 0x54)

Table 69: LED_SUB5 register

Addr: 0x54		LED_SUB5		
Bit	Bit name	Default	Access	Bit description
6:4	<i>sub5_drv2_sel</i>	0	RW	Select the LED used in subsample 5. Only one LED from LED5 to LED8 must be active. 0: No LED used 1: LED5 2: LED6 3: LED7 4-7: LED8
2:0	<i>sub5_drv1_sel</i>	0	RW	Select the LED used in subsample 5. Only one LED from LED1 to LED4 must be active. 0: No LED used 1: LED1 2: LED2 3: LED3 4-7: LED4

8.6.22 LED_SUB6 (Address 0x55)

Table 70: LED_SUB6 register

Addr: 0x55		LED_SUB6		
Bit	Bit name	Default	Access	Bit description
6:4	<i>sub6_drv2_sel</i>	0	RW	Select the LED used in subsample 6. Only one LED from LED5 to LED8 must be active. 0: No LED used 1: LED5 2: LED6 3: LED7 4-7: LED8
2:0	<i>sub6_drv1_sel</i>	0	RW	Select the LED used in subsample 6. Only one LED from LED1 to LED4 must be active. 0: No LED used 1: LED1 2: LED2 3: LED3 4-7: LED4

8.6.23 LED_SUB7 (Address 0x56)

Table 71: LED_SUB7 register

Addr: 0x56		LED_SUB7		
Bit	Bit name	Default	Access	Bit description
6:4	<i>sub7_drv2_sel</i>	0	RW	Select the LED used in subsample 7. Only one LED from LED5 to LED8 must be active. 0: No LED used 1: LED5 2: LED6 3: LED7 4-7: LED8
2:0	<i>sub7_drv1_sel</i>	0	RW	Select the LED used in subsample 7. Only one LED from LED1 to LED4 must be active. 0: No LED used 1: LED1 2: LED2 3: LED3 4-7: LED4

8.6.24 LED_SUB8 (Address 0x57)

Table 72: LED_SUB8 register

Addr: 0x57		LED_SUB8		
Bit	Bit name	Default	Access	Bit description
6:4	<i>sub8_drv2_sel</i>	0	RW	Select the LED used in subsample 8. Only one LED from LED5 to LED8 must be active. 0: No LED used 1: LED5 2: LED6 3: LED7 4-7: LED8
2:0	<i>sub8_drv1_sel</i>	0	RW	Select the LED used in subsample 8. Only one LED from LED1 to LED4 must be active. 0: No LED used 1: LED1 2: LED2 3: LED3 4-7: LED4

8.6.25 LOWVDS_WAIT (Address 0x58)

Table 73: LOWVDS_WAIT register

Addr: 0x58		LOWVDS_WAIT		
Bit	Bit name	Default	Access	Bit description
7:0	<i>lowvds_wait</i>	0	RW	LOWVDS_WAIT defines the time between switching on an LED and the start of voltage monitoring. All the LEDs use the same time. Time = lowvds_wait * 1 μ s

8.7 Photodiodes

8.7.1 PDSEL_CFG register (Address 0x59)

Table 74: PDSEL_CFG register

Addr: 0x59		PDSEL_CFG		
Bit	Bit name	Default	Access	Bit description
0	<i>pdref_sel</i>	0	RW	Select the PDREF voltage. 0: PDREF connected to VCM common-mode voltage during measurement (0.8V) 1: PDREF connected to AGND1

8.7.2 MOD1_PDSEL1 register (Address 0x5a)

Table 75: MOD 1_PDSEL1 register

Addr: 0x5a		MOD 1_PDSEL1		
Bit	Bit name	Default	Access	Bit description
7	<i>mod1_pdsel_sub1</i>	0	RW	Selects PD8 for MOD1 in subsample 1. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD1 in subsample 1, explanation at bit 7.
5		0	RW	Selects PD6 for MOD1 in subsample 1, explanation at bit 7.
4		0	RW	Selects PD5 for MOD1 in subsample 1, explanation at bit 7.
3		0	RW	Selects PD4 for MOD1 in subsample 1, explanation at bit 7.
2		0	RW	Selects PD3 for MOD1 in subsample 1, explanation at bit 7.
1		0	RW	Selects PD2 for MOD1 in subsample 1, explanation at bit 7.
0		0	RW	Selects PD1 for MOD1 in subsample 1, explanation at bit 7.

8.7.3 MOD1_PDSEL2 register (Address 0x5b)

Table 76: MOD1_PDSEL2 register

Addr: 0x5b		MOD1_PDSEL2		
Bit	Bit name	Default	Access	Bit description
7	<i>mod1_pdssel_sub2</i>	0	RW	Selects PD8 for MOD1 in subsample 2. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD1 in subsample 2, explanation at bit 7.
5		0	RW	Selects PD6 for MOD1 in subsample 2, explanation at bit 7.
4		0	RW	Selects PD5 for MOD1 in subsample 2, explanation at bit 7.
3		0	RW	Selects PD4 for MOD1 in subsample 2, explanation at bit 7.
2		0	RW	Selects PD3 for MOD1 in subsample 2, explanation at bit 7.
1		0	RW	Selects PD2 for MOD1 in subsample 2, explanation at bit 7.
0		0	RW	Selects PD1 for MOD1 in subsample 2, explanation at bit 7.

8.7.4 MOD1_PDSEL3 register (Address 0x5c)

Table 77: MOD1_PDSEL3 register

Addr: 0x5c		MOD1_PDSEL3		
Bit	Bit name	Default	Access	Bit description
7	<i>mod1_pdssel_sub3</i>	0	RW	Selects PD8 for MOD1 in subsample 3. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD1 in subsample 3, explanation at bit 7.
5		0	RW	Selects PD6 for MOD1 in subsample 3, explanation at bit 7.
4		0	RW	Selects PD5 for MOD1 in subsample 3, explanation at bit 7.
3		0	RW	Selects PD4 for MOD1 in subsample 3, explanation at bit 7.
2		0	RW	Selects PD3 for MOD1 in subsample 3, explanation at bit 7.
1		0	RW	Selects PD2 for MOD1 in subsample 3, explanation at bit 7.
0		0	RW	Selects PD1 for MOD1 in subsample 3, explanation at bit 7.

8.7.5 MOD1_PDSEL4 register (Address 0x5d)

Table 78: MOD1_PDSEL4 register

Addr: 0x5d		MOD1_PDSEL4		
Bit	Bit name	Default	Access	Bit description
7	<i>mod1_pdsel_sub4</i>	0	RW	Selects PD8 for MOD1 in subsample 4. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD1 in subsample 4, explanation at bit 7.
5		0	RW	Selects PD6 for MOD1 in subsample 4, explanation at bit 7.
4		0	RW	Selects PD5 for MOD1 in subsample 4, explanation at bit 7.
3		0	RW	Selects PD4 for MOD1 in subsample 4, explanation at bit 7.
2		0	RW	Selects PD3 for MOD1 in subsample 4, explanation at bit 7.
1		0	RW	Selects PD2 for MOD1 in subsample 4, explanation at bit 7.
0		0	RW	Selects PD1 for MOD1 in subsample 4, explanation at bit 7.

8.7.6 MOD1_PDSEL5 register (Address 0x5e)

Table 79: MOD1_PDSEL5 register

Addr: 0x5e		MOD1_PDSEL5		
Bit	Bit name	Default	Access	Bit description
7	<i>mod1_pdsel_sub5</i>	0	RW	Selects PD8 for MOD1 in subsample 5. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD1 in subsample 5, explanation at bit 7.
5		0	RW	Selects PD6 for MOD1 in subsample 5, explanation at bit 7.
4		0	RW	Selects PD5 for MOD1 in subsample 5, explanation at bit 7.
3		0	RW	Selects PD4 for MOD1 in subsample 5, explanation at bit 7.
2		0	RW	Selects PD3 for MOD1 in subsample 5, explanation at bit 7.
1		0	RW	Selects PD2 for MOD1 in subsample 5, explanation at bit 7.
0		0	RW	Selects PD1 for MOD1 in subsample 5, explanation at bit 7.

8.7.7 MOD1_PDSEL6 register (Address 0x5f)

Table 80: MOD1_PDSEL6 register

Addr: 0x5f		MOD1_PDSEL6		
Bit	Bit name	Default	Access	Bit description
7	<i>mod1_pdsel_sub6</i>	0	RW	Selects PD8 for MOD1 in subsample 6. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD1 in subsample 6, explanation at bit 7.
5		0	RW	Selects PD6 for MOD1 in subsample 6, explanation at bit 7.
4		0	RW	Selects PD5 for MOD1 in subsample 6, explanation at bit 7.
3		0	RW	Selects PD4 for MOD1 in subsample 6, explanation at bit 7.
2		0	RW	Selects PD3 for MOD1 in subsample 6, explanation at bit 7.
1		0	RW	Selects PD2 for MOD1 in subsample 6, explanation at bit 7.
0		0	RW	Selects PD1 for MOD1 in subsample 6, explanation at bit 7.

8.7.8 MOD1_PDSEL7 register (Address 0x60)

Table 81: MOD1_PDSEL7 register

Addr: 0x60		MOD1_PDSEL7		
Bit	Bit name	Default	Access	Bit description
7	<i>mod1_pdsel_sub7</i>	0	RW	Selects PD8 for MOD1 in subsample 7. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD1 in subsample 7, explanation at bit 7.
5		0	RW	Selects PD6 for MOD1 in subsample 7, explanation at bit 7.
4		0	RW	Selects PD5 for MOD1 in subsample 7, explanation at bit 7.
3		0	RW	Selects PD4 for MOD1 in subsample 7, explanation at bit 7.
2		0	RW	Selects PD3 for MOD1 in subsample 7, explanation at bit 7.
1		0	RW	Selects PD2 for MOD1 in subsample 7, explanation at bit 7.
0		0	RW	Selects PD1 for MOD1 in subsample 7, explanation at bit 7.

8.7.9 MOD1_PDSEL8 register (Address 0x61)

Table 82: MOD1_PDSEL8 register

Addr: 0x61		MOD1_PDSEL8		
Bit	Bit name	Default	Access	Bit description
7	<i>mod1_pdssel_sub8</i>	0	RW	Selects PD8 for MOD1 in subsample 8. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD1 in subsample 8, explanation at bit 7.
5		0	RW	Selects PD6 for MOD1 in subsample 8, explanation at bit 7.
4		0	RW	Selects PD5 for MOD1 in subsample 8, explanation at bit 7.
3		0	RW	Selects PD4 for MOD1 in subsample 8, explanation at bit 7.
2		0	RW	Selects PD3 for MOD1 in subsample 8, explanation at bit 7.
1		0	RW	Selects PD2 for MOD1 in subsample 8, explanation at bit 7.
0		0	RW	Selects PD1 for MOD1 in subsample 8, explanation at bit 7.

8.7.10 MOD2_PDSEL1 register (Address 0x62)

Table 83: MOD2_PDSEL1 register

Addr: 0x62		MOD2_PDSEL1		
Bit	Bit name	Default	Access	Bit description
7	<i>mod2_pdssel_sub1</i>	0	RW	Selects PD8 for MOD2 In subsample 1. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD2 in subsample 1, explanation at bit 7.
5		0	RW	Selects PD6 for MOD2 in subsample 1, explanation at bit 7.
4		0	RW	Selects PD5 for MOD2 in subsample 1, explanation at bit 7.
3		0	RW	Selects PD4 for MOD2 in subsample 1, explanation at bit 7.
2		0	RW	Selects PD3 for MOD2 in subsample 1, explanation at bit 7.
1		0	RW	Selects PD2 for MOD2 in subsample 1, explanation at bit 7.
0		0	RW	Selects PD1 for MOD2 in subsample 1, explanation at bit 7.

8.7.11 MOD2_PDSEL2 register (Address 0x63)

Table 84: MOD2_PDSEL2 register

Addr: 0x63		MOD2_PDSEL2		
Bit	Bit name	Default	Access	Bit description
7	<i>mod2_pdsel_sub2</i>	0	RW	Selects PD8 for MOD2 in subsample 2. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD2 in subsample 2, explanation at bit 7.
5		0	RW	Selects PD6 for MOD2 in subsample 2, explanation at bit 7.
4		0	RW	Selects PD5 for MOD2 in subsample 2, explanation at bit 7.
3		0	RW	Selects PD4 for MOD2 in subsample 2, explanation at bit 7.
2		0	RW	Selects PD3 for MOD2 in subsample 2, explanation at bit 7.
1		0	RW	Selects PD2 for MOD2 in subsample 2, explanation at bit 7.
0		0	RW	Selects PD1 for MOD2 in subsample 2, explanation at bit 7.

8.7.12 MOD2_PDSEL3 register (Address 0x64)

Table 85: MOD2_PDSEL3 register

Addr: 0x64		MOD2_PDSEL3		
Bit	Bit name	Default	Access	Bit description
7	<i>mod2_pdsel_sub3</i>	0	RW	Selects PD8 for MOD2 in subsample 3. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD2 in subsample 3, explanation at bit 7.
5		0	RW	Selects PD6 for MOD2 in subsample 3, explanation at bit 7.
4		0	RW	Selects PD5 for MOD2 in subsample 3, explanation at bit 7.
3		0	RW	Selects PD4 for MOD2 in subsample 3, explanation at bit 7.
2		0	RW	Selects PD3 for MOD2 in subsample 3, explanation at bit 7.
1		0	RW	Selects PD2 for MOD2 in subsample 3, explanation at bit 7.
0		0	RW	Selects PD1 for MOD2 in subsample 3, explanation at bit 7.

8.7.13 MOD2_PDSEL4 register (Address 0x65)

Table 86: MOD2_PDSEL4 register

Addr: 0x65		MOD2_PDSEL4		
Bit	Bit name	Default	Access	Bit description
7	<i>mod2_pdsel_sub4</i>	0	RW	Selects PD8 for MOD2 in subsample 4. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD2 in subsample 4, explanation at bit 7.
5		0	RW	Selects PD6 for MOD2 in subsample 4, explanation at bit 7.
4		0	RW	Selects PD5 for MOD2 in subsample 4, explanation at bit 7.
3		0	RW	Selects PD4 for MOD2 in subsample 4, explanation at bit 7.
2		0	RW	Selects PD3 for MOD2 in subsample 4, explanation at bit 7.
1		0	RW	Selects PD2 for MOD2 in subsample 4, explanation at bit 7.
0		0	RW	Selects PD1 for MOD2 in subsample 4, explanation at bit 7.

8.7.14 MDO2_PDSEL5 register (Address 0x66)

Table 87: MOD2_PDSEL5 register

Addr: 0x66		MOD2_PDSEL5		
Bit	Bit name	Default	Access	Bit description
7	<i>mod2_pdsel_sub5</i>	0	RW	Selects PD8 for MOD2 in subsample 5. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD2 in subsample 5, explanation at bit 7.
5		0	RW	Selects PD6 for MOD2 in subsample 5, explanation at bit 7.
4		0	RW	Selects PD5 for MOD2 in subsample 5, explanation at bit 7.
3		0	RW	Selects PD4 for MOD2 in subsample 5, explanation at bit 7.
2		0	RW	Selects PD3 for MOD2 in subsample 5, explanation at bit 7.
1		0	RW	Selects PD2 for MOD2 in subsample 5, explanation at bit 7.
0		0	RW	Selects PD1 for MOD2 in subsample 5, explanation at bit 7.

8.7.15 MOD2_PDSEL6 register (Address 0x67)

Table 88: MOD2_PDSEL6 register

Addr: 0x67		MOD2_PDSEL6		
Bit	Bit name	Default	Access	Bit description
7	<i>mod2_pdssel_sub6</i>	0	RW	Selects PD8 for MOD2 in subsample 6. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD2 in subsample 6, explanation at bit 7.
5		0	RW	Selects PD6 for MOD2 in subsample 6, explanation at bit 7.
4		0	RW	Selects PD5 for MOD2 in subsample 6, explanation at bit 7.
3		0	RW	Selects PD4 for MOD2 in subsample 6, explanation at bit 7.
2		0	RW	Selects PD3 for MOD2 in subsample 6, explanation at bit 7.
1		0	RW	Selects PD2 for MOD2 in subsample 6, explanation at bit 7.
0		0	RW	Selects PD1 for MOD2 in subsample 6, explanation at bit 7.

8.7.16 MOD2_PDSEL7 register (Address 0x68)

Table 89: MOD2_PDSEL7 register

Addr: 0x68		MOD2_PDSEL7		
Bit	Bit name	Default	Access	Bit description
7	<i>mod2_pdssel_sub7</i>	0	RW	Selects PD8 for MOD2 in subsample 7. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD2 in subsample 7, explanation at bit 7.
5		0	RW	Selects PD6 for MOD2 in subsample 7, explanation at bit 7.
4		0	RW	Selects PD5 for MOD2 in subsample 7, explanation at bit 7.
3		0	RW	Selects PD4 for MOD2 in subsample 7, explanation at bit 7.
2		0	RW	Selects PD3 for MOD2 in subsample 7, explanation at bit 7.
1		0	RW	Selects PD2 for MOD2 in subsample 7, explanation at bit 7.
0		0	RW	Selects PD1 for MOD2 in subsample 7, explanation at bit 7.

8.7.17 MOD2_PDSEL8 register (Address 0x69)

Table 90: MOD2_PDSEL8 register

Addr: 0x69		MOD2_PDSEL8		
Bit	Bit name	Default	Access	Bit description
7	mod2_pdsel_sub8	0	RW	Selects PD8 for MOD2 in subsample 8. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD2 in subsample 8, explanation at bit 7.
5		0	RW	Selects PD6 for MOD2 in subsample 8, explanation at bit 7.
4		0	RW	Selects PD5 for MOD2 in subsample 8, explanation at bit 7.
3		0	RW	Selects PD4 for MOD2 in subsample 8, explanation at bit 7.
2		0	RW	Selects PD3 for MOD2 in subsample 8, explanation at bit 7.
1		0	RW	Selects PD2 for MOD2 in subsample 8, explanation at bit 7.
0		0	RW	Selects PD1 for MOD2 in subsample 8, explanation at bit 7.

8.7.18 MOD2_AFESEL1 register (Address 0x6a)

Table 91: MOD2_AFESEL1 register

Addr: 0x6a		MOD2_AFESEL1		
Bit	Bit name	Default	Access	Bit description
7:4	mod2_afesel_sub2	0	RW	Source for the AFE Input for MOD2 in subsample 2.
				0: PGND0
				1: PGND1
				2: LED1
				3: LED2
				4: LED3
				5: LED4
				6: LED5
				7: LED6
				8: LED7
				9: LED8
				10: PGND0
				11: PGND1
				12: VCSELA
				13: VCSELS
				14: VDDA
				15: VSSA
3:0	mod2_afesel_sub1	0	RW	Source for the AFE Input for MOD2 in subsample 1.
				0: PGND0
				1: PGND1
				2: LED1
				3: LED2
				4: LED3
				5: LED4
				6: LED5
				7: LED6
				8: LED7
				9: LED8
				10: PGND0
				11: PGND1
				12: VCSELA
				13: VCSELS
				14: VDDA
				15: VSSA

8.7.19 MOD2_AFESEL2 register (Address 0x6b)

Table 92: MOD2_AFESEL2 register

Addr: 0x6b		MOD2_AFESEL2		
Bit	Bit name	Default	Access	Bit description
7:4	mod2_afesel_sub4	0	RW	Source for the AFE Input for MOD2 in subsample 4.
				0: PGND0
				1: PGND1
				2: LED1
				3: LED2
				4: LED3
				5: LED4
				6: LED5
				7: LED6
				8: LED7
				9: LED8
				10: PGND0
				11: PGND1
				12: VCSELA
				13: VCSELS
				14: AGND
				15: AGND
3:0	mod2_afesel_sub3	0	RW	Source for the AFE Input for MOD2 in subsample 3.
				0: PGND0
				1: PGND1
				2: LED1
				3: LED2
				4: LED3
				5: LED4
				6: LED5
				7: LED6
				8: LED7
				9: LED8
				10: PGND0
				11: PGND1
				12: VCSELA
				13: VCSELS
				14: AGND
				15: AGND

8.7.20 MOD2_AFESEL3 register (Address 0x6c)

Table 93: MOD2_AFESEL3 register

Addr: 0x6c		MOD2_AFESEL3		
Bit	Bit name	Default	Access	Bit description
7:4	mod2_afesel_sub6	0	RW	Source for the AFE Input for MOD2 in subsample 6.
				0: PGND0
				1: PGND1
				2: LED1
				3: LED2
				4: LED3
				5: LED4
				6: LED5
				7: LED6
				8: LED7
				9: LED8
				10: PGND0
				11: PGND1
				12: VCSELA
				13: VCSELS
				14: AGND
				15: AGND
3:0	mod2_afesel_sub5	0	RW	Source for the AFE Input for MOD2 in subsample 5.
				0: PGND0
				1: PGND1
				2: LED1
				3: LED2
				4: LED3
				5: LED4
				6: LED5
				7: LED6
				8: LED7
				9: LED8
				10: PGND0
				11: PGND1
				12: VCSELA
				13: VCSELS
				14: AGND
				15: AGND

8.7.21 MOD2_AFESEL4 register (Address 0x6d)

Table 94: MOD2_AFESEL4 register

Addr: 0x6d		MOD2_AFESEL4		
Bit	Bit name	Default	Access	Bit description
7:4	mod2_afesel_sub8	0	RW	Source for the AFE Input for MOD2 in subsample 8.
				0: PGND0
				1: PGND1
				2: LED1
				3: LED2
				4: LED3
				5: LED4
				6: LED5
				7: LED6
				8: LED7
				9: LED8
				10: PGND0
				11: PGND1
				12: VCSELA
				13: VCSELS
				14: AGND
				15: AGND
3:0	mod2_afesel_sub7	0	RW	Source for the AFE Input for MOD2 in subsample 7.
				0: PGND0
				1: PGND1
				2: LED1
				3: LED2
				4: LED3
				5: LED4
				6: LED5
				7: LED6
				8: LED7
				9: LED8
				10: PGND0
				11: PGND1
				12: VCSELA
				13: VCSELS
				14: AGND
				15: AGND

8.7.22 MOD2_AFE_EN register (Address 0x6e)

Table 95: MOD2_AFE_EN register

Addr: 0x6e		MOD2_AFE_EN		
Bit	Bit name	Default	Access	Bit description
7	<i>mod2_afe_en</i>	0	RW	Select the AFE Input for MOD2 in subsample 8.
6		0	RW	Select the AFE Input for MOD2 in subsample 7.
5		0	RW	Select the AFE Input for MOD2 in subsample 6.
4		0	RW	Select the AFE Input for MOD2 in subsample 5.
3		0	RW	Select the AFE Input for MOD2 in subsample 4.
2		0	RW	Select the AFE Input for MOD2 in subsample 3.
1		0	RW	Select the AFE Input for MOD2 in subsample 2.
0		0	RW	Select the AFE Input for MOD2 in subsample 1.

8.8 SINC filter

8.8.1 SINC_CFGA register (Address 0x6f)

Table 96: SINC_CFGA register

Addr: 0x6f		SINC_CFGA		
Bit	Bit name	Default	Access	Bit description
5:3	sinc_ovs	0	RW	This register enables an oversampling function for the data provided by the ADC SINC down sampling filter for signal enhancement. The oversampling ratio has an effect on the timing $t_{\text{SINC_OVS}}$ which can be calculated with $t_{\text{SINC_OVS}} = (2^N - 1) * (2^{(\text{sinc_dec} + 4)}) / f_{\text{MOD_CLK}}$ with $N = 0 \dots 7$ and $\text{sinc_dec} = 0 \dots 4$. The modulator clock frequency $f_{\text{MOD_CLK}}$ can be controlled with <i>mod_clk</i> register and is in default configuration 10 MHz. 0: SINC filter oversampling disabled 1: x2 oversampling enabled 2: x4 oversampling enabled 3: x8 oversampling enabled 4: x16 oversampling enabled 5: x32 oversampling enabled 6: x64 oversampling enabled 7: x128 oversampling enabled
				This register controls the ADC SINC down sampling filter decimation ratio which directly affects the measurement time t_{DV}. The timing can be calculated with $t_{\text{DV}} = (((\text{sel_order} + 4) * 2^{(N + 4)}) + \text{sel_order} + 6) / f_{\text{MOD_CLK}}$ with <i>filter_mode</i> = 1. In case <i>filter_mode</i> = 0 the timing is calculated with $t_{\text{DV}} = (2^{(N + 4)} + \text{sel_order} + 6) / f_{\text{MOD_CLK}}$. 0: x16 decimation ratio 1: x32 decimation ratio 2: x64 decimation ratio 3: x128 decimation ratio 4: x256 decimation ratio
2:0	sinc_dec	0	RW	

8.8.2 SINC_CFGB register (Address 0x70)

Table 97: SINC_CFGB register

Addr: 0x70		SINC_CFGB		
Bit	Bit name	Default	Access	Bit description
6:3	<i>os_delay</i>	0	RW	This register controls the oversampling delay $t_{os} = N * (2^{(sinc_dec + 4)} / f_{MOD_CLK})$ with $N = 0 \dots 15$ and $sinc_dec = 0 \dots 4$. The modulator clock frequency f_{MOD_CLK} can be controlled with <i>mod_clk</i> register and is in default configuration 10 MHz. This timing is only valid if <i>filter_mode</i> register is set to 1 CIC filter operation mode. In case <i>filter_mode</i> register is set to zero t_{os} is always 0 μs .
2	<i>comb_dly_en</i>	0	RW	Enables additional delay in COMB path. 0: Disable 1: Enable
1	<i>sel_order</i>	0	RW	Select the filter order. 0: 4 1: 5
0	<i>filter_mode</i>	0	RW	Select the mode of the filter. 0: Integrator mode (COI) 1: CIC filter mode

8.8.3 SINC_CFGC register (Address 0x71)

Table 98: SINC_CFGC register

Addr: 0x71		SINC_CFGC		
Bit	Bit name	Default	Access	Bit description
7:0	<i>start_delay</i>	0	RW	This register controls the start of decimation $t_{SD} = N * 1 / f_{MOD_CLK}$ with $N = 0 \dots 255$. The modulator clock frequency f_{MOD_CLK} can be controlled with MOD_CLK register and is in default configuration 10 MHz.

8.8.4 SINC_CFGD register (Address 0x72)

Table 99: SINC_CFGD register

Addr: 0x72		SINC_CFGD		
Bit	Bit name	Default	Access	Bit description
7:4	<i>mod1_sinc_smd</i>	0	RW	Enlargement of the measured value of the MOD1 SINC filter. 0: + 50.00% 1: + 25.00% 2: + 12.50% 3: + 6.25%
3:0	<i>mod2_sinc_smd</i>	0	RW	Enlargement of the measured value of the MOD2 SINC filter. 0: + 50.00% 1: + 25.00% 2: + 12.50% 3: + 6.25%

8.9 Photodiode offset

8.9.1 IOS_MOD1_SUB1 register (Address 0x7a)

Table 100: IOS_MOD1_SUB1 register

Addr: 0x7a		IOS_MOD1_SUB1		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ios_mod1_sub1</i>	0	RW	PD Offset Current for Modulator 1 in subsample 1.

8.9.2 IOS_MOD1_SUB2 register (Address 0x7b)

Table 101: IOS_MOD1_SUB2 register

Addr: 0x7b		IOS_MOD1_SUB2		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ios_mod1_sub2</i>	0	RW	PD Offset Current for Modulator 1 in subsample 2.

8.9.3 IOS_MOD1_SUB3 register (Address 0x7c)

Table 102: IOS_MOD1_SUB3 register

Addr: 0x7c		IOS_MOD1_SUB3		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ios_mod1_sub3</i>	0	RW	PD Offset Current for Modulator 1 in subsample 3.

8.9.4 IOS_MOD1_SUB4 register (Address 0x7d)

Table 103: IOS_MOD1_SUB4 register

Addr: 0x7d		IOS_MOD1_SUB4		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ios_mod1_sub4</i>	0	RW	PD Offset Current for Modulator 1 in subsample 4.

8.9.5 IOS_MOD1_SUB5 register (Address 0x7e)

Table 104: IOS_MOD1_SUB5 register

Addr: 0x7e		IOS_MOD1_SUB5		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ios_mod1_sub5</i>	0	RW	PD Offset Current for Modulator 1 in subsample 5.

8.9.6 IOS_MOD1_SUB6 register (Address 0x7f)

Table 105: IOS_MOD1_SUB6 register

Addr: 0x7f		IOS_MOD1_SUB6		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ios_mod1_sub6</i>	0	RW	PD Offset Current for Modulator 1 in subsample 6.

8.9.7 IOS_MOD1_SUB7 register (Address 0x80)

Table 106: IOS_MOD1_SUB7 register

Addr: 0x80		IOS_MOD1_SUB7		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ios_mod1_sub7</i>	0	RW	PD Offset Current for Modulator 1 in subsample 7.

8.9.8 IOS_MOD1_SUB8 register (Address 0x81)

Table 107: IOS_MOD1_SUB8 register

Addr: 0x81		IOS_MOD1_SUB8		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ios_mod1_sub8</i>	0	RW	PD Offset Current for Modulator 1 in subsample 8.

8.9.9 IOS_MOD2_SUB1 register (Address 0x82)

Table 108: IOS_MOD2_SUB1 register

Addr: 0x82		IOS_MOD2_SUB1		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ios_mod2_sub1</i>	0	RW	PD Offset Current for Modulator 2 in subsample 1.

8.9.10 IOS_MOD2_SUB2 register (Address 0x83)

Table 109: IOS_MOD2_SUB2 register

Addr: 0x83		IOS_MOD2_SUB2		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ios_mod2_sub2</i>	0	RW	PD Offset Current for Modulator 2 in subsample 2.

8.9.11 IOS_MOD2_SUB3 register (Address 0x84)

Table 110: IOS_MOD2_SUB3 register

Addr: 0x84		IOS_MOD2_SUB3		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ios_mod2_sub3</i>	0	RW	PD Offset Current for Modulator 2 in subsample 3.

8.9.12 IOS_MOD2_SUB4 register (Address 0x85)

Table 111: IOS_MOD2_SUB4 register

Addr: 0x85		IOS_MOD2_SUB4		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ios_mod2_sub4</i>	0	RW	PD Offset Current for Modulator 2 in subsample 4.

8.9.13 IOS_MOD2_SUB5 register (Address 0x86)

Table 112: IOS_MOD2_SUB5 register

Addr: 0x86		IOS_MOD2_SUB5		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ios_mod2_sub5</i>	0	RW	PD Offset Current for Modulator 2 in subsample 5.

8.9.14 IOS_MOD2_SUB6 register (Address 0x87)

Table 113: IOS_MOD2_SUB6 register

Addr: 0x87		IOS_MOD2_SUB6		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ios_mod2_sub6</i>	0	RW	PD Offset Current for Modulator 2 in subsample 6.

8.9.15 IOS_MOD2_SUB7 register (Address 0x88)

Table 114: IOS_MOD2_SUB7 register

Addr: 0x88		IOS_MOD2_SUB7		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ios_mod2_sub7</i>	0	RW	PD Offset Current for Modulator 2 in subsample 7.

8.9.16 IOS_MOD2_SUB8 register (Address 0x89)

Table 115: IOS_MOD2_SUB8 register

Addr: 0x89		IOS_MOD2_SUB8		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ios_mod2_sub8</i>	0	RW	PD Offset Current for Modulator 2 in subsample 8.

8.9.17 IOS_LED OFF register (Address 0x8a)

Table 116: IOS_LED OFF register

Addr: 0x8a		IOS_LED OFF		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ios_ledoff</i>	0	RW	PD Offset Current for all subsamples during LED off sampling phase (Double and Triple Sampling).

8.9.18 IOS_CFG register (Address 0x8b)

Table 117: IOS_CFG register

Addr: 0x8b		IOS_CFG		
Bit	Bit name	Default	Access	Bit description
0	<i>dis_ledoff</i>	0	RW	0 = Using of the SUBX LEDON PD Offset current for SUBX LEDOFF sampling phase (Double, Triple) 1 = Using the PDOffset current from IOS_LED OFF for all subsamples Note: If IOS_LED OFF = 0, no current is used.

8.10 Advanced automatic offset control

8.10.1 AOC_SAR_THRES (Address 0x8c)

Table 118: AOC_SAR_THRES register

Addr: 0x8c		AOC_SAR_THRES		
Bit	Bit name	Default	Access	Bit description
7:0	<i>sar_thres</i>	0	RW	Threshold for SAR single measurement.

8.10.2 AOC_SAR_RANGE (Address 0x8d)

Table 119: AOC_SAR_RANGE register

Addr: 0x8d		AOC_SAR_RANGE		
Bit	Bit name	Default	Access	Bit description
4	<i>sar_range_en</i>	0	RW	Enable the Range for SAR single measurement.
3:0	<i>sar_range</i>	0	RW	The Range for SAR single measurement.

8.10.3 AOC_SAR_MOD1 (Address 0x8e)

Table 120: AOC_SAR_MOD1 register

Addr: 0x8e		AOC_SAR_MOD1		
Bit	Bit name	Default	Access	Bit description
7:0	<i>sar_mod1_en</i>	0	RW	Enabled when using the last SAR value in MOD1. 7:0 subsample 8.... subsample 1

8.10.4 AOC_SAR_MOD2 (Address 0x8f)

Table 121: AOC_SAR_MOD2 register

Addr: 0x8f		AOC_SAR_MOD2		
Bit	Bit name	Default	Access	Bit description
7:0	<i>sar_mod2_en</i>	0	RW	Enabled when using the last SAR value in MOD2. 7:0 subsample 8.... subsample 1

8.11 Post processing

8.11.1 PP_CFG (Address 0x90)

Table 122: PP_CFG register

Addr: 0x90		PP_CFG		
Bit	Bit name	Default	Access	Bit description
4	<i>asat_on</i>	0	RW	Enable Analog Saturation post processing.
3:0	<i>asat_fil</i>	0	RW	Digital Filter for Analog Saturation

8.11.2 MOD1_PP1 (Address 0x91)

Table 123: MOD1_PP1 register

Addr: 0x91		MOD1_PP1		
Bit	Bit name	Default	Access	Bit description
7:6	<i>mod1_pp_sub4</i>	0	RW	Post-processing for MOD1 in subsample 4. 0: Normal value 1: Invert value 2: Value - <i>pp_offset</i> 3: Write value to <i>pp_offset</i>
5:4	<i>mod1_pp_sub3</i>	0	RW	Post-processing for MOD1 in subsample 3. 0: Normal value 1: Invert value 2: Value - <i>pp_offset</i> 3: Write value to <i>pp_offset</i>
3:2	<i>mod1_pp_sub2</i>	0	RW	Post-processing for MOD1 in subsample 2. 0: Normal value 1: Invert value 2: Value - <i>pp_offset</i> 3: Write value to <i>pp_offset</i>
1:0	<i>mod1_pp_sub1</i>	0	RW	Post-processing for MOD1 in subsample 1. 0: Normal value 1: Invert value 2: Value - <i>pp_offset</i> 3: Write value to <i>pp_offset</i>

8.11.3 MOD1_PP2 (Address 0x92)

Table 124: MOD1_PP2 register

Addr: 0x92		MOD1_PP2		
Bit	Bit name	Default	Access	Bit description
7:6	<i>mod1_pp_sub8</i>	0	RW	Post-processing for MOD1 in subsample 8. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset
5:4	<i>mod1_pp_sub7</i>	0	RW	Post-processing for MOD1 in subsample 7. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset
3:2	<i>mod1_pp_sub6</i>	0	RW	Post-processing for MOD1 in subsample 6. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset
1:0	<i>mod1_pp_sub5</i>	0	RW	Post-processing for MOD1 in subsample 5. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset

8.11.4 MOD2_PP1 (Address 0x93)

Table 125: MOD2_PP1 register

Addr: 0x93		MOD2_PP1		
Bit	Bit name	Default	Access	Bit description
7:6	<i>mod2_pp_sub4</i>	0	RW	Post-processing for MOD2 in subsample 4. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset
5:4	<i>mod2_pp_sub3</i>	0	RW	Post-processing for MOD2 in subsample 3. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset
3:2	<i>mod2_pp_sub2</i>	0	RW	Post-processing for MOD2 in subsample 2. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset
1:0	<i>mod2_pp_sub1</i>	0	RW	Post-processing for MOD2 in subsample 1. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset

8.11.5 MOD2_PP2 (Address 0x94)

Table 126: MOD2_PP2 register

Addr: 0x94		MOD2_PP2		
Bit	Bit name	Default	Access	Bit description
7:6	<i>mod2_pp_sub8</i>	0	RW	Post-processing for MOD2 in subsample 8. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset
5:4	<i>mod2_pp_sub7</i>	0	RW	Post-processing for MOD2 in subsample 7. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset
3:2	<i>mod2_pp_sub6</i>	0	RW	Post-processing for MOD2 in subsample 6. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset
1:0	<i>mod2_pp_sub5</i>	0	RW	Post-processing for MOD2 in subsample 5. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset

8.12 Sequencer

8.12.1 IRQ_ENABLE (Address 0x95)

Table 127: IRQ_ENABLE register

Addr: 0x95		IRQ_ENABLE		
Bit	Bit name	Default	Access	Bit description
7	<i>irq_en_iir_overflow</i>	0	RW	Enable the interrupt for IIR Filter overflow.
6	<i>irq_en_leadoff</i>	0	RW	Edge Lead-Off Interrupt.
5	<i>irq_en_vcsel</i>	0	RW	VCSEL short to the VDD/VSS or VCSEL watchdog detection.
4	<i>irq_en_asat</i>	0	RW	Analog Saturation Interrupt.
3	<i>irq_en_led_lowvds</i>	0	RW	LED lowvds Interrupt.
2	<i>irq_en_fifooverflow</i>	0	RW	FIFO overflow occurred. Next sample is lost.
1	<i>irq_en_fifothreshold</i>	0	RW	FIFO is almost full, FIFO_LEVEL > FIFO_THRESHOLD
0	<i>irq_en_sequencer</i>	0	RW	Sequencer Measurements ended in accordance with SEQ_COUNT>0. No display with continuous measurement SEQ_COUNT=0. Reset by reading the STATUS.

8.12.2 SUBWAIT (Address 0x96)

Table 128: SUBWAIT register

Addr: 0x96		SUBWAIT		
Bit	Bit name	Default	Access	Bit description
7:0	<i>sub_wait</i>	0	RW	This register controls the wait time between subsamples $t_{SUB_WAIT} = N * 1\mu s$ with $N = 0 \dots 255$

8.12.3 SAR_WAIT (Address 0x97)

Table 129: SAR_WAIT register

Addr: 0x97		SAR_WAIT		
Bit	Bit name	Default	Access	Bit description
7:0	<i>sar_wait</i>	0	RW	Distance between the SAR measurements; $N * 1 \mu s$

8.12.4 LED_INIT (Address 0x98)

Table 130: LED_INIT register

Addr: 0x98		LED_INIT		
Bit	Bit name	Default	Access	Bit description
7:0	<i>led_init</i>	0	RW	This register controls the LED initialization time as follows $t_{LED_INIT} = N * 1 \mu s$ with $N = 0 \dots 255$

8.12.5 FREQL (Address 0x99)

Table 131: FREQL register

Addr: 0x99		FREQL		
Bit	Bit name	Default	Access	Bit description
7:0	<i>freq[7:0]</i>	79	RW	Sample period sequence: $T(SEQ) = (n+1) * 31.25 \mu s$ $f(SEQ) = 1/((n+1) * 31.25 \mu s)$

8.12.6 FREQH (Address 0x9a)

Table 132: FREQH register

Addr: 0x9a		FREQH		
Bit	Bit name	Default	Access	Bit description
7:0	<i>freq[15:8]</i>	79	RW	See FREQL (Address 0x99).

8.12.7 MOD1_SUB_EN (Address 0x9b)

Table 133: MOD1_SUB_EN register

Addr: 0x9b		MOD1_SUB_EN		
Bit	Bit name	Default	Access	Bit description
7:0	<i>mod1_sub_en</i>	0	RW	Enable subsamples for Modulator1. Bit 0 to 7 enable or disable subsample 1 to 8.

8.12.8 MOD2_SUB_EN (Address 0x9c)

Table 134: MOD2_SUB_EN register

Addr: 0x9c		MOD2_SUB_EN		
Bit	Bit name	Default	Access	Bit description
7:0	<i>mod2_sub_en</i>	0	RW	Enable subsamples for Modulator2. Bit 0 to 7 enable or disable subsample 1 to 8.

8.12.9 MODE1 (Address 0x9d)

Table 135: MODE1 register

Addr: 0x9d		MODE1		
Bit	Bit name	Default	Access	Bit description
4:2	<i>mode_sub1</i>	0	RW	This register defines the number of measurement repetitions for the selected measurement mode. 0: No repetition of selected measurement mode 1: 2 measurement repetitions 2: 4 measurement repetitions 3: 8 measurement repetitions 4: 16 measurement repetitions 5: 32 measurement repetitions 6: 64 measurement repetitions 7: 128 measurement repetitions
				Measure Mode 0: Single Sampling 1: Double Sampling 2: Triple Sampling 3: SAR Single Sampling

8.12.10 MODE2 (Address 0x9e)

Table 136: MODE2 register

Addr: 0x9e		MODE2		
Bit	Bit name	Default	Access	Bit description
4:2	mode_sub2	0	RW	This register defines the number of measurement repetitions for the selected measurement mode. 0: No repetition of selected measurement mode 1: 2 measurement repetitions 2: 4 measurement repetitions 3: 8 measurement repetitions 4: 16 measurement repetitions 5: 32 measurement repetitions 6: 64 measurement repetitions 7: 128 measurement repetitions
				Measure Mode 0: Single Sampling 1: Double Sampling 2: Triple Sampling 3: SAR Single Sampling

8.12.11 MODE3 (Address 0x9f)

Table 137: MODE3 register

Addr: 0x9f		MODE3		
Bit	Bit name	Default	Access	Bit description
4:2	<i>mode_sub3</i>	0	RW	This register defines the number of measurement repetitions for the selected measurement mode. 0: No repetition of selected measurement mode 1: 2 measurement repetitions 2: 4 measurement repetitions 3: 8 measurement repetitions 4: 16 measurement repetitions 5: 32 measurement repetitions 6: 64 measurement repetitions 7: 128 measurement repetitions
1:0			RW	Measure Mode 0: Single Sampling 1: Double Sampling 2: Triple Sampling 3: SAR Single Sampling

8.12.12 MODE4 (Address 0xa0)

Table 138: MODE4 register

Addr: 0xa0		MODE4		
Bit	Bit name	Default	Access	Bit description
4:2	mode_sub4	0	RW	This register defines the number of measurement repetitions for the selected measurement mode. 0: No repetition of selected measurement mode 1: 2 measurement repetitions 2: 4 measurement repetitions 3: 8 measurement repetitions 4: 16 measurement repetitions 5: 32 measurement repetitions 6: 64 measurement repetitions 7: 128 measurement repetitions
				Measure Mode 0: Single Sampling 1: Double Sampling 2: Triple Sampling 3: SAR Single Sampling

8.12.13 MODE5 (Address 0xa1)

Table 139: MODE5 register

Addr: 0xa1		MODE5		
Bit	Bit name	Default	Access	Bit description
4:2	<i>mode_sub5</i>	0	RW	This register defines the number of measurement repetitions for the selected measurement mode. 0: No repetition of selected measurement mode 1: 2 measurement repetitions 2: 4 measurement repetitions 3: 8 measurement repetitions 4: 16 measurement repetitions 5: 32 measurement repetitions 6: 64 measurement repetitions 7: 128 measurement repetitions
				Measure Mode 0: Single Sampling 1: Double Sampling 2: Triple Sampling 3: SAR Single Sampling

8.12.14 MODE6 (Address 0xa2)

Table 140: MODE6 register

Addr: 0xa2		MODE6		
Bit	Bit name	Default	Access	Bit description
4:2	<i>mode_sub6</i>	0	RW	This register defines the number of measurement repetitions for the selected measurement mode. 0: No repetition of selected measurement mode 1: 2 measurement repetitions 2: 4 measurement repetitions 3: 8 measurement repetitions 4: 16 measurement repetitions 5: 32 measurement repetitions 6: 64 measurement repetitions 7: 128 measurement repetitions
				Measure Mode 0: Single Sampling 1: Double Sampling 2: Triple Sampling 3: SAR Single Sampling
1:0			RW	

8.12.15 MODE7 (Address 0xa3)

Table 141: MODE7 register

Addr: 0xa3		MODE7		
Bit	Bit name	Default	Access	Bit description
4:2	mode_sub7	0	RW	This register defines the number of measurement repetitions for the selected measurement mode. 0: No repetition of selected measurement mode 1: 2 measurement repetitions 2: 4 measurement repetitions 3: 8 measurement repetitions 4: 16 measurement repetitions 5: 32 measurement repetitions 6: 64 measurement repetitions 7: 128 measurement repetitions
				Measure Mode 0: Single Sampling 1: Double Sampling 2: Triple Sampling 3: SAR Single Sampling

8.12.16 MODE8 (Address 0xa4)

Table 142: MODE8 register

Addr: 0xa4		MODE8		
Bit	Bit name	Default	Access	Bit description
4:2	<i>mode_sub8</i>	0	RW	This register defines the number of measurement repetitions for the selected measurement mode. 0: No repetition of selected measurement mode 1: 2 measurement repetitions 2: 4 measurement repetitions 3: 8 measurement repetitions 4: 16 measurement repetitions 5: 32 measurement repetitions 6: 64 measurement repetitions 7: 128 measurement repetitions
1:0			RW	Measure Mode 0: Single Sampling 1: Double Sampling 2: Triple Sampling 3: SAR Single Sampling

8.12.17 CFG (Address 0xa5)

Table 143: CFG register

Addr: 0xa5		CFG		
Bit	Bit name	Default	Access	Bit description
3	<i>ext_freq</i>	0	RW	This bit disables the FREQL and FREQH registers. A rising edge on the EXTCLK_SYNC pin starts the measurement of one sample in case <i>ext_freq</i> bit is set.
2	<i>moving_average_on</i>	0	RW	Turn ON Moving Average filter function.
1:0	<i>moving_average_val</i>	0	RW	Number of samples used for the moving average filter. 0: 2 1: 4 2: 8 3: 16

8.12.18 SAMPLE_NUM (Address 0xb1)

Table 144: SAMPLE_NUM register

Addr: 0xb1		SAMPLE_NUM		
Bit	Bit name	Default	Access	Bit description
7:0	<i>sample_num</i>	1	RW	Number of samples for the active channel. If <i>sample_num</i> = 0, the sequencer runs continuously.

8.13 FIFO

8.13.1 FIFO_THRESHOLD (Address 0xca)

Table 145: FIFO_THRESHOLD register

Addr: 0xca		FIFO_THRESHOLD		
Bit	Bit name	Default	Access	Bit description
7:0	<i>fifo_threshold[7:0]</i>	64	RW	FIFO threshold Bit 7:0 0 = Interrupt on one sample

8.13.2 FIFO_CTRL (Address 0xcb)

Table 146: FIFO_CTRL register

Addr: 0xcb		FIFO_CTRL		
Bit	Bit name	Default	Access	Bit description
7	<i>fifo_clear</i>	0	RW	Write 1 here to clear the FIFO.
3	<i>seq_sync_en</i>	0	RW	Write Synchronization Information.
2	<i>sinc_randext_en</i>	1	RW	Enables SINC data extension with randomized bits, otherwise zeros are inserted.
1	<i>sar_data_en</i>	0	RW	Write 4-bit SAR into SINC data Bit (3:0).
0	<i>fifo_threshold[8]</i>	0	RW	FIFO threshold Bit 8.

8.14 Miscellaneous

8.14.1 PRODUCT_ID (Address 0xeb)

Table 147: PRODUCT_ID register

Addr: 0xeb		PRODUCT_ID		
Bit	Bit name	Default	Access	Bit description
5:1	<i>otp_part_id</i>	-	RO	Image of the OTP bit for part ID.

8.14.2 SILICON_ID (Address 0xec)

Table 148: SILICON_ID register

Addr: 0xec		SILICON_ID		
Bit	Bit name	Default	Access	Bit description
7:0	<i>silicon_id</i>	0x92	RO	Silicon identification number.

8.14.3 GPIO_CTRL (Address 0xee)

Table 149: GPIO_CTRL register

Addr: 0xee		GPIO_CTRL		
Bit	Bit name	Default	Access	Bit description
1	<i>gpio_in</i>	0	RW	Readable value from the GPIO.
0	<i>gpio_out</i>	0	RW	Programmable GPIO output.

8.14.4 CHIP_CTRL (Address 0xef)

Table 150: CHIP_CTRL register

Addr: 0xef		CHIP_CTRL		
Bit	Bit name	Default	Access	Bit description
1	<i>wd_reset</i>	0	W	Writing this register resets the watchdog output inside VCSEL safety block to remove an error condition.
0	<i>chip_reset</i>	0	W	Writing this registers triggers a power on reset condition.

8.14.5 SEQ_START (Address 0xf0)

Table 151: SEQ_START register

Addr: 0xf0		SEQ_START		
Bit	Bit name	Default	Access	Bit description
1	<i>start_seq</i>	0	R_PUSH	Write a pulse for the start or stop of the measurements. 0: Stop 1: Start Read the status of the measurement. 0: Inactive 1: Active The number of measurements is specified in the SAMPLE_NUM register.

8.14.6 STATUS_CGB (Address 0xf1)

Table 152: STATUS_CGB register

Addr: 0xf1		STATUS_CGB		
Bit	Bit name	Default	Access	Bit description
1	<i>pll_lock</i>	0	RO	PLL locked state indicator.
0	<i>clk_pll_ok</i>	0	RO	Status indicator of CLK20M.

8.14.7 STATUS_SEQ (Address 0xf2)

Table 153: STATUS_SEQ register

Addr: 0xf2		STATUS_SEQ		
Bit	Bit name	Default	Access	Bit description
1	<i>seq_end</i>	0	RO	Measurement was stopped.
0	<i>seq_error</i>	0	RO	Measurement of a sample was not started. Sample frequency is too high.

8.14.8 STATUS_LED (Address 0xf3)

Table 154: STATUS_LED register

Addr: 0xf3		STATUS_LED		
Bit	Bit name	Default	Access	Bit description
7:0	<i>led_lowvds</i>	0	RO	If active, the LED current does not reach the expected value.

8.14.9 STATUS_ASATA (Address 0xf4)

Table 155: STATUS_ASATA register

Addr: 0xf4		STATUS_ASATA		
Bit	Bit name	Default	Access	Bit description
7:4	<i>mod1_asat</i>	0	RO	Analog Saturation Modulator1.
3:0	<i>mod2_asat</i>	0	RO	Analog Saturation Modulator2.

8.14.10 STATUS_ASATB (Address 0xf5)

Table 156: STATUS_ASATB register

Addr: 0xf5		STATUS_ASATB		
Bit	Bit name	Default	Access	Bit description
3:0	<i>mod3_asat</i>	0	RO	Analog Saturation Modulator 3.

8.14.11 STATUS_VCSEL (Address 0xf6)

Table 157: STATUS_VCSEL register

Addr: 0xf6		STATUS_VCSEL		
Bit	Bit name	Default	Access	Bit description
4	<i>led_wd</i>	0	RO	VCSEL LED digital Watchdog occurred t > 1.0 ms.
3	<i>vcsel_vss</i>	0	RO	VCSEL short to PGND detected.
2	<i>vcsel_vdd</i>	0	RO	VCSEL short to VCSELS detected.
1:0	<i>vcsel_wd</i>	0	RO	VCSEL LED analog Watchdog occurred t > 3.2 ms Bit0 - LED Driver 1 Bit1 - LED Driver 2

8.14.12 STATUS_VCSEL_VSS (Address 0xf7)

Table 158: STATUS_VCSEL_VSS register

Addr: 0xf7		STATUS_VCSEL_VSS		
Bit	Bit name	Default	Access	Bit description
7	<i>vcsel_short_vss</i>	0	RO	Pin LED8
6			RO	Pin LED7
5			RO	Pin LED6
4			RO	Pin LED5
3			RO	Pin LED4
2			RO	Pin LED3
1			RO	Pin LED2
0			RO	Pin LED1

8.14.13 STATUS_VCSEL_VDD (Address 0xf8)

Table 159: STATUS_VCSEL_VDD register

Addr: 0xf8		STATUS_VCSEL_VDD		
Bit	Bit name	Default	Access	Bit description
7	<i>vcsel_short_vdd</i>	0	RO	Pin LED8
6			RO	Pin LED7
5			RO	Pin LED6
4			RO	Pin LED5
3			RO	Pin LED4
2			RO	Pin LED3
1			RO	Pin LED2
0			RO	Pin LED1

8.14.14 STATUS (Address 0xfa)

The STATUS register shows the current status of the interface. When released via IRQ_ENABLE, all the bits can trigger an interrupt.

Reading the STATUS registers only deletes *irq_iir_overflow*, *irq_fifooverflow*, and *irq_sequencer*.

To delete *irq_leadoff*, the **STATUS_LEADOFF** register must be read.

To delete *irq_vcsele*, the **STATUS_VCSEL** register must be read.

To delete *irq_asat*, the **STATUS_ASAT** register must be read.

To delete *irq_lowvds*, the **STATUS_LED** register must be read.

To delete *irq_sequencer*, the **STATUS_SEQ** register must be read.

The interrupt for the fill level of the FIFO *irq_fifothreshold* cannot be deleted directly, but only by lowering the FIFO level.

Table 160: STATUS register

Addr: 0xfa		STATUS		
Bit	Bit name	Default	Access	Bit description
7	<i>irq_iir_overflow</i>	0	RO	Interrupt status bit if the IIR filter block has an overflow condition.
6	<i>irq_leadoff</i>	0	RO	Lead-Off Interrupt. Check Register STATUS_LEADOFF.
5	<i>irq_vcsele</i>	0	RO	VCSEL short to VCSELS/PGND or VCSEL watchdog detection. Check Register STATUS_VCSEL, STATUS_VCSEL_VSS and STATUS_VCSEL_VDD.
4	<i>irq_asat</i>	0	RO	Analog Saturation Interrupt. Check Register STATUS_ASATA and STATUS_ASATB.
3	<i>irq_led_lowvds</i>	0	RO	LED lowvds Interrupt. Check Register STATUS_LED.
2	<i>irq_fifooverflow</i>	0	RO	FIFO overflow occurred. The next sample is lost.
1	<i>irq_fifothreshold</i>	0	RO	FIFO is almost full, FIFO_LEVEL > FIFO_THRESHOLD
0	<i>irq_sequencer</i>	0	RO	Sequencer Interrupt. Check Register STATUS_SEQ.

8.14.15 FIFO_LEVEL0 (Address 0xfb)

Table 161: FIFO_LEVEL0 register

Addr: 0xfb		FIFO_LEVEL0		
Bit	Bit name	Default	Access	Bit description
7:0	<i>fifo_level[7:0]</i>	0	RO	FIFO level Bit 7:0.

8.14.16 FIFO_LEVEL1 (Address 0xfc)

Table 162: FIFO_LEVEL1 register

Addr: 0xfc		FIFO_LEVEL1		
Bit	Bit name	Default	Access	Bit description
2	<i>fifo_overflow</i>	0	RO	FIFO overflow.
1:0	<i>fifo_level[9:8]</i>	0	RO	FIFO level Bit 9:8.

8.14.17 FIFOL (Address 0xfd)

Table 163: FIFOL register

Addr: 0xfd		FIFOL		
Bit	Bit name	Default	Access	Bit description
7:4	<i>fifol</i>	0	PUSHPOP	Bits 3..0 of ADC
3			PUSHPOP	Block frame
2:0			PUSHPOP	Data marker

8.14.18 FIFOM (Address 0xfe)

Table 164: FIFOM register

Addr: 0xfe		FIFOM		
Bit	Bit name	Default	Access	Bit description
7:0	<i>fifom</i>	0	PUSHPOP	Bits 11..4 of ADC

8.14.19 FIFOH (Address 0xff)

Table 165: FIFOH register

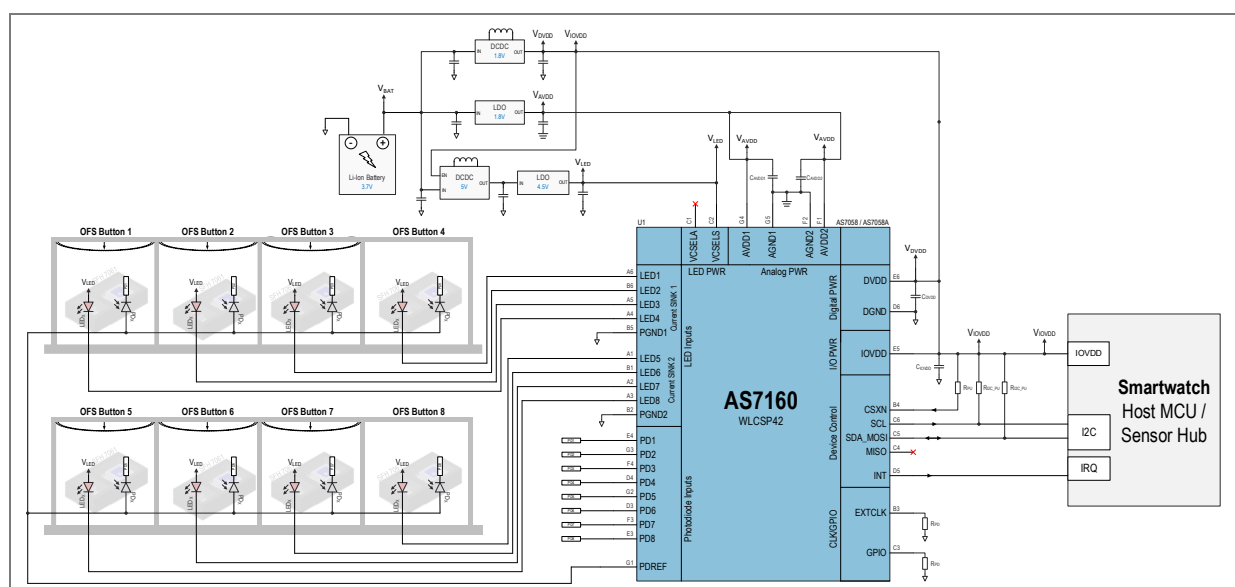
Addr: 0xff		FIFOH		
Bit	Bit name	Default	Access	Bit description
7:0	<i>fifoh</i>	0	PUSHPOP	Bits 19..12 of ADC

9 Application information

This chapter contains application related information.

9.1 Schematic

Figure 41: AS7160 schematic 8 button optical force sensing application



9.2 External components

This chapter provides recommended external components for the example schematics shown in chapter 9.1.

Table 166: External components - capacitors

Symbol	Parameter	Temp. characteristic	Min. rated voltage	Max. tolerance	Recommended typ. value
C _{DVDD}	Input capacitor for DVDD pin	Y5R; X5R	4 V	±10%	1 µF
C _{IOVDD}	Input capacitor for IOVDD pin	Y5R; X5R	4 V	±10%	100 nF
C _{AVDDx}	Input capacitor for AVDDx pin	Y5R; X5R	4 V	±10%	1 µF

Table 167: External components - resistors

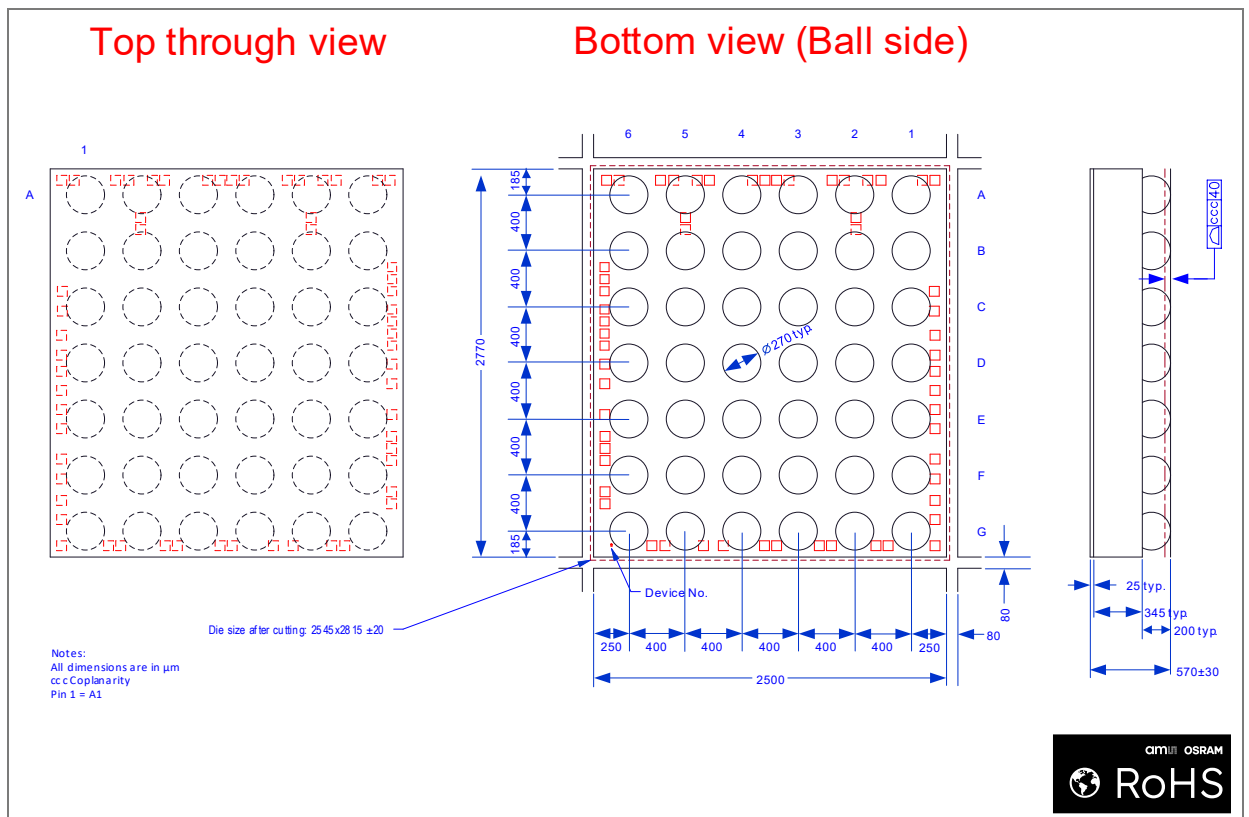
Symbol	Parameter	Min. power dissipation	Max. tolerance	Min. / Max. nominal resistance	Recommended typ. value
R _{PU}	Pull up resistor	0.03 W	±10%	1 kΩ / 100 kΩ	47 kΩ
R _{I2C_PU}	I ² C bus pull up resistors	0.03 W	±10%	1 kΩ / 47 kΩ	10 kΩ
R _{PD}	Pull down resistor	0.03 W	±10%	1 kΩ / 100 kΩ	47 kΩ

Table 168: Optical front ends

Symbol	Parameter	Vendor	Part number	LED wavelength	Typ. forward voltage IR
MODx	Top looker optical front end with one photodiode and one IR LED	ams OSRAM	SFH 7061	940 nm	1.3 V @ 20 mA
MODx	Side looker optical front end with one photodiode and one IR LED	ams OSRAM	SFH 7065	940 nm	1.3 V @ 20 mA

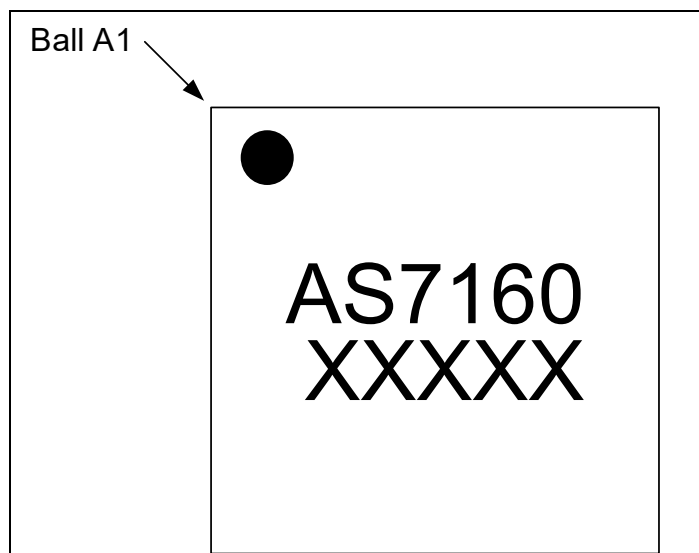
10 Package drawings & markings

Figure 42: WLCSP42 package outline drawing



- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Dimensioning and tolerancing conform to ASME Y14.5M-1994.
- (3) N is the total number of terminals.
- (4) This package contains no lead (Pb).
- (5) This drawing is subject to change without notice.

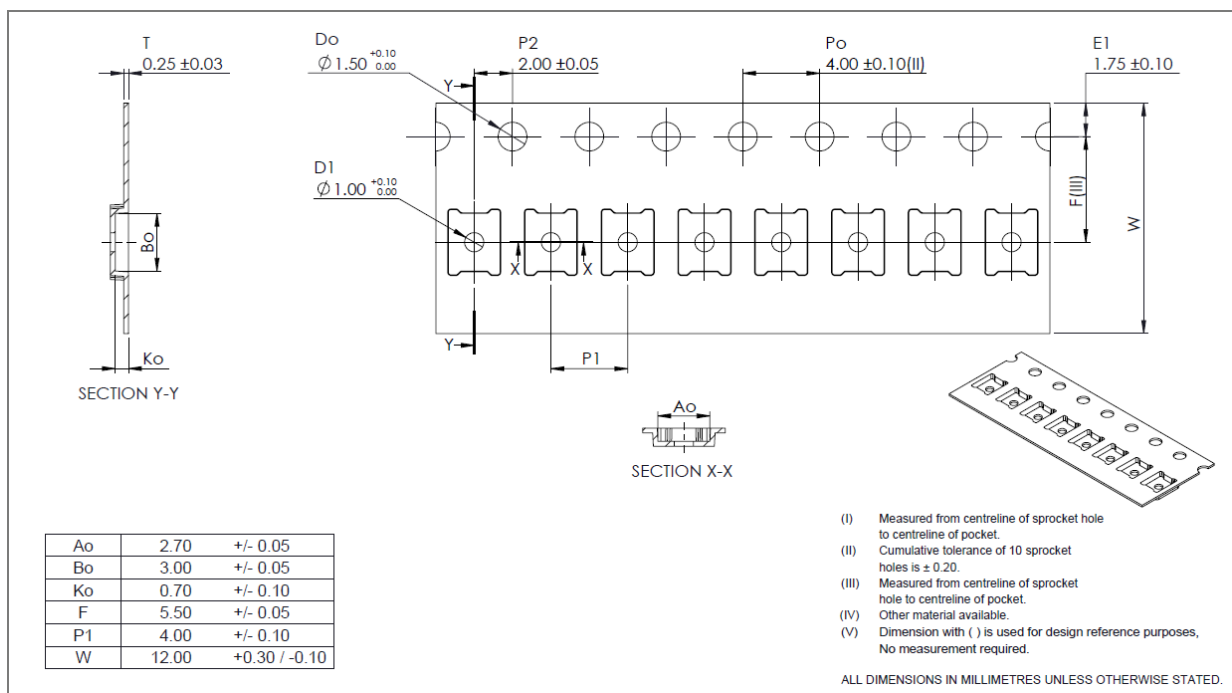
Figure 43: AS7160 WLCSP42 package marking/code



xxxxxxx Tracecode

11 Tape & reel information

Figure 44: WLCSP42 tape dimensions



12 Revision information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Changes from previous released version to current revision v2-00

Page

Document security class has been updated as "PUBLIC" in the footer

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

13 Legal information

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