16V, 6A Switching Buck Regulator Module

MCPF1606AM06

Description

The MCPF1606AM06 is an easy-to-use, fully integrated and highly efficient Point-Of-Load (POL) 6A voltage regulator module. The on-chip Pulse-Width Modulation (PWM) controller and integrated MOSFETs, plus incorporated inductor and capacitors, result in an extremely compact and accurate regulator. The low-profile package is suitable for automated assembly using standard surface-mount equipment.

This unique and optimized solution has yielded the highest density, full-featured 6A POL currently available. The user can program aspects of the MCPF1606AM06's operation using the I^2C protocol. The built-in protection features include soft start to limit inrush current and prevent overshoot at startup, overvoltage protection, thermally compensated overcurrent protection with hiccup mode, and thermal shutdown with auto-recovery.

Features

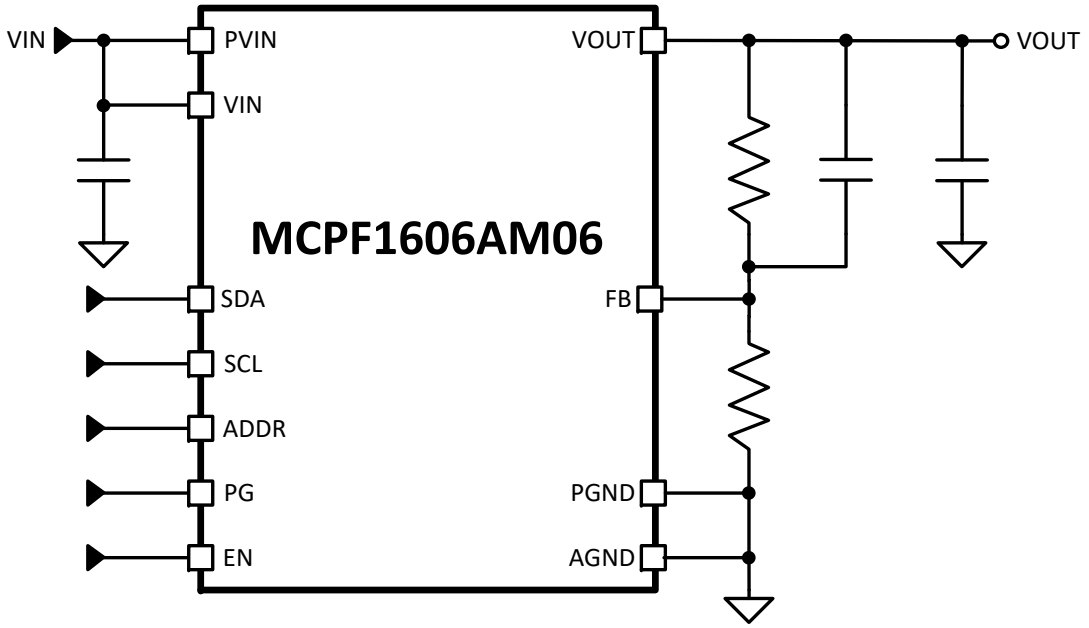
- POL Module With Output Inductor Included
- Small Size: 3.3 mm × 3.3 mm × 1.35 mm (LLGA)
- Continuous 6A Load Capability
- Wide Input Voltage Range: 4.2–16V
- Adjustable Output Voltage: 0.6–5V
- Voltage, Current and Temperature Telemetry
- 0.5% Initial Output Voltage Accuracy
- Servo Loop Output Voltage Control
- No External Compensation Required
- Programmable Operation Using I^2C Serial Bus
- Enabled Input, Programmable Under-Voltage Lock-Out (UVLO) Circuit
- Power Good Indicator
- Built-in Protection Features
- Operating Temperature From −40°C to +125°C
- Lead-Free and Halogen-Free
- Compliant With EU REACH and RoHS

Applications

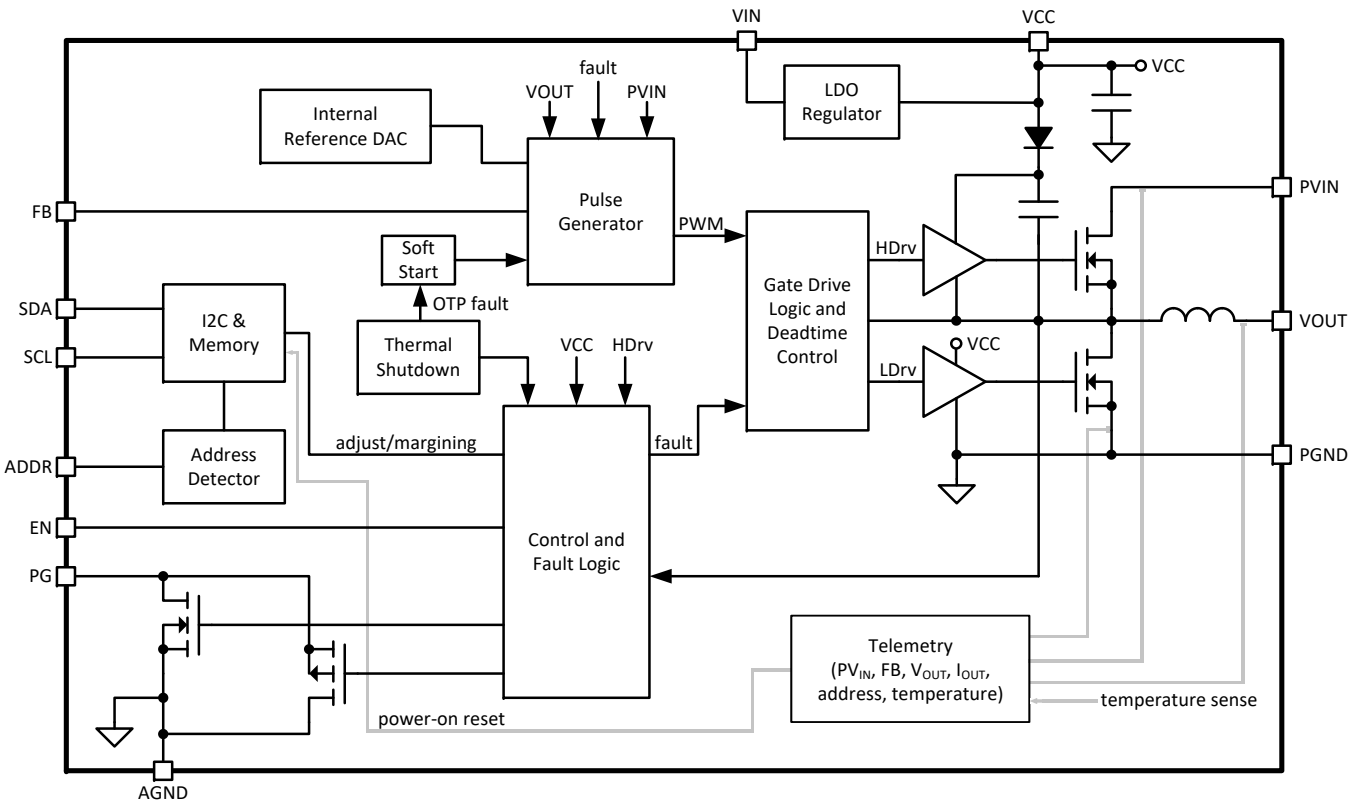
- Servers, Workstations and Cloud Computing
- Routers, Switches and Telecom Equipment
- Base Stations, Data Center Power Solutions
- High-Power Density POL Conversion

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Typical Application



Block Diagram



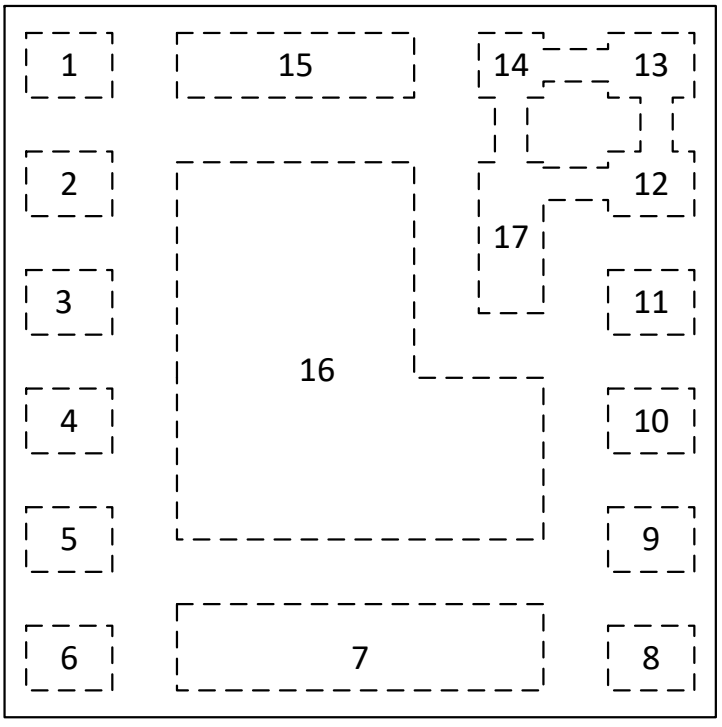
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1. Pin Configuration

Pin Number	Name	Description
1	SDA	I^2C serial data line. Pull to bus voltage with 4.99 kΩ or tie to AGND if not used.
2	PG	Power Good status indicator, open drain. Connect to pin 10 or an external bias via a resistor.
3	EN	Turns the MCPF1606AM06 ON or OFF. A resistor divider can be used to set an external UVLO threshold.
4	SCL	I^2C serial clock line. Pull to bus voltage with 4.99 kΩ or tie to AGND if not used.
5	FB	Output voltage sensing pin. Connect this to the output voltage of the converter.
6	ADDR	This sets the I^2C address. A resistor connected to AGND sets the bus address.
7	VOUT	Output voltage of the regulator. Connect the output filter capacitance from this pin to PGND.
8, 16	PGND	Power ground for the device.
9	AGND	Analog or signal ground for the device. Reference ground for the internal control circuitry.
10	VCC	Supply voltage for the internal control circuitry. This can be used as an input for an external bias supply or as the bypass connection for the internal LDO.
11	VIN	Input voltage for the internal LDO regulator.
12,13,14,17	PVIN	Power input for the MOSFET switching circuit.
15	VSW	Switching node; test point.

1.1. Package

Figure 1-1. Package Type (Top View)



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2. Functional Description

2.1. Overview

The MCPF1606AM06 is a user-friendly, fully integrated, and highly efficient DC/DC regulator. Its operation, including output voltage and system optimization parameters, can be programmed via I^2C. It employs a proprietary modulator to provide rapid transient response. The modulator features internal compensation, allowing it to be used in a variety of applications with different types of output capacitors without encountering loop stability issues.

2.2. Bias Voltage

The MCPF1606AM06 features an integrated Low Drop-Out (LDO) regulator that supplies the DC bias voltage for its internal circuitry, typically outputting 5.2V. For single-rail operation with internal bias, connect the VIN pin to the PVIN pin (see Figure 2-1). If using an external bias voltage, connect the VIN pin to the VCC pin to bypass the internal LDO regulator (see Figure 2-2). The supply voltage, whether internal or external, increases with VIN and does not require enabling via the EN pin. Consequently, I^2C communication can commence once the following conditions are met:

- The VCC_UVLO start threshold is surpassed
- Memory contents are loaded
- Initialization is complete
- The address offset is read

Note: Until initialization is complete, a small leakage current (approximately 3.4 µA) will flow from the device to the output. This may significantly pre-bias the output voltage in applications with long VIN/VCC rise times. To prevent this, a small load capable of sinking 3.4 µA should be connected for such applications.

The I^2C bus can be pulled up to either VCC or a system I^2C bus voltage. The MCPF1606AM06 provides two ranges for the I^2C bus voltage, selectable via the user register bit BUS_VOLTAGE.

Register	Bits	Name and Description
0x1A	[1]	**Bus_Voltage_sel** 0: 1.8V to 2.5V (default) 1: 3.3V to 5V

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Figure 2-1. Single Supply Connection Using the Internal LDO and an External UVLO on PVIN via the EN Pin

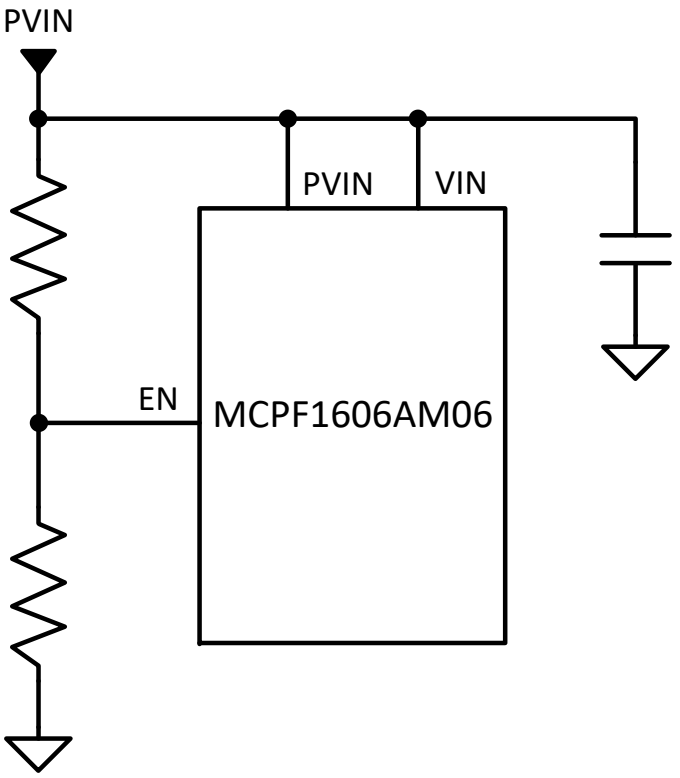
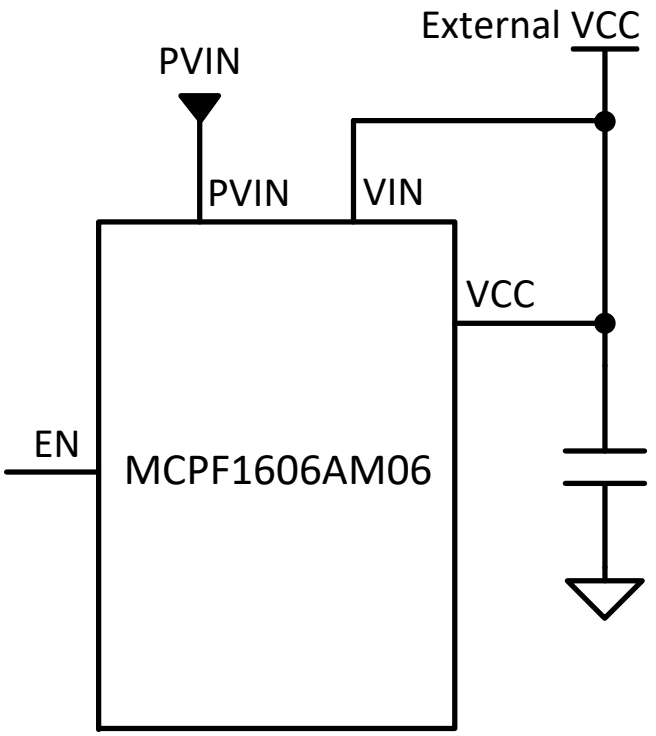


Figure 2-2. Using an External Bias Voltage



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2.3. I²C Addressing

The MCPF1606AM06 features a user register called BASE_ADDRESS (address 0x16), stored in memory, which determines its base I²C address. The default base address is 0x08. An offset ranging from 0 to 7 is set by connecting the ADDR pin to the AGND pin, either directly or via a 1% resistor. At startup, an address detector measures the resistance of this connection to determine the offset, which is then added to the base I²C address to establish the communication address for the I²C master device. To select offsets from 0 to 3, connect the pins as follows:

Resistor (kΩ)	Address offset
0	0
10	1
20	2
30.1	3
39	4
47	5
56	6
68	7

2.4. Soft Start and Output Voltage

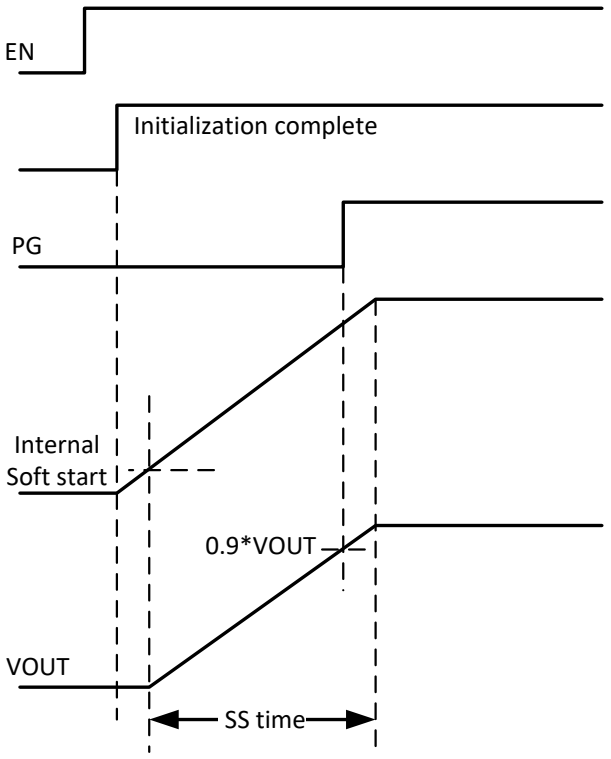
The MCPF1606AM06 features an internal digital soft start (SS) circuit that manages the rise time of the output voltage and limits the current surge during start-up. When VCC surpasses its start threshold ($VCC_{_UVLO(START)}$), the MCPF1606AM06 exits reset mode, initiating the loading of non-volatile memory contents into the working registers and calculating the address offset as previously described. After initialization is complete and the Enable (EN) pin is activated (Figure 2-3), the internal reference gradually ramps up to the target output voltage at a rate specified by the user register bit SS_rate (addres 0x14).

Register	Bits	Name and Description
0x14	[3]	**SS_rate** 0: 0.5V/ms (default) 1: 1V/ms

During initial start-up, the MCPF1606AM06 generates a minimal number of high-drive (HDrv) pulses until the output voltage rises (refer to Switching frequency and minimum values for ON-time, OFF-time). The ON-time is gradually increased until V_{OUT} achieves the target value specified by the user register bits VOUTH and VOUTL (registers 0x12 and 0x13).

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Figure 2-3. Soft Start Waveforms



Register	Bits	Name and Description
0x12	[0]	VOUTH - Vout high byte
0x13	[7:0]	VOUTL - Vout low byte

When using direct VOUT to FB connection to control the output voltage, VOUT can be adjusted in 5 mV increments for target voltages up to 1.8V. Use the following equation to determine the VOUT code to input into Vout high byte and Vout low byte, with all voltages in V:

$$VOUT_{code} = \frac{VOUT_{target} - \frac{0.4 \times resolution}{0.005}}{resolution}$$

As an example, to set VOUT to 1V, which is less than 1.8V and has a resolution of 5 mV, the following is used:

$$VOUT_{code} = \frac{1 - \frac{0.4 \times 0.005}{0.005}}{0.005} = 120$$

Converting the result to hexadecimal:

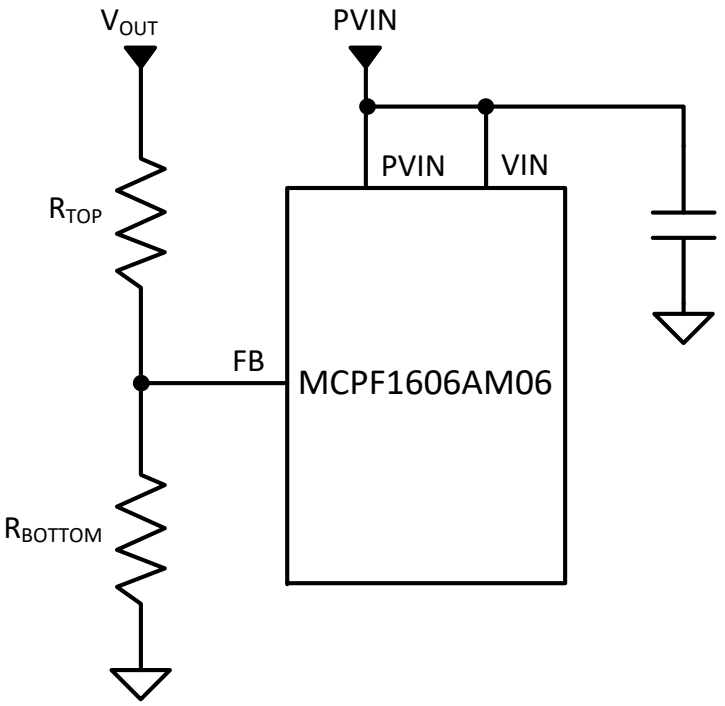
$120 = 0x078$
Overcurrent Protection (OCP) and Overvoltage Protection (OVP) are activated during the soft start phase to safeguard the MCPF1606AM06 from short circuits and excessive voltages.

For optimal system accuracy, it is recommended to set the output voltage by programming the user registers with the appropriate code. To achieve the best performance with this method, the output voltage change should not exceed ±20% of the default preset output voltage.

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Alternatively, an MCPF1606AM06 pre-programmed to 0.6V can be combined with a feedback resistor divider (Figure 2-4). This approach allows system designers the flexibility to configure all power rails within the output voltage range of 0.6V to 5V, with a maximum additional error of 1%.

Figure 2-4. Setting the Output Voltage With a Resistor Divider



The following equation outlines the correct resistor divider choice to establish the output voltage when using an MCPF1606AM06 set to 0.6V:

$$\frac{R_{TOP}}{R_{BOTTOM}} = 1.667 \times VOUT - 1 - 0.0000066R_{TOP}$$

The table details the divider ratio required to set VOUT when using an MCPF1606AM06 set to 0.6V. System designers are advised to place a feedforward capacitor ranging from 4.7 pF to 480 pF in parallel with R_{TOP}, which is recommended to be 4.12 kΩ. The appropriate value for R_{BOTTOM} varies based on the output voltage, as indicated in the following table.

Table 2-1. Divider Ratio Required to Set VOUT

VOUT (V)	R_{TOP} / R_{BOTTOM}	VOUT (V)	R_{TOP} / R_{BOTTOM}
0.65	0.0563	1.05	0.7331
0.70	0.1401	1.10	0.8063
0.72	0.1738	1.18	0.9321
0.80	0.3098	1.20	0.9763
0.85	0.3924	1.50	1.4714
0.90	0.4758	1.80	1.9619
0.95	0.5628	2.50	3.1692
1.00	0.6348	5.00	7.3309

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2.5. Pre-Bias Startup

The MCPF1606AM06 can start with a pre-charged output smoothly, avoiding oscillations and disturbances in the output voltage. During this startup, the Control and Synchronous MOSFETs remain off until the internal Soft-Start (SS) signal surpasses the sensed output voltage at the FB pin. At that moment, the first gate signal for the Control MOSFET is generated, followed by the complementary activation of the Synchronous MOSFET. The Power Good (PG) function becomes active only after this point.

2.6. Shutdown

The MCPF1606AM06 features two shutdown mechanisms:

1. **Hard Shutdown or Load-Dependent Decay**: Triggered by de-asserting the En pin. Both drivers are turned off, while the digital-to-analog converter (DAC) and soft-start are immediately pulled down.
2. **Soft-Stop or Controlled Ramp Down**: Activated by setting the user register bit SoftStopEnable to 1 and the user register bit Soft_Disable to 1. The SS signal decreases to 0 at the same rate it rises during startup, and the drivers are disabled only when it reaches 0. The output voltage follows the SS signal down to 0. The Soft_Disable bit should not be toggled while the part is enabled and switching. For applications requiring soft-stop, this bit must be set to 1, and with the EN pin asserted, the SoftStopEnable bit must be toggled to initiate soft-start or soft-stop. By default, both the Soft_Disable bit and the SoftStopEnable bit are set to 0, meaning soft-stop operation is disabled by default.

Register	Bits	Name and Description
0x14	[2]	SoftStopEnable
0x1C	[3]	Soft_Disable

2.7. Switching Frequency, Minimum ON-Time and Minimum OFF-Time, PVIN

The switching frequency of the MCPF1606AM06 varies based on the output voltage. For an output voltage of 1.8V, the nominal switching frequency is 1.97 MHz. If the output voltage is configured through user registers, the corresponding switching frequency is pre-programmed at the factory. When the output voltage is set using an external resistor divider, the switching frequency automatically adjusts to the correct value, as shown in table below:

V_{OUT} (V)	f_{SW} (MHz)
0.6	1.23
0.8	1.37
1.0	1.46
1.1	1.52
1.2	1.60
1.5	1.84
1.8	1.97
2.5	2.05
5.0	2.3

Thus, with either approach, system designers do not need to worry about selecting the switching frequency, reducing their design workload.

When the input voltage is high relative to the target output voltage, the Control MOSFET is switched ON for shorter durations, defined by the minimum ON-time ($T_{ON(MIN)}$). During start-up, when the output voltage is very low, the MCPF1606AM06 operates with this minimum ON-time.

Conversely, when the input voltage is low relative to the target output voltage, the Control MOSFET is switched on for longer durations. The shortest period it can be switched OFF is defined by the minimum off-time ($T_{OFF(MIN)}$). During this period, the Synchronous MOSFET remains ON, and its

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current is monitored for overcurrent protection. This determines the minimum input voltage that allows the device to regulate its output at the target voltage.

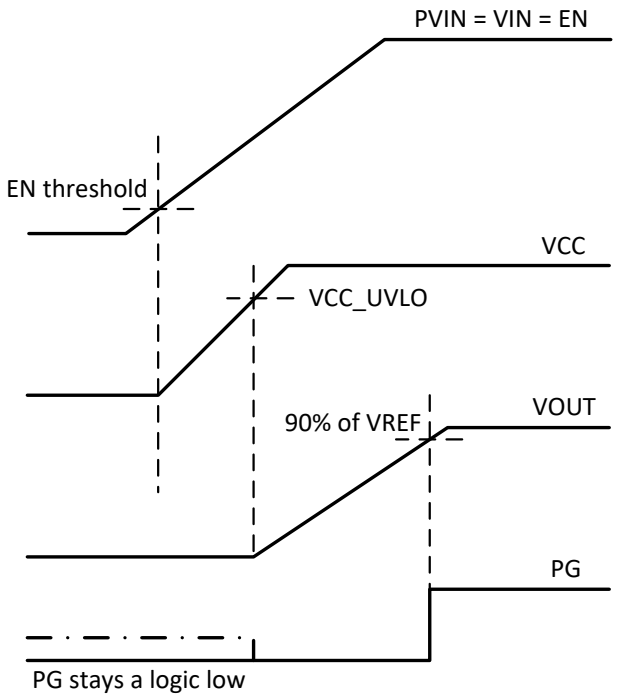
The figure below illustrates the minimum input voltage required for various typical output voltages. This curve assumes typical efficiency values; since efficiency impacts these values, system designers should verify them in their specific applications.

2.8. Enable Pin

The Enable (EN) pin serves multiple purposes:

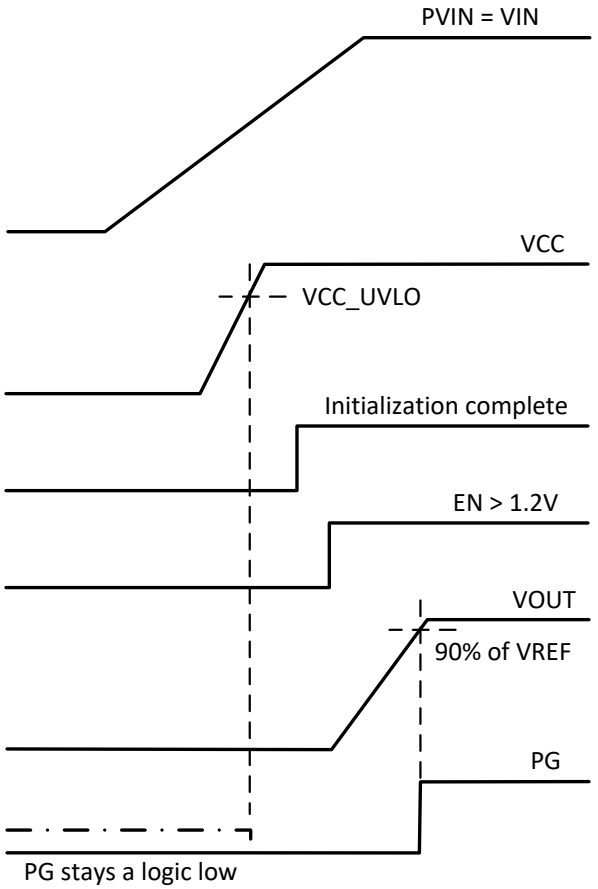
- It controls the on/off state of the MCPF1606AM06 using a precise threshold monitored by the UVLO circuit. An internal 1 MΩ resistor pulls the pin down if left floating, preventing unintentional activation of the MCPF1606AM06.
- It allows for the implementation of a precise input voltage UVLO. The EN pin input is derived from the PVIN voltage through a resistive divider (Figure 2-2). Users can set the UVLO threshold voltage by adjusting the divider ratio, ensuring the MCPF1606AM06 does not regulate when PVIN is below the desired level.
- It can be directly connected to PVIN without external resistive dividers for space-constrained designs, facilitating standalone start-up when no logic signal is available to enable the MCPF1606AM06 (Figure 2-5) or asserted separately (Figure 2-6).
- It can monitor other rails for specific power sequencing schemes.

Figure 2-5. Startup With PVIN, VIN and EN Pins Shorted Together



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Figure 2-6. Startup With EN Pin Asserted After PVIN and VIN are Established



To ensure VOUT rises and falls at the appropriate soft-start rate, proper sequencing is necessary:

- PVIN must be activated before V_{CC} and/or Enable.
- PVIN should only decrease after V_{CC} has dropped below its UVLO threshold and/or Enable has been de-asserted.

2.9. Overcurrent Protection

Overcurrent Protection (OCP) is achieved by monitoring the current through the $R_{DS(on)}$ of the low side MOSFET. When the current surpasses the OCP threshold, a fault condition is triggered. This approach offers several advantages:

- Ensures precise overcurrent protection without compromising converter efficiency (the current sensing is lossless)
- Lowers costs by removing the need for a current-sense resistor
- Minimizes layout-related noise issues

The threshold is determined by the appropriate bit settings in the register OCSet:

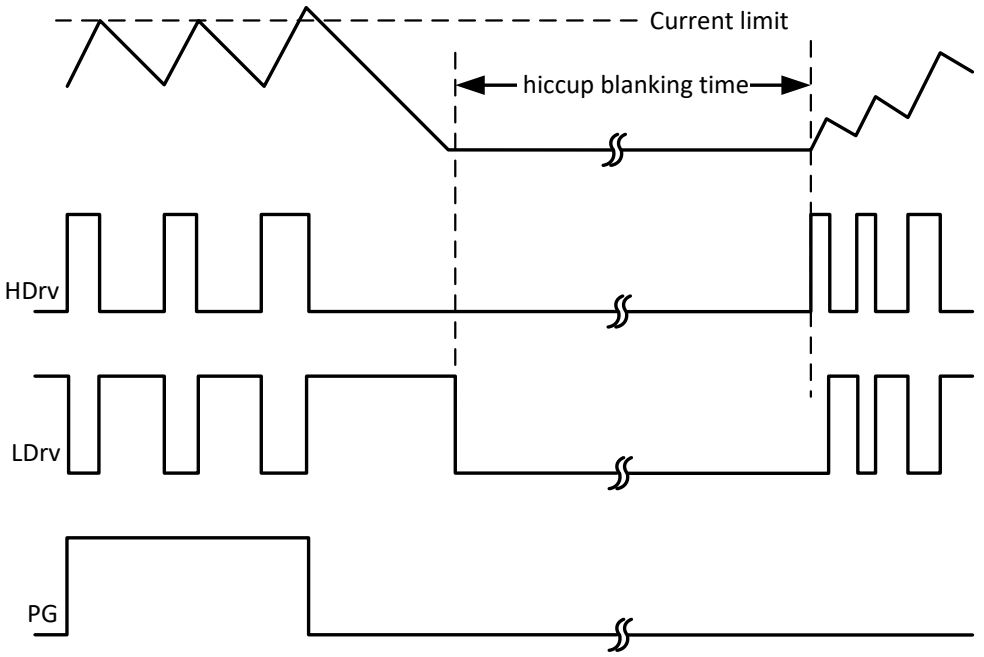
Register	Bits	Name and Description
0x15	[2:0]	**OCSet** 2: 8A (default), 1: 6A, 0: 4A

The threshold is internally adjusted to stay nearly constant across various ambient temperatures. When the current surpasses the OCP threshold, the PG and SS signals are pulled low. The

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Synchronous MOSFET stays on until the current drops to zero, after which the MCPF1606AM06 enters hiccup mode (see Figure 2-7). During the hiccup-blanking period, both the Control MOSFET and the Synchronous MOSFET remain off. Once this period ends, the MCPF1606AM06 attempts to restart. If an overcurrent fault persists, the previous actions are repeated and the MCPF1606AM06 continues in hiccup mode until the overcurrent fault is resolved.

Figure 2-7. Overcurrent and Hiccup Mode Operation



2.10. Overvoltage Protection

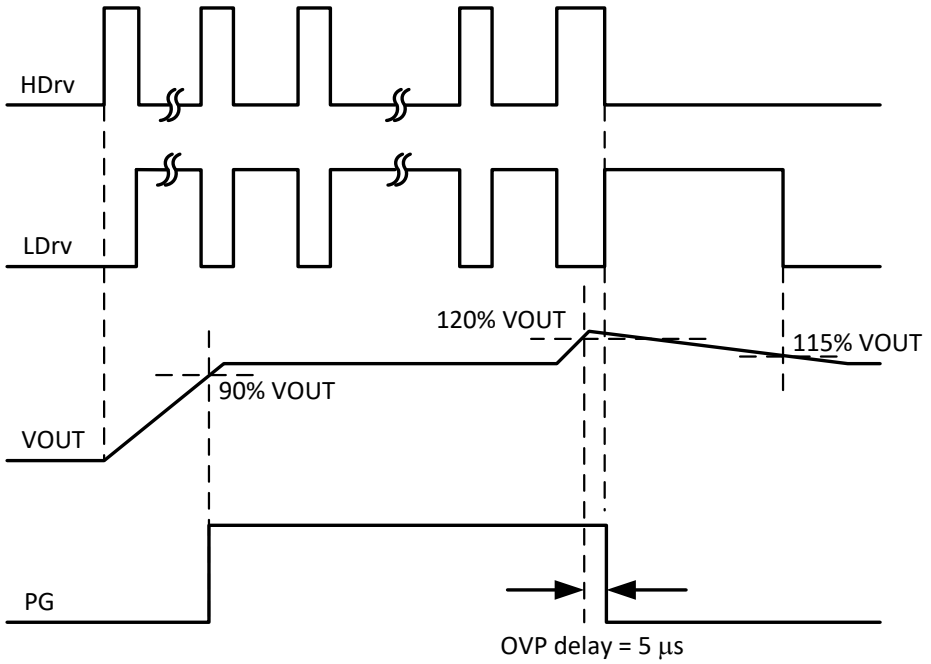
Overvoltage Protection (OVP) is achieved by monitoring the voltage at the FB pin. If the FB voltage surpasses the OVP threshold for more than the specified delay (typically 5 µs), a fault condition is triggered. The OVP threshold is set by the user through the OV_Threshold register bits.

Register	Bits	Name and Description
0x19	[1:0]	**OV_Threshold** 0: 105% of VOUT 1: 110% of VOUT 2: 115% of VOUT 3: 120% of VOUT (default)

When an over voltage condition is detected, the Control MOSFET is turned off immediately, the PG pin is pulled low, and the Synchronous MOSFET is activated to discharge the output capacitor. The Control MOSFET stays latched off until reset by cycling either VCC or EN. If the voltage at the FB pin drops below the output OVP threshold (with a 5% hysteresis), it does not turn on the Control MOSFET but does turn OFF the Synchronous MOSFET to prevent negative current build-up. The figure below illustrates a timing diagram for overvoltage protection.

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Figure 2-8. Latched OVP Response



2.11. Overtemperature Protection

The MCPF1606AM06 includes internal temperature sensing. The OTP threshold is set by the user through the OT_Threshold register bits.

Register	Bits	Name and Description
0x19	[1:0]	**OT_Threshold** 0: 75°C 1: 85°C 2: 125°C 3: 145°C (default)

When the temperature exceeds the threshold, thermal shutdown deactivates both MOSFETs and resets the internal soft start. The internal LDO regulator remains operational. Automatic restart occurs once the sensed temperature returns to the operating range. The OTP threshold includes a 25°C hysteresis.

2.12. Telemetry

The MCPF1606AM06 supports telemetry via the I²C interface, allowing parameters such as PVIN, V_{OUT}, Feedback (Fb), I_{OUT}, and temperature to be monitored. The resolution and range of the parameters monitored is show below:

Item	Resolution	Minimum	Maximum
V_{IN} (V)	0.0625	0	15.9375
V_{OUT} (V)V	0.01	0.6	2.5
I_{OUT} (A)	0.03126	0	6
Temperature (°C)	1	−40	145

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VIN Voltage

The value read from the part is 16 times the actual input voltage. The actual input voltage can be found by:

$$PVIN = \frac{Value}{16}$$

Where Value is the decimal equivalent of the value read from register 0x0C.

VOUT Voltage

The value read from the part will require some manipulation to arrive at the actual VOUT value. For the actual VOUT, read the value in register 0x0D. The actual output voltage can be calculated as below. Note that the telemetry for Vout is only effective up to 1.8V. Higher output voltages will not read correctly.

$$VOUT = Value \times 0.01 + 0.3$$

Where Value is the number (in decimal) returned by reading register 0x0D.

Temperature

Temperature is reported using register 0x0F, with each increment representing 1°C.

Current

To read the current, three values from the part need to be known:

- VOUT in decimal from above, keeping in mind that results are not reliable above 1.8V.
- The value from register 0x0E, representing the actual current telemetry value in decimal representation (IOUT_REP_DEC).
- The value from register 0x1A[7:2], (G_DEC) representing a calibration value that should not be changed on the part.

From this the output current can be calculated:

$$IOUT = \frac{\text{IOUT_REP_DEC}}{32} - (9.05 - 0.24 \times \text{G_DEC}) \times VOUT - 0.356 \times \text{G_DEC} + 13.1$$

2.13. Servo Loop Output Voltage Control

The MCPF1606AM06 uses an internal servo loop to control the output voltage precisely, resulting in 1% line and load regulation.

2.14. Power Good

The power good behavior is defined by the bit settings in the SS_PGOOD and PG_THRESHOLD registers:

Register	Bits	Name and Description
0x18	[1:0]	**PG_Threshold** 0: 80% of VOUT 1: 85% of VOUT 2: 90% of VOUT (default) 3: 95% of VOUT
0x14	[0]	**PG_Control** 1: Threshold based (default) 0: DAC Based

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PG_Threshold Bits

The PG_Threshold bit in the user register sets the PG threshold as a percentage of VOUT. A 5% hysteresis is applied, creating a lower threshold. When FB exceeds the upper threshold, the PG signal goes high. Conversely, when FB falls below the lower threshold, the PG signal goes low.

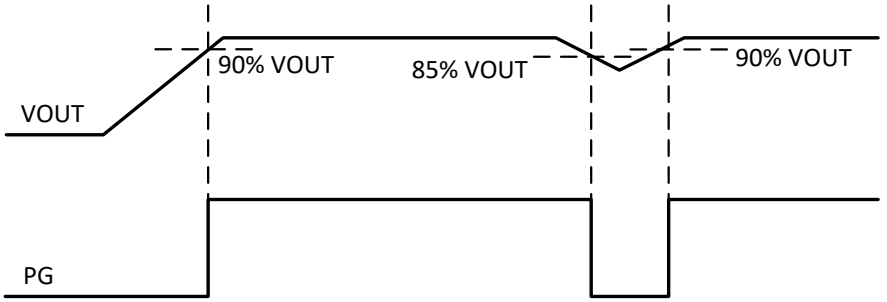
PG_Control bit set to 1 (default)

Figure 2-9 illustrates PG behavior under these conditions.

The behavior remains consistent during start-up and normal operation. The PG signal is asserted when:

- Both EN and VCC exceed their thresholds
- No faults are present (including over-current, over-voltage, and over-temperature)
- VOUT is within the target range (determined by continuously monitoring if FB is above the PG threshold)

Figure 2-9. PG Behavior When PG_Control Bit Set to 1



PG_Control bit set to 0

Figure 2-10 illustrates PG behavior under this condition.

During normal operation, the PG signal functions identically to when the PG_Control bit is set to 1.

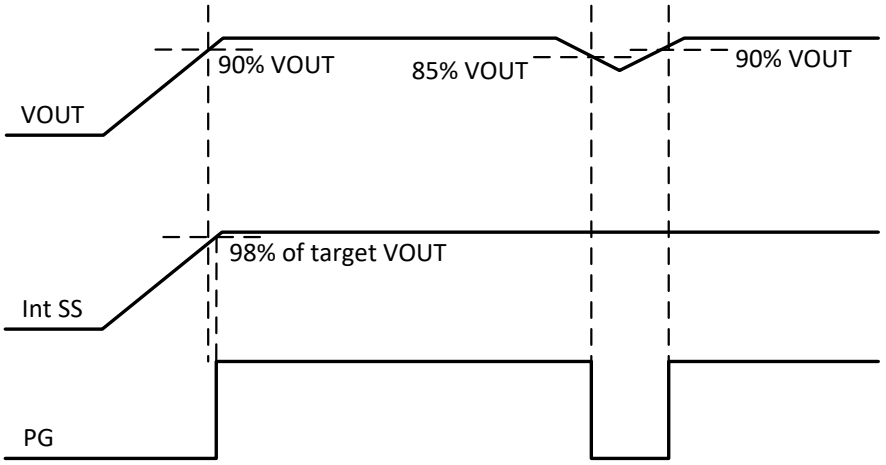
However, at start-up, the PG signal is asserted once the soft-start is within 2% of the target output voltage, rather than when FB surpasses the upper PG threshold.

For pre-biased start-up, the PG signal remains inactive until the first gate signal of the Control MOSFET is generated.

The MCPF1606AM06 also includes an additional PMOS in parallel with the NMOS, internally connected to the PG pin (Block Diagram). This PMOS ensures the PG signal remains at logic low, even if VCC is low and the PG pin is pulled up to an external voltage other than VCC (Figure 2-6 and Figure 2-7).

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Figure 2-10. PG Behavior When PG_Control Bit Set to 0



2.15. Registers

The list of registers and register map can be found below.

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2.15.1. Register Summary

> **⚠ WARNING** Bits marked as reserved (gray) should not be overwritten. Changing the state of these bits can have adverse effects on the part's operation. Preserve the state of reserved bits when writing to registers that contain them.

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x0B	Reserved									
0x0C	PVIN_REPORT	7:0	PVIN_REPORT[7:0]							
0x0D	VOUT_REPORT	7:0	VOUT_REPORT[7:0]							
0x0E	IOUT_REPORT	7:0	IOUT_REPORT[7:0]							
0x0F	TEMP_REPORT	7:0	TEMP_REPORT[7:0]							
0x10 ... 0x11	Reserved									
0x12	VOUT_HIGH_BYTE	7:0								VOUTH
0x13	VOUT_LOW_BYTE	7:0	VOUTL[7:0]							
0x14	SS_PGOOD	7:0					SS_Rate	SoftStopEnable		PG_Control
0x15	OC_SET	7:0						OCSet[2:0]		
0x16	BASE_ADDRESS	7:0	BaseAdd[7:0]							
0x17	OV_THRESHOLD	7:0							OV_Thresh[1:0]	
0x18	PG_THRESHOLD	7:0							PG_Thresh[1:0]	
0x19	OT_THRESH	7:0	CURRENT_REPORT_OFFSET[5:0]						OT_Thresh[1:0]	
0x1A	BUS_VOLTAGE	7:0							Bus Voltage	OV_RESPONSE
0x1B	Reserved									
0x1C	SOFT_DISABLE	7:0					Soft_Disable			
0x1D	NVM_BURN	7:0							OTP_on	VOUT_MAX_HIGH
0x1E	VOUT_MAX_LOW	7:0	VOUT_MAX_LOW[7:0]							
0x1F	Reserved									
0x20	TRIM_POINTER	7:0			Usr_ptr[5:3]			Trim_ptr[2:0]		
0x21	STATUS	7:0	STATUS_PGOOD	STATUS_OVP	STATUS_OCP	STATUS_OTP	STATUS_ENABLE	STATUS_NCL	CLEAR_STATUS_INDICATE	STATUS_OTP_BURN
0x22	FB_REPORT	7:0	FB_REPORT[7:0]							
0x23 ... 0x2A	Reserved									
0x2B	OTP_BURN	7:0	OTP_BURN[7:0]							
0x2C ... 0x30	Reserved									
0x31	CLEAR_STATUS	7:0	CLEAR_STATUS							

2.15.2. Register 0x0C

Name: PVIN_REPORT
Address: 0x0C
Default: varies based on PVIN
Property: R

This register is a representation of the PVIN voltage at the converter.

$$PVIN = \frac{Value}{16}$$

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Bit	7	6	5	4	3	2	1	0
	PVIN_REPORT[7:0]							
Access	R	R	R	R	R	R	R	R
Default	-	-	-	-	-	-	-	-

Bits 7:0 – PVIN_REPORT[7:0]

2.15.3. Register 0x0D

Name: VOUT_REPORT
Address: 0x0D
Default: varies based on VOUT
Property: R

This register is a representation of the output voltage of the converter. Interpreting this value depends on the actual output voltage as set by any external voltage divider that is used.

For VOUT < 1.8V:

$$VOUT = Value \times 0.01 + 0.3$$

Bit	7	6	5	4	3	2	1	0
	VOUT_REPORT[7:0]							
Access	R	R	R	R	R	R	R	R
Default	-	-	-	-	0	0	0	0

Bits 7:0 – VOUT_REPORT[7:0]

2.15.4. Register 0x0E

Name: IOUT_REPORT
Address: 0x0E
Default: varies based on IOUT
Property: R

This register is a representation of the output current. To interpret this register correctly requires reading register 0x1A and using the bits [7:2] (G_DEC) as a constant in the equation, and correctly using the results of the VOUT register calculation for register 0x0E (IOUT_REP_DEC).

$$IOUT = \frac{\text{IOUT_REP_DEC}}{32} - (9.05 - 0.24 \times \text{G_DEC}) \times VOUT - 0.356 \times \text{G_DEC} + 13.1$$

Bit	7	6	5	4	3	2	1	0
	IOUT_REPORT[7:0]							
Access	R	R	R	R	R	R	R	R
Default	-	-	-	-	0	0	0	0

Bits 7:0 – IOUT_REPORT[7:0]

2.15.5. Register 0x0F

Name: TEMP_REPORT
Address: 0x0F
Default: varies based on Junction Temperature
Property: R

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This register is a representation of the temperature of the part in degrees Celsius. The value read from this register is the device temperature.

Bit	7	6	5	4	3	2	1	0
	TEMP_REPORT[7:0]							
Access	R	R	R	R	R	R	R	R
Default	-	-	-	-	0	0	0	0

Bits 7:0 – TEMP_REPORT[7:0]

2.15.6. Register 0x12

Name: VOUT_HIGH_BYTE
Address: 0x12
Default: 0x0
Property: R/W

This register contains the high byte of the input to the DAC used to set the output voltage. This register and the VOUT_LOW_BYTE (0x13) register must be written in succession (atomically) for changes to be accepted.

Bit	7	6	5	4	3	2	1	0
								VOUTH
Access								R/W
Default								0

Bit 0 – VOUTH
VOUT high byte

2.15.7. Register 0x13

Name: VOUT_LOW_BYTE
Address: 0x13
Default: 0x29 (may vary)
Property: R/W

This register contains the low byte of the input to the DAC used to set the output voltage. This register and the VOUT_HIGH_BYTE (0x12) register must be written in succession (atomically) for changes to be accepted.

Bit	7	6	5	4	3	2	1	0
	VOUTL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	0	1	0	0	1

Bits 7:0 – VOUTL[7:0]
VOUT low byte

2.15.8. Register 0x14

Name: SS_PGOOD
Address: 0x14
Default: 0x01
Property: R/W

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This register sets the soft start rate, controls whether soft stop is used and sets the PGOOD behavior.

Bit	7	6	5	4	3	2	1	0
					SS_Rate	SoftStopEnable		PG_Control
Access					R/W	R/W		R/W
Default					0	0		1

Bit 3 – SS_Rate

Controls the startup ramp rate of VOUT:

Value	Description
1	1.0V/ms
0	0.5V/ms (default)

Bit 2 – SoftStopEnable

Enables shutdown by the soft disable bit, Register 0x1C[3].

Value	Description
1	Soft stop enabled
0	Soft stop disabled (default)

Bit 0 – PG_Control

Sets the power good function to be either DAC-based or threshold-based. See Power Good section.

Value	Description
1	Threshold based (default)
0	DAC based

2.15.9. Register 0x15

Name: OC_SET
Address: 0x15
Default: 0x02
Property: R/W

This register sets the overcurrent threshold for the device.

Bit	7	6	5	4	3	2	1	0
						OCSet[2:0]		
Access						R/W	R/W	R/W
Default						0	1	0

Bits 2:0 – OCSet[2:0]

Bits [2:0] set the overcurrent threshold for the device. Thresholds are set to support the nominal outputs currents below:

Value	Description
000	4A
001	6A
010	8A (default)
Other	Invalid selection

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2.15.10. Register 0x16

Name: BASE_ADDRESS
Address: 0x16
Default: 0x08
Property: R/W

This register sets the base address that the part uses for I^2C communication. Offsets applied with the ADDR pin are added to this address to determine the I^2C address of the part.

Bit	7	6	5	4	3	2	1	0
	BaseAdd[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	1	0	0	0

Bits 7:0 – BaseAdd[7:0]
I^2C default address

2.15.11. Register 0x17

Name: OV_THRESHOLD
Address: 0x17
Default: 0x03
Property: R/W

This register sets the output over voltage threshold for the part.

Bit	7	6	5	4	3	2	1	0
							OV_Thresh[1:0]	
Access							R/W	R/W
Default							1	1

Bits 1:0 – OV_Thresh[1:0]
Sets the overvoltage threshold for the converter:

Value	Description
00	105%
01	110%
10	115%
11	120 % (default)

2.15.12. Register 0x18

Name: PG_THRESHOLD
Address: 0x18
Default: 0x02
Property: R/W

This register sets the threshold where power good is asserted.

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Bit	7	6	5	4	3	2	1	0
							PG_Thresh[1:0]	
Access							R/W	R/W
Default							1	0

Bits 1:0 – PG_Thresh[1:0]
Sets the power good threshold for the converter:

Value	Description
00	80%
01	85%
10	90% (default)
11	95 %

2.15.13. Register 0x19

Name: OT_THRESH
Address: 0x19
Default: Bits[7:2] - varies; Bits[1:0] - 0b11
Property: R/W

This register sets the temperature threshold where the part shuts down.

Bit	7	6	5	4	3	2	1	0
	CURRENT_REPORT_OFFSET[5:0]						OT_Thresh[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	1	1

Bits 7:2 – CURRENT_REPORT_OFFSET[5:0]
This is an offset that is applied to IOUT_REPORT. The value is 2's complement and has a resolution of 0.0625A.

Bits 1:0 – OT_Thresh[1:0]
Sets the overtemperature threshold for the converter:

Value	Description
00	75°C
01	85°C
10	125°C
11	145°C (default)

2.15.14. Register 0x1A

Name: BUS_VOLTAGE
Address: 0x1A
Default: 0x02
Property: R/W

This register sets the bus voltage used by the I^2C interface and the overvoltage response of the part.

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Bit	7	6	5	4	3	2	1	0
							Bus Voltage	OV_RESPONSE
Access							R/W	R/W
Default							1	0

Bit 1 – Bus Voltage

Controls bus voltage:

Value	Description
1	3.3–5V (default)
0	1.8–2.5V

Bit 0 – OV_RESPONSE

Sets the response to an overvoltage event.

Value	Description
1	Not latched
0	Latched (default)

2.15.15. Register 0x1C

Name: SOFT_DISABLE
Address: 0x1C
Default: 0x00
Property: R/W

This register allows control of soft disable or hard shutdown of the part. This disable function is gated by the soft stop enable bit, register 0x14 [3].

Bit	7	6	5	4	3	2	1	0
					Soft_Disable			
Access					R/W			
Default					0			

Bit 3 – Soft_Disable

Controls soft disable function:

Value	Description
1	Soft disable is enabled
0	Soft disable is not enabled (default)

2.15.16. Register 0x1D

Name: NVM_BURN
Address: 0x1D
Default: 0x02
Property: R/W

This register enables the burning of current part settings into non-volatile memory. The writing of NVM requires a 0 to 1 transition to take place so the bit must be cleared and then set to 1. Section Writing NVM describes the procedure.

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Bit	7	6	5	4	3	2	1	0
							OTP_on	VOUT_MAX_HIGH
Access	-	-	-	-	-	-	R/W	R/W
Default	0	0	0	0	0	0	1	0

Bit 1 – OTP_on

Enable OTP burn:

Value	Description
1	Burn an NVM bank (requires a 0 to 1 transition, default)
0	Do not burn NVM

Bit 0 – VOUT_MAX_HIGH

This is the high order bit of a value that restricts the range of VOUT_HIGH_BYTE and VOUT_LOW_BYTE in registers 0x12 and 0x13.

2.15.17. Register 0x1E

Name: VOUT_MAX_LOW
Address: 0x1E
Default: 0xC8
Property: R/W

This register contains the low byte of a value that restricts the range of VOUT_HIGH_BYTE and VOUT_LOW_BYTE in registers 0x12 and 0x13.

Bit	7	6	5	4	3	2	1	0
	VOUT_MAX_LOW[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	0	0	1	0	0	0

Bits 7:0 – VOUT_MAX_LOW[7:0]

2.15.18. Register 0x20

Name: TRIM_POINTER
Address: 0x20
Default: 0x09
Property: R

This register shows the remaining NVM banks left available for writing. It has a pointer to the last bank of NVM burned on the controller, in the converter. There are 4 banks, one of which was used to trim the part at the factory, leaving 3 banks for the user to utilize.

Bit	7	6	5	4	3	2	1	0
			Usr_ptr[5:3]			Trim_ptr[2:0]		
Access			R	R	R	R	R	R
Default			0	0	1	0	0	1

Bits 5:3 – Usr_ptr[5:3]

Indicates the number of writes left:

Value	Description
000	4 open banks (will not be seen)

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Value	Description
001	3 open banks (default for new parts)
010	2 open banks
011	1 open banks
100	No open banks left; NVM has been fully used.

Bits 2:0 – Trim_ptr[2:0]

2.15.19. Register 0x21

Name: STATUS
Address: 0x21
Default: 0x88
Property: R

This register has several read only indicator bits that show the status of the part at any given time. Some bits are latched and indicate that an event that has occurred, while others reflect the current state of the part.

Bit	7	6	5	4	3	2	1	0
	STATUS_PGOOD	STATUS_OVP	STATUS_OCP	STATUS_OTP	STATUS_ENABLE	STATUS_NCL	CLEAR_STATUS_INDICATE	STATUS_OTP_BURN
Access	R	R	R	R	R	R	R	R
Default	1	0	0	0	0	0	0	0

Bit 7 – STATUS_PGOOD Power Good status
This bit is not latched indicates the current real time status of the part.

Value	Description
1	PGOOD is asserted.
0	PGOOD is not asserted.

Bit 6 – STATUS_OVP Overvoltage status
This bit is latched and indicates that an overvoltage event has occurred since the last status reset or power-up.

Value	Description
1	An overvoltage event has occurred.
0	An overvoltage event has not occurred.

Bit 5 – STATUS_OCP Overcurrent status
This bit is latched and indicates that an overcurrent event has occurred since the last status reset or power-up.

Value	Description
1	An overcurrent event has occurred.
0	An overcurrent event has not occurred.

Bit 4 – STATUS_OTP Overtemperature status
This bit is latched and indicates that an overtemperature event has occurred since the last status reset or power-up.

Value	Description
1	An overtemperature event has occurred.
0	An overtemperature event has not occurred.

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Bit 3 – STATUS_ENABLE Overtemperature status
This bit is not latched indicates the current real-time status of the part.

Value	Description
1	ENABLE is asserted.
0	ENABLE is not asserted.

Bit 2 – STATUS_NCL Negative overcurrent status
This bit is latched and indicates that a negative overcurrent event has occurred since the last status reset or power-up.

Value	Description
1	A negative overcurrent event has occurred.
0	A negative overcurrent event has not occurred.

Bit 1 – CLEAR_STATUS_INDICATE CLEAR_STATUS bit status
This bit shows the status of the CLEAR_STATUS bit in register 0x31.

Value	Description
1	The CLEAR_STATUS bit is set.
0	The CLEAR_STATUS bit is not set.

Bit 0 – STATUS_OTP_BURN Non-volatile memory write status
This bit shows the status of the last attempt to write to the non-volatile memory.

Value	Description
1	Write was successful.
0	Write was not successful.

2.15.20. Register 0x22

Name: FB_REPORT
Address: 0x22
Default: -
Property: R

This register is the output of an ADC reading of the FB pin voltage.

Bit	7	6	5	4	3	2	1	0
	FB_REPORT[7:0]							
Access	R	R	R	R	R	R	R	R
Default	-	-	-	-	-	-	-	-

Bits 7:0 – FB_REPORT[7:0]

2.15.21. Register 0x2B

Name: OTP_BURN
Address: 0x2B
Default: 0x00
Property: R/W

This register is used to start a write procedure to the non-volatile memory.

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Bit	7	6	5	4	3	2	1	0
	OTP_BURN[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bits 7:0 – OTP_BURN[7:0]

The **0x15** value is used to start a write to the non-volatile memory. Any other value will result in no action.

2.15.22. Register 0x31

Name: CLEAR_STATUS
Address: 0x31
Default: 0x00
Property: R/W

This register contains a bit that will clear the status indicator bits in register 0x21 once the fault conditions is no longer present.

Bit	7	6	5	4	3	2	1	0
	CLEAR_STATUS							
Access	R/W							
Default	0							

Bit 7 – CLEAR_STATUS

Clears the status indicator bits in register 0x21.

2.16. Writing NVM

The following procedure should be used to write the NVM on the converter:

1. Once all registers have been set to desired values, verify the register contents and save those values for later comparison after the NVM write.
2. Read register 0x20 and read bit[5:3]. If the value of that bit field is less than 100b, there is at least one bank of NVM that can be written to. If the value is 100b, there are no more banks of NVM and the write cannot be performed.
3. Pull the EN pin low.
4. Apply 7.5V to the VIN pin.
5. Write 0x15 to register 0x2B.
6. Read register 0x21. If bit [1] is set, the write completed successfully.
7. Power cycle the part.
8. Verify that the contents of the NVM match the values set at the start of the write procedure.
9. If steps 6 or 8 fail, repeat steps 1 through 7. If this fails a second time, discard the part and debug the procedure.

2.17. Trimming to a Specific VOUT Without Using a Voltage Divider

The part can be used without a voltage divider and still set to a specific output voltage. In this case, VOUT is connected directly to FB. Setting the output voltage must be done closed loop using this procedure:

1. The ideal code is:

$$code = \frac{VOUT_{tgt} - 0.4}{0.005}$$

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Where:

- $VOUT_{tgt}$ is the target output voltage

2. Write this code to registers 0x12 and 0x13
3. Measure VOUT
4. Calculate the error code:

$$code_{err} = \frac{VOUT_{tgt} - VOUT}{0.005}$$

Where:

- $code_{err}$ is the error code
- $VOUT_{tgt}$ is the target output voltage
- VOUT is the output voltage measured in step 3

5. Adjust the code written to registers 0x12 and 0x13 by the error code:
$code_{new} = code + code_{err}$
6. Measure VOUT and adjust the code in registers 0x12 and 0x13 until the measured output voltage is satisfactory.

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3. Electrical Characteristics

3.1. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
PVIN, VIN, EN to PGND (1)		−0.3	18	V
VCC to PGND (2)		−0.3	6	V
FB, PG, ADDR, SCL, SDA to AGND (2)		−0.3	VCC	V
PGND to AGND		−0.3	0.3	V
Maximum Junction Temperature	T_J	−40	150	°C
Storage Temperature	T_S	−55	150	°C
ESD HBM JESD22-A114		2 kV		—
Moisture Sensitivity Rating (JEDEC, J-STD-020D)		MSL 3		—

Notes:

1. PGND and AGND pins are connected together.
2. Must not exceed 6V.

⚠ WARNING Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

3.2. Operating Ratings

Parameters (1)	Symbol	Min.	Max.	Unit
Input Voltage Range with External VCC (2, 4)	PVIN	2.5	16	V
Input Voltage Range with Internal LDO (3, 4)	PVIN, VIN	4.5	16	V
Supply Voltage Range (5)	V_{CC}	4.5	5.5	V
Output Voltage Range	V_{OUT}	0.6	5	V
Continuous Output Current Range	I_O	0	6	A
Operating Junction Temperature Range	T_J	−40	125	°C

Notes:

1. The device is not guaranteed to operate outside its operating ratings.
2. VIN is connected to VCC to bypass the internal Low Drop-Out (LDO) regulator.
3. VIN is connected to PVIN (for single-rail applications with PVIN = VIN = 4.5V−5.5V).
4. Maximum switch node voltage should not exceed 22V.
5. Must not exceed 6V.

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3.3. DC/AC Specifications

Electrical Characteristics: 4.5V < PVIN = VIN < 16V, 0°C < T < 125°C unless specified otherwise, Typicals at T_A = 25°C						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max**	**Units**	**Conditions**
Input Current						
VIN Supply Current (Standby)	$I_{IN(STANDBY)}$	—	2	—	mA	Enable low
VIN Supply Current (Static)	$I_{IN(STATIC)}$	—	3	—	mA	No switching, EN = 2V
VIN Supply Current (Dynamic)	$I_{IN(DYN)}$	—	14.6	18.6	mA	Enable high, f_{SW} = 1.35 MHz, VIN = 12V, VOUT = 1.8V
Soft Start						
Rate(1)	SS_{RATE} (default)	—	0.5	—	V/ms	
Output Voltage						
Range	FB voltage (default)	—	0.6	—	V	
	$VOUT_{RES}$ (resolution)	—	5	—	mV	
Accuracy(2)		−0.5	—	0.5	%	T_J = 25°C, PVIN = 12V, FB = 0.6V
		−1	—	1	%	−40°C < T_J < 125
On Time Control						
On Time	T_{ON}	33	41	47	ns	PVIN = 12V, VOUT = 0.6V, f_{SW} = 1.35 MHz
Minimum ON Time(1)	$T_{ON(MIN)}$	—	30	—	ns	
Minimum OFF Time	$T_{OFF(MIN)}$	—	120	150	ns	PVIN = 0.6V
Internal LDO Regulator						
Output Voltage	VCC	4.9	5.2	5.5	V	5.5V < V_{IN} < 16V, 0-20 mA
		4.3	—	—	V	4.5V < V_{IN} < 5.5V, 0-20 mA
Thermal Shut Down						
Shutdown Temperature	T_{SD}	—	145	—	C	Default
Hysteresis		—	25	—	C	
Under Voltage Lock Out						
Start Threshold	$VCC_{_UVLO(START)}$	3.95	4.15	4.35	V	VCC rising
Stop Threshold	$VCC_{_UVLO(STOP)}$	3.6	3.8	3.95	V	VCC falling
Enable Threshold	$EN_{(HIGH)}$	1.1	1.2	1.3	V	Ramping up
	$EN_{(LOW)}$	0.9	1.0	1.06	V	Ramping Down
En Pin Input Impedance	R_{EN}	500	1000	1500	kΩ	
Current Limit						
Threshold	I_{OC} (default)	8.3	9	9.7	A	T_J = 25°C, PVIN = 12V, VOUT = 0.6V
Hiccup Timeout	T_{HICCUP}	—	20	—	ms	
Overvoltage Protection						
Threshold(1)	V_{OVP} (default)	115	120	125	%	VOUT = 1.8V
Delay	T_{OVPDEL}	—	5	—	µs	
Power Good						
Upper Threshold	$V_{PG(UPPER)}$	86	90	95	%	VOUT rising to 0.6V
Hysteresis	$V_{PG(HYST)}$	—	5	—	%	VOUT falling from 0.6V
PG Pin Sink Current	I_{PG}	—	9	—	mA	V_{PG} = 0.5V, V_{EN} = 2V
Telemetry						

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DC/AC Specifications (continued)

Electrical Characteristics: 4.5V < PVIN = VIN < 16V, 0°C < T < 125°C unless specified otherwise, Typicals at T_A = 25°C						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max**	**Units**	**Conditions**
Input Voltage Report Accuracy	$PVIN_{rep}$	−0.8	—	0.8	%	PVIN = 12V, T_J = 25°C
		−1.5	—	1.5	%	5V < PVIN < 16V, −40°C < T_J < 125°C, note 1
Output voltage report accuracy	$VOUT_{rep}$	−2.5	—	2.5	%	V_{OUT} = V_{FB} = 0.6V, T_J = 25°C
		−2.2	—	2.2	%	1V ≤ V_{FB} ≤ 2.5V, −40°C < T_J < 125°C, note 1
Output current report accuracy	$IOUT_{rep}$	0	—	450	mA	PVIN = 12V, T_J = 25°C, 1V ≤ V_{OUT} = V_{FB} ≤ 2.5V, I_{OUT} = 0A
		0	—	550	mA	PVIN = 12V, −40°C < T_J < 125°C, 1V ≤ V_{OUT} = V_{FB} ≤ 2.5V, I_{OUT} = 0A, note 1
Temperature report accuracy	T_{rep}	−10	—	10	°C	−40°C < T_J < 125°C

Notes:

1. Characterized parameter, not production tested.
2. Only production tested at 25°C. Limits over temperature are characterized only.

Electrical Characteristics: 4.5V < PVIN = VIN < 16V, 0°C < T < 125°C unless specified otherwise, Typicals at T_A = 25°C							
Parameter(1 – all parameters)	**Symbol**	**Fast-mode**		**Fast-mode Plus**		**Unit**	**Conditions**
		Min	**Max**	**Min**	**Max**		
I²C Parameters							
I²C Bus Voltage	V_{BUS}	1.8	5.5	1.8	5.5	V	
Vin Low	V_{IL}	−0.5	0.3*V_{BUS}	−0.5	0.3*V_{BUS}	V	
Vin High	V_{IH}	0.7*V_{BUS}	—	0.7*V_{BUS}	—	V	
Input Hysteresis	V_{HYS}	0.05*V_{BUS}	—	0.05*V_{BUS}	—	V	
Low Level Output Voltage 1	V_{OL1}	0	0.4	0	0.4	V	3 mA sink current, V_{BUS} > 2V
Low Level Output Voltage 2	V_{OL2}	0	0.2* V_{BUS}	0	0.2* V_{BUS}	V	2 mA sink current, V_{BUS} < 2V
Low level sink Current	I_{OL}	3	—	3	—	mA	V_{OL} = 0.4V
		6	—	6	—	mA	V_{OL} = 0.6V
Output Fall Time	T_{OF}	20*(V_{BUS}/5.5)	250	20*(V_{BUS}/5.5)	125	ns	
Max Noise Spike Width	T_{SP}	0	50	0	50	ns	
Input current each I/O pin	I_I	−10	10	−10	10	µA	
Input Capacitance	C_I	—	10	—	10	pF	
SCL Frequency	F_{SCL}	0	400	0	1000	kHz	
Repeated Start Hold Time	$T_{HD;STA}$	0.6	—	0.26	—	µs	
SCL Low Time	T_{LOW}	1.3	—	0.5	—	µs	
SCL High Time	T_{HIGH}	0.6	—	0.26	—	µs	
Repeated Start Setup Time	$T_{SU;STA}$	0.6	—	0.26	—	µs	
Data Hold Time	$T_{HD;DAT}$	0	—	0	—	µs	

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DC/AC Specifications (continued)

Electrical Characteristics: 4.5V < PVIN = VIN < 16V, 0°C < T < 125°C unless specified otherwise, Typicals at T_A = 25°C							
Parameter[1 – all parameters]	**Symbol**	**Fast-mode**		**Fast-mode Plus**		**Unit**	**Conditions**
		Min	**Max**	**Min**	**Max**		
Data Setup Time	$T_{SU;DAT}$	100	—	50	—	ns	
SDA, SCL Rise Time	T_R	20	300	—	120	ns	
SDA, SCL Fall Time	T_F	20*(V_{BUS}/5)	300	20*(V_{BUS}/5)	120	ns	
STOP setup Time	$T_{SU;STO}$	0.6	—	0.26	—	µs	
Bus Free Time between STOP and START	T_{BUF}	1.3	—	0.5	—	µs	
Bus Capacitive Load	C_{BUS}	—	400	—	550	pF	
Data Valid Time	$T_{VD;DAT}$	—	0.9	—	0.45	µs	
Data Valid ACK Time	$T_{VD;ACK}$	—	0.9	—	0.45	µs	
Noise Margin at LOW Level	V_{NL}	0.1*V_{BUS}	—	0.1*V_{BUS}	—	V	
Noise Margin at HIGH Level	V_{NH}	0.2*V_{BUS}	—	0.2*V_{BUS}	—	V	
SDA Timeout	T_{TO}	200	—	200	—	µs	

Note:

1. Characterized parameter, not production tested.

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4. Typical Performance Curves

The graphs and tables provided in this section are a statistical summary, based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Important: Unless otherwise stated, PVIN = 12V, VOUT = 1.8V.

Figure 4-1. VOUT vs. Temperature, VOUT = 0.6V

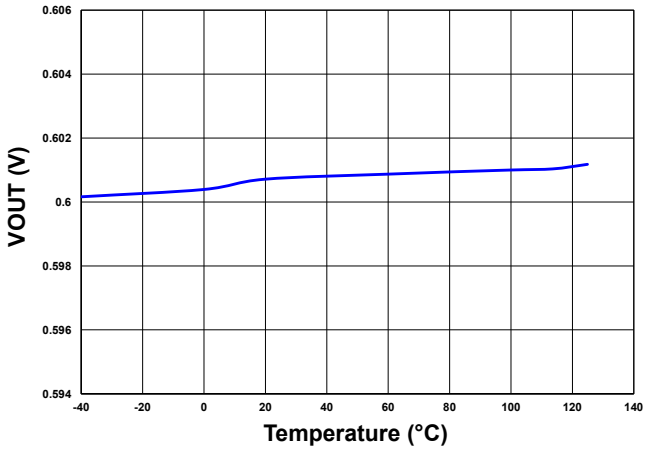


Figure 4-2. I_{IN} Supply Current vs. Temperature

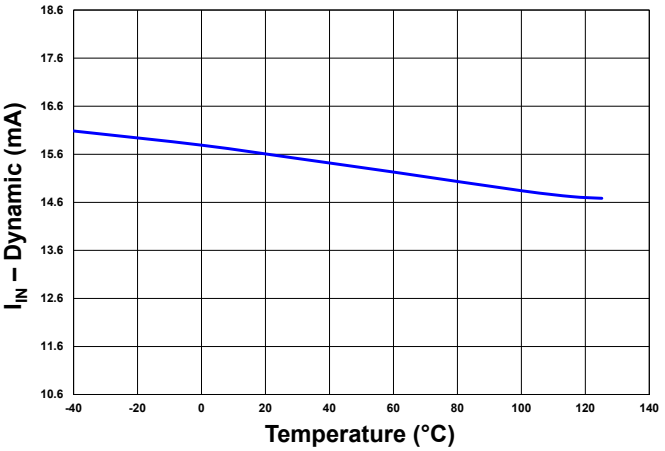


Figure 4-3. EN Start Threshold vs. Temperature

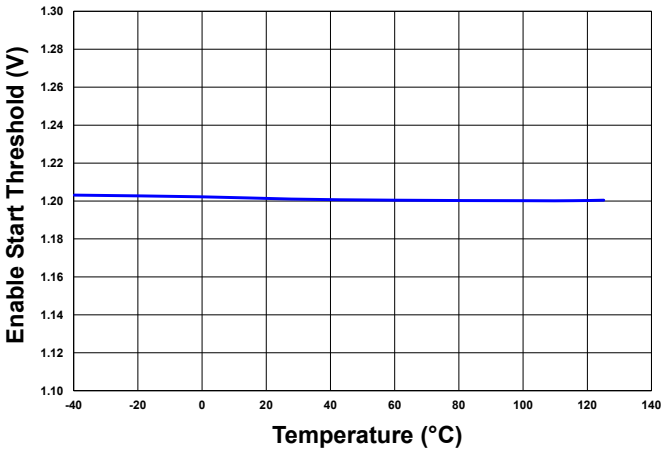
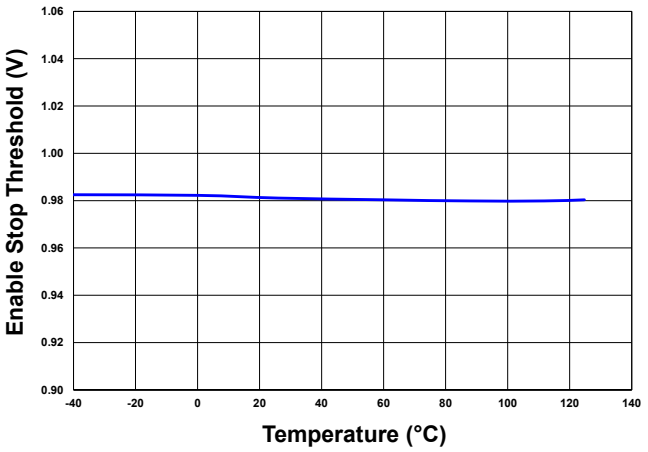


Figure 4-4. EN Stop Threshold vs. Temperature



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Figure 4-5. VCC Start Threshold vs. Temperature

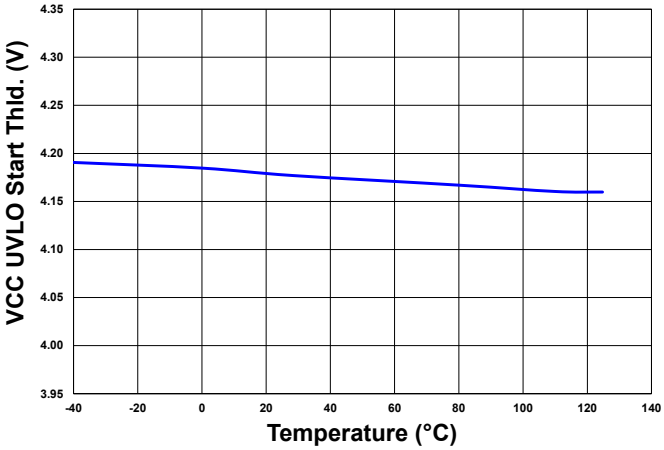


Figure 4-6. VCC Stop Threshold vs. Temperature

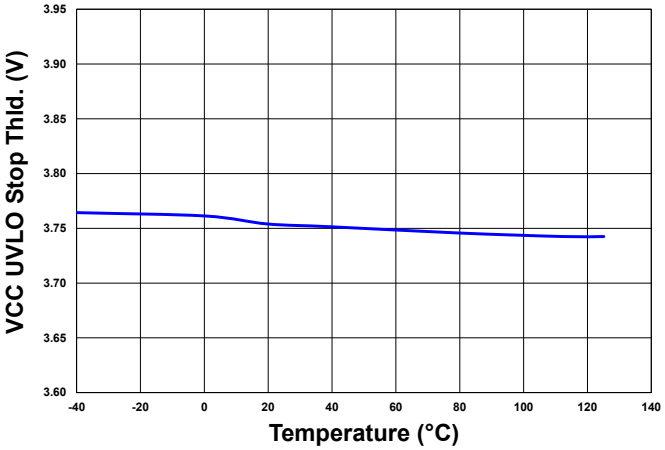


Figure 4-7. ON Time vs. Temperature, VOUT = 0.6V

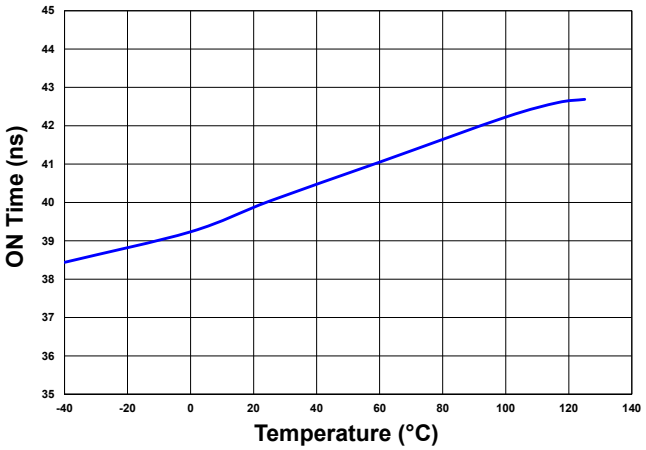


Figure 4-8. Switching Frequency vs. Temperature, VOUT = 0.6V

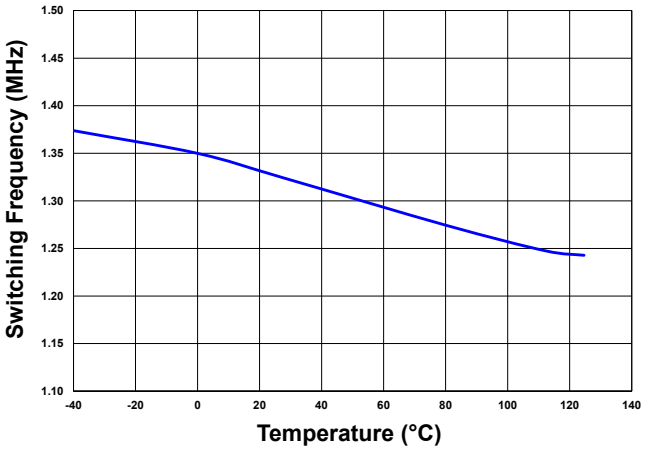


Figure 4-9. Soft Start Rate vs. Temperature

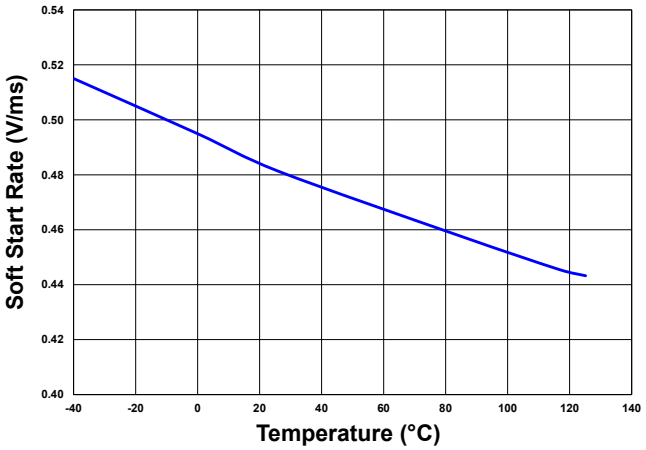
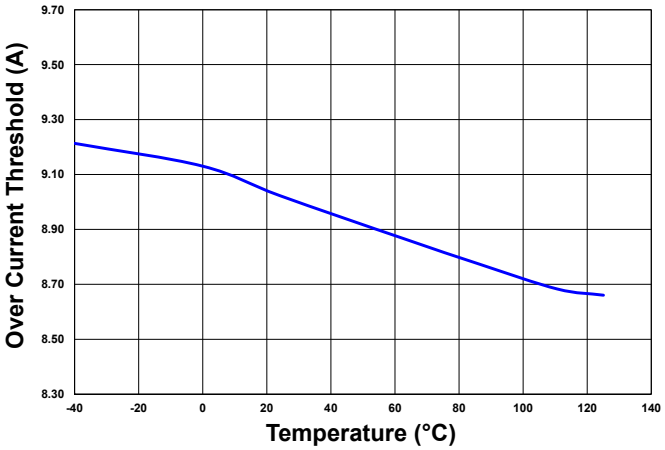


Figure 4-10. Current Limit vs. Temperature



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Figure 4-11. Efficiency, PVIN = 12V, Using Internal LDO

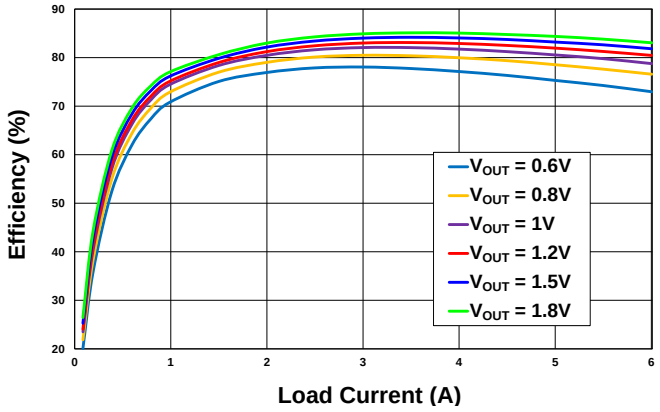


Figure 4-12. Power Loss, PVIN = 12V, Using Internal LDO

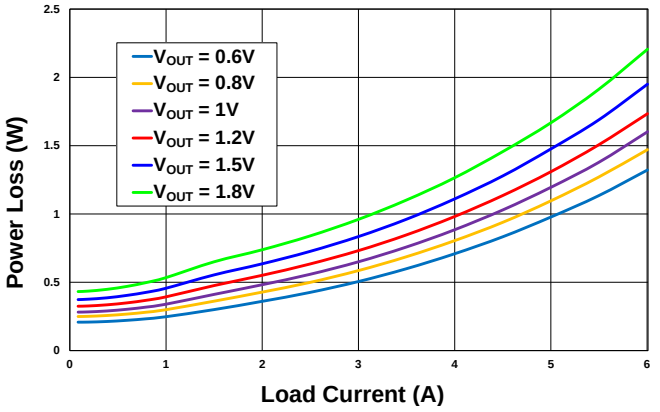


Figure 4-13. Efficiency, PVIN = VIN = VCC = 5V

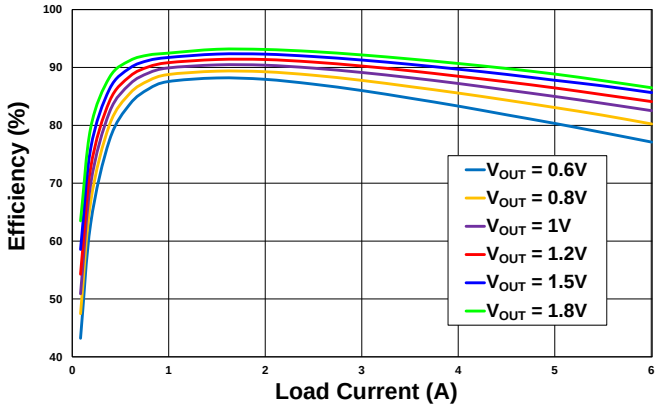


Figure 4-14. Power Loss, PVIN = VIN = VCC = 5V

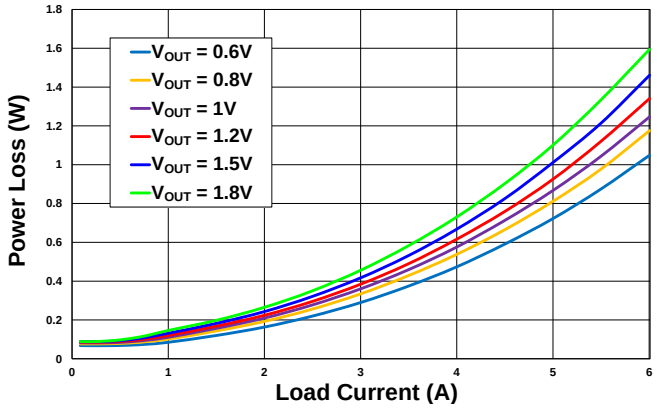


Figure 4-15. Load Regulation, PVIN = 12V, Using Internal LDO, Room Temperature and no Air Flow

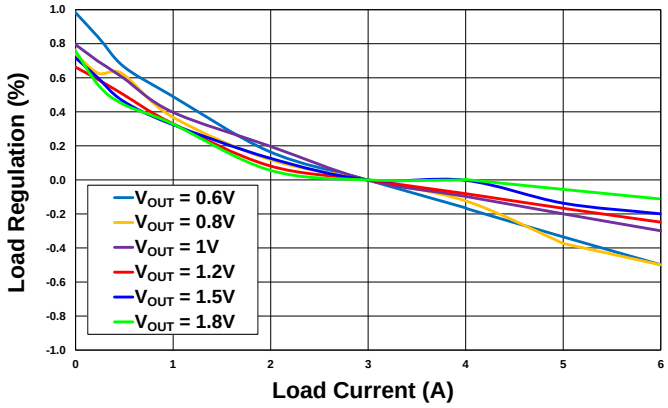
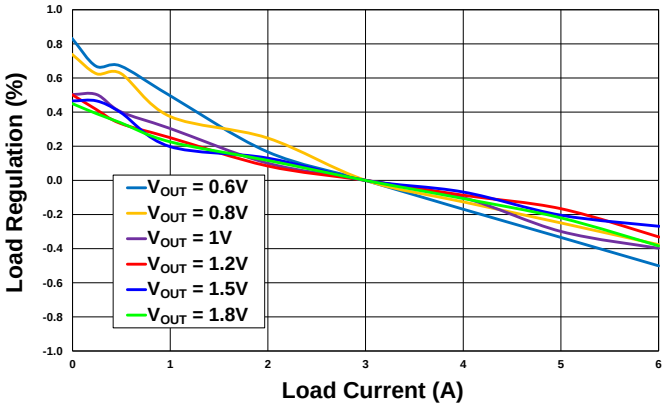


Figure 4-16. Load Regulation, PVIN = VIN = VCC = 5V, Room Temperature and no Air Flow



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Figure 4-17. Startup Into no Load

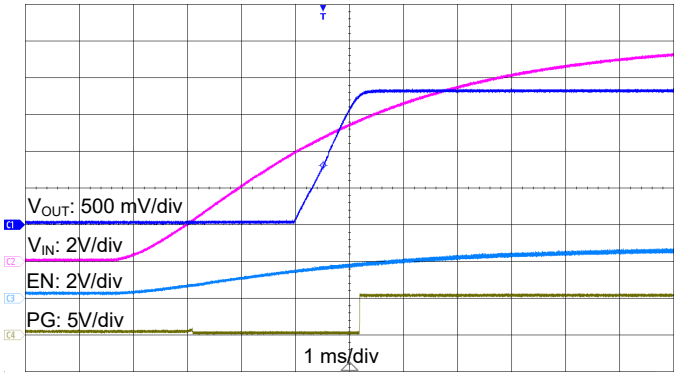


Figure 4-18. Startup With 6A Load

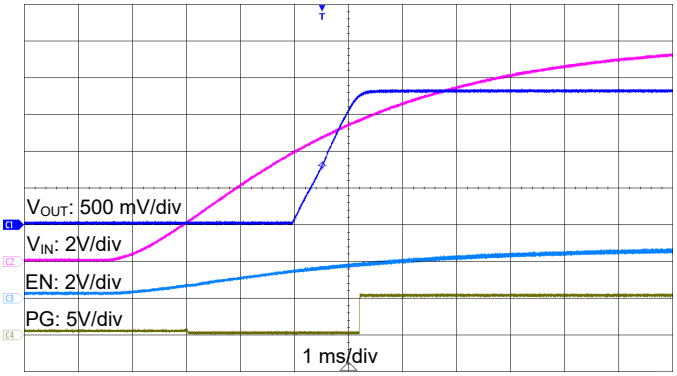


Figure 4-19. Shutdown via PVIN Pin, 6A Load

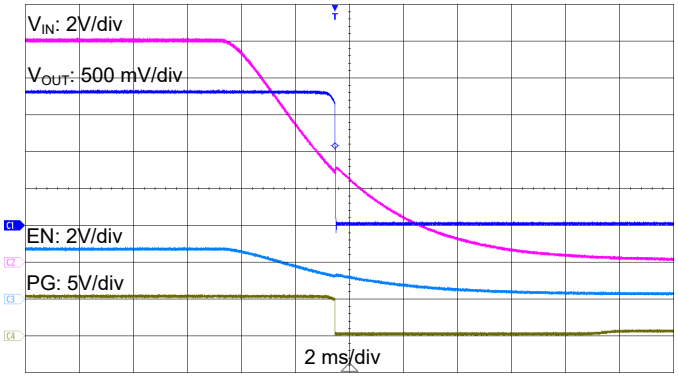


Figure 4-20. Startup via EN Pin, 6A Load

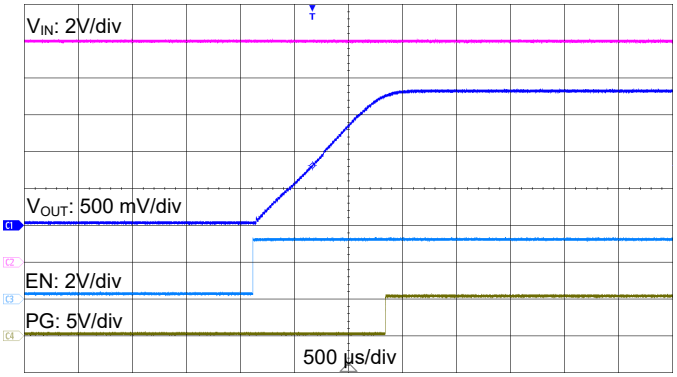


Figure 4-21. Shutdown via En Pin, 6A Load

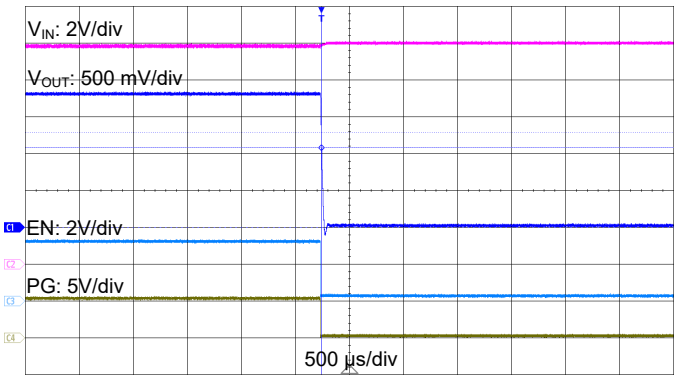
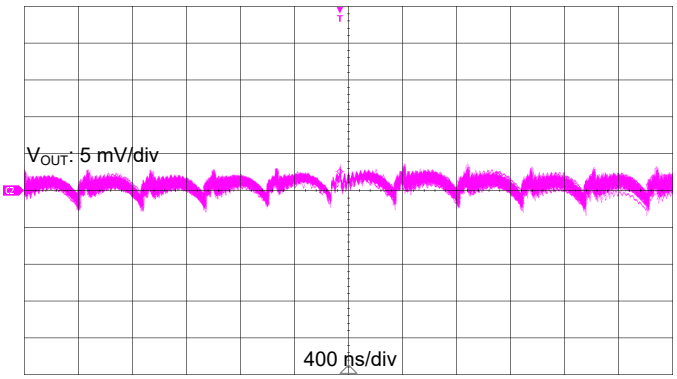


Figure 4-22. VOUT Ripple, no Load



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Figure 4-23. VOUT Ripple, 6A Load

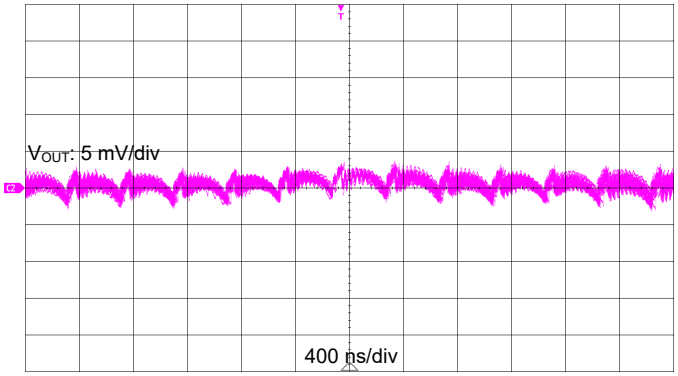
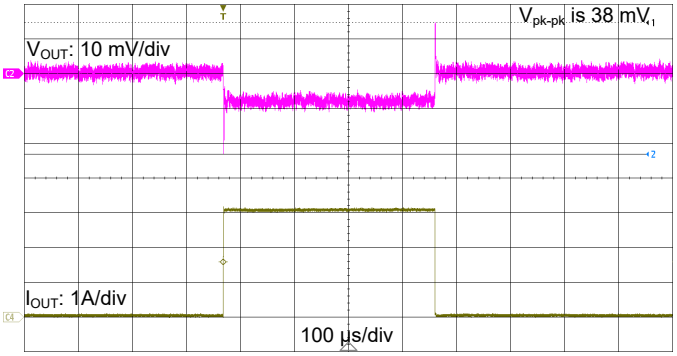


Figure 4-24. 0A to 3A Transient Response



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5. Design Example

Design requirements:

- PVIN = VIN = 12V
- VOUT = 1.8V
- I_{OUT} = 6A
- f_{SW} = 2 MHz
- C_{OUT} = 3 × 22 µF
- C_{IN} = 2 × 22 µF
- Ripple Voltage = ±1% of VOUT
- $\Delta V_{OUT(MAX)}$ = ±3% of VOUT (for a 50% load transient)

Input Capacitors

The input capacitor chosen for this design should:

- Accommodate the peak and RMS input currents demanded by the MCPF1606AM06.
- Possess low equivalent series resistance (ESR) and inductance (ESL) to minimize input voltage ripple.

Multi-layer ceramic capacitors (MLCCs) are ideal for this purpose. In a 0805 case size, they can typically manage 2A RMS current with a temperature rise of less than 5°C. This is particularly suitable for a buck converter operating at a lower duty cycle (D) and moderate output current. The RMS value of the input current for the converter is given by:

$$I_{RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

In this application, D = VOUT/PVIN = 0.15. Therefore, I_{RMS} = 2.14A, and we can select two 22 µF, 16V ceramic capacitors for the input capacitors. If the MCPF1606AM06 is not located close to the 12V power supply, a bulk capacitor (68–330 µF) may be advisable in addition to the ceramic capacitors. For VIN (input to the LDO), it is recommended to use a 1 µF capacitor very close to the pin. The VIN pin should be connected to PVIN through a 2.7Ω resistor. Together, the 2.7Ω resistor and 1 µF capacitor filter noise on PVIN.

Output Capacitors

The design necessitates minimal output capacitance to achieve the desired output voltage ripple and minimum output voltage deviation during load transients. For the MCPF1606AM06, the minimum number of output capacitors required to achieve the target peak-to-peak VOUT ripple is:

$$N_{MIN} = 4.09 \times \frac{\frac{(1 - D)}{8 \times C \times f_{SW}} + ESR \times (1 - D) + \frac{ESL \times f_{SW} \times (1 - D)^2}{D}}{\Delta VOUT_{ripple(pk - pk)}}$$

Where:

- N_{MIN} = minimum number of output capacitors
- D = duty cycle
- C = equivalent capacitance of each output capacitor
- f_{SW} = switching frequency
- ESR = equivalent series resistance of each output capacitor
- ESL = equivalent series inductance of each output capacitor

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- $\Delta VOUT_{ripple(pk-pk)}$ = target peak-to-peak VOUT ripple

This design uses a 22 µF, 6.3V MLCC with a 0805 case size. At 1.8V, considering DC bias and AC ripple derating, its equivalent capacitance (C) is 12 µF. The equivalent series resistance (ESR) is 3 mΩ, and the equivalent series inductance (ESL) is 0.44 nH. Using these parameters in the above equation results in N_{MIN} = 1.27.

To achieve the maximum voltage deviation $\Delta VOUT_{ripple(pk-pk)}$ during a ΔI_{OUT} load transient, the minimum number of output capacitors needed is:

$$N_{MIN} = \frac{0.244 \times \Delta I_{OUT}{}^2}{\Delta VOUT_{max} \times f_{SW} \times C}$$

Where:

- ΔI_{OUT} is the load step
- $\Delta VOUT_{max}$ is the maximum allowable output voltage deviation
- f_{SW} is the switching frequency
- C is the effective capacitance of each output capacitor

Using C = 12 µF, it is evident that the minimum number of output capacitors required is 0.4. For our space-constrained design, we use two C2012X5R0J226K125AB capacitors to satisfy both ripple and transient deviation constraints.

It is important to note that the calculation for the minimum number of output capacitors under a load transient is based on several assumptions:

1. No ESR or ESL.
2. The converter can instantly saturate its duty cycle.
3. No latency.
4. Step load (infinite slew rate).

Assumptions (1), (2), and (3) are optimistic, while (4) is conservative. Consequently, in a real-world application, additional capacitance may be necessary to meet transient requirements, and this should be carefully evaluated by the system designer.

The typical application waveforms in Figure 4-24, Figure 4-25 and Figure 4-26 illustrate the steady-state VOUT ripple and the voltage deviation in response to a 50% load transient. These waveforms demonstrate that using two 22 µF capacitors meets the design criteria.

Even without a specific target for VOUT ripple or maximum voltage deviation under load transient, at least one 22 µF capacitor is required to ensure stable operation without excessive jitter. Up to six 22 µF capacitors can be used in the design. If more capacitance is needed, it is recommended to use a capacitor with relatively high ESR (>3 mΩ).

Note: If the design incorporates a resistive voltage divider between VOUT and FB to set the output voltage, a feedforward capacitor in parallel with the top resistor will provide greater flexibility in selecting output capacitance.

Resistor Divider Selection

The recommended value for the top resistor (R_{TOP}) is 4.12 kΩ, while the bottom resistor (R_{BOTTOM}) should be selected based on the required output voltage, as indicated in Table 2-1 on page 7. For example, when using the MCPF1606AM06 to achieve a 1.8V output, the table specifies a ratio of 1.9619, which translates to an R_{BOTTOM} value of 2.1 kΩ. In this configuration, a Feedforward Capacitor (CFF) with a value of 680 pF is placed in parallel with R_{TOP}. This arrangement allows for greater flexibility in choosing the output capacitance, optimizing the circuit's performance for different application requirements.

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VCC Capacitor

The MCPF1606AM06 employs an on-package VCC capacitor for efficient high-frequency bypassing. Nonetheless, for applications utilizing an external VCC supply, it is advisable for system designers to position a 2.2 µF/0603/X7R/10V capacitor on the application board, as near to the VCC pin as possible.

Figure 5-1. Application Circuit for a Single Supply 12V Input to 1.8V Output, 6A Converter

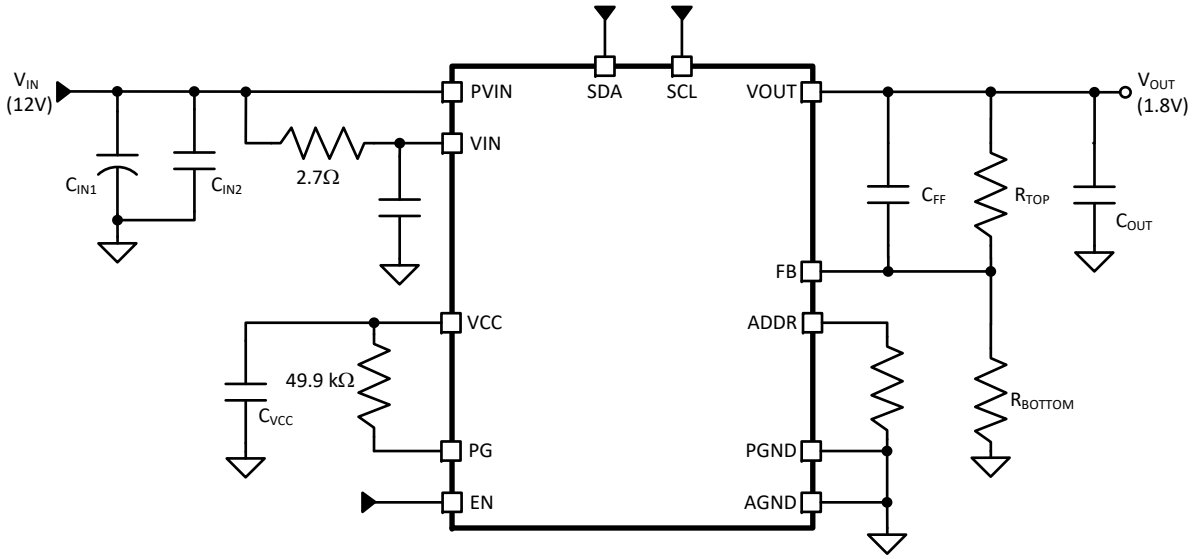


Table 5-1. Application Circuit Components

C_{IN1}	68 µF, 25V (optional)
C_{IN2}	2 × 2.2 µF, 16V, 0805, X5R
C_{VCC}	2.2 µF, 10V, 0603, X5R (optional)
C_{OUT}	2 × 2.2 µF, 6.3V, 0805, X5R
R_{TOP}	4.12 kΩ
R_{BOTTOM}	2.10 kΩ
C_{FF}	680 pF

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6. Layout Recommendations

General

The MCPF1606AM06 is a highly integrated device requiring minimal external components, which simplifies PCB layout. However, to ensure optimal performance, adhere to these general PCB design guidelines:

- Place bypass capacitors, including input/output capacitors and the VCC bypass capacitor (if used), as close as possible to the MCPF1606AM06 pins.
- Sense the output voltage with a separate trace directly from the output capacitor.
- For thermal dissipation, connect the PGND pad to the power ground plane using vias. Copper-filled vias are preferred, but plated-through-hole vias are acceptable if they are not filled with resin or covered with solder mask.
- Wide copper polygons should be used for input and output power connections.
- Use an adequate number of vias to connect between layers, especially for power traces.
- Use wide copper polygons for input and output power connections to minimize power losses and thermal dissipation.

Thermal

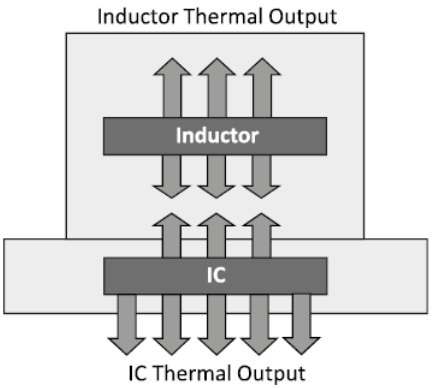
The MCPF1606AM06 has undergone thermal testing and modeling in compliance with JEDEC standards JESD 51-2A and JESD 51-8. Testing was conducted using a 4-layer application PCB, featuring thermal vias beneath the device to aid in cooling (refer to the application notes for PCB details).

The MCPF1606AM06 has two main heat sources:

- The power MOSFET section of the IC
- The inductor

The IC is effectively coupled to the PCB, which serves as its primary cooling pathway. While the inductor is also connected to the PCB, its main cooling mechanism is through convection. Ultimately, both heat sources dissipate heat through convection. The PCB functions as a heat spreader and, to some extent, a heat sink.

Figure 6-1. Heat Sources in the MCPF1606AM06



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Figure 6-2. Thermal Resistances in the MCPF1606AM06

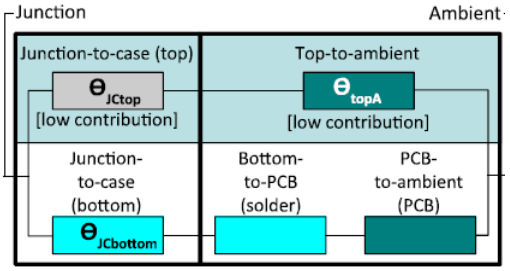


Figure 6-2 illustrates the thermal resistances in the MCPF1606AM06, described as follows:

- Θ_{JA} represents the natural convection from the assembled test sample within a confined enclosure of approximately 30 × 30 × 30 cm. The air in this environment is passive, with movement solely due to convection from the device under test.
- $\Theta_{JCbottom}$ indicates the heat flow from the IC to the bottom of the package, where it is well-coupled. The testing method follows JESD 51-8 guidelines, with the test PCB clamped between cold plates at specified distances from the device.
- Θ_{JCtop} theoretically represents the heat flow from the IC to the top of the package. However, this is not applicable for the MCPF1606AM06 for two reasons: it is not the primary conduction path of the IC, and the inductor, which generates a similar amount of heat as the IC, is positioned directly over it. Therefore, a meaningful junction-to-case (top) value cannot be determined.

The thermal resistance values are as follows:

- Θ_{JA} = 22.6°C/W
- $\Theta_{JCbottom}$ = 2.36°C/W

While these values provide a comparison of the MCPF1606AM06 with similar POL products under identical conditions and specifications, they are not sufficient for predicting overall thermal performance. Accurate modeling of the module's interaction with its environment requires Computational Fluid Dynamics (CFD) simulation software to simultaneously calculate the combined effects of conduction and convection.

Tip: All tests assumed passive or static airflow; applications using forced air may achieve better cooling.

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7. I²C Protocol

Legend:

S = Start bit	W = Write bit ('0')	White bits = Issued by Host
P = Stop bit	R = Read ('1')	Grey bits = Sent by Client (MCPF140x)
A = Ack	Sr = Repeated start	
N = Nack		

Figure 7-1. Write Transaction

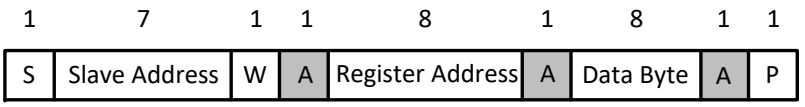
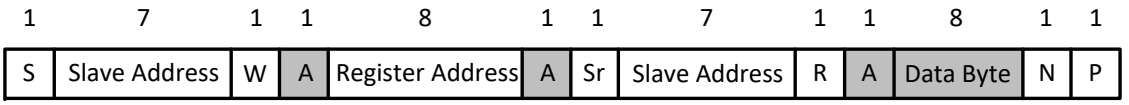


Figure 7-2. Read Transaction



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8. Package Information

Package Marking Information

Please note this package (17-Pin LLGA, 3.3 mm × 3.3 mm) has no marking.

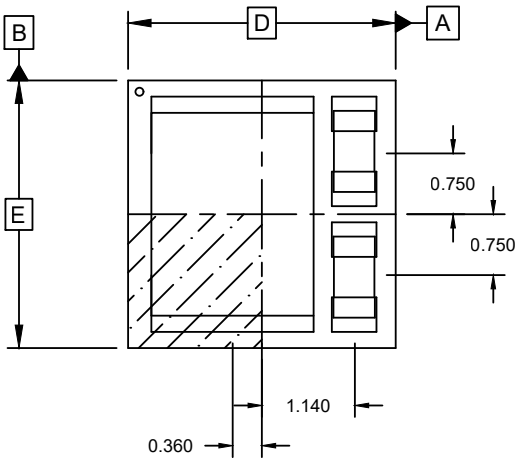
Note: The MCPF1606AM06 is engineered for compatibility with standard surface-mount technology (SMT) assembly methods. It features a raised footprint, with pads elevated above the surrounding substrate. These characteristics make the MCPF1606AM06 highly effective in lead-free environments, as the surface wets easily and the raised footprint allows for processing variations.

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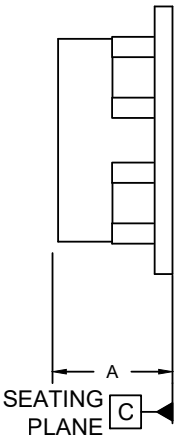
Package Outline Drawing

17-Lead Low-Profile Land Grid Array (8EW) 3.3x3.3x1.62mm [LLGA] - System In Package [SIP]

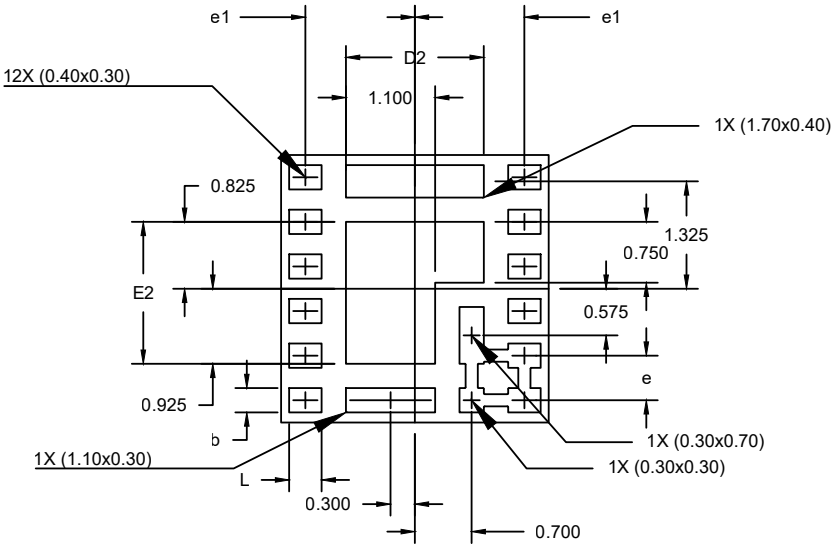
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



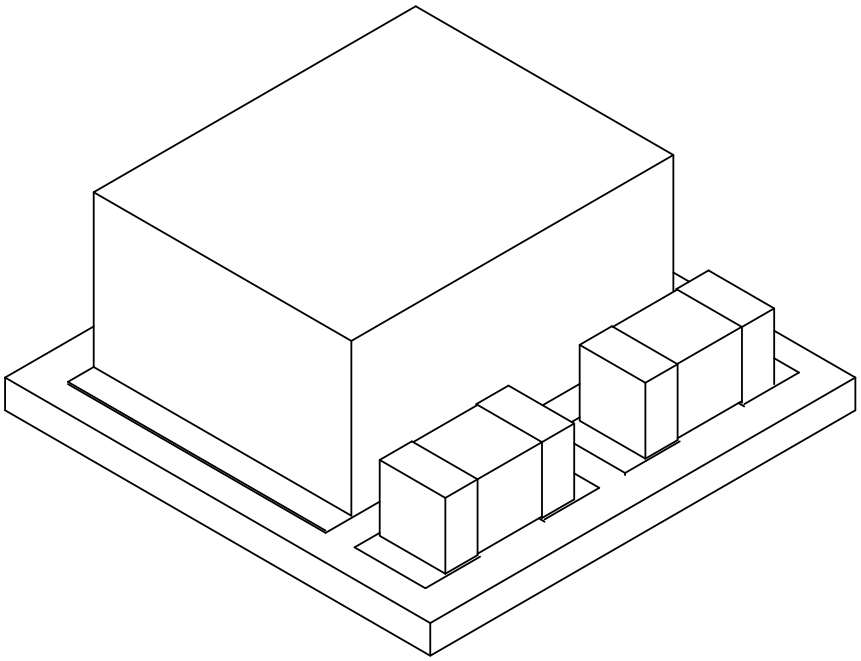
BOTTOM VIEW

Microchip Technology Drawing C04-00659 Rev B Sheet 1 of 2

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17-Lead Low-Profile Land Grid Array (8EW) 3.3x3.3x1.62mm [LLGA] - System In Package [SIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		17	
Pitch	e		0.55 BSC	
Pitch	e1		1.35 BSC	
Overall Height	A	1.20	1.35	1.62
Overall Length	D		3.30 BSC	
Exposed Pad Length	D2	1.60	1.70	1.80
Overall Width	E		3.30 BSC	
Exposed Pad Width	E2	1.65	1.75	1.85
Terminal Width	b	0.20	0.30	0.40
Terminal Length	L	0.30	0.40	0.50

Notes:

1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. The package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M

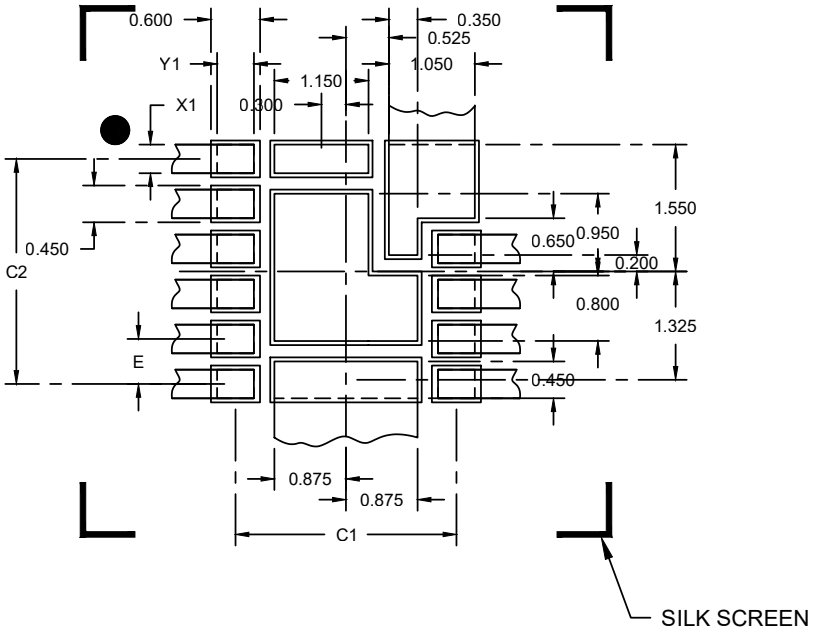
   BSC: Basic Dimension. The theoretically exact value is shown without tolerances.
   REF: Reference Dimension, usually without tolerance, is for information purposes only.

Microchip Technology Drawing C04-00659 Rev B Sheet 2 of 2

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17-Lead Low-Profile Land Grid Array (8EW) 3.3x3.3x1.62mm [LLGA] - System In Package [SIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.55 BSC	
Contact Pad Spacing	C1		2.70	
Contact Pad Spacing	C2		2.75	
Contact Pad Width (X10)	X1			0.35
Contact Pad Length (X10)	Y1			0.45

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. The theoretically exact value is shown without tolerances.
2. For best soldering results, please refer to current industry standard IPC-7093.

Microchip Technology Drawing C04-02659 Rev B

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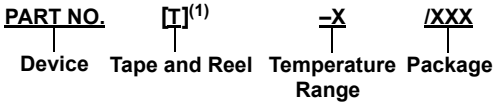
9. Revision History

Doc. Rev.	Date	Section	Comments
A	June 2026		Initial release of this document.

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Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Device:	MCPF1606AM06: 16V, 6A Switching Buck Regulator Module	
Tape & Reel Option(1):	Blank	= Tube
	T	= Tape and Reel
Temperature Range:	E	= −40°C to +125°C (Extended)
Package:	8EW	= Low-Profile Land Grid Array (LLGA), 17-Pin, 3.3 × 3.3 × 1.5 mm

Examples:

- MCPF1606AM06T-E/8EW: 16V, 6A Switching Buck Regulator Module, Tape and Reel, Extended temperature, LLGA 17-Pin package

Notes:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.

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