2.6V to 5.5V, 20A Hot-Swap E-Fuse with Current Report Output

ADP15193

General Description

The ADP15193 is an integrated device for hot-swap applications requiring the safe insertion and removal of boards from a live backplane. The device integrates a hot-swap controller, 1mΩ power MOSFET, and electronic circuit breaker.

An accurate current-sense circuitry outputs 42µA for every 1A of MOSFET current. A capacitor on the GATE pin sets the soft-start slew rate, limiting inrush current and keeping the MOSFET operating within its safe operating area (SOA).

Additional features include adjustable input undervoltage lockout, internal overtemperature protection, and power-good output.

The ADP15193 is available in a 10-pin, 2mm × 3mm, FC2QFN package and is specified over the -40°C to +125°C temperature range.

Applications

- Optical Modules
- Network Switch
- Disk Drive Power

Features

- Integration Reduces Solution Size
  - Integrated 1mΩ Internal Power MOSFET
  - Adjustable Undervoltage Lockout
  - Current Reporting without External R_{SENSE}
  - Quick Output Discharge
  - Power-Good Output
- Flexibility Enables Use in Many Unique Designs
  - 2.6V to 5.5V Operating Voltage Range
  - Adjustable Slew Rate Control
  - Adjustable Circuit Breaker Current Threshold
  - Latchoff or Automatic Retry after Fault
- Safety Features Ensure Accurate, Robust Protection
  - ±5% Circuit Breaker Threshold Accuracy
  - dI/dt Control at Startup
  - Output Precharge Detection
  - Thermal Shutdown

Ordering Information ***appears at end of data sheet.***

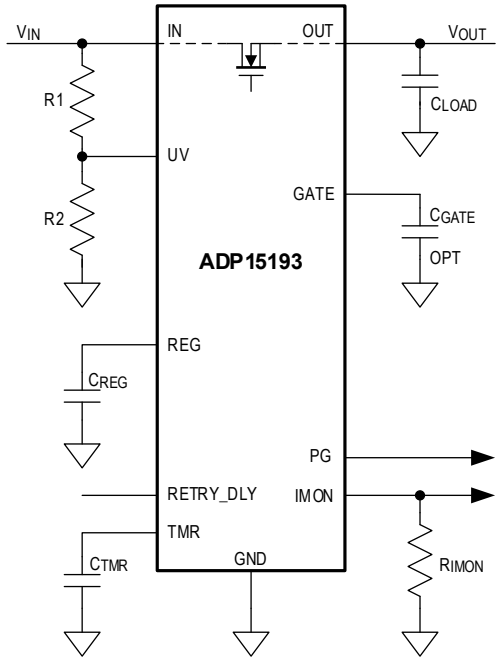
19-102150; Rev. 2; 7/26

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2.6V to 5.5V, 20A Hot-Swap E-Fuse with Current Report Output

ADP15193

Simplified Application Diagram



19-102150; Rev. 2; 7/26

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Absolute Maximum Ratings

IN to GND ..... -0.3V to +6.6V
OUT to GND ..... -0.3V to V_{IN} + 0.3V
GATE to OUT ..... -0.3V to +2V
REG to GND ..... -0.3V to +2V
UV, PG to GND ..... -0.3V to +6.6V
IMON, TMR to GND ..... -0.3V to V_{REG} + 0.3V
RETRY_DLY to GND ..... -0.3V to +2.3V
Junction Temperature (T_J) ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

10 FC2QFN

Package Code	F1023F+1
Outline Number	*21-100787*
Land Pattern Number	*90-100275*
Thermal Resistance, Four-Layer 2s2p JEDEC Board:	
Junction to Ambient (θ_{JA})	68.9°C/W
Junction to Case, Bottom (θ_{JCbot})	0.6°C/W
Junction to Case, Top (θ_{JCtop})	43°C/W

For the latest package outline information and land patterns (footprints), go to analog.com/en/resources/packaging-quality-symbols-footprints/package-index.html. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to analog.com/en/resources/technical-articles/thermal-characterization-of-ic-packages.html.

Electrical Characteristics

(V_{IN} = 2.8V to 3.6V for ADP15193A/B/D, V_{IN} = 2.6V to 5.5V for ADP15193C, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are for T_A = +25°C (Note 1) and V_{IN} = 3.3V for ADP15193A/B/D or V_{IN} = 5V for ADP15193C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
IN Operating Range	V_{IN}	ADP15193A, ADP15193B, ADP15193D		2.8		3.6	V
		ADP15193C		2.6		5.5	
IN Supply Current	I_{IN}	V_{UV} < V_{UV_TH}			2	5	mA
		V_{UV} > V_{UV_TH}, no load			1.7	4	
IN Undervoltage Lockout	V_{UVLO}	V_{IN} rising	ADP15193A	2.72	2.75	2.78	V
			ADP15193B, ADP15193D	2.61	2.64	2.67	
			ADP15193C	2.51	2.54	2.57	
IN Undervoltage Lockout Hysteresis	V_{UVLO_HYS}	ADP15193A			0		mV
		ADP15193B, ADP15193C, ADP15193D			50		
IN Overvoltage Lockout	V_{OVLO}	V_{IN} rising	ADP15193A, ADP15193B, ADP15193D	3.713	3.75	3.788	V
			ADP15193C	5.643	5.7	5.757	

(V_{IN} = 2.8V to 3.6V for ADP15193A/B/D, V_{IN} = 2.6V to 5.5V for ADP15193C, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are for T_A = +25°C (Note 1) and V_{IN} = 3.3V for ADP15193A/B/D or V_{IN} = 5V for ADP15193C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IN Overvoltage Lockout Hysteresis	V_{OVLO_HYS}				150		mV
REG Regulator Voltage	V_{REG}			1.62	1.8	1.98	V
UV Turn-on Threshold	V_{UV_TH}	V_{UV} rising		0.99	1.00	1.01	V
UV Turn-on Threshold Hysteresis	V_{UV_HYS}	V_{UV} falling			10		mV
UV Input Leakage Current	I_{LEAK}	V_{UV} = 0 to V_{IN}		-1		+1	µA
CURRENT REPORT							
IMON Gain Ratio	G_{IMON}	I_{IMON}/I_{LOAD}, I_{LOAD} ≥ 3A			42		µA/A
IMON Gain Error	G_{IMON_ERR}	I_{LOAD} ≥ 3A	T_A = +25°C	-3.5		+3.5	%
			T_A = -40°C to +125°C	-5		+5	
IMON Full-Scale Current	I_{IMON}	I_{LOAD} = 20A			840		µA
IMON Voltage Range	V_{IMON}			0		1.25	V
IMON Offset Error	I_{IMON_OFST}	I_{LOAD} = 3A	T_A = +25°C	-4		+4	µA
			T_A = -40°C to +125°C	-22		+12	
CURRENT LIMIT							
Slow Circuit Breaker Threshold	V_{CB_TH}	ADP15193B, ADP15193C, ADP15193D		0.76	0.8	0.84	V
Fast Circuit Breaker Threshold	V_{FAST_TH}	ADP15193B, ADP15193C, ADP15193D		1.14	1.2	1.26	V
Safe Circuit Breaker Threshold	I_{SAFE_TH}			20.4	21.5	23.4	A
Slow Comparator Response Time	t_{OCD_SLOW}	V_{CB_TH} < V_{IMON} < V_{FAST_TH}	ADP15193B, ADP15193C, ADP15193D		1		ms
Fast Comparator Response Time	t_{OCD_FAST}	V_{IMON} > V_{FAST_TH}	ADP15193B, ADP15193C, ADP15193D		1		µs
Safe Comparator Response Time	t_{OCD_SAFE}	I_{LOAD} > I_{SAFE_TH}			3		µs
Inrush Current Limit During Startup	I_{LIM_INRUSH}	ADP15193A, ADP15193B, ADP15193C			0.5	0.65	A
		ADP15193D			0.8	0.95	
Current Slew Rate During Startup	dI/dt_{INRUSH}	ADP15193A, ADP15193B, ADP15193C			83	105	A/s
		ADP15193D			66	100	
TMR, RETRY_DLY TIMING							
TMR Comparator High Threshold	$V_{TMR_TH_HI}$	V_{TMR} rising		0.95	1.0	1.05	V
TMR Comparator Low Threshold	$V_{TMR_TH_LO}$	To release the TMR discharge		0.15	0.2	0.25	V
TMR Source Current	I_{TMR}			5.3	6.25	7.2	µA
TMR Discharge Resistance	R_{TMR}			25	50	125	Ω
Delay Before Activating TMR	t_{DLY_TMR}	From V_{UVLO} < V_{IN} < V_{OVLO} and V_{UV} > V_{UV_TH} and V_{OUT} < V_{PC} to TMR rising			256		µs

(V_{IN} = 2.8V to 3.6V for ADP15193A/B/D, V_{IN} = 2.6V to 5.5V for ADP15193C, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are for T_A = +25°C (Note 1) and V_{IN} = 3.3V for ADP15193A/B/D or V_{IN} = 5V for ADP15193C.)

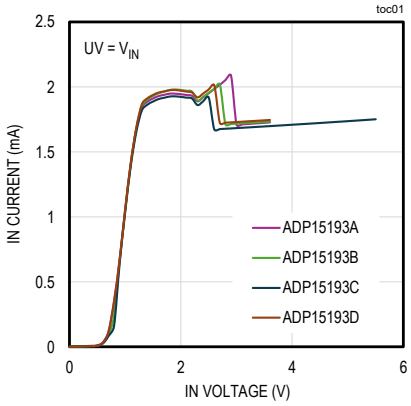
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Startup Maximum Time Duration	t_{SU}		180	200	220	ms
RETRY_DLY Comparator Threshold	V_{DLY_TH}		0.95	1.0	1.05	V
RETRY_DLY Source Current	I_{DLY}		1.6	2.0	2.4	µA
RETRY_DLY Discharge Resistance	R_{DLY}		25	50	125	Ω
Delay Time between Retries	$t_{RESTART_MIN}$	RETRY_DLY pin open	90	100	120	ms
Adjustable Delay Time between Retries	$t_{RESTART}$	With a capacitor from RETRY_DLY pin to GND pin	120		3603	ms
MOSFET						
Total On-Resistance	R_{ON}	T_A = +25°C		1.0		mΩ
		T_A = –40°C to +125°C			1.5	
Gate Charge Current	I_{GATE}		6	8	10	µA
QUICK OUTPUT DISCHARGE						
Discharge Current when MOSFET Is Disabled	$I_{DISCHARGE}$		75	150	300	mA
PG OUTPUT						
PG Assertion Threshold	V_{PG}	Measured at V_{OUT}	0.86 × V_{IN}	0.9 × V_{IN}	0.94 × V_{IN}	V
PG Deassertion Threshold		Measured at V_{OUT}	0.76 × V_{IN}	0.8 × V_{IN}	0.84 × V_{IN}	V
PG Assertion Delay	t_{PG}	From V_{OUT} > V_{PG} and (V_{GATE} - V_{OUT}) > 1V	1.8	2.4	3	ms
PG Output Low Voltage	V_{OL}	Low-impedance state, I_{PG} = 5mA			0.45	V
PG Pull-up Resistance	R_{PULL_UP}	From PG to OUT	140	200	260	kΩ
OUT DETECTION						
OUT Precharge Threshold	V_{PC}	Measured at V_{OUT}	270	300	330	mV
THERMAL SHUTDOWN						
Thermal Shutdown	T_{SD}	T_J rising		+150		°C
Thermal Shutdown Hysteresis		T_J falling		+20		°C

Note 1: All devices are 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design and characterization.

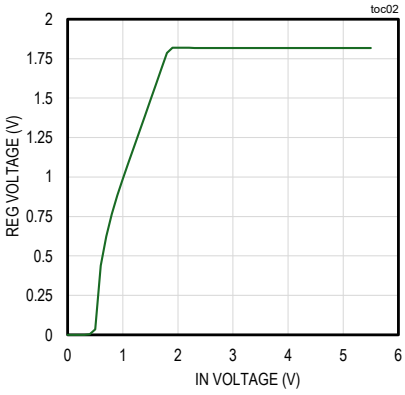
Typical Operating Characteristics

(V_{IN} = 3.3V, T_A = +25°C, unless otherwise noted.)

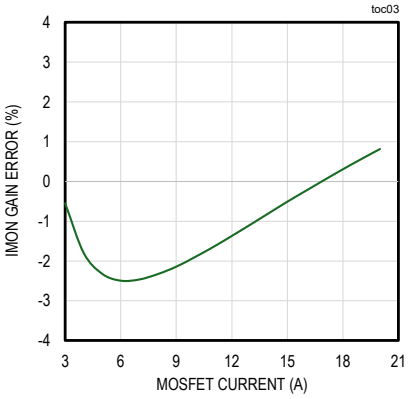
IN CURRENT vs. IN VOLTAGE



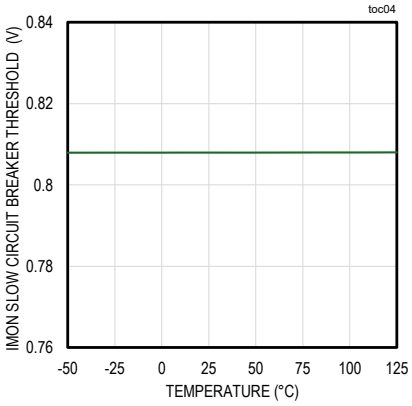
REG VOLTAGE vs. IN VOLTAGE



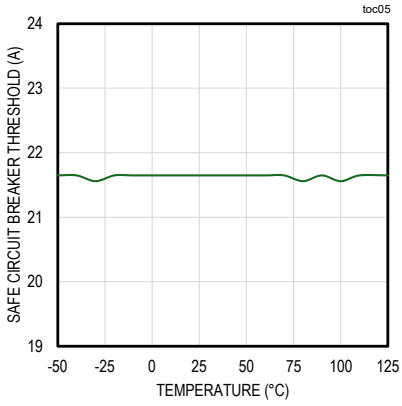
IMON GAIN ERROR vs. MOSFET CURRENT



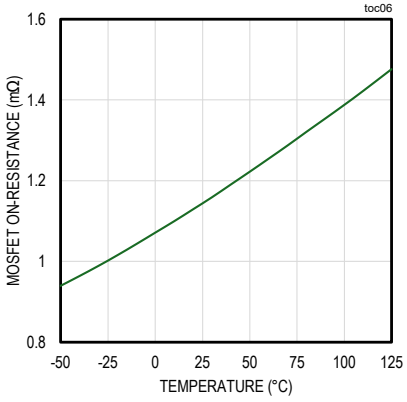
IMON SLOW CIRCUIT BREAKER THRESHOLD vs. TEMPERATURE



SAFE CIRCUIT BREAKER THRESHOLD vs. TEMPERATURE

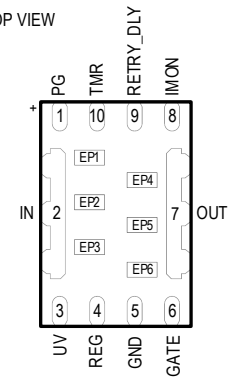


MOSFET ON-RESISTANCE vs. TEMPERATURE



Pin Configurations

10 FC2QFN

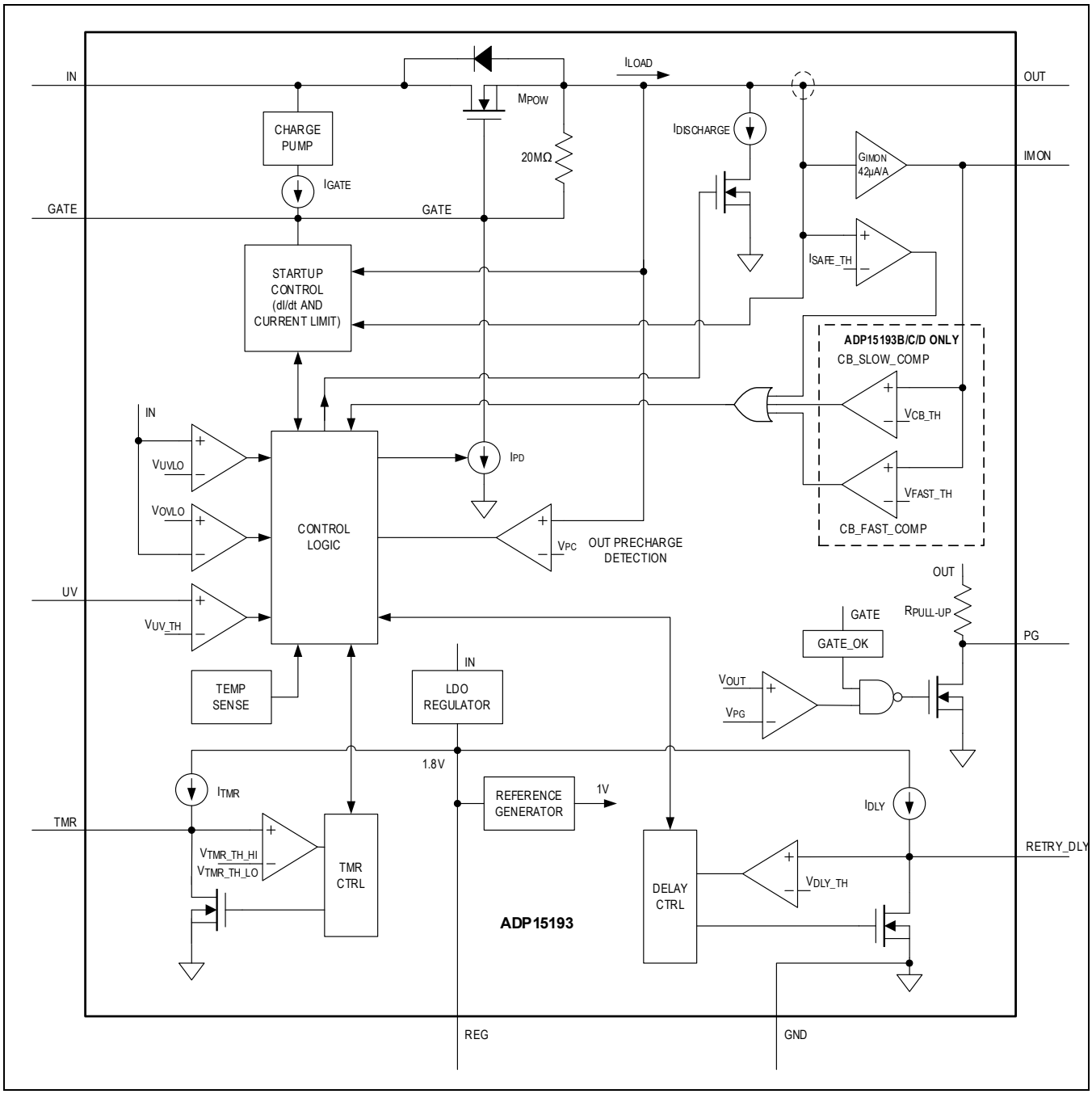


FC2QFN
(2mm × 3mm)

Pin Descriptions

PIN	NAME	FUNCTION
1	PG	Power-Good Output. PG goes high 2.4ms (t_{PG}) after OUT reaches 90% of V_{IN} voltage and $V_{GATE} - V_{OUT} > 1V$, indicating that soft-start is complete. PG pulls low when OUT drops below 80% of V_{IN} or $V_{GATE} - V_{OUT} < 1V$. PG is internally pulled up to OUT through a 200kΩ resistor.
2, EP1, EP2, EP3	IN	Supply Voltage Input. IN is connected to the drain of the internal MOSFET. For applications with significant supply inductance and no IN bypass capacitance, a TVS may be needed to clamp IN voltage spikes below its absolute maximum rating.
3	UV	Enable Comparator Input. Pulling UV high enables the internal MOSFET to turn on. UV also sets the undervoltage threshold.
4	REG	Internal 1.8V Regulator Output. Bypass to ground with at least a 0.47µF capacitor. Do not load REG externally.
5	GND	Ground
6	GATE	GATE of Internal MOSFET. Connect an external capacitor from GATE to GND to control OUT soft-start slew rate.
7, EP4, EP5, EP6	OUT	Output. Source of the internal power MOSFET.
8	IMON	Current Monitor Output. The IMON output sources a current that is proportional to the MOSFET current. Connect a resistor between IMON and GND to produce a scaled voltage. The voltage on this resistor is compared with an internal threshold for overcurrent protection (ADP15193B/C/D only).
9	RETRY_DLY	Retry Delay Input. Connect a capacitor from RETRY_DLY to GND to set the time period that must elapse after a fault turn-off before the device attempts to restart automatically.
10	TMR	Timer Input. Connect an external capacitor from TMR to GND to set the delay before soft-start, low UV turn-off, and IN OVLO turn-off.

Functional Diagrams



Detailed Description

The ADP15193 turns a board's supply voltage on and off in a controlled manner, allowing the board to be safely inserted or removed from a live backplane.

During normal operation, the device turns on the internal 1mΩ power MOSFET after a start-up debounce delay, passing power to the load. For every 1A of MOSFET current, an accurate current-sense circuit sources 42µA into the resistor (R_{IMON}) at the IMON pin, generating a voltage V_{IMON} for an external ADC monitoring the load current. For the ADP15193B/C/D, V_{IMON} is compared with an internal circuit breaker threshold for overcurrent protection.

The device includes three comparators to monitor the input voltage at all times to ensure that it is in a valid range. Two comparators internally monitor the IN voltage for the IN UVLO and OVLO. One comparator monitors the IN voltage through an external resistive divider connected to the UV pin.

A capacitor at the TMR pin sets the start-up debounce delay and the turn-off delay for undervoltage and overvoltage faults.

The device provides a GATE pin to set the output slew rate during startup by adding an external capacitor, limiting inrush current and keeping the MOSFET within its SOA.

Applications Information

Enable Logic and IN Undervoltage/Overvoltage Lockout

The ADP15193 is ready to drive the output when IN rises above the V_{UVLO} threshold.

At startup, when IN is in the operating range ($V_{UVLO} < V_{IN} < V_{OVLO}$), OUT is below its precharge threshold ($V_{OUT} < V_{PC}$), and UV is above its threshold ($V_{UV} > V_{UV_TH}$), the TMR capacitor (C_{TMR}) starts charging with 6.25µA (I_{TMR}) after a 256µs delay. The debounce delay lasts until TMR rises to 1V ($V_{TMR_TH_HI}$). TMR is pulled down before the device enters the soft-start phase to turn on the output. If IN drops below $V_{UVLO} - V_{UVLO_HYS}$ during the debounce delay, the device pulls down TMR immediately and stays off. $V_{IN} > V_{OVLO}$ or $V_{UV} < V_{UV_TH} - V_{UV_HYS}$ is ignored during debounce. But if those conditions exist at the end of the debounce delay, the device pulls down TMR and stays off (see *Figure 1*).

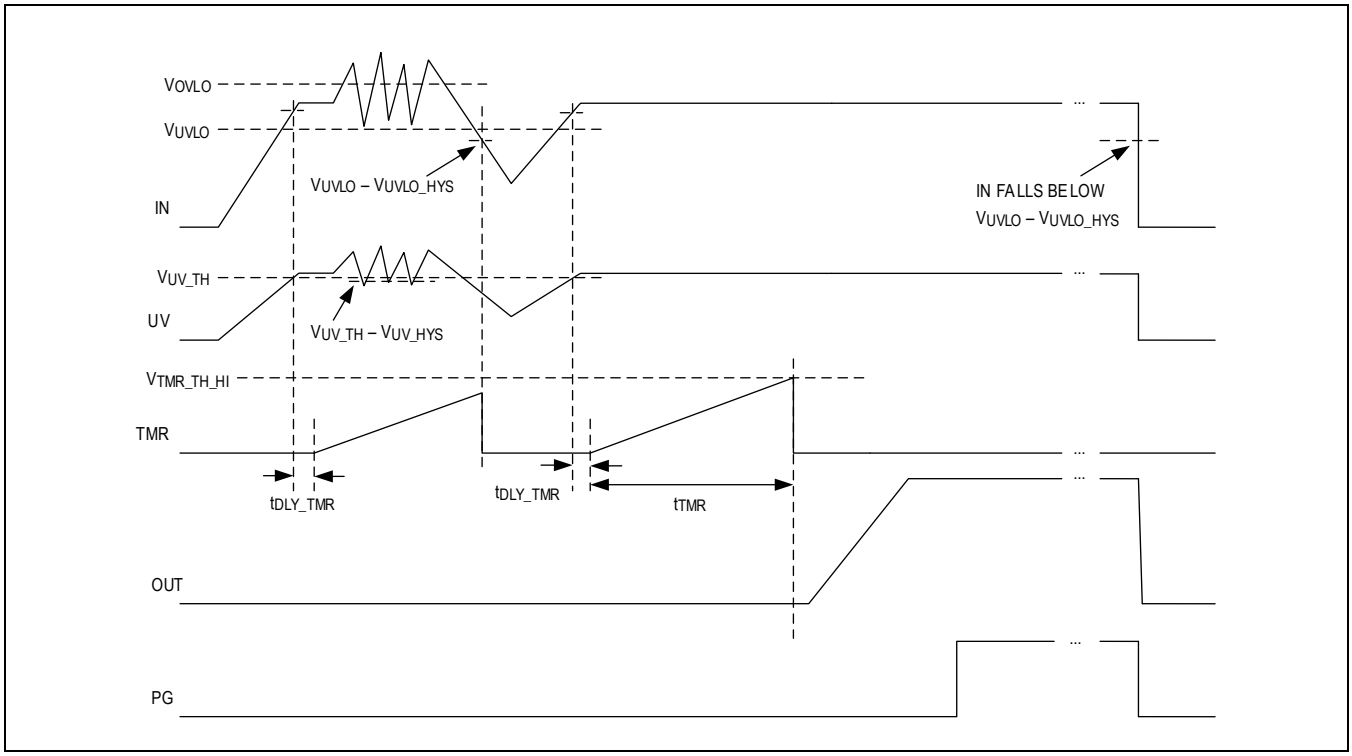


Figure 1. Debounce Delay at Startup, and IN Turn-Off

The debounce delay is given by:

$$t_{TMR} = \frac{C_{TMR} \times V_{TMR_TH_HI}}{I_{TMR}}$$

At any time when IN falls below V_{UVLO} - V_{UVLO_HYS}, the device turns off the output immediately (see *Figure 1*).

When V_{UV} falls below V_{UV_TH} – V_{UV_HYS} or IN rises above V_{OVLO}, the device starts to charge C_{TMR}. If IN is back within normal range (V_{IN} < V_{OVLO} – V_{OVLO_HYS} and V_{UV} > V_{UV_TH}) before TMR reaches $V_{TMR_TH_HI}$, the device pulls down TMR and continues operation. Any IN voltage fault reoccuring before TMR discharges below $V_{TMR_TH_LO}$ is ignored. If the IN fault is not removed (V_{IN} > V_{OVLO} or V_{UV} < V_{UV_TH} – V_{UV_HYS}) when TMR reaches $V_{TMR_TH_HI}$, the device pulls down TMR and turns off (see *Figure 2*).

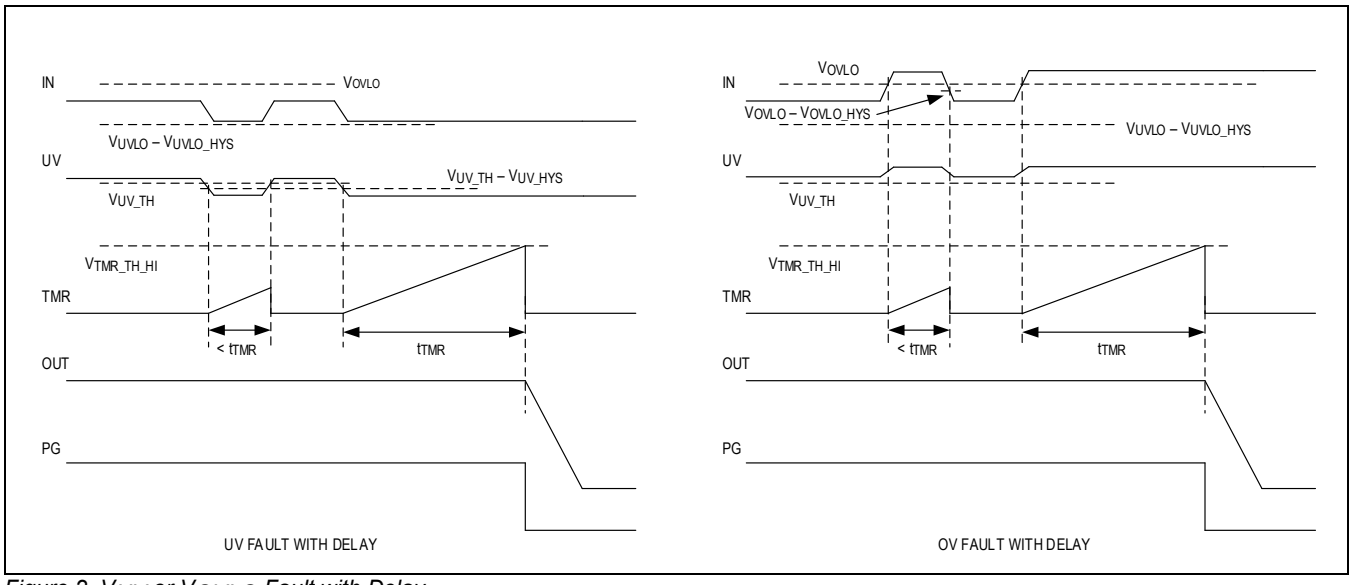


Figure 2. V_{UV} or V_{OVLO} Fault with Delay

An external resistive divider from IN to UV and ground provides the flexibility to set the undervoltage threshold (see *Figure 3*).

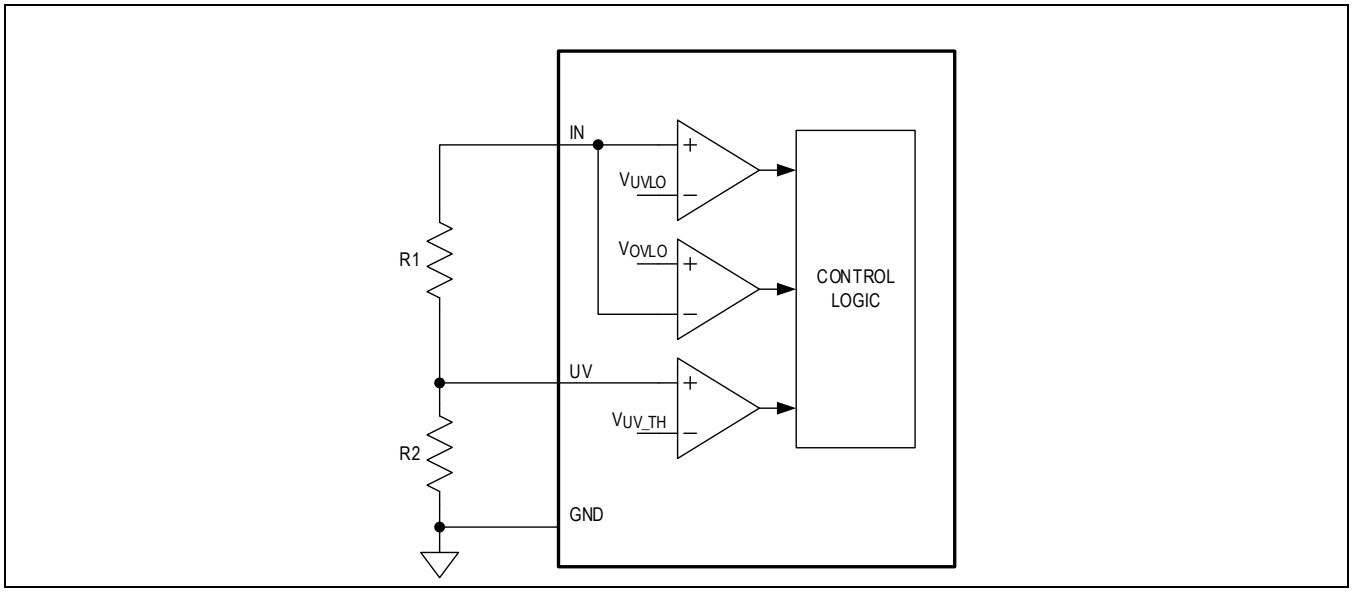


Figure 3. Undervoltage-Lockout Threshold Setting

Use the following equation to calculate the resistor values for the desired undervoltage threshold:

$$R1 = \left(\frac{V_{IN(TO)}}{V_{UV_TH}} - 1\right) \times R2$$

where $V_{IN(TO)}$ is the desired turn-on voltage for the output and V_{UV_TH} is 1.0V.

Output Precharge Detection

At startup, after all the input conditions are satisfied (V_{UVLO}, V_{OVLO}, UV), the device immediately checks for OUT voltage. If V_{OUT} is above 300mV, the internal power MOSFET cannot be turned on until V_{OUT} is discharged lower than 300mV.

Startup (GATE)

Once the device output is enabled, power is provided to the load in a controlled manner.

During startup, the device compares the output current with an internal dI/dt reference to maintain its dI/dt below 105A/s until the output current reaches the inrush current limit, I_{LIM_INRUSH}. Connecting an external capacitor (C_{GATE}) from GATE to GND allows adjustment of the output slew rate. To set the inrush current lower than the current limit, C_{GATE} can be calculated according to the following formula:

$$C_{GATE} = \frac{I_{GATE} \times C_{LOAD}}{I_{INRUSH}} - 6nF$$

where I_{GATE} is gate drive current, 8µA, C_{LOAD} is the external capacitive load, and I_{INRUSH} is the desired inrush current during startup (*Figure 4*).

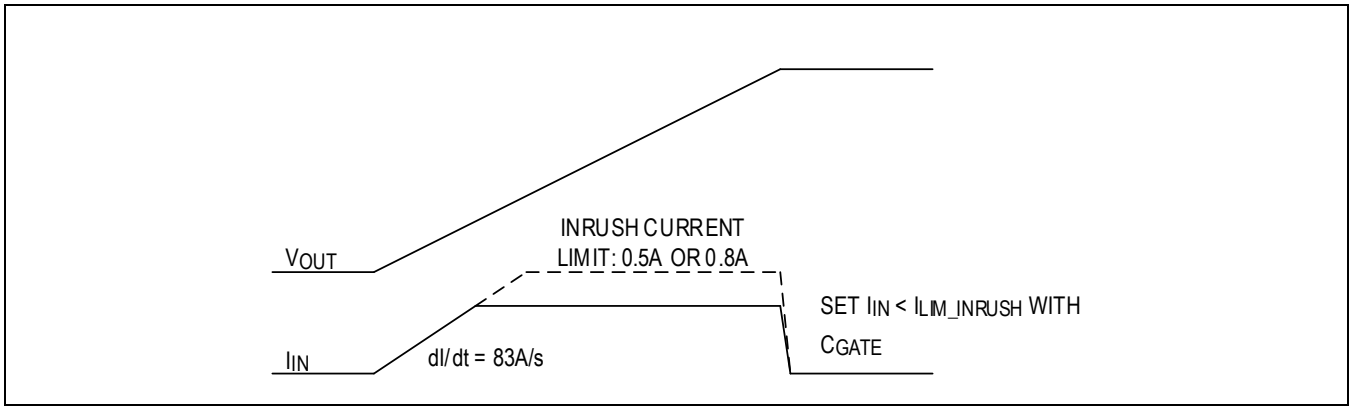


Figure 4. Inrush Current during Startup

An internal 200ms timer (t_{SU}) starts when the device enters the soft-start phase. When the soft-start is completed and the voltage at OUT rises above the threshold (0.9 × V_{IN}), there is a 16ms delay before GATE pulls up to its internal charge pump voltage allowing (V_{GATE} – V_{OUT}) > 1V. The device enters fault mode if soft-start does not complete before t_{SU} expires.

The thermal protection circuit is always active and the internal MOSFET turns off immediately when the thermal shutdown threshold is exceeded.

Current Report Output (IMON)

The IMON pin is the output of an accurate current-sense amplifier and sources a current that is proportional to the load current flowing through the power MOSFET. The current ratio is 42µA/A. Connecting a resistor (R_{IMON}) between IMON and ground produces a voltage given by:

$$V_{IMON} = G_{IMON} \times I_{LOAD} \times R_{IMON}$$

where G_{IMON} is the 42µA/A current-sense amplifier gain and I_{LOAD} is the load current.

This voltage signal can be digitized by an external ADC to provide current information to the system.

Circuit Breaker Threshold

After the soft-start phase is successfully complete, the ADP15193B/C/D provide three levels of overcurrent protection while the ADP15193A provides only the third level of overcurrent protection.

The first level of OCP is implemented by a slow circuit breaker comparator, which compares the IMON voltage (V_{IMON}) to its circuit breaker threshold (0.8V V_{CB_TH}). This comparator allows the load current to exceed the threshold for 1ms before tripping, allowing the device to tolerate load transients and noise near the circuit breaker threshold.

The second level of OCP is implemented by a fast circuit breaker comparator. When V_{IMON} exceeds the fast circuit breaker threshold (1.2V V_{FAST_TH}), the device discharges the MOSFET gate quickly, disconnecting the output from input.

The third level of OCP is implemented by a safe circuit breaker comparator, which monitors the load current directly. When load current exceeds its threshold (21.5A I_{SAFE_TH}), the device discharges the MOSFET gate quickly, disconnecting the output from input.

For the ADP15193B/C/D, adjust the resistor at IMON pin to configure the desired overcurrent threshold:

$$R_{IMON} = \frac{V_{CB_TH}}{G_{IMON} \times I_{CB}}$$

where V_{CB_TH} is the slow circuit breaker threshold (0.8V) and I_{CB} is the desired load current overcurrent threshold that should be below I_{SAFE_TH}.

Configuring Autoretry or Latch-Off after Fault (RETRY_DLY)

The following events trigger an internal fault that can cause ADP15193 to turn off: an overcurrent fault or if the device does not complete the startup before t_{SU} timer expires.

During a fault condition, the device turns off the internal power MOSFET, disconnecting the output from the input. The device either autoretries or latches off as set by the RETRY_DLY pin.

Connect a capacitor (C_{RETRY_DLY}) from RETRY_DLY pin to GND to set the autoretry delay. After a fault turn-off, the device charges C_{RETRY_DLY} with 2µA (I_{DLY}) until its voltage reaches the RETRY_DLY comparator threshold (1V V_{DLY_TH}). After that, the device pulls down RETRY_DLY and restarts automatically. The delay between retries is internally clamped in the range of 120ms to 3.6s, and calculated by:

$$t_{RESTART} = C_{RETRY_DLY} \times \frac{V_{DLY_TH}}{I_{DLY}}$$

When RETRY_DLY pin is floating or C_{RETRY_DLY} is below 180nF, the device enters into autoretry mode with the minimum delay (100ms) between retries. But if a large capacitor is used that exceeds the maximum delay (3.6s), the device latches off. Connecting RETRY_DLY to GND also causes the device to latch off. For latchoff, the device remains off after a fault turn-off until the UV or IN input is cycled off and on after a 3.6s delay. The delay prevents the latched-off device from operating with an unsafe power-dissipation duty cycle.

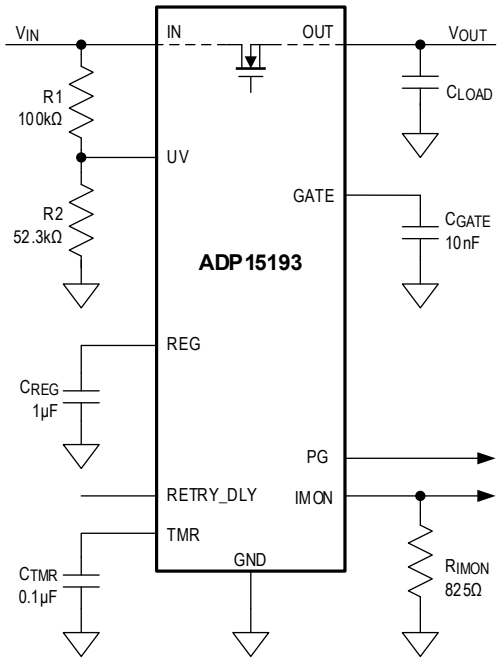
Quick Output Discharge (QOD)

The ADP15193 includes a quick output discharge (QOD) feature. When the output is disabled or a fault event has turned off the power MOSFET, an internal 150mA pull-down current ($I_{DISCHARGE}$) is activated to discharge the load capacitance.

Thermal Protection

The device monitors the internal die temperature (T_J) at all times and enters into thermal shutdown mode in the event of overheating caused by excessive power dissipation or high ambient temperature. When the junction temperature exceeds +150°C, the internal thermal protection circuitry turns off the internal power MOSFET. The device will not recover from thermal shutdown mode until the junction temperature drops below +130°C.

Typical Application Circuits



Ordering Information

PART NUMBER	OPERATING RANGE	IN UVLO	IN OVLO	INRUSH LIMIT	OCP LEVEL	TEMPERATURE RANGE	PACKAGE
ADP15193AAFB+T	2.8V to 3.6V	2.75V	3.75V	500mA	21.5A	-40°C to +125°C	10-pin, 2mm × 3mm FC2QFN
ADP15193BAFB+T		2.64V			Adjustable		
ADP15193CAFB+T	2.6V to 5.5V	2.54V	5.7V				
ADP15193DAFB+T	2.8V to 3.6V	2.64V	3.75V	800mA			

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/26	Initial release	—
1	6/26	Updated part number throughout and Ordering Information	All
2	7/26	Removed future product asterisk from ADP15193CAFB+T	13

NOTES

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