

SPOC™ Wire Guard

Features

- High-side power switch with diagnosis and embedded protection
- Daisy chain capable 24 bit SPI with CRC
- Embedded I²t wire and system protection
- Load shedding for power supply protection
- Capacitive load switching mode
- Low operating current (idle mode) for active supply during parking
- ISO 26262 safety element out of context for safety requirements up to ASIL D

Potential applications

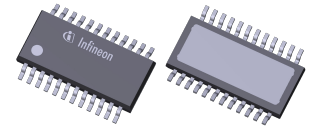
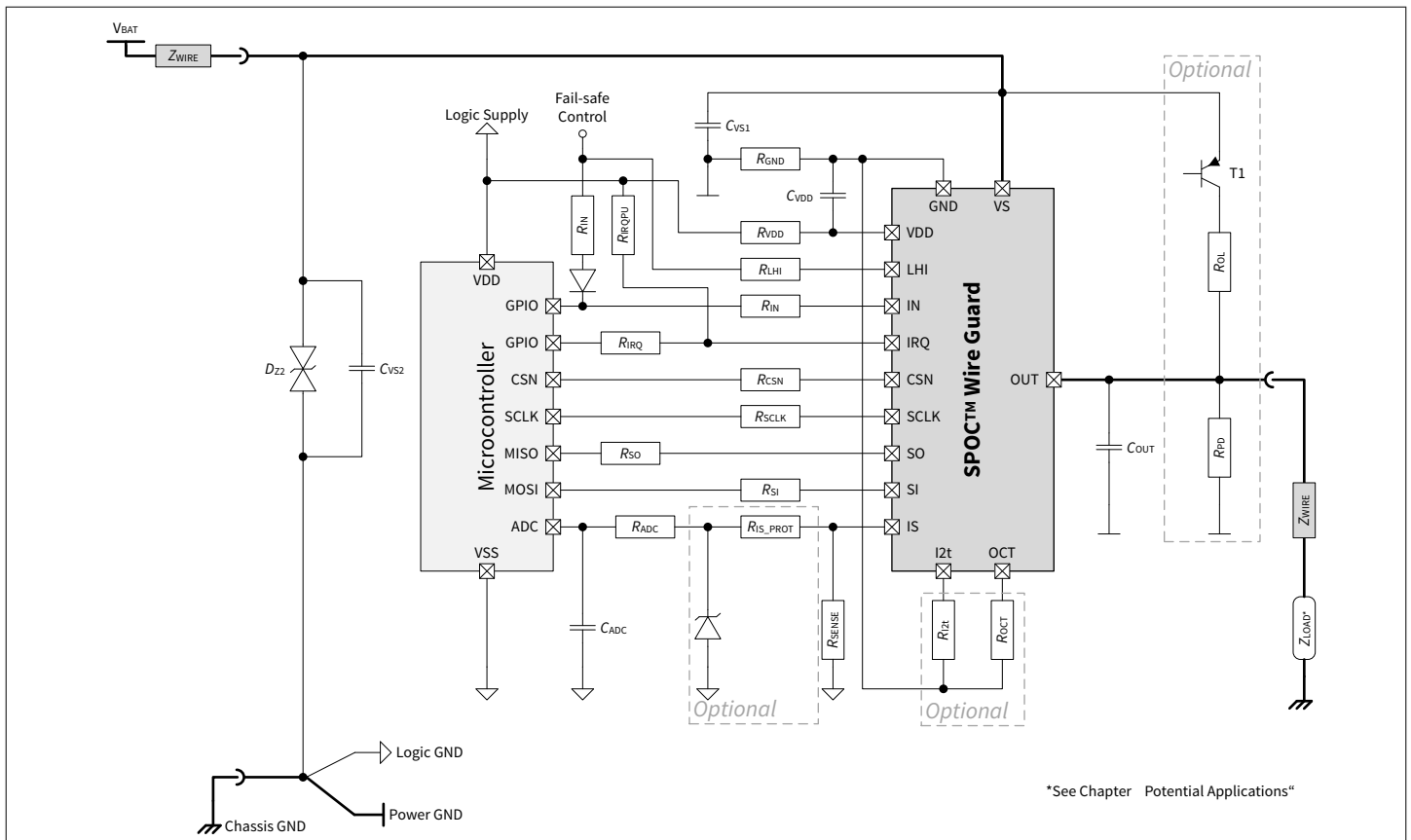
- Fail operational power supply
- Fuse and relay replacement in 12 V power distribution
- ECU main switch
- Load shedding for power supply protection
- Active supply during parking mode

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100, Grade 1.

Description

The SPOC™ Wire Guard is a smart high-side power switch with SPI as digital interface. The device is suitable for applications driving loads up to a nominal current of 34.5 A and supporting inrush currents. In addition to standard protection and standard diagnosis functions, the device offers selectable overcurrent protection, selectable I²t protection, selectable undervoltage and overvoltage lockout, idle mode, fail safe mode, limp home mode, and enhanced diagnosis via the digital interface.





Description

Package	Marking
PG-TSDSO-24	S0009SWPF1

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1 Product description

Basic features

- High-side power switch with diagnosis and embedded protection
- Daisy chain capable 24 bit SPI with CRC
- 3.3 V and 5 V compatible logic pins
- Low operating current (idle mode) for active supply during parking
- Idle mode with indication pin for microcontroller wake-up
- Capacitive load switching mode
- Reverse ON for low power dissipation in reverse polarity
- Switch-ON capability while inverse current condition (Inverse ON)
- Non-volatile memory (NVM), to store default configuration settings
- Optimized for high immunity against electromagnetic interference (EMI)
- Green product (RoHS compliant)

Protection features

- Configurable restart control
- Absolute and dynamic temperature limitation
- Overcurrent protection with selectable overcurrent threshold
- Undervoltage shutdown
- Configurable integrated I₂t function for system protection
- Configurable battery voltage dependent system protection
- Overvoltage protection with external components

Diagnosis features

- Proportional load current sense
- Proportional V_S measurement
- Proportional chip temperature measurement
- Open load in ON and OFF state
- Short circuit to ground and battery
- Enhanced diagnosis feedback via digital interface

Functional safety features

- ISO 26262 safety element out of context for safety requirements up to ASIL D
- SPI interface with error detection (CRC, invalid read/write address, and SCLK count error detection)
- Communication watchdog
- Limp home mode and fail safe mode
- Monitoring of input pin status (IN and LHI)
- Current sense verification mode

Table 1 Product summary

Parameter	Symbol	Values
Power supply voltage range for normal operation	$V_{S(NOR)}$	5 V to 20 V
Extended power supply voltage range for operation	$V_{S(EXT)}$	2.8 V to 28 V
Digital supply voltage range for normal operation	$V_{DD(NOR)}$	2.4 V to 5.5 V
Maximum digital supply current consumption in normal operation	$I_{VDD(NORMAL)}$	2.6 mA
Typical operating current in active mode (all power stages ON)	$I_{GND(ACTIVE)}$	7.2 mA
Typical operating current in idle mode (all power stages ON)	$I_{GND(IDLE)}$	60 μ A

(table continues...)

Table 1 (continued) Product summary

Parameter	Symbol	Values
Junction temperature range for normal operation	$T_{J(NOR)}$	-40°C to 150°C
Load dump voltage	$V_{BAT(LD)}$	35 V
Typical thermal resistance junction-to-ambient	$R_{th(JA)}$	20 K/W
Maximum ON-state resistance ($T_J = 150^\circ\text{C}$)	$R_{DS(ON)_150}$	1.85 mΩ
Nominal load current ($T_A = 85^\circ\text{C}$)	$I_{L(NOM)_85}$	34.5 A
Typical overcurrent detection threshold range	$I_{L(OCT)}$	72 A to 209 A

2 Block diagram and terms

2.1 Block diagram

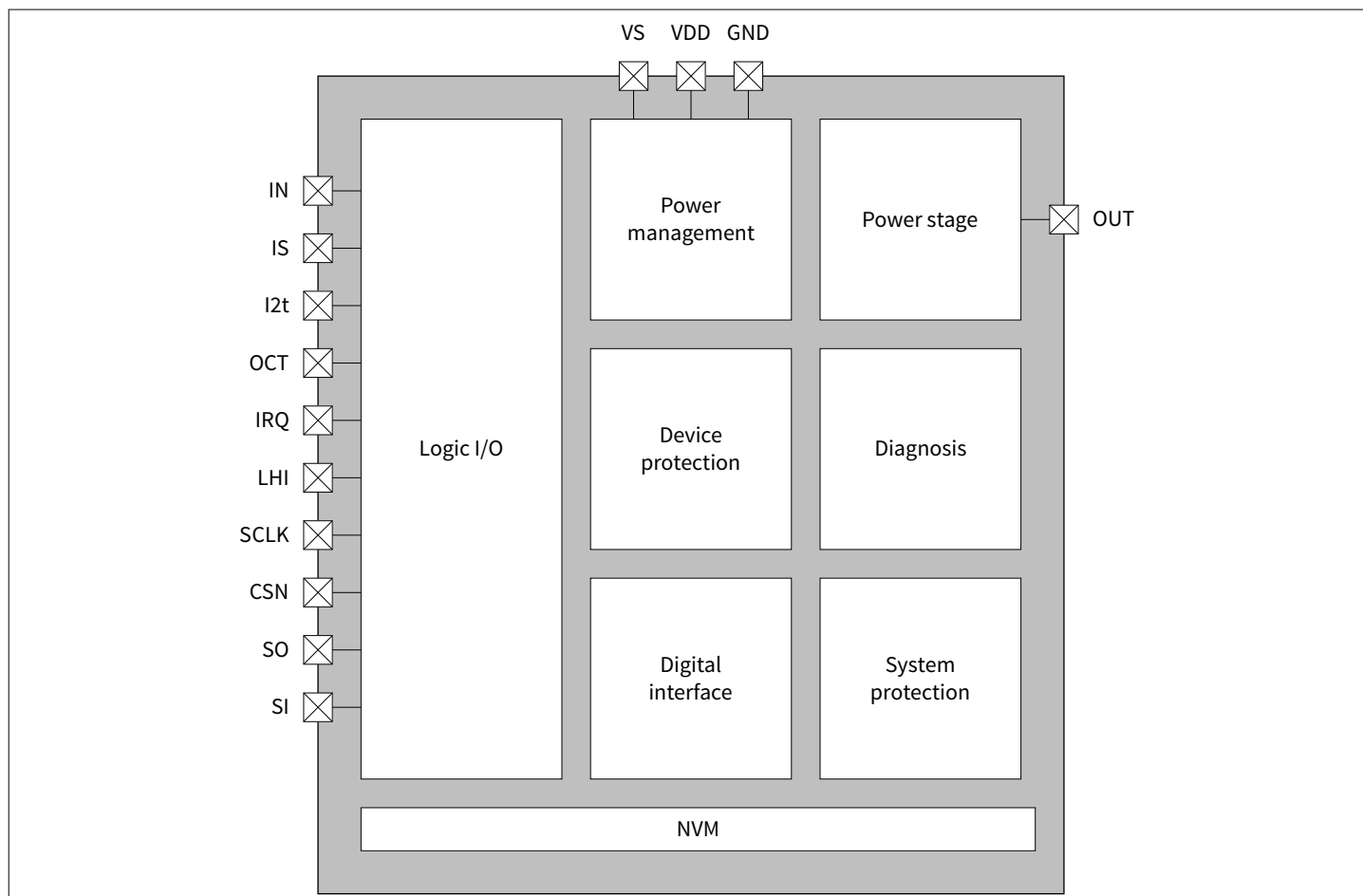


Figure 1 **Block diagram**

2.2 Terms

The figure below shows all the terms used in this datasheet, with their associated conventions for positive values. Voltages and currents are defined accordingly.

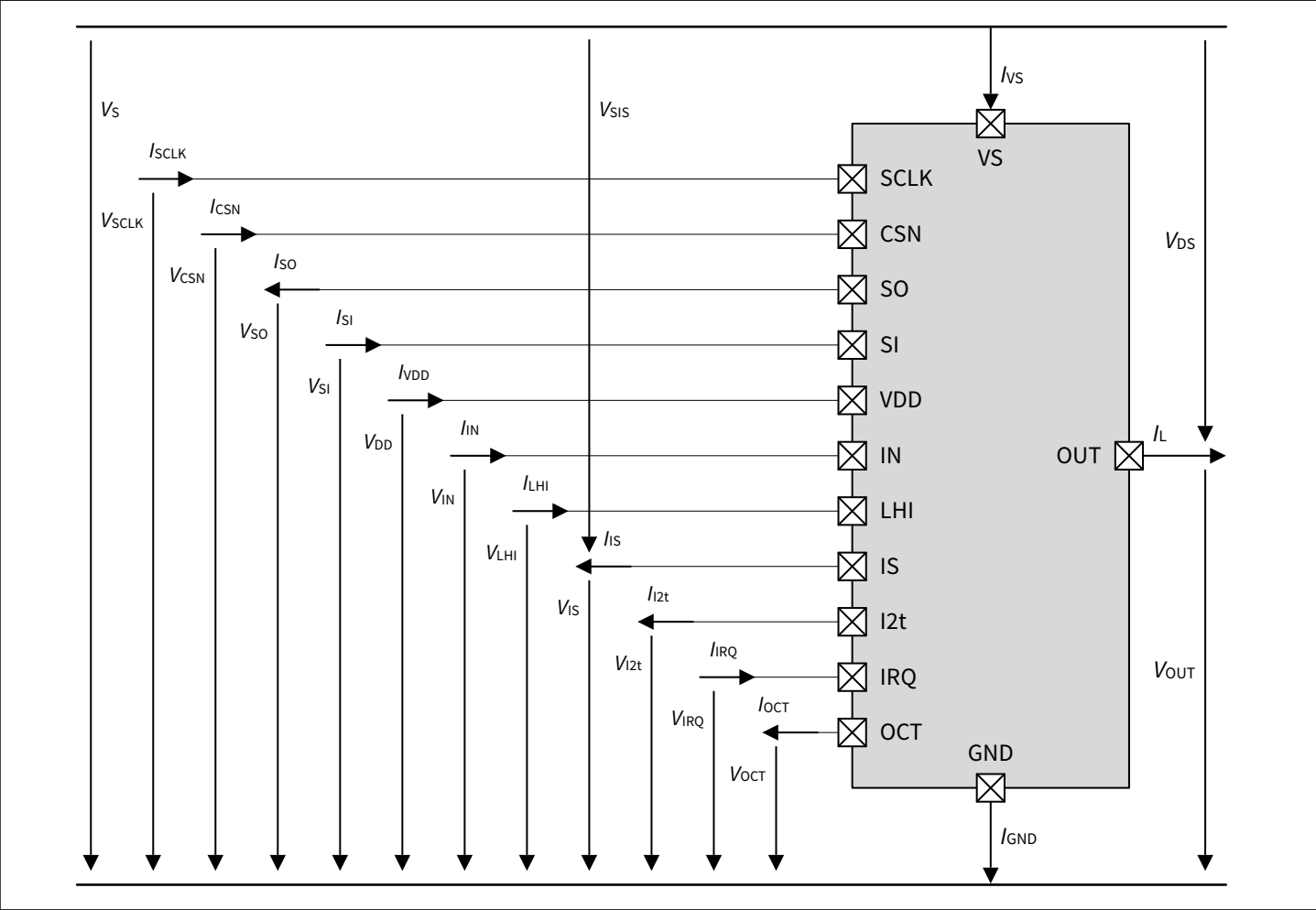


Figure 2 Voltage and current conventions

3 Pin configuration

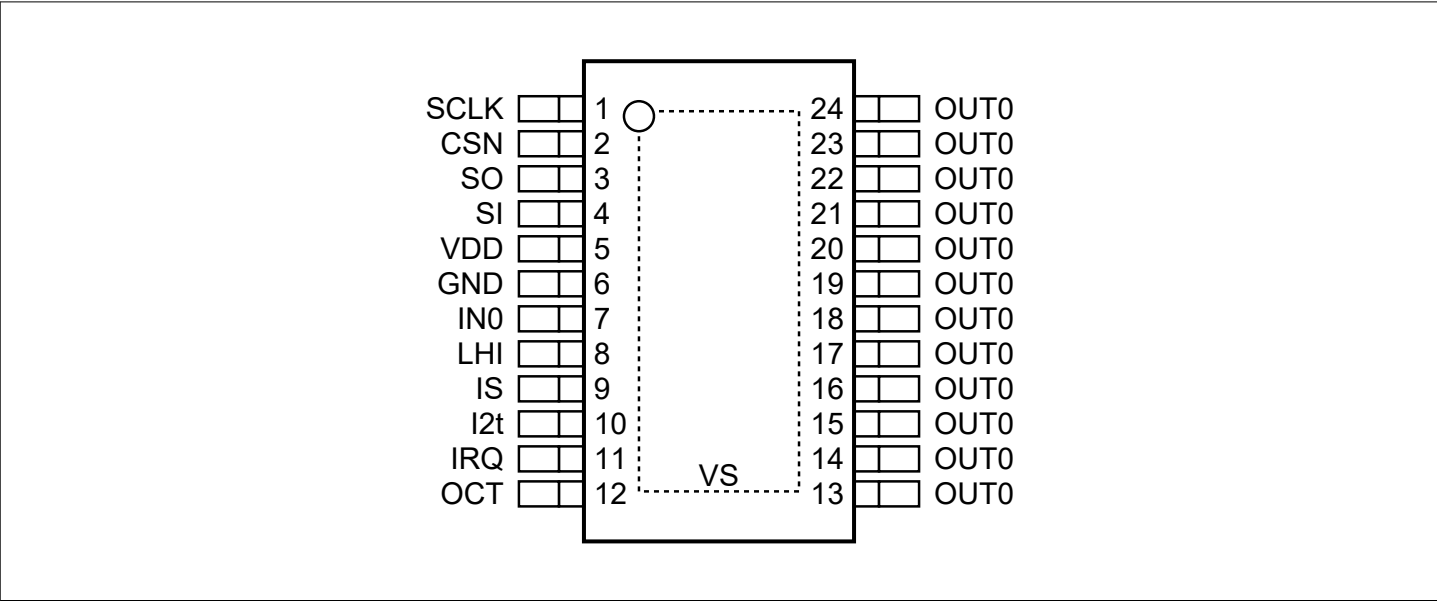


Figure 3 Pin configuration

Table 2 Pin definition

Pin	Symbol	I/O	Function
EP	VS (exposed pad)	–	Power supply voltage Battery voltage
1	SCLK	I	Serial clock Serial clock of SPI interface (active HIGH)
2	CSN	I	Chip select Chip select of SPI interface (active LOW); integrated pull up to VDD
3	SO	O	Serial output Serial output of SPI interface
4	SI	I	Serial input Serial input of SPI interface
5	VDD	–	Digital supply voltage
6	GND	–	Ground Ground connection for the internal logic
7	IN0	I	Input Digital signal to switch ON the power stage (active HIGH) If not used: connect with $R_{IN} = 4.7\text{ k}\Omega$ resistor either to GND pin or to logic GND of the module

(table continues...)

Table 2 (continued) Pin definition

Pin	Symbol	I/O	Function
8	LHI	I	Limp home input Digital signal to enter limp home mode (active HIGH) If not used: connect with $R_{LHI} = 4.7 \text{ k}\Omega$ resistor either to GND pin or to logic GND of the module
9	IS	O	SENSE current output Analog signal for diagnosis If not used: leave open
10	I2t	I	Selectable I2t protection curve A resistor R_{I2t} needs to be connected between I2t pin and GND pin to select one of the available I2t protection curves If not used: leave open. I2t protection curve selection as described in the I2t protection chapter
11	IRQ	O	Interruption request open drain output Digital signal to inform the microcontroller of idle mode, warning, error or watchdog overflow (active HIGH) If not used: connect with a $10 \text{ k}\Omega$ resistor either to GND pin or to logic GND of the module
12	OCT	I	Selectable overcurrent threshold A resistor R_{OCT} needs to be connected between OCT pin and GND pin to select one of the available overcurrent thresholds If not used: leave open. Threshold selection as described in the overcurrent protection chapter
13-24	OUT0	O	Output Protected high-side power stage output 0 ¹⁾

1) All output pins of the power stage have to be connected together on the PCB. All pins of the output are connected together internally. PCB traces have to be designed to withstand the maximum current that can flow.

4 General product characteristics

4.1 Absolute maximum ratings

Table 3 Absolute maximum ratings

$T_J = T_{J(NOR)}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			

Supply pins

Power supply voltage	V_S	-0.3	–	28	V	–	PRQ-522
Digital supply voltage	V_{DD}	-0.3	–	5.5	V	–	PRQ-546
Load dump voltage	$V_{BAT(LD)}$	–	–	35	V	Suppressed load dump acc. to ISO16750-2 (2012), $R_i = 2 \Omega$	PRQ-1410
Power supply voltage for short circuit protection	$V_{BAT(SC)}$	0	–	28	V	Setup acc. to AEC-Q100-012	PRQ-524
Reverse polarity voltage	$V_{BAT(REV)}$	-18	–	–	V	$t_{REV} \leq 5 \text{ min}$, $T_A = 25^\circ\text{C}$	PRQ-525
Current through GND pin	I_{GND}	-50	–	50	mA	–	PRQ-528
Current through VDD pin	I_{VDD}	-10	–	45	mA	$t_{REV} \leq 5 \text{ min}$	PRQ-586

Digital Input (DI) pins: IN, LHI, CSN, SCLK, SI

Current through DI pin	I_{DI}	-1	–	2	mA	¹⁾	PRQ-530
Current through DI pin - reverse battery condition	$I_{DI(REV)}$	-1	–	10	mA	$t_{REV} \leq 5 \text{ min}$ ¹⁾	PRQ-531

Analog Input (AI) pins: I2t, OCT

Current through AI pin	I_{AI}	-2	–	2	mA	²⁾	PRQ-532
Current through AI pin - reverse battery condition	$I_{AI(REV)}$	-2	–	0.1	mA	$t_{REV} \leq 5 \text{ min}$ ²⁾	PRQ-533

Digital Output (DO) pins: SO, IRQ

Current through SO pin	I_{SO}	-2	–	1	mA	³⁾	PRQ-535
Current through SO pin - reverse battery condition	$I_{SO(REV)}$	-10	–	1	mA	$t_{REV} \leq 5 \text{ min}$ ³⁾	PRQ-536
Voltage at IRQ pin	V_{IRQ}	-0.3	–	5.5	V	³⁾	PRQ-557
Current through IRQ pin	I_{IRQ}	-1	–	2	mA	³⁾	PRQ-555

(table continues...)

Table 3 (continued) Absolute maximum ratings

$$T_J = T_{J(NOR)}$$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Current through IRQ pin - reverse battery condition	$I_{IRQ(REV)}$	-1	–	10	mA	$t_{REV} \leq 5 \text{ min}$ ³⁾	PRQ-556

IS pin

Voltage at IS pin	V_{IS}	-1.5	–	V_S	V	–	PRQ-537
Current through IS pin	I_{IS}	-25	–	15	mA	–	PRQ-538

Temperatures

Junction temperature	T_J	-40	–	150	°C	–	PRQ-539
Storage temperature	T_{STG}	-55	–	150	°C	–	PRQ-540

ESD robustness

ESD robustness all pins (HBM)	V_{ESD_HBM1}	-2	–	2	kV	⁴⁾	PRQ-541
ESD robustness OUT vs GND and VS connected (HBM)	V_{ESD_HBM2}	-4	–	4	kV	⁴⁾	PRQ-542
ESD robustness all pins (CDM)	V_{ESD_CDM1}	-500	–	500	V	⁵⁾	PRQ-543
ESD robustness corner pins (CDM)	V_{ESD_CDM2}	-750	–	750	V	⁵⁾	PRQ-544

Power stage

Maximum energy dissipation - single pulse	E_{AS}	–	–	380	mJ	$I_L = 2 \cdot I_{L(NOM)_85}, T_{J(0)} = 150^\circ\text{C}, V_S = 28 \text{ V}$	PRQ-1411
Maximum energy dissipation - repetitive pulse	E_{AR}	–	–	137	mJ	$I_L = I_{L(NOM)_85}, T_{J(0)} = 85^\circ\text{C}, V_S = 13.5 \text{ V}, 1 \text{ M cycles}$	PRQ-1412
Current through output pins	I_{OUT}	$-I_{L(HOCT_H),Max}$	–	$I_{L(HOCT_H),Max}$	A	$T_J < T_{J(ABS)}, (T_J - T_{J(0)}) < 60 \text{ K}$	PRQ-548

1) Maximum V_{DI} to be considered for latch-up tests: 5.5 V2) Maximum V_{AI} to be considered for latch-up tests: 5.5 V3) Maximum V_{DO} to be considered for latch-up tests: 5.5 V

4) Human body model (HBM) robustness according to AEC-Q100-002

5) Charged device model (CDM) robustness according to AEC-Q100-011 Rev-D; voltage level refers to test condition (TC) mentioned in the standard

Notes:

1. Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect the reliability of the device.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as outside the normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional range

Table 4 Functional range

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power supply voltage range for normal operation	$V_{S(NOR)}$	5	13.5	20	V	–	PRQ-549
Lower extended power supply voltage range for operation	$V_{S(EXT,LOW)}$	2.8	–	5	V	(Parameter deviations possible) ^{1) 2) 3)}	PRQ-550
Upper extended power supply voltage range for operation	$V_{S(EXT,UP)}$	20	–	28	V	$t < 1$ h (Parameter deviations possible) ²⁾	PRQ-551
Digital supply voltage range for normal operation	$V_{DD(NOR)}$	2.4	–	5.5	V	–	PRQ-553
Junction temperature range for normal operation	$T_{J(NOR)}$	-40	25	150	°C	–	PRQ-552

1) If the V_S voltage decreases: $V_{S(EXT,LOW),MIN} = 2.8$ V. If the V_S voltage increases: $V_{S(EXT,LOW),MIN} = 4.1$ V.

2) Protection functions continue to operate.

3) For $V_S \leq V_{S(UV)_H}$ no ADC related functions are available. For I2t protection a load current of $I_L = 0$ A is used.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical characteristics tables.

4.3 Thermal resistance

Table 5 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal characterization parameter junction-to-top	Ψ_{JTOP}	–	0.8	1.3	K/W	¹⁾	PRQ-650
Thermal resistance junction-to-case	R_{thJC}	–	0.6	0.9	K/W	¹⁾	PRQ-651
Thermal resistance junction-to-ambient	R_{thJA}	–	20	–	K/W	¹⁾	PRQ-652

1) According to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board, the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 μm Cu, 2 × 35 μm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Simulation done at $T_A = 105\text{ °C}$, $P_{DISSIPATION} = 1\text{ W}$

4.3.1 PCB setup

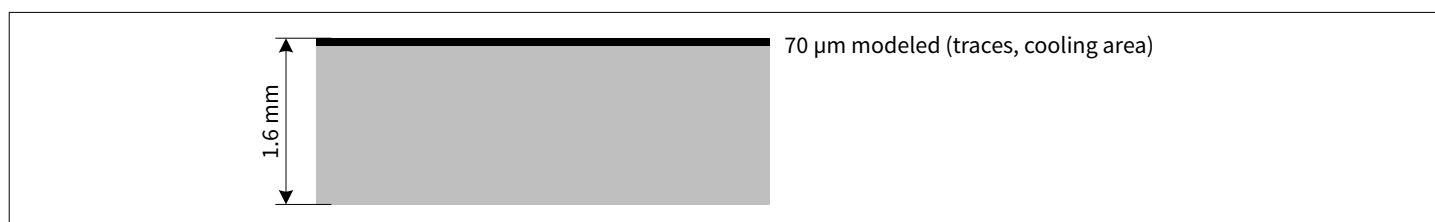


Figure 4 1s0p PCB cross section

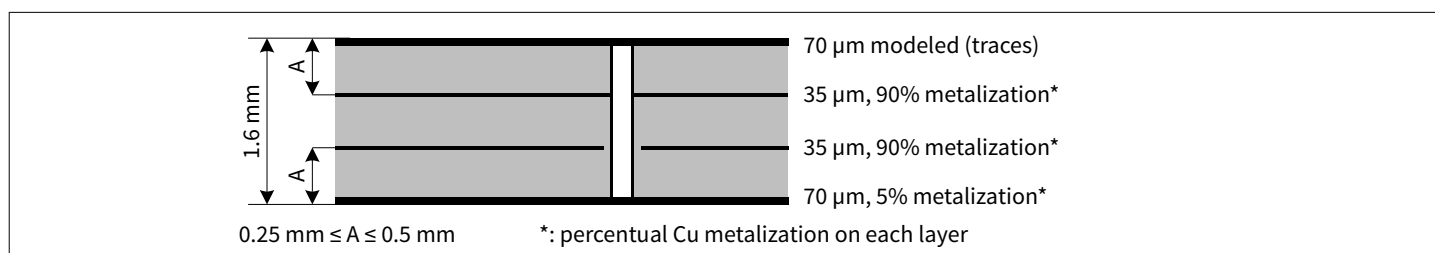


Figure 5 2s2p PCB cross section

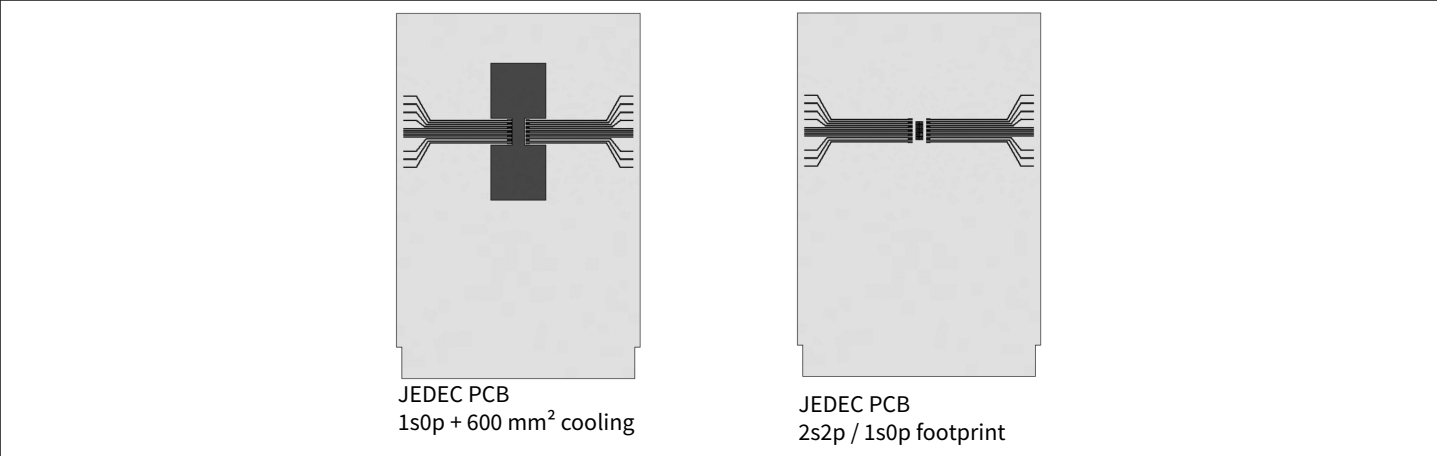


Figure 6 PCB Setup for thermal simulations

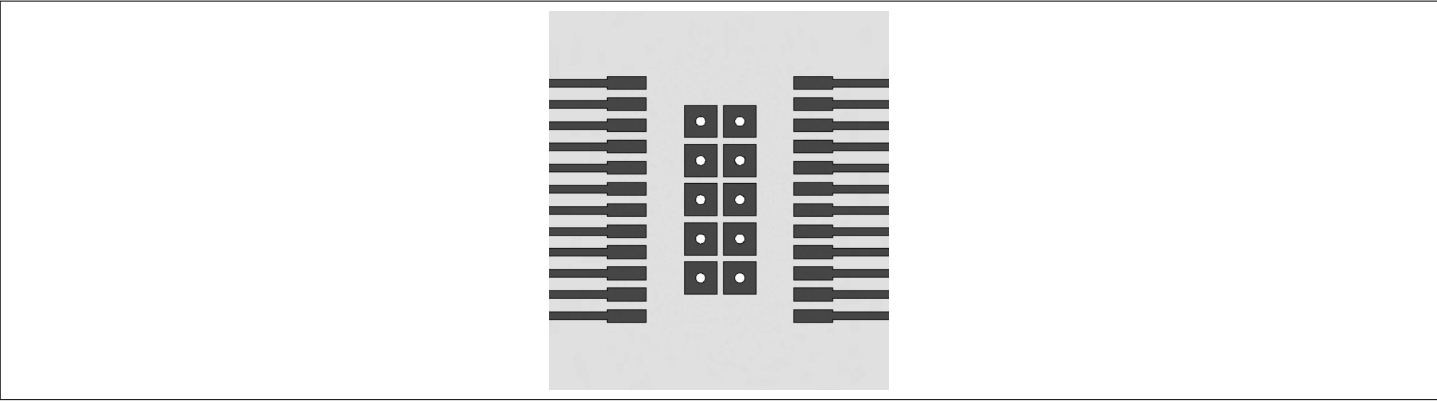


Figure 7 Thermal vias on PCB for 2s2p PCB setup

4.3.2 Thermal impedance

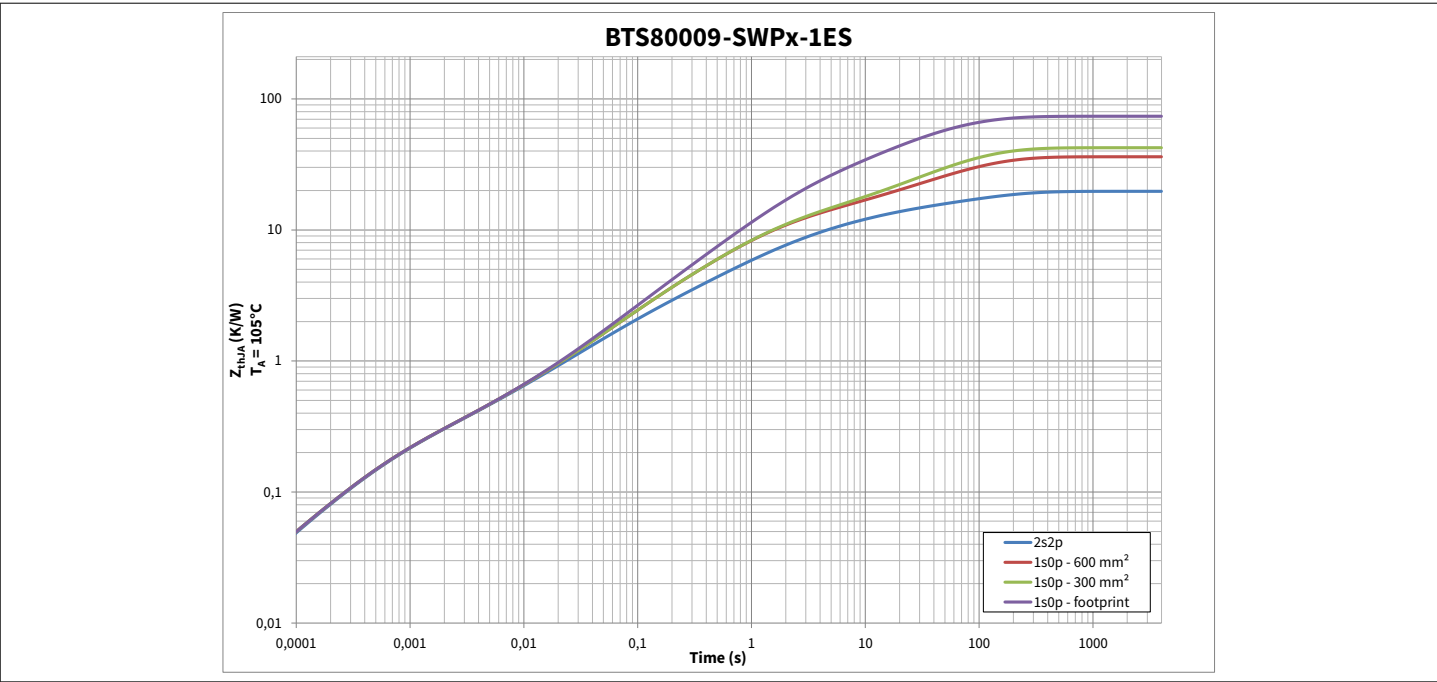


Figure 8 Typical thermal impedance

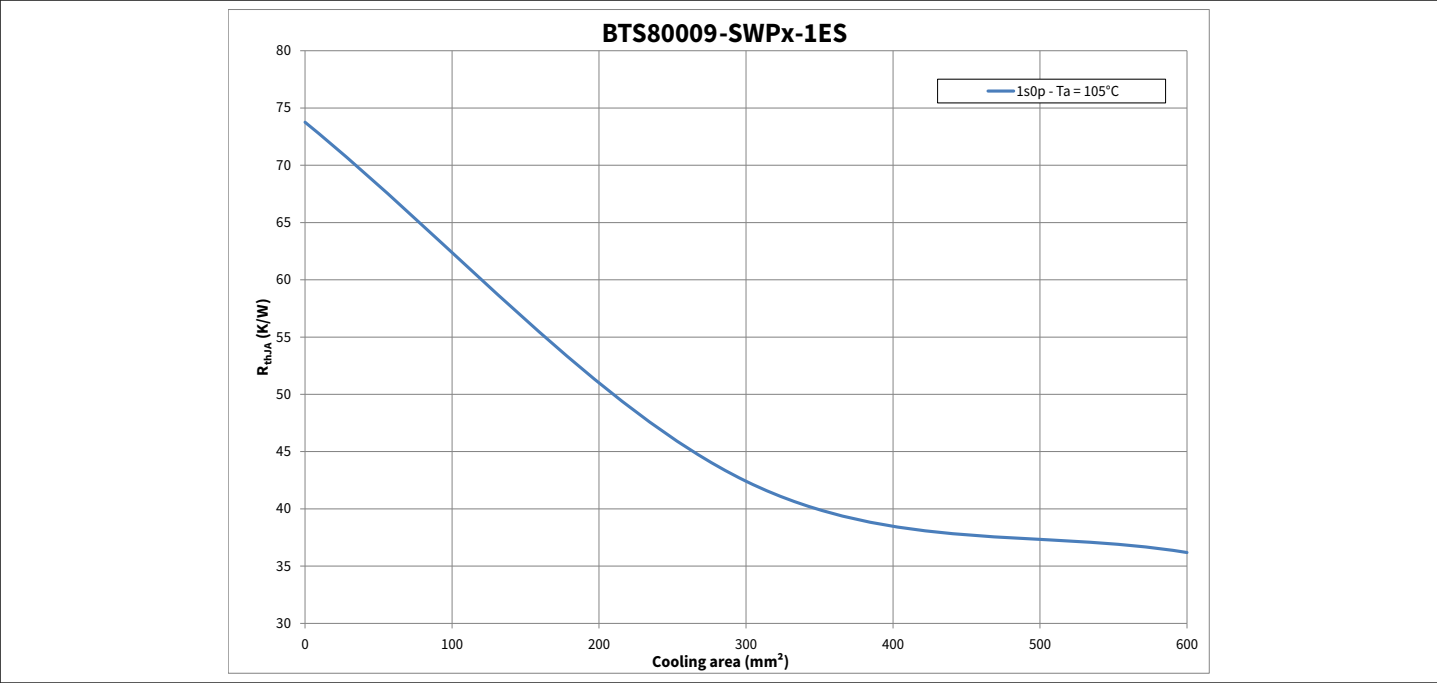


Figure 9 Typical thermal resistance on 1s0p PCB with various cooling surfaces

5 Logic I/O

The device has 6 digital pins to configure and control the device. Additionally, there are 2 analog input pins for either selecting a predefined I2t protection curve or selecting the overcurrent threshold. Furthermore, one open drain output pin is available for additional status reporting and interruption requests.

5.1 Digital I/O pins

The digital input circuitry is compatible with 3.3 V and 5 V microcontrollers. The logic thresholds for LOW and HIGH states are defined by the parameters $V_{DI(TH)}$ and $V_{DI(HYS)}$. The relationship between these two values is shown in the figure below. The voltage V_{DI} needed to ensure a HIGH state is always higher than the voltage needed to ensure a LOW state.

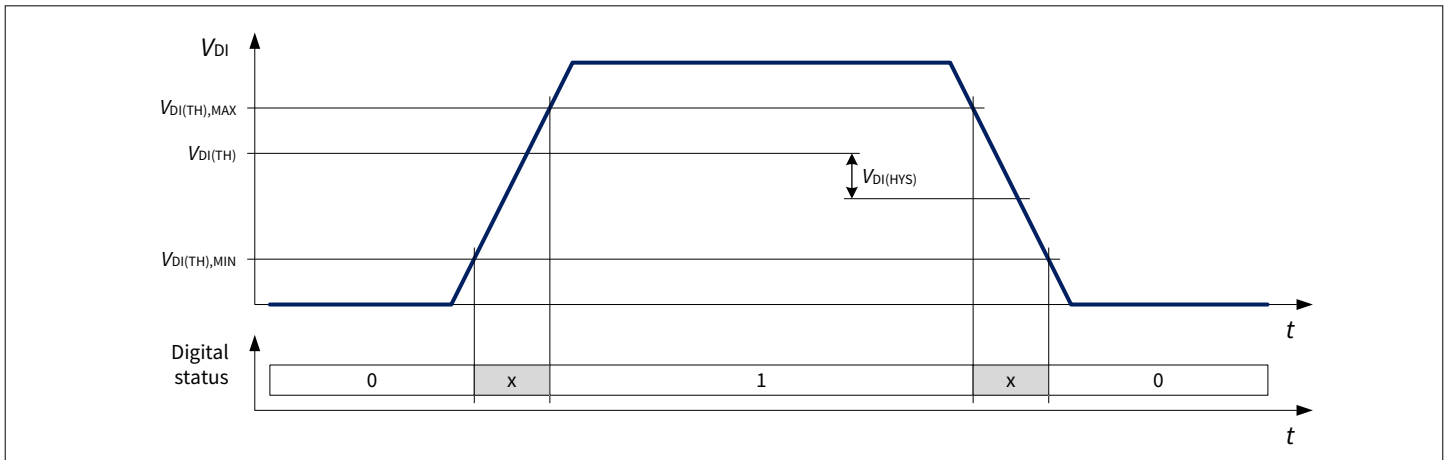


Figure 10 Digital input threshold voltages and hysteresis

5.1.1 Input pin (IN)

The IN pin sets the IN status which is further used by the power stage control logic. The simplified circuitry of the input structure is shown in the figure below.

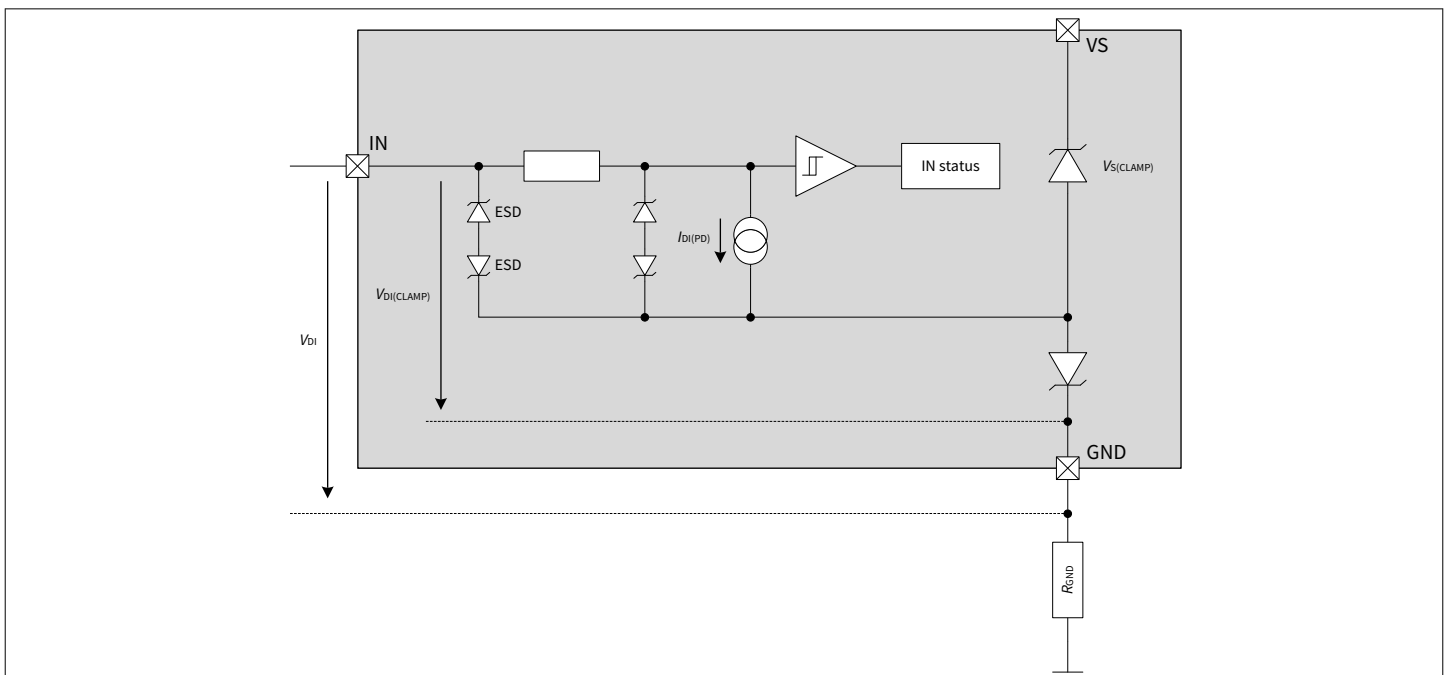


Figure 11 Input pin circuitry

To achieve a very low current consumption in idle mode, the device is not sensitive to the IN pin in idle mode. This allows the microcontroller to switch the GPIO controlling the IN pin into high impedance, while keeping the state of the input status unchanged.

The logic level of the input pin can be monitored via the input status monitoring. If there is a HIGH level on the input pin, the dedicated bit is set until the next readout of the dedicated register.

5.1.2 SPI pins

The serial peripheral interface (SPI) is a full-duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and CSN.

5.1.3 Limp home input pin (LHI)

To enter the limp home mode, the device features a limp home input pin. The simplified circuitry of the LHI structure is shown in the figure below.

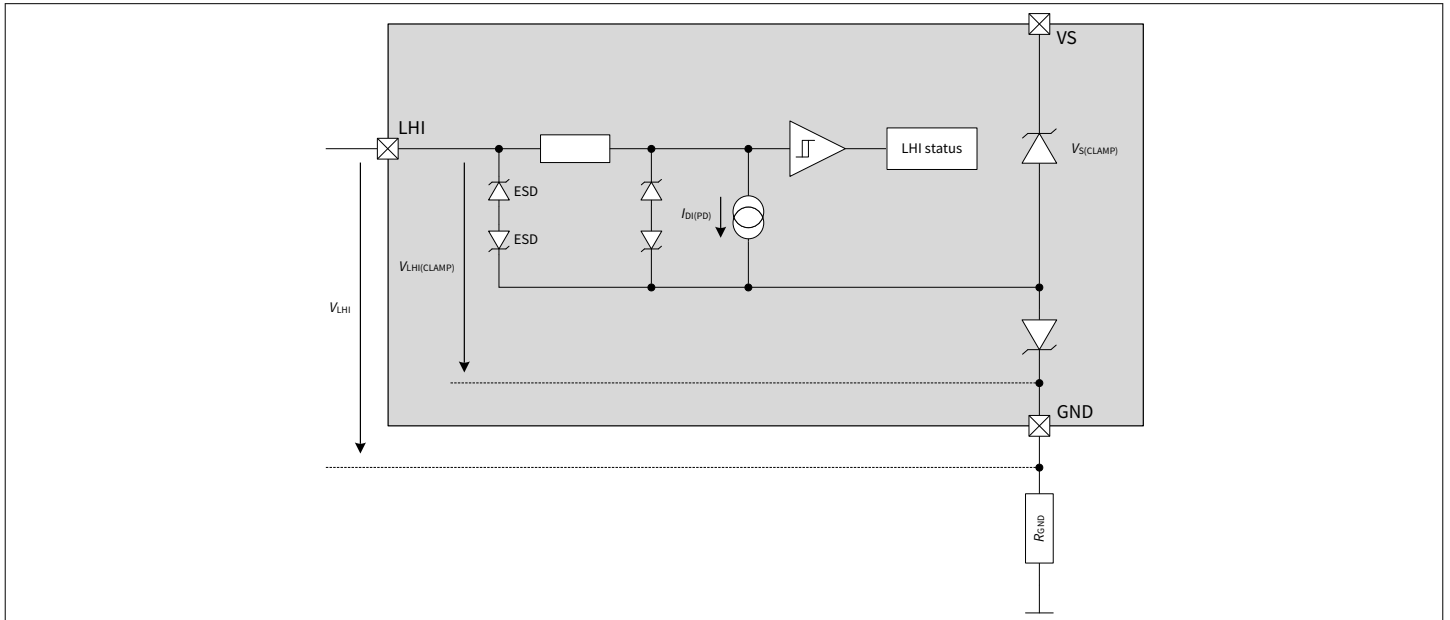


Figure 12 LHI pin circuitry

5.1.4 Interruption request pin (IRQ)

The Interruption request pin (IRQ) is an open drain output that reports the status of:

- Idle mode
- Error flags
- Protection flags
- Warning flags
- Watchdog

To minimize the current consumption in the low power modes, the IRQ pin is set there to high impedance. Once the appropriate low power mode is left, the IRQ pin is pulled down and follows the dedicated functions.

Additionally, the IRQ pin is in high impedance when the device is in NVM mode. Once the NVM mode is left, the IRQ pin is pulled down and follows the dedicated functions.

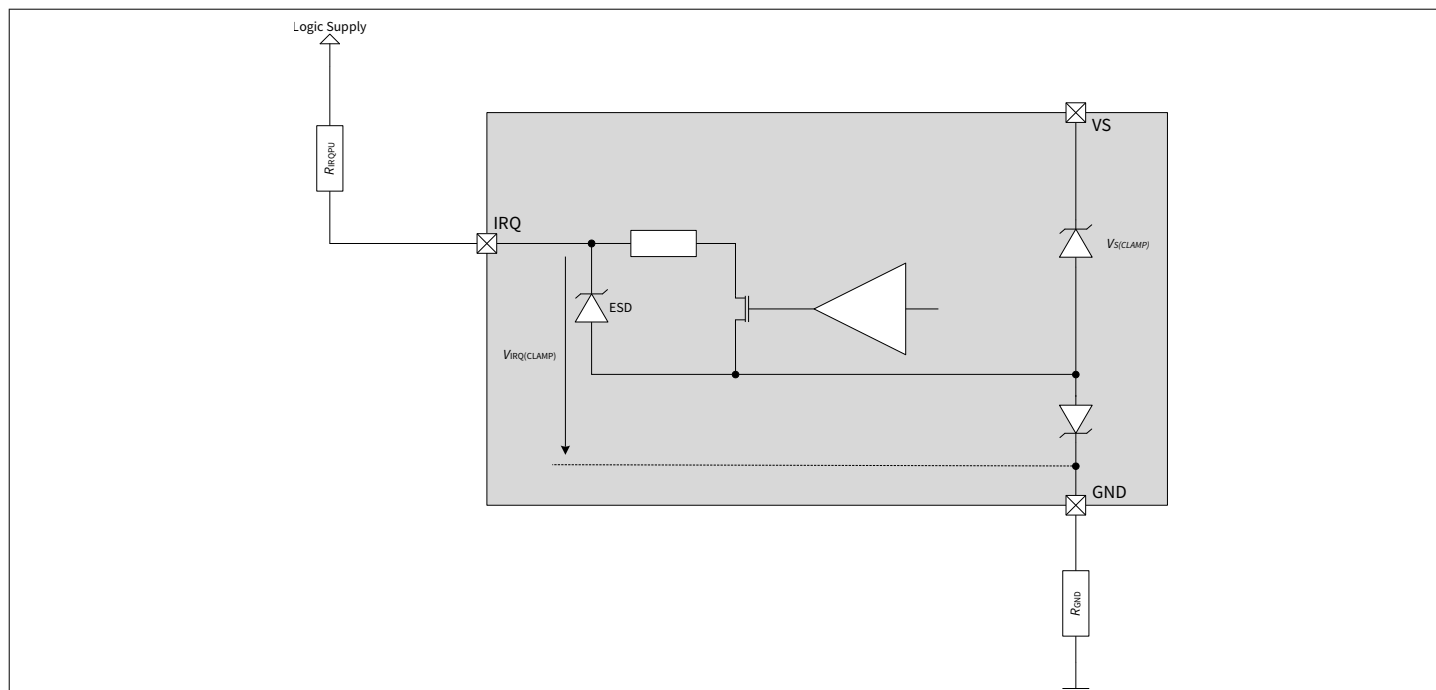


Figure 13 IRQ pin circuitry

The IRQ pin is supplied by both V_S and V_{DD} . The pin remains functional as long as at least one supply voltage is above its respective undervoltage threshold ($V_{S(UV)}$ or $V_{DD(UV)}$).

5.2 Analog I/O pins

5.2.1 I2t selection pin (I2t)

The I2t selection pin (I2t) is used to select one of the available I2t protection curves by connecting a resistor R_{I2t} between the I2t pin and the GND pin.

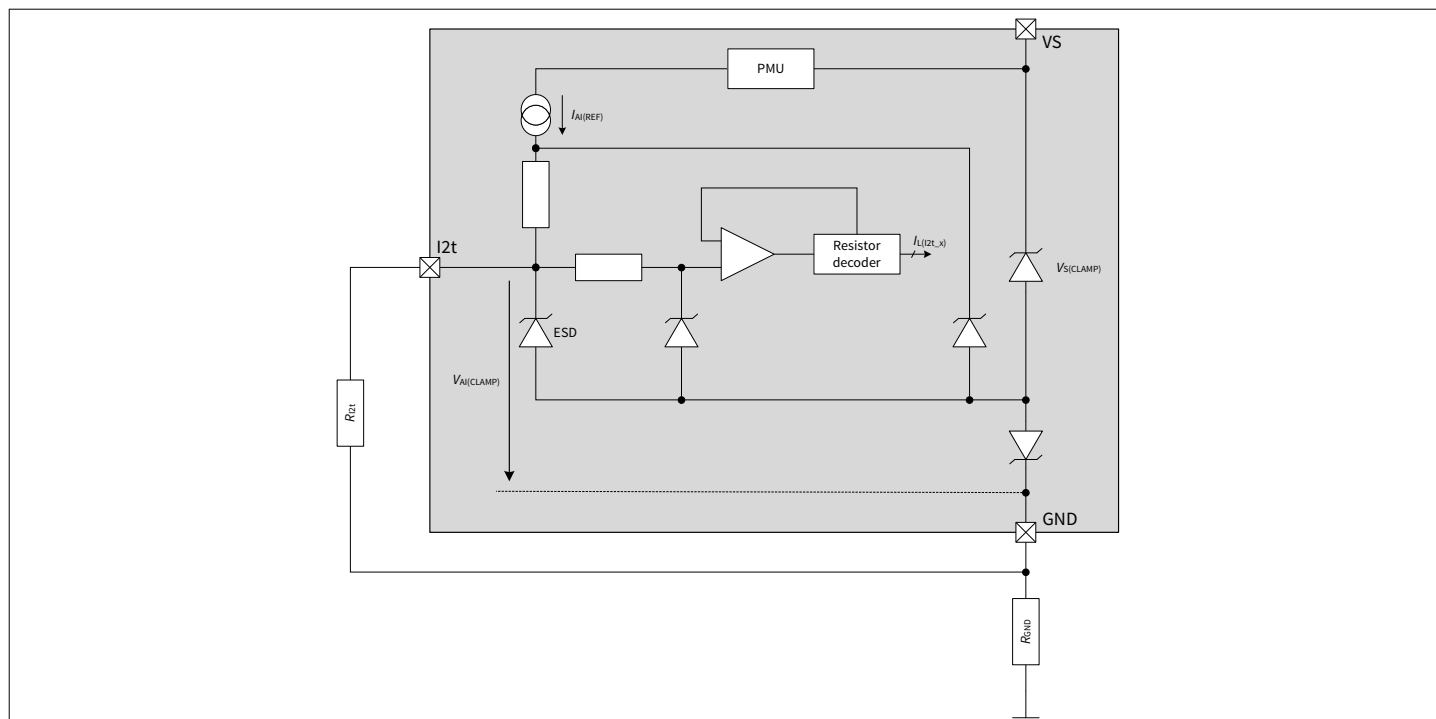


Figure 14 **I2t selection pin circuitry**

5.2.2 Overcurrent threshold selection pin (OCT)

The overcurrent threshold (OCT) selection pin is used to select one of the available overcurrent thresholds by connecting a resistor R_{OCT} between the OCT pin and the GND pin.

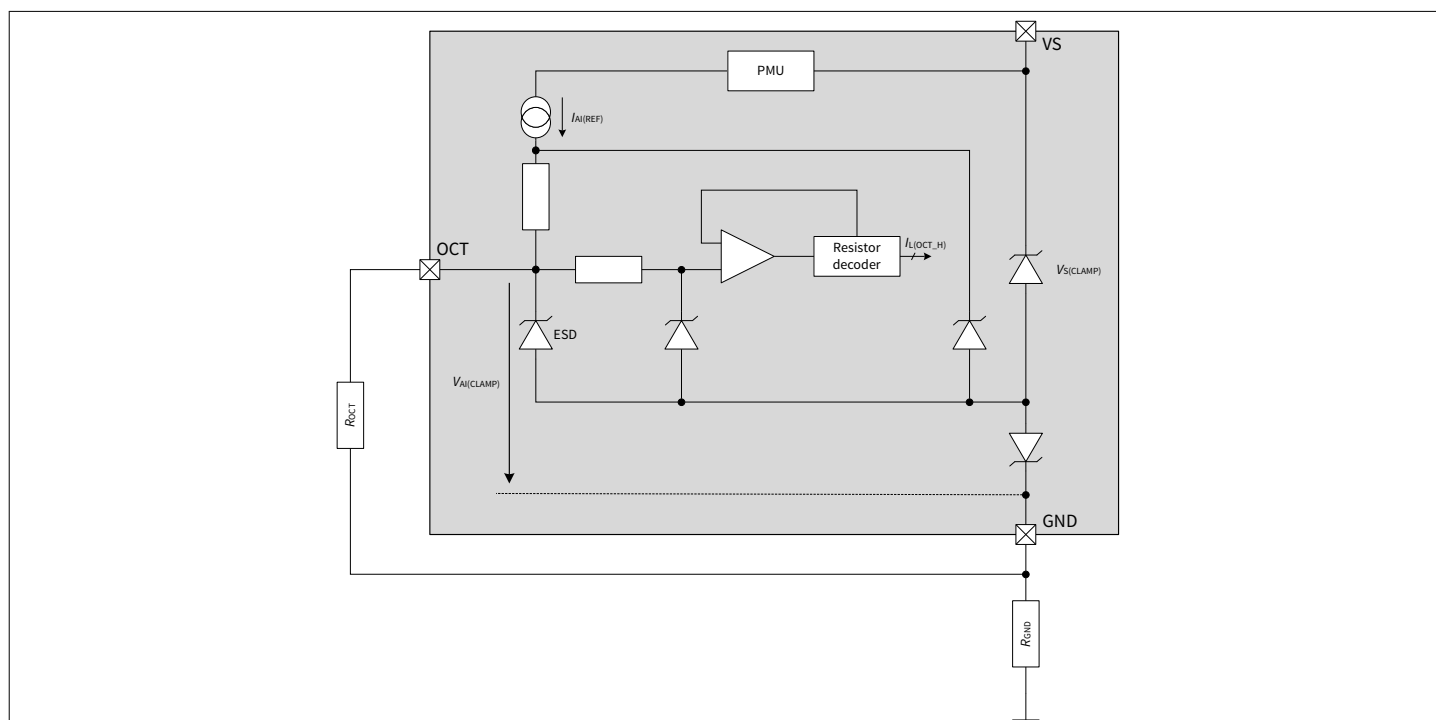


Figure 15 **OCT selection pin circuitry**

5.3 Electrical characteristics - logic pins

Table 6 Electrical characteristics - logic pins

$$V_S = V_{S(NOR)}, T_J = T_{J(NOR)}$$

Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			

Digital input (DI) pins: IN, LHI, CSN, SCLK, SI

Digital input clamping voltage of pin IN	$V_{IN(CLAMP1)}$	–	7.6	–	V	$I_{DI} = 1 \text{ mA}$	PRQ-694
Digital input clamping voltage of pin IN	$V_{IN(CLAMP2)}$	7.1	8.1	9.1	V	$I_{DI} = 2 \text{ mA}$	PRQ-695
Digital input clamping voltage of pin LHI	$V_{LHI(CLAMP1)}$	–	7.6	–	V	$I_{DI} = 1 \text{ mA}$	PRQ-1416
Digital input clamping voltage of pin LHI	$V_{LHI(CLAMP2)}$	7.1	8.1	9.1	V	$I_{DI} = 2 \text{ mA}$	PRQ-1417
Digital input clamping voltage of pin CSN	$V_{CSN(CLAMP1)}$	–	7	–	V	$I_{DI} = 1 \text{ mA}$	PRQ-702
Digital input clamping voltage of pin CSN	$V_{CSN(CLAMP2)}$	6.5	7.5	8.5	V	$I_{DI} = 2 \text{ mA}$	PRQ-703
Digital input clamping voltage of pin SCLK	$V_{SCLK(CLAMP1)}$	–	7	–	V	$I_{DI} = 1 \text{ mA}$	PRQ-704
Digital input clamping voltage of pin SCLK	$V_{SCLK(CLAMP2)}$	6.5	7.5	8.5	V	$I_{DI} = 2 \text{ mA}$	PRQ-705
Digital input clamping voltage of pin SI	$V_{SI(CLAMP1)}$	–	7	–	V	$I_{DI} = 1 \text{ mA}$	PRQ-706
Digital input clamping voltage of pin SI	$V_{SI(CLAMP2)}$	6.5	7.5	8.5	V	$I_{DI} = 2 \text{ mA}$	PRQ-707
Digital input voltage threshold	$V_{DI(TH)}$	0.8	1.3	1.8	V	–	PRQ-693
Digital input hysteresis	$V_{DI(HYS)}$	–	0.25	–	V	–	PRQ-696
Digital input pull down current	$I_{DI(PD)}$	2	10	25	μA	$V_{DI(TH),MIN} < V_{DI} < 5.5 \text{ V}$, CSN pin excluded	PRQ-698
Digital input pull up current of pin CSN	$I_{CSN(PU)}$	-25	-10	-2	μA	$0 \text{ V} < V_{CSN} < V_{DI(TH),MAX}$	PRQ-712

Digital Output (DO) pins: IRQ, SO

Digital output clamping voltage of pin IRQ	$V_{IRQ(CLAMP1)}$	–	6	–	V	IRQ pin is high impedance, $I_{IRQ} = 1 \text{ mA}$	PRQ-720
Digital output clamping voltage of pin IRQ	$V_{IRQ(CLAMP2)}$	5.7	6.7	7.7	V	IRQ pin is high impedance, $I_{IRQ} = 2 \text{ mA}$	PRQ-721

(table continues...)

Table 6 (continued) Electrical characteristics - logic pins $V_S = V_{S(NOR)}, T_J = T_{J(NOR)}$ Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}, T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Digital output voltage (LOW) of pin IRQ	$V_{IRQ(L)}$	–	–	0.35	V	$I_{IRQ} \leq 0.5 \text{ mA}$	PRQ-1386
Digital output voltage (LOW) of pin SO	$V_{SO(L)}$	–	–	0.35	V	$I_{SO} \geq -0.5 \text{ mA}$	PRQ-717
Digital output voltage (HIGH) of pin SO	$V_{SO(H)}$	$V_{DD} - 0.5$	–	V_{DD}	V	$I_{SO} \leq 0.5 \text{ mA}$	PRQ-718
Output tristate leakage current of pin IRQ	$I_{IRQ(OFF)}$	-1.5	–	1.5	μA	$V_{IRQ} \leq 5.5 \text{ V}$	PRQ-1387
Output tristate leakage current of pin SO	$I_{SO(OFF)}$	-1	–	1	μA	$V_{CSN} = V_{DD}, V_{SO} = 0 \text{ V}$ or $V_{CSN} = V_{DD}, V_{SO} = V_{DD}$	PRQ-719

Analog Input (AI) pins: I2t, OCT

Analog input clamping voltage	$V_{AI(CLAMP)}$	1.5	–	4.5	V	$V_{S(REV)} \leq V_S < 0 \text{ V}, t \leq 5 \text{ min}, I_{AI} = -2 \text{ mA}$	PRQ-723
Analog input reference current	$I_{AI(REF)}$	20	25	30	μA	–	PRQ-724

6 Power management

The device is supplied by two supply voltages:

- Power supply voltage (V_S)
- Digital supply voltage (V_{DD})

The supply line of the V_S is connected to a battery feed and used for the driving circuitry of the power stage. V_{DD} is used for the logic of the digital interface and for driving the SO pin.

6.1 Operation modes and transitions

The behavior of the device and the availability of functions, are dependent on the mode in which the device is. This operation modes and the transitions between them are illustrated in the following chapter.

6.1.1 Operation modes

The device has the following operation modes which are reflected in the state diagram, as shown in the figure below.

- Power-up mode
- Sleep mode
- Inactive mode
- Active mode
- Limp home mode
- Fail safe mode
- Idle mode
- NVM mode

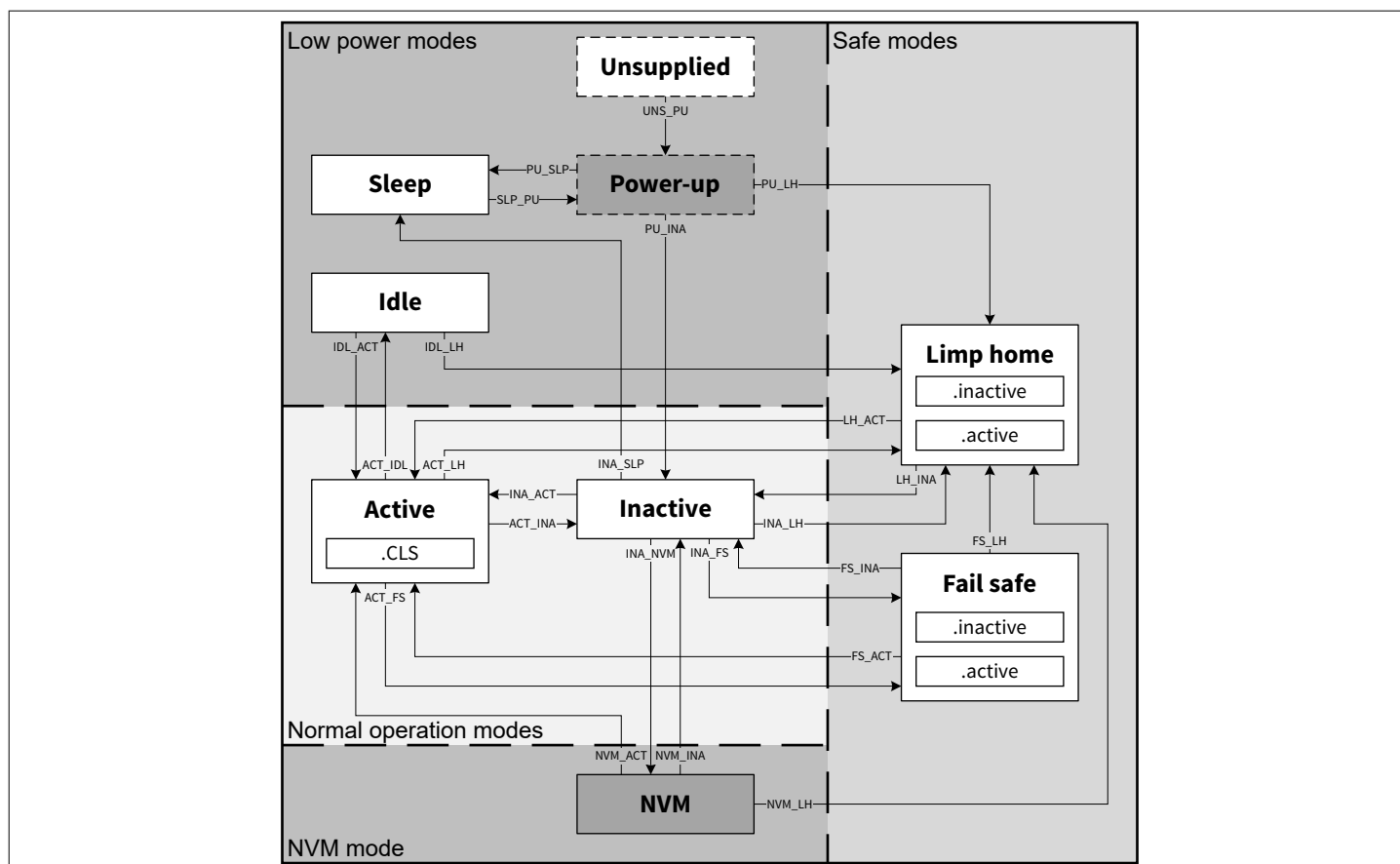


Figure 16 Operation modes - state diagram

6.1.1.1 Unsupplied

The device is in this mode if it is completely unsupplied (no voltage applied neither to the VS pin nor to the VDD pin). Unsupplied mode is left as soon as one of the supply voltages (V_{DD} or V_S) increases above its minimum operating voltage ($V_{S(OP)}$ or $V_{DD(OP)}$). In this mode, the device supports no functionality beside the overvoltage protection mechanism.

6.1.1.2 Power-up mode

Power-up mode is entered whenever the device is woken up (via CSN or LHI) or a rising edge on V_S occurs, which means also after a power supply undervoltage event.

During power-up mode, the default values are loaded to the registers within t_{PU} .

Although VDD is not mandatory for the read-out of default values, V_S needs to be above the power-up voltage ($V_{S(PU)}$).

If, during the read-out procedure, V_S drops below or is equal to $V_{S(PU)}$, the read-out process is aborted. Once the voltage is above $V_{S(PU)}$ again, the read-out is restarted.

If $V_{DD} > V_{DD(OP)}$, the digital interface is available after the wake-up time $t_{WU(SPI)}$, for read operations only. The only accepted write command is the mode selection command, which leads the device to leave power-up mode. The first response on the digital interface is the first communication frame.

Furthermore, the IRQ pin is in high impedance when the device is in power-up mode.

While the device is in power-up mode, a timeout counter is active. If no condition for a state transition is fulfilled before the counter exceeds $t_{PU(HOLD)}$, the device goes back to sleep mode.

The power-up mode can be left after t_{PU} to one of the following modes:

- Sleep mode: if the timeout counter reaches $t_{PU(HOLD)}$
- Limp home mode: if the LHI pin is HIGH
- Inactive mode: if the "normal operation modes" are requested via the mode selection command
- Idle mode: if the idle request information is retained after a power supply undervoltage event

6.1.1.3 Sleep mode

The sleep mode is entered either from power-up mode, or from one of the normal operation modes (if the conditions for entering sleep mode are fulfilled).

The conditions for entering sleep mode are:

- Mode selection is set to sleep mode
- The S_{I2t} is below the I2t status based on $I_{L(I2t_I)}$
- Power stage control = LOW (via digital interface and IN pin)
- Power stage is OFF
- No protection error is present, with latched-OFF power stage
- LHI = LOW

As long as the device is in sleep mode, the digital interface is deactivated and the IRQ pin is in high impedance.

However, the device can be woken up from sleep mode either via a rising edge on the CSN pin (in case $V_{DD} > V_{DD(OP)}$) or setting the LHI pin to HIGH. After any wake up signal is received, the device will go into the power-up mode.

The current consumption is reduced to the minimum (see parameters $I_{VS(SLEEP)}$ and $I_{VDD(SLEEP)}$).

6.1.1.4 Inactive mode

The device is in inactive mode when the power stage is disabled via the power stage control, the mode selection is set to "normal operation modes", and the LHI pin is LOW.

As the digital interface is available, the device can be configured and controlled via the intended registers.

6.1.1.5 Active mode

The device is in active mode when the power stage is enabled via the power stage control, the mode selection is set to "normal operation modes" and the LHI pin is set to LOW.

The availability of diagnosis functions and protection mechanisms within the active mode and its sub-mode are described in [Chapter 6.1.3](#).

To enable the charging of capacitive loads, the active mode provides a sub-mode called capacitive load switching mode (CLS mode).

The active.CLS mode is entered when the power stage control is set to HIGH while the corresponding bit is set (by default the bit is not set).

Transitioning from the CLS sub-mode to its active mode (active mode, limp home active mode, or fail safe active mode) can be requested by disabling the CLS mode or happens automatically when the device is in $R_{DS(ON)}$. This is indicated via the digital interface.

6.1.1.6 Limp home mode

The device enters limp home mode when the LHI pin is set to HIGH for $t > t_{LHI(AC)}$.

Once the LHI pin is set to HIGH for a time longer than $t_{FILTER(LHI)}$, the corresponding LHI bit in the communication diagnosis register is set to 1_B. This information is stored in this bit until the read-out of the communication diagnosis register by the microcontroller. For more information, refer to the figure below.

When the device enters limp home mode, the SPI registers are reset to their default values (as described in [Chapter 11](#)), and the SPI registers are available for read access only.

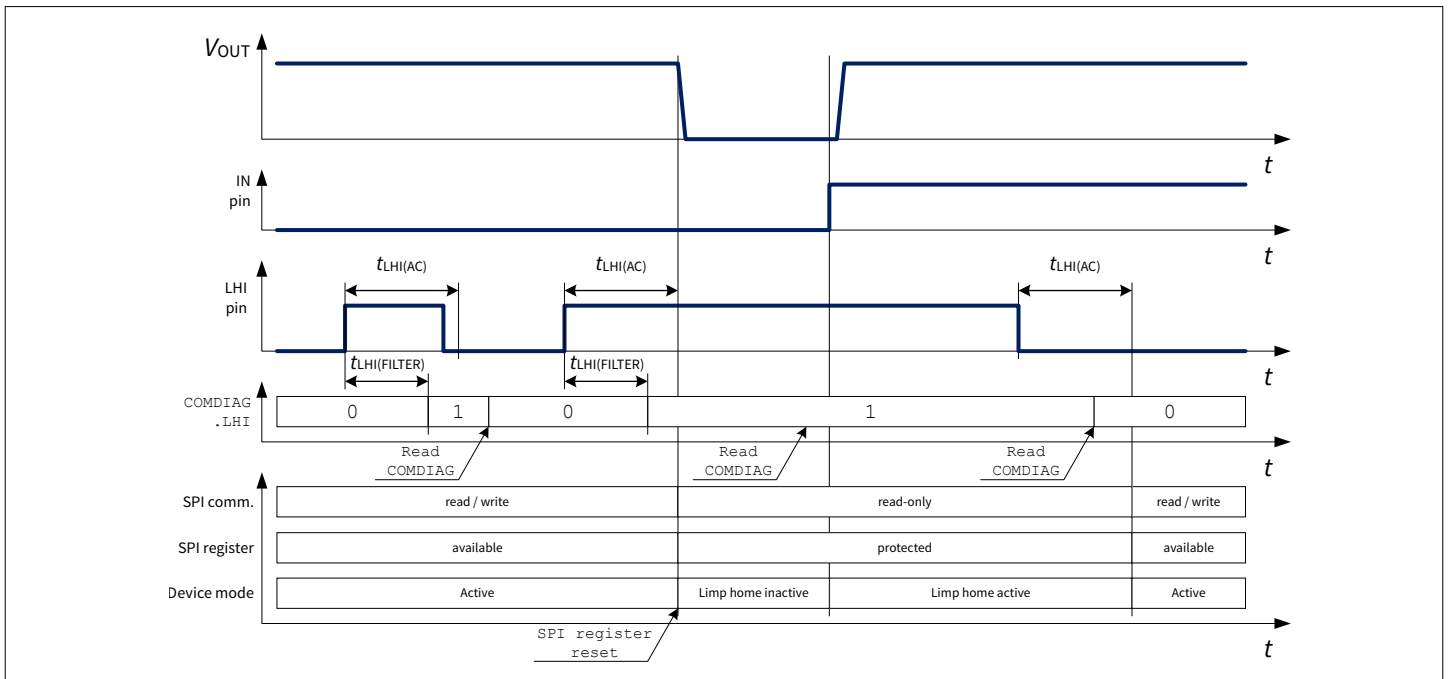


Figure 17 Limp home mode activation diagram

Depending on the IN pin, the device changes between two different limp home sub-modes:

- Limp home inactive: this sub-mode is entered when the power stage control = LOW
- Limp home active: this sub-mode is entered when the power stage control = HIGH
- Similarly to the active mode in normal operation, the limp home active mode also provides the CLS sub-mode. This can be enabled by changing the default value of the CLS bit accordingly via NVM programming, as described in [Chapter 12](#)

Once the LHI pin is released and LHI = LOW for a time longer than $t_{LHI(AC)}$, the limp home mode is left to one of the normal operation modes (inactive mode or active mode), depending on the IN pin. The transition to the normal operation mode is performed even when the mode selection is reset to its default value (mode selection = sleep mode).

As soon as the device is back to one of the normal operation modes, the sleep request is set and the transition to sleep is performed as soon as all sleep conditions are fulfilled, as described in [Chapter 6.1.1.3](#).

6.1.1.7 Fail safe mode

The device enters fail safe mode as soon as one of the following conditions is fulfilled:

- An overflow of the communication watchdog
- $V_{DD} \leq V_{DD(UV)}$ for a time longer than the fail safe mode filter time $t_{FILTER(FS)}$

The behavior of the power stage control in fail safe mode can be configured via the digital interface. This configuration updates also the output control bit when fail safe mode is entered, as described in the table below.

Table 7 Power stage control in fail safe mode

Power stage control in fail safe mode	Power stage control	Output control bit
00 _B	Power stage control = LOW	0 _B
01 _B	Power stage control = "last state"	0 _B if power stage was OFF 1 _B if power stage was ON
10 _B	Power stage control = "last state"	0 _B if power stage was OFF 1 _B if power stage was ON
11 _B	Power stage control = HIGH	1 _B

Besides the updated output control bit, the SPI registers stay unchanged and are available for read access only. The only accepted write command is the leave fail safe command.

Depending on the configuration bits for the power stage control in fail safe mode, the device changes between two different fail safe sub-modes:

- Fail safe.inactive: this sub-mode is entered when the power stage control is LOW, due to the configuration bits of the power stage control in fail safe mode.
- Fail safe.active: this sub-mode is entered when the power stage control is HIGH, due to the configuration bits of the power stage control in fail safe mode.
- Similarly to the active mode in normal operation, fail safe active mode also provides the CLS sub-mode. The enter and exit conditions are described in [Chapter 6.1.1.5](#).

To support a defined state of the power stage, the input control logic is set to "OR-combination", when the fail safe mode is entered.

To be robust against transient disturbances, the IN pin is ignored in fail safe mode.

The fail safe mode can be left to normal operation mode via the digital interface using the leave fail safe command or to limp home mode via the LHI pin.

When the fail safe mode is left to one of the normal operation modes, the latest state of the power stage control during fail safe mode is kept.

6.1.1.8 Idle mode

The idle mode is the low current consumption mode of the device. The current consumption is reduced to $I_{GND(IDLE)}$, while keeping the power stage active.

When the device is in active mode, the idle mode entry can be requested by setting the mode selection to "idle mode". After this request, the idle mode will be entered as soon as all the following entry conditions are fulfilled:

- Power stage control = HIGH
- Load current level is below $I_{L(IDLE_ENTRY)}$ and stays below $I_{L(IDLE_EXIT)}$
- The S_{I2t} is below the $I2t$ status based on $I_{L(I2t_I)}$
- No device protection or system protection has been triggered
- LHI pin is set to LOW
- $I_L > I_{L(INV_ON)}$
- $V_S < V_{S(OCT)}$

As long as the idle mode is requested, the IN pin is ignored and the power stage cannot be disabled via the power stage control signal. To reduce the current consumption to a minimum, the system protection and the diagnosis features are not available during idle mode.

The configuration registers are reset when idle mode is entered, with the exceptions of the power stage control signal, the idle mode request flag, and the OCT setting. The data relating to the exceptions is stored and is available, as soon as the device transitions from idle mode to active mode.

The device leaves idle mode either if one of the idle mode entry conditions is violated (except the condition $V_S < V_{S(OCT)}$) or if a mode transition is requested on the digital interface.

The mode transition can be requested with two dedicated commands. A rising edge on the CSN pin wakes up the device. After the $t_{WU(SPI)}$, a mode transition has to be requested within $t_{PU(HOLD)}$, by setting the mode selection to "normal operation modes". Once the mode transition has been requested, the device moves to active mode within t_{PU} . As the device configuration is not stored in idle mode, the configuration registers are set to default values. If needed they have to be re-configured as soon as the device is back in active mode.

The device indicates via the IRQ pin when it enters or exits the idle mode.

Once the idle mode is left, the power supply voltage has to stay above $V_{S(PU)}$ for at least t_{PU} . Otherwise, the power stage is switched OFF until the power-up is performed accordingly with $V_S > V_{S(PU)}$, which enables the digital measurements and their related system protection mechanisms.

6.1.1.9 NVM mode

To provide the configuration of the default values for the registers, the device offers the NVM mode. For more information on configurability, refer to [Chapter 12](#).

Entering NVM mode can be requested by sending the select NVM mode command via the digital interface while the device is in inactive mode. In any other operation mode, the transition to NVM mode is declined.

When the device is in NVM mode, the communication watchdog is paused.

Due to the current consumption required while the device is writing to the non-volatile memory, the overall operating current is optimized to $I_{GND(NVM)}$, by deactivating protection and diagnosis features as described in [Table 9](#) and [Table 8](#).

To support this, the power stage cannot be enabled within NVM mode.

NVM mode can be left after the NVM write process has finished, by requesting NVM leave via the digital interface. Once the leave command is requested, the complete NVM content is loaded to the dedicated register within t_{PU} and the NVM mode is left to one of the normal operation modes (inactive mode or active mode), depending on the power stage control signal.

When the LHI pin is set to HIGH for $t > t_{LHI(AC)}$, the NVM mode is left to limp home mode, once any ongoing write to NVM command is completed.

After the transition back to one of the normal operation modes, the configuration registers have to be re-configured if needed.

6.1.2 Transitions

To move from one operation mode to another, the following transitions can be performed in dependency on the described transition conditions:

Name	Start mode	End mode	Transition condition
PU_SLP	Power-up	Sleep	Automatic in case no communication via digital interface within $t_{PU(HOLD)}$
PU_LH	Power-up	Limp home	Default values loaded and LHI = HIGH for $t > t_{LHI(AC)}$
PU_INA	Power-up	Inactive	Default values loaded and mode selection = "normal mode"

Name	Start mode	End mode	Transition condition
SLP_PU	Sleep	Power-up	Rising edge on: CSN pin above $V_{CSN(TH)}$ or LHI pin above $V_{DI(TH)}$ or V_S above $V_{S(OP)}$
INA_SLP	Inactive	Sleep	Mode selection = "sleep mode" and all sleep entry conditions fulfilled
INA_ACT	Inactive	Active	Power stage control = HIGH
INA_LH	Inactive	Limp home	LHI = HIGH for $t > t_{LHI(AC)}$
INA_FS	Inactive	Fail safe	Watchdog overflow or $V_{DD} \leq V_{DD(UV)}$ for $t > t_{FILTER(FS)}$ with mode selection = "normal mode"
INA_NVM	Inactive	NVM	NVM mode selected
ACT_INA	Active	Inactive	Power stage control = LOW
ACT_IDL	Active	Idle	Mode selection = "idle mode" and idle entry conditions fulfilled
ACT_LH	Active	Limp home	LHI = HIGH for $t > t_{LHI(AC)}$
ACT_FS	Active	Fail safe	Watchdog overflow or $V_{DD} \leq V_{DD(UV)}$ for $t > t_{FILTER(FS)}$
LH_INA	Limp home	Inactive	LHI = LOW for $t > t_{LHI(AC)}$ with power stage control = LOW
LH_ACT	Limp home	Active	LHI = LOW for $t > t_{LHI(AC)}$ with power stage control = HIGH
FS_INA	Fail safe	Inactive	Valid leave fail safe command via digital interface with power stage control = LOW
FS_ACT	Fail safe	Active	Valid leave fail safe command via digital interface with power stage control = HIGH
FS_LH	Fail safe	Limp home	LHI = HIGH for $t > t_{LHI(AC)}$
IDL_ACT	Idle	Active	Idle entry condition violated
IDL_LH	Idle	Limp home	LHI = HIGH for $t > t_{LHI(AC)}$ and default values loaded
NVM_INA	NVM	Inactive	NVM mode selection released with power stage control = LOW



Name	Start mode	End mode	Transition condition
NVM_ACT	NVM	Active	NVM mode selection released with power stage control = HIGH
NVM_LH	NVM	Limp home	LHI = HIGH for $t > t_{LHI(AC)}$ and no read/write NVM ongoing

6.1.3 Availability of protection and diagnosis functions

The availability of protection mechanisms and diagnosis functions of the device depends on the operation mode in which the device is. A detailed overview is shown in the tables below.

Table 8 Mode vs. protection overview

Mode	Sub-mode	Overvoltage protection	Overcurrent protection	Overtemperature protection	VS undervoltage protection	VS undervoltage lockout	VS overvoltage lockout	I2t protection
Unsupplied	–	Available	Not available	Not available	Not available	Not available	Not available	Not available
Power-up	–	Available	Not available	Not available	Not available	Not available	Not available	Not available
Sleep	–	Available	Not available	Not available	Not available	Not available	Not available	Not available
Inactive	–	Available	Not available	Available	Available	Available*	Available*	Available*
Active	–	Available	Available	Available	Available	Available	Available	Available
	CLS	Available	Available	Available	Available	Available	Available	Available (with $I_{L(OCT)}$ as input)
Limp Home	Inactive	Available	Not available	Available	Available	Available*	Not available	Available*
	Active	Available	Available	Available	Available	Available	Not available	Available
Fail Safe	Inactive	Available	Not available	Available	Available	Available*	Available*	Available*
	Active	Available	Available	Available	Available	Available	Available	Available
Idle**	–	Available	Available	Not available	Available	Not available	Not available	Not available
NVM	–	Available	Not available	Available	Available	Not available	Not available	Not available

* Switch-ON is avoided

** Limited to self-protection as described in the idle mode chapter

Table 9 Mode vs. diagnosis overview

Mode	Sub-mode	Analog current sense	Digital current sense	V_{DS} measurement	V_S measurement	Temperature measurement	I2t status	Self check
Unsupplied	–	Not available	Not available	Not available	Not available	Not available	Not available	Not available

(table continues...)

Table 9 (continued) Mode vs. diagnosis overview

Mode	Sub-mode	Analog current sense	Digital current sense	V_{DS} measurement	V_S measurement	Temperature measurement	I2t status	Self check
Power-up	–	Not available	Not available	Not available	Not available	Not available	Not available	Not available
Sleep	–	Not available	Not available	Not available	Not available	Not available	Not available**	Not available
Inactive	–	Not available	Not available	Available	Available	Available	Available	Available
Active	–	Available (if current sense enabled)	Available	Available	Available	Available	Available	Available
	CLS	Not available	Not available	Available	Available	Available	Available (simulated with $I_{L(OCT)}$)	Not available
Limp Home	Inactive	Not available	Not available	Available*	Available*	Available*	Available*	Not available
	Active	According to default of analog current sense multiplexer	Available*	Available*	Available*	Available*	Available*	Not available
Fail Safe	Inactive	Not available	Not available	Available*	Available*	Available*	Available*	Not available
	Active	Available (if current sense enabled)	Available*	Available*	Available*	Available*	Available*	Not available
Idle	–	Not available	Not available	Not available	Not available	Not available	Not available**	Not available
NVM	–	Not available	Not available	Not available	Not available	Not available	Available	Not available

* If $V_{DD} \geq V_{DD(OP)}$ ** Low power modes will be entered when I2t status evaluation is below the I2t status based on $I_{L(I2t_I)}$

6.2 Undervoltage

To prevent the device from operating outside the functional range, both supply voltages (digital supply voltage and power supply voltage) have their own undervoltage detection circuit. If one of the supply voltages is below its undervoltage protection threshold, the associated functions are disabled.

In total, the device features 3 different undervoltage mechanisms:

- Power supply undervoltage shutdown

- Power supply undervoltage lockout
- Digital supply undervoltage shutdown

This chapter deals with the undervoltage shutdown mechanisms. The power supply undervoltage lockout is a system protection mechanism and is described in the dedicated chapter.

Depending on which supply voltage is in a state of undervoltage, the device supports different functionalities.

6.2.1 Undervoltage on VS

When the V_S voltage decreases below or becomes equal to $V_{S(UV)}$, the undervoltage shutdown mechanism is triggered. This mechanism switches OFF the power stage of the device, if it was previously switched ON.

As soon as the power supply voltage recovers, and the condition $V_S > V_{S(OP)}$ is fulfilled, the power stage is switched ON again (if power stage control = HIGH). According to the operation mode, the device protection and basic diagnosis functions are available. In contrast, the digital measurements and their related system protection functions are available once the voltage is above $V_{S(PU)}$ for at least $t_{VS(REC)}$.

Once the power supply undervoltage shutdown mechanism is triggered, it is indicated in the corresponding bit of the digital interface. This information is stored until readout by the microcontroller.

While the power supply undervoltage shutdown mechanism is active (with V_S constantly above 0 V) and $V_{DD} > V_{DD(OP)}$, the I2t status and the SPI register content remain available (read and write mode). Anyhow, the device protection mechanism and digital measurements are deactivated.

The power supply undervoltage shutdown threshold ($V_{S(UV)}$ and its corresponding $V_{S(OP)}$), can be set via the digital interface to one of two different values, either to $V_{S(UV)_L}$ or $V_{S(UV)_H}$.

6.2.2 Undervoltage on VDD

The undervoltage shutdown mechanism of the digital supply voltage is triggered when V_{DD} drops below or becomes equal to $V_{DD(UV)}$.

As soon as the digital supply undervoltage shutdown mechanism of the digital supply voltage is triggered, the communication via the digital interface is disabled and the fail safe mode filter timer starts ($t_{FILTER(FS)}$).

As soon as the digital supply voltage recovers, and the condition $V_{DD} > V_{DD(OP)}$ is fulfilled, the communication via the digital interface is enabled. The previous undervoltage event on the digital supply voltage is indicated in the corresponding bit of the digital interface. This information is stored until readout by the microcontroller.

For more information on the device behavior if $V_{DD} \leq V_{DD(UV)}$ for a time longer than the fail safe mode filter time ($t \geq t_{FILTER(FS)}$), refer to [Chapter 6.1.1.7](#).

Furthermore, the fail safe mode filter timer counts backwards with a quarter of the speed, when V_{DD} recovers above $V_{DD(OP)}$.

Consequently, if there is another undervoltage event on V_{DD} , the fail safe mode filter timer continues and the time cumulates until $t_{FILTER(FS)}$ is exceeded, as shown in [Figure 18](#).

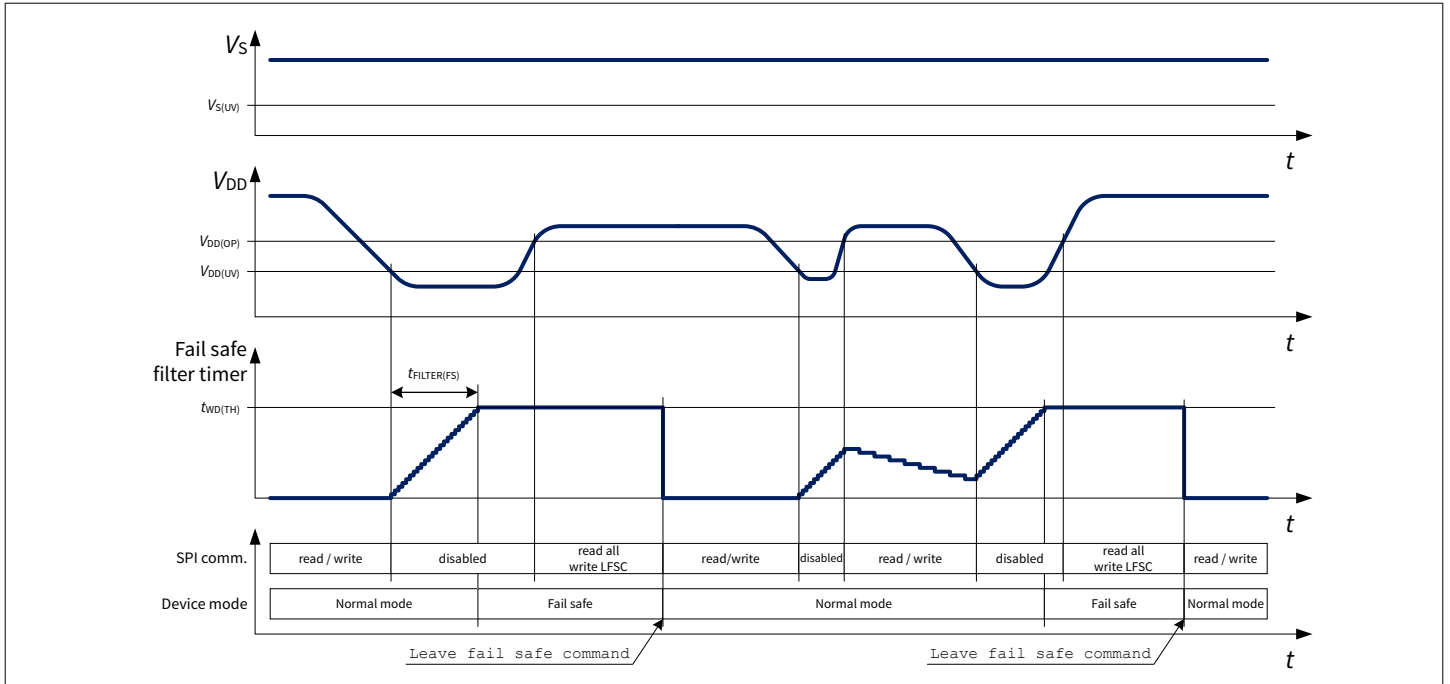


Figure 18 Undervoltage on VDD - fail safe filter timer

6.2.3 Undervoltage on VS and VDD

When both supply voltages drop below their corresponding undervoltage shutdown thresholds ($V_{S(UV)}$ and $V_{DD(UV)}$), the following information is retained for at least t_{RET} (all other information is lost):

- I2t status
- OCT configuration
- Fault flag
- Mode selection
- Output control bit

To ensure that the information is retained for t_{RET} , the power supply voltage has to be above its minimum operating voltage $V_{S(OP)}$ for a time longer than $t_{RET(REC)}$, before the undervoltage event.

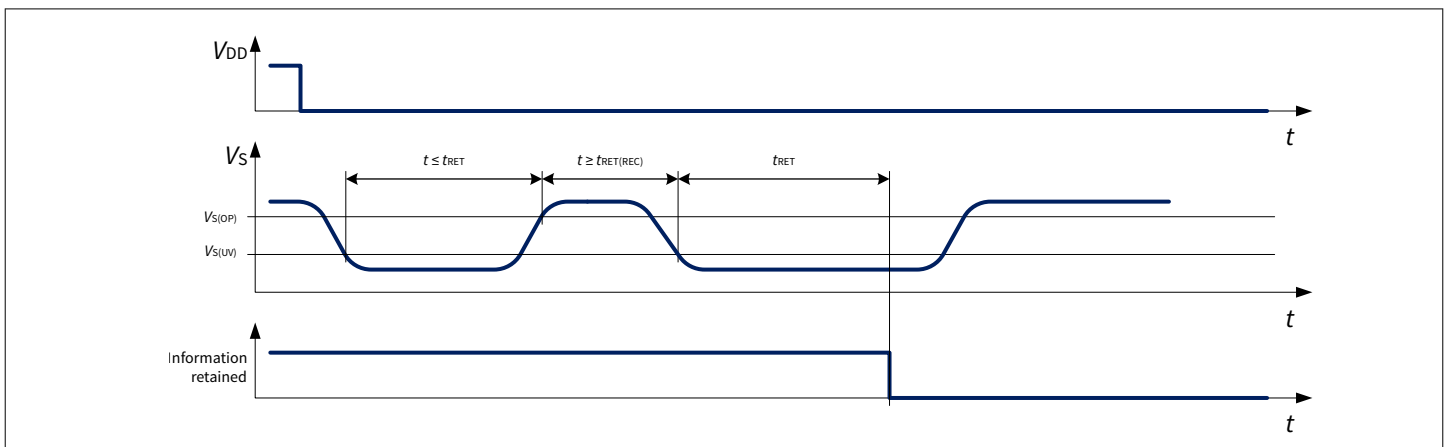


Figure 19 Undervoltage retention time

If V_S recovers above $V_{S(OP)}$ within t_{RET} the power stage control follows the retained power stage status in OR-combination with the IN pin. When $V_S > V_{S(PU)}$, the default values are loaded to the device configuration within t_{PU} . Once the default values are loaded, the functions are available as described in [Chapter 6.1.3](#).

If during the power-up phase, after an undervoltage event where V_{DD} is still in undervoltage condition, the power supply voltage drops again below $V_{S(PU)}$, the power stage is deactivated until the power-up is performed accordingly with $V_S > V_{S(PU)}$.

6.3 Electrical characteristics - power management

Table 10 Electrical characteristics - power management

$V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$

Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltages							
Power supply undervoltage shutdown low	$V_{S(UV)_L}$	2.1	2.4	2.8	V	V_S decreasing, cold cranking enabled	PRQ-562
Power supply undervoltage shutdown high	$V_{S(UV)_H}$	2.6	2.9	3.2	V	V_S decreasing, cold cranking disabled	PRQ-1366
Power supply minimum operating voltage	$V_{S(OP)}$	2.7	3.0	3.3	V	V_S increasing	PRQ-564
Power supply minimum power-up voltage	$V_{S(PU)}$	–	–	4.1	V	V_S increasing	PRQ-1367
Breakdown voltage between GND and VS pins in reverse battery	$V_{S(REV)}$	-30	–	-18	V	–	PRQ-1378
Digital supply undervoltage shutdown	$V_{DD(UV)}$	1.8	2.1	2.4	V	V_{DD} decreasing	PRQ-568
Digital supply minimum operating voltage	$V_{DD(OP)}$	1.9	2.4	2.9	V	V_{DD} increasing	PRQ-569
Digital supply clamping voltage	$V_{DD(CLAMP)}$	12	14	16	V	$I_{VDD} = 5\text{ mA}$	PRQ-1379

Current consumptions

Power supply current consumption in sleep mode with load at $T_J \leq 85^\circ\text{C}$	$I_{VS(SLEEP)_85}$	–	–	2	μA	Device in sleep mode, $T_J \leq 85^\circ\text{C}$	PRQ-573
Power supply current consumption in sleep mode with load at $T_J = 150^\circ\text{C}$	$I_{VS(SLEEP)_150}$	–	10	35	μA	Device in sleep mode, $T_J = 150^\circ\text{C}$	PRQ-574
Digital supply current consumption in sleep mode	$I_{VDD(SLEEP)}$	–	15	32	μA	Device in sleep mode, $f_{SCLK} = 0 \text{ MHz}$, $V_{CSN} = V_{DD} > V_{DD(OP)}$	PRQ-580

(table continues...)

Table 10 (continued) Electrical characteristics - power management $V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$ Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Digital supply current consumption in normal operation (average)	$I_{VDD(NORMAL)}$	–	–	2.6	mA	Device in normal operation mode, $f_{SCLK} = 5 \text{ MHz}$, $C_{L(SO)} = 50 \text{ pF}$	PRQ-1380
Operating current in active mode (all power stages on)	$I_{GND(ACTIVE)}$	–	7.2	10	mA	Device in active mode, current sense enabled	PRQ-1369
Operating current in inactive mode	$I_{GND(INACTIVE)}$	–	5.5	7	mA	Device in inactive mode	PRQ-1381
Operating current in idle mode (average)	$I_{GND(IDLE)}$	–	60	70	μA	Device in idle mode, $V_{CSN} = V_{DD}$, $V_{SCLK} = V_{SI} = V_{IN} = 0 \text{ V}$, $T_J \leq 85^\circ\text{C}$	PRQ-575
Operating current in idle mode (average)	$I_{GND(IDLE)}$	–	42	50	μA	Device in idle mode, $V_{CSN} = V_{DD} = 0 \text{ V}$, $V_{SCLK} = V_{SI} = V_{IN} = 0 \text{ V}$, $T_J \leq 85^\circ\text{C}$	PRQ-1483
Operating current in NVM mode	$I_{GND(NVM)}$	–	12	15.2	mA	Device in NVM mode	PRQ-789

Timings

Digital interface wake-up time	$t_{WU(SPI)}$	–	70	100	μs	–	PRQ-600
Power-up time	t_{PU}	–	–	900	μs	–	PRQ-749
Power-up hold time	$t_{PU(HOLD)}$	25	–	38	ms	–	PRQ-750
Recovery time after VS undervoltage	$t_{VS(REC)}$	–	–	80	μs	V_S increasing, $V_S > V_{S(PU)}$	PRQ-1495
Data retention time	t_{RET}	100	–	–	μs	V_S decreasing $0 < V_S \leq V_{S(UV)}$ and V_{DD} decreasing $V_{DD} \leq V_{DD(UV)}$	PRQ-572
Data retention recovery time	$t_{RET(REC)}$	–	–	90	μs	$V_S > V_{S(OP)}$	PRQ-727
Limp home mode acknowledgement time	$t_{LHI(AC)}$	20	30	40	μs	–	PRQ-571
LHI diagnosis filter time	$t_{FILTER(LHI)}$	–	–	13	μs	–	PRQ-1492
Fail safe mode filter time	$t_{FILTER(FS)}$	100	115	130	ms	–	PRQ-617
Transition time inactive to active	$t_{TR(INA_ACT)}$	–	–	10	μs	–	PRQ-1375

(table continues...)

Table 10 (continued) Electrical characteristics - power management $V_S = V_{S(NOR)}, T_J = T_{J(NOR)}$ Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}, T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Transition time inactive to NVM	$t_{TR(INA_NVM)}$	–	–	30	μs	–	PRQ-802
Transition time active to inactive	$t_{TR(ACT_INA)}$	–	–	$t_{OFF,MAX}$	μs	–	PRQ-1372
Transition time active to idle	$t_{TR(ACT_IDL)}$	–	–	300	μs	–	PRQ-1371
Transition time idle to active	$t_{TR(IDL_ACT)}$	–	–	$t_{PU,MAX}$	μs	–	PRQ-801
Transition time idle to protection ready	$t_{TR(IDL_PROT)}$	–	–	28	μs	–	PRQ-1778
Transition time fail safe to inactive	$t_{TR(FS_INA)}$	–	–	5	μs	–	PRQ-1374
Transition time fail safe to active	$t_{TR(FS_ACT)}$	–	–	5	μs	–	PRQ-1373
Transition time limp home to inactive	$t_{TR(LH_INA)}$	–	–	50	μs	–	PRQ-1377
Transition time limp home to active	$t_{TR(LH_ACT)}$	–	–	50	μs	–	PRQ-1376

Idle mode condition

Load current for idle mode entry	$I_{L(IDLE_ENTRY)}$	0.4	1.8	2.7	A	–	PRQ-577
Load current for idle mode exit	$I_{L(IDLE_EXIT)}$	0.9	2.2	3.6	A	–	PRQ-668

7 Power stage

The high-side power stage is built using an N-channel vertical power MOSFET with a charge pump, controlled via the power stage control.

7.1 Power stage control

The power stage control signal enables or disables the corresponding power stage and is sensitive to three input parameters:

- IN status
- Output control bit
- Input control logic

There are three ways of using the input status in combination with the output control bit, by programming the input control logic via the digital interface. This results in the power stage control matrix. The table below defines the configuration of the power stage control matrix, while the figure below shows a simplified block diagram.

The default mode of the combinatorial input control logic is the OR-combination of the input status and the output control bit.

Table 11 Power stage control matrix

IN status	output control bit	Power stage control related to the input control logic		
		input control logic = 00 _B	input control logic = 01 _B	input control logic = 10 _B
0	0	LOW	LOW	LOW
0	1	HIGH	LOW	HIGH
1	0	HIGH	LOW	LOW
1	1	HIGH	HIGH	HIGH

Note: Input control logic = 11_B is not available

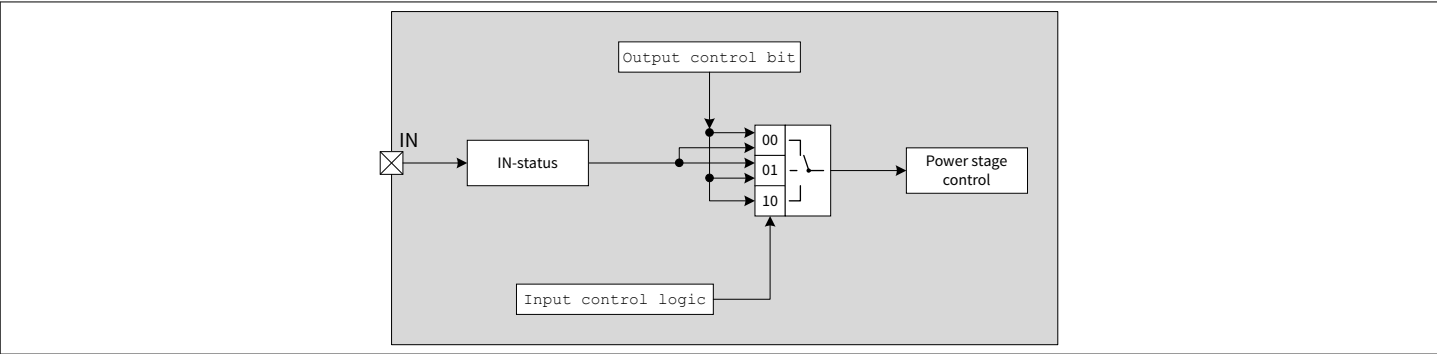


Figure 20 Power stage control switch matrix

7.2 Power stage ON-state resistance

The ON-state resistance $R_{DS(ON)}$ depends mainly on junction temperature T_J . Figure 21 shows the variation of $R_{DS(ON)}$ across the whole T_J range. The value “2” on the y-axis corresponds to the maximum $R_{DS(ON)}$ measured at $T_J = 150^{\circ}\text{C}$.

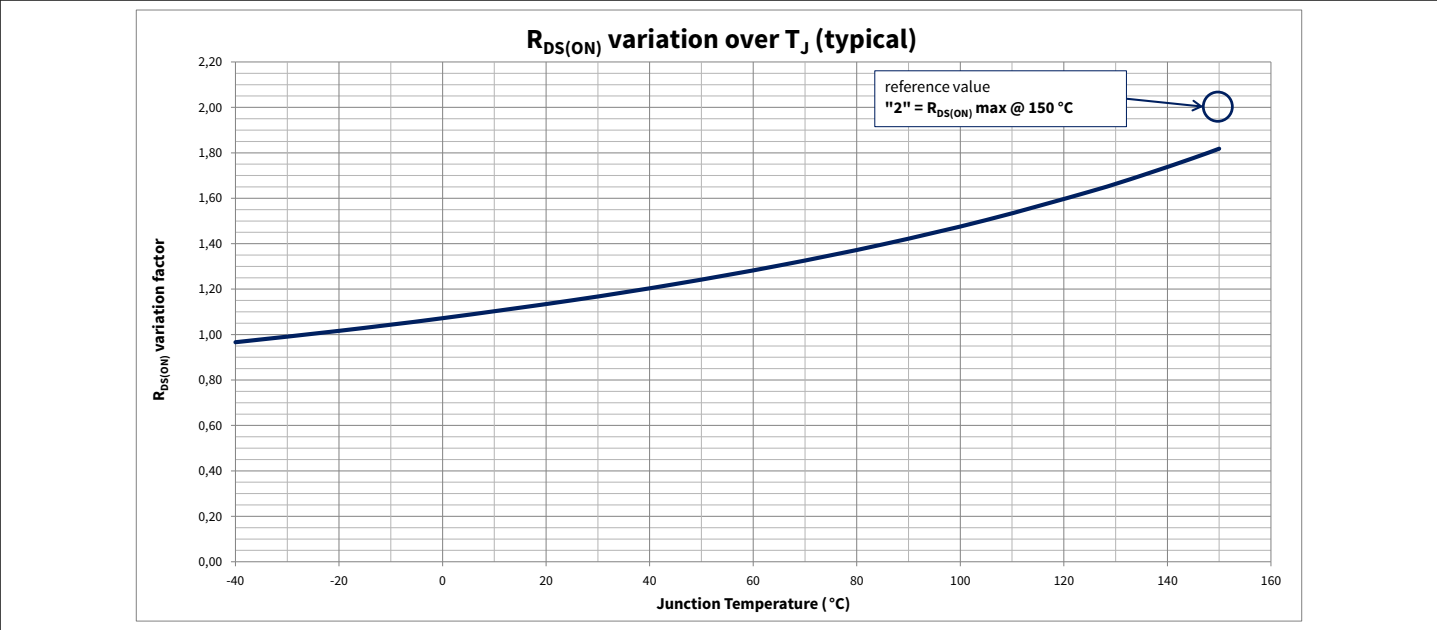


Figure 21 $R_{DS(ON)}$ variation factor

The behavior in reverse battery condition is described in [Chapter 8.5.1](#).

7.3 Switching loads

7.3.1 Switching resistive loads

When switching resistive loads, the switching times and slew rates defined in [Table 12](#) and shown in [Figure 22](#) have to be considered. The switching energy values E_{ON} and E_{OFF} are proportional to load resistance and switching times t_{ON} and t_{OFF} .

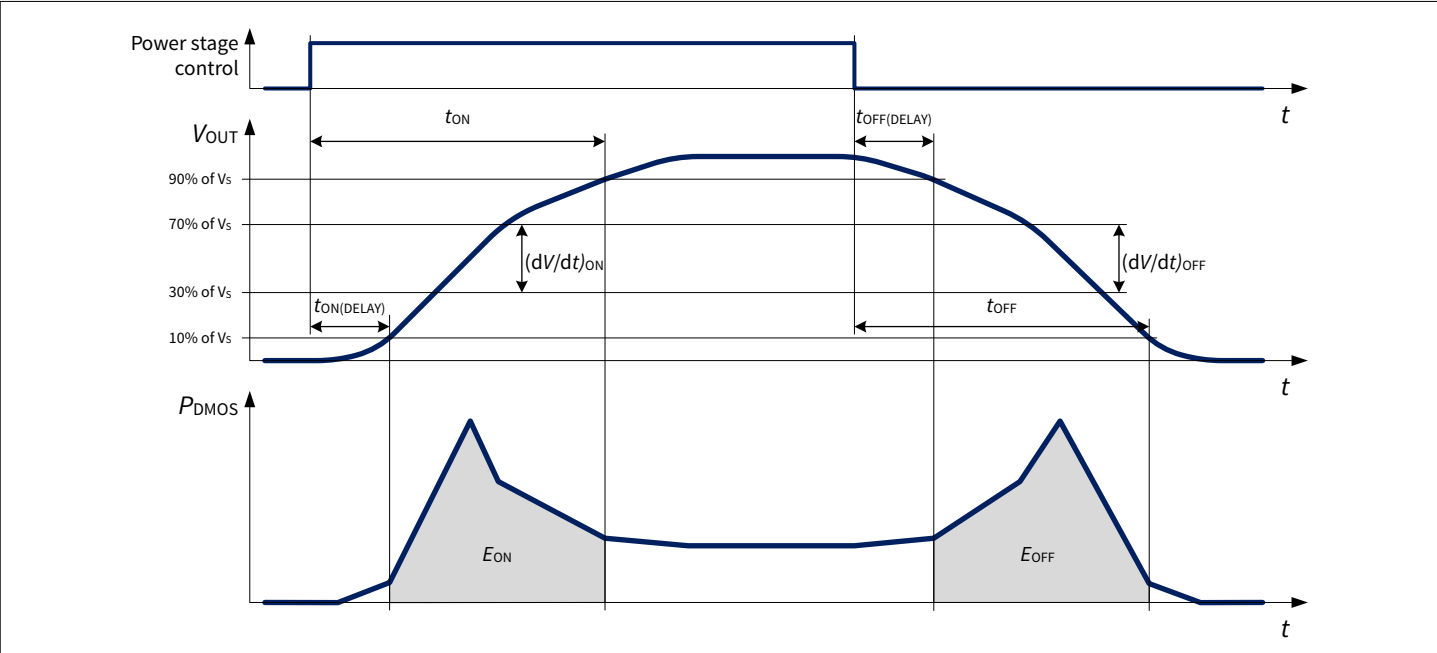


Figure 22 Switching a resistive load

7.3.2 Switching inductive loads

When switching OFF inductive loads with high-side switches, the voltage V_{OUT} drops below the ground potential, as a consequence of the fact that the inductance continues driving the load current.

To prevent the destruction of the device due to overvoltage, a voltage clamping mechanism between the VS pin and the OUT pin is implemented. The clamping structure limits the negative output voltage so that $V_{DS} = V_{DS(CLAMP)}$.

Figure 23 shows a concept drawing of the implementation. The clamping structure is available in all operation modes listed in Chapter 6.1.

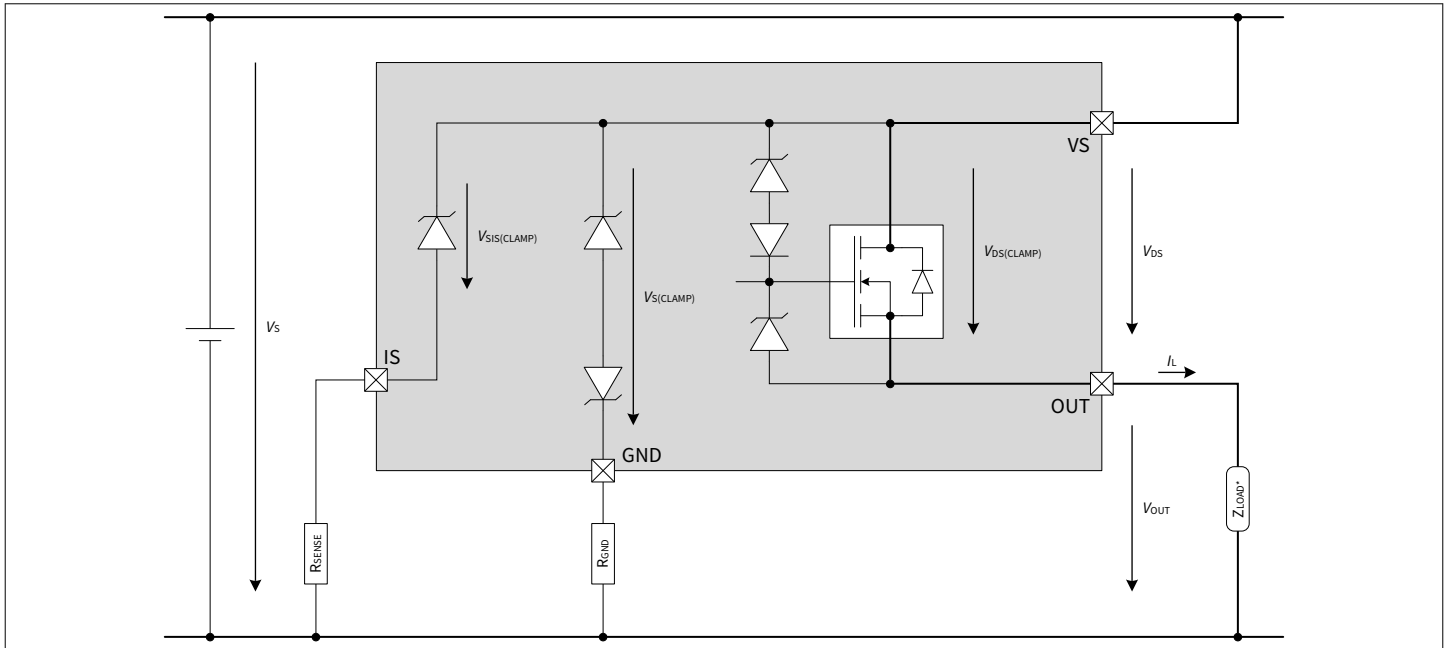


Figure 23 Output clamping concept

The energy resulting from the demagnetization of inductive loads, has to be dissipated in the power stage of the device. The energy can be calculated with:

$$E = V_{DS(CLAMP)} \times \left[\frac{V_S - V_{DS(CLAMP)}}{R_L} \times \ln \left(1 - \frac{R_L \times I_L}{V_S - V_{DS(CLAMP)}} \right) + I_L \right] \times \frac{L}{R_L} \quad (1)$$

The maximum energy, therefore the maximum inductance for a given current, is limited by the thermal design of the component. Please refer to the maximum allowed values of E_{AS} (single pulse energy) and E_{AR} (repetitive energy).

7.3.3 Switching capacitive loads

When switching capacitive loads, the load current increases due to the inrush behavior of the load. Due to the high load current and V_{DS} , the power dissipation is increased during the charging phase of the capacitor. Therefore, the load driving capability is energy limited. To enable higher load driving capability the device incorporates a sub-mode called CLS mode.

When switching a resistive load in the CLS mode, the switching times and the slew rate will change to t_{ON_CLS} , $t_{ON(Delay)_CLS}$ and $(dV/dt)_{ON_CLS}$ as shown in the figure below.

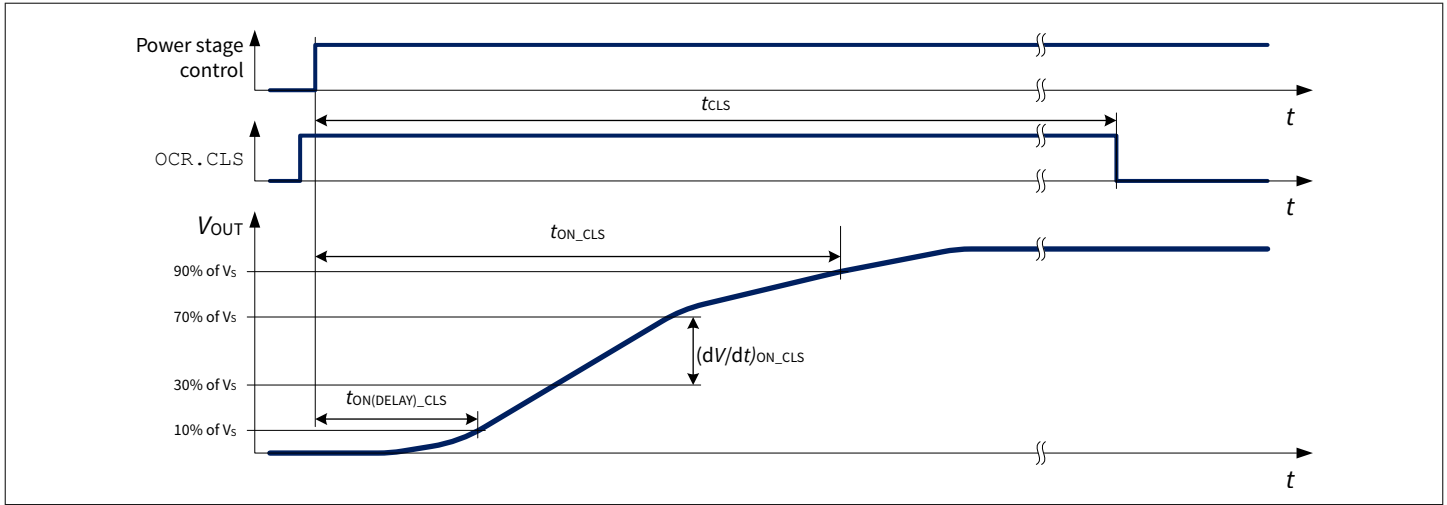


Figure 24 **Capacitive load switching times**

After a maximum time of t_{CLS} , the user has to disable CLS mode on the digital interface.

Before changing from active.CLS mode to active mode, it has to be ensured that there is no short circuit at the output. To distinguish between short circuit and normal load, the $R_{DS(ON)}$ acknowledgment status reporting can be used. If the $R_{DS(ON)}$ acknowledgment status reporting is true, the transition from active.CLS mode to active mode is possible. If $R_{DS(ON)}$ acknowledgment status reporting is false, it has to be assumed that there is either an uncharged capacitor, or a short circuit at the output. So, the transition from CLS mode to inactive mode has to be requested by setting the power stage control signal to LOW. Additionally, a short circuit condition can be excluded by an external voltage measurement at the output.

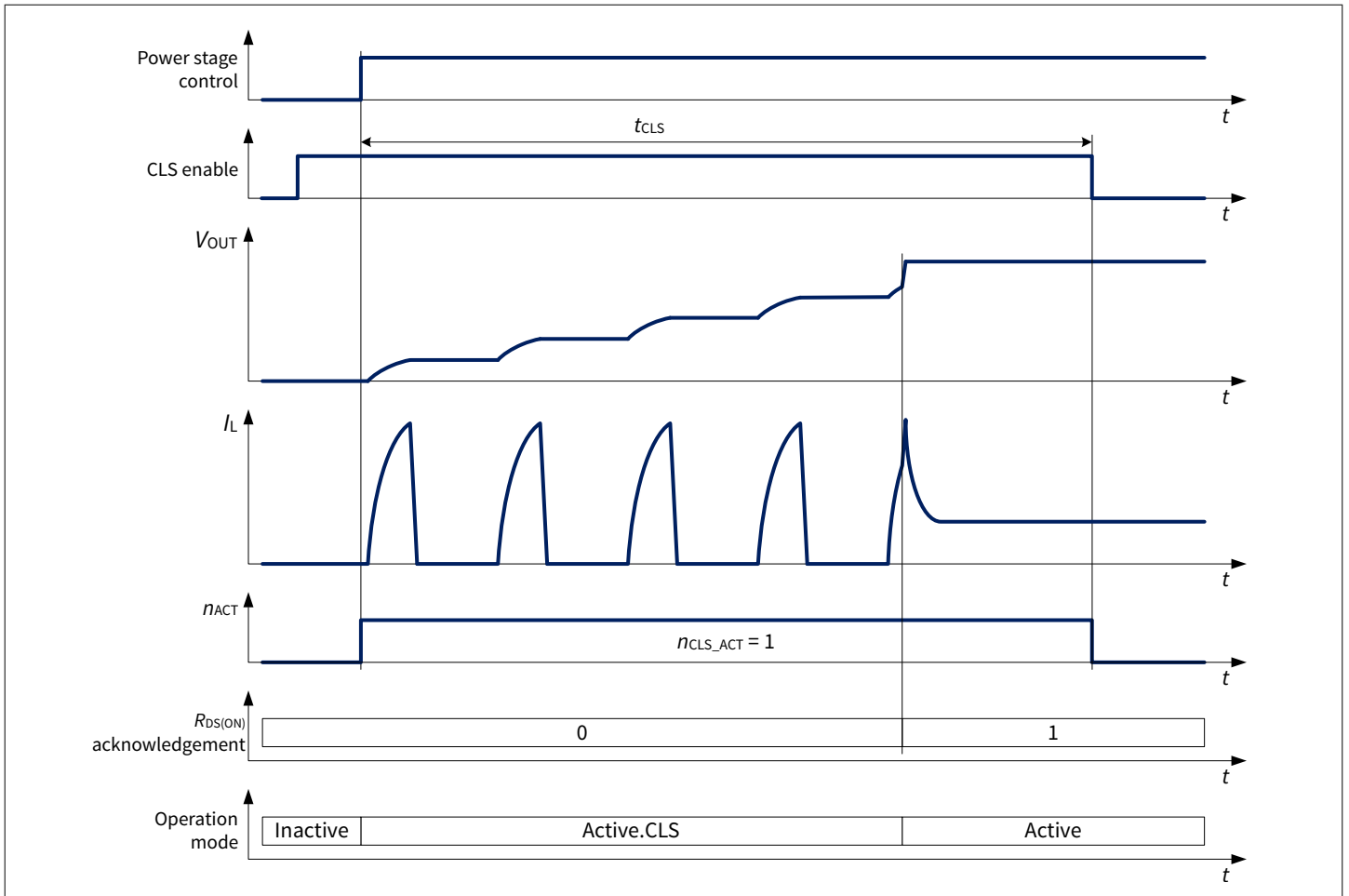


Figure 25 Capacitive load switching activations

7.4 Advanced switching characteristics

7.4.1 Inverse current behavior

When $V_{OUT} > V_S$ ($V_{DS} < 0$ V), a current I_{INV} flows from the OUT pin into the power stage (see Figure 26). This condition is known as “inverse current”.

If the power stage is OFF, the inverse current flows through the intrinsic body diode, which generates a high-power dissipation and results in an increase of the device temperature.

If the power stage is switched ON during inverse current, the power dissipation is comparable to the one during normal operation, as the ON-state resistance is given by $R_{DS(INV)}$.

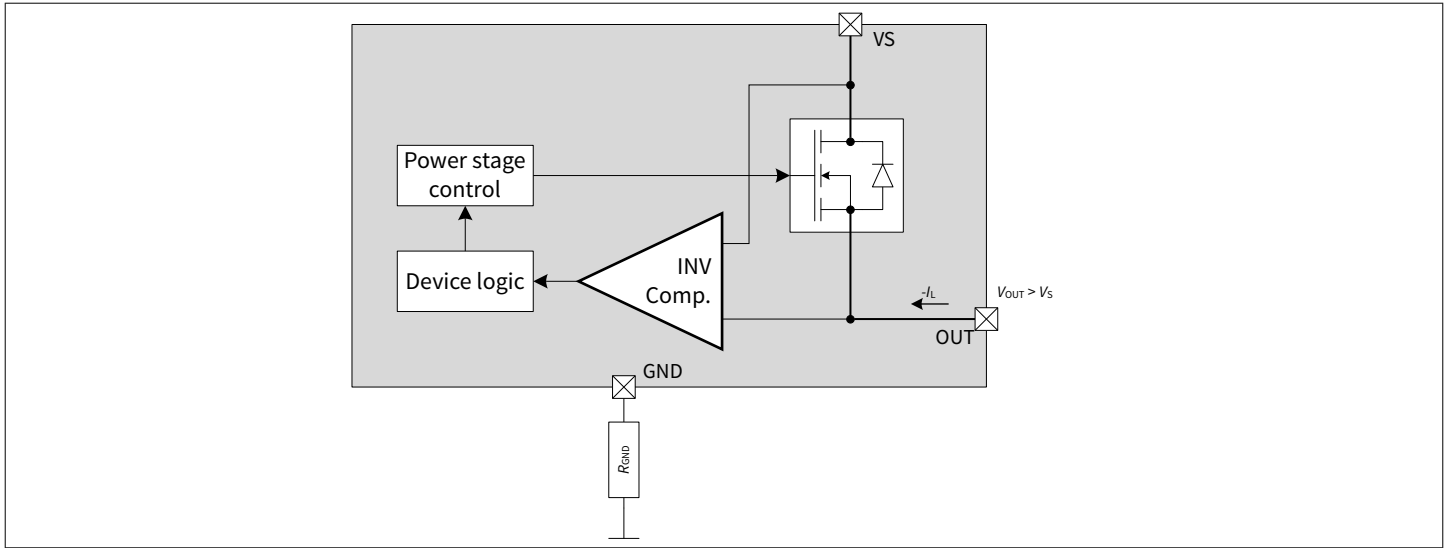


Figure 26 Inverse current circuitry

The inverse ON feature enables the switching of the power stage during inverse current as long as $|I_L| < |I_{L(INV)}|$ (see Figure 27).

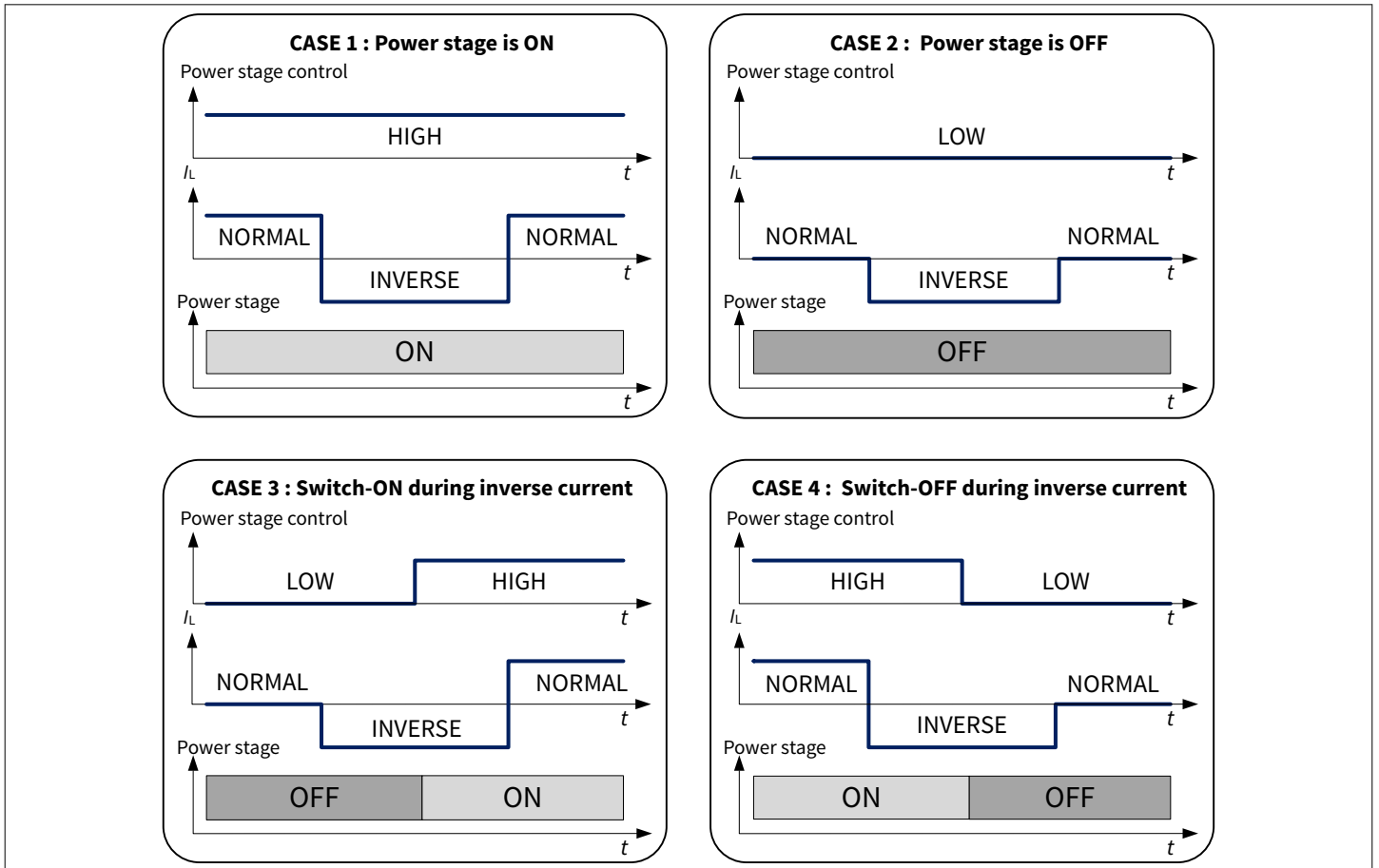


Figure 27 Inverse ON - channel behavior in the case of applied inverse current

The device indicates the inverse current condition via the digital interface as described in Chapter 10.3.3 and Chapter 10.3.6. During an inverse current condition, no system or device protection mechanisms are active. However, a fulfillment of a protection mechanism condition is reported via the digital interface. The dedicated protection mechanism gets active when the inverse condition is released and its condition is still fulfilled.

7.4.2 Cross Current robustness with H-Bridge configuration

When the device is used as high-side switch e.g. in a bridge configuration (therefore paired with a low-side switch as shown in Figure 28), the maximum slew rate applied to the output by the low-side switch has to be lower than $|dV_{OUT}/dt|$.

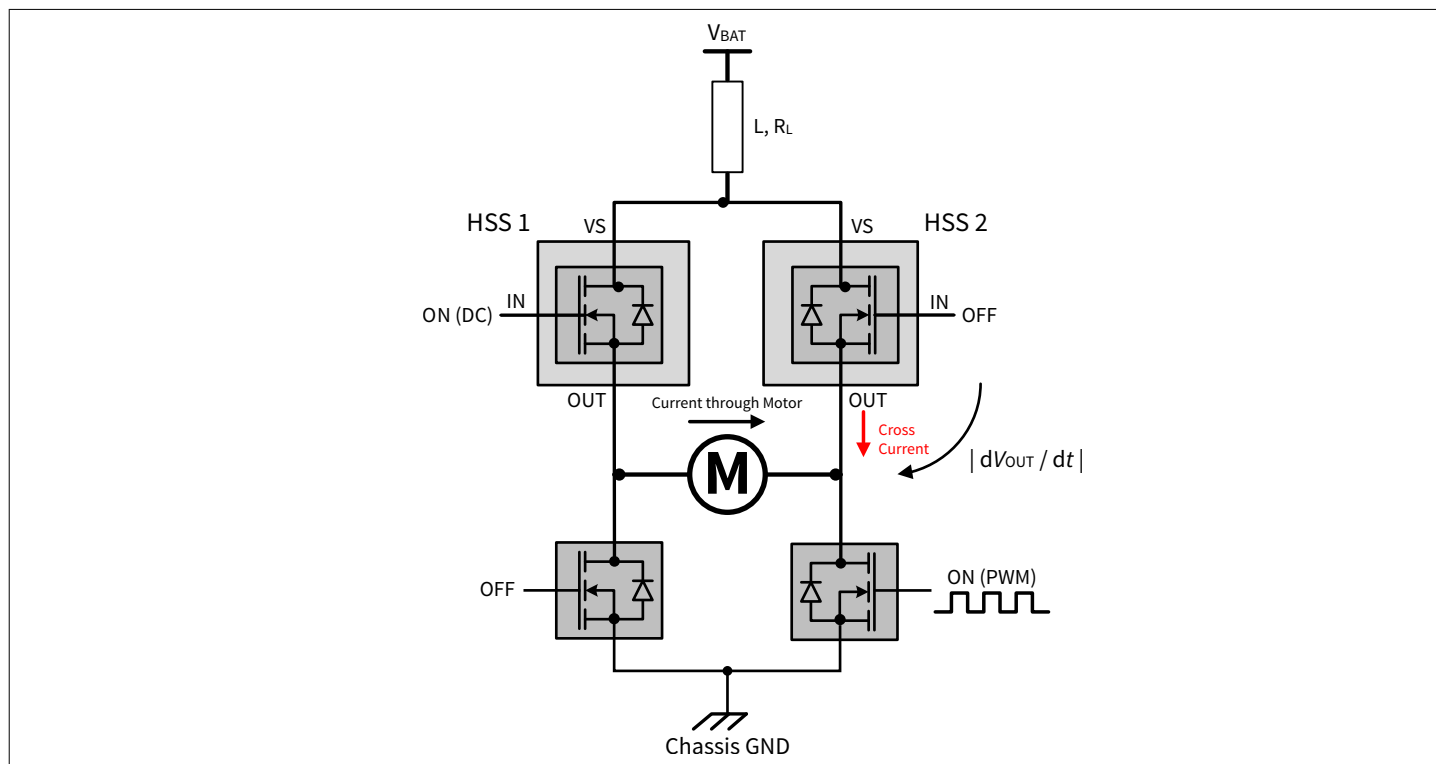


Figure 28 High-side switch used in bridge configuration

7.5 Electrical characteristics - power stage

Table 12 Electrical characteristics - power stage

$V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$

Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Drain to source clamping voltage at $T_J = -40^\circ\text{C}$	$V_{DS(CLAMP)}_{-40}$	33	35.5	39.5	V	$T_J = -40^\circ\text{C}$	PRQ-653
Drain to source clamping voltage at $T_J \geq 25^\circ\text{C}$	$V_{DS(CLAMP)}_{25}$	35	37.5	42	V	$T_J \geq 25^\circ\text{C}$ ¹⁾	PRQ-515
Drain source diode voltage	$ V_{DS(DIODE)} $	–	550	770	mV	$T_J = 150^\circ\text{C}$, $-I_{L(NOM)}_{85} \leq I_L < 0\text{ A}$	PRQ-676

(table continues...)

Table 12 (continued) Electrical characteristics - power stage $V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$ Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Passive slew rate (e.g. for Half Bridge Configuration)	$ dV_{OUT}/dt $	–	–	10	V/ μ s	$V_S = 13.5$ V	PRQ-518
Switching characteristics							
Load resistance for parameter specification	$R_{L(SP)}$	–	2	–	Ω	–	PRQ-1497
Switch-ON delay	$t_{ON(DELAY)}$	15	40	65	μ s	$V_S = V_{S(NOR),TYP}$, $R_L = R_{L(SP)}$, from power stage control = HIGH to $V_{OUT} = 10\% V_S$	PRQ-654
Switch-OFF delay	$t_{OFF(DELAY)}$	15	55	95	μ s	$V_S = V_{S(NOR),TYP}$, $R_L = R_{L(SP)}$, from power stage control = LOW to $V_{OUT} = 90\% V_S$	PRQ-655
Switch-ON time	t_{ON}	30	110	180	μ s	$V_S = V_{S(NOR),TYP}$, $R_L = R_{L(SP)}$, from power stage control = HIGH to $V_{OUT} = 90\% V_S$	PRQ-656
Switch-OFF time	t_{OFF}	30	110	180	μ s	$V_S = V_{S(NOR),TYP}$, $R_L = R_{L(SP)}$, from power stage control = LOW to $V_{OUT} = 10\% V_S$	PRQ-657
Switch-OFF time fast	$t_{OFF(FAST)}$	–	25	50	μ s	$V_S = V_{S(NOR),TYP}$, $R_L = R_{L(SP)}$, $V_{OUT} < V_S$, from (fault detected or fast OFF commanded) to $V_{OUT} = 10\% V_S$	PRQ-635
Switch-ON/OFF matching ($t_{ON} - t_{OFF}$)	Δt_{SW}	–	0	–	μ s	–	PRQ-1382
Switch-ON slew rate	$(dV/dt)_{ON}$	0.13	0.27	0.41	V/ μ s	$V_S = V_{S(NOR),TYP}$, $R_L = R_{L(SP)}$, from $V_{OUT} = 30\% V_S$ to $V_{OUT} = 70\% V_S$, setup acc. to AEC-Q100-012 (2006)	PRQ-658
Switch-OFF slew rate	$(dV/dt)_{OFF}$	-0.41	-0.27	-0.13	V/ μ s	$V_S = V_{S(NOR),TYP}$, $R_L = R_{L(SP)}$, from $V_{OUT} = 70\% V_S$ to $V_{OUT} = 30\% V_S$, setup acc. to AEC-Q100-012 (2006)	PRQ-659
Slew rate matching (dV/dt) _{ON} - (dV/dt) _{OFF}	$\Delta(dV/dt)_{SW}$	–	0	–	V/ μ s	$V_S = 13.5$ V, setup acc. to AEC-Q100-012 (2006)	PRQ-1383
Switch-ON energy	E_{ON}	–	4	–	mJ	$V_S = V_{S(NOR),MAX}$	PRQ-1419
Switch-OFF energy	E_{OFF}	–	4.6	–	mJ	$V_S = V_{S(NOR),MAX}$	PRQ-1420

(table continues...)

Table 12 (continued) Electrical characteristics - power stage
 $V_S = V_{S(NOR)}, T_J = T_{J(NOR)}$

 Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}, T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
CLS							
Switch-ON delay in CLS mode	$t_{ON(DELAY)_CLS}$	–	220	–	μs	CLS enabled, from power stage control = HIGH to $V_{OUT} = 10\% V_S$ with resistive load	PRQ-660
Switch-ON time in CLS state	t_{ON_CLS}	–	450	–	μs	CLS enabled, from power stage control = HIGH to $V_{OUT} = 90\% V_S$, with resistive load	PRQ-1421
Switch-ON slew rate in CLS state	$(dV/dt)_{ON_CLS}$	–	0.034	–	V/ μs	$V_S = 13.5\text{ V}$; CLS enabled, from $V_{OUT} = 30\% V_S$ to $V_{OUT} = 70\% V_S$, with resistive load, setup acc. to AEC-Q100-012	PRQ-1422
Maximum time in CLS mode	t_{CLS}	–	–	100	ms	$V_S = 16\text{ V}$, $T_{J(0)} = 85^\circ\text{C}$, setup acc. to AEC-Q100-012 (2006)	PRQ-513
Maximum number of CLS mode activations	n_{CLS_ACT}	–	–	50	kcycles	$t \leq t_{CLS}$, $V_S = 16\text{ V}$, $T_{J(0)} = 85^\circ\text{C}$, setup acc. to AEC-Q100-012 (2006)	PRQ-514

Power stage characteristics

ON-state resistance at $T_J = 25^\circ C$	$R_{DS(ON)_25}$	–	1.1	–	m Ω	$T_J = 25^\circ C$	PRQ-661
ON-state resistance at $T_J = 150^\circ C$	$R_{DS(ON)_150}$	–	–	1.85	m Ω	$T_J = 150^\circ C$	PRQ-662
ON-state resistance in cranking at $T_J = 150^\circ C$	$R_{DS(ON)_CRANK_150}$	–	–	2.3	m Ω	$V_S = V_{S(UV_L),MAX}, T_J = 150^\circ C$	PRQ-663
ON-state resistance in idle mode at $T_J = 150^\circ C$	$R_{DS(ON)_IDLE_150}$	–	1.8	2.1	m Ω	$T_J = 150^\circ C$	PRQ-669
ON-state resistance in inverse current at $T_J = 25^\circ C$	$R_{DS(INV)_25}$	–	1.1	–	m Ω	$T_J = 25^\circ C$	PRQ-670
ON-state resistance in inverse current at $T_J = 150^\circ C$	$R_{DS(INV)_150}$	–	–	1.85	m Ω	$T_J = 150^\circ C$	PRQ-671
ON-state resistance in reverse polarity at $T_J = 25^\circ C$	$R_{DS(REV)_25}$	–	2.2	–	m Ω	$V_{BAT(REV)} \leq V_S \leq -8 V, T_J = 25^\circ C$	PRQ-672

(table continues...)

Table 12 (continued) Electrical characteristics - power stage $V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$ Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ON-state resistance in reverse polarity at $T_J = 150^\circ\text{C}$	$R_{DS(REV)_150}$	–	–	3.7	m Ω	$V_{BAT(REV)} \leq V_S \leq -8\text{ V}$, $T_J = 150^\circ\text{C}$	PRQ-673
Nominal load current ($T_A = 85^\circ\text{C}$)	$I_{L(NOM)_85}$	–	34.5	–	A	$T_A = 85^\circ\text{C}$, $T_J \leq 150^\circ\text{C}$	PRQ-516
Output leakage current at $T_J \leq 85^\circ\text{C}$	$I_{L(OFF)_85}$	–	0.6	2.5	μA	Power stage control = LOW, $V_{OUT} = 0\text{ V}$, $T_J \leq 85^\circ\text{C}$	PRQ-674
Output leakage current at $T_J = 150^\circ\text{C}$	$I_{L(OFF)_150}$	–	–	62	μA	Power stage control = LOW, $V_{OUT} = 0\text{ V}$, $T_J = 150^\circ\text{C}$	PRQ-675
Inverse current capability	$I_{L(INV)}$	–	$-I_{L(NOM)_85}$	–	A	Power stage control = HIGH, $V_S < V_{OUT}$	PRQ-517

1) Tested at $T_J = 150^\circ\text{C}$.

8 Device protections

The device is protected against overtemperature, overcurrent, reverse battery (with Reverse ON), and overvoltage. The availability of the protection functions depends on the operation mode, as described in the power management chapter.

The overtemperature and overcurrent protections are not active during inverse current condition or in reverse battery condition.

The indication of an overtemperature event operates even during inverse current condition.

8.1 Overtemperature protection

To avoid thermal overstress in the power stage, the device incorporates both an absolute ($T_{J(ABS)}$) and a dynamic ($T_{J(DYN)}$) temperature protection circuitry.

An increase of junction temperature T_J above one of the two thresholds ($T_{J(ABS)}$ or $T_{J(DYN)}$) switches OFF the overheated power stage.

To prevent destruction, the power stage, where the overtemperature is detected, switches OFF within $t_{OFF(FAST)}$. The power stage remains switched OFF until the junction temperature T_J fulfills the reactivation condition. Besides this, the restart strategy has to be considered as described in [Chapter 8.3](#).

Table 13 Device protection reactivation conditions

Fault condition	Switch-OFF event	Reactivation condition
Overtemperature	$T_J \geq T_{J(ABS)}$ or $(T_J - T_{J(REF)}) \geq T_{J(DYN)}$	$T_J < T_{J(ABS)}$ and $(T_J - T_{J(REF)}) < T_{J(DYN)}$ (including hysteresis)

An indication of the device behavior, with the restart strategy set to counted restart, is shown in the figures below. $T_{J(REF)}$ is the reference temperature used for the dynamic temperature protection.

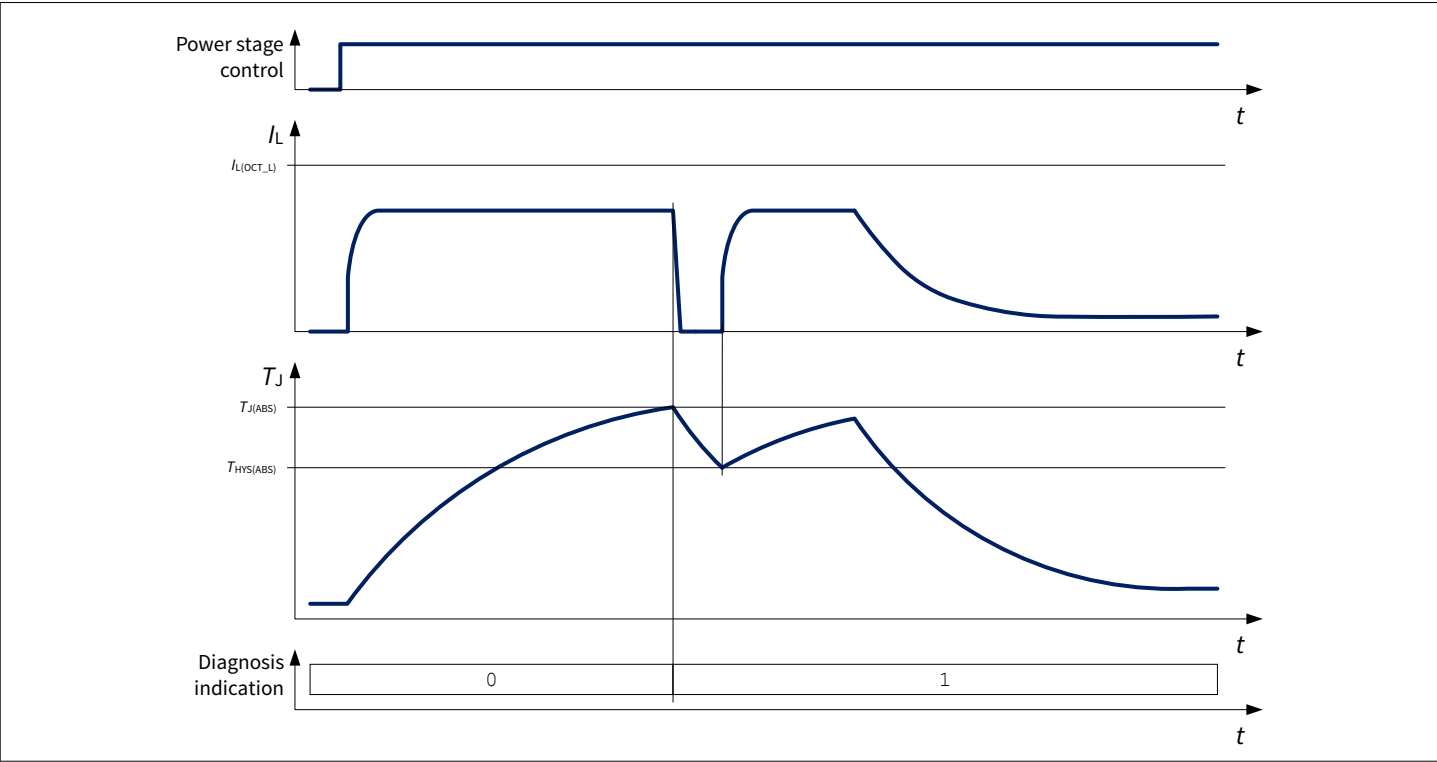


Figure 29 Overtemperature protection (absolute)

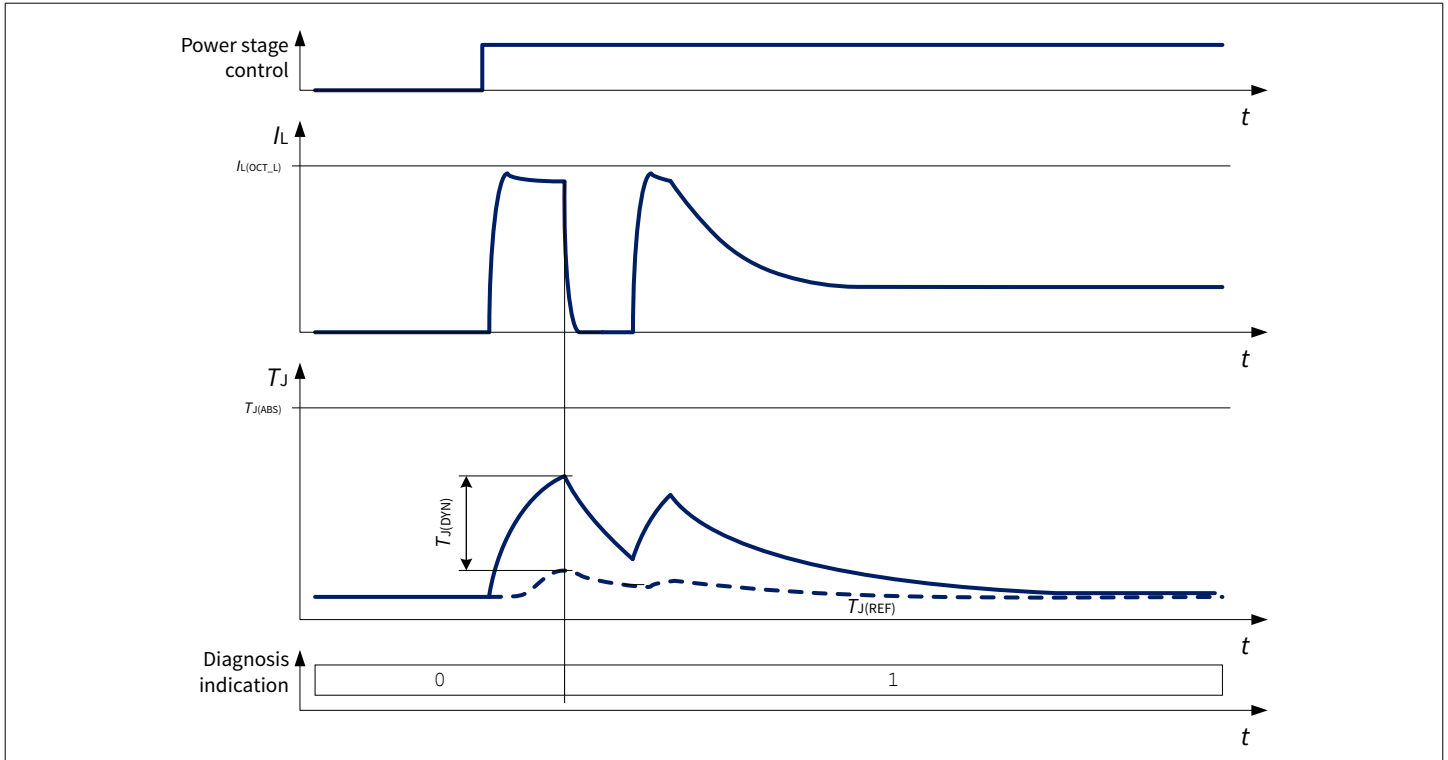


Figure 30 **Overtemperature protection (dynamic)**

When the overtemperature protection circuitry allows the power stage to be switched ON again, the restart strategy is followed as described in [Chapter 8.3](#).

8.2 Overcurrent protection

To protect the load as well as the power stage against an overload condition, the device offers an overcurrent limitation mechanism.

The overcurrent limitation consists of two interdependent detection thresholds $I_{L(OCT_L)}$ and $I_{L(OCT_H)}$, where:

$$I_{L(OCT_L)} = I_{L(OCT_H)} \cdot (1 - d_{OCT}) \quad (2)$$

If the load current increases above $I_{L(OCT_L)}$, the overcurrent limitation starts to limit the load current.

An activation of the overcurrent limitation mechanism is indicated via diagnosis.

Once an increase of the load current to $I_{L(OCT_H)}$ is detected, the protection mechanism switches OFF the power stage, and the load current starts to decrease within t_{OCT_PEAK} .

When the load current drops below $I_{L(OCT_L)}$ again, the overcurrent protection mechanism is released.

The figure below illustrates the overcurrent limitation behavior.

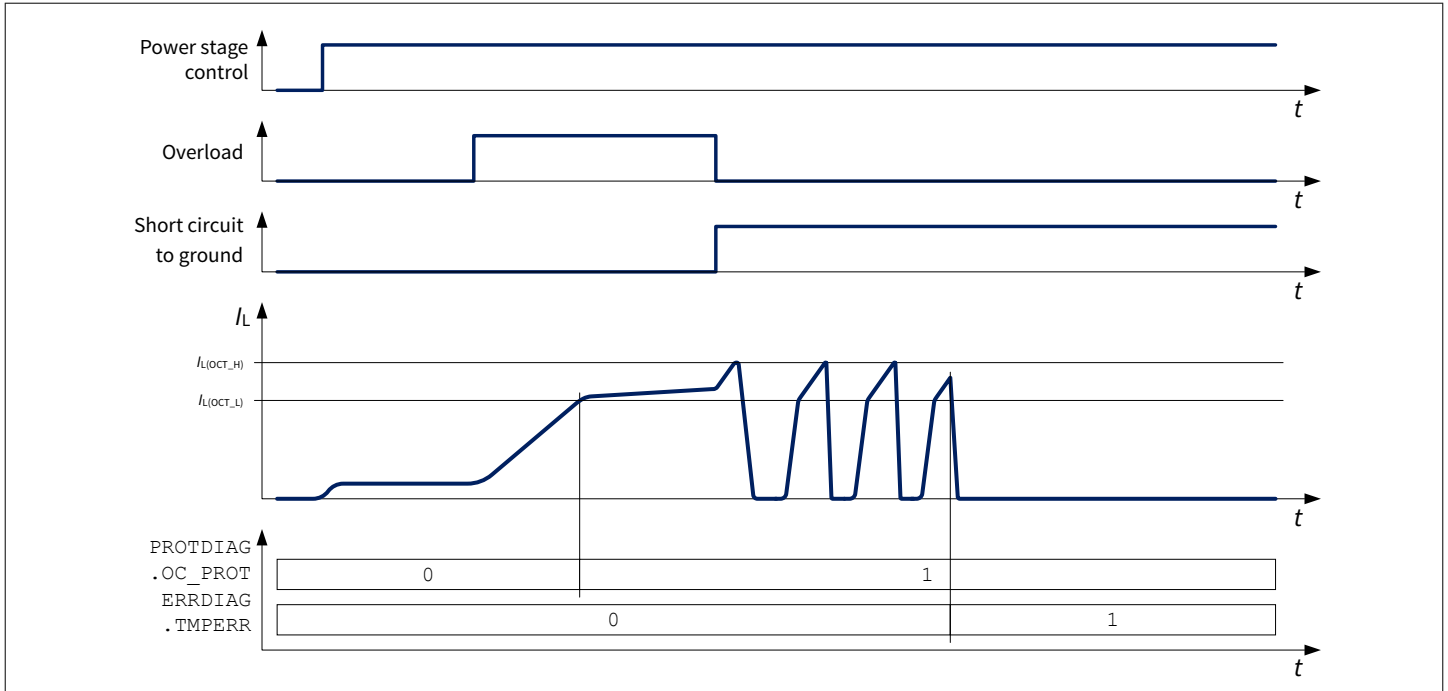


Figure 31 Overcurrent limitation behavior

Note: System-level oscillations and voltage transients, resulting from application-specific impedances and high current load disconnection, can cause overvoltage events and disturbed device communication, and thus require damping.

8.2.1 Overcurrent detection threshold

As soon as the device is in one of the normal operation modes, the $I_{L(OCT_H)}$ and its interdependent $I_{L(OCT_L)}$ can be selected via the digital interface.

The range for the selection is defined by the lowest and the highest configurable overcurrent detection threshold ($I_{L(OCT_H)}$ and $I_{L(OCT_L)}$).

For the selection of the overcurrent protection threshold the following equations are true:

- During switch-ON of the power stage ($R_{DS(ON)}$ acknowledgement status reporting is false) the overcurrent protection threshold is:

$$I_{L(OCT_H),TYP} = (I_{L(OCT_H),TYP} + OCT_{decimal} \cdot I_{L(OCT_H_LSB),TYP}) \cdot d_{OCT_SW} \quad (3)$$

- Once the power stage is in $R_{DS(ON)}$ ($R_{DS(ON)}$ acknowledgement status reporting is true) the overcurrent protection threshold is:

$$I_{L(OCT_H),TYP} = I_{L(OCT_H),TYP} + OCT_{decimal} \cdot I_{L(OCT_H_LSB),TYP} \quad (4)$$

In both cases the interdependent $I_{L(OCT_L),TYP}$ can be derived from the selected $I_{L(OCT_H),TYP}$ with the ratio

$$I_{L(OCT_L),TYP} = I_{L(OCT_H),TYP} \cdot (1 - d_{OCT}) \quad (5)$$

The default configuration of the overcurrent detection threshold high $I_{L(OCT_H)}$ can be selected from a choice of 9 values, by connecting a resistor R_{OCT} between OCT pin and GND pin. The R_{OCT} resistor is read during power-up.

An overview on which R_{OCT} is assigned to which typical $I_{L(OCT_H)}$ value is given in the table below:

Table 14 R_{OCT} mapping to $I_{L(OCT_H)}$

R_{OCT}	$I_{L(OCT_H)}$
R_{OCT_SHORT}	$I_{L(HOCT_H)}$
R_{OCT_1}	$I_{L(OCT_H)} + 0 \cdot I_{L(OCT_H_LSB)}$
R_{OCT_2}	$I_{L(OCT_H)} + 4 \cdot I_{L(OCT_H_LSB)}$
R_{OCT_3}	$I_{L(OCT_H)} + 8 \cdot I_{L(OCT_H_LSB)}$
R_{OCT_4}	$I_{L(OCT_H)} + 12 \cdot I_{L(OCT_H_LSB)}$
R_{OCT_5}	$I_{L(OCT_H)} + 16 \cdot I_{L(OCT_H_LSB)}$
R_{OCT_6}	$I_{L(OCT_H)} + 20 \cdot I_{L(OCT_H_LSB)}$
R_{OCT_7}	$I_{L(OCT_H)} + 24 \cdot I_{L(OCT_H_LSB)}$
R_{OCT_8}	$I_{L(OCT_H)} + 28 \cdot I_{L(OCT_H_LSB)}$
R_{OCT_OPEN}	$I_{L(HOCT_H)}$

During power-up, the device recognizes an OCT pin shorted to the GND pin if $R_{OCT} \leq R_{OCT_SHORT}$. In this case, the default of the $I_{L(OCT_H)}$ is set to the $I_{L(HOCT_H)}$.

An open circuit at the OCT pin is detected during power-up, if $R_{OCT} \geq R_{OCT_OPEN}$. In this case, the default of the $I_{L(OCT_H)}$ is set to $I_{L(HOCT_H)}$.

If a fault (open circuit or short circuit) at the OCT pin is detected during power-up, this is indicated on the digital interface.

In addition, the default configuration of the $I_{L(OCT_H)}$ can be set via NVM programming, as described in [Chapter 12](#).

The default settings are used under either of the following circumstances:

- During the power-up of the device
- When an SPI register reset occurs (refer to [Chapter 11.2](#))

The configurable overcurrent detection threshold $I_{L(OCT_H)}$ depends on the power supply voltage V_S . Whenever $V_S \geq V_{S(OCT)}$ and the configured $I_{L(OCT_H)} > I_{L(OCT_H_VS)}$, the overcurrent detection threshold high is set to $I_{L(OCT_H_VS)}$ as shown in the figure below. Otherwise, if the $I_{L(OCT_H)}$ is configured to a value lower than $I_{L(OCT_H_VS)}$, the overcurrent detection threshold remains at $I_{L(OCT_H)}$.

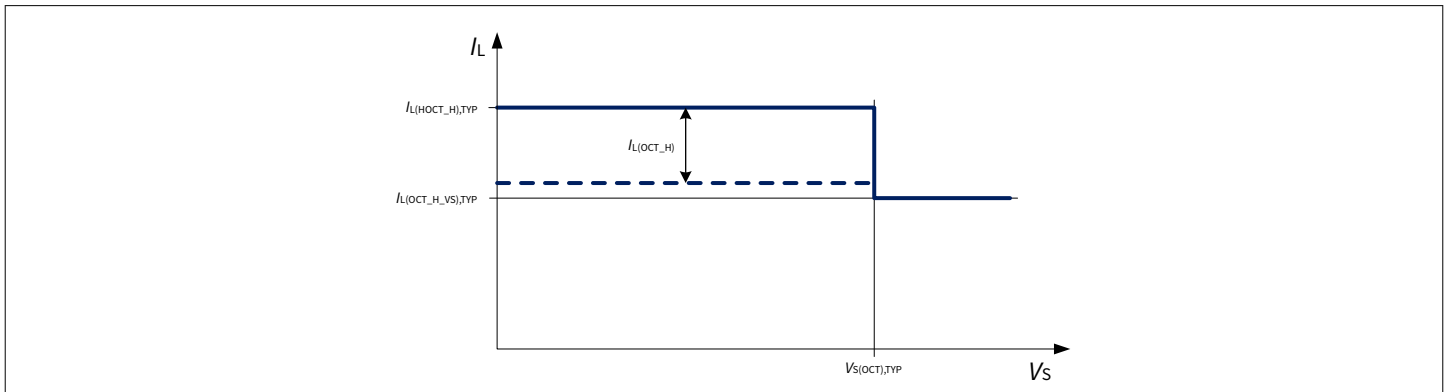


Figure 32 Overcurrent detection threshold reduction with V_S voltage

8.3 Device protection restart strategy

On the digital interface, the device offers the possibility to set the restart enable to either single latch or counted restart behavior. This defines how the device behaves if an overtemperature protection mechanism is triggered.

If an overtemperature protection mechanism is triggered and the device protection restart strategy is set to single latch, the protection latch is set and the power stage is latched OFF.

If an overtemperature protection mechanism is triggered and the device protection restart strategy is set to counted restart, the device protection restart counter (n_{RESTART}) is incremented.

The device protection restart counter can be read on the digital interface.

When the device protection restart counter exceeds $n_{\text{RESTART(LR)}}$, the protection latch is set and the power stage is latched OFF.

If the protection latch is not set, the power stage is switched ON again and the current sense is reactivated, if both of the following conditions apply:

- The power stage control = HIGH
- All protection mechanisms fulfill the reactivation conditions

There are three options to reset the protection latch and the device protection restart counter:

- Using SPI command in one of the normal operation modes: by sending a clear latch command on the digital interface, the device resets the protection latch and the device protection restart counter.
- Using the LHI pin: when the limp home mode is entered, the protection latch and the device protection restart counter are cleared to allow the activation of the power stage.
- Using the IN pin in limp home mode: the protection latch and device protection restart counter are cleared if the IN pin is set to LOW for a time longer than $t_{\text{DELAY(LR)}}$. If the IN pin is set to HIGH before $t_{\text{DELAY(LR)}}$ has elapsed, then the power stage remains latched OFF and the timer $t_{\text{DELAY(LR)}}$ is reset. The timer $t_{\text{DELAY(LR)}}$ restarts as soon as the IN pin is set to LOW again.

As soon as the protection latch is cleared and all reactivation conditions are fulfilled, the power stage switches ON again (if power stage control = HIGH) and the current sense is reactivated.

Any reset of the protection latch and device protection restart counter leads to a clearing of the error, warning and protection flags.

The device protection restart strategy and the required timings are shown in [Figure 33](#).

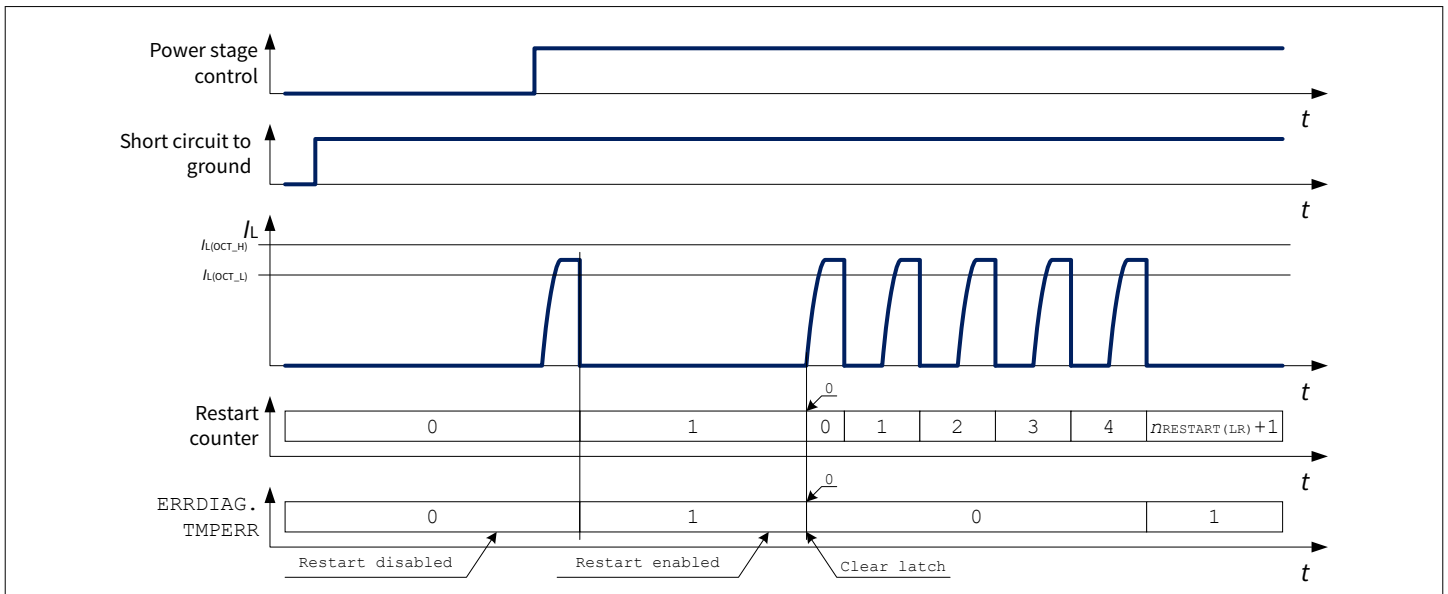


Figure 33 Restart strategy timings

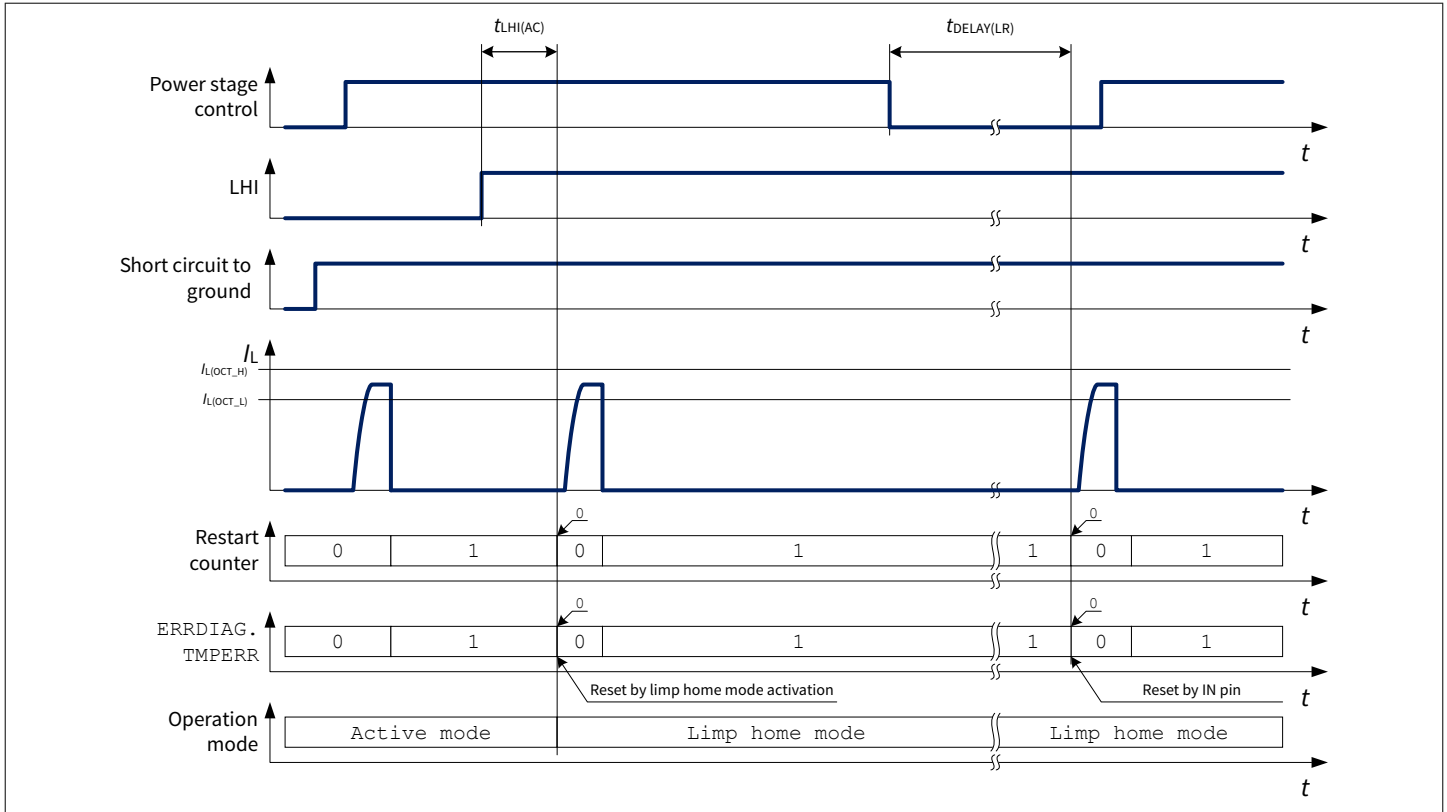


Figure 34 Restart strategy timings in limp home mode

8.4 Protection against loss of connection

8.4.1 Loss of battery and loss of load

The loss of connection to either the battery or to the load has no influence on the device robustness in the case of purely resistive loads. In this case, only the energy stored in the parasitic inductance of the wire harness needs to be handled. When driving an inductive load, the energy stored in the load and the wire harness have to be handled. In this case, an external suppressor diode (such as the diode D_{Z2} shown in [Chapter 13](#)) is recommended for handling the energy and to provide a well-defined path to the load current.

8.4.2 Loss of ground

If the device loses the connection to the ground potential, the power stage can enter an undefined state.

To avoid this undefined state during a loss of device GND, the device either switches OFF the power stage or goes into fail safe mode.

The ESD structure at the logic pins provides a parasitic ground path from the device to the ground of the microcontroller. The resulting voltage drop along this parasitic ground path defines if the power stage is deactivated or not. To support the deactivation of the power stage, it is recommended to connect a resistor between any digital input pin and the microcontroller (as described in [Chapter 13](#)). If the IN pin is evaluated as HIGH due to the aforementioned parasitic ground path, the power stage is able to switch ON or remain ON.

8.5 Additional protections

8.5.1 Reverse polarity protection

If the GND and VS pins are reversely supplied, the device is in reverse polarity condition. The load current is limited by the load itself and goes over the body diode of the power stage, which can lead to excessive overheating.

To protect the device from a thermal event while it is in reverse polarity condition ($V_{BAT(REV)} \leq V_S < 0\text{ V}$), the power stage can be switched ON automatically for self-protection if required (see parameter $R_{DS(REV)}$).

The Reverse ON feature limits the power dissipation in the power stage. Each ESD diode of the logic contributes to the total power dissipation. The reverse current through the power stage has to be limited by the connected load. The current through the digital input pins also has to be limited by an external resistor (refer to [Chapter 4.1](#) and to [Chapter 13](#)). The figure below shows a typical application including a device with the Reverse ON feature. A current flowing into the GND pin ($-I_{GND}$) during reverse polarity condition is necessary to activate the Reverse ON feature. Therefore, a resistive path between power GND of the module and device GND has to be present.

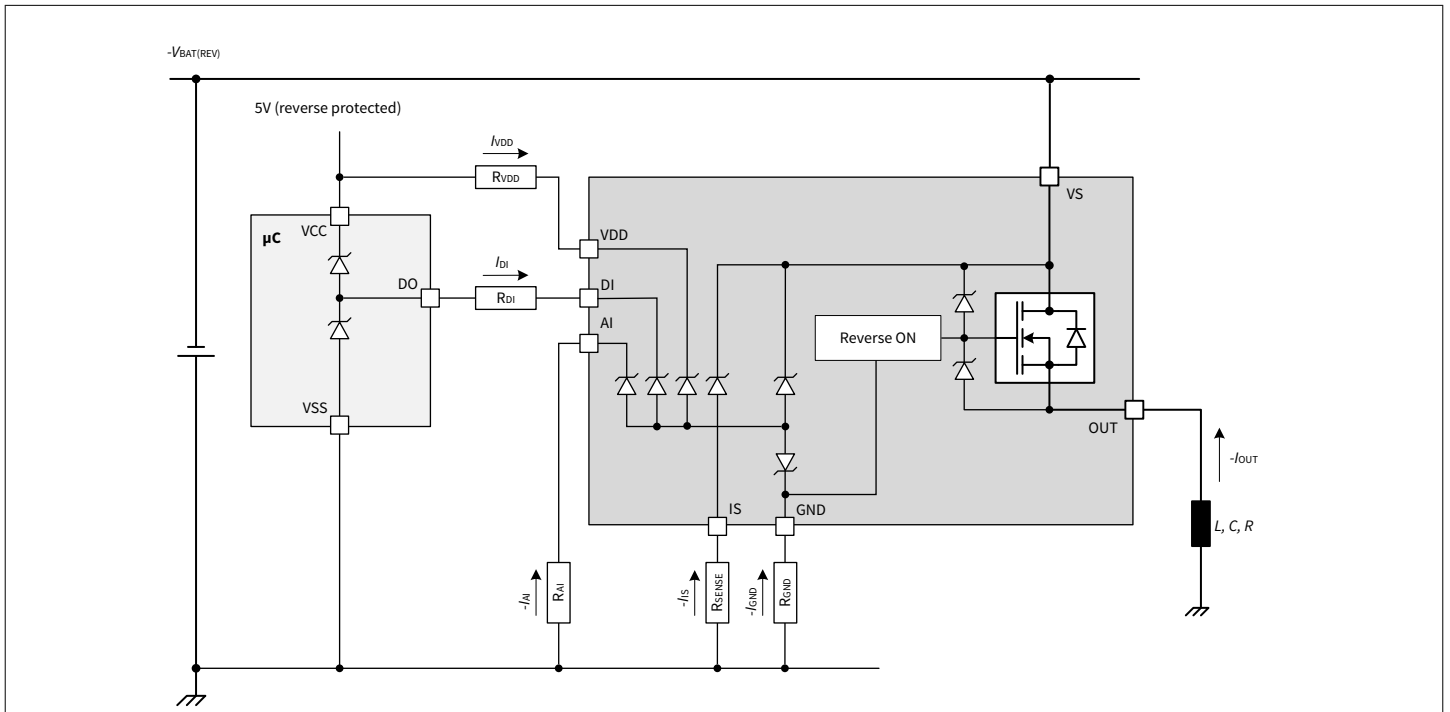


Figure 35 Reverse battery protection (application example)

8.5.2 Overvoltage protection

The device provides the following overvoltage protection mechanisms:

- $V_{S(CLAMP)}$ limits the voltage between VS and GND to protect the logic circuits
- $V_{DS(CLAMP)}$ limits the voltage between VS and OUT to protect the power stage
- $V_{SIS(CLAMP)}$ limits the voltage between VS and IS to protect the sense circuit

If the power supply voltage is above $V_{S(EXT,UP)}$ and no overvoltage protection mechanism is active, the power stage is still operational and follows the power stage control command.

To minimize overshoots above the clamping voltages, the overvoltage protection mechanisms must react quickly. However, this fast response, combined with the high-energy switch-OFF event and system impedances, can cause high dV_S/dt and oscillations on the power line. This can lead to increased current flow to the GND pin, limited by R_{GND} , resulting in a ground shift. Consequently, the logic thresholds on digital input pins may not be reached, causing disturbed device communication.

8.6 Electrical characteristics - device protections

Table 15 Electrical characteristics - device protections

$$V_S = V_{S(NOR)}, T_J = T_{J(NOR)}$$

Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			

Thermal

Thermal shutdown temperature (absolute)	$T_{J(ABS)}$	150	175	200	°C	–	PRQ-468
Thermal shutdown hysteresis (absolute)	$T_{HYS(ABS)}$	–	30	–	K	–	PRQ-728
Thermal shutdown temperature (dynamic)	$T_{J(DYN)}$	–	80	–	K	–	PRQ-469

Voltages

Power supply clamping voltage at $T_J = -40^\circ\text{C}$	$V_{S(CLAMP)_{-40}}$	33	35.5	39.5	V	$T_J = -40^\circ\text{C}$	PRQ-1283
Power supply clamping voltage at $T_J \geq 25^\circ\text{C}$	$V_{S(CLAMP)_{25}}$	35	37.5	42	V	$T_J \geq 25^\circ\text{C}$ ¹⁾	PRQ-470
Power supply voltage threshold for overcurrent threshold reduction	$V_{S(OCT)}$	20.5	22.5	24.5	V	Setup acc. to AEC-Q100-012	PRQ-471

Restart characteristics

Automatic restarts in case of fault after a latch reset	$n_{RESTART(LR)}$	–	4	–	–	²⁾	PRQ-597
Latch reset delay time after fault condition	$t_{DELAY(LR)}$	40	70	100	ms	–	PRQ-472

Overcurrent detection threshold

Lowest configurable overcurrent detection threshold low	$I_{L(LOCT_L)}$	54.5	72	89.5	A	$I_{L(OCT_H)} = I_{L(LOCT_H)}$	PRQ-1217
Lowest configurable overcurrent detection threshold high	$I_{L(LOCT_H)}$	60.6	80	99.4	A	$I_{L(OCT_H)} = I_{L(LOCT_H)}$	PRQ-474
Highest configurable overcurrent detection threshold low	$I_{L(HOCT_L)}$	157.1	188.1	219.1	A	$I_{L(OCT_H)} = I_{L(HOCT_H)}$	PRQ-1218
Highest configurable overcurrent detection threshold high	$I_{L(HOCT_H)}$	174.5	209	243.5	A	$I_{L(OCT_H)} = I_{L(HOCT_H)}$	PRQ-473

(table continues...)

Table 15 (continued) Electrical characteristics - device protections $V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$ Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overcurrent detection threshold high at high VS	$I_{L(OCT_H_VS)}$	–	142.5	–	A	$V_S \geq V_{S(OCT)}$, $I_{L(OCT_H)} > I_{L(OCT_H_VS)}$	PRQ-1430
Configurable overcurrent detection threshold LSB value	$I_{L(OCT_H_LSB)}$	–	4.1613	–	A	–	PRQ-1219
Overcurrent detection threshold interdependency ratio	d_{OCT}	–	10%	–	–	–	PRQ-1260
Overcurrent detection threshold during switch-ON ratio	d_{OCT_SW}	–	65%	–	–	$R_{DS(ON)}$ acknowledgement = 0 _B	PRQ-1781
Overcurrent peak time	t_{OCT_PEAK}	–	–	6	μs	From $I_L = I_{L(OCT_H)}$ to the value reached by I_L when I_L starts to decrease	PRQ-1761
OCT resistor threshold for short detection	R_{OCT_SHORT}	–	6.98	2%	kΩ	–	PRQ-646
OCT programming resistor 1	R_{OCT_1}	-2%	10.2	2%	kΩ	–	PRQ-1438
OCT programming resistor 2	R_{OCT_2}	-2%	14	2%	kΩ	–	PRQ-1439
OCT programming resistor 3	R_{OCT_3}	-2%	20	2%	kΩ	–	PRQ-1440
OCT programming resistor 4	R_{OCT_4}	-2%	26.7	2%	kΩ	–	PRQ-1441
OCT programming resistor 5	R_{OCT_5}	-2%	36.5	2%	kΩ	–	PRQ-1442
OCT programming resistor 6	R_{OCT_6}	-2%	47.5	2%	kΩ	–	PRQ-1449
OCT programming resistor 7	R_{OCT_7}	-2%	63.4	2%	kΩ	–	PRQ-1450
OCT programming resistor 8	R_{OCT_8}	-2%	82.5	2%	kΩ	–	PRQ-1451
OCT resistor threshold for open detection	R_{OCT_OPEN}	-2%	118	–	kΩ	–	PRQ-645

1) Tested at $T_J = 150^\circ\text{C}$ only.

2) Functional test only.

9 System protections

The device supports a stable and protected system environment by offering dedicated system protection mechanisms. This includes integrated I2t protection, configurable undervoltage lockout function, configurable overvoltage lockout function and the commanded fast switch-OFF feature, as illustrated in the block diagram below.

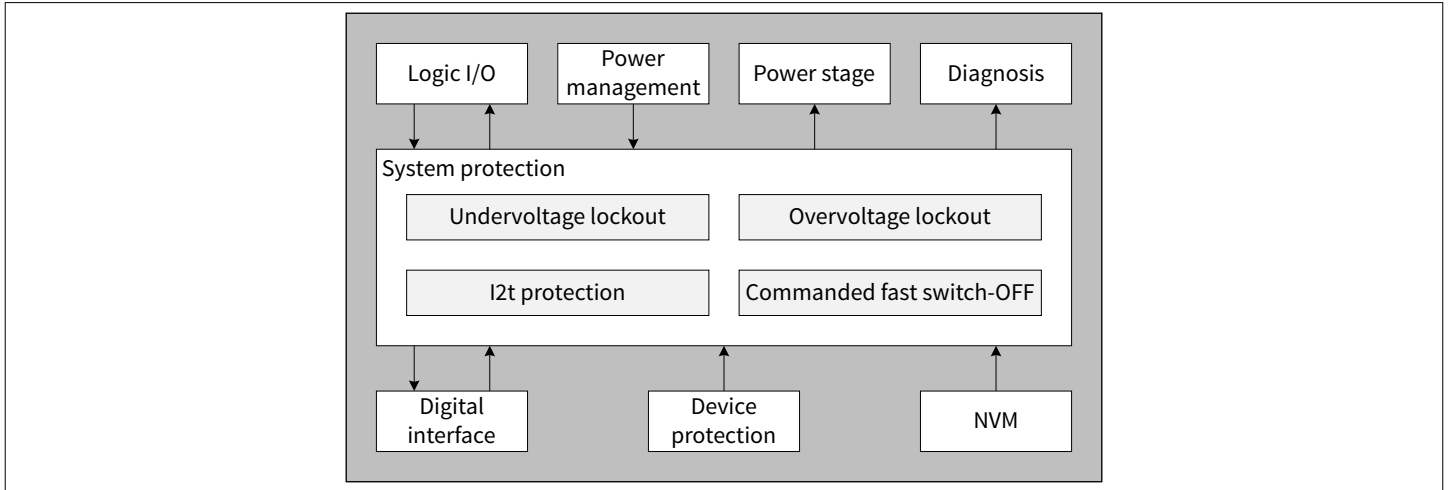


Figure 36 System protection block diagram

9.1 I2t protection

The integrated I2t protection supports the protection of the system including the wire harness and PCB traces.

The I2t protection feature calculates an I2t status S_{I2t} , which is based on the load current, the time constant and the DC current of the I2t protection curve.

The actual status of the I2t calculation can be read via the digital interface.

Once the S_{I2t} reaches 100%, the internal logic switches OFF the power stage.

When the power stage is switched OFF due to an I2t protection event, the power stage is latched OFF and the I2t status is further calculated with $I_L = 0$ A.

The time needed to trigger the I2t protection depends on the actual I2t status S_{I2t_A} and can be calculated for constant load currents by:

$$t_{I2t_TRIG} = \begin{cases} \infty & \text{for } I_L < I_{L(I2t_x)} \\ \tau_{I2t_x} \cdot \ln \left(\frac{I_L^2 - I_{L(I2t_x)}^2 \cdot S_{I2t_A}}{I_L^2 - I_{L(I2t_x)}^2} \right) & \text{for constant } I_L \geq I_{L(I2t_x)} \end{cases} \quad (6)$$

As the ambient temperature and PCB layout influence the thermal behavior of the device, the overtemperature protection might be triggered before t_{I2t_TRIG} is reached. Therefore, the maximum time for a given current is potentially limited by the thermal design of the component. For more information, refer to [Chapter 4.3](#).

If a clear latch is commanded and the $S_{I2t} < 100\%$, the power stage switches ON again (if the power stage control = HIGH) and the I2t status calculation continues with the actual load current.

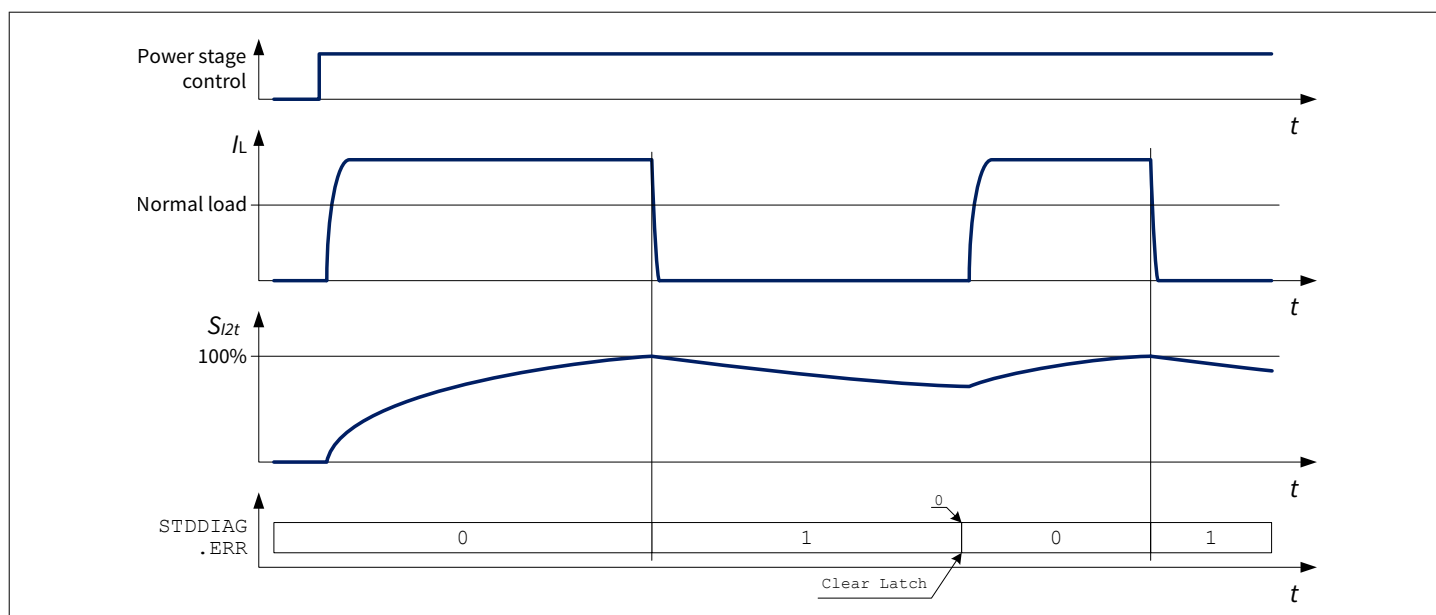


Figure 37 Restart strategy in case of triggered I2t protection

The availability of the I2t status evaluation in dependency of the operating mode is shown in [Chapter 6.1.3](#).

9.1.1 I2t protection configuration

The time constant (τ_{I2t_x}) and the DC current ($I_{L(I2t_x)}$) of the I2t protection curve can be enabled and configured via the digital interface, when the device is in one of the normal operation modes.

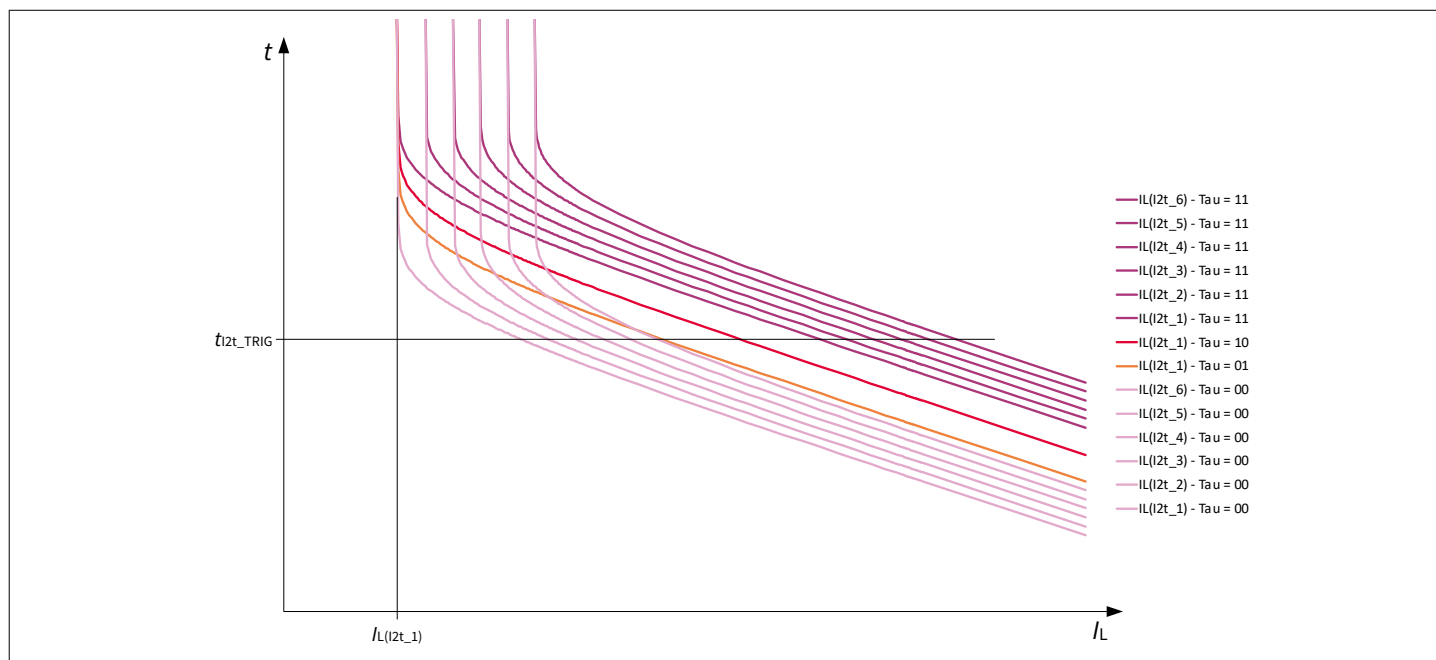


Figure 38 Energy graph of I2t protection curve

Note: This is a very simplified overview of the implemented wire protection function with different time constants. For the detailed switch-OFF behavior, refer to [Table 20](#).

The default I2t protection curve $I_{L(I2t_x)}$ can be selected with the R_{I2t} resistor connected between the I2t pin and the GND pin. The R_{I2t} resistor is read during power-up.

During power-up, the device recognizes an I2t pin shorted to the GND pin if $R_{I2t} \leq R_{I2t_SHORT}$. In this case, the default of the I2t protection curve is set to the I2t protection curve 6 with $I_{L(I2t_6)}$.

An open circuit at the I2t pin is detected during power-up, if $R_{I2t} \geq R_{I2t_OPEN}$. In this case, the default of the I2t protection curve is set to the I2t protection curve 6 with $I_{L(I2t_6)}$.

If a fault (open circuit or short circuit) at the I2t pin is detected during power-up, this is indicated on the digital interface.

In addition, both default configuration values of the I2t protection ($I_{L(I2t_x)}$ and τ_{I2t_x}) can be set via NVM programming, as described in [Chapter 12](#).

The default I2t configuration is applied:

- During the power-up of the device
- When an SPI reset occurs (refer to [Chapter 11.2](#))

9.1.2 I2t protection special conditions

As the evaluation of the I2t status and the I2t protection function is not supported in the low power modes, the I2t status is cleared in these modes to minimize the current consumption.

To ensure the protection of the system, including the wire harness, the I2t status is initialized when one of the low power modes is left. The initial value represents the I2t status due to $I_{L(I2t_I)}$.

Therefore, for the calculation of t_{I2t_TRIG} , (see equation (6)) the actual I2t status S_{I2t_A} has to be replaced by the initial I2t status S_{I2t_I} , which is given by:

$$S_{I2t_I} = \frac{I_{L(I2t_I)}^2}{I_{L(I2t_x)}^2} \quad (7)$$

If a transition to a low power mode is commanded, the I2t status is further calculated until the status goes below the initial value. Once the I2t status is below the initial value, which represents the I2t status based on the $I_{L(I2t_I)}$, the requested mode transition takes place and the I2t status is cleared.

During inverse current operation, the internal current measurement is not available for the calculation of the I2t status. Therefore, the I2t status is evaluated with $I_L = 0$ A.

9.2 Undervoltage lockout

The undervoltage lockout feature enables the definition of certain thresholds at which the device switches OFF the power stage in order to protect the power supply line. The feature can be configured as a function of the power supply voltage only, or as a combination of the function of the power supply voltage and the load current. Therefore, the device offers adjustable voltage and current thresholds, filter time, and restart behavior. [Figure 39](#) shows the device behavior if the restart is disabled. The enabled thresholds are marked with bold lines.

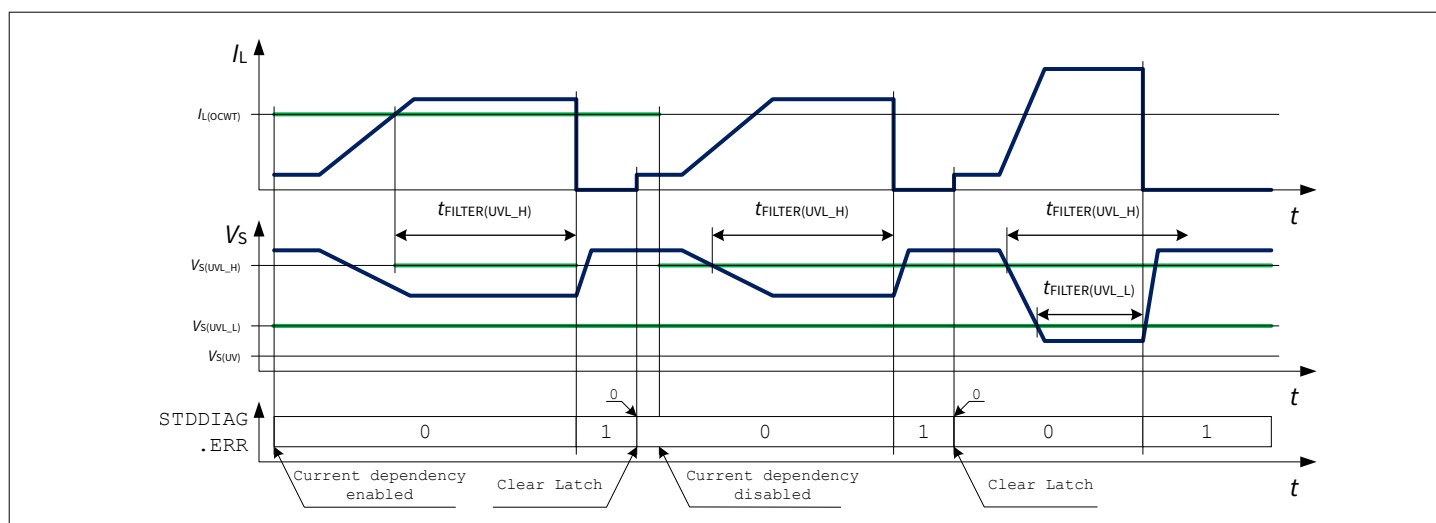


Figure 39 Undervoltage lockout

The following thresholds can be configured via the digital interface to adjust the undervoltage lockout to the application needs:

- Undervoltage lockout low threshold $V_{S(UVL_L)}$
- Undervoltage lockout high threshold $V_{S(UVL_H)}$
- Threshold for load current dependency $I_{L(OCWT)}$
- Undervoltage lockout high filter time $t_{FILTER(UVL_H)}$

The configuration ranges of the above-mentioned thresholds are given in the following table.

Table 16 Range of undervoltage lockout thresholds

	Lowest typical	Highest typical	Resolution	Accuracy
$V_{S(UVL_L)}$	4.25 V	7.53 V	$2 \cdot V_{S(LSB)}$	$V_{S(UVL_ACC)}$
$V_{S(UVL_H)}$	7.53 V	10.8 V	$2 \cdot V_{S(LSB)}$	$V_{S(UVL_ACC)}$
$I_{L(OCWT)}$	0 A	165.17 A	$8 \cdot I_{DCS(LSB)}$	According digital current measurement
$t_{FILTER(UVL_H)}$	$t_{FILTER(UVL_H_1)}$	$t_{FILTER(UVL_H_8)}$	–	–

Additionally, the device offers one bit within the digital interface to:

- Enable each undervoltage lockout threshold
- Define the restart behavior for each voltage threshold
- Enable the current dependency of the undervoltage lockout high threshold

Note: As long as the device is in active.CLS mode, the current dependency is internally disabled and the undervoltage lockout feature is sensitive to the power supply voltage measurement only.

When the power supply voltage decreases below one of the configured undervoltage lockout thresholds for a time longer than the corresponding filter time, the internal logic either switches OFF the power stage within $t_{OFF(FAST)}$ or keeps the power stage disabled.

Table 17 shows an overview on the enabled undervoltage lockout conditions as a function of the enable bits.

Table 17 Undervoltage lockout conditions, function of enable bits

UVLR2.UVL_LEN	UVLR1.UVL_HEN	UVLR2.CDEN	UVL_L	UVL_H
1	1	1	Enabled	Enabled if $I_L \geq I_{L(OCWT)}$ or $I_L \geq I_{L(OCT_L)}$
1	1	0	Enabled	Enabled
1	0	x	Enabled	Disabled
0	1	1	Disabled	Enabled if $I_L \geq I_{L(OCWT)}$ or $I_L \geq I_{L(OCT_L)}$
0	1	0	Disabled	Enabled
0	0	x	Disabled	Disabled

Note: If the current dependency of UVL_H is enabled, the UVL_H threshold is enabled by both thresholds ($I_L \geq I_{L(OCWT)}$, $I_L \geq I_{L(OCT)}$).

The undervoltage lockout restart enable bits define the restart behavior after one of the undervoltage lockout conditions is triggered.

If the undervoltage lockout restart is disabled, the power stage latches OFF and a restart can be requested with a clear latch command. If a clear latch is commanded the power stage is switched ON, independent of the reactivation conditions.

If the undervoltage lockout restart is enabled, the power stage is switched ON automatically as soon as the reactivation conditions are fulfilled, or a clear latch is commanded.

For more information on the switch-OFF and reactivation conditions, refer to [Table 18](#).

Table 18 Undervoltage lockout - switch-OFF and reactivation conditions

Fault conditions	Switch-OFF conditions	Reactivation conditions
Voltage dependent shutdown (low)	$V_{S(UV)} < V_S \leq V_{S(UVL_L)}$ for $t \geq t_{FILTER(UVL_L)}$	$V_S \geq (V_{S(UVL_L)} + V_{S(UVL_HYS)})$ for $t \geq t_{FILTER(UVL_L)}$
Voltage dependent shutdown (high)	$V_{S(UV)} < V_S \leq V_{S(UVL_H)}$ for $t \geq t_{FILTER(UVL_H)}$ if current dependency disabled	$V_S \geq (V_{S(UVL_H)} + V_{S(UVL_HYS)})$ for $t \geq t_{FILTER(UVL_L)}$
Load current and voltage dependent shutdown	$(V_{S(UV)} < V_S \leq V_{S(UVL_H)})$ and $(I_L \geq I_{L(OCWT)}$ or $I_L \geq I_{L(OCT_L)})$ for $t \geq t_{FILTER(UVL_H)}$ if current dependency enabled	$V_S \geq (V_{S(UVL_H)} + V_{S(UVL_HYS)})$ for $t \geq t_{FILTER(UVL_L)}$

The bit assignments, configurations, and default values of the undervoltage lockout feature are described in [Chapter 11](#).

Additionally, the default configuration of the undervoltage lockout feature can be set using NVM programming as described in [Chapter 12](#).

The default configuration of the undervoltage lockout feature is applied to the device:

- During the power-up of the device
- When a SPI reset occurs (refer to [Chapter 11.2](#))

9.3 Commanded fast switch-OFF

The device offers the possibility to trigger an emergency disconnection of the load via the digital interface.

This commanded fast switch-OFF function can be used in active mode, as an externally triggered protection mechanism, enabled via the digital interface. When the function is enabled the next deactivation of the power stage via the power stage control signal leads to a switch-OFF of the power stage within $t_{\text{OFF(FAST)}}$.

In the case of any primary or secondary inductivity, the overvoltage protection can be triggered, which can impact the device's reliability. Therefore, it is recommended to use this function for emergency switch-OFF only.

Therefore, the commanded fast switch-OFF function is deactivated by default.

9.4 Overvoltage lockout

The overvoltage lockout feature enables the definition of certain thresholds at which the device switches OFF the power stage in order to protect the load from transient overvoltage.

The following thresholds can be configured via the digital interface, to adjust the overvoltage lockout to the application needs:

- Overvoltage lockout threshold $V_{\text{S(OVL)}}$
- Overvoltage lockout filter time $t_{\text{FILTER(OVL)}}$

The ranges of the above-mentioned thresholds are specified in [Table 19](#)

Table 19 Range of overvoltage lockout thresholds

	Lowest typical	Highest typical	Resolution	Accuracy
$V_{\text{S(OVL)}}$	17.89 V	24 V	$8 \cdot V_{\text{S(LSB)}}$	$V_{\text{S(OVL_ACC)}}$
$t_{\text{FILTER(OVL)}}$	$t_{\text{FILTER(OVL_1)}}$	$t_{\text{FILTER(OVL_8)}}$	–	–

Additionally, the device offers one bit for the enabling and disabling of the overvoltage lockout feature.

When the power supply voltage increases above the selected $V_{\text{S(OVL)}}$ for a time longer than the selected $t_{\text{FILTER(OVL)}}$, the internal logic either switches OFF the power stage with standard slew rate or keeps the power stage disabled.

If V_{S} decreases again for one hysteresis value below the overvoltage lockout threshold ($V_{\text{S}} < V_{\text{S(OVL)}} - V_{\text{S(OVL_HYS)}}$), or a clear latch is commanded, the power stage switches ON automatically if the power stage control is HIGH.

9.5 Electrical characteristics - system protection

Table 20 Electrical characteristics - system protection

$V_{\text{S}} = V_{\text{S(NOR)}}$, $T_{\text{J}} = T_{\text{J(NOR)}}$

Typical values (unless otherwise specified): $V_{\text{S}} = V_{\text{S(NOR),TYP}}$, $T_{\text{J}} = T_{\text{J(NOR),TYP}}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
I2t protection							
IDC of I2t protection curve 1	$I_{L(I2t_1)}$	19.3	21.4	23.5	A	1)	PRQ-494
IDC of I2t protection curve 2	$I_{L(I2t_2)}$	21.6	24	26.4	A	1)	PRQ-495
IDC of I2t protection curve 3	$I_{L(I2t_3)}$	24.3	27	29.7	A	1)	PRQ-496
IDC of I2t protection curve 4	$I_{L(I2t_4)}$	27.3	30.3	33.4	A	1)	PRQ-497
IDC of I2t protection curve 5	$I_{L(I2t_5)}$	30.7	34.1	37.5	A	1)	PRQ-498

(table continues...)

Table 20 (continued) Electrical characteristics - system protection $V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$ Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
IDC of I2t protection curve 6	$I_{L(I2t_6)}$	34.5	38.3	42.1	A	1)	PRQ-499
Time constant 1 of I2t protection curve	τ_{I2t_1}	3.2	3.5	3.9	s	–	PRQ-664
Time constant 2 of I2t protection curve	τ_{I2t_2}	6.3	7.1	7.8	s	–	PRQ-665
Time constant 3 of I2t protection curve	τ_{I2t_3}	12.7	14.1	15.5	s	–	PRQ-666
Time constant 4 of I2t protection curve	τ_{I2t_4}	25.4	28.2	31	s	–	PRQ-667
Initial current for I2t protection	$I_{L(I2t_I)}$	–	5.33	–	A	–	PRQ-1357
I2t resistor threshold for short detection	R_{I2t_SHORT}	–	6.98	2%	k Ω	–	PRQ-647
I2t programming resistor for I2t protection curve 1	R_{I2t_1}	-2%	10.2	2%	k Ω	–	PRQ-1443
I2t programming resistor for I2t protection curve 2	R_{I2t_2}	-2%	14	2%	k Ω	–	PRQ-1444
I2t programming resistor for I2t protection curve 3	R_{I2t_3}	-2%	20	2%	k Ω	–	PRQ-1445
I2t programming resistor for I2t protection curve 4	R_{I2t_4}	-2%	26.7	2%	k Ω	–	PRQ-1446
I2t programming resistor for I2t protection curve 5	R_{I2t_5}	-2%	36.5	2%	k Ω	–	PRQ-1447
I2t programming resistor for I2t protection curve 6	R_{I2t_6}	-2%	47.5	2%	k Ω	–	PRQ-1448
I2t resistor threshold for open detection	R_{I2t_OPEN}	-2%	63.4	–	k Ω	–	PRQ-648

Undervoltage lockout

Undervoltage lockout accuracy	$V_{S(UVL_ACC)}$	$-4 \cdot V_{S(LS)}$ B)	–	$4 \cdot V_{S(LSB)}$)	–	–	PRQ-735
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(table continues...)

Table 20 (continued) Electrical characteristics - system protection $V_S = V_{S(NOR)}, T_J = T_{J(NOR)}$ Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}, T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Undervoltage lockout hysteresis	$V_{S(UVL_HYS)}$	–	$2 \cdot V_{S(LSB)}$	–	–	–	PRQ-736
Undervoltage lockout high filter time 1	$t_{FILTER(UVL_H_1)}$	17	32	47	μs	V_S decreasing, $V_{S(UV)} < V_S \leq V_{S(UVL_H)}$	PRQ-1460
Undervoltage lockout high filter time 2	$t_{FILTER(UVL_H_2)}$	77	100	123	μs	V_S decreasing, $V_{S(UV)} < V_S \leq V_{S(UVL_H)}$	PRQ-1461
Undervoltage lockout high filter time 3	$t_{FILTER(UVL_H_3)}$	165	200	235	μs	V_S decreasing, $V_{S(UV)} < V_S \leq V_{S(UVL_H)}$	PRQ-1462
Undervoltage lockout high filter time 4	$t_{FILTER(UVL_H_4)}$	450	520	590	μs	V_S decreasing, $V_{S(UV)} < V_S \leq V_{S(UVL_H)}$	PRQ-1463
Undervoltage lockout high filter time 5	$t_{FILTER(UVL_H_5)}$	900	1025	1150	μs	V_S decreasing, $V_{S(UV)} < V_S \leq V_{S(UVL_H)}$	PRQ-1464
Undervoltage lockout high filter time 6	$t_{FILTER(UVL_H_6)}$	8990	10045	11100	μs	V_S decreasing, $V_{S(UV)} < V_S \leq V_{S(UVL_H)}$	PRQ-1465
Undervoltage lockout high filter time 7	$t_{FILTER(UVL_H_7)}$	44900	50000	55100	μs	V_S decreasing, $V_{S(UV)} < V_S \leq V_{S(UVL_H)}$	PRQ-1466
Undervoltage lockout high filter time 8	$t_{FILTER(UVL_H_8)}$	90000	100050	110100	μs	V_S decreasing, $V_{S(UV)} < V_S \leq V_{S(UVL_H)}$	PRQ-1467
Undervoltage lockout low filter time	$t_{FILTER(UVL_L)}$	17	32	47	μs	V_S decreasing, $V_{S(UV)} < V_S \leq V_{S(UVL_L)}$	PRQ-500

Overvoltage lockout

Overvoltage lockout accuracy	$V_{S(OVL_ACC)}$	$-10 \cdot V_{S(LSB)}$	–	$10 \cdot V_{S(LSB)}$	–	–	PRQ-740
Overvoltage lockout hysteresis	$V_{S(OVL_HYS)}$	–	$8 \cdot V_{S(LSB)}$	–	–	–	PRQ-734
Overvoltage lockout filter time 1	$t_{FILTER(OVL_1)}$	24	35	45	μs	V_S increasing	PRQ-1468
Overvoltage lockout filter time 2	$t_{FILTER(OVL_2)}$	80	98	115	μs	V_S increasing	PRQ-1469
Overvoltage lockout filter time 3	$t_{FILTER(OVL_3)}$	170	200	230	μs	V_S increasing	PRQ-1470
Overvoltage lockout filter time 4	$t_{FILTER(OVL_4)}$	480	540	600	μs	V_S increasing	PRQ-1471
Overvoltage lockout filter time 5	$t_{FILTER(OVL_5)}$	930	1040	1150	μs	V_S increasing	PRQ-1472

(table continues...)

Table 20 (continued) Electrical characteristics - system protection
 $V_S = V_{S(NOR)}, T_J = T_{J(NOR)}$

 Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}, T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overvoltage lockout filter time 6	$t_{\text{FILTER(OVL_6)}}$	9000	10000	11000	μs	V_S increasing	PRQ-1473
Overvoltage lockout filter time 7	$t_{\text{FILTER(OVL_7)}}$	45000	50000	55000	μs	V_S increasing	PRQ-1474
Overvoltage lockout filter time 8	$t_{\text{FILTER(OVL_8)}}$	90000	100000	110000	μs	V_S increasing	PRQ-1475

 1) I_{2t} DC trigger level specified for times longer than 200 s.

10 Diagnosis

The device offers enhanced analog and digital diagnosis features. The analog diagnosis is available at the IS pin via the current sense signal (I_{IS}). The digital diagnosis is available via the digital interface in combination with the IRQ pin.

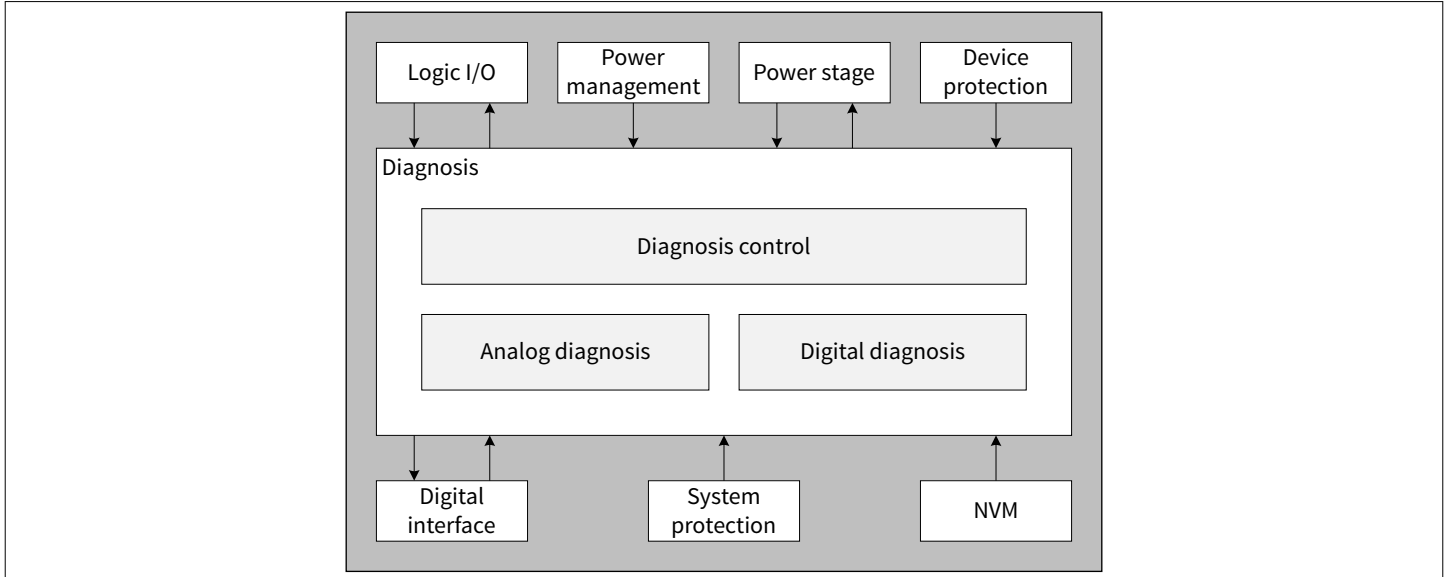


Figure 40 **Diagnosis block diagram**

10.1 Diagnosis control

The diagnosis control coordinates which diagnosis is executed and reported, either analog via the IS pin or digitally via the digital interface and the IRQ pin. The device provides control registers to enable, disable, and select the appropriate diagnosis features.

The functionality and availability of the IS pin can be configured via the analog current sense multiplexer within the diagnosis control register as listed below:

- With the analog current sense multiplexer, the power stage and its corresponding current sense signal is selected, which is routed to the IS pin
- By setting the analog current sense multiplexer to "sense verification mode", a predefined current $I_{IS(VER)}$ is provided on the IS pin, independent of the load condition
- By setting the analog current sense multiplexer to high impedance, no signal is routed to the IS pin, which is also the default setting of the analog current sense multiplexer
- Additionally, the IS pin is also set to high impedance if the analog current sense multiplexer is set to a reserved value

The default value of the analog current sense multiplexer can be set via NVM programming as described in [Chapter 12](#).

With the diagnosis control, a digital current measurement in the low range can be triggered. The start of conversion can be initiated via the digital interface.

The warning and protection-based interrupt requests, that are issued via the IRQ pin, can be activated and deactivated via the digital interface.

The device offers the possibility to perform self-checks, which can be activated via the digital interface.

10.2 Analog diagnosis

To use the analog diagnosis, which is provided on the IS pin, a sense resistor R_{SENSE} has to be connected between the IS pin and the logic GND of the module. The value for the sense resistor has to be higher than 820 Ω to limit the power losses in the sense circuitry during reverse battery condition. R_{SENSE} can be reduced to 400 Ω , when a central reverse battery protection on the used battery feed is present. A typical value for the sense resistor is $R_{SENSE} = 1.2 \text{ k}\Omega$. Due to

the internal connection between the IS pin and the supply voltage V_S , it is not recommended to connect the IS pin to the sense current output of other devices if they are supplied by a different battery feed or if a different sense concept is applied.

10.2.1 Current sense

The current sense is provided at the IS pin if the following conditions are fulfilled:

- The power stage is in $R_{DS(ON)}$ (indicated via the $R_{DS(ON)}$ acknowledgement)
- The power stage is not in inverse condition
- The current sense is enabled
- No device protection mechanism is active or power stage is latched OFF

The accuracy of the sense current I_S depends on the temperature and the load current I_L . I_S increases linearly with I_L until it reaches the saturation current $I_{S(SAT)}$. In case of open load at the power stage (I_L close to 0 A), the maximum possible sense current $I_{S(EN)}$ is specified. This condition is shown in [Figure 41](#). The blue line represents the ideal k_{ILIS} line, while the red lines show the behavior of a typical device.

An external RC filter between the IS pin and the microcontroller ADC input pin is recommended to reduce signal ripple and oscillations (a minimum time constant of 1 μ s for the RC filter is recommended). The k_{ILIS} factor is provided with limits that take the influence of temperature, supply voltage and manufacturing processes into account. Tighter limits are possible (within a defined current window) with calibration:

- A well-defined and precise current ($I_{L(CAL)}$) is applied at the output during end of line test at customer side
- The corresponding current at the IS pin is measured and the k_{ILIS} is calculated ($k_{ILIS} @ I_{L(CAL)}$)
- The calculated k_{ILIS} value can be considered within the current range going from $I_{L(CAL)_L}$ to $I_{L(CAL)_H}$ with limits defined by Δk_{ILIS}

The derating of k_{ILIS} after calibration is calculated using [\(8\)](#) and [\(9\)](#) and is specified by Δk_{ILIS} .

$$\Delta k_{ILIS, MAX} = 100 \times MAX \left(\frac{k_{ILIS @ I_{L(CAL)_L}}}{k_{ILIS @ I_{L(CAL)}}} - 1, \frac{k_{ILIS @ I_{L(CAL)_H}}}{k_{ILIS @ I_{L(CAL)}}} - 1 \right) \quad (8)$$

$$\Delta k_{ILIS, MIN} = 100 \times MIN \left(\frac{k_{ILIS @ I_{L(CAL)_L}}}{k_{ILIS @ I_{L(CAL)}}} - 1, \frac{k_{ILIS @ I_{L(CAL)_H}}}{k_{ILIS @ I_{L(CAL)}}} - 1 \right) \quad (9)$$

The calibration is intended to be performed at $T_{A(CAL)} = 25^\circ\text{C}$. The parameter Δk_{ILIS} includes the drift over the temperature and the drift over the current range from $I_{L(CAL)_L}$ to $I_{L(CAL)_H}$.

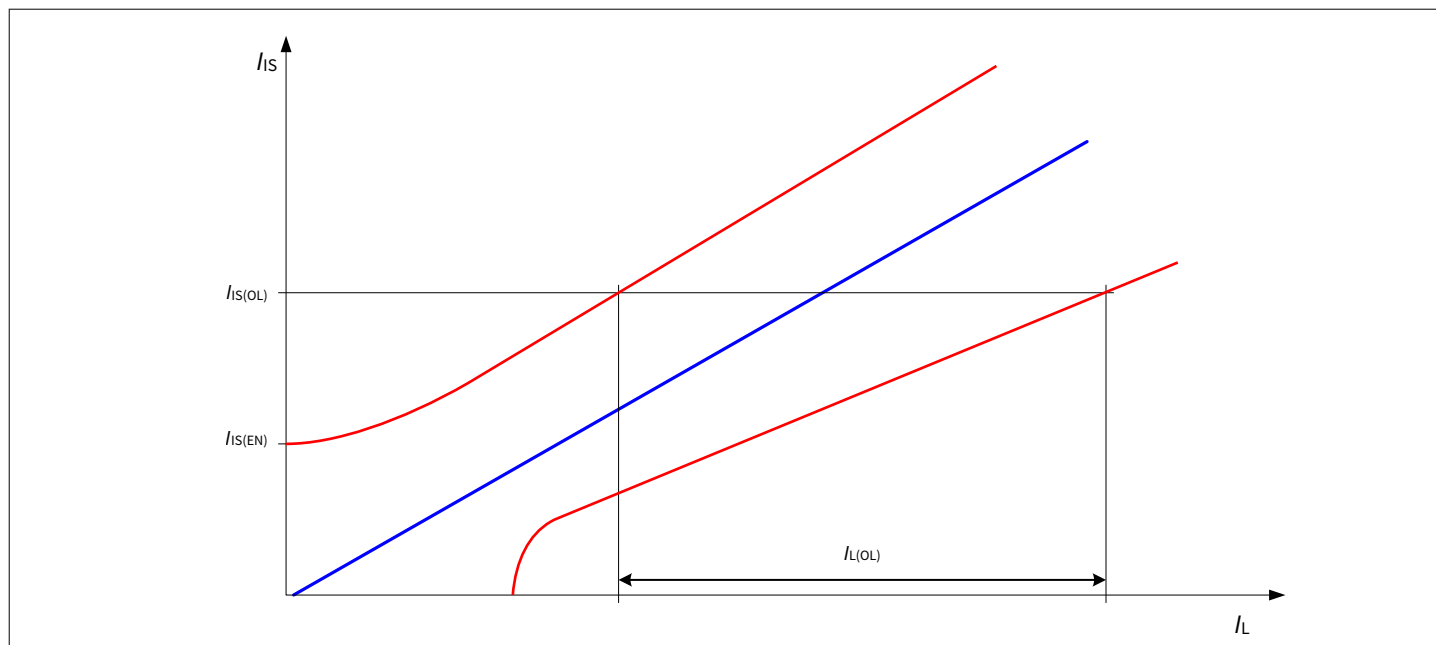


Figure 41 Current sense ratio in open load at ON condition

10.2.1.1 SENSE timings

The figure below shows the timings during enabling and disabling of the analog current sense (including the case of load change).

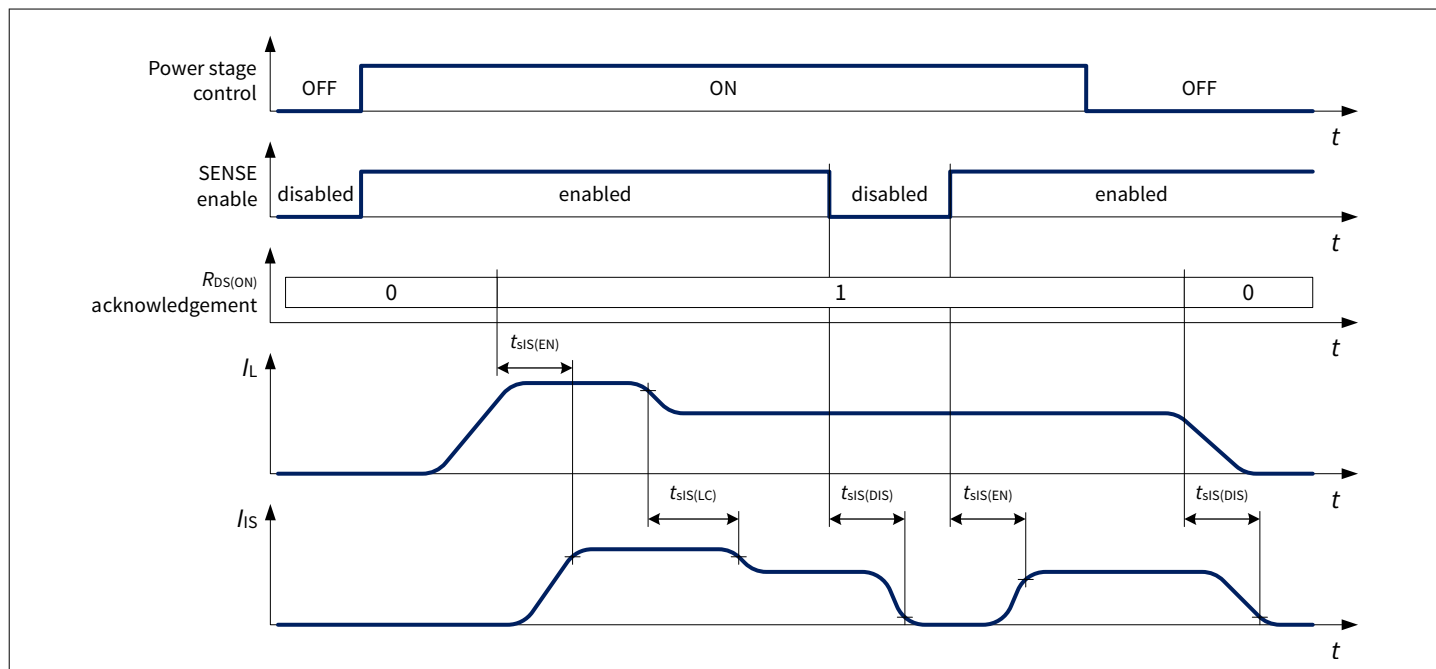


Figure 42 Current sense timings

10.3 Digital diagnosis

The digital diagnosis provides detailed information about the device status, according to the following categories:

- Error information
- Protection information
- Warning information

- Digital measurements
- Status reporting
- Self-check information

10.3.1 Error information

The information about a latched fault condition is reported in the standard diagnosis and error diagnosis registers, until a clear latch command is received.

The device provides the error diagnosis register to evaluate which type of device protection or system protection was triggered. This information is important for the microcontroller to initiate the correct restart strategy. For information on the causes of a latched error, refer to [Chapter 8](#) and [Chapter 9](#).

In addition to the error information provided via the digital interface, the device indicates via the IRQ pin that an error flag is set, by setting the IRQ pin to high impedance.

To be able to distinguish on the IRQ pin between an error event and the idle mode indication, the error information is propagated with a PWM signal with $f_{\text{IRQ(ERR_IDL)}}$ and $DC_{\text{IRQ(ERR_IDL)}}$ on the IRQ pin, if the idle mode is requested.

10.3.2 Protection information

The device incorporates protection mechanisms with and without automatic restart. Whereas the error information provides the information about the triggered protection mechanism leading to a latched-OFF power stage, the protection flag indicates a triggered protection mechanism which does not have to lead to a latched-OFF power stage.

A protection flag is set, when at least one of the following protection mechanisms is triggered:

- Undervoltage lockout low
- Undervoltage lockout high
- Overvoltage lockout
- Overcurrent protection
- Absolute overtemperature protection
- Dynamic overtemperature protection

When a protection flag is set, the information is stored and indicated via the digital interface until the dedicated registers are read by the microcontroller.

Additionally, the device provides a protection-based interrupt on the IRQ pin by setting the pin to high impedance. The protection flags are clustered and can be linked to the IRQ pin via the digital interface as follows:

- Power supply voltage
 - Undervoltage lockout low
 - Undervoltage lockout high
 - Overvoltage lockout
- Overcurrent protection
- Device temperature
 - Absolute overtemperature protection
 - Dynamic overtemperature protection

10.3.3 Warning information

The device offers several warning flags to inform the microcontroller about a potential issue in the application.

Warning flags for the following quantities are available:

- Inverse current
- Load current
- Device temperature
- I2t status
- Power supply voltage

A warning flag is set when the respective device parameter violates its predefined threshold, which can be set via the digital interface.

While the thresholds for load current, device temperature, I2t status, and power supply voltage can be selected via digital interface, the inverse current detection is a fixed value, as described in [Chapter 10.3.6](#).

As the overcurrent warning threshold depends on the current sense, which is disabled when the $V_{DS} \geq V_{DS(ON)}$, also the warning flag for overcurrent is not available in these conditions.

However, the overcurrent flag is also set when the device is in overcurrent limitation.

When a warning flag is set, the information is stored and indicated via the digital interface until the dedicated registers are read by the microcontroller.

Additionally, the device provides a warning-based interrupt on the IRQ pin by setting the pin to high impedance. The following warning flags can be linked to the IRQ pin via the digital interface:

- Inverse current warning flag
- Load current warning flag
- Device temperature warning flag
- I2t status warning flag
- Power supply voltage warning flag

10.3.4 Communication information

The device offers following communication flags to inform the microcontroller about a potential issue in the communication path:

- Modulo counter error
- Register access error

When a communication flag is set, the information is stored and indicated via the digital interface until the dedicated registers are read by the microcontroller.

10.3.5 Digital measurements

The device offers several diagnosis registers in the digital interface, which provides information about the following quantities:

- Load current
- Device temperature
- Power supply voltage

10.3.5.1 Digital current sense

The 8-bit digital current sense is provided in a dedicated diagnosis register, if the following conditions are fulfilled:

- The power stage is in $R_{DS(ON)}$ (indicated via the $R_{DS(ON)}$ acknowledgement)
- The power stage is not in inverse condition
- No device protection mechanism is active
- Power stage is not latched OFF

To calculate the corresponding load current from the digital current sense, the following equation has to be used:

$$I_L = I_{DCS(LSB)} \cdot DCS_{decimal} \quad (10)$$

To provide valuable information about the load current in the low current range down to the open load range, the digital current sense low range can be requested via the digital interface.

When requested, the low range current measurement is performed when the load current is within the low range ($I_L \leq I_{DCSLR(ENTRY)}$).

To allow sufficient time for the low range measurement, the settling time t_{SDCSLR} has to be considered between start of conversion and results available in the dedicated register.

The device indicates via the digital interface that the value within the digital interface is invalid if one of the following points is true:

- No measurement was ever requested (register content = 0xFF)
- A measurement was requested but the load current is out of the low range (register content = 0xFF)
- A measurement was requested and started, but the load current increased during the measurement out of the low range (register content = 0xFF)
- A measurement was requested but the measurement is not yet finished ($t < t_{sDCSLR}$) (register content = 0x00)

The current measurement range is set automatically back to normal range if either the low range measurement is finished or was aborted.

10.3.5.2 Device temperature measurement

The device features a 6 bit temperature measurement, which reflects the device temperature within the logic area. The measurement result is provided via the digital interface.

To calculate the device temperature, the content of the corresponding register has to be used within the following equation:

$$T_{DEV} = T_{DEV(LSB)} \cdot DEVT_{decimal} + T_{DEV(RANGE), MIN} \quad (11)$$

10.3.5.3 VS measurement

The implemented voltage measurement reflects the power supply voltage of the device in reference to the device GND. The measurement result is provided in a dedicated register via the digital interface.

To calculate the power supply voltage, the content of the corresponding register has to be used within the following equation:

$$V_S = V_{S(LSB)} \cdot VS_{decimal} \quad (12)$$

10.3.6 Status reporting

The device offers the possibility to read the following information via the digital interface:

- I2t status
- External programming resistor for I2t
- External programming resistor for OCT
- IN pin status
- LHI pin status
- ON-state diagnosis
- OFF-state diagnosis
- Power stage control status
- Inverse current diagnosis

Furthermore, the power stage status is evaluated and results in the following status reports:

- The ON-state status reporting (ONDIAG) indicates that the power stage is switched ON if $V_{DS} \leq V_{DS(ON)}$ for a time longer than $t_{FILTER(PSD_SET)}$. The result of the comparison can be read via the digital interface.
- The OFF-state status reporting (OFFDIAG) indicates that the power stage is switched OFF if $V_{OUT} \leq V_{OUT(OFF)}$ for a time longer than $t_{FILTER(PSD_SET)}$. The result of the comparison can be read via the digital interface.
- The $R_{DS(ON)}$ acknowledgement indicates that the power stage is in $R_{DS(ON)}$. This information can be read via the digital interface.

- When the device is in active mode, the inverse reporting (INVDIAG) indicates that $I_L \leq I_{L(INV_ON)}$ for a time longer than $t_{FILTER(INV)}$. The result of the comparison can be read via the digital interface.
- When the device is in inactive mode, the inverse reporting (INVDIAG) indicates that $I_L \leq I_{L(INV_OFF)}$ for a time longer than $t_{FILTER(INV)}$. The result of the comparison can be read via the digital interface.

The status reporting via the digital interface is reset, if the condition for the ON-state status ($V_{DS} \leq V_{DS(ON)}$) or OFF-state status ($V_{OUT} \leq V_{OUT(OFF)}$) is not fulfilled for a time longer than $t_{FILTER(PSD_RES)}$.

The behavior of the ON-state status reporting and the OFF-state status reporting is shown in the figure below.

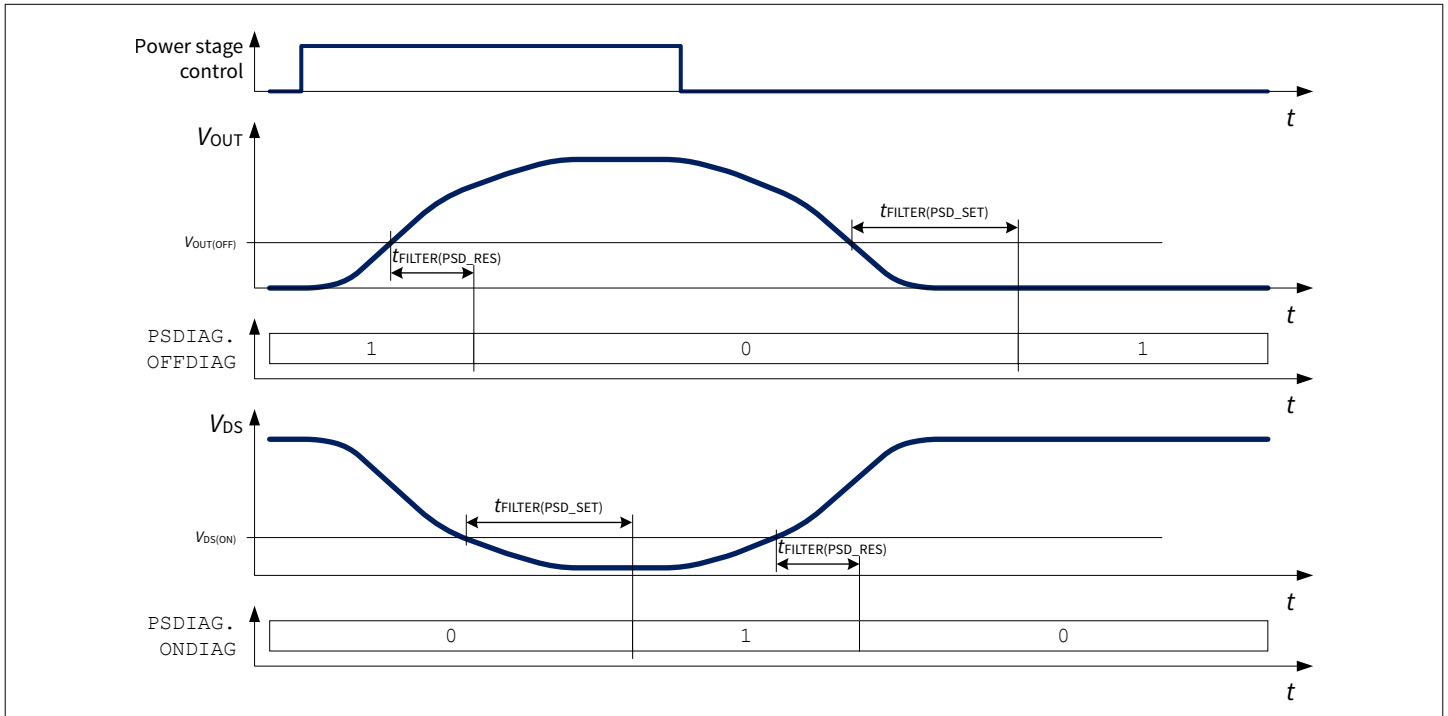


Figure 43 Power stage diagnosis indication timings

10.3.7 Self-check information

The device offers the feature to perform the following self-checks:

- IRQ pin check
- ON to OFF switchability check of the power stage

The activation of the self-checks can be requested via the self-check register.

By enabling the IRQ self-check via the digital interface, the IRQ pin is forced to high impedance within t_{IRQ} . Once the IRQ self-check is disabled, the IRQ pin is released and operates again according to the device configuration within t_{IRQ} .

The ON to OFF switchability check can be activated while the device is in active mode and the power stage is enabled. By activating the ON to OFF switchability check, the power stage starts to switch OFF until $V_{DS} > V_{DS(ON)}$. Once the threshold is reached, the power stage switches ON again.

If the V_{DS} does not increase above $V_{DS(ON)}$ within $t_{SC(ON2OFF)}$, the switchability check is stopped. This is indicated in the dedicated bitfield of the self-check register.

Additionally, the device automatically performs a self-diagnosis. If an internal fault is detected, which can potentially lead to unreliable device behavior, this is indicated via the digital interface and the IRQ pin.

10.4 Electrical characteristics - diagnosis

Table 21 Electrical characteristics - diagnosis

 $V_S = V_{S(NOR)}, T_J = T_{J(NOR)}$

 Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}, T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Analog diagnosis							
SENSE saturation current	$I_{IS(SAT)}$	4.2	–	–	mA	$V_{SIS} = V_S - V_{IS} \geq 1\text{ V}$, $I_{L(OCT_H)} = I_{L(HOCT_H)}$	PRQ-476
SENSE leakage current when disabled	$I_{IS(OFF)}$	–	0.01	0.5	μA	Current sense disabled	PRQ-477
SENSE leakage current when enabled	$I_{IS(EN)}$	–	0.2	2	μA	Current sense enabled, $I_L = 0\text{ A}$	PRQ-1265
SENSE current in sense verification mode	$I_{IS(VER)}$	400	500	600	μA	Sense verification mode enabled	PRQ-1270
Saturation voltage in kILIS operation (VS - VIS)	V_{SIS_k}	–	0.5	1	V	Device in active mode, current sense enabled, $V_S = 5\text{ V}$	PRQ-479
Power supply to IS pin clamping voltage at $T_J = -40^\circ\text{C}$	$V_{SIS(CLAMP)_-40}$	33	35.5	39.5	V	$T_J = -40^\circ\text{C}$	PRQ-1266
Power supply to IS pin clamping voltage at $T_J \geq 25^\circ\text{C}$	$V_{SIS(CLAMP)_25}$	35	37.5	42	V	$T_J \geq 25^\circ\text{C}$ ¹⁾	PRQ-480
SENSE settling time after diagnosis enable	$t_{SIS(EN)}$	–	5	20	μs	Device in active mode, from (current sense enabled and $RON_ACK = 1_B$) to $I_{IS} = I_L / (k_{ILIS,MAX} @ I_L) \cdot 0.9$, $I_L > I_{L(CAL)_OL_H}$	PRQ-481
SENSE settling time after diagnosis enable with small load current	$t_{SIS(EN)_SLC}$	–	–	60	μs	Device in active mode, from (current sense enabled and $RON_ACK = 1_B$) to $I_{IS} = I_L / (k_{ILIS,MAX} @ I_L) \cdot 0.9$, $I_L \leq I_{L(CAL)_OL_H}$	PRQ-1431
SENSE disable time	$t_{SIS(DIS)}$	–	5	20	μs	Device in active mode, from (current sense disabled or $RON_ACK = 0_B$) to $I_{IS} \leq I_{IS(OFF)}$	PRQ-1268
SENSE settling time after load change	$t_{SIS(LC)}$	–	5	20	μs	Device in active mode, current sense enabled, load change from $I_L = I_{L(CAL)}$ to $I_{L(CAL)} / 2$ or vice versa	PRQ-482

(table continues...)

Table 21 (continued) Electrical characteristics - diagnosis
 $V_S = V_{S(NOR)}, T_J = T_{J(NOR)}$

 Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}, T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SENSE settling time after load change with small load current	$t_{SIS(LC_SLC)}$	–	20	100	µs	Device in active mode, current sense enabled, load change from $I_L = I_{L(CAL)}$ to $I_{L(CAL_OL)}$	PRQ-1269
Open load output current at $I_{IS} = 4 \mu A$	$I_{L(OL_4u)}$	60	180	300	mA	Device in active mode, $I_{IS} = I_{IS(OL)} = 4 \mu A$	PRQ-485
Current sense ratio #09	k_{ILIS09}	-26.7%	39300	+26.7%	–	$400 \text{ mA} \leq I_L < I_{L(OCT_L)}$	PRQ-1273
Current sense ratio #12	k_{ILIS12}	-9.9%	39300	+9.9%	–	$1.5 \text{ A} \leq I_L < I_{L(OCT_L)}$	PRQ-1274
Current sense ratio #15	k_{ILIS15}	-5.8%	39300	+5.8%	–	$4 \text{ A} \leq I_L < I_{L(OCT_L)}$	PRQ-1275
Current sense ratio #20	k_{ILIS20}	-4.4%	39300	+4.4%	–	$15 \text{ A} \leq I_L < I_{L(OCT_L)}$	PRQ-1277
Current sense ratio #22	k_{ILIS22}	-4.1%	39300	+4.1%	–	$25 \text{ A} \leq I_L < I_{L(OCT_L)}$	PRQ-1278
Current sense ratio #24	k_{ILIS24}	-3.9%	39300	+3.9%	–	$35 \text{ A} \leq I_L < I_{L(OCT_L)}$	PRQ-1279
Current sense ratio #27	k_{ILIS27}	-3.9%	39300	+3.9%	–	$50 \text{ A} \leq I_L < I_{L(OCT_L)}$	PRQ-490
SENSE current derating with low current calibration	$\Delta k_{ILIS(OL)}$	-14%	–	+14%	–	$I_{L(CAL_OL)} = 1.5 \text{ A}, I_{L(CAL_OL_H)} = 4 \text{ A}, I_{L(CAL_OL_L)} = 400 \text{ mA}, T_{A(CAL)} = 25^\circ\text{C}$	PRQ-488
SENSE current derating with nominal current calibration	$\Delta k_{ILIS(NOM)}$	-2%	–	+2%	–	$I_{L(CAL)} = 35 \text{ A}, I_{L(CAL_H)} = 50 \text{ A}, I_{L(CAL_L)} = 25 \text{ A}, T_{A(CAL)} = 25^\circ\text{C}$	PRQ-489

Digital diagnosis

Frequency for error indication at IRQ pin during idle mode request	$f_{IRQ(ERR_IDL)}$	–	100	–	Hz	–	PRQ-1477
Duty cycle for error indication at IRQ pin during idle mode request	$DC_{IRQ(ERR_IDL)}$	–	50%	–	–	–	PRQ-1478
Drain source voltage for ON-state detection	$V_{DS(ON)}$	0.5	0.7	0.9	V	–	PRQ-483
Output voltage for OFF-state detection	$V_{OUT(OFF)}$	1.2	1.6	2.7	V	–	PRQ-1243
Load current for inverse current detection in ON state	$I_{L(INV_ON)}$	-19	–	-0.1	A	Device in active mode	PRQ-1731

(table continues...)

Table 21 (continued) Electrical characteristics - diagnosis
 $V_S = V_{S(NOR)}, T_J = T_{J(NOR)}$

 Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}, T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Load current for inverse current detection in OFF state	$I_{L(INV_OFF)}$	-300	–	-1	μA	Device in inactive mode	PRQ-1768
Power stage diagnosis set filter time	$t_{FILTER(PSD_SET)}$	200	240	280	μs	–	PRQ-1488
Power stage diagnosis reset filter time	$t_{FILTER(PSD_RES)}$	100	120	140	μs	–	PRQ-1489
Inverse current indication filter time	$t_{FILTER(INV)}$	0.9	1	1.1	ms	–	PRQ-1244
ON to OFF self-check time	$t_{SC(ON2OFF)}$	90	100	110	ms	–	PRQ-1246
Switching time of IRQ pin	t_{IRQ}	–	–	3	μs	–	PRQ-1491

Digital measurements

ADC sample time	$t_{SAMPLE(ADC)}$	7.5	8.4	9.3	μs	–	PRQ-1362
Digital current sense range	$I_{DCS(RANGE)}$	0	–	$I_{L(HOCT_L),Min}$	A	–	PRQ-1340
Digital current sense LSB value	$I_{DCS(LSB)}$	–	666	–	mA	–	PRQ-1250
Digital current sense settling time	t_{sDCS}	–	40	74	μs	$0.1 * I_{L(NOM)_85} \leq I_L \leq I_{L(OCT_L)}$	PRQ-1363
Digital current sense accuracy #13	ACC_{DCS13}	-67%	–	+67%	–	$2 A \leq I_L < I_{L(OCT_L)}$	PRQ-1341
Digital current sense accuracy #15	ACC_{DCS15}	-17%	–	+17%	–	$4 A \leq I_L < I_{L(OCT_L)}$	PRQ-1342
Digital current sense accuracy #18	ACC_{DCS18}	-7%	–	+7%	–	$10 A \leq I_L < I_{L(OCT_L)}$	PRQ-1343
Digital current sense accuracy #20	ACC_{DCS20}	-7%	–	+7%	–	$15 A \leq I_L < I_{L(OCT_L)}$	PRQ-1344
Digital current sense accuracy #22	ACC_{DCS22}	-7%	–	+7%	–	$25 A \leq I_L < I_{L(OCT_L)}$	PRQ-1345
Digital current sense accuracy #24	ACC_{DCS24}	-7%	–	+7%	–	$35 A \leq I_L < I_{L(OCT_L)}$	PRQ-1346
Digital current sense accuracy #27	ACC_{DCS27}	-7%	–	+7%	–	$50 A \leq I_L < I_{L(OCT_L)}$	PRQ-1360

(table continues...)

Table 21 (continued) Electrical characteristics - diagnosis
 $V_S = V_{S(NOR)}, T_J = T_{J(NOR)}$

 Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}, T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Digital current sense low range LSB value	$I_{DCSLR(LSB)}$	–	30	–	mA	–	PRQ-1721
Digital current sense low range settling time	t_{sDCSLR}	–	170	205	μs	$0 A < I_L < I_{DCSLR(ENTRY)}$	PRQ-1455
Digital current sense low range entry threshold	$I_{DCSLR(ENTRY)}$	2	2.5	3	A	–	PRQ-1757
Accuracy of digital current sense low range #05	$ACC_{DCSLR05}$	-70%	–	+70%	–	$100 mA \leq I_L < I_{DCSLR(ENTRY)}$	PRQ-1725
Accuracy of digital current sense low range #08	$ACC_{DCSLR08}$	-30%	–	+30%	–	$300 mA \leq I_L < I_{DCSLR(ENTRY)}$	PRQ-1726
Accuracy of digital current sense low range #10	$ACC_{DCSLR10}$	-12%	–	+12%	–	$750 mA \leq I_L < I_{DCSLR(ENTRY)}$	PRQ-1727
Accuracy of digital current sense low range #11	$ACC_{DCSLR11}$	-12%	–	+12%	–	$1 A \leq I_L < I_{DCSLR(ENTRY)}$	PRQ-1728
Accuracy of digital current sense low range #13	$ACC_{DCSLR13}$	-10%	–	+10%	–	$2 A \leq I_L < I_{DCSLR(ENTRY)}$	PRQ-1729
Device temperature measurement range	$T_{DEV(RANGE)}$	-40	–	171.7	°C	–	PRQ-1347
Device temperature measurement LSB value	$T_{DEV(LSB)}$	–	3.36	–	°C	–	PRQ-1251
Accuracy of device temperature measurement	ACC_{TDEV}	-7	–	7	°C	–	PRQ-1348
Power supply voltage measurement range	$V_{S(RANGE)}$	3.5	–	24	V	–	PRQ-1349
Power supply voltage measurement LSB value	$V_{S(LSB)}$	–	109.1	–	mV	–	PRQ-1249
Power supply voltage measurement settling time	t_{sVS}	–	–	20	μs	–	PRQ-1364

(table continues...)

Table 21 (continued) Electrical characteristics - diagnosis
 $V_S = V_{S(NOR)}, T_J = T_{J(NOR)}$

 Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}, T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Accuracy of power supply voltage measurement low range	$ACC_{VS(LOW)}$	$-4 \cdot V_{S(LSB)}$	–	$4 \cdot V_{S(LSB)}$	–	$3.5 \text{ V} \leq V_S < 12 \text{ V}$	PRQ-1248
Accuracy of power supply voltage measurement high range	$ACC_{VS(HIGH)}$	$-10 \cdot V_{S(LSB)}$	–	$10 \cdot V_{S(LSB)}$	–	$12 \text{ V} \leq V_S < 24 \text{ V}$	PRQ-1361

 1) Tested at $T_J = 150^\circ\text{C}$

11 Digital interface

The serial peripheral interface (SPI) is a full duplex synchronous serial slave interface, which uses four signal lines: SO, SI, SCLK, and CSN. While on the SI and SO, the data is transferred at the data rate set by SCLK, the signal on CSN defines whether the device is listening to the communication.

The falling edge of CSN indicates the beginning of an access frame. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access frame has to be terminated on a rising edge of CSN.

A modulo 8 counter ensures that a command is accepted only when a multiple of 8-bits has been transferred, with a minimum of 24 bits.

Starting from the most significant bit (MSB), these 24 bits consist of 8-bit CRC, 8-bit address, and 8-bit data (as shown in Figure 44). For further information on the CRC calculation, refer to Chapter 11.5.

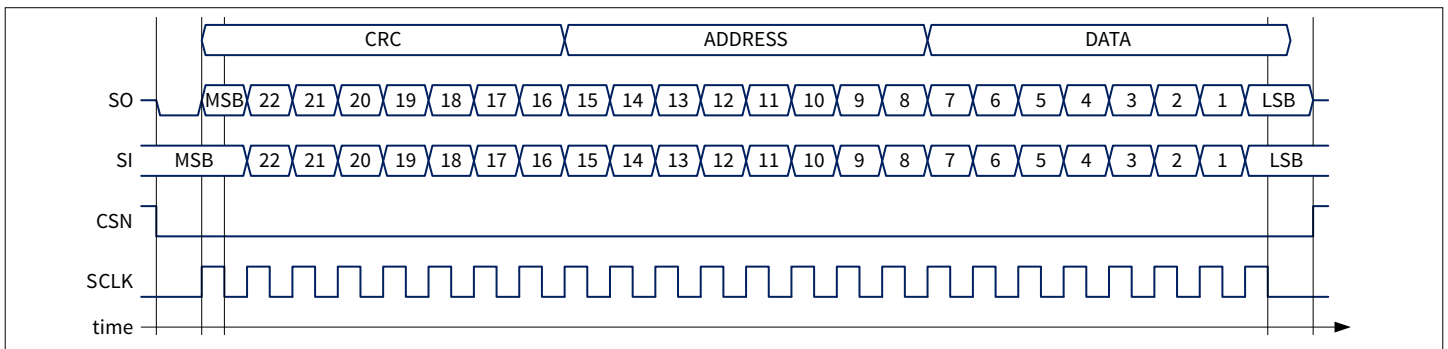


Figure 44 Serial peripheral interface

11.1 SPI signal description

CSN - chip select negated

The system microcontroller selects the device by means of the CSN pin. When the pin is in LOW state, data can be transmitted. When CSN is in HIGH state, any signal at the SCLK and SI pins are ignored, and the SO pin is driven to a high impedance state.

- **CSN HIGH to LOW transition**

- The previously requested information is transferred into the shift register
- The SO pin changes from high impedance to LOW

- **CSN LOW to HIGH transition**

- Command decoding is only done when, after the falling edge of CSN, an exact multiple (1, 2, 3, ...) of 8 SCLK signals have been detected, with a minimum of 24. In the case of an incorrect SCLK count, the communication error flag and modulo counter error flag are set and the command is ignored
- Data from the shift register is transferred into the addressed register

SCLK - serial clock

This input pin clocks the internal shift register. It is essential that the SCLK pin is in LOW state whenever the CSN makes any transition, otherwise the command may not be accepted.

SI - serial input

Serial input data bits are shifted in at this pin, the most significant bit first. The information at the SI pin is read by the device on the falling edge of SCLK. For more information, refer to Chapter 11.1.1.

SO - serial output

During transmission, the response data is serially shifted out at this pin, the most significant bit first. The SO pin is in high impedance until the CSN pin goes to LOW. New data is shifted out at the SO pin at every rising edge of the SCLK. For further information refer to Chapter 11.1.1.

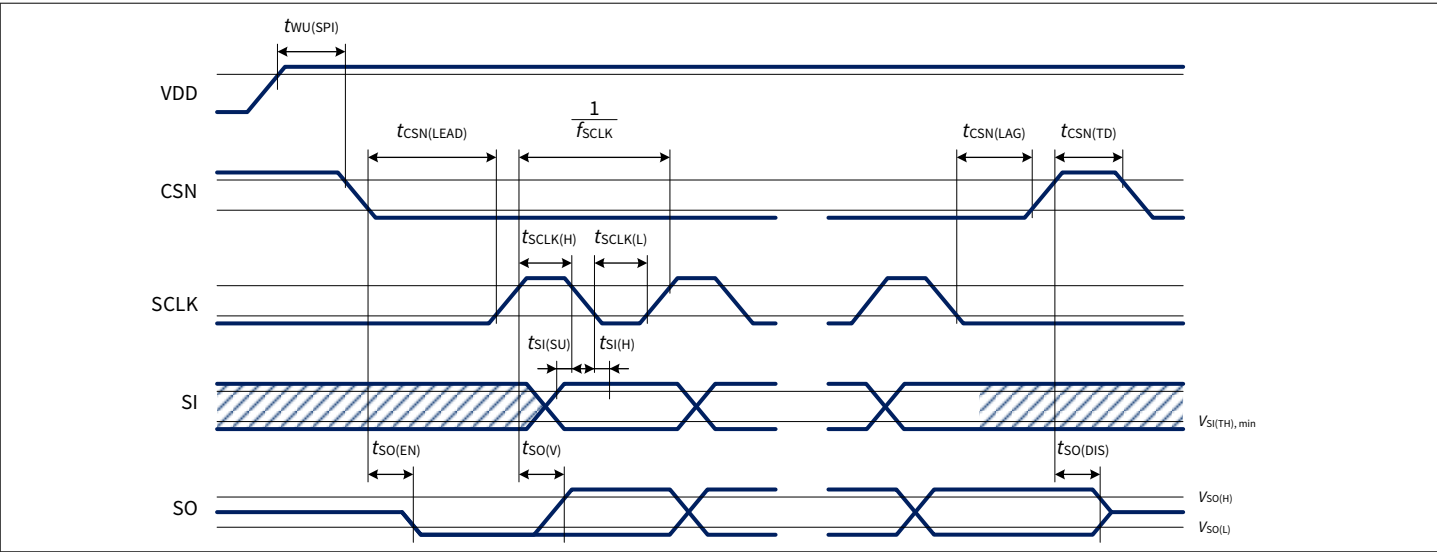


Figure 45 Timing diagram SPI access

11.1.1 SPI protocol

The relationship between SI and SO content during SPI communication is shown in Figure 46. The SI line represents the frame sent from the microcontroller and the SO line is the answer provided by the device. The “previous response” means that the frame sent back depends on the command frame received before frame A.

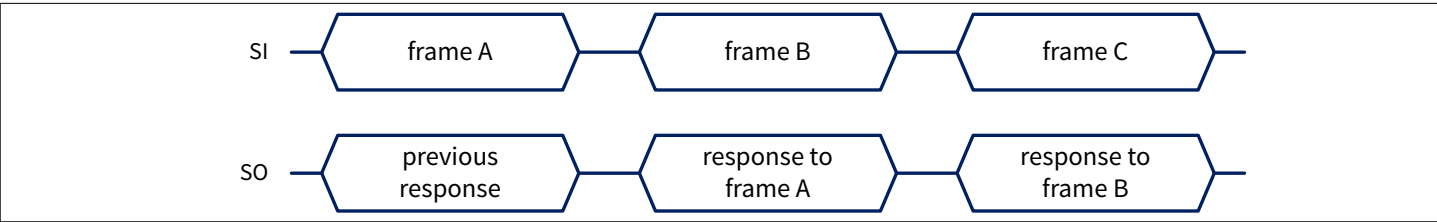


Figure 46 Relationship between SI and SO during SPI communication

The SPI protocol provides the response to a command frame only with the next transmission triggered by the microcontroller. The response to write commands is the standard diagnosis frame. To decode the response to read commands, the previous transmission has to be taken into consideration.

The sequence of commands to read and write the content of a register appears as follows:

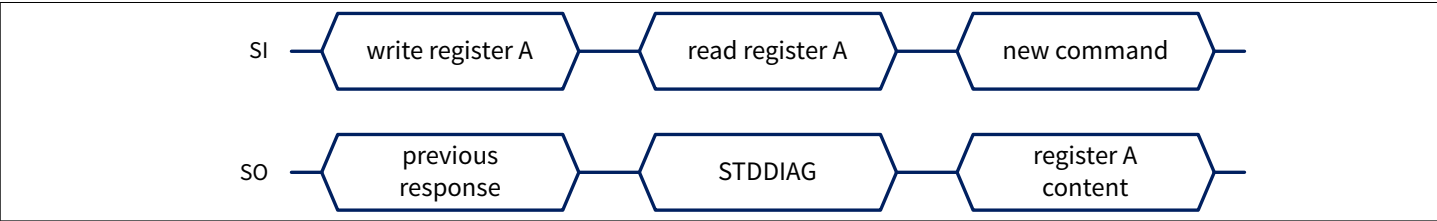


Figure 47 Register content sent back to the microcontroller

There are two specific situations where the content of the frame that is sent back to the microcontroller does not depend on the previously received frame:

- If a communication error occurred during the previously sent read or write command (for instance, the clock pulses were not multiples of 8), the device responds with the standard diagnosis (where the communication error flag is set), as shown in Figure 48
- When the device is in power-up mode (after wake-up from sleep mode) the first response is the first communication frame, as shown in Figure 49

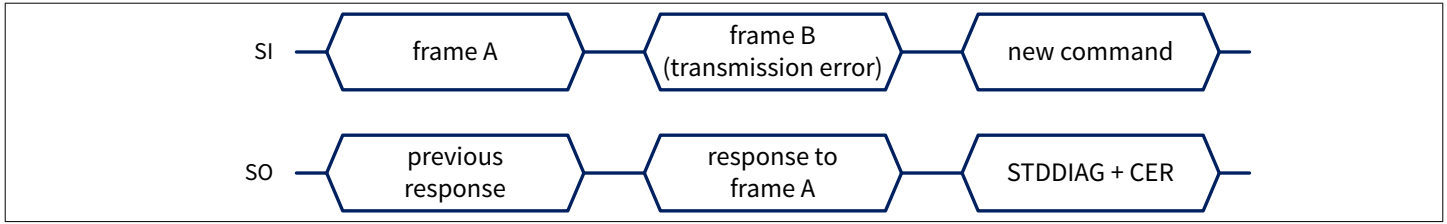


Figure 48 SPI response after an error in transmission

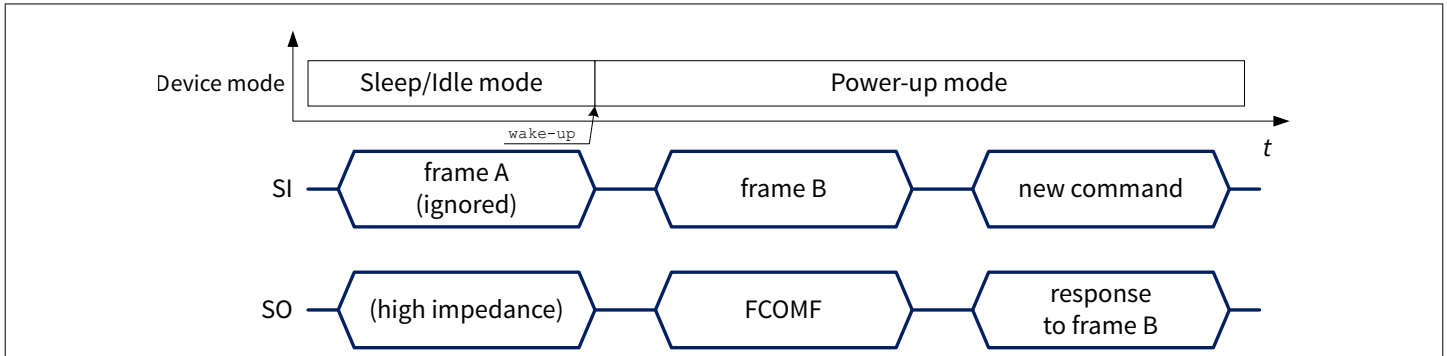


Figure 49 First SPI response in power-up mode after wake-up

11.2 SPI register reset conditions

The following conditions have an impact on the SPI register content:

When the limp home state is entered (refer to [Chapter 6.1.1.6](#)):

- Configuration and control registers are reset to their default values
- Self-check registers are reset to their default values
- The restart counter and protection latches are reset. Therefore, also the error, warning and protection flags are reset

When a reset command is executed via the digital interface:

- Configuration and control registers are reset to their default values
- Self-check registers are reset to their default values
- The protection latches are not reset. Therefore, also the error, warning, and protection flags are not reset
- The device protection counter
 - is reset if the default value of the device protection restart strategy is single latch
 - is not reset if the default value of the device protection restart strategy is counted restart

When both supply voltages drop below their corresponding undervoltage shutdown thresholds ($V_{S(UV)}$ and $V_{DD(UV)}$):

- Configuration and control registers are reset to their default values
- Self-check registers are reset to their default values
- The restart counter and protection latches are reset. Therefore, also the error, warning, and protection flags are reset

As long as the conditions for data retention (t_{RET}) are fulfilled, a subset of register content is retained, as described in the undervoltage chapter.

If the IN pin is set to LOW after a register reset, the power stage is switched OFF.

11.3 Daisy chain capability

The interface provides daisy chain capability with modulo 8-bit SPI devices.

In this configuration, several devices are activated by the same CSN signal MCSN. The SI line of one device is connected with the SO line of another device to build a chain (see [Figure 50](#)). The two ends of the chain are connected

to the output and input of the master device, MOSI and MISO respectively. The master device provides the master clock MCLK, which is connected to the SCLK line of each device in the chain.

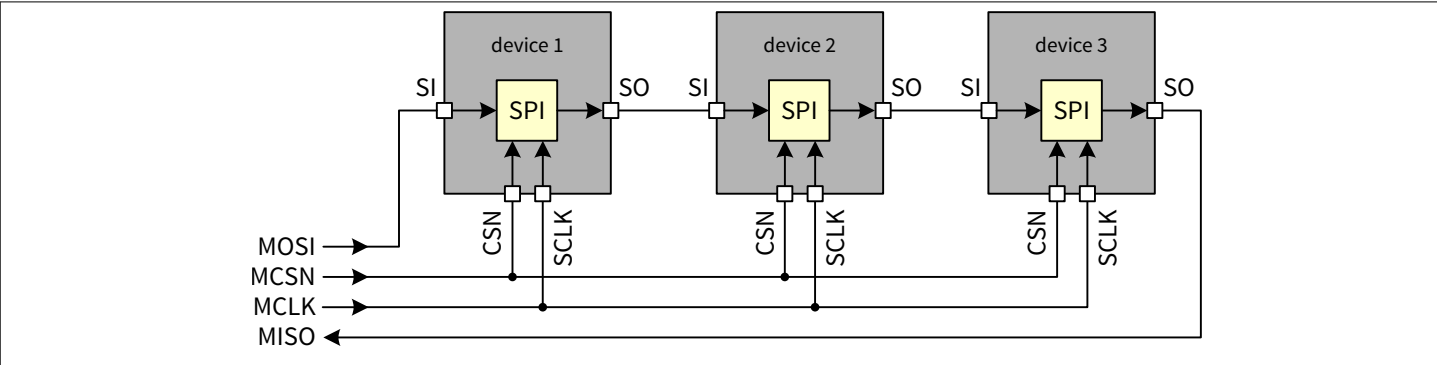


Figure 50 Daisy chain configuration

In the SPI block of each device there is one shift register, where each bit from SI line is shifted in every SCLK cycle. The bit is shifted out on the SO pin. After 24 SCLK cycles, the data transfer for one device is finished. In single chip configuration, the CSN line has to turn HIGH to make the device acknowledge the transferred data. In daisy chain configuration, the data shifted out at device 1 has been shifted in at device 2. When using three devices in a daisy chain, three times 24 bits have to be shifted through the devices. After that, the MCSN line has to turn HIGH (see [Figure 51](#)).

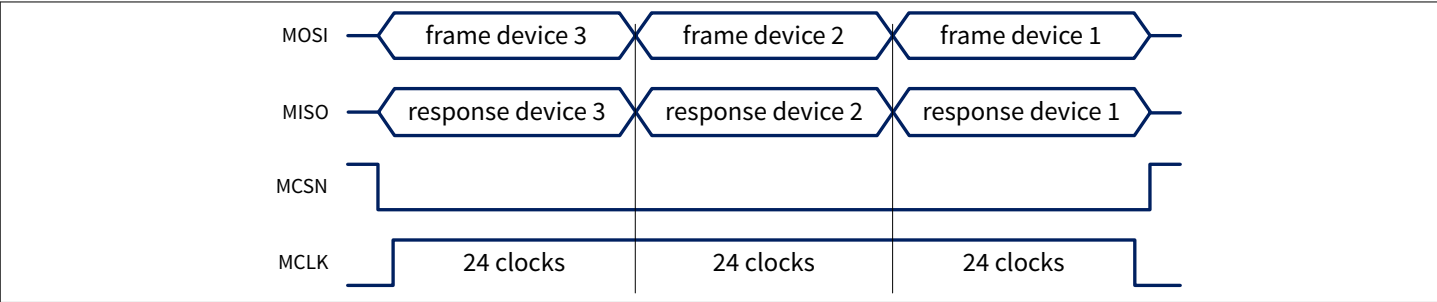


Figure 51 Data transfer in a daisy chain configuration

11.4 SPI register description

11.4.1 Read command

The content of a register is read using the RC command. For this purpose, the address of the register to be read has to be selected within the data bit fields of the RC command.

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0
RC	00 _H	A							

Table 22 Read command bit description

Field	Bits	Type	Description
A	7:0		Address of register to be read

11.4.2 Register address overview

The table below provides an overview of the available diagnosis and configuration registers including their address. Write-registers are configured by sending the corresponding address together with the data bits. For detailed information on the data bits, refer to the dedicated register description.

Table 23 **Register overview**

Name	Type	Address	Description
STDDIAG	r	01 _H	Standard diagnosis
ERRDIAG	r	03 _H	Error diagnosis
PROTDIAG	r	06 _H	Protection diagnosis
WDIAG	r	11 _H	Warning diagnosis
PSDIAG	r	18 _H	Power stage diagnosis
COMDIAG	r	1E _H	Communication diagnosis
RPSR	r	20 _H	Resistor programming status register
I2TDIAG	r	21 _H	I2t protection diagnosis
VSMR	r	25 _H	Supply voltage measurement register
TEMPMR	r	26 _H	Temperature measurement register
DCSLRR	r	29 _H	Digital current sense low range register
DCSR	r	31 _H	Digital current sense register
SCR	r/w	43 _H	Self check register
IRQCR	r/w	47 _H	IRQ control register
DIAGCR	r/w	48 _H	Diagnosis control register
DVIDR	r/w	49 _H	Device ID register
VIDR	r	4A _H	Variant device ID register
COMCR	r/w	4C _H	Communication control register
LFSC	w	4F _H	Leave fail safe command
DCR	r/w	54 _H	Device control register
OCR	r/w	55 _H	Output control register
DPR	r/w	5B _H	Device protection configuration register
I2TR	r/w	65 _H	I2t protection configuration register
OVLRL	r/w	6B _H	Overvoltage lockout register
UVLR1	r/w	6C _H	Undervoltage lockout register 1
UVLR2	r/w	6D _H	Undervoltage lockout register 2

(table continues...)

Table 23 (continued) Register overview

Name	Type	Address	Description
OCWR	r/w	6E _H	Overcurrent warning threshold register
OTWR	r/w	78 _H	Overtemperature warning threshold register
I2TWR	r/w	79 _H	I2t warning threshold register
NVMCR	r/w	7E _H	NVM mode control register
NVM_MSB	r/w	7F _H	NVM MSB register
NVM_LSB	r/w	80 _H	NVM LSB register
NVM_CMD	r/w	81 _H	NVM command register
S_DIAGCR	r	82 _H	Shadow - DIAGCR
S_DVIDR	r	83 _H	Shadow - DVIDR
S_COMCR	r	84 _H	Shadow - COMCR
S_OCR	r	87 _H	Shadow - OCR
S_DPR	r	89 _H	Shadow - DPR
S_I2TR	r	91 _H	Shadow - I2TR
S_UVLR1	r	95 _H	Shadow - UVLR1
S_UVLR2	r	96 _H	Shadow - UVLR2
S_OCWR	r	97 _H	Shadow - OCWR
FCOMF	r	FF _H	First communication frame

11.4.3 Diagnosis registers

11.4.3.1 Standard diagnosis

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
STDDIAG	01 _H	SMS	NRM	VSUV	WDS	CER	WRN	PROT	ERR	50 _H

Table 24 Standard diagnosis bit descriptions

Field	Bits	Type	Description
SMS	7	r	Safe mode status indication 0 _B (default) Device is not in a safe mode 1 _B Device is in limp home mode or fail safe mode
NMR	6	r	Normal mode indication 0 _B Device is not in one of the normal operation modes and therefore not configurable 1 _B (Default) Device is in one of the normal operation modes and configurable

(table continues...)

Table 24 (continued) Standard diagnosis bit descriptions

Field	Bits	Type	Description
VSUV	5	rc	Power supply voltage undervoltage triggered 0_B (Default) $V_S > V_{S(UV)}$ since last STDDIAG readout 1_B $V_S \leq V_{S(UV)}$ since last STDDIAG readout
WDS	4	r	Watchdog Status 0_B Watchdog is active and below overflow 1_B (default) Watchdog disabled OR overflow
CER	3	r	Communication error 0_B (default) No communication error detected 1_B Communication error detected
WRN	2	r	Warning threshold monitor 0_B (default) No warning threshold violated 1_B Warning threshold violated
PROT	1	r	Protection mechanism monitor 0_B (default) No protection mechanism triggered 1_B Protection mechanism triggered
ERR	0	r	Error monitor 0_B (default) No error 1_B Error detected and power stage latched OFF

11.4.3.2 Error diagnosis

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
ERRDIAG	03 _H	0	0	0	0	UVL_HERR	UVL_LERR	I2TERR	TMPERR	00 _H

Table 25 Error diagnosis bit descriptions

Field	Bits	Type	Description
UVL_HERR	3	r	Undervoltage lockout high error 0_B (default) No error 1_B Undervoltage lockout high triggered and device latched OFF
UVL_LERR	2	r	Undervoltage lockout low error 0_B (default) No error 1_B Undervoltage lockout low triggered and device latched OFF
I2TERR	1	r	I2t error 0_B (default) No error 1_B I2t protection triggered and device latched OFF
TMPERR	0	r	Temperature error 0_B (default) No error 1_B Temperature protection triggered ($T_{J(ABS)}$ or $T_{J(DYN)}$) and device latched OFF

11.4.3.3 Protection diagnosis

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
PROTDIAG	06 _H	0	0	dT_PROT	OT_PROT	OC_PROT	OVL_PROT	UVL_HPROT	UVL_LPROT	00 _H

Table 26 Protection diagnosis bit descriptions

Field	Bits	Type	Description
dT_PROT	5	rc	Dynamic overtemperature protection indication 0 _B No dT protection triggered ($T_{J(DYN)}$) since last PROTDIAG readout 1 _B dT protection triggered ($T_{J(DYN)}$) since last PROTDIAG readout
OT_PROT	4	rc	Absolute overtemperature protection indication 0 _B No OT protection triggered ($T_{J(ABS)}$) since last PROTDIAG readout 1 _B OT protection triggered ($T_{J(ABS)}$) since last PROTDIAG readout
OC_PROT	3	rc	Overcurrent protection indication 0 _B No current limitation triggered since last PROTDIAG readout 1 _B Current limitation triggered since last PROTDIAG readout
OVL_PROT	2	rc	Overvoltage lockout triggered 0 _B No OVL triggered since last PROTDIAG readout 1 _B OVL triggered since last PROTDIAG readout
UVL_HPROT	1	rc	Undervoltage lockout high triggered 0 _B No UVLH triggered since last PROTDIAG readout 1 _B UVLH triggered since last PROTDIAG readout
UVL_LPROT	0	rc	Undervoltage lockout low triggered 0 _B No UVLL triggered since last PROTDIAG readout 1 _B UVLL triggered since last PROTDIAG readout

11.4.3.4 Warning diagnosis

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
WDIAG	11 _H	0	0	VSW	OTW	I2TW	0	OCW	INVDIAG	00 _H

Table 27 Warning diagnosis bit descriptions

Field	Bits	Type	Description
VSW	5	rc	Supply voltage warning threshold indication 0 _B (default) $V_S > V_{S(UVLH)}$ since last WDIAG readout 1 _B $V_S \leq V_{S(UVLH)}$ since last WDIAG readout
OTW	4	rc	Overtemperature warning threshold indication 0 _B (default) $T_J < OTWTn$ since last WDIAG readout 1 _B $T_J \geq OTWTn$ since last WDIAG readout

(table continues...)

Table 27 (continued) Warning diagnosis bit descriptions

Field	Bits	Type	Description
I2TW	3	rc	I2t warning threshold indication 0_B (default) $I_{2TSn} < I_{2TWTn}$ since last WDIAG readout 1_B $I_{2TSn} \geq I_{2TWTn}$ since last WDIAG readout
OCW	1	rc	Overcurrent warning threshold indication 0_B (default) $I_L < I_{L(OCWT)}$ since last WDIAG readout 1_B $I_L \geq I_{L(OCWT)}$ since last WDIAG readout
INVDIAG	0	rc	Inverse diagnosis 0_B (default) No inverse status reporting since last WDIAG readout 1_B Inverse status reporting triggered since last WDIAG readout

11.4.3.5 Power stage diagnosis

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
PSDIAG	18 _H	0	RCS			RON_ACK	PSC	OFFDIAG	ONDIAG	02 _H

Table 28 Power stage diagnosis bit descriptions

Field	Bits	Type	Description
RCS	6:4	r	Restart counter status 000_B (default) Restart counter is zero 001_B Restart counter is 1 ... 101_B Restart counter is 5 and the device is latched OFF 110_B and 111_B n.a.
RON_ACK	3	r	$R_{DS(ON)}$ acknowledgement 0_B (default) Power stage is not in $R_{DS(ON)}$ 1_B Power stage is in $R_{DS(ON)}$
PSC	2	r	Power stage control diagnosis 0_B (default) Power stage control = LOW 1_B Power stage control = HIGH
OFFDIAG	1	r	OFF-state diagnosis 0_B V_{OUT} to GND pin $> V_{OUT(OFF)}$ 1_B (default) V_{OUT} to GND pin $\leq V_{OUT(OFF)}$
ONDIAG	0	r	ON-state diagnosis 0_B (default) $V_{DS} > V_{DS(ON)}$ 1_B $V_{DS} \leq V_{DS(ON)}$

11.4.3.6 Communication diagnosis

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
COMDIAG	1E _H	0	IN	LHI	VDDUV	WDERR	RAERR	MCERR	0	00 _H

Table 29 Communication diagnosis bit descriptions

Field	Bits	Type	Description
IN	6	rc	Input pin monitor 0 _B (default) always LOW level at IN pin since last COMDIAG readout 1 _B HIGH level at IN pin at least once since last COMDIAG readout
LHI	5	rc	Limp home input pin monitor 0 _B (default) always LOW level at LHI pin since last COMDIAG readout 1 _B HIGH level at LHI pin at least once since last COMDIAG readout
VDDUV	4	rc	Digital supply voltage undervoltage triggered 0 _B (default) $V_{DD} > V_{DD(UV)}$ since last COMDIAG readout 1 _B $V_{DD} \leq V_{DD(UV)}$ at least once since last COMDIAG readout
WDERR	3	rc	Watchdog error 0 _B (default) No error since last COMDIAG readout 1 _B Watchdog overflow occurred since last COMDIAG readout
RAERR	2	rc	Register access error 0 _B (default) No error since last COMDIAG readout 1 _B Read or write access to a non-existent register or write to a read-only register, since last COMDIAG readout. The device responds with the STDDIAG
MCERR	1	rc	Modulo counter error 0 _B (default) No modulo counter error since last COMDIAG readout 1 _B Modulo counter error occurred since last COMDIAG readout

11.4.3.7 Resistor programming status register

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
RPSR	20 _H	RI2T				ROCT				

Table 30 Resistor programming status register bit descriptions

Field	Bits	Type	Description
RI2T	7:4	r	R_{I2t} value 0000 _B I2t pin short ($R_{I2t} \leq R_{I2t_SHORT}$) - I2t protection curve 6 0001 _B $R_{I2t} = R_{I2t_1}$: protection curve 1 0010 _B $R_{I2t} = R_{I2t_2}$: protection curve 2 0011 _B $R_{I2t} = R_{I2t_3}$: protection curve 3 0100 _B $R_{I2t} = R_{I2t_4}$: protection curve 4 0101 _B $R_{I2t} = R_{I2t_5}$: protection curve 5 0110 _B $R_{I2t} = R_{I2t_6}$: protection curve 6 0111 _B I2t pin open ($R_{I2t} \geq R_{I2t_OPEN}$) - I2t protection curve 6
ROCT	3:0	r	R_{OCT} value 0000 _B OCT pin short ($R_{OCT} \leq R_{OCT_SHORT}$): $I_{L(OCT_H)} = I_{L(HOCT_H)}$ 0001 _B $R_{OCT} = R_{OCT_1}$: $I_{L(OCT_H)} = I_{L(LOCT_H)} + 0 \cdot I_{L(OCT_H_LSB)}$ 0010 _B $R_{OCT} = R_{OCT_2}$: $I_{L(OCT_H)} = I_{L(LOCT_H)} + 4 \cdot I_{L(OCT_H_LSB)}$ 0011 _B $R_{OCT} = R_{OCT_3}$: $I_{L(OCT_H)} = I_{L(LOCT_H)} + 8 \cdot I_{L(OCT_H_LSB)}$ 0100 _B $R_{OCT} = R_{OCT_4}$: $I_{L(OCT_H)} = I_{L(LOCT_H)} + 12 \cdot I_{L(OCT_H_LSB)}$ 0101 _B $R_{OCT} = R_{OCT_5}$: $I_{L(OCT_H)} = I_{L(LOCT_H)} + 16 \cdot I_{L(OCT_H_LSB)}$ 0110 _B $R_{OCT} = R_{OCT_6}$: $I_{L(OCT_H)} = I_{L(LOCT_H)} + 20 \cdot I_{L(OCT_H_LSB)}$ 0111 _B $R_{OCT} = R_{OCT_7}$: $I_{L(OCT_H)} = I_{L(LOCT_H)} + 24 \cdot I_{L(OCT_H_LSB)}$ 1000 _B $R_{OCT} = R_{OCT_8}$: $I_{L(OCT_H)} = I_{L(LOCT_H)} + 28 \cdot I_{L(OCT_H_LSB)}$ 1001 _B OCT pin open ($R_{OCT} \geq R_{OCT_OPEN}$): $I_{L(OCT_H)} = I_{L(HOCT_H)}$

11.4.3.8 I2t protection diagnosis

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
I2TDIAG	21 _H	I2TS								00 _H

Table 31 I2t protection diagnosis bit descriptions

Field	Bits	Type	Description
I2TS	7:0	r	I2t protection status 0000 0000 _B (default) $S_{I2t} = 0\%$ or invalid measurement Curve 1: 0x00 _H - 0x41 _H ($S_{I2t} = 100\%$) Curve 2: 0x00 _H - 0x51 _H ($S_{I2t} = 100\%$) Curve 3: 0x00 _H - 0x67 _H ($S_{I2t} = 100\%$) Curve 4: 0x00 _H - 0x82 _H ($S_{I2t} = 100\%$) Curve 5: 0x00 _H - 0xA4 _H ($S_{I2t} = 100\%$) Curve 6: 0x00 _H - 0xCF _H ($S_{I2t} = 100\%$)

11.4.3.9 Supply voltage measurement register

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
VSMR	25 _H	VS								00 _H

Table 32 Supply voltage measurement register bit descriptions

Field	Bits	Type	Description
VS	7:0	r	Supply voltage measurement register $V_S = VS_{\text{decimal}} \cdot V_{S(\text{LSB})}$ for $32 \leq VS_{\text{decimal}} \leq 220$ 0000 0000 _B (default) invalid measurement

11.4.3.10 Temperature measurement register

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
TEMPMR	26 _H	0	0				DEVT			00 _H

Table 33 Temperature measurement register bit descriptions

Field	Bits	Type	Description
DEVT	5:0	r	Device temperature measurement $T_{\text{DEV}} = -40^{\circ}\text{C} + \text{DEVT}_{\text{decimal}} \cdot T_{\text{DEV}(\text{LSB})}$ 00 0000 _B (default) $T_{\text{DEV}} = -40^{\circ}\text{C}$ or invalid measurement

11.4.3.11 Digital current sense low range register

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
DCSLRR	29 _H									FF _H

Table 34 Digital current sense low range register bit descriptions

Field	Bits	Type	Description
DCSLR	7:0	r	Digital current sense low range 0000 0000 _B low range measurement running 0000 0001 _B ... 1001 0110 _B $I_L = I_{\text{DCSLR}(\text{LSB})} \cdot \text{DCSLR}_{\text{decimal}}$ 1001 0111 _B ... 1111 1110 _B not available 1111 1111 _B (default) Invalid measurement

11.4.3.12 Digital current sense register

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
DCSR	31 _H									00 _H

Table 35 Digital current sense register bit descriptions

Field	Bits	Type	Description
DCS	7:0	r	Digital current sense $I_L = I_{\text{DCS}(\text{LSB})} \cdot \text{DCS}_{\text{decimal}}$ 0000 0000 _B (default) 0 A or invalid measurement

11.4.3.13 Variant ID register

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
VIDR	4A _H	0	0	0	VID					1F _H

Table 36 Variant ID register bit descriptions

Field	Bits	Type	Description
VID	4:0	r	Variant ID 1 1111 _B Variant = BTS80xxx-SWPF-1ES Other values internal fault / invalid variant

11.4.4 Self-check register

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
SCR	43 _H	0	0	INTFAUL T	ON2OFF DIAG	0	0	IRQSC	ON2OFF SC	00 _H

Table 37 Self-check register bit descriptions

Field	Bits	Type	Description
INTFAULT	5	r	Internal fault indication 0 _B (default) No internal fault detected 1 _B Internal fault detected and device is probably unreliable
ON2OFFDIAG	4	r	ON to OFF diagnosis 0 _B (default) Last ON to OFF self-check abortive, or no self-check requested 1 _B Last ON to OFF self-check successful
IRQSC	1	r/w	IRQ self-check 0 _B (default) IRQ pin follows device configuration 1 _B IRQ pin is forced to HZ
ON2OFFSC	0	r/w	ON to OFF switchability self-check Register read: 0 _B (default) No self-check in execution or already finished 1 _B Self-check in execution Register write: 0 _B (default) No self-check requested 1 _B The device starts to switch OFF until $V_{DS} > V_{DS(ON)}$ then it switches ON again automatically

11.4.5 Control registers

11.4.5.1 IRQ control register

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
IRQCR	47 _H	0	IRQIN VDIAG	IRQVDD UV	IRQWWD	IRQWVS	IRQWI2T	IRQWOC	IRQWOT	00 _H

Table 38 IRQ control register bit descriptions

Field	Bits	Type	Description
IRQINVDIAG	6	r/w	Inverse diagnosis warning on IRQ pin 0 _B (default) Disabled 1 _B Warning enabled
IRQVDDUV	5	r/w	VDD undervoltage warning on IRQ pin 0 _B (default) Disabled 1 _B Warning enabled
IRQWWD	4	r/w	Watchdog warning on IRQ pin 0 _B (default) Disabled 1 _B Warning enabled
IRQWVS	3	r/w	Supply voltage indication on IRQ pin 0 _B (default) Disabled 1 _B Warning threshold violation, UVL and OVL protection indication enabled
IRQWI2T	2	r/w	I2t warning on IRQ pin 0 _B (default) Disabled 1 _B Warning threshold violation indication enabled
IRQWOC	1	r/w	Overcurrent indication on IRQ pin 0 _B (default) Disabled 1 _B Warning threshold violation and overcurrent protection indication enabled
IRQWOT	0	r/w	Overtemperature indication on IRQ pin 0 _B (default) Disabled 1 _B Warning threshold violation and overtemperature protection indication enabled

11.4.5.2 Diagnosis control register

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
DIAGCR	48 _H	0	0	0	LRSOC	AMUX				0F _H

Table 39 Diagnosis control register bit descriptions

Field	Bits	Type	Description
LRSOC	4	w	Digital current sense low range start of conversion 0 _B (default) Digital current sense low range measurement not triggered 1 _B Start of digital current sense low range measurement
AMUX	3:0	r/w	Analog Multiplexer 0000 _B Analog current sense of OUT0 is routed to IS pin 0001 _B Reserved ... 1101 _B Reserved 1110 _B Sense verification mode 1111 _B (default) IS pin is high impedance

11.4.5.3 Communication control register

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
COMCR	4C _H	0	WD			FSOUT		CRCEN	RST	06 _H

Table 40 Communication control register bit descriptions

Field	Bits	Type	Description
WD	6:4	r/w	Watchdog time 000 _B (default) Watchdog disabled 001 _B $t_{WD(TH)} = t_{WD1}$ 010 _B $t_{WD(TH)} = t_{WD2}$ 011 _B $t_{WD(TH)} = t_{WD3}$ 100 _B $t_{WD(TH)} = t_{WD4}$ 101 _B $t_{WD(TH)} = t_{WD5}$ 110 _B $t_{WD(TH)} = t_{WD6}$ 111 _B $t_{WD(TH)} = t_{WD7}$
FSOUT	3:2	r/w	Power stage control in fail safe mode 00 _B Power stage control = LOW 01 _B (default) Power stage control = "last state" 10 _B Power stage control = "last state" 11 _B Power stage control = HIGH
CRCEN	1	r/w	CRC enable 0 _B CRC disabled 1 _B (default) CRC enabled
RST	0	r/w	Register reset 0 _B (default) Normal operation 1 _B Execute register reset command

11.4.5.4 Leave fail safe command

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
LFSC	4F _H	LFS								00 _H

Table 41 Leave fail safe command bit descriptions

Field	Bits	Type	Description
LFS	7:0	w	Leave fail safe mode 1100 0111 _B command to leave fail safe mode

11.4.5.5 Device control register

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
DCR	54 _H	0	0	ICOL		CL	VSUVSE L	MSEL		00 _H

Table 42 Device control register bit descriptions

Field	Bits	Type	Description
ICOL	5:4	r/w	Input control logic 00 _B (default) Input status is or-combined with OUT bit 01 _B Input status is and-combined with OUT bit 10 _B OUT bit only 11 _B N.a.
CL	3	r/w	Clear latch 0 _B (default) Protection latch and restart counter are untouched 1 _B Protection latch and restart counter are reset
VSUVSEL	2	r/w	Undervoltage shutdown level selection 0 _B (default) $V_{S(UV)} = V_{S(UV)_H}$ 1 _B $V_{S(UV)} = V_{S(UV)_L}$
MSEL	1:0	r/w	Mode selection 00 _B (default) Sleep mode 01 _B Normal modes 10 _B Idle mode 11 _B N.a.

11.4.5.6 Output control register

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
OCR	55 _H	0	0	0	0	0	FASTOFF	CLS	OUT	00 _H

Table 43 Output control register bit descriptions

Field	Bits	Type	Description
FASTOFF	2	r/w	Fast OFF control 0 _B (default) Use standard switch-OFF time 1 _B Use $t_{OFF(FAST)}$ switch-OFF time
CLS	1	r/w	Capacitive load switching 0 _B (default) CLS sub-mode deactivated 1 _B CLS sub-mode entered at next power stage activation
OUT	0	r/w	Output control 0 _B (default) Output control = LOW 1 _B Output control = HIGH

11.4.6 Configuration registers

11.4.6.1 Device ID register

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
DVIDR	49 _H	0	0	0	0	DVID				00 _H

Table 44 Device ID register bit descriptions

Field	Bits	Type	Description
DVID	3:0	r/w	Device ID 0000 _B (default) Device ID = 0 ... 1111 _B Device ID = 15

11.4.6.2 Device protection configuration register

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
DPR	5B _H	0	0	DPREN			OCT			1F _H

Table 45 Device protection configuration register bit descriptions

Field	Bits	Type	Description
DPREN	5	r/w	Device protection restart enable 0 _B (default) Single latch 1 _B Restart counter enabled
OCT	4:0	r/w	Overcurrent threshold high $I_{L(OCT_H)} = I_{L(LOCT_H)} + OCT_{decimal} I_{L(OCT_H_LSB)}$ 1 1111 _B (default) $I_{L(OCT_H)} = I_{L(HOCT_H)}$

11.4.6.3 I2t protection configuration register

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
I2TR	65 _H	0	0	TAU		0		DC		27 _H

Table 46 I2t protection configuration register bit descriptions

Field	Bits	Type	Description
TAU	5:4	r/w	Time constant of I2t protection 00 _B $\tau = \tau_{I2t_1}$ selected 01 _B $\tau = \tau_{I2t_2}$ selected 10 _B (default) $\tau = \tau_{I2t_3}$ selected 11 _B $\tau = \tau_{I2t_4}$ selected
DC	2:0	r/w	DC current of I2t protection 000 _B I2t protection is disabled 001 _B I2t curve 1 with $I_{L(I2t_1)}$ 010 _B I2t curve 2 with $I_{L(I2t_2)}$ 011 _B I2t curve 3 with $I_{L(I2t_3)}$ 100 _B I2t curve 4 with $I_{L(I2t_4)}$ 101 _B I2t curve 5 with $I_{L(I2t_5)}$ 110 _B I2t curve 6 with $I_{L(I2t_6)}$ 111 _B (default) n.a. (I2t curve 6 is used)

11.4.6.4 Overvoltage lockout register

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
OVLR	6B _H	0	OVLF			OVLEN	OVL			27 _H

Table 47 Overvoltage lockout register 1 - bit descriptions

Field	Bits	Type	Description
OVLF	6:4	r/w	Overvoltage lockout filter time 000 _B Filter time set to 35 μs 001 _B Filter time set to 98 μs 010 _B (default) Filter time set to 200 μs 011 _B Filter time set to 540 μs 100 _B Filter time set to 1.04 ms 101 _B Filter time set to 10 ms 110 _B Filter time set to 50 ms 111 _B Filter time set to 100 ms
OVLEN	3	r/w	Overvoltage lockout enable 0 _B (default) $V_{S(OVL)}$ disabled 1 _B $V_{S(OVL)}$ enabled
OVL	2:0	r/w	Overvoltage lockout threshold 000 _B Threshold set to 17.89 V 001 _B Threshold set to 18.76 V 010 _B Threshold set to 19.64 V 011 _B Threshold set to 20.51 V 100 _B Threshold set to 21.38 V 101 _B Threshold set to 22.25 V 110 _B Threshold set to 23.13 V 111 _B (default) Threshold set to 24.00 V

11.4.6.5 Undervoltage lockout register 1

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
UVLR1	6C _H	UVL_HF			UVL_HEN	UVL_H				50 _H

Table 48 Undervoltage lockout register 1 - bit descriptions

Field	Bits	Type	Description
UVL_HF	7:5	r/w	Undervoltage lockout high filter time 000 _B Filter time set to 35 μ s 001 _B Filter time set to 100 μ s 010 _B (default) Filter time set to 200 μ s 011 _B Filter time set to 500 μ s 100 _B Filter time set to 1 ms 101 _B Filter time set to 10 ms 110 _B Filter time set to 50 ms 111 _B Filter time set to 100 ms
UVL_HEN	4	r/w	Undervoltage lockout high enable 0 _B $V_{S(UVL_H)}$ disabled 1 _B (default) $V_{S(UVL_H)}$ enabled
UVL_H	3:0	r/w	Undervoltage lockout high threshold 0000 _B (default) Threshold set to 7.53 V 0001 _B Threshold set to 7.75 V 0010 _B Threshold set to 7.96 V 0011 _B Threshold set to 8.18 V 0100 _B Threshold set to 8.40 V 0101 _B Threshold set to 8.62 V 0110 _B Threshold set to 8.84 V 0111 _B Threshold set to 9.05 V 1000 _B Threshold set to 9.27 V 1001 _B Threshold set to 9.49 V 1010 _B Threshold set to 9.71 V 1011 _B Threshold set to 9.93 V 1100 _B Threshold set to 10.15 V 1101 _B Threshold set to 10.36 V 1110 _B Threshold set to 10.58 V 1111 _B Threshold set to 10.80 V

11.4.6.6 Undervoltage lockout register 2

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
UVLR2	6D _H	CDEN	UVL_HREN	UVL_LREN	UVL_LEN	UVL_L				B0 _H

Table 49 Undervoltage lockout register 2 - bit descriptions

Field	Bits	Type	Description
CDEN	7	r/w	Current dependency enable 0_B $V_{S(UVL_H)}$ is always active 1_B (default) $V_{S(UVL_H)}$ is active when $I_L > I_{L(OCWT)}$
UVL_HREN	6	r/w	Undervoltage lockout high restart enable 0_B (default) Single latch 1_B Unlimited restart
UVL_LREN	5	r/w	Undervoltage lockout low restart enable 0_B Single latch 1_B (default) Unlimited restart
UVL_LEN	4	r/w	Undervoltage lockout low enable 0_B $V_{S(UVL_L)}$ disabled 1_B (default) $V_{S(UVL_L)}$ enabled
UVL_L	3:0	r/w	Undervoltage lockout low threshold 0000_B (default) Threshold set to 4.25 V 0001_B Threshold set to 4.47 V 0010_B Threshold set to 4.69 V 0011_B Threshold set to 4.91 V 0100_B Threshold set to 5.13 V 0101_B Threshold set to 5.35 V 0110_B Threshold set to 5.56 V 0111_B Threshold set to 5.78 V 1000_B Threshold set to 6.00 V 1001_B Threshold set to 6.22 V 1010_B Threshold set to 6.44 V 1011_B Threshold set to 6.65 V 1100_B Threshold set to 6.87 V 1101_B Threshold set to 7.09 V 1110_B Threshold set to 7.31 V 1111_B Threshold set to 7.53 V

11.4.6.7 Overcurrent warning threshold register

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
OCWR	$6E_H$	0	0	0	OCWT					$1F_H$

Table 50 Overcurrent warning threshold register bit descriptions

Field	Bits	Type	Description
OCWT	4:0	r/w	Overcurrent warning threshold 0 0000 _B $I_{L(OCWT)} = 0\text{ A}$ Stepsize with 5.328 A 1 1111 _B (default) $I_{L(OCWT)} = 165.168\text{ A}$

11.4.6.8 Overtemperature warning threshold register

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
OTWR	78 _H	0	0	OTWT						38 _H

Table 51 Overtemperature warning threshold register bit descriptions

Field	Bits	Type	Description
OTWT	5:0	r/w	Overtemperature warning threshold 00 0000 _B N.a. ... 00 1111 _B N.a. 01 0000 _B OTWT = 13.8°C ... stepsize with 3.36 K 11 1000 _B (default) OTWT = 148.1°C 11 1001 _B N.a. ... 11 1111 _B N.a.

11.4.6.9 I2t warning threshold register

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
I2TWR	79 _H	I2TWT								FF _H

Table 52 I2t warning threshold register bit descriptions

Field	Bits	Type	Description
I2TWT	7:0	r/w	I2t warning threshold Curve 1: from 0x00 _H (0%) to 0x41 _H (100%) Curve 2: from 0x00 _H (0%) to 0x51 _H (100%) Curve 3: from 0x00 _H (0%) to 0x67 _H (100%) Curve 4: from 0x00 _H (0%) to 0x82 _H (100%) Curve 5: from 0x00 _H (0%) to 0xA4 _H (100%) Curve 6: from 0x00 _H (0%) to 0xCF _H (100%)

11.4.7 NVM register

11.4.7.1 NVM mode control

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
NVM	7E _H	0	0	0	0	0	0	0	NVM_SE L	00 _H

Table 53 NVM mode control bit descriptions

Field	Bits	Type	Description
NVM_SEL	0	w	Select NVM mode 0 _B Leave NVM mode is requested, load default values triggered (default) 1 _B Enter NVM mode is requested

11.4.7.2 NVM MSB of word line

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
NVM_MSB	7F _H	WL_A				WL_D_MSB				–

Table 54 NVM MSB of word line bit descriptions

Field	Bits	Type	Description
WL_A	7:5	rw	Word line address 000 _B - 011 _B See NVM description
WL_D_MSB	4:0	rw	MSB of word line data Data for D12 to D8 of corresponding word line address

11.4.7.3 NVM LSB of word line

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
NVM_LSB	80 _H	WL_D_LSB								–

Table 55 NVM LSB of word line bit descriptions

Field	Bits	Type	Description
WL_D_LSB	7:0	rw	LSB of word line data Data for D7 to D0 of corresponding word line address

11.4.7.4 NVM command register

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
NVM_CMD	81 _H	VS_NVM_UV	NVM_FULL	ACS_ER_R	WLA_ER_R	VIRGIN	READY	0	R/W	0C _H

Table 56 NVM command register bit descriptions

Field	Bits	Type	Description
VS_NVM_UV	7	r	Undervoltage during NVM operation 0 _B $V_S < V_{S(NVM)}$ during write command or $V_S \leq V_{S(PU)}$ during read command 1 _B (default) $V_S = V_{S(NVM)}$ during write command or $V_S > V_{S(PU)}$ during read command
NVM_FULL	6	r	NVM is full 0 _B (default) At least one word line can be written 1 _B NVM is full

(table continues...)

Table 56 (continued) NVM command register bit descriptions

Field	Bits	Type	Description
ACS_ERR	5	r	Access error 0 _B (default) No access error occurred 1 _B write to NVM is requested from outside the NVM mode
WLA_ERR	4	r	Word line access error 0 _B (default) Last write command addressed valid word line (NVM_MSB.WL_A = valid) 1 _B Last write command addressed invalid word line (NVM_MSB.WL_A = invalid)
VIRGIN	3	r	NVM virgin check 0 _B At least one word line was written to NVM 1 _B (default) NVM is virgin
READY	2	r	Ready check 0 _B NVM is not ready to read or write (read or write is ongoing) 1 _B (default) NVM is ready for next read or write command
R/W	0	r/w	Read or write access Register read: 0 _B (default) Last command was a read command 1 _B Last command was a write command Register write: 0 _B (default) Read out NVM and load data to shadow register 1 _B Write data from NVM_MSB and NVM_LSB into NVM

11.4.8 Shadow registers

11.4.8.1 Shadow - DIAGCR

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_DIAGCR	82 _H	0	0	0	0	AMUX				–

Table 57 Shadow - DIAGCR bit descriptions

Field	Bits	Type	Description
AMUX	3:0	r	Default value of DIAGCR.AMUX

11.4.8.2 Shadow - DVIDR

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_DVIDR	83 _H	0	0	0	0	DVID				–

Table 58 Shadow - DVIDR bit descriptions

Field	Bits	Type	Description
DVID	3:0	r	Default value of DVIDR.DVID

11.4.8.3 Shadow - COMCR

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_COMCR	84 _H	0	WD			FSOUT		CRCEN	RST_TIE 0	–

Table 59 Shadow - COMCR bit descriptions

Field	Bits	Type	Description
WD	6:4	r	Default value of COMCR.WD
FSOUT	3:2	r	Default value of COMCR.FSOUT
CRCEN	1	r	Default value of COMCR.CRCEN
RST_TIE0	0	r	Default value of COMCR.RST

11.4.8.4 Shadow - OCR

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_OCR	87 _H	0	0	0	0	0	FASTOF F_TIE0	CLS	OUT_TI E0	–

Table 60 Shadow - OCR bit descriptions

Field	Bits	Type	Description
FASTOFF_TIE 0	2	r	Default value of OCR.FASTOFF
CLS	1	r	Default value of OCR.CLS
OUT_TIE0	0	r	Default value of OCR.OUT

11.4.8.5 Shadow - DPR

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_DPR	89 _H	0	0	DPREN	OCT					–

Table 61 Shadow - DPR register bit descriptions

Field	Bits	Type	Description
DPREN	5	r	Default value of DPR.DPREN
OCT	4:0	r	Default value of DPR.OCT

11.4.8.6 Shadow - I2TR

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_I2TR	91 _H	0	0	TAU		0	DC			–

Table 62 Shadow - I2TR bit descriptions

Field	Bits	Type	Description
TAU	5:4	r	Default value of I2TR.TAU

(table continues...)

Table 62 (continued) Shadow - I2TR bit descriptions

Field	Bits	Type	Description
DC	2:0	r	Default value of I2TR.DC

11.4.8.7 Shadow - UVLR1

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_UVLR1	95 _H	UVL_HF			UVL_HEN	UVL_H				–

Table 63 Undervoltage lockout register 1 bit descriptions

Field	Bits	Type	Description
UVL_HF	7:5	r	Default value of UVLR1.UVL_HF
UVL_HEN	4	r	Default value of UVLR1.UVL_HEN
UVL_H	3:0	r	Default value of UVLR1.UVL_H

11.4.8.8 Shadow - UVLR2

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_UVLR2	96 _H	CDEN	UVL_HREN	UVL_LREN	UVL_LEN	UVL_L				–

Table 64 Shadow - UVLR2 bit descriptions

Field	Bits	Type	Description
CDEN	7	r	Default value of UVLR2.CDEN
UVL_HREN	6	r/w	Default value of UVLR2.UVL_HREN
UVL_LREN	5	r/w	Default value of UVLR2.UVL_LREN
UVL_LEN	4	r/w	Default value of UVLR2.UVL_LEN
UVL_L	3:0	r/w	Default value of UVLR2.UVL_L

11.4.8.9 Shadow - OCWR

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_OCWR	97 _H	0	0	0	OCWT					–

Table 65 Shadow - OCWR bit descriptions

Field	Bits	Type	Description
OCWT	4:0	r	Default value of OCWR.OCWT

11.4.9 First communication frame

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
FCOMF	FF _H	IN	MINFO2	MINFO1	MINFO0	VDDUV	VSUV	PROT	ERR	00 _H

Table 66 First communication frame bit descriptions

Field	Bits	Type	Description
IN	7	r	Input pin monitor 0 _B (default) LOW level at pin IN 1 _B HIGH level at pin IN
MINFOn n = 2 to 0	6:4	r	Mode information 000 _B (default) Device is in one of the normal modes 001 _B Device is in limp home mode 010 _B Device is in fail safe mode 011 _B Device is in NVM mode 100 _B N.a. 101 _B Device is in power-up mode coming from idle mode 110 _B Device is in power-up mode coming from sleep mode 111 _B Device is in power-up mode after V_S undervoltage event for $t < t_{RET}$
VDDUV	3	r	Digital supply voltage undervoltage triggered 0 _B (default) $V_{DD} > V_{DD(UV)}$ since last COMDIAG readout 1 _B $V_{DD} \leq V_{DD(UV)}$ at least once since last COMDIAG readout
VSUV	2	r	Power supply voltage undervoltage triggered 0 _B (Default) $V_S > V_{S(UV)}$ since last STDDIAG readout 1 _B $V_S \leq V_{S(UV)}$ since last STDDIAG readout
PROT	1	r	Protection mechanism monitor 0 _B (Default) No protection mechanism triggered 1 _B Protection mechanism triggered
ERR	0	r	Error monitor 0 _B (Default) No error 1 _B Error detected and power stage latched OFF

11.5 **Cyclic redundancy check (CRC)**

The device provides an 8-bit cyclic redundancy check (CRC) for each SPI transmission, which complies with SAE CRC-8 (SAE-J1850).

The 8-bit CRC follows the following definitions:

Table 67 SAE-J1850 CRC8 standard

CRC result width	8 bits
Polynomial	0x1D
Initial value	0xFF
Input data reflected	No
Result data reflected	No
Final XOR value	0xFF
Check	0x4B
Magic check	0xC4

The CRC is calculated with 24-bit input data, consisting of the device ID out of the device ID register, the address of the received or transmitted command, and the data bits of the dedicated command. The order of the input data is as follows: {dev_id[23:16], address [15:8], data[7:0]}. As an example, the table below shows the CRC calculation of the output control command with CLS enable and power stage enable for a device with device ID set to 0x01.

The device ID register can also be read with invalid CRC to provide input for the CRC calculation.

Table 68 CRC- calculation example

Byte name	Value
Device ID	0x01
Address	0x55
Data	0x03
CRC input	0x01 0x55 0x03
CRC result	0x66

By default, the CRC is enabled when the device is powered up. However, it can be disabled via the digital interface. The default of the CRC enable bit can be set via NVM programming, as described in [Chapter 12](#).

In any condition where the device is in power-up, with duration less than or equal to t_{PU} , the CRC has to be calculated by using the device ID value of 0x00.

If the CRC is disabled, any CRC is accepted on the SI line, even if it is wrong. However, the full 24-bit communication frame has to be sent on the SI line to fulfill the 24-bit frame length. Independent of the CRC enable/disable setting, the device sends the calculated CRC to the SO line.

If the device is used in a daisy chain configuration, the CRC has to be calculated separated for each device, as shown in the figure below.

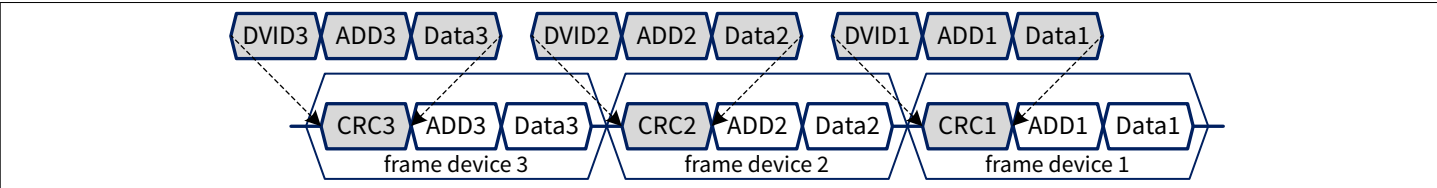


Figure 52 CRC in a daisy chain configuration

11.6 Communication watchdog

The device offers a communication watchdog to enable an improvement of the system integrity. This feature monitors the communication over the digital interface. If communication is missing or invalid, the function is activated and the device executes a configurable failure behavior.

By default, the communication watchdog is disabled. It can be enabled in inactive mode and active mode by setting the watchdog threshold time ($t_{WD(TH)}$) via the digital interface to one of the available watchdog times (t_{WDx}), as described in [Chapter 11.4.5.3](#).

In addition, the default configuration of the communication watchdog can be changed via NVM programming, as described in [Chapter 12](#).

As soon as the communication watchdog is enabled, the internal watchdog counter starts.

The internal watchdog counter is reset to zero with each valid SPI communication frame.

As soon as the internal watchdog counter exceeds the configured watchdog threshold time ($t_{WD(TH)}$), a watchdog overflow occurs.

The watchdog overflow is indicated in the standard diagnosis, communication diagnosis, and on the IRQ pin (if it is enabled).

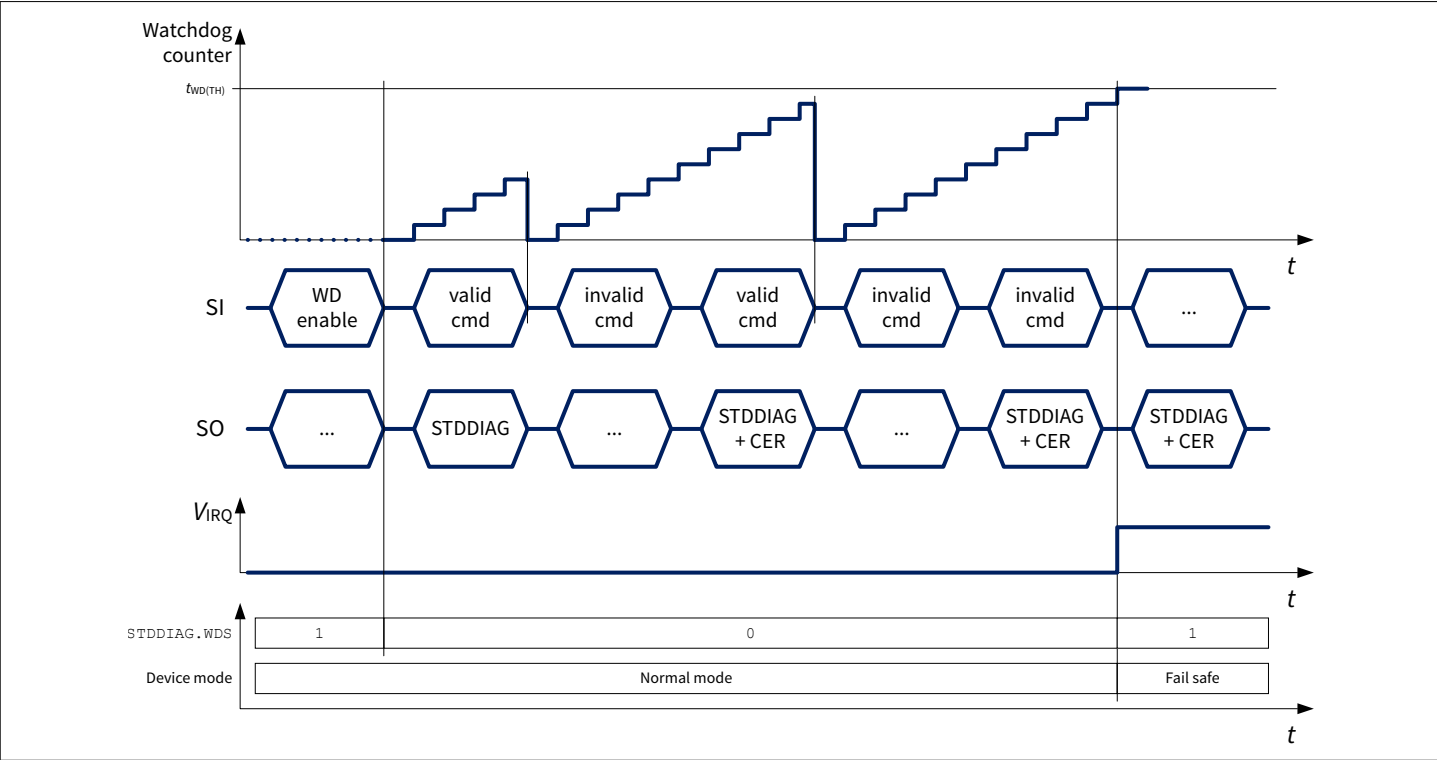


Figure 53 Communication watchdog - timing diagram

As shown in [Figure 53](#), a watchdog overflow triggers a transition to fail safe mode. For more information, refer to [Chapter 6.1.1.7](#).

11.7 Electrical characteristics - digital interface

Table 69 Electrical characteristics - digital interface

 $V_S = V_{S(NOR)}, V_{DD} = V_{DD(NOR)}, T_J = T_{J(NOR)}$

 Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}, V_{DD} = V_{DD(NOR),TYP}, T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			

SPI signal timings

Enable lead time (falling CSN to rising SCLK)	$t_{CSN(LEAD)}$	400	–	–	ns	–	PRQ-501
Enable lag time (falling SCLK to rising CSN)	$t_{CSN(LAG)}$	400	–	–	ns	–	PRQ-502
Transfer delay time (rising CSN to falling CSN)	$t_{CSN(TD)}$	1.3	–	–	μs	–	PRQ-503
Output enable time (falling CSN to SO valid)	$t_{SO(EN)}$	–	30	100	ns	$C_{L(SO)} = 50 \text{ pF}$	PRQ-504
Output disable time (rising CSN to SO tristate)	$t_{SO(DIS)}$	–	30	100	ns	$C_{L(SO)} = 50 \text{ pF}$	PRQ-505
Serial clock frequency	f_{SCLK}	–	–	5	MHz	–	PRQ-506
Serial clock HIGH time	$t_{SCLK(H)}$	90	–	–	ns	–	PRQ-508
Serial clock LOW time	$t_{SCLK(L)}$	90	–	–	ns	–	PRQ-509
Data setup time (required time SI to falling SCLK)	$t_{SI(SU)}$	20	–	–	ns	–	PRQ-510
Data hold time (falling SCLK to SI)	$t_{SI(H)}$	20	–	–	ns	–	PRQ-511
Output data valid time with capacitive load	$t_{SO(V)}$	–	–	60	ns	$C_{L(SO)} = 50 \text{ pF}$	PRQ-512

Communication watchdog

Watchdog time 1	t_{WD1}	0.9	1	1.1	ms	–	PRQ-622
Watchdog time 2	t_{WD2}	1.8	2	2.2	ms	–	PRQ-623
Watchdog time 3	t_{WD3}	4.5	5	5.5	ms	–	PRQ-624
Watchdog time 4	t_{WD4}	9	10	11	ms	–	PRQ-625
Watchdog time 5	t_{WD5}	22.5	25	27.5	ms	–	PRQ-626
Watchdog time 6	t_{WD6}	45	50	55	ms	–	PRQ-627
Watchdog time 7	t_{WD7}	90	100	110	ms	–	PRQ-628

12 Non-volatile memory

The device offers a non-volatile memory (NVM) to store default values of the following control and configuration registers:

- Analog multiplexer
- Device ID
- Communication control
 - CRC enable
 - Watchdog timings
 - Power stage control in fail safe
- CLS mode
- Overcurrent threshold
- Device protection restart enable
- I2t settings
 - DC current - $I_{L(I2t_x)}$
 - Time constant - τ_{I2t_x}
- Undervoltage lockout setting
 - $V_{S(UVL_L)}$
 - $V_{S(UVL_H)}$
 - $I_{L(OCWT)}$
 - $t_{FILTER(UVL_H)}$
 - UVL enable bits
 - UVL restart enable bits
 - UVL_H current dependency enable bit

The registers mentioned above are grouped into 4 groups, called word lines. Each of these word lines consists of 16 bits and can be stored individually in the NVM. With one write to NVM request, only a subset of default values can be stored in the non-volatile memory.

In total, 12 word lines can be stored in the NVM. This means either the same word line can be written 12 times, or each word line can be written 3 times.

The above-mentioned control and configuration registers are grouped together as shown in [Table 70](#).

Table 70 NVM - word line overview

A D D 2	A D D 1	A D D 0	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	DPCR_DPRE	0	COMCR_FSOUT			COMCR_WD		COMCR_CRCEN			DVIDR_DVID	
0	0	1	I2TCR_TAU		I2TCR_DC			0	0	0				DPCR_OCT	
0	1	0		UVLR1_UVL_HF		UVLR2_UVL_HREN	UVLR2_UVL_LREN		UVLR2_UVL_L					UVLR1_UVL_H	
0	1	1		OCWR_OCWT				UVLR1_UVL_HEN	UVLR2_UVL_LEN	UVLR2_UVL_CDEN			DIAGCR_AMUX		OCR_CLS

Requesting a read from non-volatile memory or write to non-volatile memory is enabled only in NVM mode. While the requested operation is processed, the device indicates, via the digital interface, that the NVM block is not ready for a further action.

For reading or writing to the NVM the digital interfaces offers 3 registers:

- NVM_MSB: Here, the MSB information of the word line to be stored in the NVM has to be entered. ADD2 down to D8.
- NVM_LSB: Here, the LSB information of the word line to be stored in the NVM has to be entered. D7 down to D0.
- NVM_CMD: This register contains the status information and the read/write command.

For more information, refer to [Chapter 11.4.7](#).

While the write to NVM request is processed, the power supply voltage must be in the power supply voltage range for write to NVM ($V_{S(NVM)}$). If, during the writing procedure, V_S leaves the $V_{S(NVM)}$, the write to NVM process is aborted and the undervoltage event is indicated in the NVM_CMD register.

As a result of leaving the $V_{S(NVM)}$, all above-mentioned word lines have to be rewritten. This is due to the fact that an undervoltage event can lead to the misinterpretation of the word line address, which leads to a pseudo-overwrite of already programmed NVM content.

An undervoltage event on the digital supply voltage does not lead to the abortion of the write process.

The time that is needed to write the information from NVM_MSB and NVM_LSB into the corresponding WL within the non-volatile memory is defined by t_{NVM} .

The read-out of the non-volatile memory uses the power-up sequence described in [Chapter 6.1.1.2](#).

After the write to NVM is performed for all desired default values according to [Table 70](#), the NVM mode can be left as described in [Chapter 6.1.1.9](#).

12.1 Electrical Characteristics - NVM

Table 71 Electrical characteristics - Non-volatile memory

$V_S = V_{S(NOR)}$, $T_J = T_{J(NOR)}$

Typical values (unless otherwise specified): $V_S = V_{S(NOR),TYP}$, $T_J = T_{J(NOR),TYP}$

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power supply voltage range for write to NVM	$V_{S(NVM)}$	10	12	20	V	–	PRQ-466
NVM writing duration	t_{NVM}	–	–	2.5	ms	–	PRQ-467

13 Application information

Note: The information provided in this chapter is a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition, or quality of the device. The function must be verified in the real application. For sizing and dimensioning of external components, refer to the additional technical documentation or contact our technical support team for assistance.

13.1 Application setup

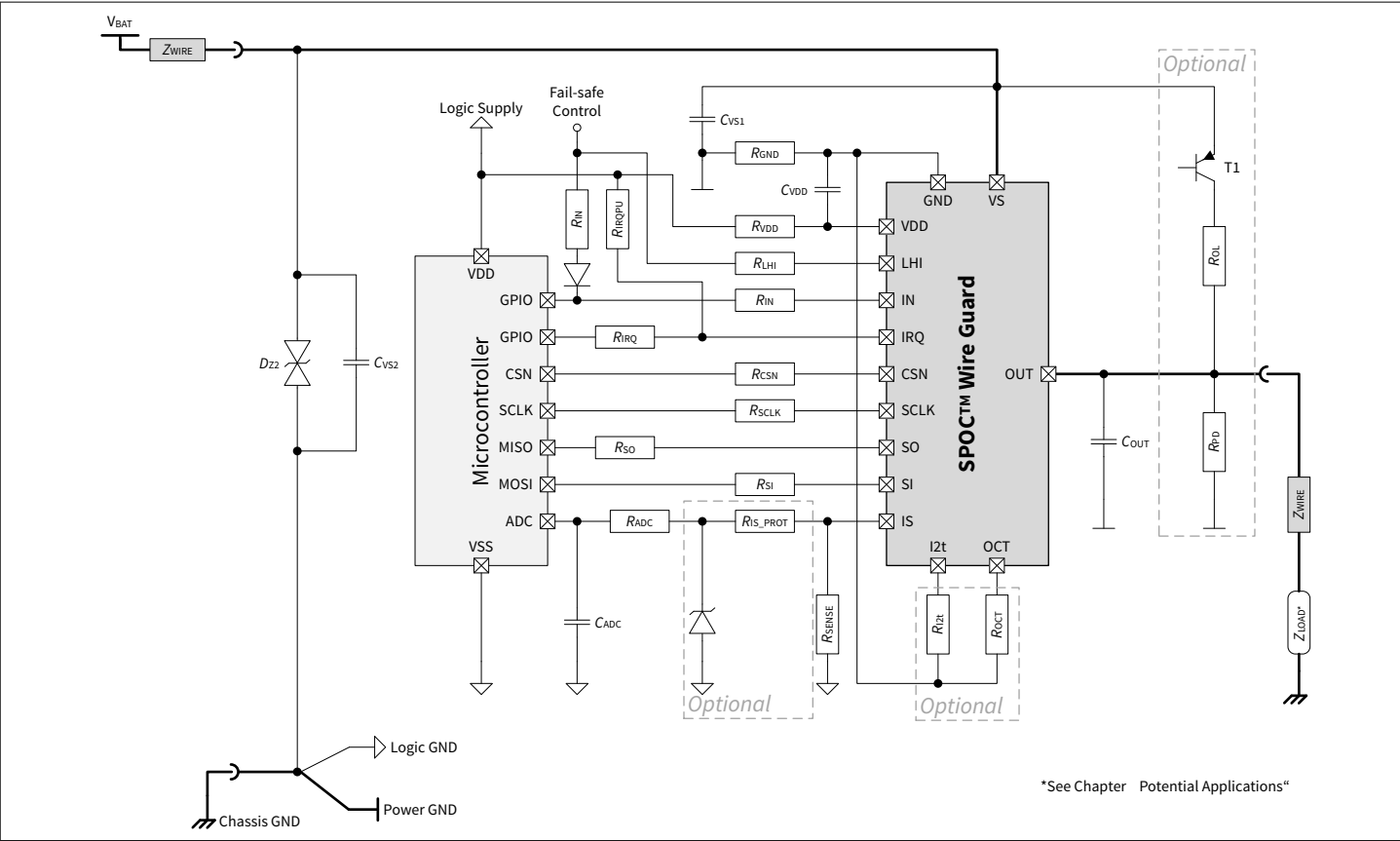


Figure 54 Application diagram

13.2 External components

Table 72 Suggested component values

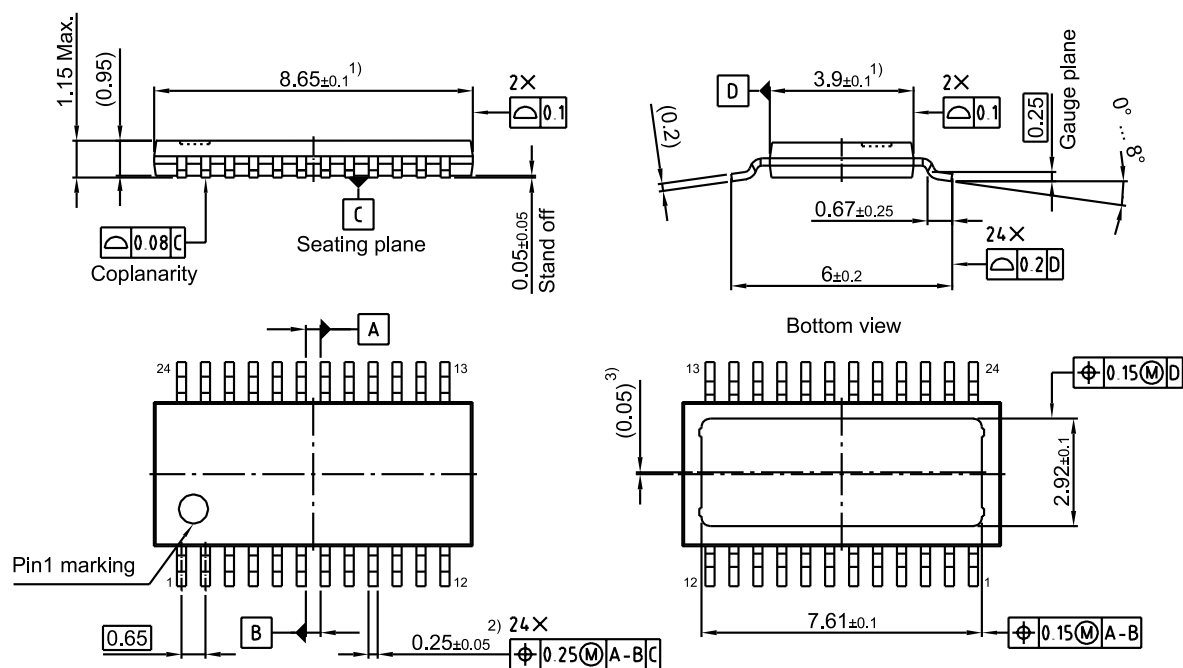
Refer ence	Value	Purpose
R_{GND}	40.2 Ω	Ground voltage spikes filtering for improved robustness against battery voltage transients
R_{VDD}	150 Ω for VDD = 3.3 V 750 Ω for VDD = 5 V	Device logic protection
R_{LHI}	4.7 k Ω	Protection of the microcontroller during overvoltage and reverse polarity
R_{IN}	4.7 k Ω	Protection of the microcontroller during overvoltage and reverse polarity Necessary to switch OFF the power stage during loss of ground

(table continues...)

Table 72 (continued) **Suggested component values**

Reference	Value	Purpose
R_{IRQ}	4.7 k Ω	Protection of the microcontroller during overvoltage and reverse polarity
R_{IRQP} U	10 k Ω	Interrupt request polarization (pull-up) Ensure the polarization of the open drain IRQ pin for interrupt request at the microcontroller
R_{CSN}	1.2 k Ω	Protection of the microcontroller during overvoltage and reverse polarity
R_{SCLK}	1.2 k Ω	Protection of the microcontroller during overvoltage and reverse polarity
R_{SO}	1.2 k Ω	Protection of the microcontroller during overvoltage and reverse polarity
R_{SI}	1.2 k Ω	Protection of the microcontroller during overvoltage and reverse polarity
R_{IS_PROT}	4.7 k Ω	Protection resistor for overvoltage, reverse polarity, and loss of ground Value to be tuned with microcontroller specification
R_{SENSE}	1.2 k Ω	Sense resistor
R_{ADC}	4.7 k Ω	Microcontroller ADC voltage spikes filtering
R_{I2t}	R_{I2t_SHORT} to R_{I2t_OPEN}	Selection of the default I2t protection curve during power-up mode Protection of the device during overvoltage and reverse polarity
R_{OCT}	R_{OCT_SHORT} to R_{OCT_OPEN}	Selection of the default overcurrent threshold high during power-up mode Protection of the device during overvoltage and reverse polarity
R_{OL}	1.5 k Ω	Output polarization (pull-up) Ensure polarization of power stage during open load in OFF diagnosis
R_{PD}	47 k Ω	Output polarization (pull-down) Ensure polarization of power stage to distinguish between open load and short to V_S in OFF diagnosis
C_{ADC}	220 pF	Microcontroller ADC voltage spikes filtering A time constant $((R_{IS_PROT} + R_{ADC}) * C_{ADC})$ longer than 1 μ s is recommended
C_{VDD}	680 nF	Digital supply voltage spikes filtering and for improved robustness against battery voltage transients
C_{VS1}	100 nF	Battery voltage spikes filtering
C_{VS2}	–	Conditional buffer capacitor to support battery voltage spikes filtering in dependency of application setup (EMC)
C_{OUT}	10 nF	For improved electromagnetic compatibility (EMC)
D_{Z1}	–	Protection of microcontroller during overvoltage
D_{Z2}	–	Transient voltage suppressor diode Protection against overvoltage, loss of battery while driving an inductive load, and voltage spikes caused by fast load disconnection
T_1	–	Switch the battery voltage for open load in OFF diagnosis

14 Package information



- 1) Does not include plastic or metal protrusion of 0.15 max. per side
 2) Dambar protrusion shall be maximum 0.1 mm total in excess of lead width.
 3) Distance from centerline exposed pad to package centerline
 All dimensions are in units mm
 The drawing is in compliance with ISO 128-30, Projection Method 1 []
 Drawing according to ISO 8015, general tolerances ISO 2768-mK

Figure 55 PG-TSDSO-24 package outlines

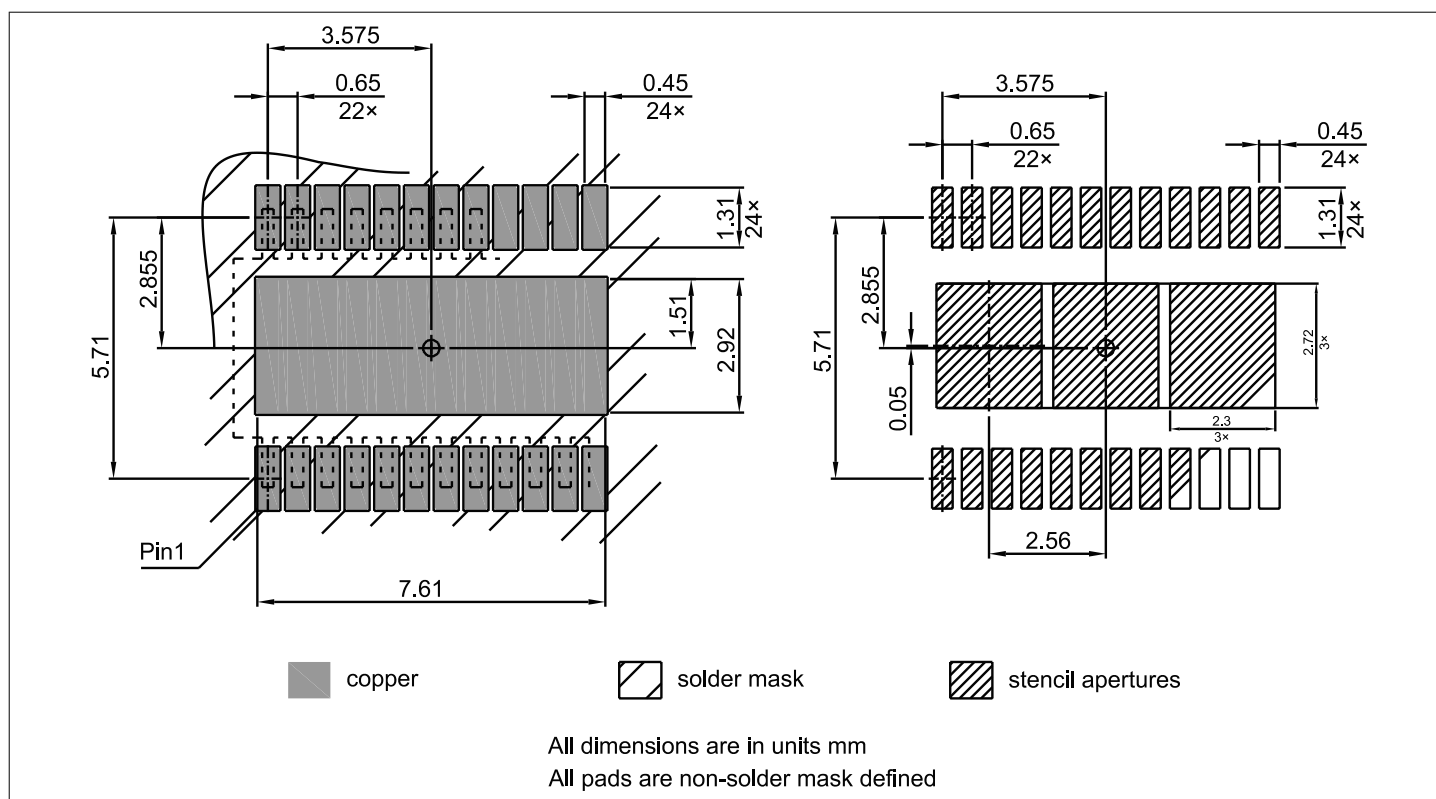


Figure 56 PG-TSDSO-24 footprint

Note: For minimum environmental impact and compliance with government regulations, the package of the device fulfills the requirements of a green product. Green products are RoHS-compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020). For further information, please refer to <https://www.infineon.com/packages>.

15 Revision history

Table 73 Revision History

Revision number	Date of release	Description of changes
1.10	2026-07-15	Typos fixed Chapter 5.1.4 updated Chapter 7.5 updated <ul style="list-style-type: none">PRQ-660, PRQ-1421, PRQ-1422 added Chapter 10.4 updated <ul style="list-style-type: none">PRQ-1341 updated (min./max.: -80%/+80% → -67%/+67%)PRQ-1342 updated (min./max.: -38%/+38% → -17%/+17%)PRQ-1343 updated (min./max.: -18%/+18% → -7%/+7%)PRQ-1344 updated (min./max.: -14%/+14% → -7%/+7%)PRQ-1345 updated (min./max.: -9%/+9% → -7%/+7%)PRQ-1726 updated (min./max.: -40%/+40% → -30%/+30%)PRQ-1727 updated (min./max.: -20%/+20% → -12%/+12%)PRQ-1728 updated (min./max.: -15%/+15% → -12%/+12%)PRQ-488, PRQ-489 added
1.01	2026-03-09	Chapter 4.1 updated <ul style="list-style-type: none">PRQ-1411 added Chapter 6.3 updated <ul style="list-style-type: none">PRQ-1372 added
1.00	2026-03-03	Datasheet available

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