



## Product Change Notification: SYST-06MESY573

---

**Date:**

08-Sep-2026

**Product Category:**

32-Bit Microcontrollers

**Notification Subject:**

PIC32CM MC00 Family Silicon Errata and Data Sheet Clarifications

**Affected CPNs:**

[SYST-06MESY573\\_Affected\\_CPN\\_09082026.pdf](#)

[SYST-06MESY573\\_Affected\\_CPN\\_09082026.csv](#)

**Notification Text:**

SYST-06MESY573

Microchip has released a new Document for the PIC32CM MC00 Family Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at [PIC32CM MC00 Family Silicon Errata and Data Sheet Clarifications](#).

**Notification Status:** Final

**Description of Change:**

Added a note to the OSC48M Start-Up errata.

**Impacts to Data Sheet:** None

**Reason for Change:** To improve Productivity

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 07 Sep 2026

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

## **Attachments:**

### **PIC32CM MC00 Family Silicon Errata and Data Sheet Clarifications**

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

## **Terms and Conditions:**

If you wish to receive Microchip PCNs via email please register for our PCN email service at our [PCN home page](#) select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the [PCN FAQ](#) section.

If you wish to change your PCN profile, including opt out, please go to the [PCN home page](#) select login and sign into your myMicrochip account. Select a profile option from

Affected Catalog Part Numbers (CPN)

PIC32CM1216MC00032T-E/RTB

PIC32CM1216MC00032T-E/RTBV01

PIC32CM1216MC00032T-I/PT

PIC32CM1216MC00032T-I/RTB

PIC32CM1216MC00048-E/U5B

PIC32CM1216MC00048-E/Y8X

PIC32CM1216MC00048-I/U5B

PIC32CM1216MC00032-E/PT

PIC32CM1216MC00032-E/RTB

PIC32CM1216MC00032-I/PT

PIC32CM1216MC00032-I/RTB

PIC32CM1216MC00032T-E/PT

PIC32CM1216MC00048-I/U5BESU

PIC32CM1216MC00048-I/Y8X

PIC32CM1216MC00048T-E/U5B

PIC32CM1216MC00048T-E/Y8X

PIC32CM1216MC00048T-I/U5B

PIC32CM1216MC00048T-I/U5BESU

PIC32CM1216MC00048T-I/Y8X

PIC32CM6408MC00032-E/PT

PIC32CM6408MC00032-E/RTB

PIC32CM6408MC00032-E/RTBVAO

PIC32CM6408MC00032-I/PT

PIC32CM6408MC00032-I/RTB

PIC32CM6408MC00032T-E/PT

PIC32CM6408MC00032T-E/RTB

PIC32CM6408MC00032T-I/PT

PIC32CM6408MC00032T-I/RTB

PIC32CM6408MC00048-E/U5B

---

Date: Monday, September 7, 2026

---

PIC32CM6408MC00048-E/Y8X

PIC32CM6408MC00048-I/U5B

PIC32CM6408MC00048-I/Y8X

PIC32CM6408MC00048T-E/U5B

PIC32CM6408MC00048T-E/Y8X

PIC32CM6408MC00048T-I/U5B

PIC32CM6408MC00048T-I/U5BS2

PIC32CM6408MC00048T-I/Y8X

## PIC32CM MC00 Family Errata

The PIC32CM MC00 family of devices that you have received conforms functionally to the current Device Data Sheet (DS60001638), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following table.

The errata described in this document will be addressed in future revisions of the PIC32CM MC00 family of devices.

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in [Data Sheet Clarifications](#), following the discussion of silicon issues.

**Table 1.** PIC32CM MC00 Family Silicon Device Identification

| Devices            | Device ID<br>(DID[31:0]) | Silicon Revision ID<br>(DID.REVISION[3:0]) |     |
|--------------------|--------------------------|--------------------------------------------|-----|
|                    |                          | A1                                         | A2  |
| PIC32CM1216MC00032 | 0x11070x00               | 0x0                                        | 0x1 |
| PIC32CM6408MC00032 | 0x11070x01               | 0x0                                        | 0x1 |
| PIC32CM1216MC00048 | 0x11070x06               | 0x0                                        | 0x1 |
| PIC32CM6408MC00048 | 0x11070x07               | 0x0                                        | 0x1 |

**Note:**

1. Refer to the “*Device Service Unit*” chapter in the current Device Data Sheet (DS60001638) for a detailed information on Device Identification and Revision IDs for a specific device.

## Silicon Errata Summary

| Module                  | Feature                        | Errata Number | Issue Summary                                                                                                                                                                                                                            | Affected Revisions |    |
|-------------------------|--------------------------------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|----|
|                         |                                |               |                                                                                                                                                                                                                                          | A1                 | A2 |
| NVMCTRL                 | DATA FLASH                     | 1.1.1         | CPU writes to any memory or register while a write or erase operation is ongoing in the Data Flash address space will stall the AHB bus for the duration of the write or erase operation. CPU reads are not impacted.                    | X                  |    |
| NVMCTRL                 | CEHL                           | 1.1.2         | The CEHL feature is not functional.                                                                                                                                                                                                      | X                  |    |
| SERCOM I <sup>2</sup> C | Repeated Start                 | 1.2.1         | For Host Write operations (excluding High-Speed mode) in 10-bit addressing mode, writing CTRLB.CMD = 0x1 does not correctly issue a Repeated Start command.                                                                              | X                  | X  |
| SERCOM I <sup>2</sup> C | Repeated Start                 | 1.2.2         | For High-Speed Host Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start, making repeated start not possible in that mode.                                                                        | X                  | X  |
| SERCOM I <sup>2</sup> C | NACK and Repeated Start        | 1.2.3         | For High-Speed Host Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued, making repeated start not possible in that mode.                                                                                       | X                  | X  |
| SERCOM I <sup>2</sup> C | RXNACK                         | 1.2.4         | The RXNACK status bit is invalid during the first DRDY interrupt.                                                                                                                                                                        | X                  | X  |
| OSCCTRL                 | FDPLL Unlock                   | 1.3.1         | Spurious DPLL unlocks may be detected during operation.                                                                                                                                                                                  | X                  | X  |
| OSCCTRL                 | FDPLL ONDEMAND                 | 1.3.2         | The FDPLL96M On Demand mode (DPLLCTRLA.ONDEMAND = 1) is not functional in Standby Sleep mode.                                                                                                                                            | X                  | X  |
| AC                      | INTREF                         | 1.4.1         | For AC reference voltage do not use the INTREF.                                                                                                                                                                                          | X                  | X  |
| PDEC                    | STATUS                         | 1.5.1         | When the INTFLAG.ERR is rising the associated STATUS.xERR is set after a delay.                                                                                                                                                          | X                  | X  |
| PDEC                    | STATUS                         | 1.5.2         | When the INTFLAG.DIR is rising the associated STATUS.DIR is set after a delay.                                                                                                                                                           | X                  | X  |
| PDEC                    | HALL MODE                      | 1.5.3         | In Hall mode, a spurious WINERR can be reported at start command or when leaving standby.                                                                                                                                                | X                  | X  |
| PDEC                    | HALL MODE                      | 1.5.4         | In Hall mode, when rotation is very slow or stopped then several WINERR interrupts can occur.                                                                                                                                            | X                  | X  |
| SERCOM USART            | LIN Host Delays                | 1.6.1         | In SERCOM USART LIN Host mode, when break, sync, and identifier fields are automatically transmitted when data is written with the identifier, the LIN Host Header Delay between the sync and the ID transmission fields is not correct. | X                  | X  |
| SERCOM USART            | Two stop bits mode in LIN Host | 1.6.2         | Two stop bits mode is not supported in SERCOM USART LIN Host mode when break, sync, and identifier fields are automatically transmitted when data is written with the identifier.                                                        | X                  | X  |
| OSC48M                  | Start-Up                       | 1.7.1         | In some very rare cases, the OSC48M internal oscillator may not start at power-up or may not re-start during runtime after having been turned off manually or automatically by the system.                                               | X                  | X  |

## Table of Contents

|                                                    |    |
|----------------------------------------------------|----|
| PIC32CM MC00 Family Errata.....                    | 1  |
| Silicon Errata Summary.....                        | 2  |
| 1. PIC32CM MC00 Errata Issues.....                 | 4  |
| 1.1. Non-Volatile Memory Controller (NVMCTRL)..... | 4  |
| 1.2. SERCOM I <sup>2</sup> C.....                  | 4  |
| 1.3. OSCCTRL.....                                  | 5  |
| 1.4. AC.....                                       | 6  |
| 1.5. PDEC.....                                     | 6  |
| 1.6. SERCOM USART.....                             | 7  |
| 1.7. OSC48M.....                                   | 8  |
| 2. Data Sheet Clarifications.....                  | 9  |
| 3. Appendix A: Revision History.....               | 10 |
| Microchip Information.....                         | 12 |
| Trademarks.....                                    | 12 |
| Legal Notice.....                                  | 12 |
| Microchip Devices Code Protection Feature.....     | 12 |

# 1. PIC32CM MC00 Errata Issues

The following issues apply to the PIC32CM MC00 family of devices.

## 1.1. Non-Volatile Memory Controller (NVMCTRL)

### 1.1.1. DATA FLASH

CPU writes to any memory or register while a write or erase operation is ongoing in the Data Flash address space will stall the AHB bus for the duration of the write or erase operation. CPU reads are not impacted.

The stall duration will be up to the maximum time of the Flash write or erase operation:

Page Write time: 2.5 ms

Row Erase time: 6 ms

Sector Erase time: 8 ms

#### Workaround

Perform Data Flash modify operations in a safe region of the application where CPU writes are not required.

#### Affected Silicon Revisions

| A1 | A2 |  |  |  |
|----|----|--|--|--|
| X  |    |  |  |  |

### 1.1.2. CEHL

The Chip Erase Hard Lock (CEHL) feature is not functional and will not provide any code protection capabilities. The Secure Bit (SB) is not affected and can be used for code protection.

#### Workaround

None.

#### Affected Silicon Revisions

| A1 | A2 |  |  |  |
|----|----|--|--|--|
| X  |    |  |  |  |

## 1.2. SERCOM I<sup>2</sup>C

### 1.2.1. Repeated Start

For Host Write operations (excluding High-Speed mode) in 10-bit Addressing mode, writing CTRLB.CMD = 0x1 does not correctly issue a Repeated Start command.

#### Workaround

Write the same 10-bit address with the same direction bit to the ADDR.ADDR register to generate a Repeated Start.

#### Affected Silicon Revisions

| A1 | A2 |  |  |  |
|----|----|--|--|--|
| X  | X  |  |  |  |

### 1.2.2. Repeated Start

For High-Speed Host Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start, making a repeated start not possible in that mode.

## Workaround

None.

## Affected Silicon Revisions

| A1 | A2 |  |  |  |
|----|----|--|--|--|
| X  | X  |  |  |  |

### 1.2.3. NACK and Repeated Start

For High-Speed Host Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued, making a repeated start not possible in that mode.

## Workaround

None.

## Affected Silicon Revisions

| A1 | A2 |  |  |  |
|----|----|--|--|--|
| X  | X  |  |  |  |

### 1.2.4. RXNACK

The RXNACK status bit is invalid during the first DRDY interrupt.

## Workaround

Use a software flag to track when to ignore RXNACK and reset this flag in the I2CS\_AMATCH interrupt handler (workaround not applicable when AACKEN = 1).

## Affected Silicon Revisions

| A1 | A2 |  |  |  |
|----|----|--|--|--|
| X  | X  |  |  |  |

## 1.3. OSCCTRL

### 1.3.1. FDPLL Unlock

When using FDPLL at temperatures below 25°C, spurious DPLL unlocks (OSCCTRL.DPLLSTATUS.LOCK = 0) may be detected while the FDPLL still adheres to the electrical characteristics metrics defined in section 43.16 of the data sheet. During these unlock periods, the DPLL output clock is halted and then restarts.

## Workaround

When using FDPLL at temperatures below 25°C, enable the lock bypass (OSCCTRL.DPLLCTRLB.LBYPASS = 1) to avoid losing FDPLL clock output during a false unlock status. The workaround does not prevent false unlock indications, but it disables the gating of the FDPLL clock output by the lock status; therefore, the clock is issued even if the FDPLL status shows unlocked.

## Pseudo Code

Set OSCCTRL.DPLLCTRLB.LBYPASS = 1

Set DPLLCTRLA.ENABLE = 1

Wait (OSCCTRL.DPLLSTATUS.CLKRDY = 1)

Set Source for GCLK with DPLL

### Affected Silicon Revisions

| A1 | A2 |  |  |  |
|----|----|--|--|--|
| X  | X  |  |  |  |

#### 1.3.2. FDPLL ONDEMAND

The FDPLL96M On Demand mode (DPLLCTRLA.ONDEMAND = 1) is not functional in Standby Sleep mode.

#### Workaround

Set the DPLLCTRLA.ONDEMAND = 0 which makes the FDPLL96M always run in Standby Sleep mode.

### Affected Silicon Revisions

| A1 | A2 |  |  |  |
|----|----|--|--|--|
| X  | X  |  |  |  |

#### 1.4. AC

##### 1.4.1. INTREF

When using the AC module, do not use the INTREF (AC.COMPCTRLx.MUXNEG = INTREF) as an internal reference voltage.

#### Workaround

Use the DAC (AC.COMPCTRLx.MUXNEG = DAC) for the internal reference of the AC module.

### Affected Silicon Revisions

| A1 | A2 |  |  |  |
|----|----|--|--|--|
| X  | X  |  |  |  |

#### 1.5. PDEC

##### 1.5.1. STATUS

When the INTFLAG.ERR is raised, the associated STATUS.xERR is set after a delay.

#### Workaround

Poll the STATUS register until the ERR bit is set.

### Affected Silicon Revisions

| A1 | A2 |  |  |  |
|----|----|--|--|--|
| X  | X  |  |  |  |

##### 1.5.2. STATUS

When the INTFLAG.DIR is rising, the associated STATUS.DIR is set after a delay. It is not recommended to use the INTFLAG.DIR and STATUS.DIR in conjunction with each other.

#### Workaround

None.

### Affected Silicon Revisions

| A1 | A2 |  |  |  |
|----|----|--|--|--|
| X  | X  |  |  |  |

##### 1.5.3. HALL MODE

In Hall mode, a spurious WINERR can be reported at the Start command or when leaving standby.

## Workaround

Ignore WINERR in Hall mode at the Start command or when leaving standby.

## Affected Silicon Revisions

| A1 | A2 |  |  |  |
|----|----|--|--|--|
| X  | X  |  |  |  |

### 1.5.4. HALL MODE

In Hall mode, when rotation is very slow or stopped, several WINERR interrupts can occur.

## Workaround

When a stop or low speed is indicated by the WINERR interrupt, disable the Hall error interrupts until the error condition has disappeared.

## Affected Silicon Revisions

| A1 | A2 |  |  |  |
|----|----|--|--|--|
| X  | X  |  |  |  |

## 1.6. SERCOM USART

### 1.6.1. LIN Host Delays

In SERCOM USART LIN Host mode (CTRLA.FORM = 0x2), when break, sync, and identifier fields are automatically transmitted when data is written with the identifier (CTRLB.LINCMD = 0x2), the LIN Host Header Delay between the sync and the ID transmission fields is not correct for the following cases:

- CTRLC.HDRDLY = 0x2: Where the delay between the sync and ID transmission fields is 8-bit time instead of 4-bit time.
- CTRLC.HDRDLY = 0x3: Where the delay between the sync and ID transmission fields is 14-bit time instead of 4-bit time.

## Workaround

None.

## Affected Silicon Revisions

| A1 | A2 |  |  |  |
|----|----|--|--|--|
| X  | X  |  |  |  |

### 1.6.2. Two Stop Bits Mode in LIN Host

Two Stop Bits mode (CTRLB.SBMODE = 0x1) is not supported in SERCOM USART LIN Host mode (CTRLA.FORM = 0x2) when break, sync, and identifier fields are automatically transmitted when data is written with the identifier (CTRLB.LINCMD = 0x2). Only One stop bit is supported.

## Workaround

None.

## Affected Silicon Revisions

| A1 | A2 |  |  |  |
|----|----|--|--|--|
| X  | X  |  |  |  |

## 1.7. OSC48M

### 1.7.1. Start-Up

In some very rare cases, the OSC48M internal oscillator may not start at power-up or may not restart during runtime after having been turned off manually or automatically by the system.

#### Workaround

Failures at power-up can be resolved by power cycling the unit.

Failures at runtime can be addressed by keeping the OSC48M always enabled (OSC48MCTRL.ENABLE = 1, OSC48MCTRL.ONDEMAND = 0, OSC48MCTRL.RUNSTDBY = 1).

**Note:** Affects only those versions of the device manufactured prior to January 2025.

#### Affected Silicon Revisions

| A1 | A2 |  |  |  |
|----|----|--|--|--|
| X  | X  |  |  |  |

## 2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001638D):

**Note:** Corrections in tables, registers, and text are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

There are no data sheet clarifications to report.

### 3. Appendix A: Revision History

#### Revision G - 09/2026

The following updates were performed for this revision:

- Added a note to the [OSC48M](#) Start-Up errata .

#### Revision F - 03/2023

This revision contains numerous typographical updates throughout the document along with the updates listed here.

Obsolete [Data Sheet Clarifications](#) were removed for this revision.

- The following Errata were added in this revision:
  - [SERCOM USART: 1.6.1 LIN Host Delays](#)
  - [SERCOM USART: 1.6.2 Two stop bits mode in LIN Host](#)
  - [OSC48M: 1.7.1 Start-Up](#)

#### Revision E - 06/2021

This revision contains numerous typographical updates throughout the document along with the updates listed here.

The I<sup>2</sup>C, SPI and I<sup>2</sup>S standards use the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client" respectively.

- The following Errata were added in this revision:
  - SERCOM I<sup>2</sup>C: 1.2.4 RXNACK
  - PDEC: STATUS 1.5.1
  - PDEC: STATUS 1.5.2
  - PDEC: HALL MODE 1.5.3
  - PDEC: HALL MODE 1.5.4
- The following Data Sheet Clarifications were added:
  - Absolute Maximum Ratings
  - Internal 48MHz RC Oscillator (OSC48M)
  - I/O Pin Electrical Characteristics
  - SERCOM SPI Host/Client

#### Revision D - 04/2021

This revision contains numerous typographical updates throughout the document along with the updates listed here.

The I<sup>2</sup>C, SPI and I<sup>2</sup>S standards use the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client" respectively.

- The following Errata were added in this revision:
  - AC: INTREF 1.4.1
  - OSCCTRL: FDPLL ONDEMAND 1.3.2

#### Revision C - 02/2021

The following update was performed for this revision:

- Added Silicon Issue OSCCTRL FDPLL Unlock 1.3.1

**Revision B - 11/2020**

The following updates were performed for this revision:

- Updated Silicon Die Revision from A0 to A1
- Updated the errata numbering schema

**Revision A - 07/2020**

This is the initial released version of this document.

## Microchip Information

### Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at <https://www.microchip.com/en-us/about/legal-information/microchip-trademarks>.

### Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at [www.microchip.com/en-us/support/design-help/client-support-services](http://www.microchip.com/en-us/support/design-help/client-support-services).

THIS INFORMATION IS PROVIDED BY MICROCHIP “AS IS”. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP’S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

### Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip products are strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.