



Product Change Notification: SYST-26VLSV663

Date:

01-Sep-2026

Product Category:

Digital Signal Controllers

Notification Subject:

dsPIC33CK1024MP710 Family Silicon Errata and Data Sheet Clarification

Affected CPNs:

[SYST-26VLSV663_Affected_CPN_09012026.pdf](#)

[SYST-26VLSV663_Affected_CPN_09012026.csv](#)

Notification Text:

SYST-26VLSV663

Microchip has released a new Document for the dsPIC33CK1024MP710 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at [dsPIC33CK1024MP710 Family Silicon Errata and Data Sheet Clarification](#).

Notification Status: Final

Description of Change:

Added silicon revision A2. Removed all data sheet clarifications, as they have been addressed in the latest revision of the data sheet.

Impacts to Data Sheet: None

Change Implementation Status: Complete

Date Document Changes Effective: 01 September 2026

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

dsPIC33CK1024MP710 Family Silicon Errata and Data Sheet Clarification

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

DSPIC33CK1024MP405-E/M7

DSPIC33CK1024MP405-E/PT

DSPIC33CK1024MP405-H/M7

DSPIC33CK1024MP405-H/M7VAO

DSPIC33CK1024MP405-H/PT

DSPIC33CK1024MP405-I/M7

DSPIC33CK1024MP405-I/PT

DSPIC33CK1024MP405T-E/M7

DSPIC33CK1024MP405T-E/PT

DSPIC33CK1024MP405T-I/M7

DSPIC33CK1024MP405T-I/PT

DSPIC33CK1024MP406-E/MR

DSPIC33CK1024MP406-E/PT

DSPIC33CK1024MP406-H/MR

DSPIC33CK1024MP406-H/PT

DSPIC33CK1024MP406-I/MR

DSPIC33CK1024MP406-I/PT

DSPIC33CK1024MP406T-E/MR

DSPIC33CK1024MP406T-E/PT

DSPIC33CK1024MP406T-I/MR

DSPIC33CK1024MP406T-I/PT

DSPIC33CK1024MP408-E/PT

DSPIC33CK1024MP408-H/PT

DSPIC33CK1024MP408-I/PT

DSPIC33CK1024MP408T-E/PT

DSPIC33CK1024MP408T-I/PT

DSPIC33CK1024MP410-E/PT

DSPIC33CK1024MP410-H/PT

DSPIC33CK1024MP410-I/PT

Date: Monday, August 31, 2026

DSPIC33CK1024MP410T-E/PT

DSPIC33CK1024MP410T-I/PT

DSPIC33CK1024MP705-E/M7

DSPIC33CK1024MP705-E/M7V01

DSPIC33CK1024MP705-E/M7VAO

DSPIC33CK1024MP705-E/PT

DSPIC33CK1024MP705-H/M7

DSPIC33CK1024MP705-H/PT

DSPIC33CK1024MP705-I/M7

DSPIC33CK1024MP705-I/PT

DSPIC33CK1024MP705T-E/M7

DSPIC33CK1024MP705T-E/M7VAO

DSPIC33CK1024MP705T-E/PT

DSPIC33CK1024MP705T-I/M7

DSPIC33CK1024MP705T-I/PT

DSPIC33CK1024MP706-E/MR

DSPIC33CK1024MP706-E/PT

DSPIC33CK1024MP706-E/PTVAO

DSPIC33CK1024MP706-H/MR

DSPIC33CK1024MP706-H/PT

DSPIC33CK1024MP706-I/MR

DSPIC33CK1024MP706-I/PT

DSPIC33CK1024MP706T-E/MR

DSPIC33CK1024MP706T-E/PT

DSPIC33CK1024MP706T-I/MR

DSPIC33CK1024MP706T-I/PT

DSPIC33CK1024MP708-E/PT

DSPIC33CK1024MP708-E/PTVAO

DSPIC33CK1024MP708-H/PT

DSPIC33CK1024MP708-I/PT

DSPIC33CK1024MP708T-E/PT

DSPIC33CK1024MP708T-E/PTVAO

DSPIC33CK1024MP708T-I/PT

DSPIC33CK1024MP710-E/PT

DSPIC33CK1024MP710-E/PTVAO

DSPIC33CK1024MP710-H/PT

DSPIC33CK1024MP710-I/PT

DSPIC33CK1024MP710T-E/PT

DSPIC33CK1024MP710T-E/PTVAO

DSPIC33CK1024MP710T-I/PT

DSPIC33CK256MP405-E/M7

DSPIC33CK256MP405-E/PT

DSPIC33CK256MP405-H/M7

DSPIC33CK256MP405-H/PT

DSPIC33CK256MP405-I/M7

DSPIC33CK256MP405-I/PT

DSPIC33CK256MP405T-E/M7

DSPIC33CK256MP405T-E/PT

DSPIC33CK256MP405T-I/M7

DSPIC33CK256MP405T-I/PT

DSPIC33CK256MP406-E/MR

DSPIC33CK256MP406-E/PT

DSPIC33CK512MP710T-E/PT

DSPIC33CK512MP710T-I/PT

DSPIC33CK256MP706-H/PT

DSPIC33CK256MP706-I/MR

DSPIC33CK256MP706-I/PT

DSPIC33CK256MP706T-E/MR

DSPIC33CK256MP706T-E/PT

DSPIC33CK256MP706T-I/MR

DSPIC33CK256MP706T-I/PT

DSPIC33CK256MP708-E/PT

DSPIC33CK256MP708-H/PT

DSPIC33CK256MP708-I/PT

DSPIC33CK256MP708T-E/PT

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DSPIC33CK256MP710-E/PT

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DSPIC33CK256MP710T-E/PT

DSPIC33CK256MP710T-I/PT

DSPIC33CK512MP405-E/M7

DSPIC33CK512MP405-E/PT

DSPIC33CK512MP405-H/M7

DSPIC33CK512MP405-H/PT

DSPIC33CK512MP405-I/M7

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DSPIC33CK512MP405T-E/PT

DSPIC33CK512MP405T-I/M7

DSPIC33CK512MP405T-I/PT

DSPIC33CK512MP406-E/MR

DSPIC33CK512MP406-E/PT

DSPIC33CK512MP406-H/MR

DSPIC33CK512MP406-H/PT

DSPIC33CK512MP406-I/MR

DSPIC33CK512MP406-I/PT

DSPIC33CK512MP406T-E/MR

DSPIC33CK512MP406T-E/PT

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DSPIC33CK512MP406T-I/PT

DSPIC33CK512MP408-E/PT

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DSPIC33CK512MP410-I/PT

DSPIC33CK512MP410T-E/PT

DSPIC33CK512MP410T-I/PT

DSPIC33CK512MP705-E/M7

DSPIC33CK512MP705-E/PT

DSPIC33CK512MP705-H/M7

DSPIC33CK512MP705-H/PT

DSPIC33CK512MP705-I/M7

DSPIC33CK512MP705-I/PT

DSPIC33CK512MP705T-E/M7

DSPIC33CK512MP705T-E/PT

DSPIC33CK512MP705T-I/M7

DSPIC33CK512MP705T-I/PT

DSPIC33CK512MP706-E/MR

DSPIC33CK512MP706-E/PT

DSPIC33CK512MP706-H/MR

DSPIC33CK512MP706-H/PT

DSPIC33CK512MP706-I/MR

DSPIC33CK512MP706-I/PT

DSPIC33CK512MP706T-E/MR

DSPIC33CK512MP706T-E/PT

DSPIC33CK512MP706T-I/MR

DSPIC33CK512MP706T-I/PT

DSPIC33CK512MP708-E/PT

DSPIC33CK512MP708-H/PT

DSPIC33CK512MP708-I/PT

DSPIC33CK512MP708T-E/PT

DSPIC33CK512MP708T-I/PT

DSPIC33CK512MP710-E/PT

DSPIC33CK512MP710-E/PTVAO

DSPIC33CK512MP710-H/PT

DSPIC33CK512MP710-I/PT

DSPIC33CK256MP408T-I/PT

DSPIC33CK256MP410-E/PT

DSPIC33CK256MP410-H/PT

DSPIC33CK256MP410-I/PT

DSPIC33CK256MP410T-E/PT

DSPIC33CK256MP410T-I/PT

DSPIC33CK256MP705-E/M7

DSPIC33CK256MP705-E/M7VAO

DSPIC33CK256MP705-E/PT

DSPIC33CK256MP705-H/M7

DSPIC33CK256MP705-H/PT

DSPIC33CK256MP705-I/M7

DSPIC33CK256MP705-I/PT

DSPIC33CK256MP705T-E/M7

DSPIC33CK256MP705T-E/M7VAO

DSPIC33CK256MP705T-E/PT

DSPIC33CK256MP705T-I/M7

DSPIC33CK256MP705T-I/PT

DSPIC33CK256MP706-E/MR

DSPIC33CK256MP706-E/PT

DSPIC33CK256MP706-H/MR

DSPIC33CK256MP406-E/PTVAO

DSPIC33CK256MP406-H/MR

DSPIC33CK256MP406-H/PT

DSPIC33CK256MP406-I/MR

DSPIC33CK256MP406-I/PT

DSPIC33CK256MP406T-E/MR

DSPIC33CK256MP406T-E/PT

DSPIC33CK256MP406T-I/MR

DSPIC33CK256MP406T-I/PT

DSPIC33CK256MP408-E/PT

DSPIC33CK256MP408-H/PT

DSPIC33CK256MP408-I/PT

DSPIC33CK256MP408T-E/PT

dsPIC33CK1024MP710 Family Silicon Errata and Data Sheet Clarification

The dsPIC33CK1024MP710 family devices that you have received conform functionally to the current Device Data Sheet (DS70005496D), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).

The errata described in this document will be addressed in future revisions of the dsPIC33CK1024MP710 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on [page 6](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
 - a) For MPLAB IDE 8, select Programmer > Reconnect.
 - b) For MPLAB X IDE, select Window > Dashboard and click the **Refresh Debug Tool Status** icon ().
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various dsPIC33CK1024MP710 silicon revisions are shown in [Table 1](#).

dsPIC33CK1024MP710

TABLE 1: SILICON DEVREV VALUES

Device	Device ID ⁽¹⁾	Revision ID for Silicon Revision		Device	Device ID ⁽¹⁾	Revision ID for Silicon Revision	
		A1	A2			A1	A2
dsPIC33CK1024MP710 Family with CAN FD				dsPIC33CK1024MP710 Family without CAN FD			
dsPIC33CK1024MP710	0xA065	0x0001	0x0002	dsPIC33CK1024MP410	0xA025	0x0001	0x0002
dsPIC33CK1024MP708	0xA064			dsPIC33CK1024MP408	0xA024		
dsPIC33CK1024MP706	0xA063			dsPIC33CK1024MP406	0xA023		
dsPIC33CK1024MP705	0xA062			dsPIC33CK1024MP405	0xA022		
dsPIC33CK512MP710	0xA055			dsPIC33CK512MP410	0xA015		
dsPIC33CK512MP708	0xA054			dsPIC33CK512MP408	0xA014		
dsPIC33CK512MP706	0xA053			dsPIC33CK512MP406	0xA013		
dsPIC33CK512MP705	0xA052			dsPIC33CK512MP405	0xA012		
dsPIC33CK256MP710	0xA045			dsPIC33CK256MP410	0xA005		
dsPIC33CK256MP708	0xA044			dsPIC33CK256MP408	0xA004		
dsPIC33CK256MP706	0xA043			dsPIC33CK256MP406	0xA003		
dsPIC33CK256MP705	0xA042			dsPIC33CK256MP405	0xA002		

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾	
				A1	A2
I2C	Idle	1.	Address cannot be received in Idle mode.	X	X
CPU	DIV.SD Instruction	2.	Overflow bit is not getting set when an overflow occurs.	X	X
I2C	Collision Detection	3.	Bus collision is not detected during Host reception if there is a Start/Stop condition.	X	X
I2C	Client Mode	4.	Unexpected Client interrupt if there is a Stop bit in the 9th clock, followed by a Start bit.	X	X
I2C	Client Mode	5.	When data hold is enabled and software sends a NACK, a Client interrupt is asserted if there are more bytes on the bus.	X	X
ADC	Differential-Mode	6.	Errors may occur when enabling Differential-mode when F _{SRC} is greater than 50 MHz.	X	X
Reset	BOR	7.	BOR may stop functioning when V _{DD} drops in the window between the BOR level and BOR-25 mV.	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

dsPIC33CK1024MP710

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (A2).

1. Module: I²C

In Client mode, an address cannot be received when the device is in Idle and the module is set to discontinue in Idle (I2CSIDL = 1).

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

2. Module: CPU

When using the Signed 32/16-bit Division instruction, DIV.SD, the Overflow bit may not always get set when an overflow occurs.

Work around

Test for and handle Overflow conditions outside of the DIV.SD instruction.

Affected Silicon Revisions

A1	A2						
X	X						

3. Module: I²C

Bus collision detection can fail during a Start/ Stop condition when a host is receiving data from a client. This condition can occur in a noisy environment or during hot swapping of I²C.

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

4. Module: I²C

An unexpected Client interrupt will occur if the host sends a NACK and a Stop bit, followed by a Start bit in the ACK phase (9th clock) during Client transmit.

Work around

Software should ignore the Client interrupt that is asserted after sending a NACK.

Affected Silicon Revisions

A1	A2						
X	X						

5. Module: I²C

In Client mode with DHEN = 1 (Data Hold Enable), if software sends a NACK, the Client interrupt is asserted if there are any bytes on the bus.

Work around

Software should ignore the Client interrupt that is asserted after sending a NACK.

Affected Silicon Revisions

A1	A2						
X	X						

6. Module: ADC

When operating ADC with an Input Frequency (F_{SRC}) above 50 MHz, conversion errors may occur when enabling Differential-mode (DIFFx = 1).

Work around

During initialization of the ADC to write the ADMODxL/H registers, use a slower input frequency of 50 MHz or less. After completion of the 1st conversion of each channel in Differential-mode, Input Frequency (F_{SRC}) can be increased to the maximum specified in the “Electrical Characteristics”.

Affected Silicon Revisions

A1	A2						
X	X						

7. Module: Reset

After start-up, if VDD decreases to a value between VBOR-25 mV and VBOR, the BOR may unintentionally disable. The device may incorrectly operate down to 1.8V. However, while operating at a VDD between 3V and 3.6V, the device will operate as expected. A tri-state I/O can be used to observe this behavior. The VBOR specification is listed in the “**Electrical Characteristics**”.

Work around

An external voltage monitor IC may be used as a workaround. MCP111-300E and similar devices are recommended for this purpose.

Affected Silicon Revisions

A1	A2						
X							

dsPIC33CK1024MP710

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70005496D):

Note: Corrections are shown in bold . Where possible, the original bold text formatting has been removed for clarity.

None

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (5/2022)

Initial version of this document; issued for revision **A1**.

Rev B Document (7/2023)

Added silicon errata issue 7 ([Reset](#)).

Rev C Document (12/2023)

Added data sheet clarifications 1 (Document Revision History), 2 (Electrical Characteristics), 3 (Special Features) 4 (Direct Memory Access (DMA) Controller), 5 (Direct Memory Access (DMA) Controller) and 6 (Direct Memory Access (DMA) Controller).

Rev D Document (8/2026)

Added silicon revision **A2**.

Removed all data sheet clarifications, as they have been addressed in the latest revision of the data sheet.

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