12500 TI Boulevard, MS 8640, Dallas, Texas 75243

PCN Number:	20260915001.1	PCN Issued	September 17, 2026
Qualification of RFAB as an additional Fab site option, Die Revision, Datasheet, Marking update and TIPI as an additional Assembly site options for select devices		Sample request deadline:	November 16, 2026
		Estimated 1st ship date:	December 16, 2026
Sample requests received after November 16, 2026 will not be supported.			

Change type(s)
Assembly Site
Assembly Material
Packing/Shipping/Labeling
Design
Data Sheet/Electrical Specification
Wafer Fab Site
Wafer Fab Material
Wafer Fab Process

PCN Details

Description of Change:

Texas Instruments is pleased to announce the qualification of RFAB as an additional Fab site option, marking update & TIPI as additional Assembly site options for the devices listed below.

Current Fab Site			Additional Fab site		
Current Fab Site	Process	Wafer Diameter	Additional Fab site	Process	Wafer Diameter
FFAB	ASLNONC10	200mm	RFAB	LBC9PLV	300mm

The die was also changed as a result of the process change.

Construction differences are as follows:

Group 1 device (Fab, Design, Marking)

Group 2 device (Fab, Design, Assembly site)

	Current Site	Additional Site
Assembly/Test site	TFME	TIPI
Mount compound	SID# A-03	8095733
Mold compound	SID# R-13	4222198

Device Marking

Device name	Current	Additional
SN74LVC1G00DBVR	C005, C00S, C00J, C00R, C00H, C00F, C00P	49MU
SN74LVC1G08DBVR	C085, C08S, C08J, C08R, C08F, C08P, C08J	49NU
SN74LVC1G125DBVR	C255, C25J, C25R, C255, C25F	49OU
SN74LVC1G126DBVR	C265, C26J, C26R, C26J, C26F	49PU
SN74LVC1G240DBVR	C405, C40J, C40R, C40J, C40F	49QU
SN74LVC1G32DBVR	C325, C32S, C32J, C32R, C32H, C32F, C32P	49RU
SN74LVC1G79DBVR	C795, C79J, C79R, C79F	49SU
SN74LVC1G80DBVR	C805, C80J, C80R, C80F	49TU
SN74LVC1G86DBVR	C865, C86J, C86R, C86F	49UU
SN74LVC1G132DBVR	C3BJ, C3BR	49VU
SN74LVC1G02DBVR	C025, C02S, C02J, C02R, C02H, C02F, C02P	49WU
SN74LVC1G38DBVR	C385, C38S, C38J, C38R, C38H, C38F, C38P	49XU
SN74LVC1G08DBVRG4	C08F, C08P	C084
74LVC1G126DBVRG4	C26F	C26J

Data sheet update

The datasheets will be changing as a result of the above mentioned changes. The datasheet change details can be reviewed in the datasheet revision history. The links to the revised datasheets are available in the table below.

TEXAS INSTRUMENTS

SN74LVC1G00

SCES212AC – APRIL 1999 – REVISED AUGUST 2026

Changes from April 1, 2014 to August 12, 2026 (from Revision AB (April 2014) to Revision AC (August 2026)) **Page**

- Updated *Device Information* table to include body and package dimensions 1
- Changed *Handling Ratings* to *ESD Ratings* 4
- Moved *Storage temperature range* from *Handling Ratings* to *Absolute Maximum Ratings* 4
- Updated format for *Thermal Information* table 5
- Changed Junction-to-ambient thermal resistance value for DBV package from: 229°C/W to: 357.1°C/W 5
- Changed Junction-to-case (top) thermal resistance value for DBV package from: 164°C/W to: 263.7°C/W 5
- Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 264.4°C/W 5
- Changed Junction-to-top characterization value for DBV package from: 44°C/W to: 195.6°C/W 5
- Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 262.2°C/W 5

- Changed Junction-to-ambient thermal resistance value for DCK package from: 278°C/W to: 371°C/W..... 5
- Changed Junction-to-case (top) thermal resistance value for DCK package from: 93°C/W to: 297.5°C/W..... 5
- Changed Junction-to-board characterization value for DCK package from: 65°C/W to: 258.6°C/W..... 5
- Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W..... 5
- Changed Junction-to-board characterization value for DCK package from: 64°C/W to: 256.2°C/W..... 5
- Removed redundant t_{pd} specification from *Switching Characteristics, –40°C to 125°C* 7
- Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately"..... 14
- Updated *Overview*, *Application and Implementation*, *Device and Documentation Support* sections to extend detailed feature descriptions and more detailed information. 16

Changes from April 1, 2014 to August 12, 2026 (from Revision X (April 2014) to Revision Y (August 2026)) **Page**

- Updated *Device Information* table to include body and package dimensions..... 1
- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Moved T_{stg} to *Absolute Maximum Ratings* table..... 4
- Changed *Handling Ratings* to *ESD Ratings*..... 4
- Updated format for *Thermal Information* table..... 5
- Changed Junction-to-ambient thermal resistance value for DBV package from: 229°C/W to: 357.1°C/W..... 5
- Changed Junction-to-case (top) thermal resistance value for DBV package from: 164°C/W to: 263.7°C/W..... 5
- Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 264.4°C/W..... 5
- Changed Junction-to-top characterization value for DBV package from: 44°C/W to: 195.6°C/W..... 5
- Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 262.2°C/W..... 5
- Changed Junction-to-ambient thermal resistance value for DCK package from: 278°C/W to: 371°C/W..... 5
- Changed Junction-to-case (top) thermal resistance value for DCK package from: 93°C/W to: 297.5°C/W..... 5
- Changed Junction-to-board characterization value for DCK package from: 65°C/W to: 258.6°C/W..... 5
- Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W..... 5
- Changed Junction-to-board characterization value for DCK package from: 64°C/W to: 256.2°C/W..... 5
- Changed Junction-to-ambient thermal resistance value for DRL package from: 243°C/W to: 364.1°C/W..... 5
- Changed Junction-to-case (top) thermal resistance value for DRL package from: 78°C/W to: 280.6°C/W..... 5
- Changed Junction-to-board characterization value for DRL package from: 78°C/W to: 261.5°C/W..... 5
- Changed Junction-to-top characterization value for DRL package from: 10°C/W to: 195.6°C/W..... 5
- Changed tpd maximum value at V_{CC} = 1.8V ± 0.15V from: 7.2ns to: 7.7ns..... 6
- Changed tpd maximum value at V_{CC} = 2.5V ± 0.2V from: 4.4ns to: 4.5ns..... 6
- Changed tpd maximum value at V_{CC} = 1.8V ± 0.15V from: 8ns to: 8.4ns..... 6
- Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately"..... 14
- Updated *Overview*, *Application and Implementation*, *Device and Documentation Support* sections to extend detailed feature descriptions and more detailed information. 16

Changes from December 1, 2013 to August 12, 2026 (from Revision L (December 2013) to Revision M (August 2026)) **Page**

- Updated *Device Information* table to include body and package dimensions..... 1
- Added *Applications*, *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section..... 1
- Added Device Information table..... 1
- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Moved T_{stg} to *Absolute Maximum Ratings* table..... 4
- Added *Thermal Information* table..... 5
- Changed Junction-to-ambient thermal resistance value for DBV package from: 206°C/W to: 357.1°C/W..... 5

- Changed Junction-to-ambient thermal resistance value for DCK package from: 252°C/W to: 371°C/W..... 5
- Updated *Overview*, *Application and Implementation*, *Device and Documentation Support* sections to extend detailed feature descriptions and more detailed information. 9
- Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately"..... 14

Changes from November 1, 2016 to August 12, 2026 (from Revision S (November 2016) to Revision T (August 2026)) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Added *Thermal Information* table..... 5
- Changed Junction-to-ambient thermal resistance value for DBV package from: 243.4°C/W to: 357.1°C/W..... 5
- Changed Junction-to-case (top) thermal resistance value for DBV package from: 179°C/W to: 263.7°C/W..... 5
- Changed Junction-to-board characterization value for DBV package from: 77.6°C/W to: 264.4°C/W..... 5
- Changed Junction-to-top characterization value for DBV package from: 58.4°C/W to: 195.6°C/W..... 5
- Changed Junction-to-board characterization value for DBV package from: 77°C/W to: 262.2°C/W..... 5
- Changed Junction-to-ambient thermal resistance value for DCK package from: 278.9°C/W to: 371°C/W..... 5
- Changed Junction-to-case (top) thermal resistance value for DCK package from: 121.3°C/W to: 297.5°C/W.. 5
- Changed Junction-to-board characterization value for DCK package from: 65.6°C/W to: 258.6°C/W..... 5
- Changed Junction-to-top characterization value for DCK package from: 7.5°C/W to: 195.6°C/W..... 5
- Changed Junction-to-board characterization value for DCK package from: 64.9°C/W to: 256.2°C/W..... 5

Changes from August 1, 2015 to August 12, 2026 (from Revision V (August 2015) to Revision W (August 2026)) **Page**

- Updated *Device Information* table to include body and package dimensions..... 1
- Added *Applications*, *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section..... 1
- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Added *Thermal Information* table..... 6
- Changed Junction-to-ambient thermal resistance value for DBV package from: 229°C/W to: 357.1°C/W..... 6
- Changed Junction-to-case (top) thermal resistance value for DBV package from: 164°C/W to: 263.7°C/W..... 6
- Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 264.4°C/W..... 6
- Changed Junction-to-top characterization value for DBV package from: 44°C/W to: 195.6°C/W..... 6
- Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 262.2°C/W..... 6
- Changed Junction-to-ambient thermal resistance value for DCK package from: 278°C/W to: 371°C/W..... 6
- Changed Junction-to-case (top) thermal resistance value for DCK package from: 93°C/W to: 297.5°C/W..... 6
- Changed Junction-to-board characterization value for DCK package from: 65°C/W to: 258.6°C/W..... 6
- Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W..... 6
- Changed Junction-to-board characterization value for DCK package from: 64°C/W to: 256.2°C/W..... 6
- Changed Junction-to-ambient thermal resistance value for DRL package from: 243°C/W to: 364.1°C/W..... 6
- Changed Junction-to-case (top) thermal resistance value for DRL package from: 78°C/W to: 280.6°C/W..... 6
- Changed Junction-to-board characterization value for DRL package from: 78°C/W to: 261.5°C/W..... 6
- Changed Junction-to-top characterization value for DRL package from: 10°C/W to: 195.6°C/W..... 6
- Changed Junction-to-board characterization value for DRL package from: 77°C/W to: 259.2°C/W..... 6
- Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately"..... 15
- Updated *Overview*, *Application and Implementation*, *Device and Documentation Support* sections to extend detailed feature descriptions and more detailed information. 17

Changes from February 1, 2014 to June 1, 2026 (from Revision R (February 2014) to Revision S (August 2026)) **Page**

- Updated *Device Information* table to include body and package dimensions..... 1
- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Updated format for *Thermal Information* table.....5
- Extended *Thermal Information* table to include $R_{\theta JC(top)}$, $R_{\theta JB}$, Ψ_{JT}, Ψ_{JB}, $R_{\theta JC(bot)}$ 5
- Changed Junction-to-ambient thermal resistance value for DBV package from: 206°C/W to: 357.1°C/W..... 5
- Changed Junction-to-ambient thermal resistance value for DCK package from: 252°C/W to: 371°C/W.....5
- Changed Junction-to-ambient thermal resistance value for DRL package from: 142°C/W to: 364.1°C/W..... 5
- Updated *Overview*, *Application and Implementation*, *Device and Documentation Support* sections to extend detailed feature descriptions and more detailed information. 9
- Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately".....15

Changes from May 1, 2019 to August 12, 2026 (from Revision Z (May 2019) to Revision AA (August 2026)) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Updated *Device Information* table to include body and package dimensions..... 1
- Updated format for *Thermal Information* table.....5
- Changed Junction-to-ambient thermal resistance value for DBV package from: 207.6°C/W to: 357.1°C/W..... 5
- Changed Junction-to-case (top) thermal resistance value for DBV package from: 145.2°C/W to: 263.7°C/W..5
- Changed Junction-to-board characterization value for DBV package from: 53.5°C/W to: 264.4°C/W.....5
- Changed Junction-to-top characterization value for DBV package from: 37.5°C/W to: 195.6°C/W.....5
- Changed Junction-to-board characterization value for DBV package from: 53.1°C/W to: 262.2°C/W.....5
- Changed Junction-to-ambient thermal resistance value for DCK package from: 283.1°C/W to: 371°C/W.....5
- Changed Junction-to-case (top) thermal resistance value for DCK package from: 92.3°C/W to: 297.5°C/W....5
- Changed Junction-to-board characterization value for DCK package from: 60.9°C/W to: 258.6°C/W.....5
- Changed Junction-to-top characterization value for DCK package from: 1.7°C/W to: 195.6°C/W.....5
- Changed Junction-to-board characterization value for DCK package from: 60.1°C/W to: 256.2°C/W.....5
- Changed Junction-to-ambient thermal resistance value for DRL package from: 242.9°C/W to: 364.1°C/W..... 5
- Changed Junction-to-case (top) thermal resistance value for DRL package from: 77.5°C/W to: 280.6°C/W.... 5
- Changed Junction-to-board characterization value for DRL package from: 77.5°C/W to: 261.5°C/W.....5
- Changed Junction-to-top characterization value for DRL package from: 9.6°C/W to: 195.6°C/W..... 5
- Changed Junction-to-board characterization value for DRL package from: 77.3°C/W to: 259.2°C/W.....5
- Updated *Overview*, *Application and Implementation*, *Device and Documentation Support* sections to extend detailed feature descriptions and more detailed information. 9
- Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately".....14

Changes from April 1, 2014 to August 12, 2026 (from Revision D (June 2017) to Revision E (August 2026)) **Page**

- Updated *Device Information* table to include body and package dimensions..... 1
- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Updated format for *Thermal Information* table.....5
- Extended *Thermal Information* table to include $R_{\theta JC(top)}$, $R_{\theta JB}$, Ψ_{JT}, Ψ_{JB}, $R_{\theta JC(bot)}$ 5
- Changed Junction-to-ambient thermal resistance value for DBV package from: 206°C/W to: 357.1°C/W..... 5
- Changed Junction-to-ambient thermal resistance value for DCK package from: 252°C/W to: 371°C/W..... 5
- Updated *Overview*, *Application and Implementation*, *Device and Documentation Support* sections to extend detailed feature descriptions and more detailed information. 9
- Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately".....14

Changes from February 1, 2020 to August 12, 2026 (from Revision G (February 2020) to Revision H (August 2026)) **Page**

- Updated *Device Information* table to include body and package dimensions..... 1
- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Added *Thermal Information* table..... 5
- Changed Junction-to-ambient thermal resistance value for DBV package from: 247.2°C/W to: 357.1°C/W..... 5
- Changed Junction-to-case (top) thermal resistance value for DBV package from: 154.5°C/W to: 263.7°C/W..5
- Changed Junction-to-board characterization value for DBV package from: 86.8°C/W to: 264.4°C/W.....5
- Changed Junction-to-top characterization value for DBV package from: 58°C/W to: 195.6°C/W.....5
- Changed Junction-to-board characterization value for DBV package from: 86.4°C/W to: 262.2°C/W.....5
- Changed Junction-to-ambient thermal resistance value for DCK package from: 276.1°C/W to: 371°C/W.....5
- Changed Junction-to-case (top) thermal resistance value for DCK package from: 178.9°C/W to: 297.5°C/W..5
- Changed Junction-to-board characterization value for DCK package from: 70.9°C/W to: 258.6°C/W.....5
- Changed Junction-to-top characterization value for DCK package from: 47°C/W to: 195.6°C/W.....5
- Changed Junction-to-board characterization value for DCK package from: 69.3°C/W to: 256.2°C/W.....5

Changes from April 1, 2017 to August 12, 2026 (from Revision U (April 2017) to Revision V (August 2026)) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Changed Junction-to-ambient thermal resistance value for DBV package from: 247.2°C/W to: 357.1°C/W..... 5
- Changed Junction-to-case (top) thermal resistance value for DBV package from: 154.5°C/W to: 263.7°C/W..5
- Changed Junction-to-board characterization value for DBV package from: 86.8°C/W to: 264.4°C/W.....5
- Changed Junction-to-top characterization value for DBV package from: 58°C/W to: 195.6°C/W.....5
- Changed Junction-to-board characterization value for DBV package from: 86.4°C/W to: 262.2°C/W.....5
- Changed Junction-to-ambient thermal resistance value for DCK package from: 277.6°C/W to: 371°C/W.....5
- Changed Junction-to-case (top) thermal resistance value for DCK package from: 179.5°C/W to: 297.5°C/W..5
- Changed Junction-to-board characterization value for DCK package from: 75.9°C/W to: 258.6°C/W.....5
- Changed Junction-to-top characterization value for DCK package from: 49.7°C/W to: 195.6°C/W.....5
- Changed Junction-to-board characterization value for DCK package from: 75.1°C/W to: 256.2°C/W.....5
- Changed Junction-to-ambient thermal resistance value for DRL package from: 294.3°C/W to: 364.1°C/W..... 5
- Changed Junction-to-case (top) thermal resistance value for DRL package from: 129.9°C/W to: 280.6°C/W..5
- Changed Junction-to-board characterization value for DRL package from: 143.4°C/W to: 261.5°C/W.....5
- Changed Junction-to-top characterization value for DRL package from: 14.3°C/W to: 195.6°C/W..... 5
- Changed Junction-to-board characterization value for DRL package from: 144°C/W to: 259.2°C/W.....5
- Added *Thermal Information* table..... 5

Changes from October 1, 2014 to August 13, 2026 (from Revision T (October 2014) to Revision U (August 2026)) **Page**

- Updated *Device Information* table to include body and package dimensions..... 1
- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Changed *Handling Ratings* to *ESD Ratings* 4
- Moved *Storage temperature range* from *Handling Ratings* to *Absolute Maximum Ratings* 4
- Updated format for *Thermal Information* table..... 5
- Changed Junction-to-ambient thermal resistance value for DBV package from: 229°C/W to: 357.1°C/W..... 5
- Changed Junction-to-case (top) thermal resistance value for DBV package from: 164°C/W to: 263.7°C/W..... 5
- Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 264.4°C/W..... 5
- Changed Junction-to-top characterization value for DBV package from: 44°C/W to: 195.6°C/W..... 5
- Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 262.2°C/W..... 5
- Changed Junction-to-ambient thermal resistance value for DCK package from: 278°C/W to: 371°C/W..... 5
- Changed Junction-to-case (top) thermal resistance value for DCK package from: 93°C/W to: 297.5°C/W..... 5
- Changed Junction-to-board characterization value for DCK package from: 65°C/W to: 258.6°C/W..... 5
- Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W..... 5
- Changed Junction-to-board characterization value for DCK package from: 64°C/W to: 256.2°C/W..... 5
- Changed Junction-to-ambient thermal resistance value for DRL package from: 243°C/W to: 364.1°C/W..... 5
- Changed Junction-to-case (top) thermal resistance value for DRL package from: 78°C/W to: 280.6°C/W..... 5
- Changed Junction-to-board characterization value for DRL package from: 78°C/W to: 261.5°C/W..... 5
- Changed Junction-to-top characterization value for DRL package from: 10°C/W to: 195.6°C/W..... 5
- Changed Junction-to-board characterization value for DRL package from: 77°C/W to: 259.2°C/W..... 5
- Updated *Overview*, *Application and Implementation*, *Device and Documentation Support* sections to extend detailed feature descriptions and more detailed information. 9
- Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately"..... 14

Changes from June 1, 2017 to August 12, 2026 (from Revision Q (June 2017) to Revision R (August 2026)) **Page**

- Added *Thermal Information* table..... 5
- Changed Junction-to-ambient thermal resistance value for DBV package from: 206°C/W to: 357.1°C/W..... 5
- Changed Junction-to-ambient thermal resistance value for DCK package from: 252°C/W to: 371°C/W..... 5
- Changed tpd maximum value for V_{CC} = 2.5V ± 0.2V from: 4.5ns to: 4.9ns..... 6

Product Folder	Current Datasheet Number	New Datasheet Number	Link to full datasheet
SN74LVC1G00	SCES212AB	SCES212AC	http://www.ti.com/product/SN74LVC1G00
SN74LVC1G02	SCES213X	SCES213Y	http://www.ti.com/product/SN74LVC1G02
SN74LVC1G240	SCES305L	SCES305M	http://www.ti.com/product/SN74LVC1G240
SN74LVC1G80	SCES221S	SCES221T	http://www.ti.com/product/SN74LVC1G80
SN74LVC1G32	SCES219V	SCES219W	http://www.ti.com/product/SN74LVC1G32
SN74LVC1G126	SCES224R	SCES224S	http://www.ti.com/product/

			SN74LVC1G126
SN74LVC1G08	SCES217Z	SCES217AA	http://www.ti.com/product/SN74LVC1G08
SN74LVC1G132	SCES546D	SCES546E	http://www.ti.com/product/SN74LVC1G132
SN74LVC1G38	SCES538G	SCES538H	http://www.ti.com/product/SN74LVC1G38
SN74LVC1G79	SCES220U	SCES220V	http://www.ti.com/product/SN74LVC1G79
SN74LVC1G125	SCES223T	SCES223U	http://www.ti.com/product/SN74LVC1G125
SN74LVC1G86	SCES222Q	SCES222R	http://www.ti.com/product/SN74LVC1G86

Qual details are provided in the Qual Data Section.
Test coverage, insertions, conditions will remain consistent with current testing.

Reason for Change:	Supply Continuity

Anticipated impact on Form, Fit, Function, Quality or Reliability:	These devices include new die based on existing schematics in a larger diameter wafer fab with a die shrink. There are changes in the electrical tables. Physical aspects of the device have changed. Request the Supporting Data Packet (SDP) for more details on the changes. Evaluating samples is encouraged.
Impact on Environmental Ratings	Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.

RoHS	REACH	Green Status	IEC 62474
☒ No Change	☒ No Change	☒ No Change	☒ No Change

Changes to product identification resulting from this PCN:

Fab Site Information

Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
FFAB	TID	DEU	Freising
RFAB	RFB	USA	Richardson

Die Rev:

Current	New
Die Rev [2P]	**Die Rev [2P]**
D, E	A

Assembly Site

Information

Assembly Site	Assembly Site Origin (22L)	Assembly Country Code (23L)	Assembly City
TFME	NFM	CHN	Chongchuan
TIPI	PHI	PHL	Baguio city

Sample product shipping label (not actual product label):



Group 1 Products Affected: (Fab, Design, Marking)

SN74LVC1G00DBVR	SN74LVC1G126DBVR.A	SN74LVC1G38DBVR
SN74LVC1G02DBVR	SN74LVC1G132DBVR	SN74LVC1G79DBVR
SN74LVC1G08DBVR	SN74LVC1G240DBVR	SN74LVC1G80DBVR
SN74LVC1G125DBVR	SN74LVC1G32DBVR	SN74LVC1G86DBVR
SN74LVC1G126DBVR	SN74LVC1G32DBVR.A	

Group 2 Products Affected: (Fab, Design, Assembly site, Marking)

74LVC1G126DBVRG4	SN74LVC1G08DBVRG4
74LVC1G126DBVRE4	SN74LVC1G08DBVRE4

Group 1 Qualification Report

Approve Date 19-March -2026

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Name	Condition	Duration	Qual Device: SN74LVC1G08DBVR	Qual Device: SN74LVC1G125DBVR	Qual Device: SN74LVC1G38DBVR	Qual Device: SN74LVC1G132DBVR	QBS Package Reference: TLV1805QDBVRQ1	QBS Process Reference: SN74HCS74QPWRQ1	QBS Package Reference: SN74LVC1G16DBVRQ1	QBS Process, Product Reference: SN74LVC1G08DTXRQ1	QBS Product Reference: SN74LVC1G09DBVRQ1	QBS Product Reference: SN74LVC1G08QDBVRQ1	QBS Product Reference: CLVC1G125QDBVRQ1
HAST	A2	Biased HAST	130C/85%RH	96 Hours	-	-	-	-	3/231/0	-	1/77/0	-	-	-	-
UHAST	A3	Autoclave	121C/15psig	96 Hours	-	-	-	-	3/231/0	-	-	-	-	-	-
UHAST	A3	Unbiased HAST	130C/85%RH	96 Hours	-	-	-	-	-	-	1/77/0	-	-	-	-
TC	A4	Temperature Cycle	-65C/150C	500 Cycles	-	-	-	-	3/231/0	-	1/77/0	-	-	-	-
HTSL	A6	High Temperature Storage Life	175C	500 Hours	-	-	-	-	3/135/0	-	1/45/0	-	-	-	-
HTOL	B1	Life Test	125C	1000 Hours	-	-	-	-	-	3/231/0	-	-	-	-	-
HTOL	B1	Life Test	150C	300 Hours	-	-	-	-	-	-	-	1/77/0	-	-	-
ELFR	B2	Early Life Failure Rate	125C	48 Hours	-	-	-	-	-	3/2400/0	-	-	-	-	-
SD	C3	PB Solderability	Precondition w.155C Dry Bake (4 hrs +/- 15 minutes)	-	-	-	-	-	1/15/0	-	-	-	-	-	-
SD	C3	PB-Free Solderability	Precondition w.155C Dry Bake (4 hrs +/- 15 minutes)	-	-	-	-	-	1/15/0	-	1/15/0	-	-	-	-
PD	C4	Physical Dimensions	Cpk>1.67	-	-	-	-	-	3/30/0	-	1/10/0	1/10/0	-	-	-
ESD	E2	ESD CDM	-	500 Volts	-	-	-	-	-	-	-	1/3/0	1/3/0	1/3/0	1/3/0
ESD	E2	ESD HBM	-	2000 Volts	-	-	-	-	-	-	-	1/3/0	1/3/0	1/3/0	1/3/0
LU	E4	Latch-Up	Per JESD78	-	-	-	-	-	-	-	-	1/3/0	1/3/0	1/3/0	1/3/0
CHAR	E5	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	-	-	-	-	-	-	-	3/90/0	1/30/0	1/30/0	1/30/0

QBS: Qual By Similarity, also known as Generic Data
Qual Device SN74LVC1G08DBVR is qualified at MSL1 260C
Qual Device SN74LVC1G125DBVR is qualified at MSL1 260C
Qual Device SN74LVC1G38DBVR is qualified at MSL1 260C
Qual Device SN74LVC1G132DBVR is qualified at MSL1 260C
Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles
Quality and Environmental data is available at TI's external Web site: http://www.ti.com/
TI Qualification ID: R-CHG-2603-025

Group 2 Qualification Report

Approve Date 19-March -2026

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Name	Condition	Duration	Qual Device: SN74LVC1G08DBVRG4	Qual Device: 74LVC1G126DBVRG4	QBS Package Reference: TLV1805QDBVRQ1	QBS Process Reference: SN74HCS74QPWRQ1	QBS Package, Process, Product Reference: SN74LVC1G09DBVRQ1	QBS Product Reference: SN74LVC1G08QDBVRQ1	QBS Product Reference: CLVC1G125QDBVRQ1
HAST	A2	Biased HAST	130C/85%RH	96 Hours	-	-	3/231/0	-	1/77/0	-	-
UHAST	A3	Autoclave	121C/15psig	96 Hours	-	-	3/231/0	-	-	-	-
UHAST	A3	Unbiased HAST	130C/85%RH	96 Hours	-	-	-	-	1/77/0	-	-
TC	A4	Temperature Cycle	-65C/150C	500 Cycles	-	-	3/231/0	-	1/77/0	-	-
HTSL	A6	High Temperature Storage Life	150C	1000 Hours	-	-	-	-	1/45/0	-	-
HTSL	A6	High Temperature Storage Life	175C	500 Hours	-	-	3/135/0	-	-	-	-
HTOL	B1	Life Test	125C	1000 Hours	-	-	3/231/0	3/231/0	-	-	-
ELFR	B2	Early Life Failure Rate	125C	48 Hours	-	-	-	3/2400/0	-	-	-
SD	C3	PB Solderability	Precondition w.155C Dry Bake (4 hrs +/- 15 minutes)	-	-	-	1/15/0	1/15/0	-	-	-
SD	C3	PB-Free Solderability	Precondition w.155C Dry Bake (4 hrs +/- 15 minutes)	-	-	-	1/15/0	1/15/0	1/15/0	-	-
PD	C4	Physical Dimensions	Cpk>1.67	-	-	-	3/30/0	3/30/0	1/10/0	-	-
ESD	E2	ESD CDM	-	500 Volts	-	-	-	-	-	1/3/0	1/3/0
ESD	E2	ESD HBM	-	2000 Volts	-	-	-	-	1/3/0	1/3/0	1/3/0
LU	E4	Latch-Up	Per JESD78	-	-	-	-	-	1/3/0	1/3/0	1/3/0
CHAR	E5	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	-	-	-	-	1/30/0	1/30/0	1/30/0

QBS: Qual By Similarity, also known as Generic Data
Qual Device SN74LVC1G08DBVRG4 is qualified at MSL1 260C
Qual Device 74LVC1G126DBVRG4 is qualified at MSL1 260C
Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles
Quality and Environmental data is available at TI's external Web site: http://www.ti.com/
TI Qualification ID: R-CHG-2512-006

Qualification Report
Automotive Qualification Summary
(As per AEC-Q100 Rev. J and JEDEC Guidelines)

Approve Date 17-March -202

Product Attributes

Attributes	Qual Device: SN74LVC1G08QDBVRQ1	Qual Device: CLVC1G125QDBVRQ1	QBS Package Reference: TLV1805QDBVRQ1	QBS Process Reference: SN74HCS74QPWRQ1	QBS Package Reference: SN74LVC1G16DBVRQ1	QBS Process, Product Reference: SN74LVC1G08DTXRQ1	QBS Package, Product Reference: SN74LVC1G09DBVRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Logic	Logic	Signal Chain	Logic	Logic	Logic	Logic
Wafer Fab Supplier	PFAB	PFAB	PFAB	PFAB	PFAB	PFAB	PFAB
Assembly Site	PHI	PHI	PHI	MLA	PHI	CDAT	PHI
Package Group	SOT	SOT	SOT	TSSOP	SOT	UXQFN	SOT
Package Designator	DBV	DBV	DBV	PW	DBV	DTX	DBV
Pin Count	5	5	6	14	5	5	5

QBS: Qual By Similarity, also known as Generic Data
Qual Device SN74LVC1G08QDBVRQ1 is qualified at MSL1 260C
Qual Device CLVC1G125QDBVRQ1 is qualified at MSL1 26

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: SN74LVC1G08QDBVRQ1	Qual Device: CLVC1G125QDBVRQ1	QBS Package Reference: TLV1805QDBVRQ1	QBS Process Reference: SN74HCS74QPWRQ1	QBS Package Reference: SN74LVC1G16DBVRQ1	QBS Process, Product Reference: SN74LVC1G08DTXRQ1	QBS Package, Product Reference: SN74LVC1G09DBVRQ1
Test Group A - Accelerated Environment Stress Tests														
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	-	-	3/All/0	-	1/All/0	-	1/All/0
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	-	3/231/0	-	1/77/0	-	1/77/0
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Autoclave	121C/15psig	96 Hours	-	-	3/231/0	-	-	-	-

AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	-	-	-	-	1/77/0	-	1/77/0
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	-	-	3/231/0	-	1/77/0	-	1/77/0
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	-	-	1/5/0	-	1/5/0	-	1/5/0
TC-SAM	A4	-	3	3	Post TC SAM	<50% delamination	-	-	-	-	-	1/12/0	-	1/12/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	-	-	-	-	-	-	1/45/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	175C	500 Hours	-	-	3/135/0	-	1/45/0	-	-
Test Group B - Accelerated Lifetime Simulation Tests														
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	-	-	-	3/231/0	-	-	-
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	150C	300 Hours	-	-	-	-	-	1/77/0	-
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	-	-	-	3/2400/0	-	-	-
Test Group C - Package Assembly Integrity Tests														
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-	-	3/90/0	-	1/30/0	-	1/30/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-	-	3/90/0	-	1/30/0	-	1/30/0
SD	C3	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	-	1/15/0	-	-	-	-
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	-	1/15/0	-	1/15/0	-	1/15/0
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	-	-	3/30/0	-	1/10/0	-	1/10/0
Test Group D - Die Fabrication Reliability Tests														
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDB	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests														
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	2000 Volts	1/3/0	1/3/0	-	-	-	-	1/3/0
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	500 Volts	1/3/0	1/3/0	-	-	-	-	-
LU	E4	AEC Q100-004	1	3	Latch-Up	Per AEC Q100-004	-	1/3/0	1/3/0	-	-	-	-	1/3/0
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0	1/30/0	-	-	-	-	1/30/0

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles
Ambient Operating Temperature by Automotive Grade Level:
Grade 0 (or E): -40C to +150C
Grade 1 (or Q): -40C to +125C
Grade 2 (or T): -40C to +105C
Grade 3 (or I) : -40C to +85C
E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):
Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room : AC/uHAST
Quality and Environmental data is available at TI's external Web site: http://www.ti.com/
TI Qualification ID: R-CHG-2507-020

In performing change qualifications, Texas Instruments follows integrated circuit industry standards in performing defect mechanism analysis and failure mechanism-based accelerated environmental testing to ensure wafer fab process, assembly process and product quality and reliability. As encouraged by these standards, TI uses both product-specific and generic (family) data in

qualifying its changes. For devices to be categorized as a 'product qualification family' for generic data purposes, they must share similar product, wafer fab process and assembly process elements. The applicability of generic data (also known at TI as Qualification by Similarity (QBS)) is determined by the Reliability Engineering function following these industry standards. Generic data is shown in the qualification report in columns titled "QBS Process" (for wafer fab process), "QBS Package" (for assembly process) and "QBS Product" (for product family).

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