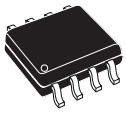
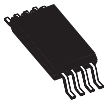
TSC240

Datasheet

High-side and low-side bidirectional zero-drift current sense amplifier with enhanced PWM rejection



SO8



TSSOP8

Maturity status link
TSC240

Features

- AEC-Q100 qualified
- Enhanced PWM rejection
- Excellent CMRR: 132 dB DC CMRR
- Wide common-mode range: –4 V to 100 V
- Accuracy:
  - Gain:
    - Gain error: 0.20% (maximum)
    - Gain drift: 2.5 ppm/°C (maximum)
  - Offset:
    - Offset voltage: ±20 µV (maximum)
    - Offset drift: 150 nV/°C (maximum)
- Available gains:
  - A1: 20 V/V
  - A4: 200 V/V
- Quiescent current: 2.4 mA (maximum)
- SO8 and TSSOP8 packages

Applications

- Motor controls
- Solenoid and valve controls
- Power management
- Industrial process control
- Telecom equipment
- Automotive

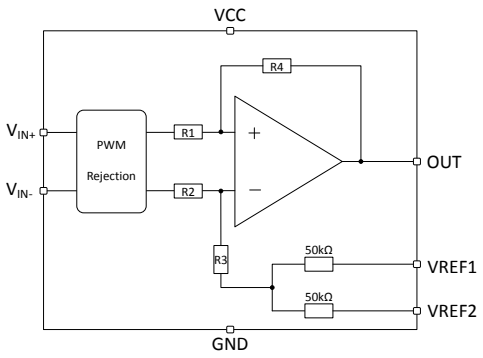
Description

The TSC240 is a high-precision current sense amplifier with enhanced PWM rejection. It can sense current via a shunt resistor over a wide range of common-mode voltages, from -4 to +100 V, regardless of the supply voltage. It is available with a preset gain of 20 and 200 V/V. Thanks to its high precision, it can sense very low drop voltages, minimizing measurement error.

The TSC240 is a current sense amplifier that can be used in various functions such as precision current measurement, overcurrent protection, current monitoring, and feedback loops. These devices fully operate over the broad supply voltage range of 2.7 to 5.5 V and over the industrial temperature range of -40 to +125 °C.

1 Block diagram and pin description

Figure 1. Block diagram



1.1 Pin description

Figure 2. Pin connections (top view)

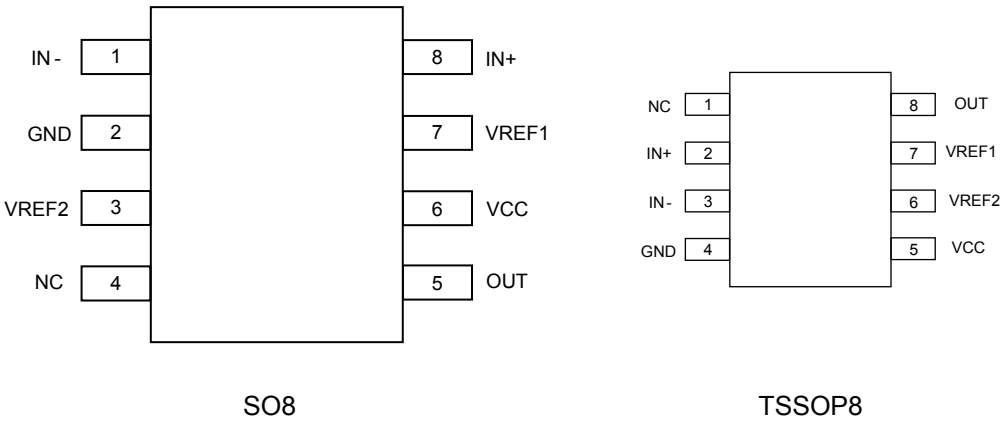


Table 1. Pin description

Pin name	Pin (TSSOP8)	Pin (SO8)	Description
IN-	3	1	Current sense amplifier, negative input
GND	4	2	Ground
REF2	6	3	Reference voltage 2
NC	1	4	Not connected
OUT	8	5	Current sense amplifier, output
VCC	5	6	Supply voltage
REF1	7	7	Reference voltage 1
IN+	2	8	Current sense amplifier, positive input

2 Maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.3 to +6	V
V_{IN+}, V_{IN-}	Differential voltage (V_{IN+}) – (V_{IN-})	-100 to +100	
	Common-mode voltage on input pins	-10 to +110	
REF1, REF2	Voltage on pins REF1, REF2	GND -0.3 to V_{CC}+0.3	
OUT	Analog output	GND -0.3 to V_{CC} +0.3	
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature	-65 to +150	°C
ESD	Human Body Model (HBM)	2000	V
	Charged Device Model (CDM) SO8 TSSOP8	 1000 750	
RTH_{JA}	Thermal resistance junction to ambient SO8 TSSOP8	 125 120	°C/W

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 5.5	V
V_{ICM}	Common-mode voltage on input pins	-4 to +100	V
REF	Reference input range	0 to V_{CC}	V
T	Operating free-air temperature range	-40 to +125	°C

3 Electrical characteristics

V_{CC} = 5 V, V_{ICM} = 12 V, V_{SENSE} = V_{IN+} - V_{IN-}, V_{REF1} = V_{REF2} = V_{CC}/2, T = 25 °C (unless otherwise specified).

Table 4. Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power supply						
I_{CC}	Current consumption	V_{ICM} = -4 to +100 V, V_{SENSE} = 0 mV, T_{min} < T < T_{max}		1.9	2.4 2.6	mA
INPUT						
$\|V_{os}\|$	Offset voltage, RTI	V_{ICM} = 12 V, V_{SENSE} = 0 mV		3	20	µV
		V_{ICM} = 48 V, V_{SENSE} = 0 mV		12	56	
$\|\Delta V_{os}/\Delta T\|$	Offset drift (RTI) vs. temperature (1)	V_{SENSE} = 0 mV, V_{ICM} = 12 and 48 V T_{min} < T < T_{max}		30	150	nV/°C
CMR	Common-mode rejection	V_{IN+} = -4 to +100 V, V_{SENSE} = 0 mV T_{min} < T < T_{max}	120 120	132		dB
		f = 50 kHz		75		
I_{IB}	Input bias current	V_{ICM} = 12 V, I_{IB+}, I_{IB-}, V_{SENSE} = 0 mV T_{min} < T < T_{max}		110	150 150	µA
		V_{ICM} = 48 V, I_{IB+}, I_{IB-}, V_{SENSE} = 0 mV T_{min} < T < T_{max}		210	250 250	
SVR	Supply voltage rejection	V_{CC} = 2.7 to 5.5 V, V_{SENSE} = 0 mV T_{min} < T < T_{max}	 100	120		dB
$\|V_{SENSE}\|$	V_{sense} operating voltage with E_G ≤ 0.2% (2)	TSC240A1, T_{min} < T < T_{max}			239	mV
		TSC240A4, T_{min} < T < T_{max}			23.9	
OUTPUT						
G	Gain	TSC240A1		20		V/V
		TSC240A4		200		
E_G	Gain error	V_{ICM} = 12 and 48 V GND + 100 mV ≤ V_{OUT} ≤ V_{CC} - 100 mV T_{min} < T < T_{max}		±0.05	±0.20 ±0.20	%
$\Delta E_G/\Delta T$	Gain error vs. temperature	T_{min} < T < T_{max}		±0.5	±2.5	ppm/°C
NLE	Non-linearity error	GND + 10 mV ≤ V_{OUT} ≤ V_{CC} - 200 mV		±0.001		%
V_{CC} - V_{OH}	Output swing to the positive rail	RL = 10 kΩ to GND, T_{min} < T < T_{max}		30	 200	mV
V_{OL}	Output swing to GND	RL = 10 kΩ to GND, V_{SENSE} = 0 mV, V_{REF1} = V_{REF2} = 0 V, T_{min} < T < T_{max}		4	 10	
I_{OUT}	Output current	Sink mode, V_{ICM} = 12 and 48 V T_{min} < T < T_{max}	10 8	20	30 40	mA
		Source mode, V_{ICM} = 12 and 48 V T_{min} < T < T_{max}	20 10	26	40 50	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Reg load	Load regulation	I_{OUT} = -5 to +5 mA		0.4	1.5	mV/mA
C_L	Maximum capacitive load	No sustained oscillation		2.2		nF
OFFSET ADJUSTEMENT						
RT	Reference voltage rejection ratio, RTI (3)	TSC240A1		20		µV/V
		TSC240A4		1		
Acc	Reference divider accuracy	$V_{REF1} = V_{CC}$, V_{REF2} = GND, V_{SENSE} = 0 mV $T_{min} < T < T_{max}$		0.02	0.1	%
Dynamic performances						
BW	C_L = 5 pF	TSC240A1, -3dB bandwidth $T_{min} < T < T_{max}$	300 300	560		kHz
		TSC240A4, -3dB bandwidth $T_{min} < T < T_{max}$	200 190	400		
		0.5% THD-N		100		
SR	Slew rate	V_{ICM} = 12 and 48 V $T_{min} < T < T_{max}$	1.4 1.2	2		V/µs
T_S	Settling time	TSC240A1, up to 0.5% of final value (V_{OUT} = 4 V)		3.5		µs
		TSC240A4, up to 0.5% of final value (V_{OUT} = 4 V)		3		
	PWM rejection, settling time	V_{ICM} = [0, 48 V], rise/fall time = 20 ns TSC240A1, up to 0.5% of final value		2.5		µs
Noise, RTI						
En	Voltage noise density			50		nV/√Hz

1. *Guaranteed by design and characterization on a sample of parts, not tested in production.*
2. *$V_{SENSE} = (V_{IN+}) – (V_{IN-})$.*
3. *RTI stands for “Related to input”.*

4 Typical characteristics

TSC240A1 is used for typical characteristics, T_A = 25 °C, V_S = 5 V, V_{ICM} = 12 V and V_{REF} = V_{CC}/2 (unless otherwise specified).

Figure 3. Input offset production distribution

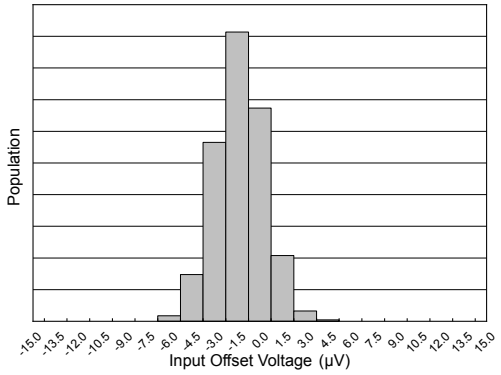


Figure 4. Gain error production distribution

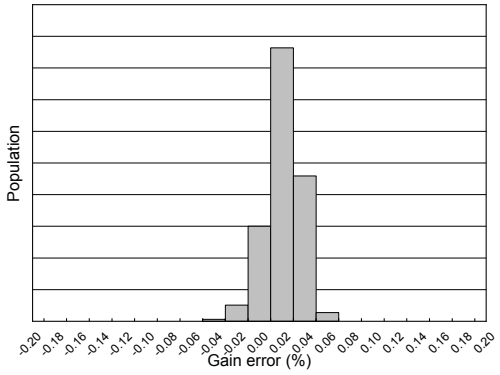


Figure 5. Common-mode rejection ratio production distribution

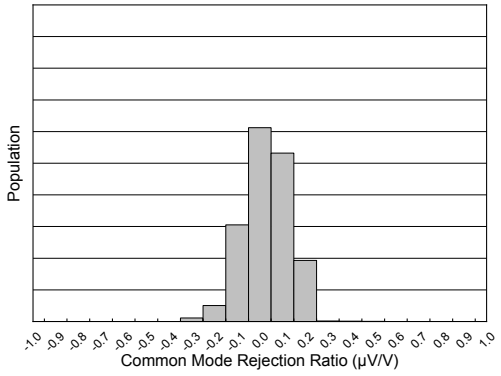


Figure 6. Supply current vs. supply voltage

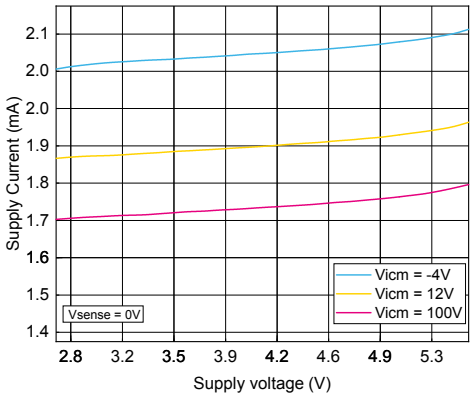


Figure 7. Supply current vs. input common-mode

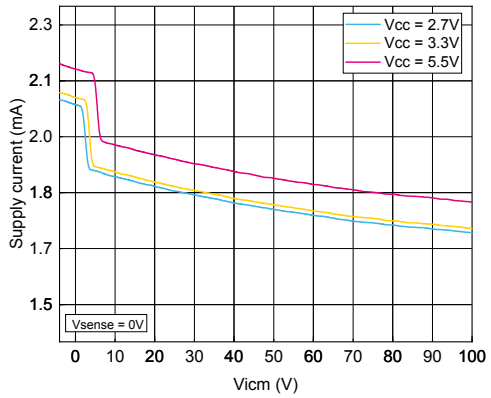


Figure 8. Supply current vs. temperature

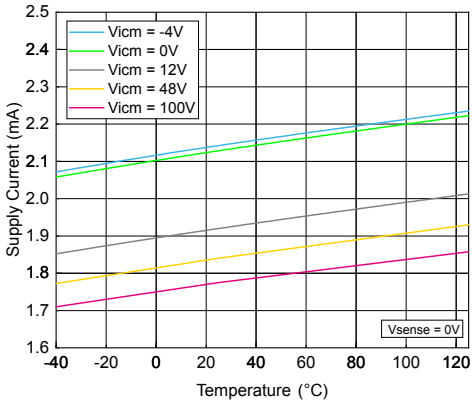


Figure 9. Input bias current vs. common-mode

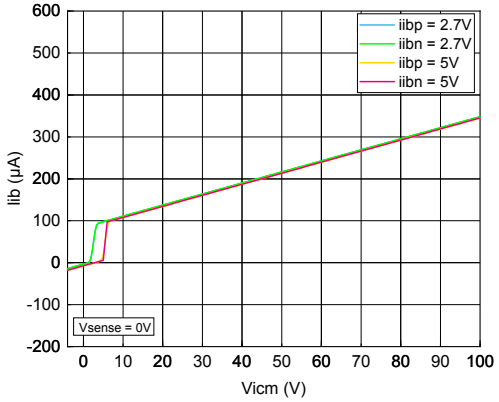


Figure 10. Input bias current vs. temperature

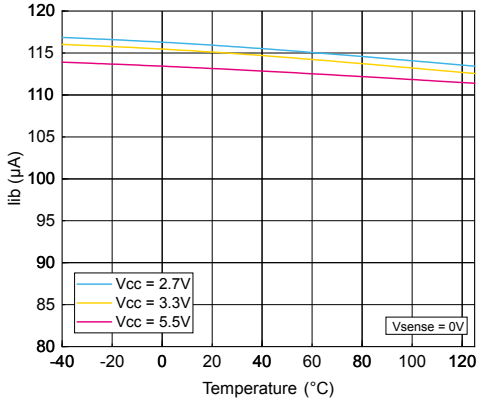


Figure 11. Input bias current vs. input common-mode voltage V_{CC} = 0 V

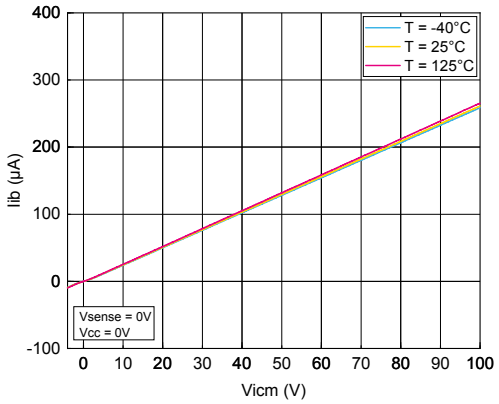


Figure 12. Input bias current vs. V_{SENSE}

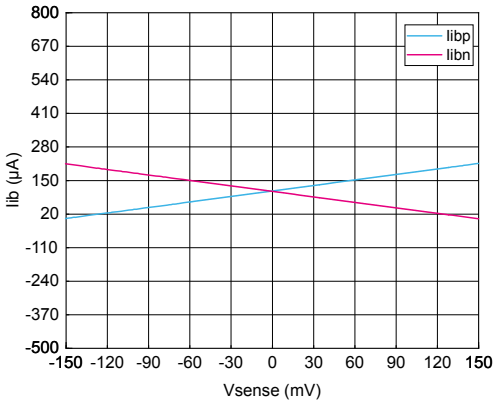


Figure 13. Input offset voltage vs. temperature

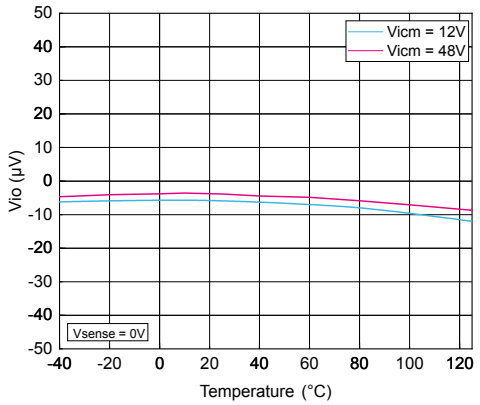


Figure 14. Input offset voltage vs. input common-mode with V_{CC} = 5 V

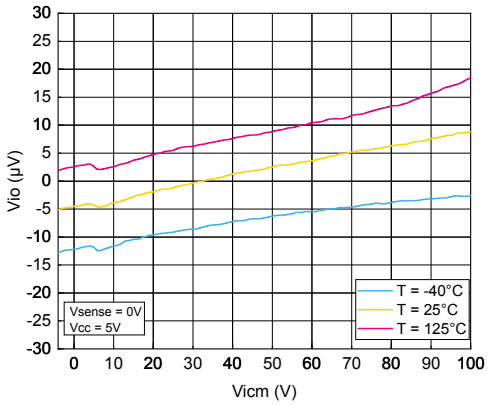


Figure 15. Input offset voltage vs. input common-mode with V_{CC} = 2.7 V

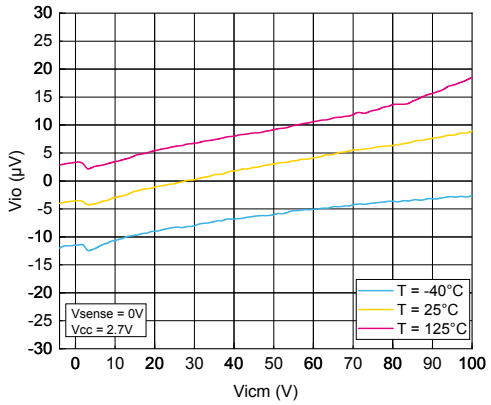


Figure 16. Input offset voltage vs. supply voltage

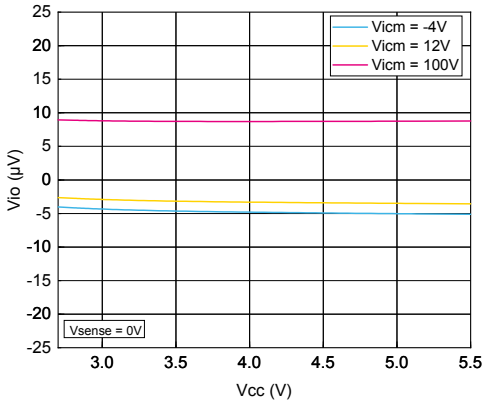


Figure 17. Output current vs. output voltage

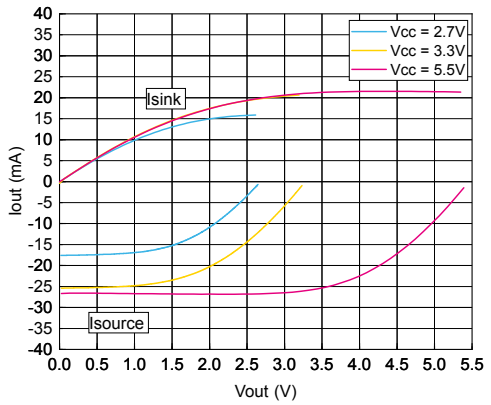


Figure 18. Output current vs. temperature with V_{CC} = 5 V

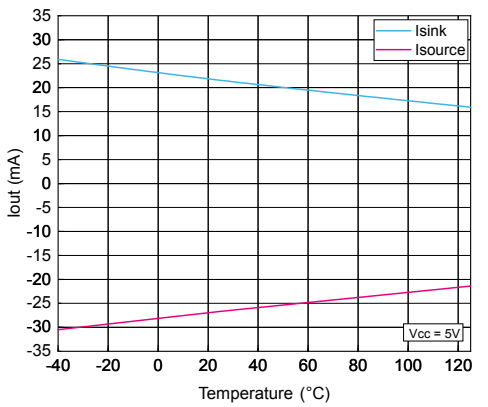


Figure 19. Output current vs. temperature with V_{CC} = 2.7 V

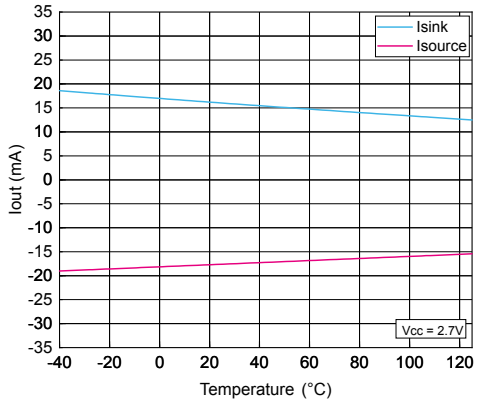


Figure 20. V_{OH} vs. temperature

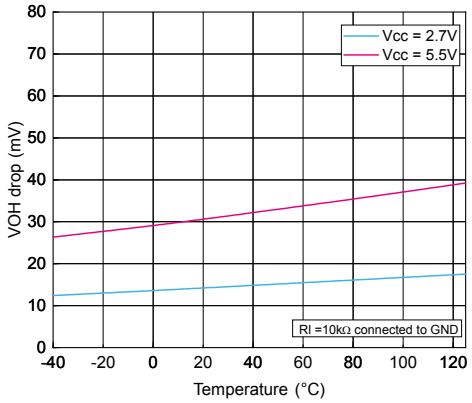


Figure 21. V_{OL} vs. temperature

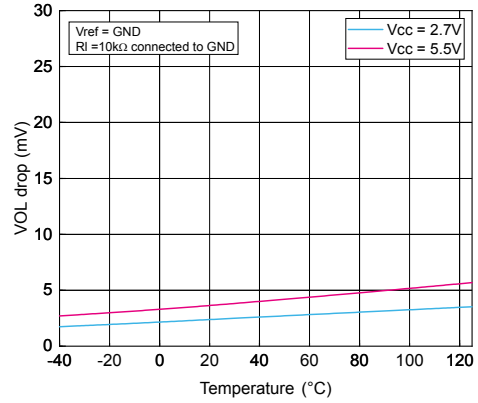


Figure 22. Linearity vs. V_{SENSE}

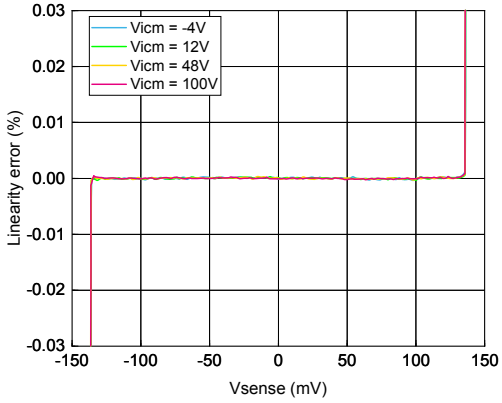


Figure 23. Linearity vs. V_{SENSE} and temperature

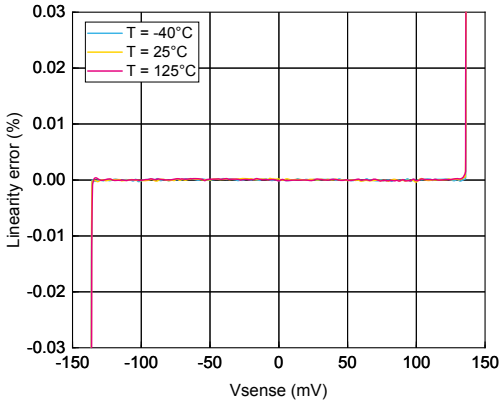


Figure 24. Gain error vs. input common-mode

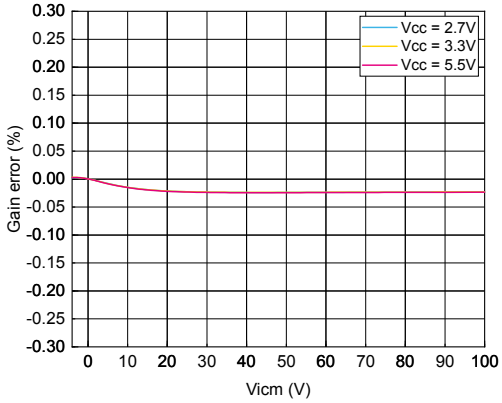


Figure 25. Gain error vs. V_{ICM} and temperature

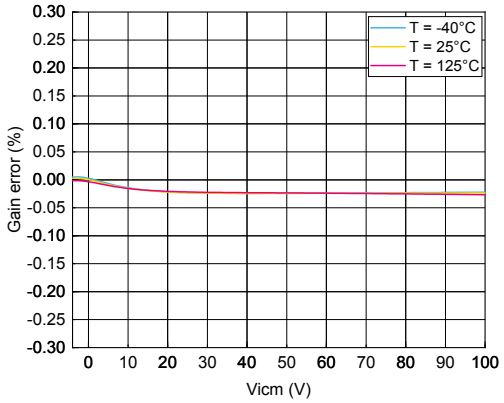


Figure 26. Load regulation

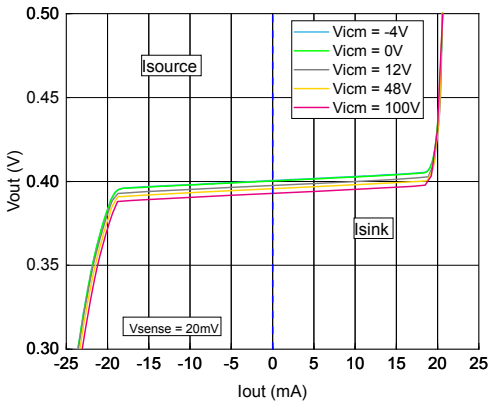


Figure 27. Gain vs. frequency

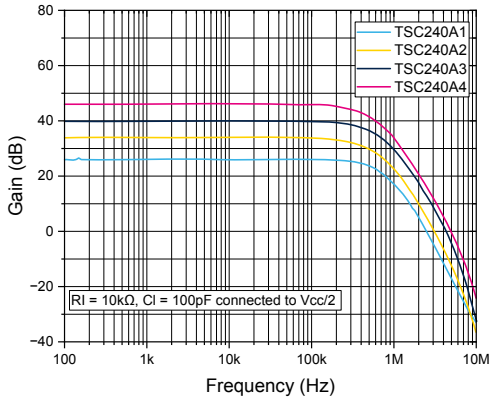


Figure 28. Gain vs. frequency with different capacitive load

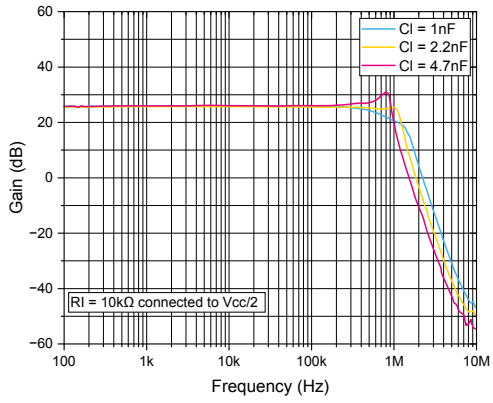


Figure 29. Gain vs. frequency with different capacitive load (TSC240A2)

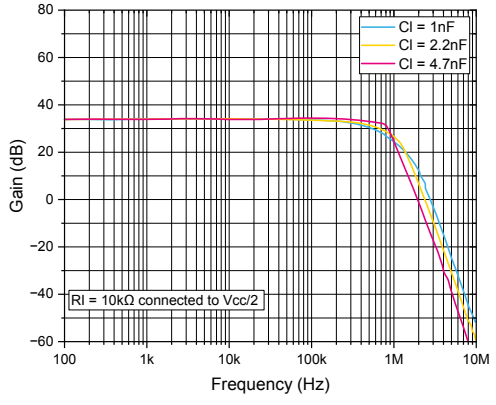


Figure 30. Gain vs. frequency with different capacitive load (TSC240A3)

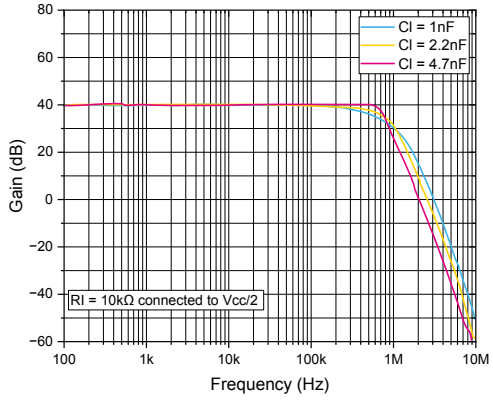


Figure 31. Gain vs. frequency with different capacitive load (TSC240A4)

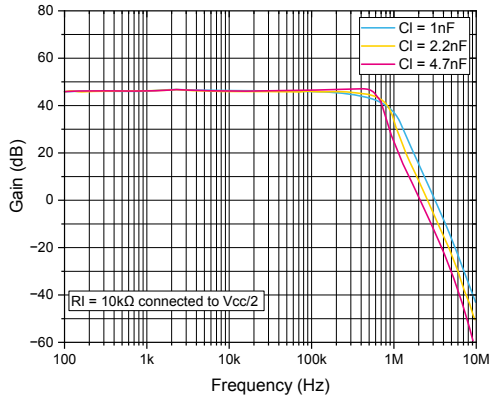


Figure 32. Bandwidth vs. input common-mode

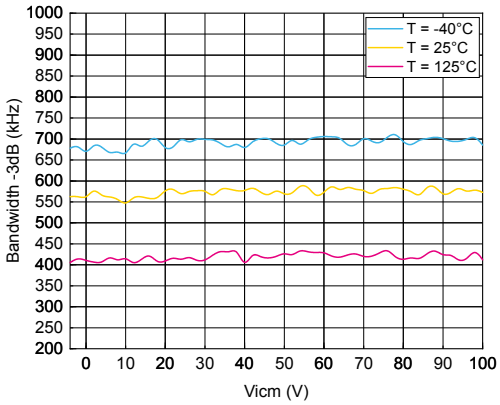


Figure 33. Overshoot vs. capacitive load

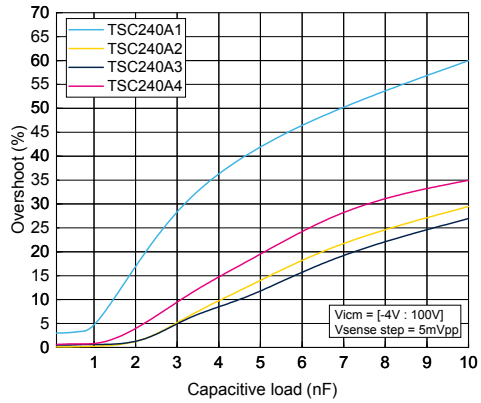


Figure 34. Small signal response

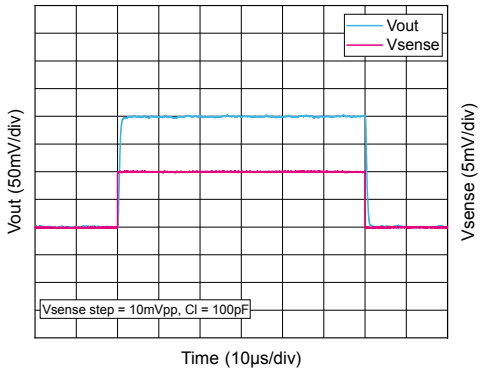


Figure 35. Large signal response

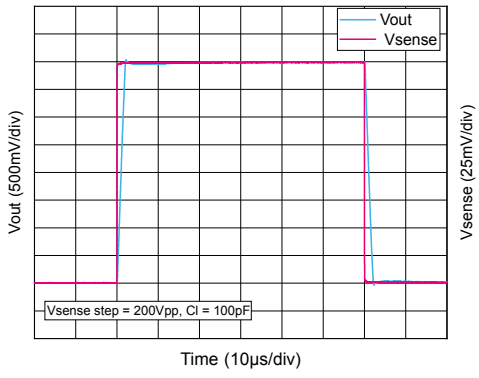


Figure 36. Positive settling time 0.5%

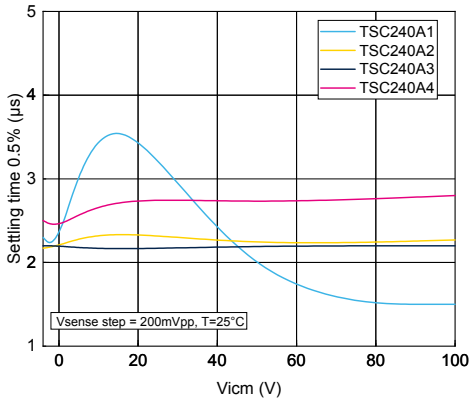


Figure 37. Negative settling time 0.5%

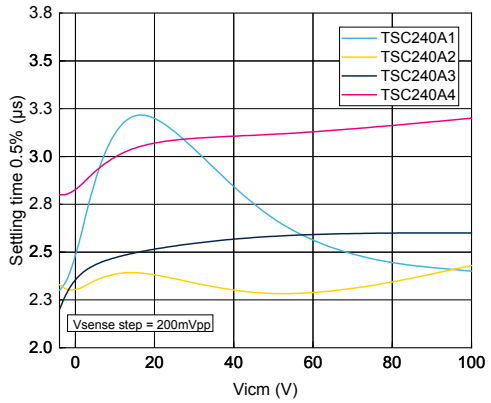


Figure 38. 12 V positive common-mode step response recovery

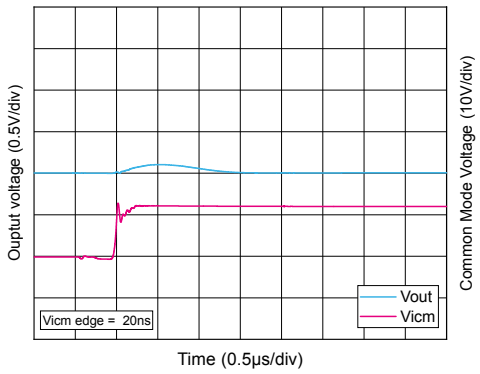


Figure 39. 12 V negative common-mode step response recovery

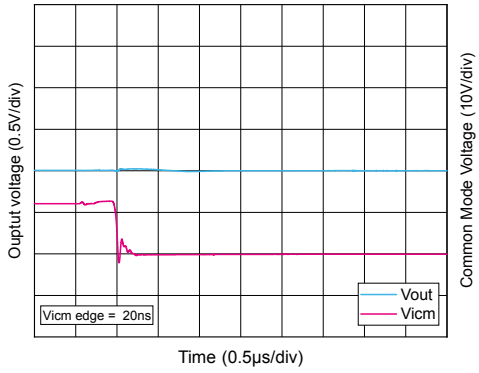


Figure 40. 48 V positive common-mode step response recovery

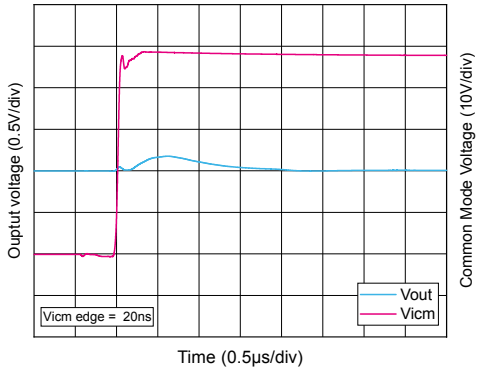


Figure 41. 48 V negative common-mode step response recovery

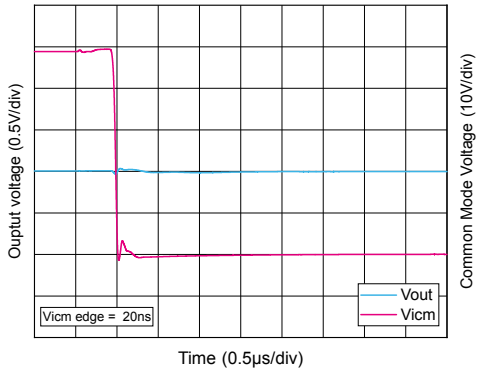


Figure 42. 100 V positive common-mode step response recovery

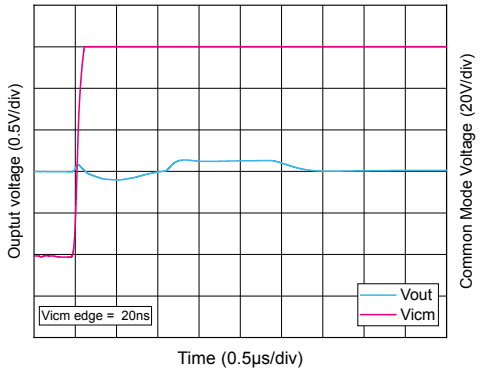


Figure 43. 100 V negative common-mode step response recovery

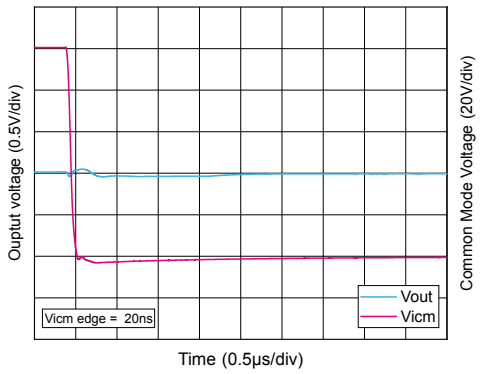


Figure 44. PSRR vs. frequency

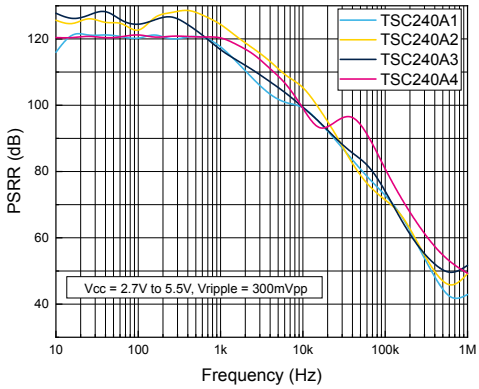


Figure 45. CMRR vs. frequency

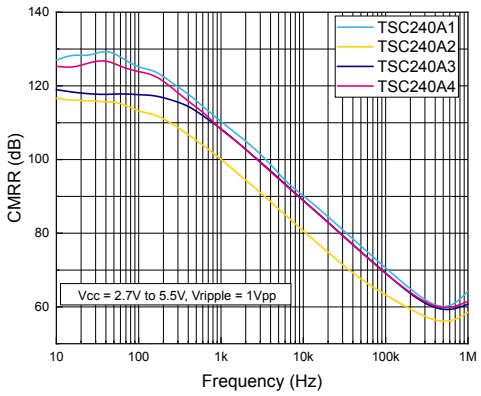


Figure 46. Positive overvoltage recovery

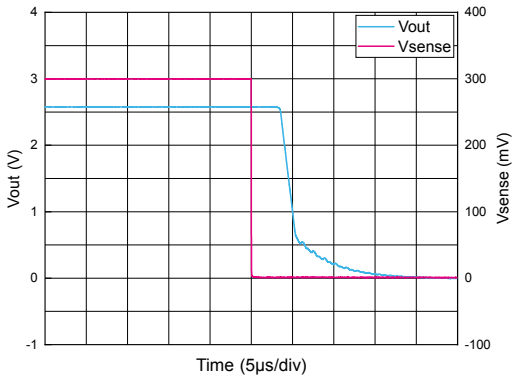


Figure 47. Negative overvoltage recovery

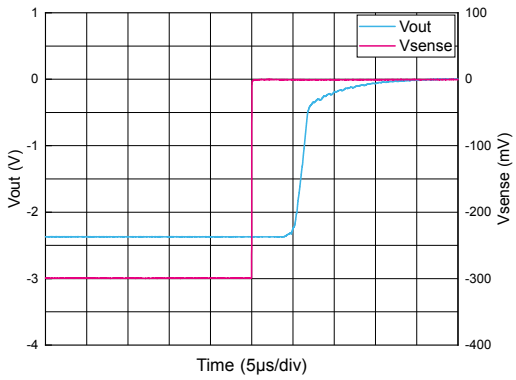


Figure 48. Overvoltage recovery vs. V_{ICM}

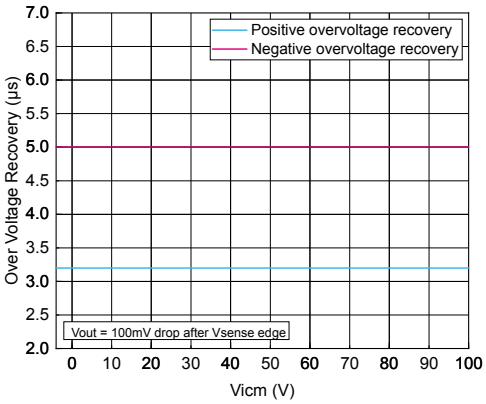


Figure 49. Noise vs. frequency

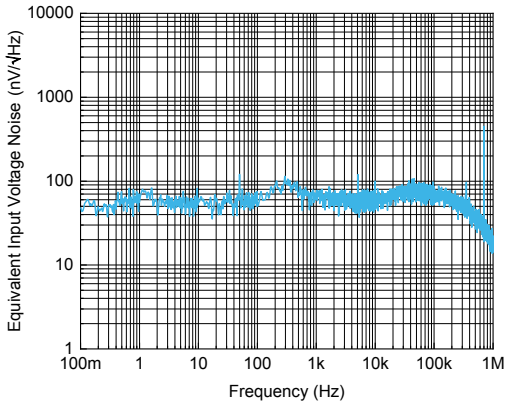


Figure 50. 0.1 Hz to 10 Hz voltage noise

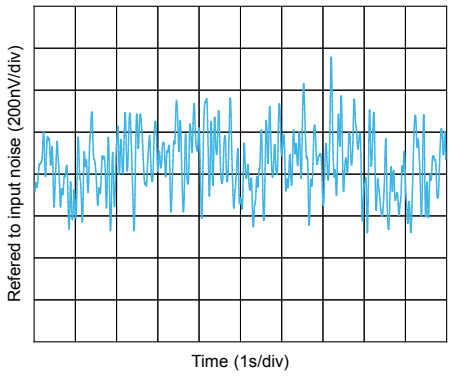


Figure 51. Power-up time delay

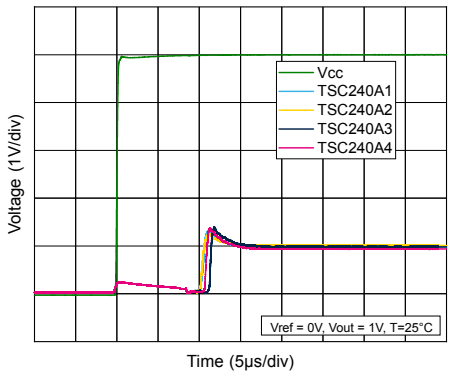
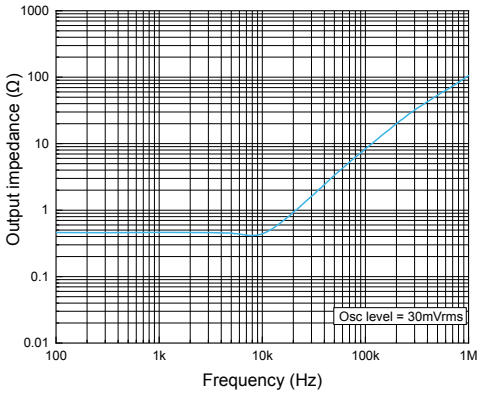


Figure 52. Output impedance vs. frequency



5 Application information

5.1 Overview

The TSC240 series are current sense amplifiers specially designed to accurately measure current by amplifying the voltage across a shunt resistor connected to its input. It is a zero-drift topology, allowing a high CMRR level of min. 120 dB, a high level of input-offset voltage of max. 20 µV at 12 V common-mode voltage, and a very high level of drift at 150 nV/°C.

Multiple fixed gain versions are available (x20, x50, x100, x200) for design optimization. Thanks to the use of a thin film resistor, the TSC240 series offers extremely precise gain and very high CMRR performance, even in a high frequency range. Moreover, the output common-mode voltage can be fixed, allowing the TSC240 series to be used as either a unidirectional or bidirectional current sensing amplifier.

The TSC240 series provides an extended input common range, from -4 V below the negative supply voltage up to 100 V, allowing either low-side or high-side current sensing, while TSC240 series devices can operate from 2.7 to 5.5 V.

The TSC240 series embeds a system to optimize PWM rejection, reducing the effect of fast input common-mode voltage variations on the output signal.

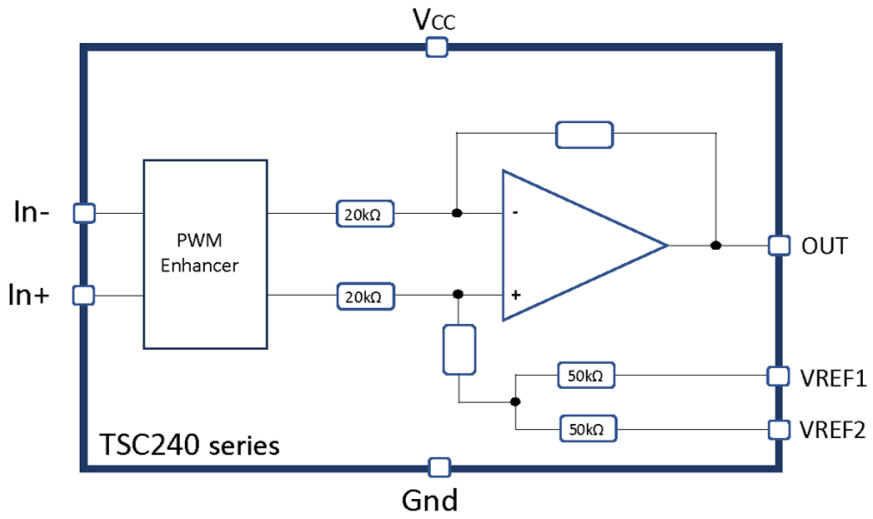
The parameters are very stable over the full V_{CC} range, and several characterization curves show the TSC240 device characteristics at 2.7 V and 5.0 V. Additionally, the main specifications are ensured over extended temperature ranges from -40 to 125 °C.

5.2 Theory of operation

The main feature of the TSC240 series is its ability to work with a wide input common-mode voltage range. It is an excellent device to work with a 48 V application, as the TSC240 series can support and measure the current online at voltages up to 100 V without any additional protective components. It is also a good candidate for use in low-side configurations. It can also support, without any additional protection, fast current variations into a shunt, which is always slightly inductive, thanks to its ability to work with a negative common-mode voltage down to -4 V,

The TSC240 series family embeds a PWM enhancer, allowing it to be used in applications dealing with fast variations of input common-mode voltage, such as motor control or solenoid valve. Its excellent DC performance makes the TSC240 series an ideal device to accurately measure the current. Figure 53 provides a global overview of the TSC240 series.

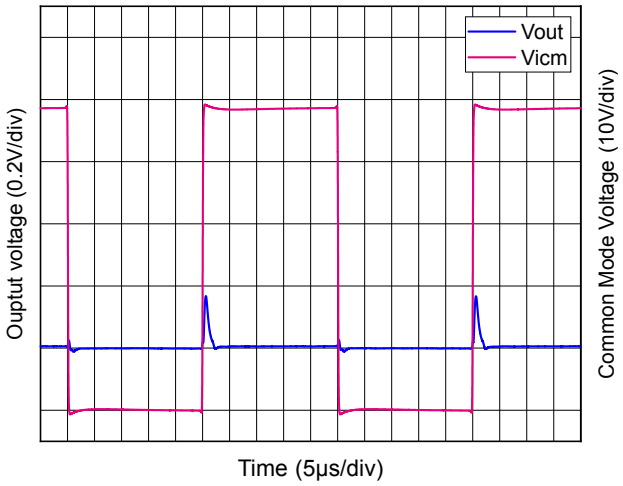
Figure 53. Functional block diagram



5.3 PWM enhancer

The TSC240 series current sensing integrates a detection of transient signal on the input common bus to reduce the impact of such an event on the output pin. Such large ΔV/Δt common-mode signals are commonly seen in applications such as motor control, where current sensing is used in inline sensing. Figure 54 shows the TSC240 output voltage response when the input pins are subjected to a 20 kHz PWM with a 0 - 48 V amplitude.

Figure 54. Output response to large ΔV/Δt input common-mode signals



The output impact to a fast input common-mode variation is typically limited to hundreds of mV for less than 2.5 µs, allowing it to work with a wide range of PWM duty cycle conditions in motor control applications.

5.4 Unidirectional / bidirectional operation

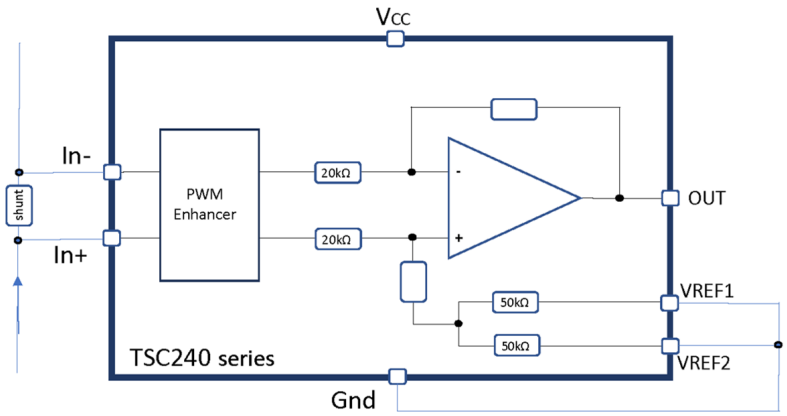
The TSC240 series output common-mode voltage level can be set using the voltages applied to the VREF1 and VREF2 pins. These two pins set the device to either bidirectional or unidirectional operation. The voltage applied to those pins must not exceed the V_{CC} range. There is no difference between the two reference pins; the voltage can be applied to either pin without distinction.

- **Unidirectional operation**

The unidirectional mode of operation allows the device to measure the current through a shunt resistor in one direction only. The output reference can be ground or V_{CC} and can be set using the VREF1 and VREF2 pins for adjustment.

- **Ground-referenced**

Figure 55. Output referenced to ground



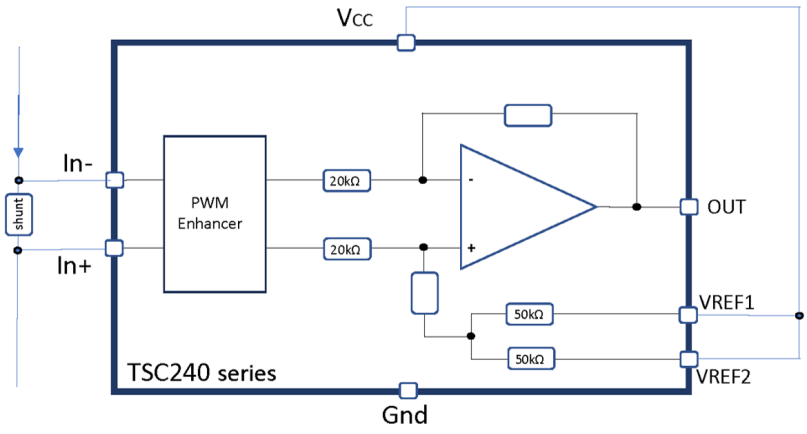
In the configuration described in Figure 55, both the VREF1 pin and VREF2 pin are connected to the ground. The output common-mode voltage is then automatically set to GND, and the output voltage can be expressed by Equation (1).

$$Vout = (IN_+ - IN_-) * Gain \quad (1)$$

This configuration allows the full-scale output in unidirectional mode to measure current flowing into the shunt from IN+ to IN-.

- **V_{CC} referenced**

Figure 56. Output referenced to V_{CC}



In the configuration described in Figure 56, the VREF1 pin and VREF2 pin are connected to the V_{CC} power supply. The output common-mode voltage is then automatically set to the V_{CC} voltage, and the output voltage can be expressed by Equation (2):

$$Vout = (IN_+ - IN_-) * Gain + Vcc \quad (2)$$

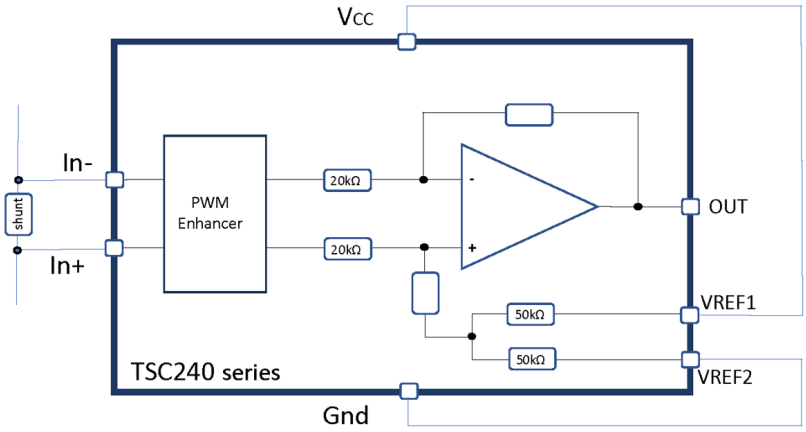
This configuration allows the full-scale output in unidirectional mode to measure current flowing into the shunt from IN- to IN+.

- **Bidirectional operation**

The bidirectional mode of operation allows the device to measure currents through a shunt resistor in two directions. The output reference can be set anywhere within the power supply range. If the output common-mode voltage is set at mid-range, the full-scale current measurement range is equal in both directions. This is achieved by connecting one VREF pin to V_{CC} and the other VREF pin to GND as described in Figure 57.

- **Split supply**

Figure 57. Split supply

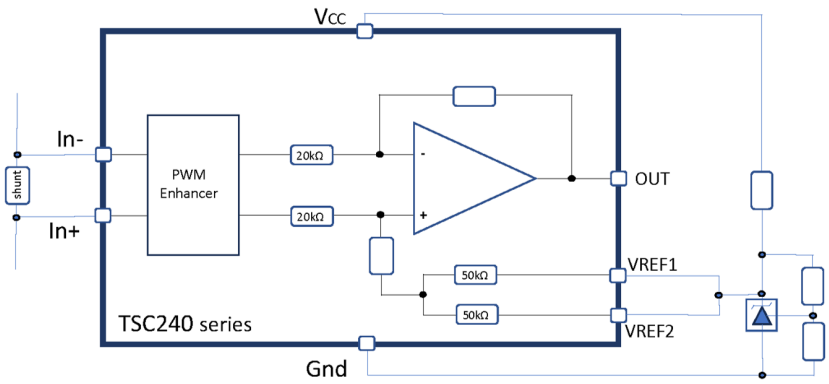


The significant advantage of this configuration is that the TSC240 series can be used in bidirectional mode with an output common-mode voltage set at mid-scale with an accuracy of 0.2%, without any added external component or power supply. This configuration creates a mid-scale offset that is ratiometric to the power supply. The output voltage can be expressed by Equation (3):

$$Vout = \left(IN_+ - IN_-\right) * Gain + \frac{Vref1 + Vref2}{2} \quad (3)$$

- **External with a reference voltage**

Figure 58. External supply



This can be done by connecting both VREF pins to a voltage reference as described in Figure 58. Users can set the output in a non-symmetrical configuration, adjusting V_{REF} according to their needs.

In this configuration, the VREF1 pin and VREF2 pin are connected to an adjustable reference voltage TS431 (Vka). The output common-mode voltage is then automatically set to the reference voltage when no current flows through the Rshunt resistance.

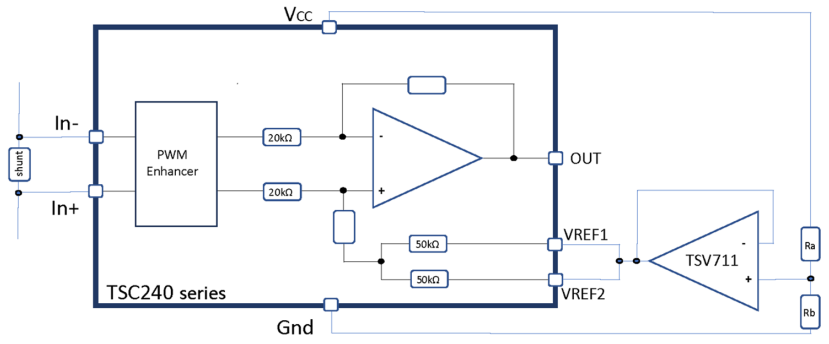
The output voltage can be expressed by Equation (4):

$$Vout = (IN_+ - IN_-) * Gain + Vka \quad (4)$$

- **External with a divider bridge**

It is recommended to buffer the resistor divider as depicted in Figure 59 using a precise op amp such as the TSV711.

Figure 59. Recommended schematic



The output voltage can be expressed by Equation (5):

$$Vout = \left(IN_+ - IN_-\right) * Gain + Vcc * \frac{Rb}{Ra + Rb} \quad (5)$$

When the output common-mode voltage is supplied by an external power supply, to improve the output voltage measurement, it is recommended to measure the V_{OUT} differentially with respect to V_{REF} voltage. It provides the best CMRR measurement, the best noise immunity, and a more accurate V_{OUT} voltage. A decoupling capacitance of 100 nF minimum can be also added to better filter the power supply.

5.5 Rsense selection

The selection of the shunt resistor is a trade-off between dynamic range and power dissipation.

Generally, in high-current sensing applications, the focus is on reducing power dissipation (RI²) as much as possible by choosing the smallest shunt resistance value as per Equation (6):

$$Rsense \leq \frac{Pmax}{Imax^2} \quad (6)$$

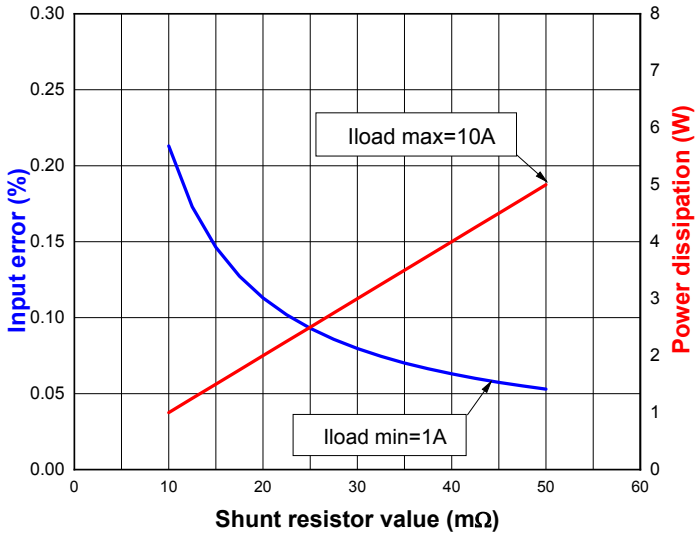
In low-current applications the Rsense value can be higher to minimize the impact of the circuit's offset voltage on the accuracy measurement.

The trade-off arises mainly when the dynamic range of current to be measured is large, meaning the ability to measure with the same shunt value low current to high current. Generally, the full-scale current (Imax-Imin) defines the shunt value based on the full output voltage range and the TSC240 series gain. The TSC240 series offers the possibility to work with full-scale ΔVout = 100 mV to Vcc - 100 mV with a maximum gain accuracy of 0.2%. At first order, the full current range to be measured through Rsense can be defined by Equation (7), just taking the gain error and input offset voltage as inaccuracy parameters:

$$Isense_{fullscale} * Rsense = \frac{V_{cc} - 200mV}{TSC_{Gain}(1 + Eg)} - 2 * \left| Vio \right| \quad (7)$$

Figure 60 shows an example of the trade-off between power dissipation and accuracy for TSC240 current sensing. A current from 1 A to 10 A is measured through different shunt values from 10 mΩ up to 50 mΩ. The maximum current (10 A) gives an idea of the worst-case power dissipation expected, whereas the lowest current (1 A) gives a first-order indication of the error that can be expected at the output.

Figure 60. Trade-off between shunt resistance, power dissipation, and accuracy



5.6 Input offset voltage drift over temperature

The maximum input voltage drift variation over temperature specified in the electrical characteristics Table 4 is defined as the offset variation from -40 °C to 125 °C. The maximum input voltage drift over temperature is computed using Equation (8);

$$\frac{\Delta Vio}{\Delta T} = \left(\frac{Vio_{-40°C} - Vio_{125°C}}{-40°C - 125°C} \right) \quad (8)$$

The datasheet maximum value is guaranteed by measurements on a representative sample size, ensuring a C_{pk} (process capability index) greater than 1.67. The value reported in the datasheet is the highest value of the |min| and |max| calculated to get this C_{pk}.

The signal chain accuracy at 25 °C can be compensated for during production at the application level. In this case, the maximum input-offset voltage drift over temperature enables the system designer to anticipate the effect of temperature variations. For this purpose, Table 5 can be used, which shows the minimum and maximum values for such drifts computed between T = (Tmin or Tmax) and T = 25 °C.

Table 5. Input offset voltage drifts relative to T = 25 °C for TSC240A1

|Δ Vio/ΔT|	T = -40°C to T =25°C min / max (nV/°C)	T = 25°C to T = 125°C min / max (nV/°C)
V_{CC} = 5 V, Vicm = 12 V	-96 / 94	-205 / 200

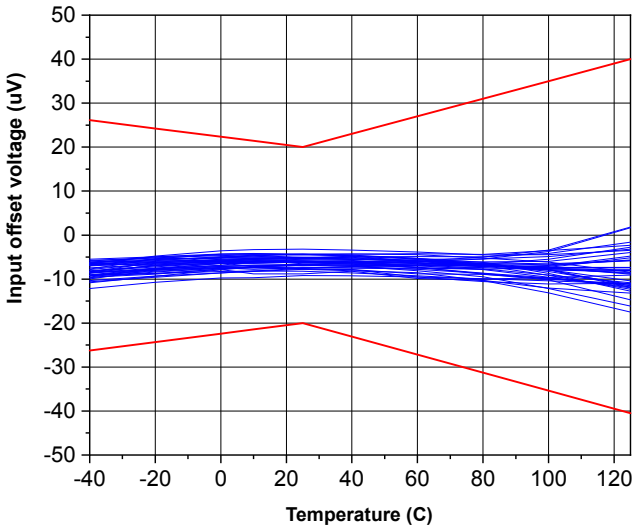
The input-offset drift values shown in Table 5 are computed from the input-offset voltage measurements at three temperatures (-40 °C, 25 °C, 125 °C) using Equation (9):

$$\frac{\Delta Vio}{\Delta T} = \left(\frac{Vio_T - Vio_{25°C}}{T - 25°C}\right) \quad (9)$$

These measurements were performed on a representative sample size, ensuring a C_{pk} (process capability index) greater than 1.67.

Figure 61 depicts the variation of the input offset voltage on 40 TSC240A1 samples for a V_{CC} = 5 V and Vicm = 12 V.

Figure 61. Input offset voltage vs. temperature



5.7 Error calculation

The principal sources of errors, such as the input-offset voltage, gain error, and common-mode rejection ratio, are described separately in the electrical characteristics. This section summarizes the most important errors to consider during the design phase.

- **Input offset voltage error**

A first-order error calculation can consider only the input-offset voltage. In a temperature environment, the deviation of the Vio is also considered, and the error linked to the input offset on the output voltage can be written as Equation (10):

$$Vio \quad Error = (\pm Vio \pm \Delta Vio/\Delta T) * Gain \tag{10}$$

- **Gain error and shunt resistance accuracy**

$$Gain \quad error = Gain(1 + \varepsilon gain) \tag{11}$$

$$Rshunt \quad error = Gain(1 + \varepsilon Rsense) \tag{12}$$

Where εgain is the gain error, 0.2% max. for the TSC240 series.

Where εRshunt is the shunt resistance error. Shunt resistors from 5 mΩ to 100 mΩ are available with 1% accuracy or better.

- **CMR error**

In the electrical characteristics, CMRR is specified at one input common-mode voltage. So, in order to consider the variation of the input voltage offset depending on the Vicm, the calculation must be performed relative to this known point. Let us take the Vicm = 12 V as a reference point.

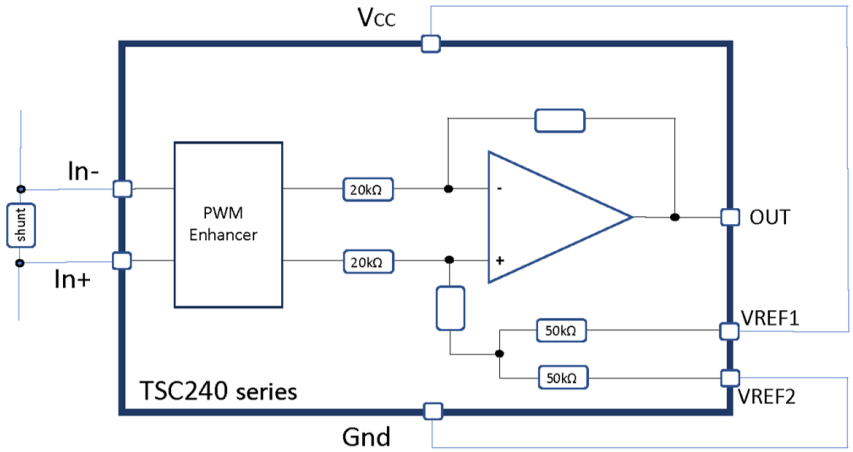
Therefore, the error on V_{out} due to a common-mode voltage variation can be written as Equation (13):

$$CMRR \quad error = \pm \frac{Vicm - 12V}{CMRR} * Gain \tag{13}$$

- **Output common-mode error**

This error can be considered when the output common-mode voltage is set as suggested in Figure 62, and thus by using the internal divider bridge. Otherwise, it is important to consider the error linked to the voltage source applied on the VREF1 pin and VREF2 pin.

Figure 62. Schematic for V_{ocm} error



The divider bridge consists of two resistances of 50 kΩ given an output common-mode voltage of $\frac{Vref1 + Vref2}{2}$.

Due to a small mismatch in internal resistance, the error on the output common-mode voltage can be described as Equation (14):

$$Vocm = \left(\frac{Vref1 + Vref2}{2}\right).\left(1 + \varepsilon Acc\right) \quad (14)$$

Where εAcc is the accuracy referred to the output with a max value of 0.1%.

- **Noise**

Figure 49 expresses the TSC240 noise referred to input. This device shows that there is only a white noise density of $\frac{50nV}{\sqrt{Hz}}$ over the TSC240 bandwidth.

Considering that there is no additional filter on the TSC240 and it is only bandwidth limited, it can be considered that at over 560 kHz, there is an attenuation of the noise with a first-order filtering. So, the equivalent noise bandwidth is $560 \quad kHz \cdot \frac{\pi}{2}$.

The RMS value of the output noise is the integration of the spectral noise over the bandwidth of interest and can be expressed as Equation (15):

$$enRMS = \left(\sqrt{\int_{0.1}^{560000 \cdot \frac{\pi}{2}} \left(50 \cdot 10^{-9}\right)^2 df}\right) * Gain \quad (15)$$

- **Total error**

The maximum total error expected on the output of the device can be considered as the sum of the different sources described above, considering all the maximum parameters of the datasheet. This approach is very pessimistic, and the probability of obtaining all the maximum parameter values on the same die is extremely low, if not null. To get a more realistic picture of the maximum possible error on the output, the total error can be determined by using a simplified statistical approach such as the root sum of squares (RSS), a method for combining the error terms.

So, the error can be written as Equation (16):

$$Error_{Rss} = \sqrt{(\varepsilon G)^2 + (\varepsilon shunt)^2 + \left(\frac{Vio}{Rshunt \cdot I}\right)^2 + \left(\frac{\frac{Vicm - 12V}{CMRR}}{Rshunt \cdot I}\right)^2 + \left(\frac{Vref \cdot (\varepsilon ref)}{G \cdot Rshunt \cdot I}\right)^2} \quad (16)$$

Note that the input bias currents are not considered in this section, as this current is already considered as integrated in the Vsense. The TSC240 cannot measure currents of the same order as the input bias current (several hundreds of µA).

Linearity is not considered in the error calculation, as it represents only 0.001% error and is negligible. Nevertheless, as the gain error has been calculated using the best-fit line approach, it indicates that the gain error can be relatively constant throughout the linear input range of the TSC240.

Equation 16 has been defined for a temperature of 25 °C. With temperature variation, the $\Delta V_{IO}/\Delta T$ error term must certainly be added. And if the power supply is susceptible to change, the SVR parameter must also be considered. For more information about the expected error at the current sensing output, please refer to the application note AN5849. The shunt accuracy must also be considered.

- **Example**

Let us consider an example to obtain a better understanding of the maximum total error that can happen on the output of the TSC240 (x20).

- **Use case**:
  - V_{CC} = 5 V
  - V_{icm} = 24 V
  - V_{ocm} = 2.5 V
  - Temperature = 25 °C
  - I_{load} = 10 A
  - Shunt 5 mΩ

Theoretically, the expected output voltage should be $V_{out} = R_{shunt} * I_{load} * 20 + V_{ocm}$ = 3.5 V.

From the above equations, let us detail all the error terms by using the maximum value of the electrical characteristics (when available). The error % at output in the following table is expressed in reference to $V_{out} – V_{ref}$, so in this typical example: 1 V.

Table 6. Error

Error source	Calculus	Output voltage error	% error on output
Gain error	$20*5 . 10^{-3}*10*0.2\%$	2 mV	0.2%
Vio error	20*25 µV	0.5 mV	0.05%
CMRR error	$20 * \frac{24V - 12V}{\frac{120}{10\ 20}}$	0.24 mV	0.02%
Vocm error	2.5*0.1%	2.5 mV	0.25%
Noise	$20 * \frac{50nV}{\sqrt{Hz}}\sqrt{560kHz * \frac{\pi}{2} - 0.1Hz}$	0.9 mVrms	0.3% (1)

1. *The percentage is based on the voltage peak value and is 3 times the RMS value.*

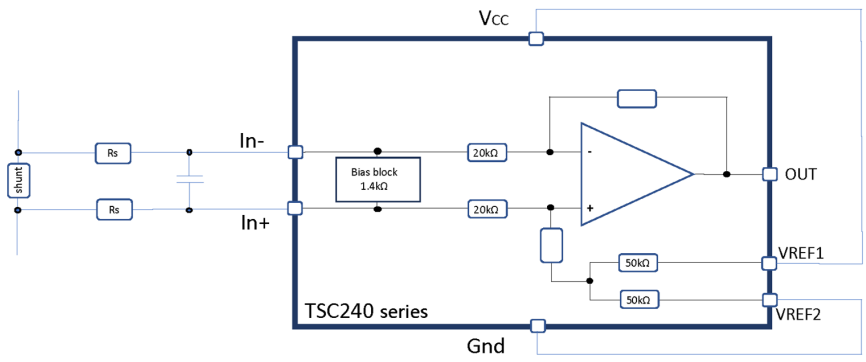
An error of 0.44% can be expected on the output of the TSC240 @ 25 °C for a current of 10 A.

5.8 Input filtering

Although the TSC240 does not require input filtering to achieve good measurement accuracy, depending on the application requirements, a low-pass filter may be needed. In this case, it is always better to filter the TSC240 output rather than the input pins. Anyway, the TSC240 output shows a low impedance even at high frequencies shown in Figure 52, and adding an output filter certainly increases the output impedance.

Adding resistances on the input pins creates an impedance mismatch with the internal bias block, which allows the input stage to be correctly polarized when the common-mode voltage is higher than the power supply voltage. The block diagram is described in Figure 63.

Figure 63. Input filter



When an input differential voltage is applied, the bias block has a differential impedance of 1.4 kΩ as shown in Figure 63. This mismatch has a direct impact on gain accuracy, as described by Equation (17):

$$Gain \quad error = 1 - \frac{700}{Rs + 700} \tag{17}$$

In a second-order due to a mismatch in the external series resistances, an input-offset voltage may also be added as depicted by Equation (18):

$$Input \quad Offset \quad voltage = Rs.\varepsilon\alpha.(Iibp + Iibm) \tag{18}$$

Where εα is the resistance precision.

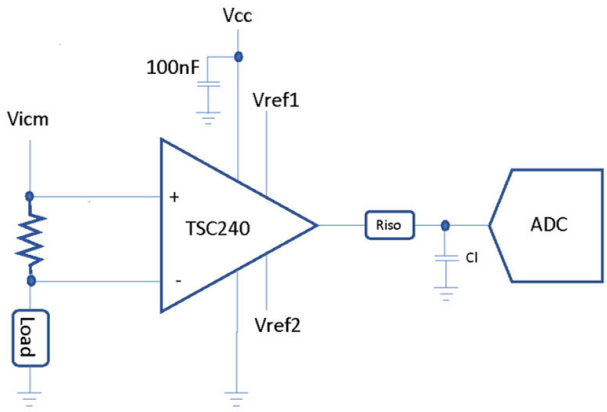
To limit the error, it is recommended to keep series resistances at the input as low as possible. 10 Ω or lower is recommended.

By using a series resistance of 10 Ω (±1%) at the input pins of the TSC240 in a 48 V application (corresponding to an Iib = 200 µA), a gain error of 1.4% can appear and an added input offset of 40 µV.

5.9 Stability

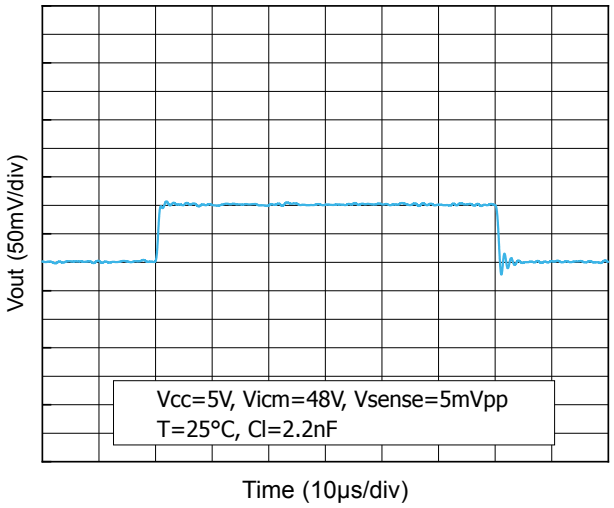
Driving a large capacitive Cload can produce gain peaking in the frequency response, with overshoot and ringing in the step response. In order to smooth the output, a series resistor (Riso) can be inserted between the TSC240 output and the capacitive load as depicted by Figure 64.

Figure 64. Series resistor Riso



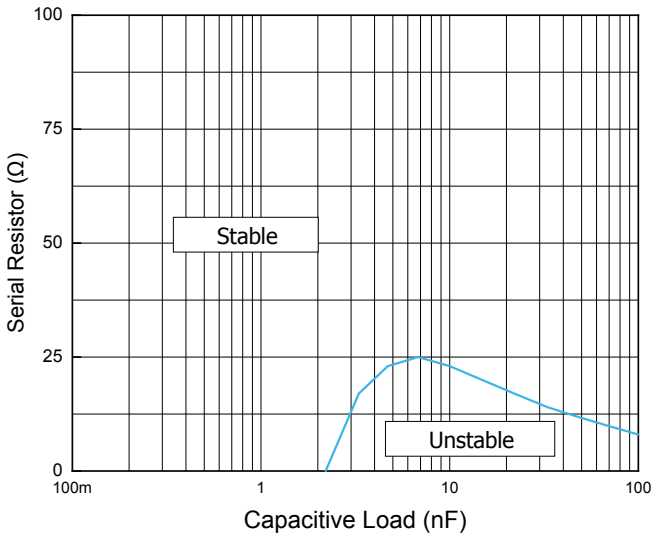
The criteria applied to ensure the stability of the system is an overshoot of less than 24% to a small input step voltage. Figure 65 shows the TSC240 output response, loaded with a 2.2 nF capacitor, to a 5 mV input step. It illustrates the stability criteria acceptance with an overshoot of less than 24%.

Figure 65. **Stability criteria overshoot 24%**



For load capacitances higher than 2.2 nF, to respect an overshoot of less than 24%, and expecting an output signal like the one in Figure 65, a series resistor must be added at the output, as shown in Figure 66.

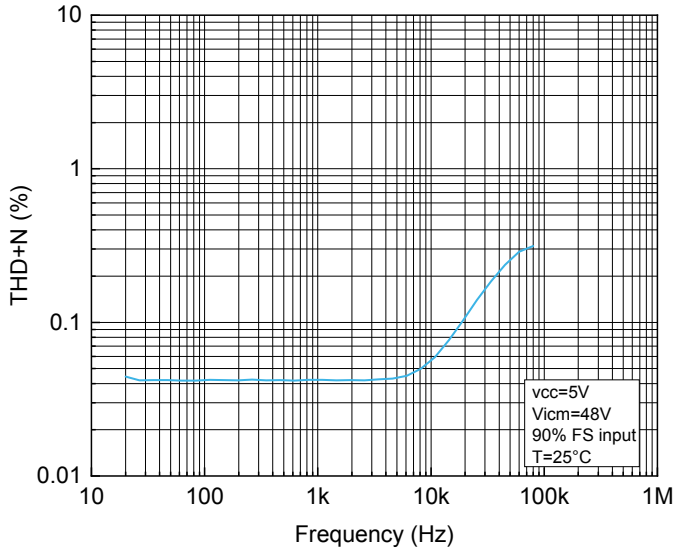
Figure 66. **Stability criteria with a series resistor at V_{CC} = 5 V**



5.10 Low distortion

The TSC240 demonstrates a low level of distortion, especially at low frequencies. Figure 67 shows an optimum accuracy in the 10 kHz bandwidth. It remains well below 1% in the bandwidth range of the TSC240.

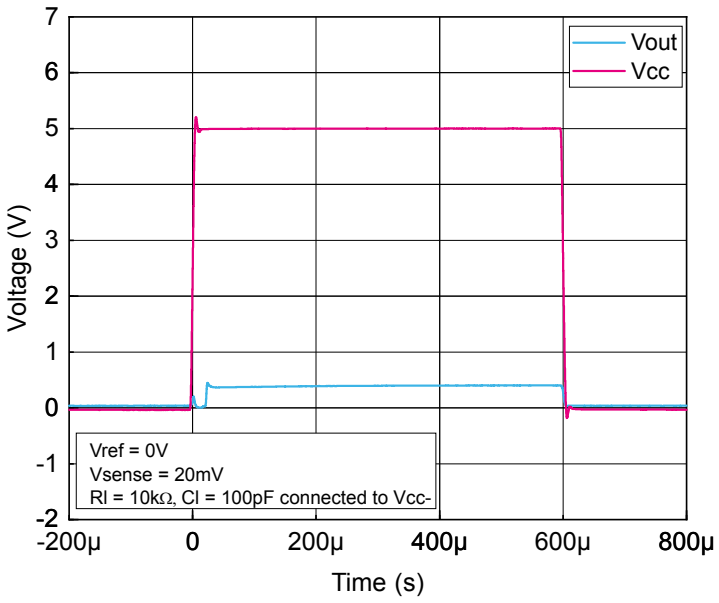
Figure 67. **THD+N**



5.11 Power supply recommendation

To correctly decouple the TSC240 series, it is recommended to place a 100 nF bypass capacitor between VCC and GND. This capacitor must be placed as close as possible to the supply pins. Figure 68 shows a startup time with a decoupling capacitance of 100 nF.

Figure 68. **Startup time with a decoupling capacitance of 100 nF**



It is also important to consider the VREF pins, which is used to fix the output common-mode voltage. Effectively, these pins must be driven by a low impedance voltage source and can be decoupled using a 10 nF bypass capacitor.

A larger bypass capacitor added at the VCC pin and VREF pins should help enhance CMRR and PSRR performance.

5.12 PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the current sensing, load, and power supply. It is good practice to use short and wide PCB traces to minimize voltage drops and parasitic inductance.

When using shunt resistances of less than 1 Ω, it is important to use a 4-wire connection technique to sense the current, as described in the schematic below. Effectively, this technique allows pairs of current-carrying and voltage-sensing electrodes to be separated to make more accurate measurements by eliminating the lead and contact resistance from the measurement.

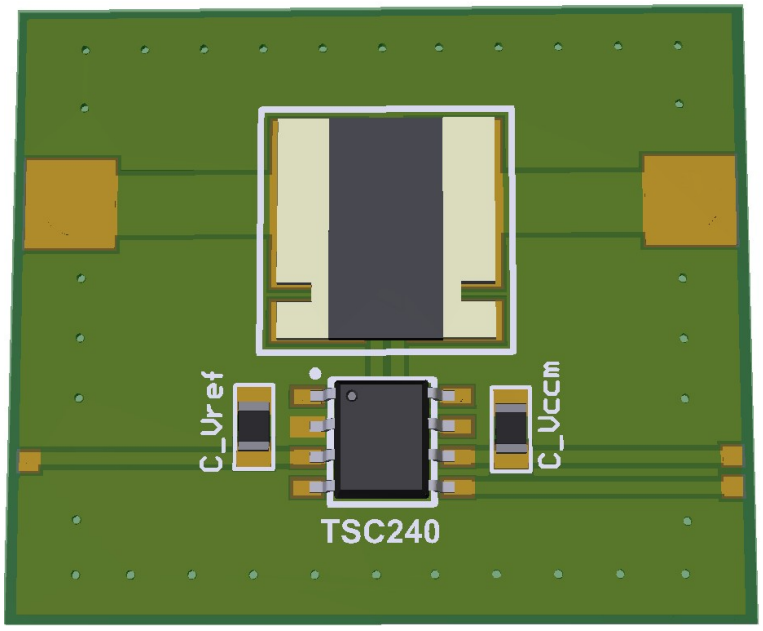
It is also important to treat the track connected to the input pin of the TSC240 series as a differential pair; it must have the same length and width, ideally placed on the same PCB plane, and above all must be routed as far as possible from noisy sources. As this track carries the input bias current, which is in a range of hundreds of µA, it can be designed small, but its resistivity must always be taken into account. Vias are not recommended in these input tracks to avoid any parasitic resistance in this path.

To minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes in many locations is often used.

A ground plane generally helps to reduce EMI, which is why it is generally recommended to use a multilayer PCB and use the ground planes as a shield to protect the internal track. In this case, ensure the digital and analog grounds are separated, and avoid ground loops. To minimize EMI impact, it is important to reduce the loop area or antenna.

Figure 69 suggests a possible routing for the TSC240 series in order to minimize parasitic effect as much as possible.

Figure 69. Recommended layout

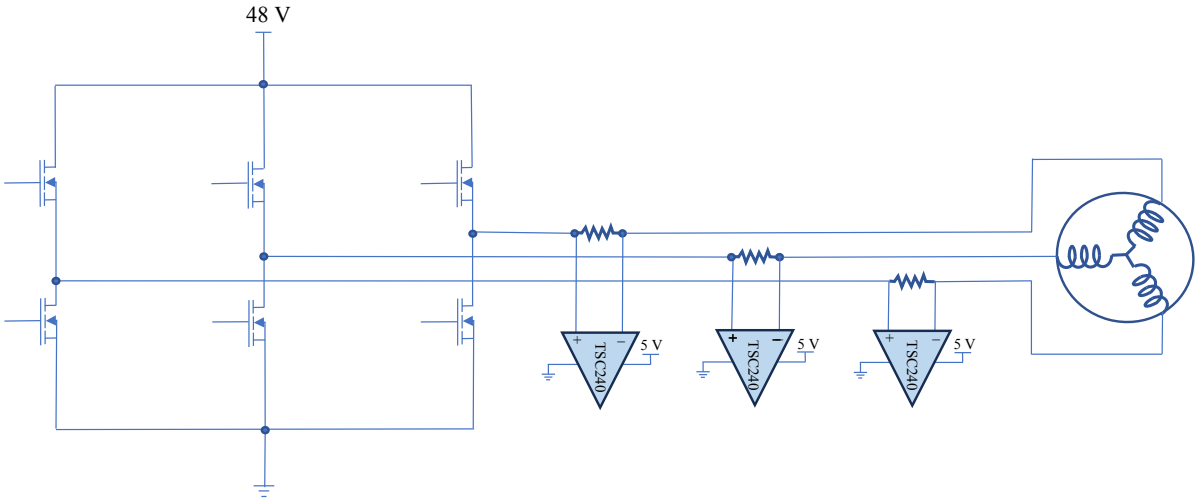


5.13 Application examples

Inline motor control application

The configuration described in Figure 70, inline phase current sensing is the best method for precisely determining the phase current flowing into the motor. This current measurement offers the best information that can be used in feedback motor control, to optimize the motor performance. The main advantage of this topology is that the current can be read without a strong linkage to the PWM status and without timing limitations when a very small PWM is applied to the phase (low-side current sensing can only be executed while the low-side transistor of that leg is on). It also allows the detection of phase short-circuits.

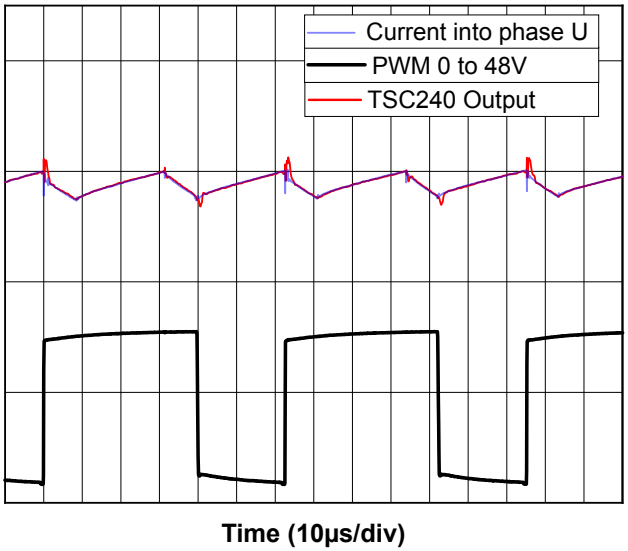
Figure 70. **Inline motor control application schematic**



As the shunt resistance is placed directly in line with the PWM driver, the input pins of the TSC240 series can see several tens of volts in few nanoseconds, depending on the motor to drive. As demonstrated in Figure 71, the TSC240 can limit unwanted disturbance at the output and offer a stable output in few µs after a common-mode transient.

The TSC240 is a bidirectional high-side current sensing especially designed for this kind of application and offers optimized performance.

Figure 71. **TSC240 used in inline topology**



6 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SO8 package information

Figure 72. SO8 package outline

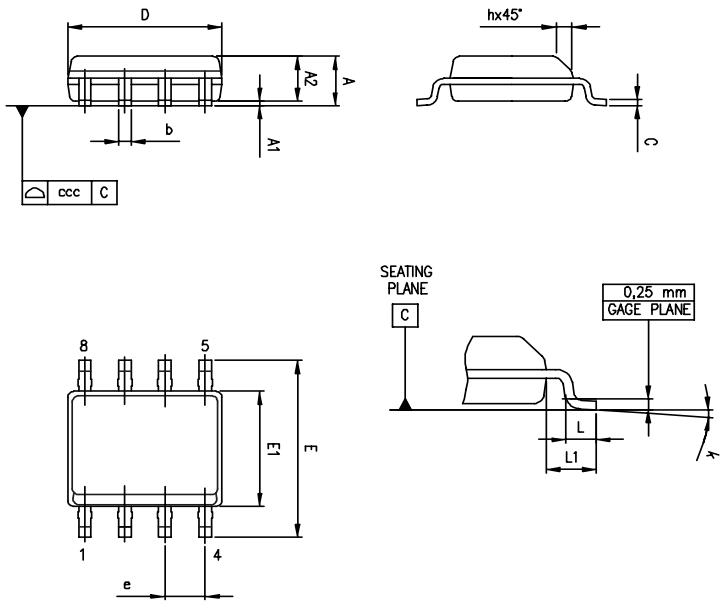


Table 7. SO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0°		8°	0°		8°
ccc			0.10			0.004

6.2 TSSOP8 package information

Figure 73. **TSSOP8 package outline**

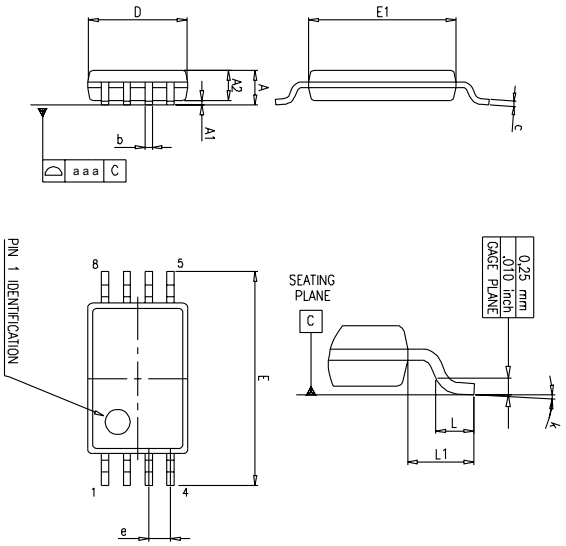


Table 8. **TSSOP8 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa		0.10			0.004	

7 Ordering information

Table 9. Order codes

Order code	Gain (V/V)	Temp. range	Package	Packaging	Marking
TSC240A1IDT	20	-40 to 125 °C	SO8	Tape & Reel	240A1I
TSC240A1IPT			TSSOP8		240A1
TSC240A1IYDT (1)			SO8		240A1IY
TSC240A1IYPT (1)			TSSOP8		40A1Y
TSC240A4IDT	200		SO8		240A4I
TSC240A4IPT			TSSOP8		240A4
TSC240A4IYDT (1)			SO8		240A4IY
TSC240A4IYPT (1)			TSSOP8		40A4Y

1. *Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.*

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
23-Sep-2025	1	Initial release.
14-Oct-2025	2	Updated features and applications on the cover page.
09-Oct-2026	3	Added new Section 5: Application information and new TSC240A4 order code in Table 9.

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