

GANC050-650TBH

650 V, 50 mOhm Gallium Nitride (GaN) FET in a TOLL package

1 September 2026 **Product data sheet**

1. General description

The GANC050-650TBH is a 650 V, 50 mΩ gallium nitride (GaN) FET in a TOLL package. This normally-off device combines high-voltage GaN HEMT and low-voltage silicon MOSFET technologies to deliver robust, high-efficiency switching performance.

2. Features and benefits

- Simplified driver design as standard MOSFET gate drivers can be used:
  - 0 V to 10 or 12 V drive voltage
- Robust gate oxide with -20 V to 20 V V_{GS} rating
- High gate threshold voltage for gate bounce immunity
- Low body diode V_F for reduced losses and simplified dead-time adjustments
- Transient over-voltage capability for increased robustness

3. Applications

- Data center and telecom power supplies (AC-DC and DC-DC)
- Photovoltaics (PV) inverters
- Battery Energy Storage Systems (BESS)
- Industrial motor drives and automation power

4. Quick reference data

Table 1. Quick reference data

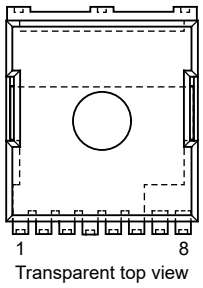
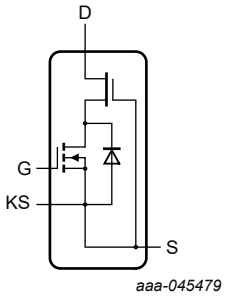
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 150 °C		-	-	650	V
I_D	drain current	T_{mb} = 25 °C		-	-	32	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	104	W
T_j	junction temperature			-55	-	150	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 22 A; T_j = 25 °C	[1]	-	50	60	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 22 A; V_{DS} = 400 V; 0 V ≤ V_{GS} ≤ 10 V; T_j = 25 °C		-	13	-	nC
$Q_{G(tot)}$	total gate charge	I_D = 22 A; V_{DS} = 400 V; 0 V ≤ V_{GS} ≤ 10 V; T_j = 25 °C; Fig. 11		-	31	-	nC

[1] Dynamic on-resistance

nexperia

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	Source	 Transparent top view **TOLL (SOT8136-1)**	
2	S	Source		
3	S	Source		
4	S	Source		
5	S	Source		
6	S	Source		
7	KS	Kelvin Source		
8	G	Gate		
Drain	D	Drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
GANC050-650TBH	TOLL	TOLL: Plastic, thermal enhanced surface mounted package; 9 terminals; 1.2 mm pitch; 10.43 mm × 9.9 mm × 2.3 mm body	SOT8136-1

7. Marking

Table 4. Marking codes

Type number	Marking code
GANC050-650TBH	`050ITBH`

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

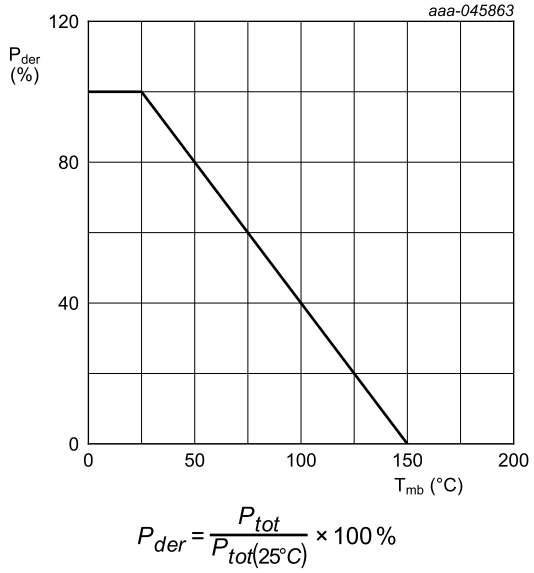
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 150 °C		-	650	V
V_{DSM}	peak drain-source voltage	non-repetitive	[1]	-	800	V
		repetitive	[2]	-	750	V
V_{GS}	gate-source voltage	DC		-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	104	W
I_D	drain current	T_{mb} = 25 °C		-	32	A
		T_{mb} = 100 °C		-	20	A
I_{DM}	peak drain current	pulsed; t_p = 10 µs; T_{mb} = 25 °C		-	150	A
T_{stg}	storage temperature			-55	150	°C
T_j	junction temperature			-55	150	°C

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Symbol	Parameter	Conditions		Min	Max	Unit
$T_{sld(M)}$	peak soldering temperature		[3]	-	260	°C

[1] duty cycle < 1% , spike duration < 30µs, non-repetitive
[2] duty cycle < 1% , spike duration < 30µs, repetitive for ≤ 85 °C , non-repetitive up to 150 °C
[3] Reflow MSL3



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base			-	1.2	-	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	45	-	K/W

[1] Soldered on a PCB of 6cm^2 metal area

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{S\ (pulsed)}$	Pulsed reversed current	V_{SD} = 6 V; T_j = 150 °C; $t_p \leq$ 10 µs; V_{GS} = 0 V		-	-	69	A
Static characteristics							
$V_{GS(th)}$	gate-source threshold voltage	I_D = 3 mA; $V_{DS} = V_{GS}$		3	3.5	4	V
I_{DSS}	drain leakage current	V_{DS} = 650 V; V_{GS} = 0 V; T_j = 25 °C		-	2	40	µA
		V_{DS} = 650 V; V_{GS} = 0 V; T_j = 150 °C		-	15	-	µA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 22 A; T_j = 25 °C	[1]	-	50	60	mΩ
		V_{GS} = 10 V; I_D = 22 A; T_j = 150 °C	[1]	-	105	-	mΩ

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{GSS}	gate leakage current (drain shorted)	-20 V ≤ V_{GS} ≤ 20 V		-20	-	20	µA
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 22 A; V_{DS} = 400 V; 0 V ≤ V_{GS} ≤ 10 V; T_j = 25 °C; Fig. 11		-	31	-	nC
Q_{GS}	gate-source charge	I_D = 22 A; V_{DS} = 400 V; 0 V ≤ V_{GS} ≤ 10 V; T_j = 25 °C		-	8	-	nC
Q_{GD}	gate-drain charge			-	13	-	nC
C_{iss}	input capacitance	V_{DS} = 400 V; V_{GS} = 0 V; f = 500 kHz; T_j = 25 °C; Fig. 12		-	1560	-	pF
C_{oss}	output capacitance			-	80	-	pF
C_{rss}	reverse transfer capacitance			-	10	-	pF
$C_{o(er)}$	effective output capacitance, energy related	0 V ≤ V_{DS} ≤ 400 V; V_{GS} = 0 V; T_j = 25 °C		-	124	-	pF
$C_{o(tr)}$	effective output capacitance, time related			-	224	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 400 V; 0 V ≤ V_{GS} ≤ 12 V; R_{ON} = 47 Ω , R_{OFF} = 22 Ω, I_D = 22 A, Z_{FB} = 120 Ω at 100 MHz		-	66	-	ns
t_r	rise time			-	8	-	ns
$t_{d(off)}$	turn-off delay time			-	84	-	ns
t_f	fall time			-	9	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; 0 V ≤ V_{DS} ≤ 400 V		-	90	-	nC
Source-drain characteristics							
V_{SD}	source-drain voltage	I_S = 22 A; V_{GS} = 0 V; T_j = 25 °C	[2]	-	1.6	1.9	V
t_{rr}	reverse recovery time	I_S = 22 A; dI_S/dt = 1000 A/µs; V_{GS} = 0 V; V_{DS} = 400 V		-	30	-	ns
I_S	reverse current	V_{GS} = 0 V; δ ≤ 25 %; T_{mb} = 100 °C		-	-	20	A

[1] Dynamic on-resistance
[2] Including the effect of dynamic on-resistance

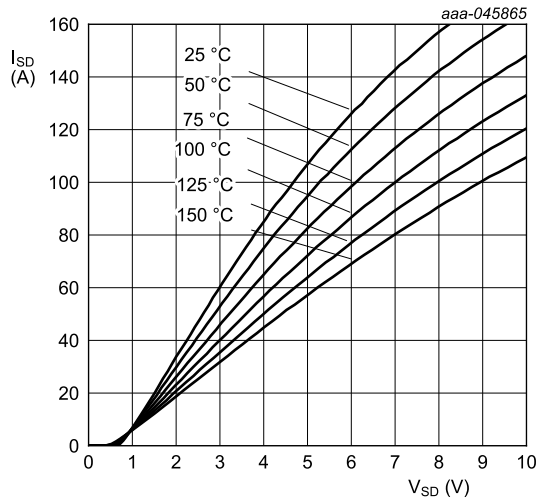
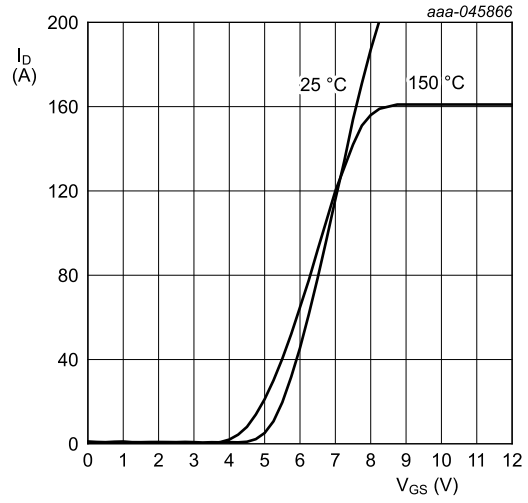


Fig. 2. Reverse conduction characteristics



V_{DS} = 20 V

Fig. 3. Transfer characteristics

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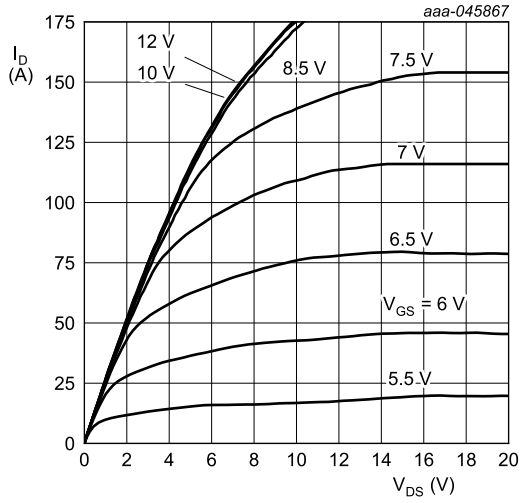


Fig. 4. Output characteristics: drain current as a function of drain-source voltage

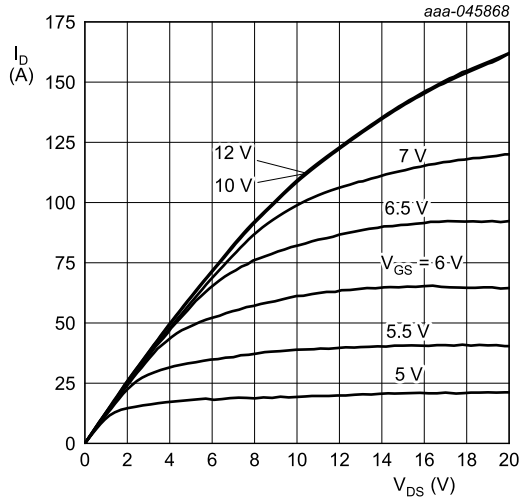


Fig. 5. Output characteristics: drain current as a function of drain-source voltage

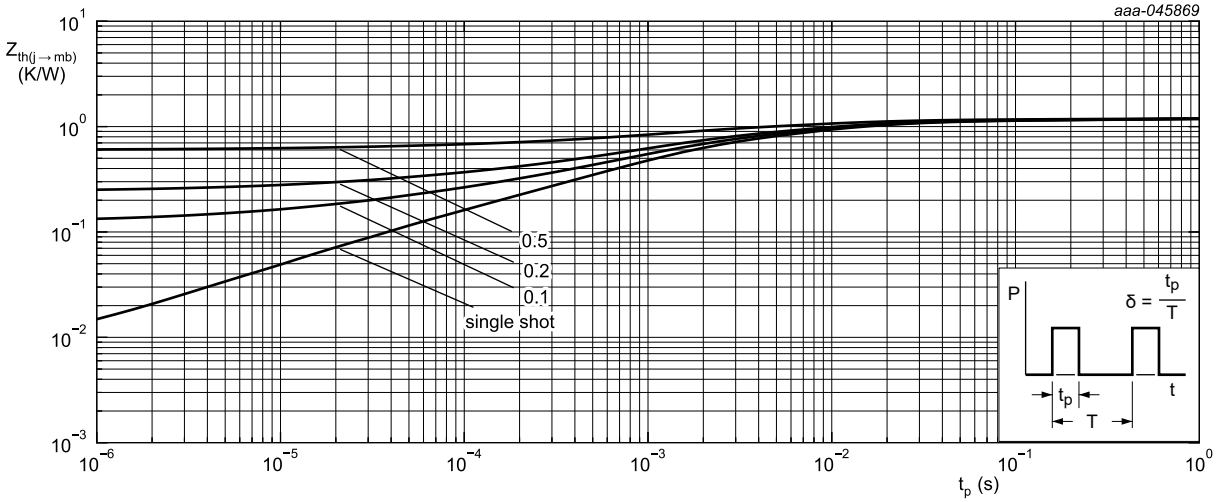


Fig. 6. Transient thermal resistance from junction to mounting base as a function of pulse duration

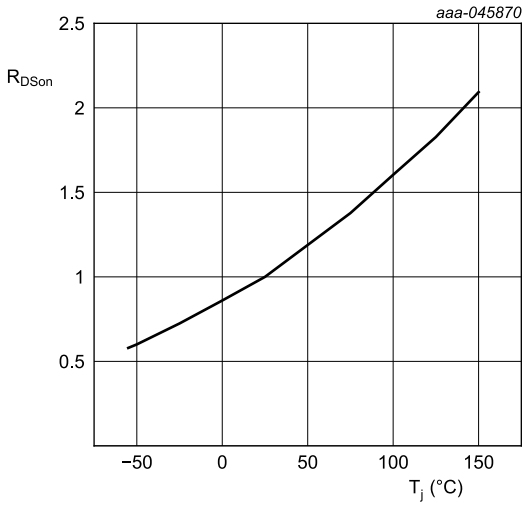


Fig. 7. Normalized on-resistance as a function of junction temperature

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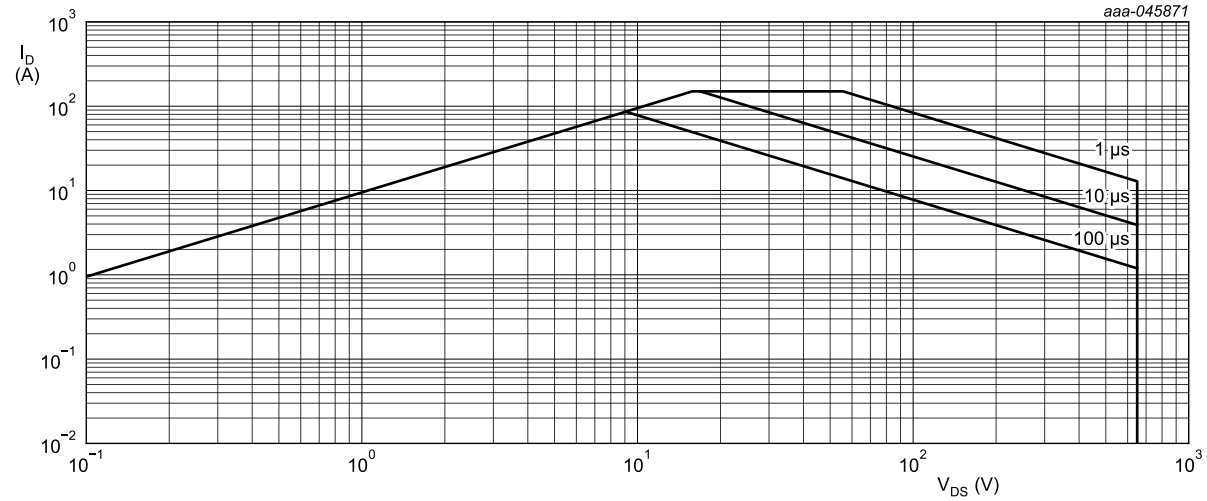


Fig. 8. Safe operating area T_{mb} = 25 °C

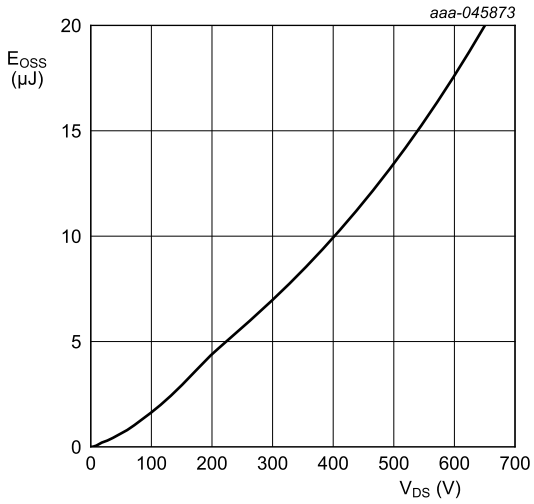
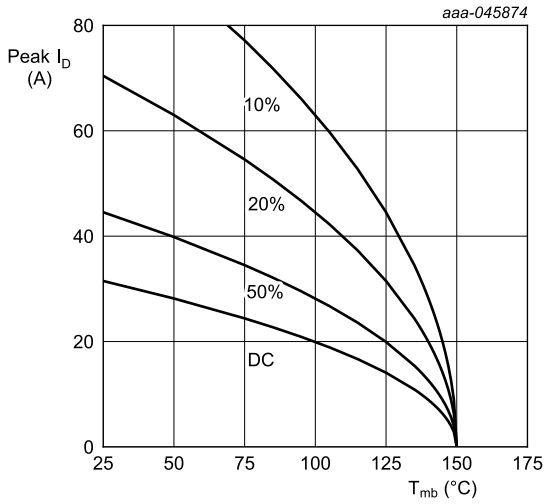


Fig. 9. Typical C_{oss} stored energy



Pulse Width ≤ 10 µs, V_{GS} ≥ 10 V

Fig. 10. Current derating

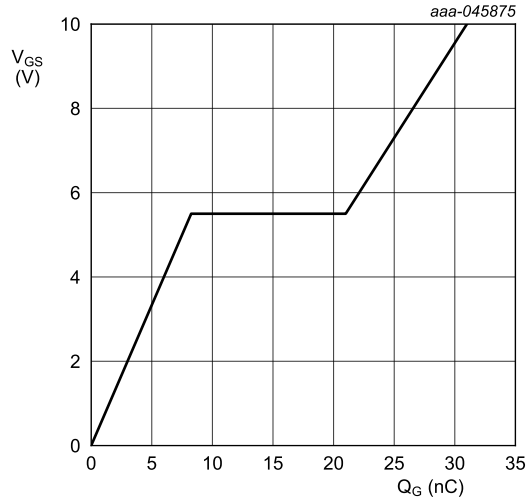


Fig. 11. Gate-source voltage as a function of gate charge

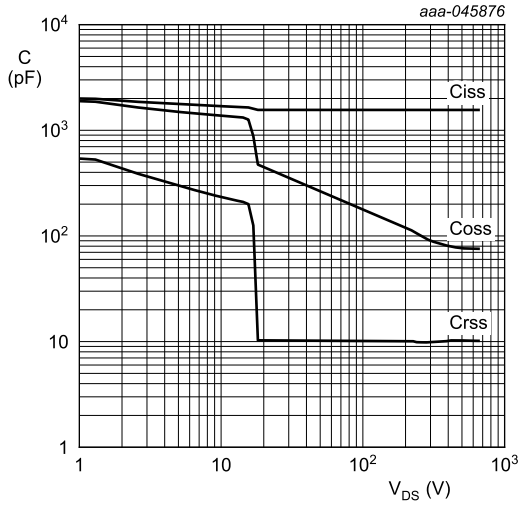


Fig. 12. Typical capacitance

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11. Application information

A ferrite bead must be fitted in series with the gate of the GaN FET and should be located as close as possible to the gate pin (see Fig. 13).

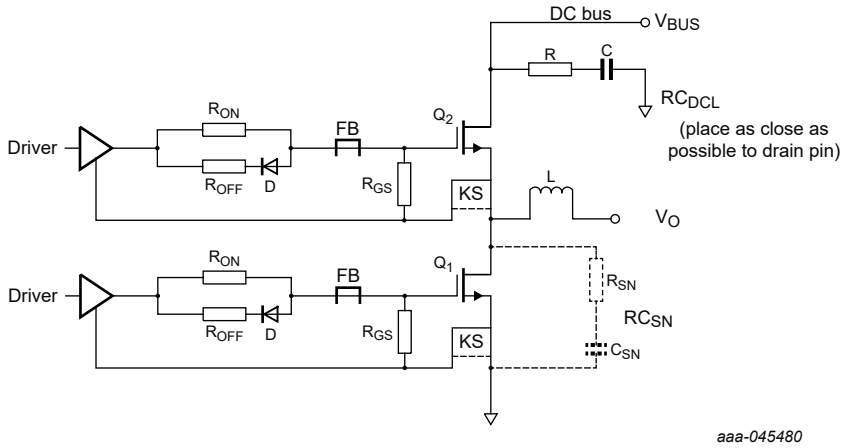


Fig. 13. Application diagram

Keeping the gate-source loop as compact as possible minimizes the gate-loop inductance. The ferrite bead damps the resonant circuit made up of the gate-source loop inductance and the GaN FET input capacitance, thus providing fast switching stability. It is recommended that the impedance of the ferrite bead should be between 80 to 120 Ω at 100 MHz (recommended part numbers: MH1608-800Y or BLM18PG121SN1D). Series resistance R_{ON} between 33 to 150 Ω and R_{OFF} between 20 to 47 Ω is also recommended.

A DC-link resonance damper is strongly recommended in all cases. An optimal value is 10 nF in series with 5.1 Ω, most easily achieved with a parallel combination of 4.7 nF and 10 Ω (see Fig. 14).

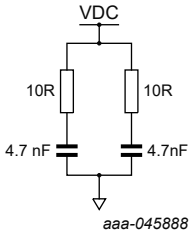


Fig. 14. DC-link resonance damper circuit

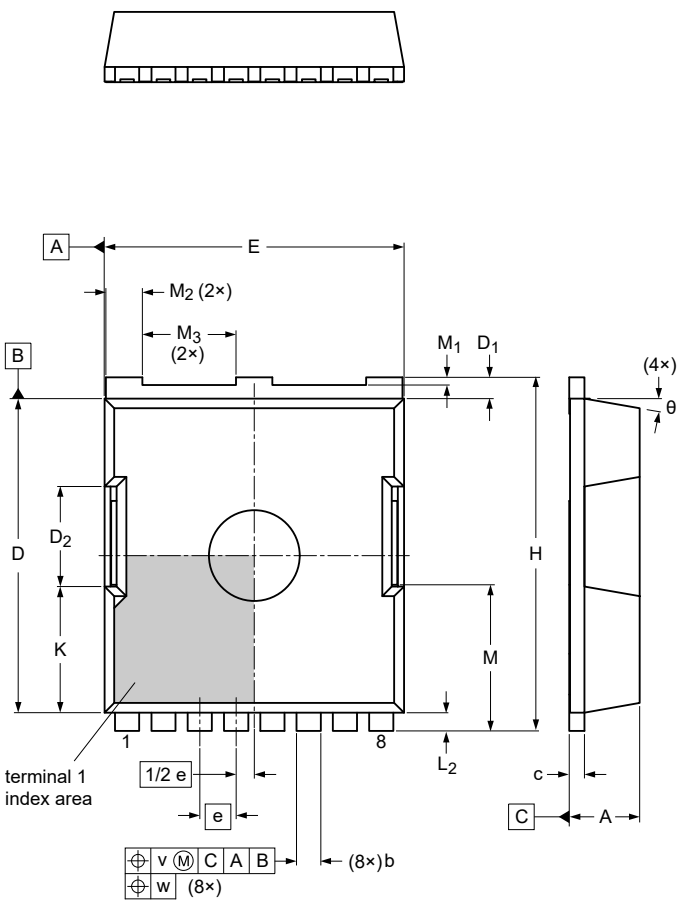
This resonance damper lowers the Q-factor of any resonance in the bus. That resonance will act as a load on the high-gain amplifier that is the GaN FET and can lead to instability. For very high current, or if R_{ON}/R_{OFF} are lower than suggested, an RC snubber is recommended for the switching node. This will increase switching loss, so this is only recommended at high power levels where the switching losses are a very small percentage of the total power.

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12. Package outline

TOLL: Plastic, thermal enhanced surface mounted package; 9 terminals; 1.2 mm pitch; 10.43 mm × 9.9 mm × 2.3 mm body **SOT8136-1**



Dimensions (mm are the original dimensions)

Unit[1]		A	b	b_1	c	D	D_1	D_2	D_3	D_4	D_5	D_6	E	E_1	E_2	E_3	e	e_1	H	K	L	L_1
mm	max	2.40	0.90	0.55	0.60	10.58	0.80	3.30 REF	2.77 REF	2.28 REF	2.55 REF	2.05 REF	10.10	8.50 REF	8.50 REF	9.46 REF	1.20 BSC	4.30 BSC	11.88	4.17 REF	1.30	0.33
	nom																					
	min	2.20	0.70	0.35	0.40	10.28	0.60						9.70						11.48		1.10	0.13

Unit[1]	L_2	L_3	L_4	L_5	L_6	M	M_1	M_2	M_3	v	w	θ
mm	0.70	1.30	0.65 REF	0.50 REF	2.88 REF	4.23 REF	0.36	1.30	3.20	0.25	0.20	10°
	0.50	1.10					0.16	1.10	3.00			4°

Note
1. Lead length L and L_3 up to anti flash profile, mold flashed excluded.
2. Plastic protrusion of 0.3 mm maximum is not included for dimension E.
3. Mold flash of 0.15 mm maximum per side is not included for dimensions D and E.

sot8136-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8136-1						26-02-03

Fig. 15. Package outline TOLL (SOT8136-1)

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13. Soldering

Footprint information for reflow soldering of TOLL package **SOT8136-1**

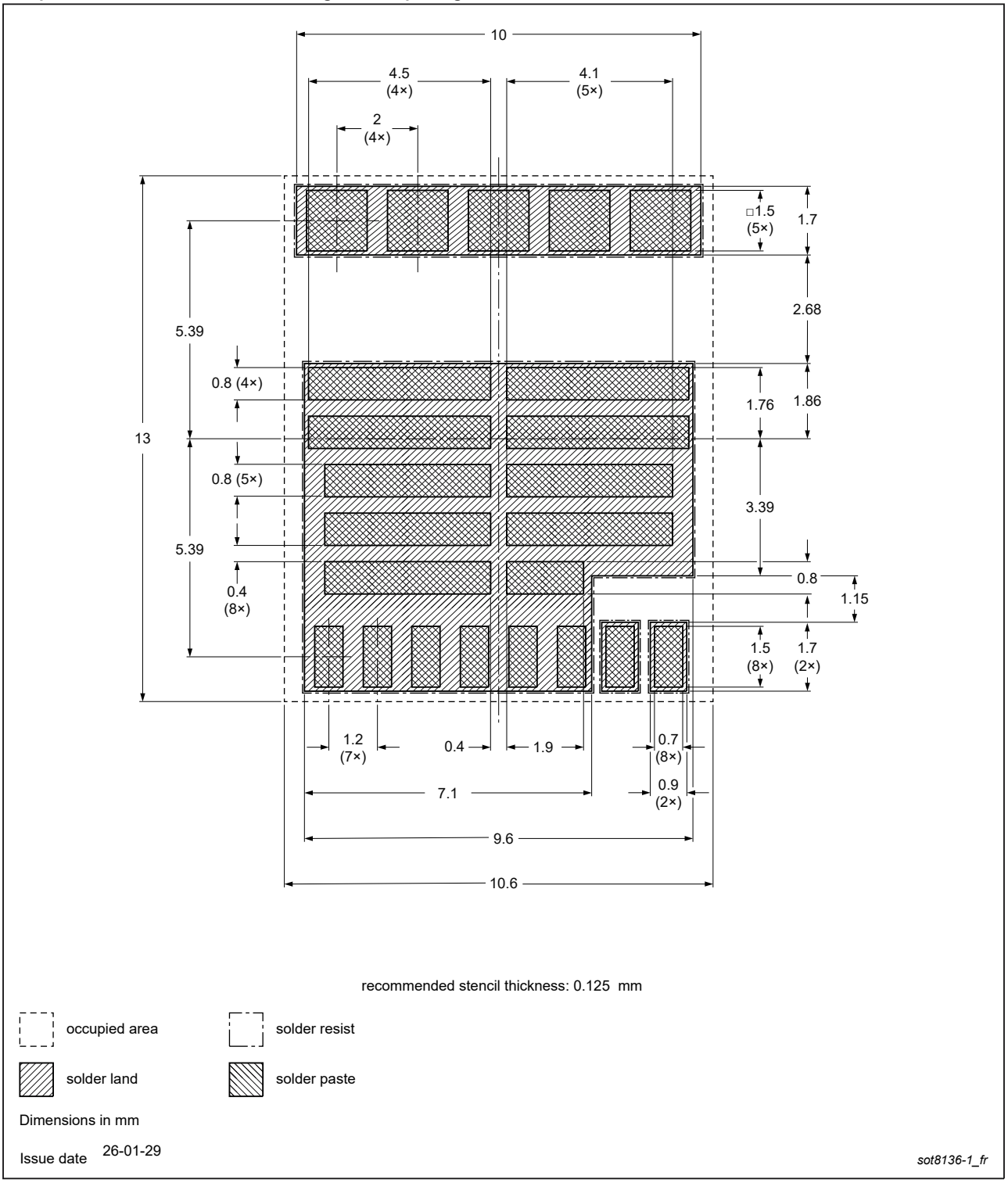


Fig. 16. Reflow soldering footprint for TOLL (SOT8136-1)

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14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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