

GANC050-650VSH

650 V, 50 mOhm Gallium Nitride (GaN) FET in a TO-247-4 package

1 September 2026 **Product data sheet**

1. General description

The GANC050-650VSH is a 650 V, 50 mΩ gallium nitride (GaN) FET in a TO-247-4 package. This normally-off device combines high-voltage GaN HEMT and low-voltage silicon MOSFET technologies to deliver robust, high-efficiency switching performance.

2. Features and benefits

- Simplified driver design as standard MOSFET gate drivers can be used:
  - 0 V to 10 or 12 V drive voltage
- Robust gate oxide with -20 V to 20 V V_{GS} rating
- High gate threshold voltage for gate bounce immunity
- Low body diode V_F for reduced losses and simplified dead-time adjustments
- Transient over-voltage capability for increased robustness

3. Applications

- Data center and telecom power supplies (AC-DC and DC-DC)
- Photovoltaics (PV) inverters
- Battery Energy Storage Systems (BESS)
- Industrial motor drives and automation power

4. Quick reference data

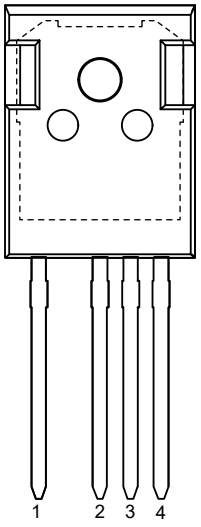
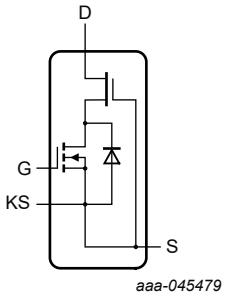
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 150 °C		-	-	650	V
I_D	drain current	T_{mb} = 25 °C		-	-	32	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	104	W
T_j	junction temperature			-55	-	150	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 22 A; T_j = 25 °C	[1]	-	50	60	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 22 A; V_{DS} = 400 V; 0 V ≤ V_{GS} ≤ 10 V; T_j = 25 °C		-	13	-	nC
$Q_{G(tot)}$	total gate charge	I_D = 22 A; V_{DS} = 400 V; 0 V ≤ V_{GS} ≤ 10 V; T_j = 25 °C; Fig. 11		-	31	-	nC

[1] Dynamic on-resistance

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	Drain	 Transparent top view **TO-247-4L (SOT8071-2)**	
2	S	Source		
3	KS	Kelvin Source		
4	G	Gate		
Tab	S	Source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
GANC050-650VSH	TO-247-4L	Plastic, single-ended package (heatsink mounted, 1 mounting hole); 4 leads; 2.54 mm pitch; 20.95 mm × 15.94 mm × 5.02 mm body	SOT8071-2

7. Marking

Table 4. Marking codes

Type number	Marking code
GANC050-650VSH	`050IVSH`

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

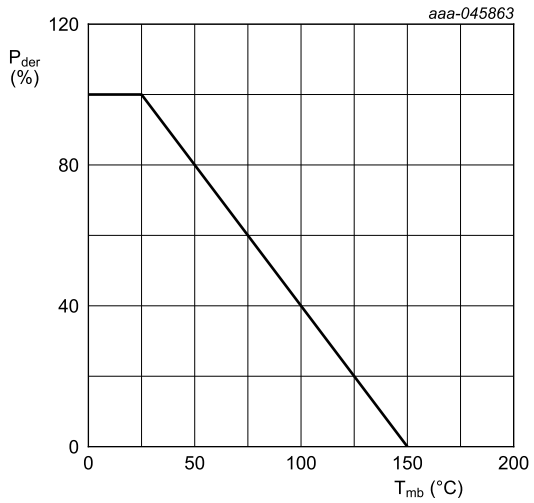
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 150 °C		-	650	V
V_{DSM}	peak drain-source voltage	non-repetitive	[1]	-	800	V
		repetitive	[2]	-	750	V
V_{GS}	gate-source voltage	DC		-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	104	W

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Symbol	Parameter	Conditions		Min	Max	Unit
I_D	drain current	T_{mb} = 25 °C		-	32	A
		T_{mb} = 100 °C		-	20	A
I_{DM}	peak drain current	pulsed; t_p = 10 µs; T_{mb} = 25 °C		-	150	A
T_{stg}	storage temperature			-55	150	°C
T_j	junction temperature			-55	150	°C
$T_{sld(M)}$	peak soldering temperature		[3]	-	260	°C

[1] duty cycle < 1% , spike duration < 30µs, non-repetitive
[2] duty cycle < 1% , spike duration < 30µs, repetitive for ≤ 85 °C , non-repetitive up to 150 °C
[3] for 10 seconds, 1.6mm from the case



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base			-	1.2	-	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient			-	40	-	K/W

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{S\ (pulsed)}$	Pulsed reversed current	V_{SD} = 6 V; T_j = 150 °C; $t_p \leq$ 10 µs; V_{GS} = 0 V		-	-	69	A
Static characteristics							
$V_{GS(th)}$	gate-source threshold voltage	I_D = 3 mA; V_{DS} = V_{GS}		3	3.5	4	V

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DSS}	drain leakage current	V_{DS} = 650 V; V_{GS} = 0 V; T_j = 25 °C		-	2	40	µA
		V_{DS} = 650 V; V_{GS} = 0 V; T_j = 150 °C		-	15	-	µA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 22 A; T_j = 25 °C	[1]	-	50	60	mΩ
		V_{GS} = 10 V; I_D = 22 A; T_j = 150 °C	[1]	-	105	-	mΩ
I_{GSS}	gate leakage current (drain shorted)	-20 V ≤ V_{GS} ≤ 20 V		-20	-	20	µA
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 22 A; V_{DS} = 400 V; 0 V ≤ V_{GS} ≤ 10 V; T_j = 25 °C; Fig. 11		-	31	-	nC
Q_{GS}	gate-source charge	I_D = 22 A; V_{DS} = 400 V; 0 V ≤ V_{GS} ≤ 10 V; T_j = 25 °C		-	8	-	nC
Q_{GD}	gate-drain charge			-	13	-	nC
C_{iss}	input capacitance	V_{DS} = 400 V; V_{GS} = 0 V; f = 500 kHz; T_j = 25 °C; Fig. 12		-	1560	-	pF
C_{oss}	output capacitance			-	80	-	pF
C_{rss}	reverse transfer capacitance			-	10	-	pF
$C_{o(er)}$	effective output capacitance, energy related	0 V ≤ V_{DS} ≤ 400 V; V_{GS} = 0 V; T_j = 25 °C		-	124	-	pF
$C_{o(tr)}$	effective output capacitance, time related			-	224	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 400 V; 0 V ≤ V_{GS} ≤ 12 V; I_D = 22 A, R_{ON} = 47 Ω , R_{OFF} = 22 Ω, Z_{FB} = 120 Ω at 100 MHz		-	66	-	ns
t_r	rise time			-	8	-	ns
$t_{d(off)}$	turn-off delay time			-	84	-	ns
t_f	fall time			-	9	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; 0 V ≤ V_{DS} ≤ 400 V		-	90	-	nC
Source-drain characteristics							
V_{SD}	source-drain voltage	I_S = 22 A; V_{GS} = 0 V; T_j = 25 °C	[2]	-	1.6	-	V
t_{rr}	reverse recovery time	I_S = 22 A; dI_S/dt = 1000 A/µs; V_{GS} = 0 V; V_{DS} = 400 V		-	30	-	ns
I_S	reverse current	V_{GS} = 0 V; δ ≤ 25 %; T_{mb} = 100 °C		-	-	20	A

[1] Dynamic on-resistance
[2] Including the effect of dynamic on-resistance

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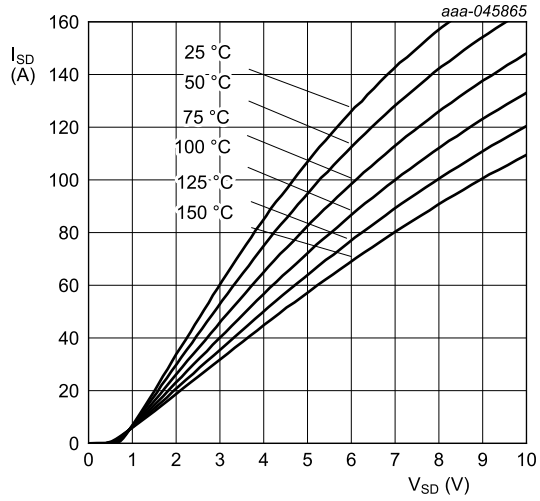
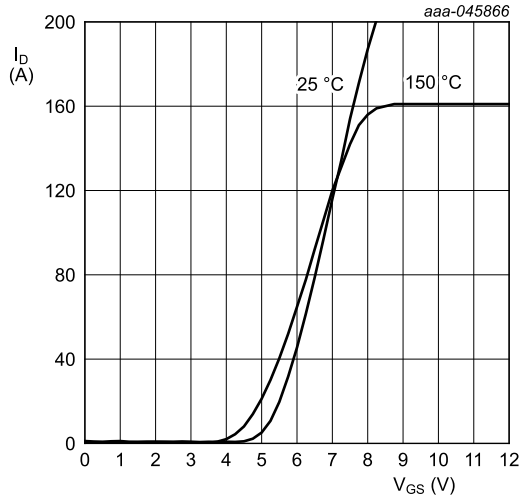
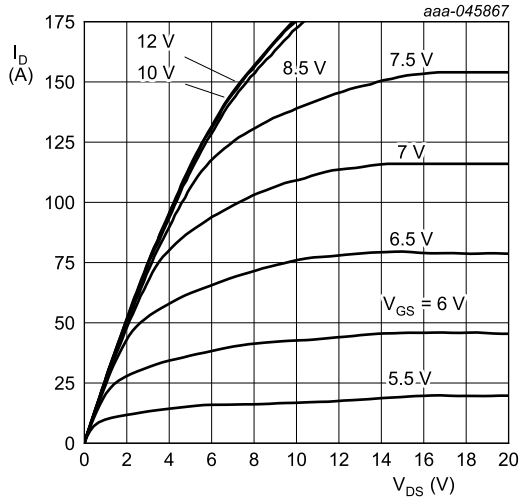


Fig. 2. Reverse conduction characteristics



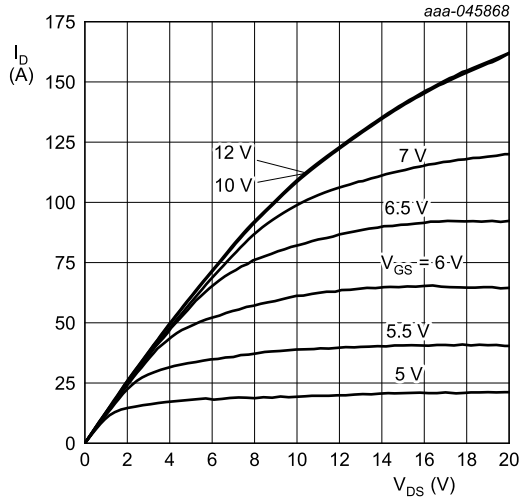
V_{DS} = 20 V

Fig. 3. Transfer characteristics



T_j = 25 °C

Fig. 4. Output characteristics: drain current as a function of drain-source voltage



T_j = 150 °C

Fig. 5. Output characteristics: drain current as a function of drain-source voltage

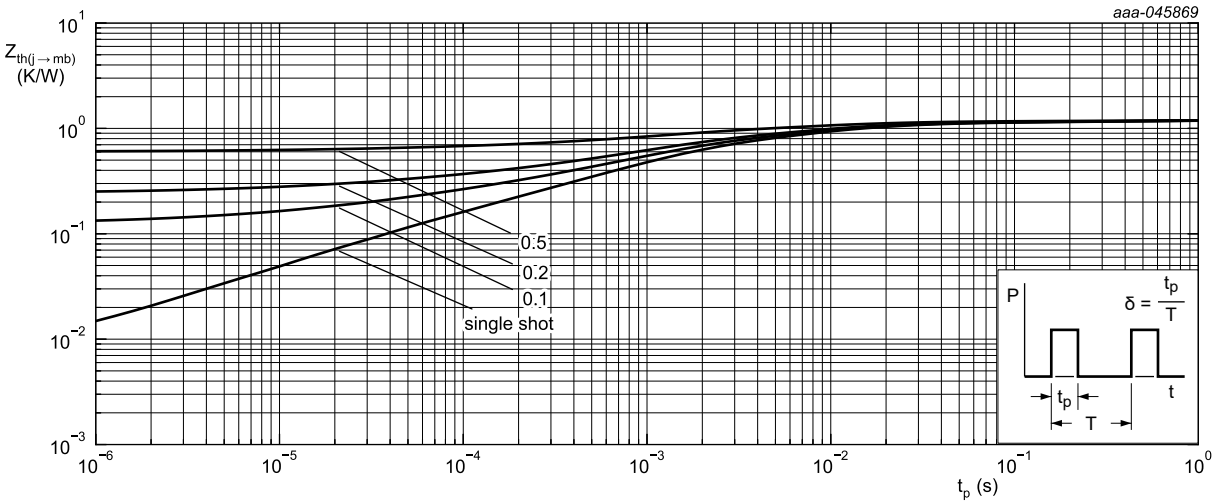


Fig. 6. Transient thermal resistance from junction to mounting base as a function of pulse duration

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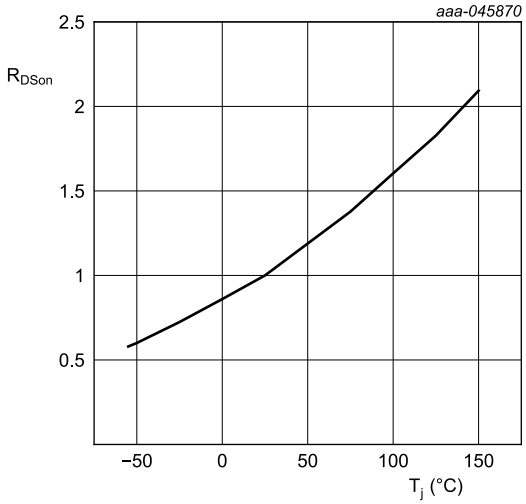


Fig. 7. Normalized on-resistance as a function of junction temperature

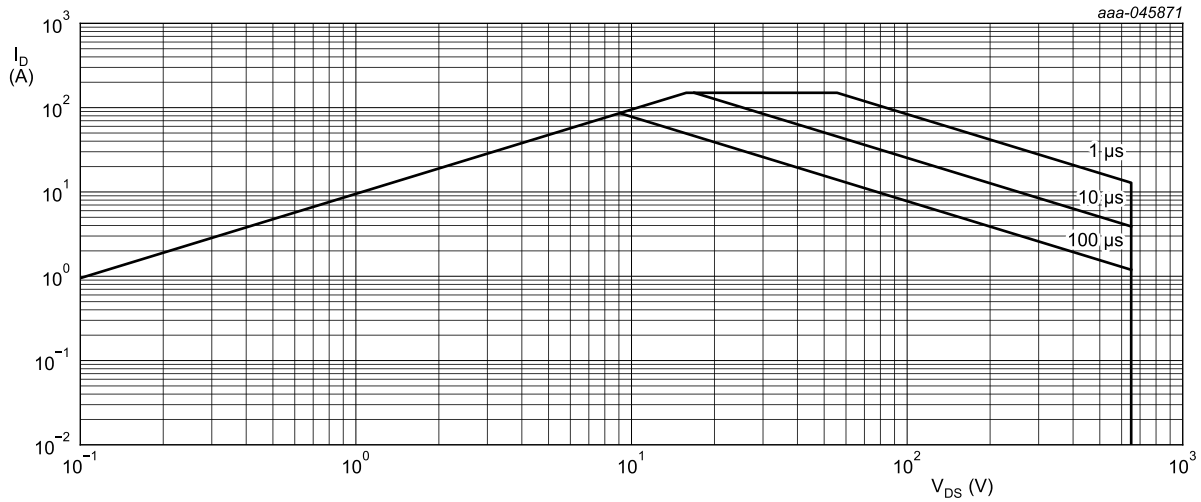


Fig. 8. Safe operating area T_{mb} = 25 °C

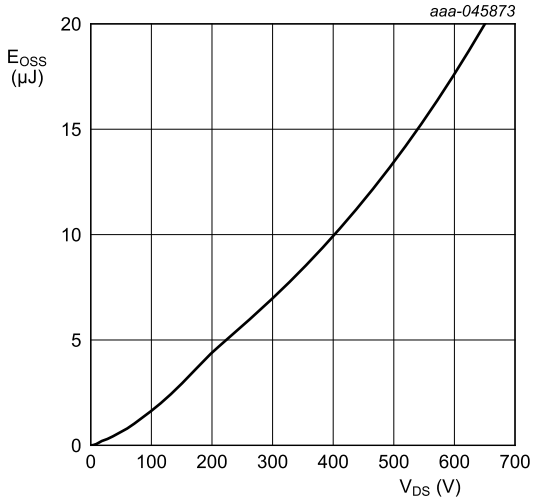
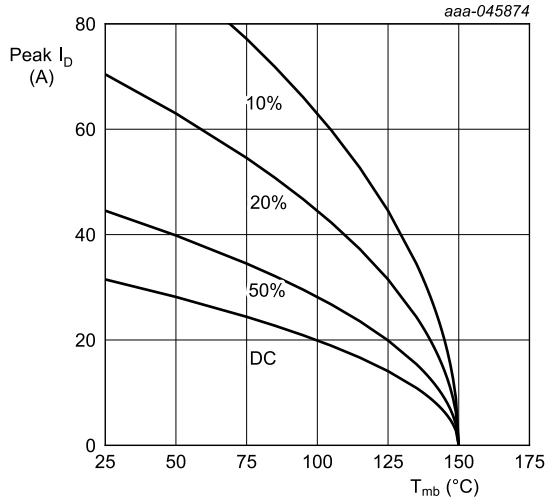


Fig. 9. Typical C_{oss} stored energy



Pulse Width ≤ 10 µs, V_{GS} ≥ 10 V

Fig. 10. Current derating

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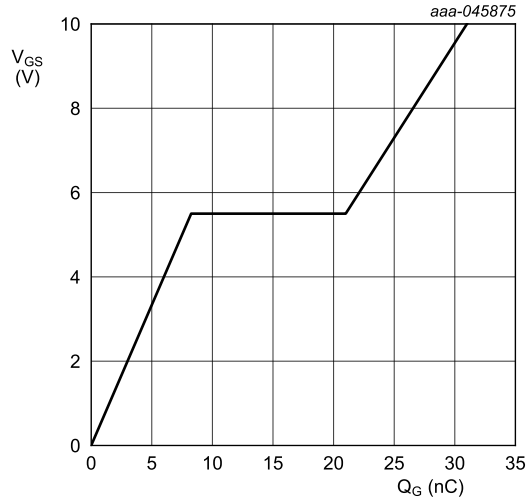


Fig. 11. Gate-source voltage as a function of gate charge

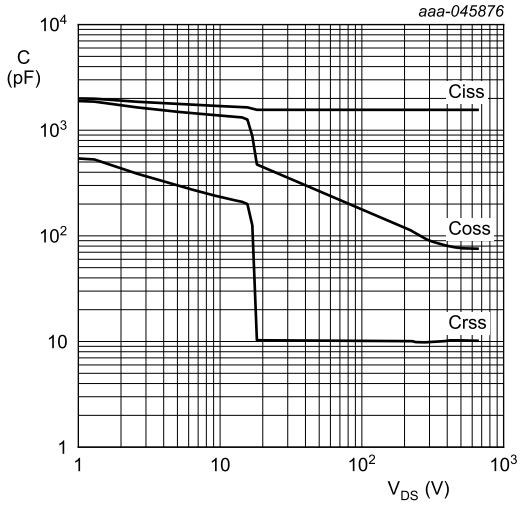


Fig. 12. Typical capacitance

11. Application information

A ferrite bead must be fitted in series with the gate of the GaN FET and should be located as close as possible to the gate pin (see Fig. 13).

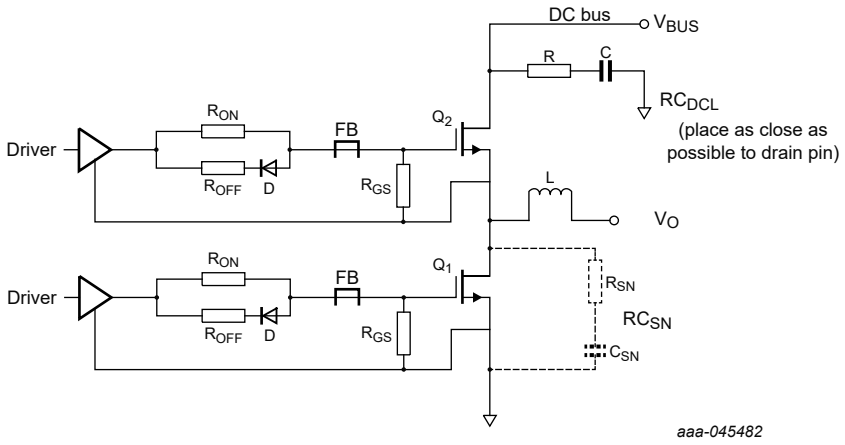


Fig. 13. Application diagram

Keeping the gate-source loop as compact as possible minimizes the gate-loop inductance. The ferrite bead damps the resonant circuit made up of the gate-source loop inductance and the GaN FET input capacitance, thus providing fast switching stability. It is recommended that the impedance of the ferrite bead should be between 80 to 120 Ω at 100 MHz (recommended part numbers: MH1608-800Y or BLM18PG121SN1D). Series resistance R_{ON} between 33 to 150 Ω and R_{OFF} between 20 to 47 Ω is also recommended.

A DC-link resonance damper is strongly recommended in all cases. An optimal value is 10 nF in series with 5.1 Ω, most easily achieved with a parallel combination of 4.7 nF and 10 Ω (see Fig. 14).

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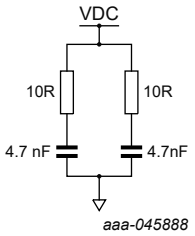


Fig. 14. DC-link resonance damper circuit

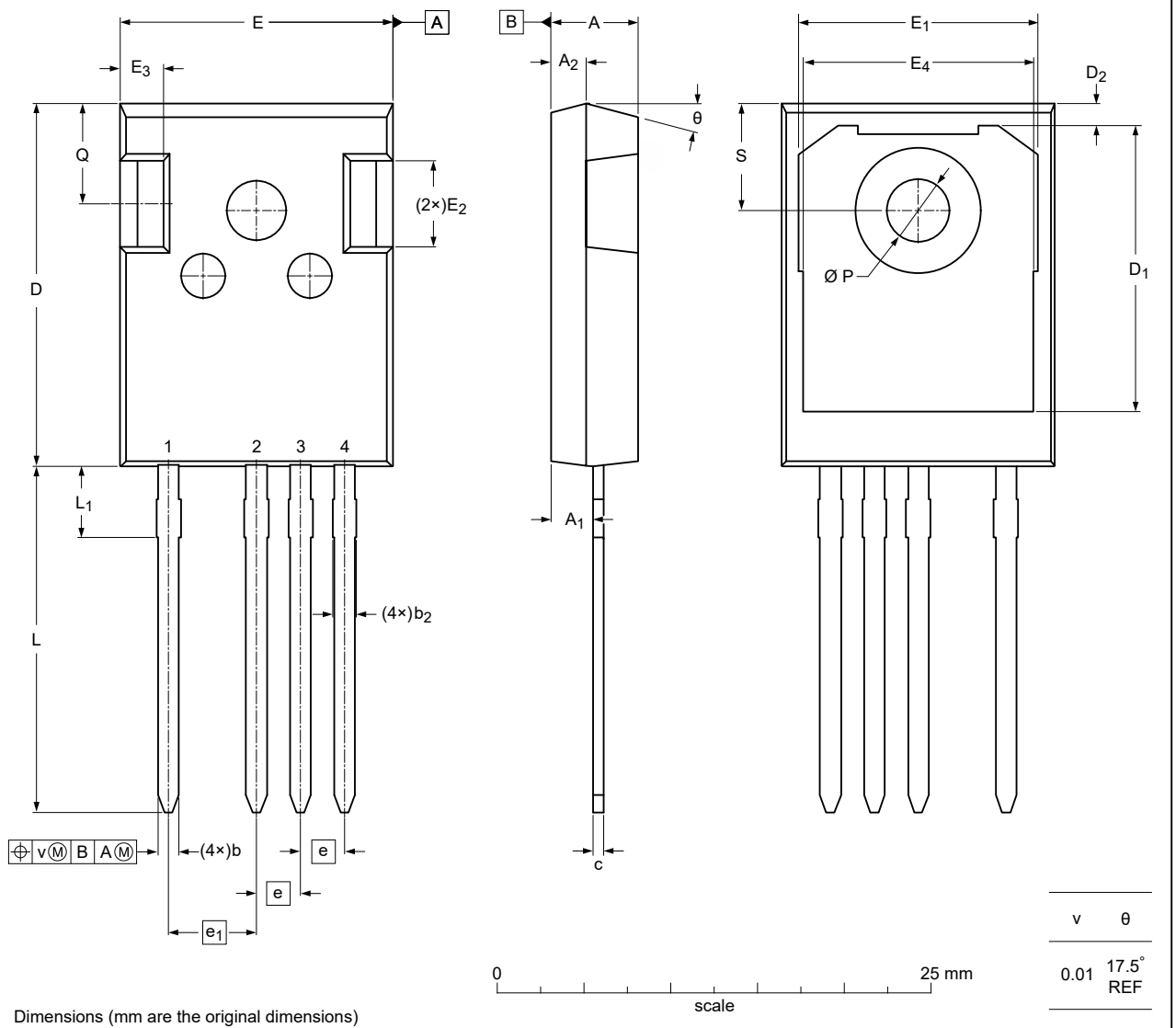
This resonance damper lowers the Q-factor of any resonance in the bus. That resonance will act as a load on the high-gain amplifier that is the GaN FET and can lead to instability. For very high current, or if R_{ON}/R_{OFF} are lower than suggested, an RC snubber is recommended for the switching node. This will increase switching loss, so this is only recommended at high power levels where the switching losses are a very small percentage of the total power.

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12. Package outline

Plastic, single-ended package (heatsink mounted, 1 mounting hole); 4 leads; 2.54 mm pitch; 20.95 mm × 15.94 mm × 5.02 mm body **SOT8071-2**



v	θ
0.01	17.5° REF

Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	b	b_2	c	D	D_1	D_2	E	E_1	E_2	E_3	E_4	e	e_1	L	L_1	P	Q	S
mm	max	5.21	2.54	2.16	1.30	1.50	0.68	21.10	17.65	1.25	16.13	14.15	5.10	1.90	13.43	2.54 BSC	5.08 BSC	20.32	4.44	3.65	6.00	6.30
	nom	4.83	2.29	1.91	1.10	1.30	0.55	20.80	16.25	0.95	15.75	13.10	4.32	1.00	12.38			19.72	4.04	3.51	5.49	6.04
	min																					

Note
1. All dimensions do not include mold flash or protrusions.

sot8071-2

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8071-2						26-01-30

Fig. 15. Package outline TO-247-4L (SOT8071-2)

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