DELKIN DEVICES®

Utility

microSD

Engineering Specification

Document Number: 401-0667-00

Revision: A



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Overview

- **Capacity**
  - 32GB up to 128GB
- **Bus Speed Mode**
  - UHS-I
- **Flash Interface**
  - Flash Type: 3D TLC
- **Power Consumption**[Note1]
  - Power Up Current < 250uA
  - Standby Current < 1mA
  - Read Current < 400mA
  - Write Current < 400mA
- **Performance**
  - Read: Up to 95 MB/s
  - Write: Up to 85 MB/s
- **Advanced Flash Management**
  - Static and Dynamic Wear Leveling
  - Bad Block Management
  - SMART Function
  - ECC Correction
- **Storage Temperature Range**
  - -40°C ~ 85°C
- **Operation Temperature Range**
  - -25°C ~ 85°C
- **RoHS compliant**
- **EMI compliant**

Notes:

1. Varies by capacity, please see Section “5.1 Power Consumption” for details.

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Performance and Power Consumption

Capacity	Performance		Power Consumption (Maximum)		
	TestMetrix Test		Read (mA)	Write (mA)	Standby (mA)
	Read (MB/s)	Write (MB/s)			
32GB	95	50	400	400	1
64GB	95	50	400	400	1
128GB	95	85	400	400	1

NOTE:

For more details on Power Consumption, please refer to Section 5.1.

Power Consumption figures shown are maximum values and may vary with usage model, SDR configuration or host platform.

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1. INTRODUCTION

1.1. General Description

Delkin's 3D TLC Utility microSD card version 6.10 is fully compliant with the specification released by the SD Card Association. The Command List supports [Part 1 Physical Layer Specification Version 6.10 Final] definitions and Card Capacity of Non-secure Area, Secure Area Supports [Part 3 Security Specification Ver4.00 Final] Specifications.

The Utility microSD 6.10 card utilizes the standard 8-pin interface, designed to operate at a maximum operating frequency of 208MHz. It can alternate between SD mode and SPI mode communication protocols. microSD also has the benefits of lower power consumption.

Delkin's Utility microSD 6.10 card is an extremely popular choice today based on its high performance, excellent reliability and wide compatibility. It is ideal for OEM applications in semi-industrial, medical, handheld, and other markets requiring a controlled, yet cost-effective solution.

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1.2. Flash Management

1.2.1. Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, Delkin's SD/microSD 6.10 controller applies the SECC Algorithm, which can detect and correct errors that occur during the Read process, ensure data has been read correctly, as well as protect data from corruption.

1.2.2. Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas are updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling techniques are applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media. Delkin's controller utilizes an advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND Flash is greatly improved.

1.2.3. Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as "Initial Bad Blocks". Bad blocks that are developed during the lifespan of the flash are named "Later Bad Blocks". Delkin's SD 6.10 controller implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that develop with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

1.2.4. Smart Function

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is a special function that allows a memory device to automatically monitor its health. Delkin provides a dashboard to observe Utility SD and microSD cards. **Note that this tool can only support Delkin Utility or Industrial SD and microSD cards which are SMART-enabled and contain specific controllers.** This dashboard will display the, endurance life ratio, good block ratio, and so forth. In addition, a warning message will appear under the following 3 conditions:

(1) When the life ratio remained is less than **10%**,

(2) When the amount of abnormal power on is more than **3,500** cycles, and

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(3) When there are less than **5** usable blocks for replacing bad blocks.

1.2.5. Auto-Read Refresh

Auto-Read Refresh is applied on devices that mostly read data but rarely write data, GPS systems, for example. When blocks are continuously read, then the device cannot activate wear leveling since it is only applied while writing data. Thus, errors can accumulate and become uncorrectable. Therefore, to avoid the accumulation of errors that exceed the quantity correctable by the controller's ECC, which would result in bad blocks, Delkin's controller firmware will automatically refresh the bit errors when the error number in one block approaches the threshold, ex., 24 bits.

1.2.6. Embedded Mode

Embedded mode is a function specially designed for Linux or customized OS use. Often under non-Windows OS, the default FAT system will not be used. In this case, the wear leveling mechanism of the SD cards will be affected, or even disabled in some cases. Embedded mode ensures that under any circumstances, the wear leveling mechanism will be activated, to keep the usage of blocks even throughout the card's life cycle. Embedded mode is enabled as a standard feature on the Utility Endurance microSD cards denoted in this specification.

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2. PRODUCT SPECIFICATION OVERVIEW

- **Capacity**
  - 32GB up to 128GB
- **Operation Temp. Range**
  - -25~85°C
- **Storage Temp. Range**
  - -40~+85°C
- **Support SD system specification version 3.00**
- **Card capacity of non-secure area and secure area support [Part 3 Security Specification Ver4.0 Final] Specifications**
- **Supports SD SPI mode**
- **Designed for read-only and read/write cards**
- **Bus Speed Mode (use 4 parallel data lines)**
  - **UHS-I mode**
    - SDR12: SDR up to 25MHz, 1.8V signaling
    - SDR25: SDR up to 50MHz, 1.8V signaling
    - SDR50: 1.8V signaling, frequency up to 100MHz, up to 50 MB/sec
    - SDR104: 1.8V signaling, frequency up to 208MHz, up to 104MB/sec
    - DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50 MB/sec

    Note: Timing in 1.8V signaling is different from that of 3.3V signaling.
- **The command list supports [Part 1 Physical Layer Specification Ver6.10 Final] definitions**
- **Copyright Protection Mechanism**
  - Compliant with the highest security of SDMI standard
- **Supports optional CPRM (Content Protection for Recordable Media) of SD Card**
  - Compliant with [Physical Layer Specification Ver6.10 Final] CPRM optional definition.

    Note: CPRM card is compliant with [Physical Layer Specification Ver5.10 Final]
- **Password Protection of cards (optional)**
- **Built-in write protection features (permanent and temporary)**
- **Operation voltage range: 2.7 ~ 3.6V**

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2.1. Performance

Capacity	Mode	UHS Speed Class	Sequential	
			Read (MB/s)	Write (MB/s)
32GB	UHS-I	Speed Class 1	95	50
64GB	UHS-I	Speed Class 1	95	50
128GB	UHS-I	Speed Class 1	95	85

NOTES:

1. Benchmark performance measured with TestMetrix Test

2.2. Part Numbers

Utility microSD

Capacity	Part Number
32GB	S432CWMY3-U3000-3
64GB	S464CWMY3-U3000-3
128GB	S41HCWMY3-U3000-3

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3. ENVIRONMENTAL SPECIFICATIONS

3.1. Environmental Conditions

3.1.1. Temperature and Humidity

- Storage Temperature Range
  - -40°C ~ 85°C
- Operation Temperature Range
  - -25°C ~ 85°C
- Humidity
  - 95% RH at 40°C

  Test Time
    - Storage 500 hours
    - Operation 4 hours

3.1.2. Shock & Vibration

- Shock Specification
  - Acceleration Force: 1500G, Half Sin Pulse Duration: 0.5ms
- Vibration Specification
  - Frequency/Displacement: 20Hz ~80Hz/1.52mm
  - Frequency/Acceleration: 80Hz~2000Hz / 20G Acceleration, 3 axes
    - Vibration Orientation: X, Y, Z axis/30 min for each

3.1.3. Durability

- Mating Cycles
  - 10,000 mating cycles

3.1.4. Electrostatic Discharge (ESD)

- Contact
  - ± 4KV each item 25 times
- Air
  - ± 8KV 10 times

3.1.5. EMI Compliance

- FCC: CISPR22
- CE: EN55022
- BSMI 13438

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3.2. MTBF

MTBF, an acronym for Mean Time Between Failures, is a measure of a device's reliability. Its value represents the average time between a repair and the next failure. The measure is typically in units of hours. The higher the MTBF value, the higher the reliability of the device. The predicted result of Delkin's Utility Endurance microSD is more than 3,000,000 hours.

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4. SD CARD COMPARISON

Table 4-1 Comparing SD6.X Standard, SD6.0 SDHC and SD6.0 SDXC

	microSDSC	microSDHC	microSDXC
Addressing Mode	Byte (1 byte unit)	Block (512 byte unit)	Block (512 byte unit)
HCS/CCS bits of ACMD41	Supported	Supported	Supported
CMD8 (SEND_IF_COND)	Supported	Supported	Supported
CMD16 (SET_BLOCKLEN)	Supported	Supported (Only CMD42)	Supported (Only CMD42)
Partial Read	Supported	Not Supported	Not Supported
Lock/Unlock Function	Mandatory	Mandatory	Mandatory
Write Protect Groups	Optional	Not Supported	Not Supported
Supply Voltage 2.7v – 3.6v (for operation)	Supported	Supported	Supported
Total Bus Capacitance for each signal line	40pF	40pF	40pF
CSD Version (CSD_STRUCTURE Value)	1.0 (0x0)	2.0 (0x1)	2.0 (0x1)
Speed Class	Optional	Mandatory (Class 2 / 4 / 6 / 10)	Mandatory (Class 2 / 4 / 6 / 10)

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5. ELECTRICAL SPECIFICATIONS

5.1. Electrical Specifications

Absolute Maximum Rating

Item	Symbol	Parameter	Min	Max	Unit
1	T_a	Operating Temp	-40	+85	°C
2	T_{st}	Storage Temp	-40	+85	°C

Parameter	Symbol	Min	Max	Unit
Operating Temp	T_a	-40	+85	°C
V_{DD} Voltage	V_{DD}	2.7	3.6	V

5.2. DC Characteristics

5.2.1. Bus Operation Conditions for 3.3V Signaling

Table 5-1 Threshold Level for High Voltage Range

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75*V_{DD}		V	I_{OH}=-2mA VDD Min
Output Low Voltage	V_{OL}		0.125*V_{DD}	V	I_{OL}=2mA VDD Min
Input High Voltage	V_{IH}	0.625*V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.25*V_{DD}	V	
Power Up Time			250	ms	From 0V to V_{DD} min

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4	-	V	I_{OH}=-2mA
Output Low Voltage	V_{OL}	-	0.45	V	I_{OL}=2mA
Input High Voltage	V_{IH}	1.27	2.00	V	
Input Low Voltage	V_{IL}	V_{ss}-0.3	0.58	V	

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Parameter	Symbol	Min	Max.	Unit	Remarks
Input Leakage Current		-2	2	uA	DAT3 pull-up is disconnected.

Table 5-2 Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max.	Unit	Remarks
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

5.2.2. Bus Signal Line Load

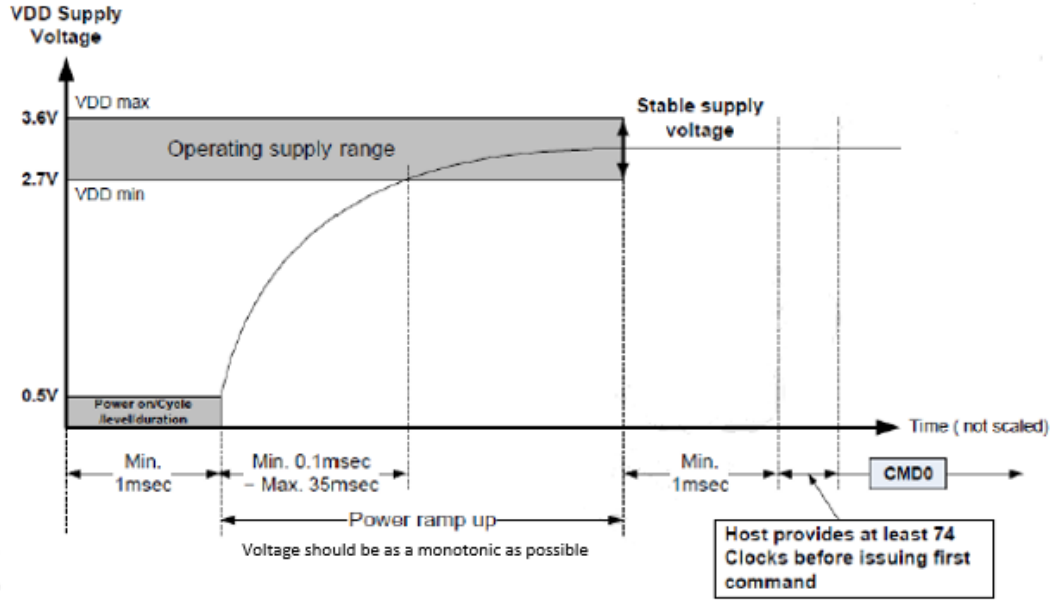
Bus Operation Conditions – Signal Line's Load

Total Bus Capacitance = C_{HOST} + C_{BUS} + N C_{CARD}

Parameter	symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card CHOST+CBUS shall not exceed 30 pF
Card Capacitance for each signal pin	C_{CARD}		10[1]	pF	
Maximum signal line inductance			16	nH	
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	kΩ	May be used for card detection
Capacity Connected to Power Line	C_C		5	uF	To prevent inrush current

5.2.3. Power Up Time of Host

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.



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Power On or Power Cycle

Followings are requirements for Power on and Power cycle to assure a reliable SD Card hard reset.

(1) Voltage level shall be below 0.5V.
(2) Duration shall be at least 1ms.

Power Supply Ramp Up

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD (min.) and VDD (max.) and host can supply SDCLK.

The following are recommendations of Power ramp up:

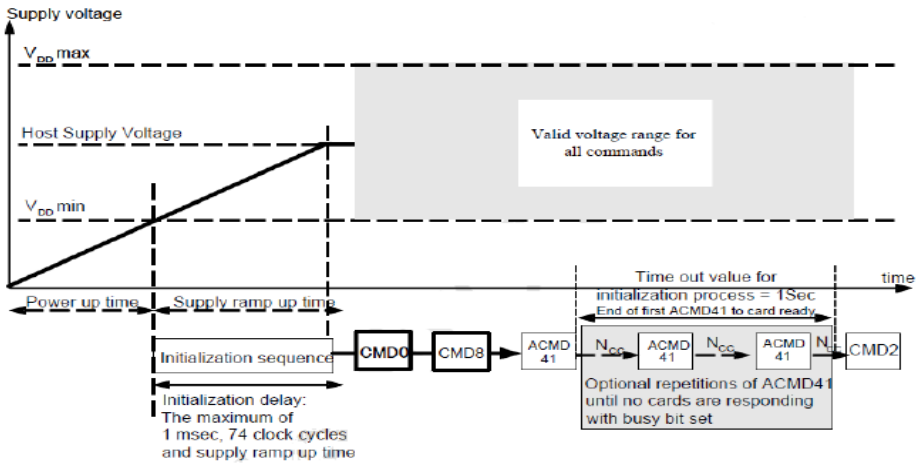
(1) Voltage of power ramp up should be monotonic as much as possible.
(2) The minimum ramp up time should be 0.1ms.
(3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.
(4) Host shall wait until VDD is stable.
(5) After 1ms VDD stable time, host provides at least 74 clocks before issuing the first command.

Power Down and Power Cycle

(1) When the host shuts down the power, the card VDD shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.
(2) If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in *Inactive State.* To create a power cycle the host shall follow the power down description before power up the card (i.e. the card VDD shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

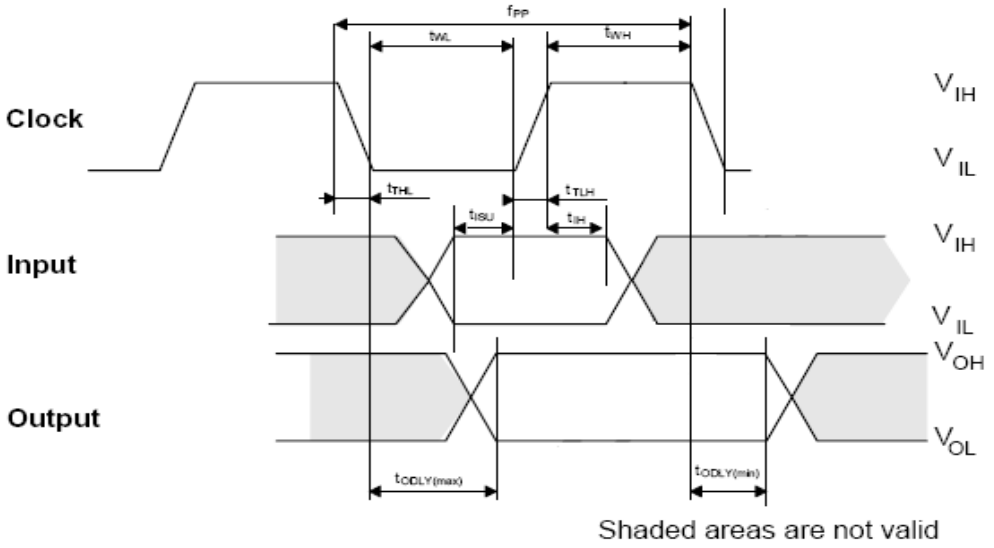
5.2.4. Power Up Time of Card

A device shall be ready to accept the first command within 1ms from detecting VDD min. Device may use up to 74 clocks for preparation before receiving the first command.



5.3. AC Characteristics

5.3.1. microSD Interface Timing (Default)

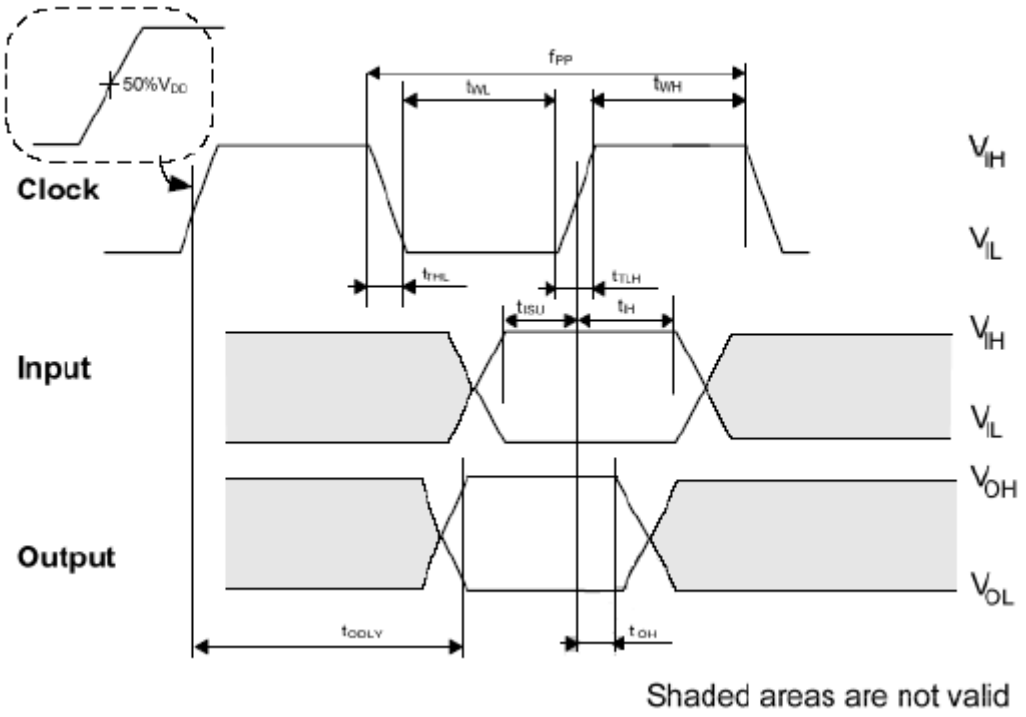


Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{card}≤10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	0(1)/100	400	kHz	C_{card}≤10 pF (1 card)
Clock low time	t_{WL}	10		ns	C_{card}≤10 pF (1 card)
Clock high time	t_{WH}	10		ns	C_{card}≤10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{card}≤10 pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{card}≤10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{card}≤10 pF (1 card)
Input hold time	t_{IH}	5		ns	C_{card}≤10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L≤40 pF (1 card)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	C_L≤40 pF (1 card)

(1) 0Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

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5.3.2. microSD Interface Timing (High-Speed Mode)



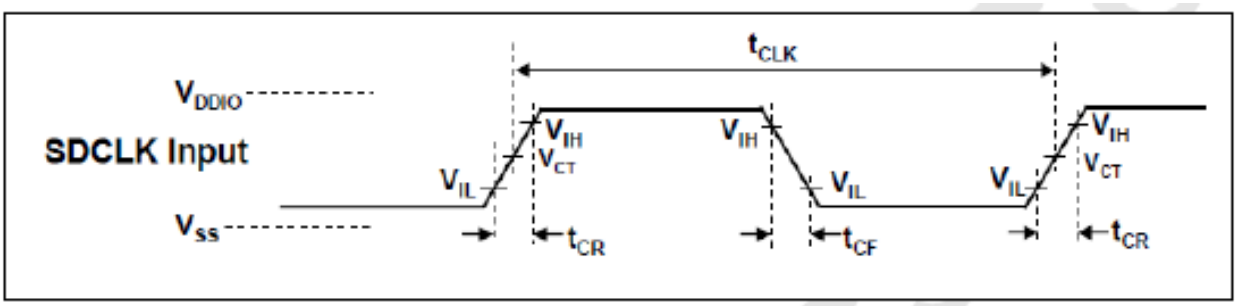
Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	$C_{card} \leq 10$ pF (1 card)
Clock low time	t_{WL}	7		ns	$C_{card} \leq 10$ pF (1 card)
Clock high time	t_{WH}	7		ns	$C_{card} \leq 10$ pF (1 card)
Clock rise time	t_{TLH}		3	ns	$C_{card} \leq 10$ pF (1 card)
Clock fall time	t_{THL}		3	ns	$C_{card} \leq 10$ pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	$C_{card} \leq 10$ pF (1 card)
Input hold time	t_{IH}	2		ns	$C_{card} \leq 10$ pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	$C_L \leq 40$ pF (1 card)
Output Hold time	T_{OH}	2.5		ns	$C_L \leq 15$ pF (1 card)
Total System capacitance of each line[1]	C_L		40	pF	CL ≤ 15 pF (1 card)

(1) In order to satisfy severe timing, the host shall drive only one card.

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5.3.3. microSD Interface Timing (SDR12, SDR25 and SDR 50 Modes)

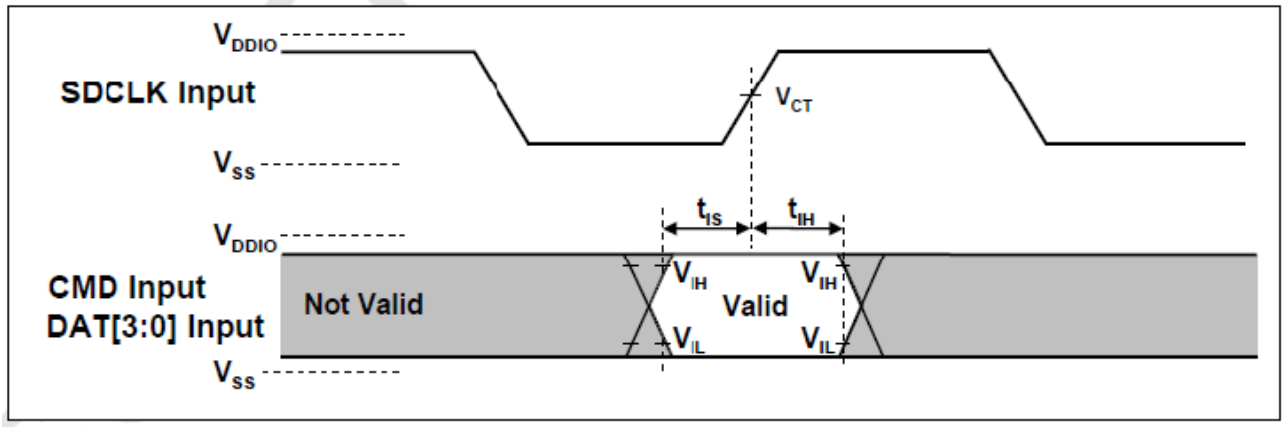
Input:



Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	4.8	-	ns	208MHz (Max.), Between rising edge, VCT= 0.975V
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR} , t_{CF} < 0.96ns (max.) at 208MHz, C_{CARD} =10pF t_{CR} , t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD} =10pF The absolute maximum value of t_{CR} , t_{CF} is 10ns regardless of clock frequency
Clock Duty	30	70	%	

SDR50 and SDR 104 Input Timing:

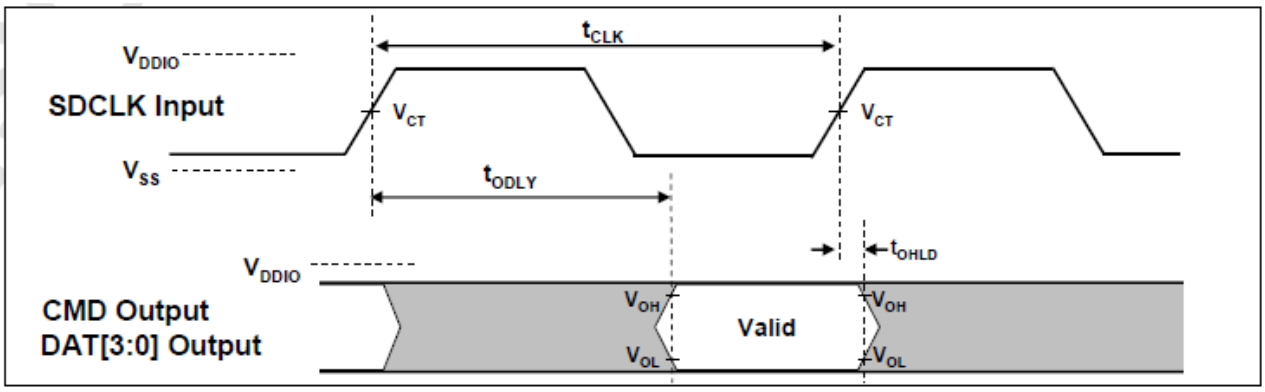


Card Input Timing

Symbol	Min	Max	Unit	SDR104 Mode
t_{IS}	1.40	-	ns	C_{CARD} =10pF, VCT= 0.975V
t_{IH}	0.80[1]	-	ns	C_{CARD} =5pF, VCT= 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR50 Mode**
t_{IS}	6.100	-	ns	C_{CARD} =10pF, VCT= 0.975V
t_{IH}	0.80[1]	-	ns	C_{CARD} =5pF, VCT= 0.975V

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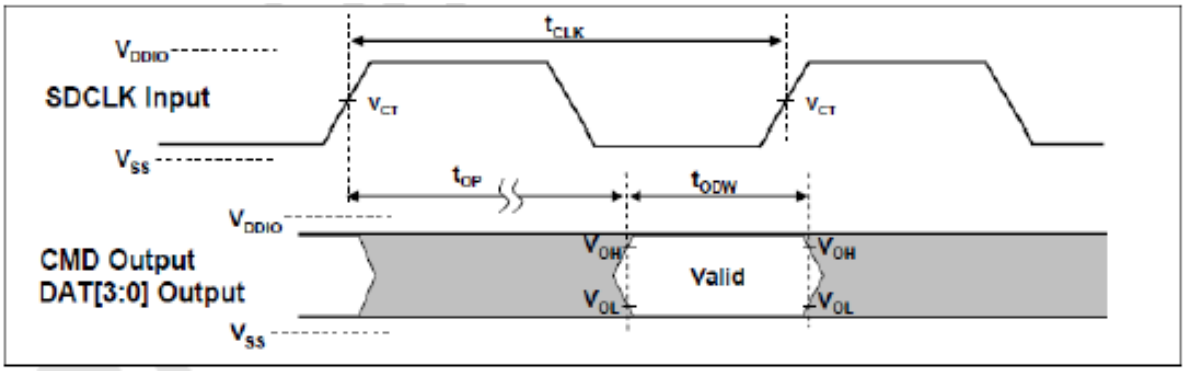
Output:



Output Timing of Fixed Data Window

Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK}>=10.0ns, C_L=30pF, using driver Type B, for SDR50
t_{ODLY}	-	14	ns	t_{CLK}>=20.0ns, C_L=40pF, using driver Type B, for SDR25 and SDR12
TOH	1.5	-	ns	Hold time at the t_{ODLY} (min.), C_L=15pF

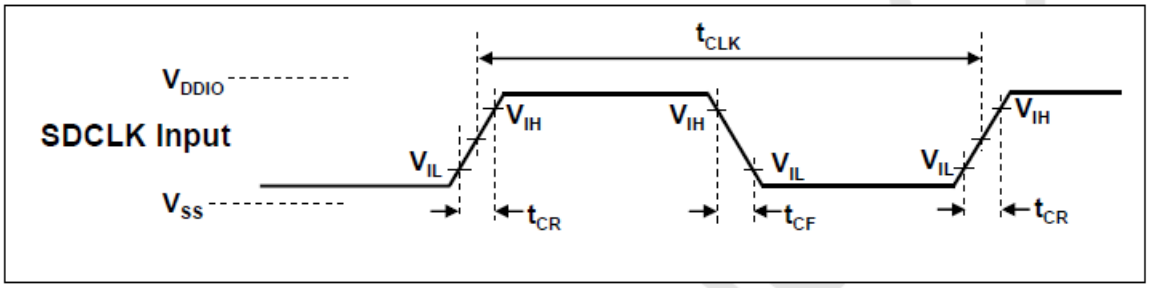
Output (SDR104 mode):



Symbol	Min	Max	Unit	Remark
t_{OP}	-	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variable due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

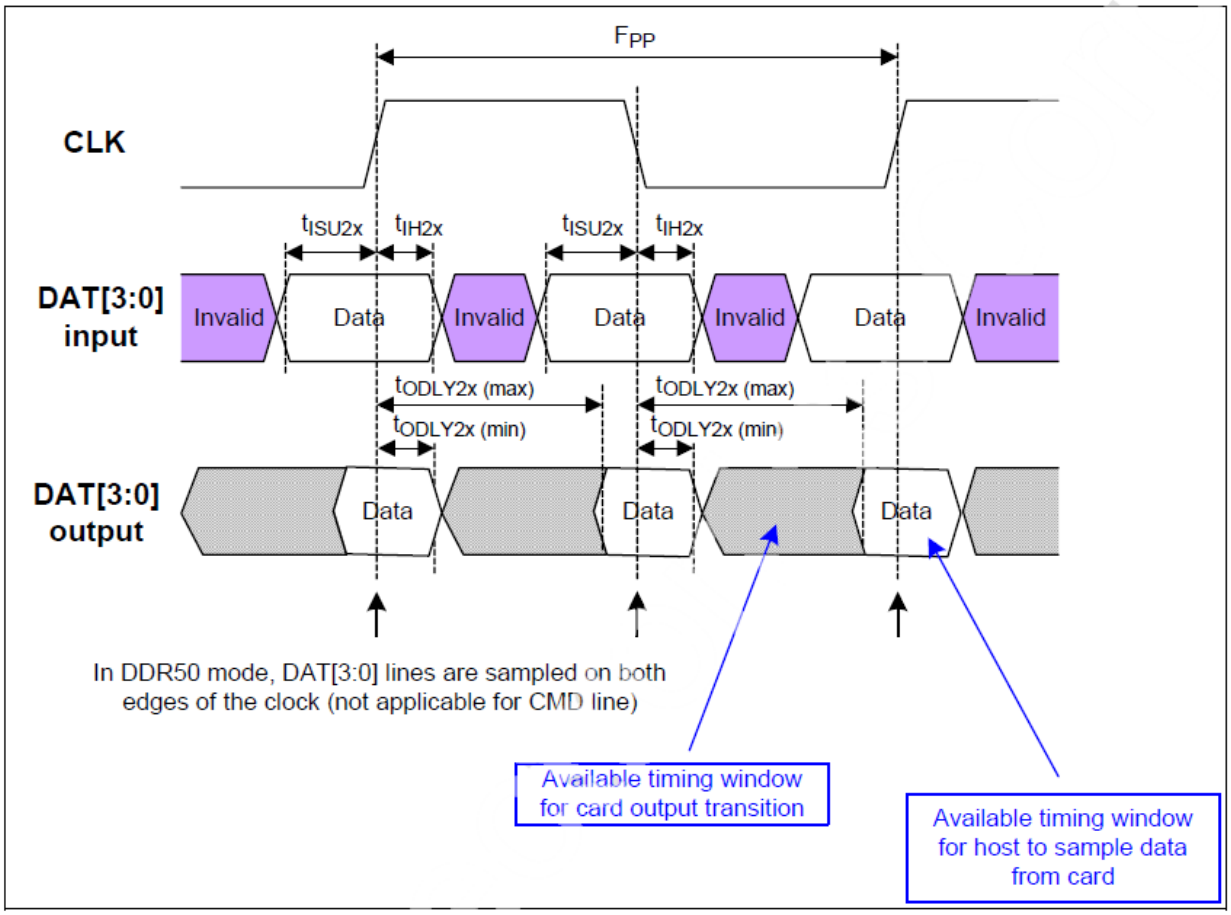
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5.3.4. microSD Interface Timing (DDR50 Mode)



Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, C_{CARD}=10pF
Clock Duty	45	55	%	



Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

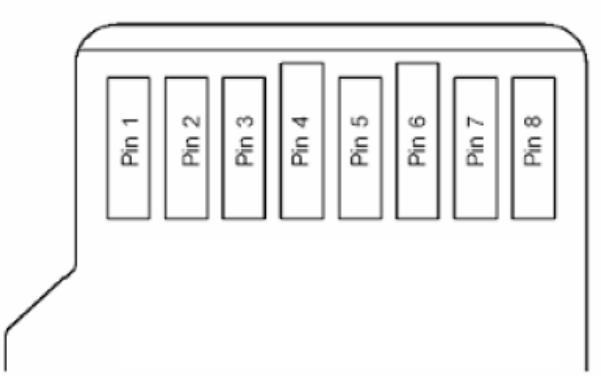
Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	3	-	ns	C_{card}≤10 pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{card}≤10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	C_L≤30 pF (1 card)
Output Hold time	T_{OH}	1.5	-	ns	C_L≥15 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	C_{card}≤□10 pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{card}≤□10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	C_L≤25 pF (1 card)
Output Hold time	T_{OH2x}	1.5	-	ns	C_L≥15 pF (1 card)

BUS TIMINGS PARAMETERS VALUES (DDR50 MODE)

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6. INTERFACE

6.1. Pad Assignment and Descriptions



pin	SD Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type	Description
1	DAT2	I/O/PP	Data Line[bit2]	RSV		
2	CD/DAT3 [2]	I/O/PP [3]	Card Detect/ Data Line[bit3]	CS	I [3]	Chip Select (neg true)
3	CMD	PP	Command/Response	DI	I	Data In
4	V_{DD}	S	Supply voltage	V_{DD}	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS}	S	Supply voltage ground	V_{SS}	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line[bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line[bit1]	RSV		

(1) S: power supply, I: input; O: output using push-pull drivers; PP:I/O using push-pull drivers

(2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMedia Cards.

(3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer period, with SET_CLR_CARD_DETECT (ACMD42) command.

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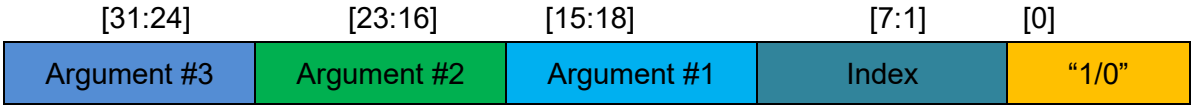
Name	Width	Description
CID	128bit	Card identification number; card individual number for identification. **Mandatory**
RCA[1]	16bit	Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization. **Mandatory**
DSR	16bit	Driver Stage Register; to configure the card's output drivers. **Optional**
CSD	128bit	Card Specific Data; information about the card operation conditions. **Mandatory**
SCR	64bit	SD Configuration Register; information about the SD Memory Card's Special Features capabilities **Mandatory**
OCR	32bit	Operation conditions register. **Mandatory.**
SSR	512bit	SD Status; information about the card proprietary features **Mandatory**
OCR	32bit	Card Status; information about the card status **Mandatory**

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7. SMART

7.1. Direct Host Access to SMART Data via SD General Command (CMD56)

CMD 56 is structured as a 32-bit argument. The implementation of the general purpose functions will arrange the CMD56 argument into the following format:



Bit [0] Indicates Read Mode when bit is set to [1] or Write Mode when bit is cleared [0]. Depending on the function, either Read Mode or Write Mode can be used.

Bit [7:1] Indicates the index of the function to be executed:

- Read Mode
  - Index = 0x10 Get SMART Command Information
- Write Mode
  - Index = 0x08 Pre-Load SMART Command Information

Bit [15:8] Function argument #1 (1-byte)

Bit [23:16] Function argument #2 (1-byte)

Bit [31:24] Function argument #3 (1-byte)

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7.1.1. Process for Retrieving SMART Data

STEP 1:

Write Mode – [0x08] Pre-Load SMART Command Information

Sequence	Command	Argument	Expected Data
Pre-Load SMART Command Information	CMD56	[0] "0" (Write Mode) [1:7] "0001 000" (Index = 0x08) [8:511] All '0' Reserved)	No Expected Data

STEP 2:

Read Mode – [0x10] Get SMART Command Information

Sequence	Command	Argument	Expected Data
Get SMART Command Information	CMD56	[0] "1" (Read Mode) [1:7] "0010 000" (Index = 0x10) [8:511] All '0' Reserved)	1 sector (512 bytes) of response data Byte [0-8] Flash ID Byte [9-10] IC Version Byte [11-12] FW Version Byte [13] Reserved Byte [14] CE Number Byte [15] Reserved Byte [16-17] Maximum Bad Block Replacement Byte [18] Reserved Byte [32-63] Bad Block Count per CE Byte [64-65] Good Block Rate (%) Byte [66-79] Reserved Byte [80-83] Total Erase Count Byte [84-95] Reserved Byte [96-97] Calculated Remaining Life (%) Byte [98-99] Average Erase Count Byte [100-101] Minimum Erase Count Byte [102-103] Maximum Erase Count Byte [104-111] Reserved Byte [112-115] Power Cycle Count Byte [116-127] Reserved Byte [128-129] Abnormal Power Down Count Byte [130-159] Reserved Byte [160-161] Total Refresh Count Byte [176-183] Product "Marker" Byte [184-511] Reserved

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Note: Both steps are required to retrieve SMART data - Pre-Load SMART Command followed by Get SMART Command, and must be in accordance with the SD Association standard flowchart for CMD56 (below.)

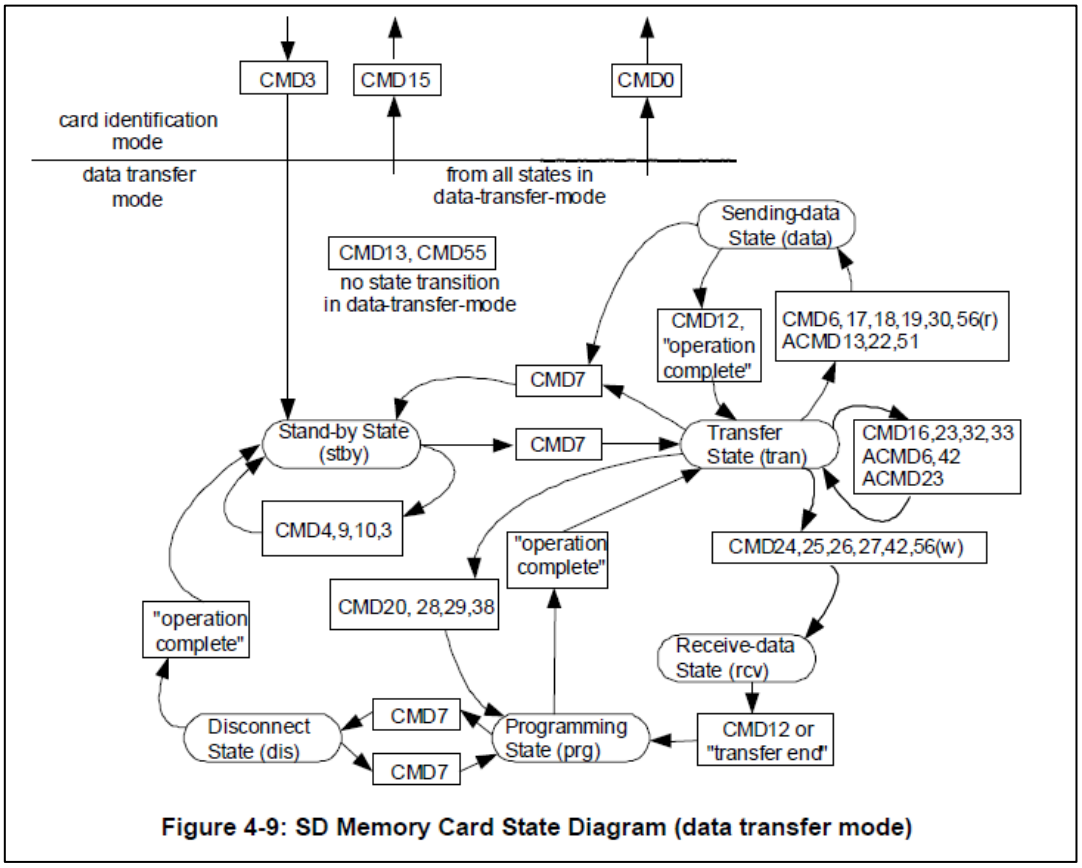


Figure 4-9: SD Memory Card State Diagram (data transfer mode)

Extracted from the SD Specifications Part 1 Physical Layer Simplified Specification Version 6.101.

7.1.2. Definitions for Response Data Bytes

Response Data	Description
Flash ID	NAND Flash Type
IC Version	Controller Version
FW Version	Firmware Version
CE Number	Number of chip enables active
Maximum Bad Block Replacement	Number of spare blocks remaining
Bad Block Count per CE	Number of initial & new bad blocks per chip enable
Good Block Rate (%)	Percent of total blocks that are still marked good
Total Erase Count	Total number of block erases at the card level
Calculated Remaining Card Life	[(Rated P/E cycles – Current Erase Count) / Rated P/E Cycles] * 100%
Average Erase Count	Average erase count over all blocks
Minimum Erase Count	Minimum erase count over all blocks
Maximum Erase Count	Maximum erase count over all blocks
Power Cycle Count	Number of normal power up sequences
Abnormal Power Down Count	Number of unexpected power interruptions
Total Refresh Count	Total read refresh count
Product “Marker”	Product type

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7.2. Direct Host Access via DLL for Windows or Linux Operating Systems

Note: Card must be in Idle state before and while accessing card as per steps below.

API entry:

```
int Get_Smart_Data(char drive_letter, unsigned char *buffer, int buffer_len, int *bytes_read);
```

Arguments:

1: Drive letter is a character of the drive letter, i.e. ‘E’
2: buffer is a pointer to a pre-allocated array to store SMART data, min 512 bytes
3: buffer_len indicates to the API the size of the buffer, typically it is 512 bytes
4: bytes_read indicates the number of bytes returned in the buffer

Return Value:

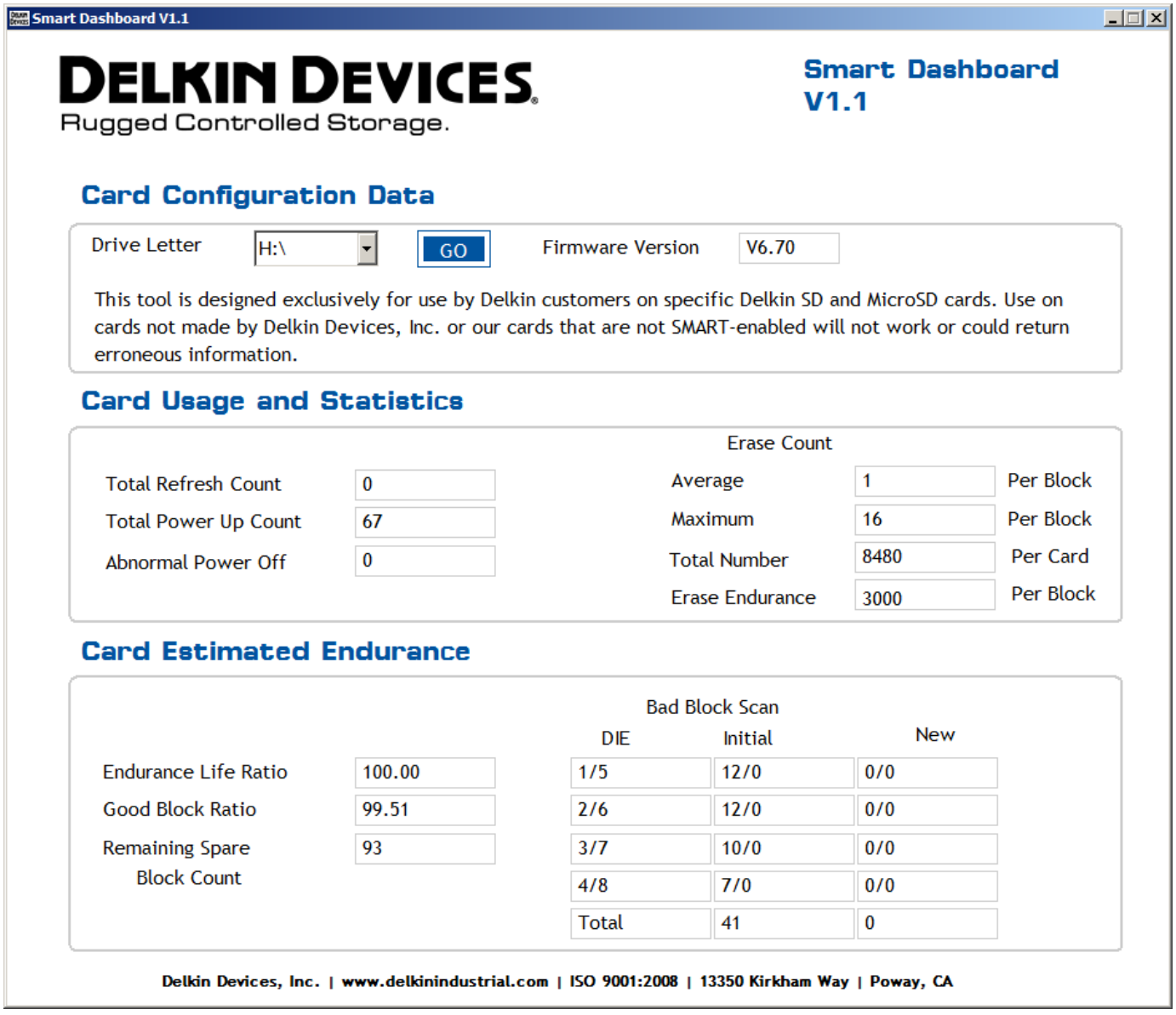
0 is success; Non zero is fail, with the following definitions:

1: "Initial Command Flow Fail"
2: "Read Capacity Fail"
3: "Switch To Vendor Mode Fail"
4: "Send Smart Info Command Fail"
5: "Get Command Response Fail"
6: "Command Response Info Incorrect"
7: "Read Command Info Fail"
8: "Check Command State Fail"
9: "Close Command Flow Fail"

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7.3. Access via Delkin SMART Dashboard Utility+

Please contact your Delkin Devices Account Manager to download the Delkin SMART dashboard Utility Endurance (for Windows OS only). SMART data is accessed by inserting a card in a USB reader or directly in a laptop SD slot (with an SD adapter.) Below is a screen shot of the dashboard with sample data:



Instructions for use:

1. Insert microSD in card reader or in SD slot on laptop (in SD adapter)
2. Select appropriate drive letter on Dashboard
3. Click “Go”

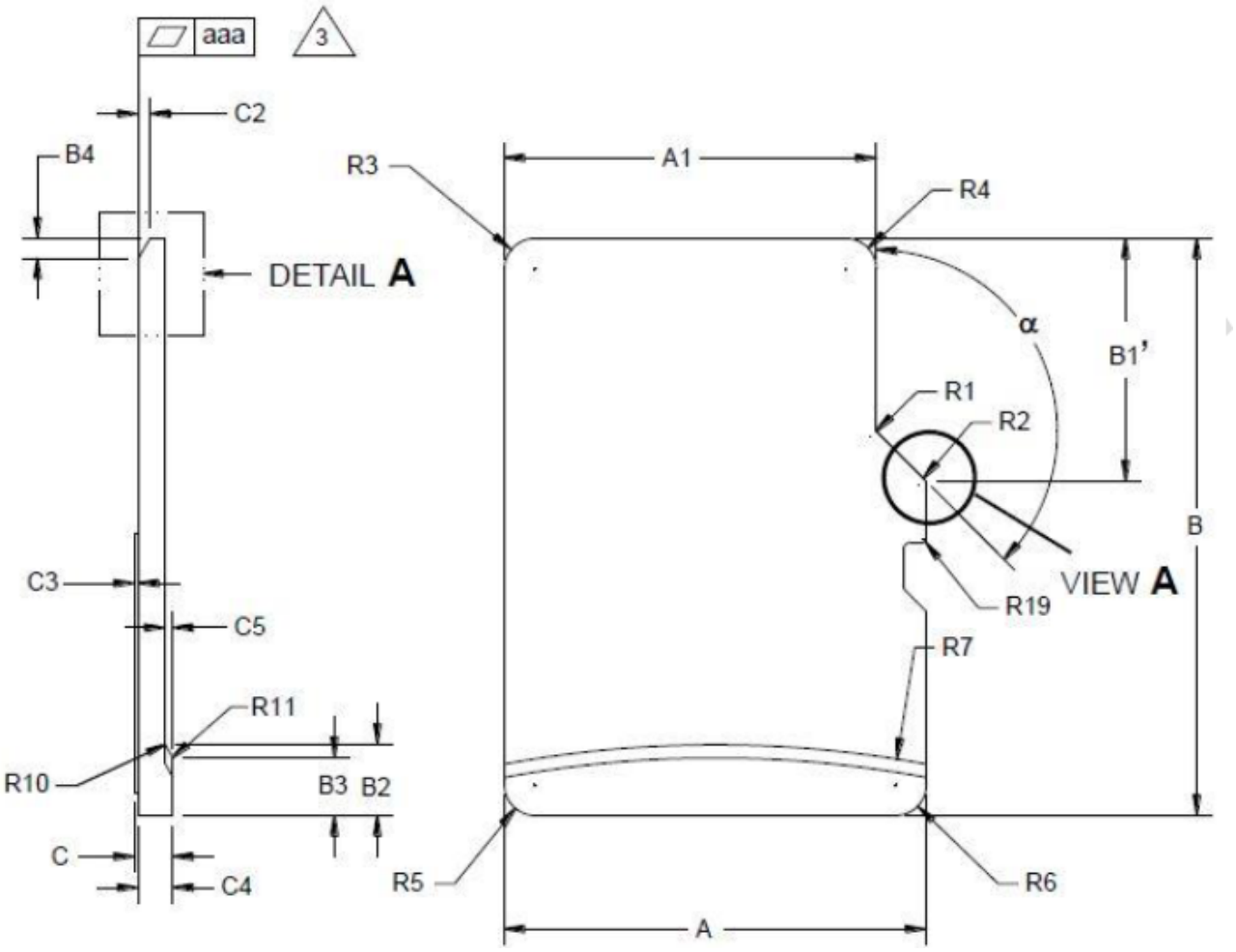
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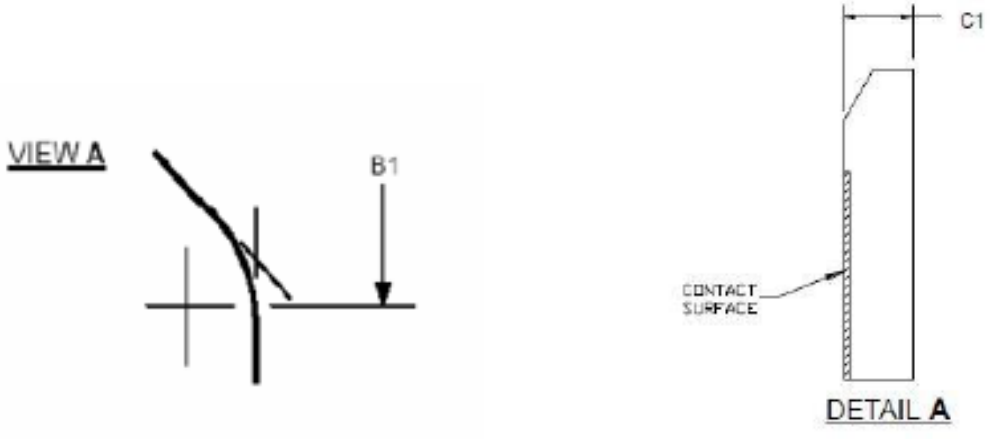
7.3.1. Dashboard Field Descriptions

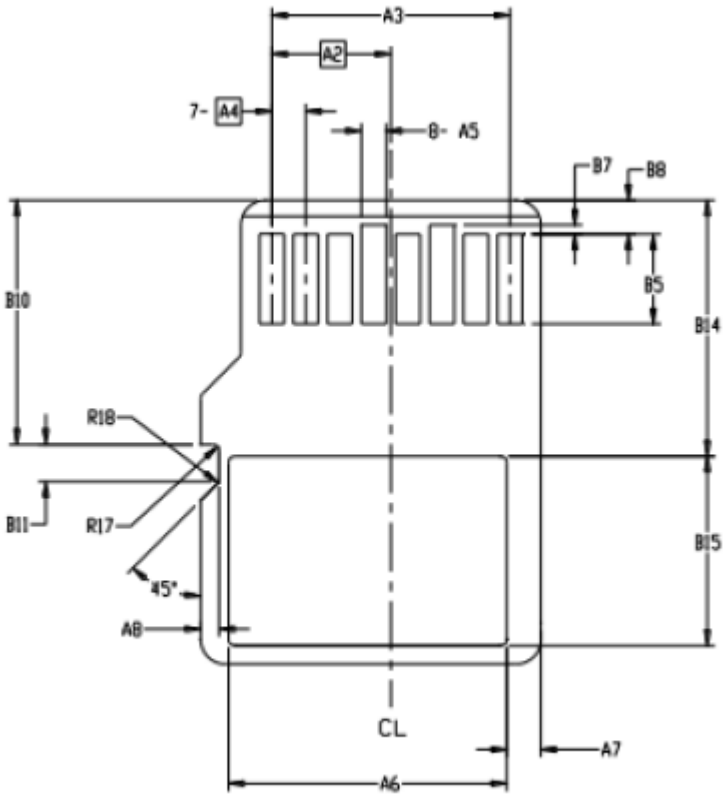
Response Data	Description
FW Version	Firmware Version
Total Refresh Count	Total read refresh count
Total Power Up Count	Number of normal power up sequences
Abnormal Power Off	Number of unexpected power interruptions
Average Erase Count	Average erase count over all blocks
Maximum Erase Count	Maximum erase count over all blocks
Total Erase Count	Total number of block erases at the card level
Erase Endurance	Flash program / erase cycle rating per block
Endurance Life Ratio	[(Rated P/E cycles – Current Erase Count) / Rated P/E Cycles] * 100%
Good Block Ratio	Percent of total blocks that are still marked good
Remaining Spare Block Count	Number of spare blocks remaining
Bad Block Scan - Initial (per die)	Bad blocks in flash from inception, prior to card use
Bad Block Scan - New (per die)	Bad blocks created after card use

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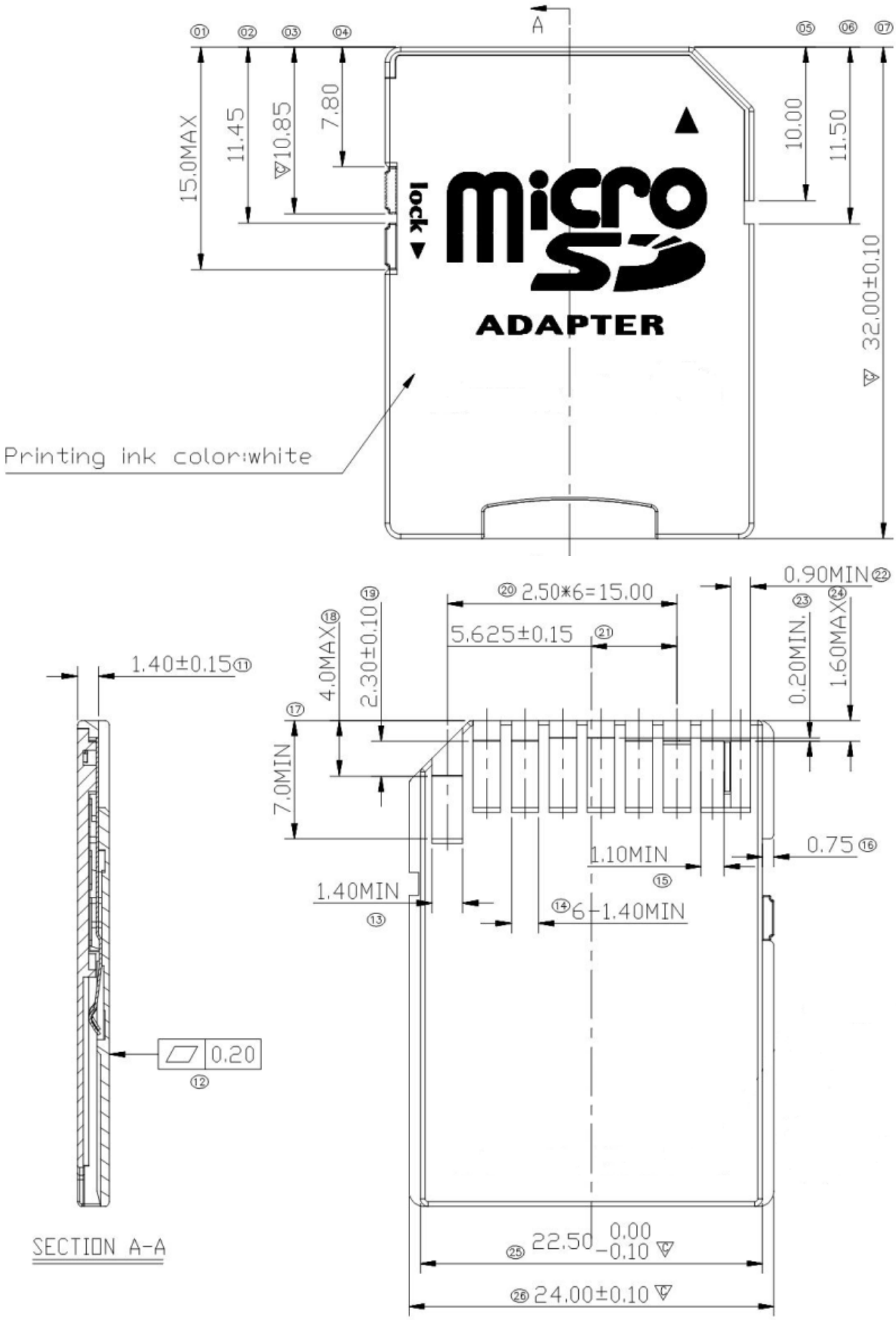
8. PHYSICAL DIMENSIONS







Type A


A
01
02
03
04
05
06
07
15.0MAX
11.45
10.85
7.80
10.00
11.50
32.00±0.10
lock
ADAPTER
Printing ink color:white
0.90MIN
22
20 2.50*6=15.00
19
5.625±0.15
21
4.0MAX
18
2.30±0.10
23
0.20MIN.
24
1.60MAX
1.40±0.15
11
17
7.0MIN
1.10MIN
15
0.75
16
1.40MIN
13
14 6-1.40MIN
0.20
12
SECTION A-A
25 22.50 0.00 -0.10
26 24.00±0.10

	COMMON DIMENSION			
SYMBOL	MIN	NOM	MAX	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
A10	1.35	1.40	1.45	
A11	6.50	6.60	6.70	
A12	0.50	0.55	0.60	
A13	0.40	0.45	0.50	
A14	0.05	-	-	
A15	5.71	5.91	5.91	
A16	6.47	6.57	6.67	
A17	6.62	6.72	6.82	
A18	7.38	7.48	7.58	
A19	7.76	7.86	7.96	
A20	8.55	8.65	8.75	
A21	0.90	-	-	
A22	-	-	8.50	
B	14.90	15.00	15.10	
B1'	6.13	6.23	6.33	
B2	1.04	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
B12	3.60	3.70	3.80	
B13	2.80	2.90	3.00	
B14	6.20	-	-	
B15	-	-	6.20	
B16	5.80	5.90	6.00	
B17	0.20	0.30	0.40	
B18	7.80	8.90	8.90	
B19	8.70	8.80	8.90	
B20	-	3.20	-	REF
B21	1.90	2.00	2.10	
B22	0.00	-	-	
B23	0.10	-	-	

Notes:

1. DIMENSIONING and TOLERANCING per ASME Y14.5M-1994.
2. Dimensions are in millimeters.
3. COPLANARITY is additive to C1 MAX thickness.
4. All edges shall not be sharp as tested per UL1439 "Test for Sharpness of Edges on Equipment."
5. Refer to Appendix E about test method of warpage.
6. As measurement point is changed, symbol B1 is changed to symbol B1'.
7. C4 and C5 are added from Version 4.00.

C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
C4	0.80	-	1.10	
C5	0.15	-	-	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.60	0.80	0.90	
R6	0.60	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20	⚠4	-	0.15	
α	133°	135°	137°	
aaa	-	-	0.10	

WARNING: This product may contain chemicals known to the State of California to cause cancer, birth defects, or other reproductive harm. For more information go to www.p65warnings.ca.gov.

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